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(54) **Circuit and method for driving source lines in a liquid crystal display**

Einrichtung und Verfahren zur Steuerung von Source-Leitungen in einer Flüssigkristallanzeige

Dispositif et méthode de commande de lignes de source dans un dispositif d'affichage à cristaux liquides

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(56) References cited:
EP-A- 0 755 044
EP-A- 0 895 220
EP-A1- 0 747 748
WO-A-99/12072
JP-A- H10 153 986
US-A- 5 282 234
US-A- 5 414 443
US-A- 5 528 256
US-A- 5 926 158

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Description

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to a liquid crystal display, in more particular, to a circuit and a method for driving the source lines of a liquid crystal display, which reduces the consumption power thereof.

Discussion of Related Art

[0002] A liquid crystal display (LCD) draws growing attentions as a display device for displaying video signals and studies and researches for this device are being actively carried out. In general, the LCD is roughly divided into a liquid crystal panel part and a driving part. The liquid crystal panel includes a lower glass plate on which pixel electrodes and thin film transistors (TFTs) are arranged in matrix form, a upper glass plate on which a common electrode and a color filter layer are formed, and a liquid crystal layer filled between the upper and the lower glass plates.

[0003] The driving part includes a video signal processor for processing video signals externally inputted, a controller for receiving a composite synchronous signal outputted from the video signal processor, dividing it into horizontal and vertical synchronous signals and controlling timing in response to mode (NTSC, PAL or SECAM) selecting signal, a source driver for supplying a signal voltage to the source lines of the liquid crystal panel in response to the output signal of the controller, and a gate driver for sequentially applying driving voltages to the scanning lines of the liquid crystal panel in response to the output signal of the controller. There have been actively performed researches for reducing the consumption power of the liquid crystal display constructed as above.

[0004] A conventional circuit and method for driving the source of a LCD is explained with reference to the attached drawings.

[0005] FIG. 1 shows the configuration of a conventional TFT-LCD. Referring to FIG. 1, the TFT-LCD includes a liquid crystal panel 10 having pixels each of which is located at each of points where a plurality of gate lines GL and a plurality of source lines SL intersect each other, a source driver 20 for providing each pixel with a video signal through the source lines SL, and a gate driver 30 for selecting a certain gate line GL of the liquid crystal panel 10 to turn on plural pixels. Here, each pixel consists of a TFT 1 whose gate is connected to the gate line GL and whose drain is connected to the source line SL, a storage capacitor Cs connected to the source of the TFT 1 in parallel, and a liquid crystal capacitor Clc.

[0006] FIG. 2 shows the configuration of the source driver of the conventional TFT-LCD. In this drawing, a 384-channel 6-bit driver is illustrated as an example of the source driver. That is, each of R, G, and B data is 6-bit and the number of the column lines is equal to 384. Referring to FIG. 2, the source driver includes a shift register 21, a sampling latch 22, a holding latch 23, a digital/analog converter 24, and an output buffer 25.

[0007] The shift register 21 shifts the horizontal synchronous signal pulse HSYNC in response to a source pulse clock HCLK, to output a latch enable clock to the sampling latch 22. The sampling latch 22 samples and latches digital R, G, and B data by column lines in response to the latch enable clock outputted from the shift register 21. The holding latch 23 simultaneously receives the R, G, and B data latched by the sampling latch 22 in response to a load signal LD to latch the R, G, and B data. The digital/analog converter 24 converts the digital R, G, and B data stored in the holding latch 23 into analog R, G, and B data. Then, the output buffer 25 amplifies signal current corresponding to the R, G, and B data to output it to the source line of the liquid crystal panel.

[0008] The source driver constructed as above samples and holds the digital R, G, and B data during one horizontal period, converts it into the analog R, G, and B data, and current-amplifies it. Here, when the holding latch 23 holds R, G, and B data corresponding to the nth column line, the sampling latch 22 samples R, G, and B data corresponding to the (n+1)th column line.

[0009] FIG. 3 shows the gate driver of the conventional TFT-LCD. Referring to FIG. 3, the gate driver includes a shift register 31, a level shifter, and an output buffer 33. The shift register 31 shifts the vertical synchronous signal pulse VSYNC in response to a gate pulse VCLK, to sequentially enable the scanning lines. The level shifter 32 sequentially level-shifts a signal applied to the scanning lines to output it to the output buffer 33. By doing so, the plural scanning lines connected to the output buffer 33 are sequentially enabled.

[0010] A method for driving the conventional TFT-LCD constructed as above is explained below.

[0011] First of all, the sampling latch 22 of the source driver 20 sequentially receives video data corresponding to a single pixel and stores video data corresponding to the source lines SL. The gate driver 30 outputs a gate line selection signal GLSS to select one of the plural gate lines GL. Then, the TFT 1 connected to the selected gate line GL is turned on so as to apply the video data stored in the holding latch 23 to the drain thereof, thereby displaying the video data on the liquid crystal panel 10.

[0012] Subsequently, the above-described operation is repeated to display video data on the liquid crystal panel 10.

[0013] At this time, the source driver 20 provides VCOM, positive and negative video signals to the liquid crystal panel 10 to display the video data thereon.

[0014] FIG. 4 shows the voltage range of the video signals of FIG. 1. Referring to FIG. 4, the positive and the negative video signals are alternately supplied to the pixels every time frame is changed, in order not to directly apply DC voltage to the liquid crystal during operation of the TFT-LCD and, for this, the electrode of the TFT-LCD upper plate is provided with the VCOM that is the medium voltage between the positive and negative video signals. In case where the positive and negative video signals are alternately applied to the pixels on the bases of the VCOM, however, light transmission curves of the liquid crystal do not agree with each other, generating flicker.

[0015] Accordingly, for the purpose of reducing the generation of flicker, four inversion modes are employed as shown in FIGS. 5A, 5B, 5C and 5D. They are frame inversion, line inversion, column inversion and dot inversion modes.

[0016] FIG. 5A shows the frame inversion mode in which the polarity of a video signal is modulated only when the frame is changed, and FIG. 5B shows the line inversion mode in which the video signal polarity varies every time the gate line GL is changed. Furthermore, the FIG. 5C shows the column inversion mode in which the video signal polarity varies when the source line and the frame are changed, and FIG. 5D shows the dot inversion in which the polarity changes whenever each source line SL and gate line GL are changed and the frame is changed. The picture quality is good in the order of the frame inversion, line inversion, column inversion, and dot inversion, and the number of times of polarity change becomes larger in proportion to the picture quality, to result in the increases in power consumption. This is explained below in detail with reference to the dot inversion mode for driving the conventional LCD shown in FIG. 6. FIG. 6 shows the waveform of a video signal applied to odd-numbered source lines SL or even-numbered source lines SL of the liquid crystal panel 10. This illustrates that the polarity of the video signal of the source lines SL is modulated at every gate line change on the basis of the VCOM.

[0017] Here, it is assumed that the entire TFT-LCD panel displays the same gray color, the variation width (V) of the video signal of the source lines SL becomes twice that of the VCOM plus positive video signal or that of the VCOM plus negative video signal. Accordingly, the conventional dot inversion consumes a large amount of power because the polarity of the video signal changes from positive to negative or from negative to positive on the basis of the VCOM at every time when the gate line GL is changed.

[0018] FIG. 6 shows the video signal swing width when a black image is displayed using the normally-white mode liquid crystal. In this case, every horizontal period requires a voltage swing with a wide width, this voltage swing being obtained by energy provided by the voltage power VDD of the output amplifier, and power consumption occurs at every two horizontal periods (period : H).

[0019] FIG. 7 is a circuit diagram of a general CMOS for driving a capacitance load. Referring to FIG. 7, the source of a PMOS transistor P1 is connected to a power supply V_H and its drain is connected to the drain of an NMOS transistor N1 to construct an output side, the source of the NMOS transistor N1 is connected to other power supply V_L, the gates of the NMOS and the PMOS transistors N1 and P1 receive an output signal (or input signal) frequency F, and a load capacitor C_{LOAD} is connected between the drains of the NMOS and the PMOS transistors N1 and P1 and the source of the NMOS transistor N1.

[0020] The consumption power of the conventional CMOS driving circuit constructed as above is represented by the following equation (1).

$$P_{CONV} = C_{LOAD} \cdot V_H \cdot (V_H - V_L) \cdot F \quad \text{--------- (1)}$$

where C_{LOAD} indicates the capacitance of the load capacitor C_{LOAD}, and F indicates the output signal (or input signal) frequency, and $V_H > V_L$.

[0021] However, in the conventional method of driving the source of the LCD, a large amount of power consumption occurs at every two horizontal periods because the amount of power consumed for driving the source is proportional to the swing width of the video signal, requiring a large amount of consumption power.

[0022] JP10-153986 describes a liquid crystal display.

[0023] EP0747748 describes a liquid crystal driving device, liquid crystal display device, analog buffer, and liquid crystal driving method.

SUMMARY OF THE INVENTION

[0024] Accordingly, the present invention is directed to a circuit and a method for driving the source lines of a liquid crystal display that substantially obviates one or more of the problems due to limitations and disadvantages of the related art.

[0025] An object of the present invention is to provide a circuit and a method for driving the source lines of a liquid

crystal display, which reduces consumption power required for polarity conversion accompanying a voltage swing with a wide width and, at the same time, decreases the driving consumption power of an amplifier.

[0026] According to an embodiment of the present invention there is provided a source driving ciruit for driving the source lines of a liquid crystal display as recited in claim 1. According to a second aspect of the present invention there is provided a source driving method as recited in claim 10. Preferred features of aspects of the present invention are recited in the dependent claims.

[0027] There is also provided a source driving method in a liquid crystal display, which applies negative and positive video signals to source lines of the liquid crystal display including a first and a second plates and a liquid crystal being inserted therebetween, in which each video signal is applied, with its voltage being divided two phases of polarity modulation and gray scale decision.

[0028] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE ATTACHED DRAWINGS

[0029] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention:

[0030] In the drawings:

FIG. 1 shows the configuration of a conventional TFT-LCD;
FIG. 2 shows the configuration of a source driving circuit of the conventional TFT-LCD;
FIG. 3 shows the configuration of a gate driving circuit of the conventional TFT-LCD;
FIG. 4 shows the voltage range of the video signal of FIG. 1;
FIGS. 5A, 5B, 5C and 5D show inversion modes of TFT-LCD;
FIG. 6 shows the output waveform of the conventional source driving circuit according to the dot inversion method;
FIG. 7 is a circuit diagram of a general CMOS for driving a capacitance load;
FIG. 8 shows the output waveform of a source driving circuit according to the dot inversion method;
FIG. 9A shows the waveform of a driving signal of an all-black image in the stepwise source driving method;
FIG. 9B shows the waveform of a driving signal of an all-white image in the stepwise source driving method;
FIGS. 10A, 10B, and 10C show the configuration of a source driving circuit of a TFT-LCD according to the present invention;
FIGS. 11A and 11B show waveforms of control signals for controlling the MUX_A and MUX_B or switches of FIGS. 10A, 10B, and 10C;
FIGS. 12A and 12B are circuit diagrams of amplifiers of the output buffer of FIGS. 10B and 10C;
FIG. 13 is a circuit diagram of a polarity modulator;
FIG. 14 shows an example of the polarity modulating circuit for driving the source driving circuit according to the present invention;
FIG. 15 shows another example of the polarity modulating circuit for driving the source driving circuit according to the present invention;
FIG. 16 shows a 30-inch UXGA panel;
FIG. 17 shows a load model being divided into ten segments;
FIG. 18 shows a driving signal waveform and a control signal waveform for displaying an all-black image; and
FIG. 19 shows a driving signal waveform and a control signal waveform for displaying an all-white image.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENT

[0031] Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

[0032] FIG. 8 illustrates the operating range of a video signal according to the dot inversion mode.

[0033] In the stepwise source driving method as a source driving method for a TFT-LCD according to the present invention, the transmission of a video signal is performed, being divided into 2-phase of polarity modulation and gray scale decision. Referring to FIG.8, a voltage swing B ranging between a voltage VL corresponding to the medium gray of the negative video signal and a voltage VH corresponding to the medium gray of the positive video signal is executed according to the polarity modulation, and then voltage swings C and D for deciding gray scale are accomplished by an amplifier of a source driver. Here, the voltages VL and VH are not needed to be limited to the medium voltages of the negative and the positive video signals, and they can be arbitrary voltages within the negative and the positive video signals.

[0034] The power consumption according to the dot inversion driving method of the present invention is described below, being divided into the one due to the polarity modulation and the other one due to the gray scale decision. Referring to FIG. 8, the consumption power due to the polarity modulation B is provided by the polarity modulation voltage VH while the consumption power required for the gray scale display C (black image in this case) is provided by the power supply VDD of the amplifier. Furthermore, to display a white image after polarity modulation into the voltage VL within the negative video region needs the voltage swing D which is also provided by the power supply VDD of the amplifier. However, when a black image is displayed after polarity modulation into the voltage VL within the negative video region, power consumption caused by the amplifier does not occur but power consumption due to the polarity modulation voltage VL generates when there is executed the polarity modulation back into the voltage VH within the positive video region. This is arranged in the following table 1.

Table 1

Voltage swing	A	B	C	D
Power supply	Polarity modulation VL	Polarity modulation VH	Amplifier	Amplifier

[0035] The table 1 shows the occurrence of power consumption according to the dot inversion driving method of the present invention.

[0036] FIGS. 9A and 9B illustrate driving signal waveforms of a stepwise source driving circuit of the present invention, exemplifying case of an all-black image and case of an all-white image, respectively. That is, FIG. 9A shows the driving signal waveform of the all-black image in the stepwise source driving method, and FIG. 9B shows the driving signal waveform of the all-white image in the stepwise source driving method.

[0037] Referring to FIGS. 9A and 9B, a dot inversion method implemented by the source driving circuit of the present invention drives the source lines with one horizontal period H being divided into two phases of polarity modulation and gray scale decision. In this stepwise source driving method, the polarity modulation with a wide voltage swing width reduces the consumption power using charge recovery through stepwise charging and allows the amplifier to supply only the consumption power required for gray scale display, to thereby decrease the driving consumption power.

[0038] There will be described the configuration of the source driving circuit of the TFT-LCD, capable of reducing the consumption power, according to the present invention.

[0039] FIGS. 10A, 10B, and 10C show the configuration of the source driving circuit of the TFT-LCD according to the present invention. Referring to FIG. 10A, a plurality of multiplexers (MUXs) 80 or switches 81 select one of the output signal of an output buffer 50 and the output signals of an odd-numbered polarity modulator 60 and an even-numbered polarity modulator 70 in response to an external control signal CON, and transmit the selected one to the pixels.

[0040] In the dot inversion of the TFT-LCD, since the signal polarities of neighboring source lines are opposite to each other, the stepwise charge driving directions in the source lines are also opposite to each other. That is, in case where stepwise charging is carried out in an odd-numbered source line capacitor, stepwise discharging should be performed in an even-numbered source line capacitor. Also, switches constructing the polarity modulator operate in opposite orders to each other. Accordingly, the source driving circuit of the present invention has the odd-numbered polarity modulator 60 and the even-numbered polarity modulator, separately set from each other, to separately drive the odd-numbered source lines and the even-numbered source lines.

[0041] The source driving circuit of the TFT-LCD according to the present invention includes the output buffer 50 for amplifying the current of the analog data signal converted by the digital/analog converter 24 of FIG. 2 and outputting it to the source lines of the panel, the odd-numbered polarity modulator 60 for driving the odd-numbered source lines, the even-numbered polarity modulator 70 for driving the even-numbered source lines, and the plurality of MUXs 80 or switches 81 for selecting one of the output signal of the output buffer 50 and the output signals of the odd-numbered and the even-numbered polarity modulators 60 and 70 in response to the external control signal CON and outputting it to the pixels.

[0042] That is, the source driving circuit of the TFT-LCD according to the present invention has the same configuration as the source driving circuit of the conventional TFT-LCD, excepting the section following the output buffer, i.e., the odd-numbered and the even-numbered polarity modulators 60 and 70 and the MUXs 80 or switches 81. The MUXs 80 determine the polarity modulation and the gray scale decision according to the external control signal CON.

[0043] Referring to FIG. 10B, there are provided a first multiplexing part MUX_A 80a receiving the output signals of the output buffer 50 consisting of amplifiers AMP_H and AMP_L for amplifying the current of the analog data signal converted by the digital/analog converter 24 of FIG. 2 and selecting one of the output signals in response to an external control signal EO to output the selected one to the pixels, and a second multiplexing part MUX_B 80b receiving the output signals of the first multiplexing part 80a and the odd-numbered and the even-numbered polarity modulators 60 and 70 and selecting one of them in response to the external control signal CON to output the selected one to the pixels.

[0044] And, FIG.10C is the more simple circuit than that of FIGS. 10A and 10B. Instead of the plurality of the first multiplexing part MUX_A 80a and the second multiplexing part MUX_B 80b for each column, three switches 81 may be used as shown in FIG. 10C. The PMO and PME shown in FIG. 10C mean the Polarity Modulator for Odd-numbered Columns and Polarity Modulator for Even-numbered Columns, respectively.

[0045] FIG. 11A shows the waveforms of the control signals for controlling the MUX_B and MUX_A of FIGS. 10A and 10B, and FIG.11B shows the waveforms of the control signals for controlling the switches of FIG. 10C, and FIGS. 12A and 12B are circuit diagrams of the amplifiers of the output buffer of FIGS. 10B and 10C. Referring to FIG. 11A, the polarity modulation is carried out when the control signal CON is in "1" state and the gray scale decision is performed when the control signal CON is in "0" state. Here, the control signal CON controls the MUX_B of FIGS. 10A and 10B while the control signal EO controls the MUX_A of FIG. 10A.

[0046] The circuit shown in FIG. 10C is operated by the control signals shown FIG. 11B. In the operation of the circuit, the polarity modulation is carried out when the control signal CON is in "1" state (CON=1) and the gray scale decision is performed when the control signal CON is in "0" state (CON=0). In the gray scale decision, the decision of displaying the positive or negative video signal depends on when EO1=1 or EO2=1.

[0047] The amplifier of the output buffer 50 includes two kinds of AMP_H and AMP_L which have different power voltages VDD from each other as shown in FIGS. 12A and 12B. That is, the AMP_H (VDD=10V) is for only the gray scale of the positive video region and the AMP_L (VDD=5V) is for only that of the negative video region.

[0048] Furthermore, it is possible to use a low-voltage amplifier when the negative video signal is transmitted as shown as D of FIG. 6, to reduce the consumption power compared to the case where only a high-voltage amplifier is employed. The configuration of the odd-numbered and the even-numbered polarity modulators is explained in more detail below.

[0049] FIG. 13 is a circuit diagram of each polarity modulator. Referring to FIG. 13, when a load capacitor C_{LOAD} is driven by stepwise voltages obtained by dividing the voltage ranging from the V_L to V_H by 5 (generally, N), the consumption power $P_{STEPWISE}$ decreases to 1/5 (generally, 1/N) of the consumption power represented by the equation (1). This is shown in the following equation (2).

$$P_{STEPWISE} = C_{LOAD}\, V_H\, F(V_H - V_L)/5 = P_{CONV}/5 \quad \text{----------(2)}$$

[0050] Here, the load capacitance C_{LOAD} is the sum of the capacitances of M column lines, where M corresponds to 1/2 of the number of outputs of a single source driver.

[0051] In the source driving method of the present invention, the polarity modulating circuit PM is required to perform polarity modulation of the even-numbered columns and polarity modulation of the odd-numbered columns opposite to each other for the dot inversion driving so that a single source driving circuit should be in charge of the even-numbered and the odd-numbered columns, dividing them from each other. Thus, two polarity modulating circuits PM are required for one source driving circuits. For example, when this method is applied to the source driving circuit of a TFT-LCD having 300 outputs, M becomes 150.

[0052] External capacitors C_{EXT1}, C_{EXT2}, C_{EXT3}, and C_{EXT4} are capacitors which are set outside the source driver chip, the size of each one corresponding to one hundred times that of M load capacitors C_{LOAD}, approximately. These external capacitors C_{EXT1}, C_{EXT2}, C_{EXT3}, and C_{EXT4} are respectively charged with $V_L+(4/5)(V_H-V_L)$, $V_L+(3/5)(V_H-V_L)$, $V_L+(2/5)(V_H-V_L)$, and $V_L+(1/5)(V_H-V_L)$, which are obtained by equally dividing the difference voltage between the V_H and V_L. Here, V_H is higher than V_L. In addition, the V_H, V_L and the external capacitors C_{EXT1}, C_{EXT2}, C_{EXT3} and C_{EXT4} are connected to the load capacitor C_{LOAD} via switches SW6, SW5, SW4, SW3, SW2, and SW1, which are turned on or turned off according to an external signal, respectively.

[0053] Meantime, the stepwise source driving method should provide sufficiently short period of time required for each step and small driving circuit size in addition to reduction effect of the consumption power, to be actually used for driving the source lines of the TFT-LCD.

[0054] There will be explained the reason why the consumption power of the stepwise source driving circuit employing the polarity modulating circuit used as the source driving circuit of the TFT-LCD of the present invention is reduced.

[0055] Referring to FIG. 13, when it is assumed that the external capacitors C_{EXT1}, C_{EXT2}, C_{EXT3}, and C_{EXT4} are initially charged with the voltages, there equally exists the difference of 1/5 between the voltages of neighboring external capacitors. When is assumed that the load capacitor C_{LOAD} is initially charged with the voltage V_L, and it is desired to be charged up to V_H, the switches are sequentially turned on, from SW1 to SW6. In doing so, the voltage thereof increases from V_L to V_H stepwise and the voltage of each step corresponds to the result that corresponding external capacitor has been charged.

[0056] On the contrary, when the load capacitor C_{LOAD} is discharged from V_H to V_L, the switches are sequentially turned on from SW6 to SW1 opposite to the case of charging. Here, $V_L+(1/5)(V_H=V_L)$, provided to the load capacitor

C_{LOAD} while each external capacitors is charged up to V_H, is returned while discharging to V_L so that the power that each external capacitor supplies to the load capacitor C_{LOAD} becomes "0" substantially.

[0057] Furthermore, power supply according to V_H is accomplished by turning on the switch SW6. Here, because the load capacitor C_{LOAD} has been charged with $V_L+(4/5)(V_H-V_L)$ right before the switch SW6 is turned on, the voltage substantially charged by V_H is $1/5(V_H-V_L)$ and the consumption power decreases to 1/5 as shown in the equation (1).

[0058] FIG. 14 is a circuit diagram of an embodiment of the polarity modulating circuit for driving the source driving circuit according to the present invention. Referring to FIG. 14, the odd-numbered polarity modulator 60 and the even-numbered polarity modulator 70 share the external capacitors. Resistors R are for determining the initial charging voltages of the external capacitors. When switches S controlled by a signal STR at the initial operation stage of the source driving circuit is turned on, current flows through the resistors R so that voltage distribution is carried out according to the resistors and each distributed voltage is stored at each external capacitor. Once a desired voltage is stored at each external capacitor, the switches are turned off by the STR signal, to prevent unnecessary current from flowing through the resistors to occur power consumption. Accordingly, the resistors can be integrated inside the source driver chip while the external capacitors are set outside the chip as shown in FIG. 13.

[0059] First and second shift registers 90a and 90b shown in FIG. 14 generate a signal for controlling the switches SW1-SW6 of the stepwise source driving circuit. The signal controlling each switch is internally generated inside the source driver chip using these first and second shift registers 90a and 90b rather than it is externally provided from the outside of the chip so that the number of input signals can be reduced. In FIG. 14, CLK2 is a clock signal used for the first and the second shift registers 90a and 90b, PMS is a trigger signal of the first and the second shift registers 90a and 90b and PMD is a signal determining shift direction.

[0060] When the PMD signal of "1" is applied to the first shift register 90a, the second shift register 90b is provided with "0". This can be accomplished in such a manner that an inverter 100 is set before the first or the second shift registers 90a or 90b to apply the signals opposite to each other to the shift registers. This is required because, in the odd-numbered polarity modulator 60 and even-numbered polarity modulator 70, since the order of turning on and turning off the switches of one of them is opposite to that of the other one, the order of the turn-on signal applied to the switches of one of them should be opposite to that of the other one.

[0061] Alternatively, instead of the first and the second shift registers 90a and 90b, only one shift register may be used as shown in FIG. 15. In this case, the connection order of the switched may be arranged oppositely to that of FIG. 14.

[0062] There will be explained below simulation results with respect to the timing of the dot inversion method of the present invention and the size of the circuit used therein.

[0063] For example, the present invention is applied to 30-inch UXGA panel and 14-inch XGA panel. Mostly, the 30-inch UXGA panel is described hereinafter.

[0064] As shown in FIG. 16, since 30-inch LCD panels currently developed operate by four-division driving, the present invention performs simulations on the assumption that the 30-inch UXGA panel also operates by the four-division driving. In case of the four-division driving, each of the four divided panels corresponds to a 15-inch SVGA panel. Here, the column lines operate with the load of C=128pF and R=2.5kΩ and the line time is equal to 22μsec. The values C and R are obtained through Raphael 3D simulation for typical pixels. A load model divided into 10 segments as shown in FIG. 17 is used because C and R are dispersed in the actual source lines.

[0065] Let it be assumed that the 5-step method as shown in FIG. 13 is used, the period of time required for the polarity modulation is limited below 1/2 of one horizontal period 1H and the remaining period of time is allocated to the period of time required for the gray scale display according to the amplifier, the XGA panel has the line time of 16¥isec approximately and the SVGA panel has the line time of 22 ¥isec approximately. Thus, the permitted step time periods in the XGA and SVGA panel are respectively 1.5μsec and 2μsec approximately. The transistor sizes of the switches of FIG. 13 for the purpose of satisfying this timing condition are arranged in tables 2, 3, 4, and 5.

[0066] Here, each switch may be configured of only NMOS transistor or configured of NMOS and PMOS transistors, the channel length of each transistor being commonly 0.6μm-. In addition, in the polarity modulation, each switch (NMOS transistor) is provided with 10V and 0V to be turned on and turned off, respectively, because a voltage of 2.25-7.75V should be supplied to the load capacitor C_{LOAD}. On the contrary, in case of the switch configured of a PMOS transistor, it is provided with 0V and 10V to be turned on and turned off, respectively, which is opposite to the above case.

Table 2. The sizes of transistors when the step time is 1.5μsec and each switch is configured of an NMOS transistor

Switch	SW1	SW2	SW3	SW4	SW5	SW6
Size (μm)	400	400	400	500	500	600

[0067] As shown in table 2, each of the switches is configured of only NMOS transistor, with SW1, SW2, and SW3 having the size of 400μm, SW4 and SW5 having the size of 500μm, and SW6 transmitting the highest voltage having

the size of 600μm.

[0068] The following table 3 shows the sizes of the transistors when the switch SW6 transmitting the highest voltage is configured of a PMOS. Since the switch SW6 should transmit the highest voltage, it is desirable that 0V is applied as the turn-on signal to increase the value of $|V_{GS}|$.

Table 3 The sizes of transistors when the step time is 1.5μsec and the switches are configured of NMOS and PMOS transistors

Switch	SW1	SW2	SW3	SW4	SW5	SW6
Type	N	N	N	N	N	P
Size (μm)	400	400	400	500	500	600

[0069] As shown in table 3, it is advantageous in terms of the transistor size that the switch SW6 is configured of the PMOS transistor rather than the NMOS transistor.

Table 4 The sizes of transistors when the step time is 2.0μsec and each switch is configured of an NMOS transistor

Switch	SW1	SW2	SW3	SW4	SW5	SW6
Size (μm)	100	100	100	200	200	300

Table 5 The sizes of transistors when the step time is 2.0μsec and the switches are configured of NMOS and PMOS transistors

Switch	SW1	SW2	SW3	SW4	SW5	SW6
Type	N	N	N	N	N	P
Size (μm)	100	100	100	200	200	250

[0070] There will be arranged in the following tables the result of power consumption simulation according to the above-described source driving circuit of the LCD according to the present invention. The conditions for the power consumption simulation is shown in Table 6.

Table 6 Conditions for power consumption simulation

Diagonal length	Resolution	Frame frequency	Load	Remarks
30 inches	UXGA	75	C=255pF R=5kΩ	four-division driving

[0071] Here, the result of AC power consumption simulation in the stepwise source driving method is compared with the result of AC power consumption simulation in the conventional high-voltage driving method. FIG. 18 shows driving waveforms and control signals when the panel displays an all-black image, and FIG. 19 shows driving waveforms and control signals when the panel displays an all-white image. FIGS. 18 and 19 show the results obtained by performing HSPICE simulation under the conditions of the table 6. That is, the polarity modulation or gray scale decision are carried out according to the control signal CON.

[0072] Meanwhile, current values and consumption powers are arranged in the following tables 7, 8, and 9. Here, VDDH and VDDL of Table 7 correspond to the power voltages of AMP_H and AMP_L shown in FIGS. 12A and 12B, respectively.

Table 7 Comparison of consumption powers for displaying all-black image

	Stepwise source driving				Conventional high-voltage driving
Power	VDDH	VDDL	VH	VL	VDD
Voltage (V)	10	5	7.75	2.25	10

(continued)

	Stepwise source driving				Conventional high-voltage driving
Power	VDDH	VDDL	VH	VL	VDD
Average AC current value (μA)	3.8	0	3.2	3.6	23.1
AC consumption power (mW)	91.2	0	59.5	19.4	554.4
AC consumption power (mW) of each of 4 divided panels	170.1				554.4
AC consumption power (mW) of entire panel	680.4				2218

Table 8 Comparison of consumption powers for displaying all-white image 1

	Stepwise source driving				Conventional high-voltage driving
Power	VDDH	VDDL	VH	VL	VDD
Voltage (V)	10	5	7.75	2.25	10
Average AC current value (μA)	0	3.6	6.9	0	8.7
AC consumption power (mW)	0	43.2	128.3	0	208.8
AC consumption power (mW) of each of 4 divided panels	171.5				208.8
AC consumption power (mW) of entire panel	686				835.2

Table 9 Comparison of consumption powers for displaying all-medium gray image

	Stepwise source driving				Conventional high-voltage driving
Power	VDDH	VDDL	VH	VL	VDD
Voltage (V)	10	5	7.75	2.25	10
Average AC current value(μA)	0	0	3.2	0	16.0
AC consumption power (mW)	0	0	59.5	0	384
AC consumption power(mW) of each of 4 divided panels	59.5				384
AC consumption power(mW) of entire panel	238				1536

[0073] According to the stepwise source driving method of the present invention, the consumption power required for the polarity modulation with a wide voltage swing width is reduced using charge recovery through the stepwise charging, and the amplifier supplies only the amount of consumption power required for the gray scale display, to thereby decrease the driving consumption power.

[0074] It will be apparent to those skilled in the art that various modifications and variations can be made in the circuit and method for driving the source of a liquid crystal display of the present invention without departing from the scope of the appended claims. Thus, it is intended that the present invention cover the modifications and the variations of this invention provided they come within the scope of the appended claims.

Claims

1. A source driving circuit for driving the source lines of a liquid crystal display, the source driving circuit having a shift

register, a sampling latch, a holding latch, a digital/analog converter, and an output buffer, the source driving circuit comprising:

a polarity modulator for performing polarity modulation of source lines; and
a plurality of first switches, each being arranged for selecting one of an output signal of the output buffer and output signals of the polarity modulator in response to a control signal, to output the selected one to pixels via a source line,
wherein
the output buffer comprises an amplifier arranged to amplify gray scale signals of a positive video region and an amplifier arranged to amplify gray scale signals of a negative video region, the amplifier arranged to amplify the gray scale signals of the positive video region having a highest supply voltage that is higher than the highest supply voltage of the amplifier arranged to amplify the gray scale signals of the negative video region,
the polarity modulator comprises a first polarity modulator for performing polarity modulation of odd-numbered source lines, a second polarity modulator for performing polarity modulation of even-numbered source lines, opposite to the first polarity modulator, and n external capacitors set outside a source driver chip,
each of the first and second polarity modulators has a respective output terminal for the output signal and comprises a plurality of second switches connecting the n external capacitors to a load capacitance seen by the output terminal,
the polarity modulator further comprises means for controlling the plurality of second switches so as to sequentially connect the external capacitors to the load capacitance, and
the polarity modulator further comprises a plurality of resistors configured for setting the initial charging voltages of the external capacitors, resistors of the plurality of resistors being connected to the external capacitors by a plurality of third switches, the plurality of third switches being configured to be turned off once a desired voltage is stored on each of the external capacitors.

2. A circuit according to claim 1, wherein each of the switches comprises a NMOS transistor.

3. A circuit according to claim 2, wherein the NMOS transistors constructing the switches have different sizes from one another.

4. A circuit according to claim 1, wherein each of the switches is configured using NMOS and PMOS transistors.

5. A circuit according to any preceding claim, wherein the n external capacitors are charged with voltages obtained by equally dividing a voltage value ranging from a predetermined gray value of a negative video signal to a predetermined gray value of a positive video signal.

6. A circuit according to any preceding claim, wherein each of the external capacitor has the size larger than that of the load capacitance.

7. A circuit according to any preceding claim, wherein each of the first and the second polarity modulators includes first and second shift registers, respectively, having shift directions opposite to each other.

8. A circuit according to any of claims 1-6, wherein the plurality of second switches comprises a first plurality of second switches and a second plurality of second switches, and each of the first and the seconde polarity modulators includes a single shift register connected to the first and the second pluralities of second switches such that the shift register causes the switches of the first plurality of second switches to turn on in a first order and the switches of the second plurality of second switches to turn on in a second order opposite to the first order.

9. A circuit according to claim 1, wherein the plurality of first switches is a plurality of multiplexers.

10. A source driving method for driving source lines in a liquid crystal display by means of a source driving circuit as in claim 1, which applies negative and positive video signals to source lines of the liquid crystal display including a first and a second plates and a liquid crystal being inserted therebetween,
wherein each video signal is applied, with its voltage being applied in two phases of polarity modulation and gray scale decision;
the source driving method comprising the step of
amplifying the gray scale signal of the positive video region with the first amplifier and the gray scale signal of the negative video region with the second amplifier,

wherein during the polarity modulation phase a video voltage applied to the source lines is caused to swing between two predetermined voltages, the two predetermined voltages being the gray scale signals of the positive region and the gray scale signal of the negative video region and during the decision phase the video voltage is caused to swing from the predetermined voltage reached during the polarity modulation phase to a voltage corresponding to a desired gray scale level to be displayed, wherein the polarity modulation phase comprises controlling the plurality of second switches so as to sequentially connect the plurality of external capacitors to the load capacitance,
wherein the method comprises controlling the plurality of third switches so as to initially charge the external capacitors to the desired voltages through the resistors and, once a desired voltage is stored at each external capacitor, disconnect the resistors from the external capacitors.

11. A method according to claim 10, wherein the polarity modulation transmits voltage swing ranging between a voltage corresponding to a predetermined gray value of the negative video signal and a voltage corresponding to a predetermined gray value of the positive video signal.

12. A method according to claim 10, wherein the polarity modulation uses charge recovery through stepwise charging.

13. A method according to claim 10 or 12, wherein the amplifiers supply only the amount of consumption power, required during the phase of gray scale decision.

Patentansprüche

1. Source-Ansteuerungsschaltung zur Ansteuerung der Source-Leitungen einer Flüssigkristallanzeige, wobei die Source-Ansteuerungsschaltung ein Schieberegister, einen Abtastspeicher, einen Haltespeicher, einen Digital/Analog-Wandler und einen Ausgabepuffer hat, wobei die Source-Ansteuerungsschaltung umfasst:

einen Polaritätsmodulator zur Durchführung der Polaritätsmodulation von Source-Leitungen; und
eine Vielzahl von ersten Schaltern, die jeweils dafür eingerichtet sind, als Antwort auf ein Steuersignal eines von Folgendem auszuwählen, nämlich ein Ausgangssignal des Ausgabepuffers und Ausgangssignale des Polaritätsmodulators, um das Ausgewählte über eine Source-Leitung an Pixel auszugeben,
wobei
der Ausgabepuffer umfasst: einen Verstärker, der dafür eingerichtet ist, Graustufensignale eines positiven Videobereichs zu verstärken, und einen Verstärker, der dafür eingerichtet ist, Graustufensignale eines negativen Videobereichs zu verstärken, wobei der Verstärker dafür eingerichtet ist, die Graustufensignale des positiven Videobereichs mit einer höchsten Versorgungsspannung zu verstärken, die höher ist als die höchste Versorgungsspannung des Verstärkers, der dafür eingerichtet ist, die Graustufensignale des negativen Videobereichs zu verstärken,
der Polaritätsmodulator umfasst: einen ersten Polaritätsmodulator zur Durchführung der Polaritätsmodulation ungeradzahliger Source-Leitungen, einen zweiten Polaritätsmodulator zur Durchführung der Polaritätsmodulation geradzahliger Source-Leitungen entgegengesetzt zu dem ersten Polaritätsmodulator, und n externe Kondensatoren, die außerhalb eines Source-Treiberchips angeordnet sind,
jeder der ersten und zweiten Polaritätsmodulatoren einen jeweiligen Ausgangsanschluss für das Ausgangssignal hat und eine Vielzahl von zweiten Schaltern umfasst, die die n externen Kondensatoren aus Sicht des Ausgangsanschlusses mit einer Lastkapazität verbinden,
der Polaritätsmodulator ferner ein Mittel zur Steuerung der Vielzahl von zweiten Schaltern umfasst, um die externen Kondensatoren mit der Lastkapazität sequentiell zu verbinden, und
der Polaritätsmodulator ferner eine Vielzahl von Widerständen umfasst, die dafür konfiguriert sind, Anfangsladespannungen der externen Kondensatoren festzulegen, wobei Widerstände aus der Vielzahl von Widerständen mit den externen Kondensatoren durch eine Vielzahl von dritten Schaltern verbunden sind, wobei die Vielzahl von dritten Schaltern dafür konfiguriert ist, ausgeschaltet zu werden, sobald eine gewünschte Spannung in jedem der externen Kondensatoren gespeichert ist.

2. Schaltung nach Anspruch 1, wobei jeder der Schalter einen NMOS-Transistor umfasst.

3. Schaltung nach Anspruch 2, wobei die NMOS-Transistoren, die die Schalter bilden, Größen haben, die sich voneinander unterscheiden.

4. Schaltung nach Anspruch 1, wobei jeder der Schalter unter Verwendung von NMOS- und PMOS-Transistoren

konfiguriert ist.

5. Schaltung nach einem der vorhergehenden Ansprüche, wobei die n externen Kondensatoren mit Spannungen geladen werden, die durch gleichmäßiges Teilen eines Spannungswertes gewonnen werden, der von einem vorbestimmten Grauwert eines negativen Videosignals bis zu einem vorbestimmten Grauwert eines positiven Videosignals reicht.

6. Schaltung nach einem der vorhergehenden Ansprüche, wobei jeder der externen Kondensatoren die Größe hat, die größer ist als die der Lastkapazität.

7. Schaltung nach einem der vorhergehenden Ansprüche, wobei jeder der ersten und der zweiten Polaritätsmodulatoren erste bzw. zweite Schieberegister aufweist, die einander entgegengesetzte Verschiebungsrichtungen haben.

8. Schaltung nach einem der Ansprüche 1 bis 6, wobei die Vielzahl von zweiten Schaltern eine erste Vielzahl von zweiten Schaltern und eine zweite Vielzahl von zweiten Schaltern umfasst und jeder der ersten und zweiten Polaritätsmodulatoren ein einzelnes Schieberegister aufweist, das mit der ersten und der zweiten Vielzahl von zweiten Schaltern verbunden ist, so dass das Schieberegister bewirkt, dass die Schalter der ersten Vielzahl von zweiten Schaltern in einer ersten Reihenfolge einschalten und die Schalter der zweiten Vielzahl von zweiten Schaltern in einer zweiten Reihenfolge entgegengesetzt zur ersten Reihenfolge einschalten.

9. Schaltung nach Anspruch 1, wobei die Vielzahl von ersten Schaltern eine Vielzahl von Multiplexern ist.

10. Source-Ansteuerungsverfahren zur Ansteuerung von Source-Leitungen in einer Flüssigkristallanzeige mittels einer Source-Ansteuerungsschaltung nach Anspruch 1, das positive und negative Videosignale an Source-Leitungen der Flüssigkristallanzeige anlegt, die eine erste und eine zweite Platte und einen zwischen diesen eingefügten Flüssigkristall aufweist,
wobei jedes Videosignal angelegt wird, indem seine Spannung in zwei Phasen, nämlich Polaritätsmodulations- und Graustufenentscheidungsphase angelegt wird;
wobei das Source-Ansteuerungsverfahren den folgenden Schritt umfasst:

Verstärken des Graustufensignals des positiven Videobereichs mit dem ersten Verstärker und des Graustufensignals der negativen Videobereichs mit dem zweiten Verstärker,
wobei während der Polaritätsmodulationsphase bewirkt wird, dass eine Videospannung, die an die Source-Leitungen angelegt wird, sich zwischen zwei vorbestimmten Spannungen bewegt, wobei die beiden vorbestimmten Spannungen die Graustufensignale des positive Bereichs und die Graustufensignal des negativen Videobereichs sind, und während des Entscheidungsphase bewirkt wird, dass die Videospannung sich von der vorbestimmten Spannung, die während der Polaritätsmodulationsphase erreicht wird, zu einer Spannung bewegt, die einem darzustellenden gewünschten Graustufenpegel entspricht, wobei die Polaritätsmodulationsphase umfasst: Steuern der Vielzahl von zweiten Schaltern, um die Vielzahl von externen Kondensatoren für die Lastkapazität sequentiell zu verbinden,
wobei das Verfahren umfasst: Steuern der Vielzahl von dritten Schaltern, um die externen Kondensatoren über die Widerstände anfänglich auf die gewünschten Spannungen zu laden, und sobald eine gewünschte Spannung in jedem externen Kondensator gespeichert ist, die Widerstände von den externen Kondensatoren zu trennen.

11. Verfahren nach Anspruch 10, wobei die Polaritätsmodulation den Spannungshub überträgt, der sich zwischen einer Spannung, die einem vorbestimmten Grauwert des negativen Videosignals entspricht, und einer Spannung bewegt, die einem vorbestimmten Grauwert des positiven Videosignals entspricht.

12. Verfahren nach Anspruch 10, wobei die Polaritätsmodulation Ladungsrückgewinnung durch schrittweises Laden nutzt.

13. Verfahren nach Anspruch 10 oder 12, wobei die Verstärker nur den Verbrauchsleistungsbetrag liefern, der während der Graustufenentscheidungsphase erforderlich ist.

Revendications

1. Circuit de commande de source des lignes de source d'un affichage à cristaux liquides, le circuit de commande de

source présentant un registre à décalage, un verrou d'échantillonnage, un verrou de maintien, un convertisseur numérique/analogique, et une mémoire tampon de sortie, le circuit de commande de source comprenant :

un modulateur de polarité pour réaliser une modulation de polarité de lignes de source ; et
une pluralité de premiers commutateurs, chacun étant agencé pour sélectionner un signal parmi un signal de sortie de la mémoire tampon de sortie et des signaux de sortie du modulateur de polarité en réaction à un signal de commande, pour produire le signal sélectionné vers des pixels par l'intermédiaire d'une ligne de source, dans lequel
la mémoire tampon de sortie comprend un amplificateur agencé pour amplifier des signaux en niveaux de gris d'une région de vidéo positive et un amplificateur agencé pour amplifier des signaux en niveaux de gris d'une région de vidéo négative, l'amplificateur étant agencé pour amplifier les signaux en niveaux de gris de la région de vidéo positive présentant une tension d'alimentation la plus élevée qui est supérieure à la tension d'alimentation la plus élevée de l'amplificateur agencé pour amplifier les signaux en niveaux de gris de la région de vidéo négative,
le modulateur de polarité comprend un premier modulateur de polarité pour réaliser une modulation de polarité de lignes de source impaires, un second modulateur de polarité pour réaliser une modulation de polarité de lignes de source paires, à l'inverse du premier modulateur de polarité, et n condensateurs externes placés à l'extérieur d'une puce de commande de source,
chacun des premier et second modulateurs de polarité présente une borne de sortie respective pour le signal de sortie et comprend une pluralité de deuxièmes commutateurs connectant les n condensateurs externes à une capacité de charge vue par la borne de sortie,
le modulateur de polarité comprend en outre un moyen pour commander la pluralité de deuxièmes commutateurs de manière à connecter de manière séquentielle les condensateurs externes à la capacité de charge, et
le modulateur de polarité comprend en outre une pluralité de résistances configurées pour définir les tensions de chargement initiales des condensateurs externes, les résistances de la pluralité de résistances étant connectées aux condensateurs externes grâce à une pluralité de troisièmes commutateurs, la pluralité de troisièmes commutateurs étant configurés pour être désactivés une fois qu'une tension souhaitée est stockée sur chacun des condensateurs externes.

2. Circuit selon la revendication 1, dans lequel chacun des commutateurs comprend un transistor NMOS.

3. Circuit selon la revendication 2, dans lequel les transistors NMOS constituant les commutateurs présentent des tailles différentes les uns des autres.

4. Circuit selon la revendication 1, dans lequel chacun des commutateurs est configuré en utilisant des transistors NMOS et PMOS.

5. Circuit selon l'une quelconque des revendications précédentes, dans lequel les n condensateurs externes sont chargés avec des tensions obtenues en divisant de manière égale une valeur de tension allant d'une valeur de gris prédéterminée d'un signal de vidéo négative à une valeur de gris prédéterminée d'un signal de vidéo positif.

6. Circuit selon l'une quelconque des revendications précédentes, dans lequel chacun des condensateurs externes présente une taille supérieure à celle de la capacité de charge.

7. Circuit selon l'une quelconque des revendications précédentes, dans lequel chacun des premier et second modulateurs de polarité comprend des premier et second registres à décalage, respectivement, présentant des directions de décalage opposées les unes aux autres.

8. Circuit selon l'une quelconque des revendications 1 à 6, dans lequel la pluralité de deuxièmes commutateurs comprend une première pluralité de deuxièmes commutateurs et une seconde pluralité de deuxièmes commutateurs, et chacun des premier et second modulateurs de polarité comprend un registre à décalage unique connecté aux première et seconde pluralités de deuxièmes commutateurs de sorte que le registre à décalage active les commutateurs de la première pluralité de deuxièmes commutateurs selon un premier ordre et active les commutateurs de la seconde pluralité de deuxièmes commutateurs selon un second ordre opposé au premier ordre.

9. Circuit selon la revendication 1, dans lequel la pluralité de premiers commutateurs est une pluralité de multiplexeurs.

10. Procédé de commande de source permettant de commander des lignes de source dans un affichage à cristaux

liquides au moyen d'un circuit de commande de source selon la revendication 1, qui envoie des signaux vidéo négatifs et positifs à des lignes de source de l'affichage à cristaux liquides comprenant des première et seconde plaques et un cristal liquide inséré entre celles-ci,
dans lequel chaque signal vidéo est envoyé, sa tension s'appliquant en deux phases de modulation de polarité et de décision de niveau de gris ;
le procédé de commande de source comprenant les étapes consistant à
amplifier le signal en niveaux de gris de la région de vidéo positive avec le premier amplificateur et le signal en niveaux de gris de la région de vidéo négative avec le second amplificateur,
dans lequel, pendant la phase de modulation de polarité, une tension vidéo envoyée aux lignes de source est amenée à basculer entre deux tensions prédéterminées, les deux tensions prédéterminées étant les signaux en niveaux de gris de la région positive et le signal en niveaux de gris de la région de vidéo négative et, pendant la phase de décision, la tension de vidéo est amenée à basculer de la tension prédéterminée atteinte pendant la phase de modulation de polarité à une tension correspondant à un niveau de gris souhaité à afficher, la phase de modulation de polarité comprenant une étape consistant à commander la pluralité de deuxièmes commutateurs de manière à connecter de manière séquentielle la pluralité de condensateurs externes à la capacité de charge,
dans lequel le procédé comprend une étape consistant à commander la pluralité de troisièmes commutateurs de manière à charger initialement les condensateurs externes aux tensions souhaitées par l'intermédiaire des résistances et, une fois qu'une tension souhaitée est stockée au niveau de chaque condensateur externe, déconnecter les résistances des condensateurs externes.

11. Procédé selon la revendication 10, dans lequel la modulation de polarité transmet un écart de tension compris entre une tension correspondant à une valeur de gris prédéterminée du signal vidéo négatif et une tension correspondant à une valeur de gris prédéterminée du signal vidéo positif.

12. Procédé selon la revendication 10, dans lequel la modulation de polarité utilise une récupération de charge par l'intermédiaire d'un chargement progressif.

13. Procédé selon la revendication 10 ou 12, dans lequel les amplificateurs ne fournissent que la quantité de puissance de consommation demandée pendant la phase de décision de niveau de gris.

FIG.1

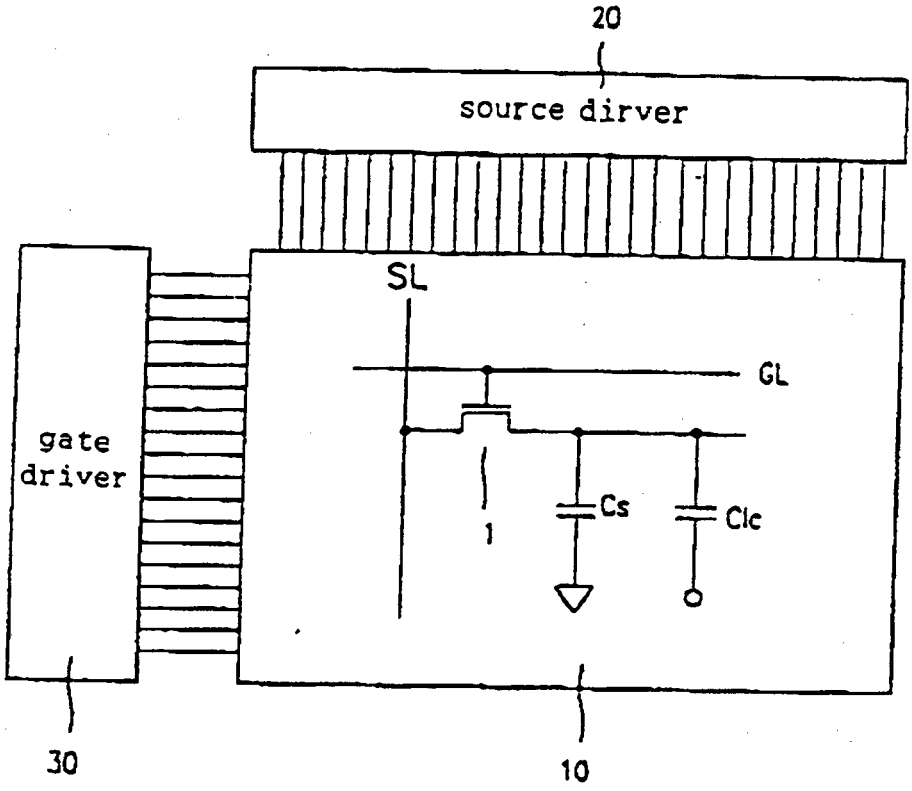


FIG.2

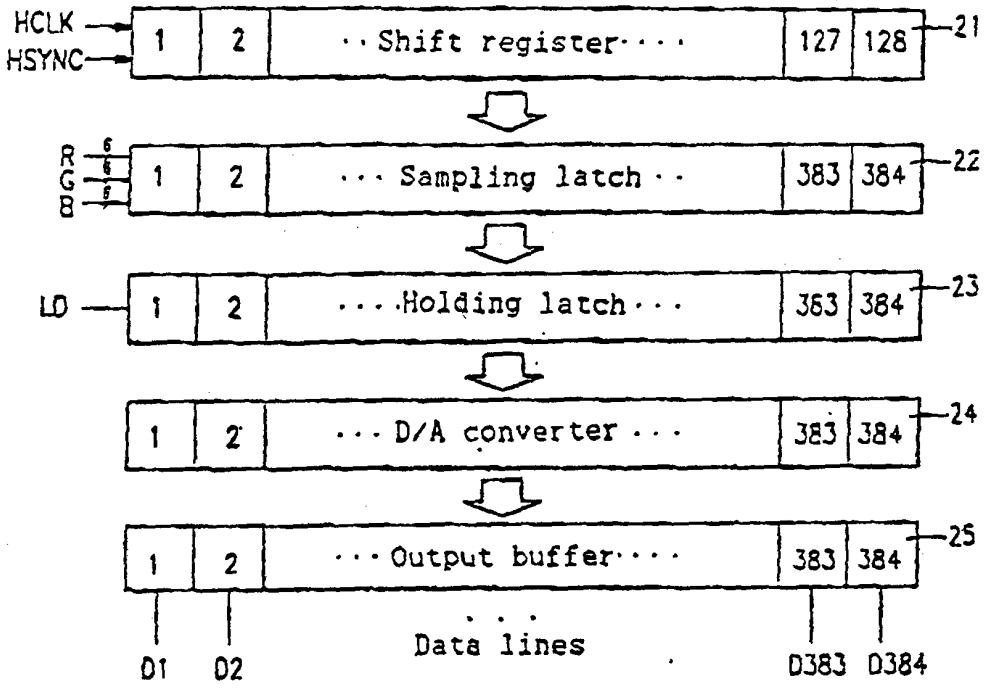

HCLK
HSYNC
1
2
··Shift register····
127
128
21
R
G
B
6
6
6
1
2
···Sampling latch··
383
384
22
LD
1
2
····Holding latch···
383
384
23
1
2
···D/A converter···
383
384
24
1
2
···Output buffer····
383
384
25
D1
D2
Data lines
D383
D384

FIG.3

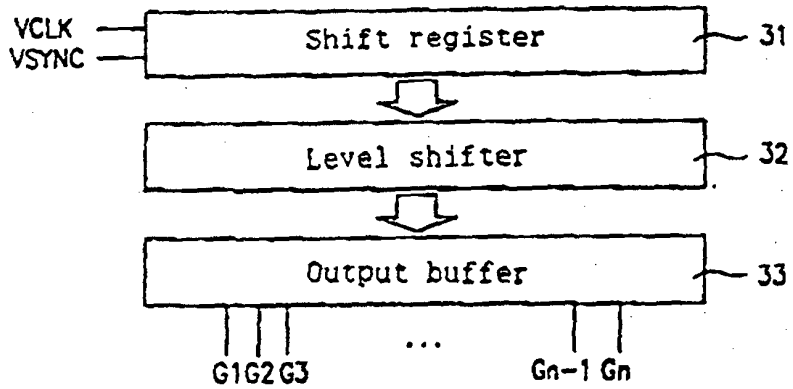

VCLK
VSYNC
Shift register
31
Level shifter
32
Output buffer
33
G1
G2
G3
Gn-1
Gn

FIG. 4

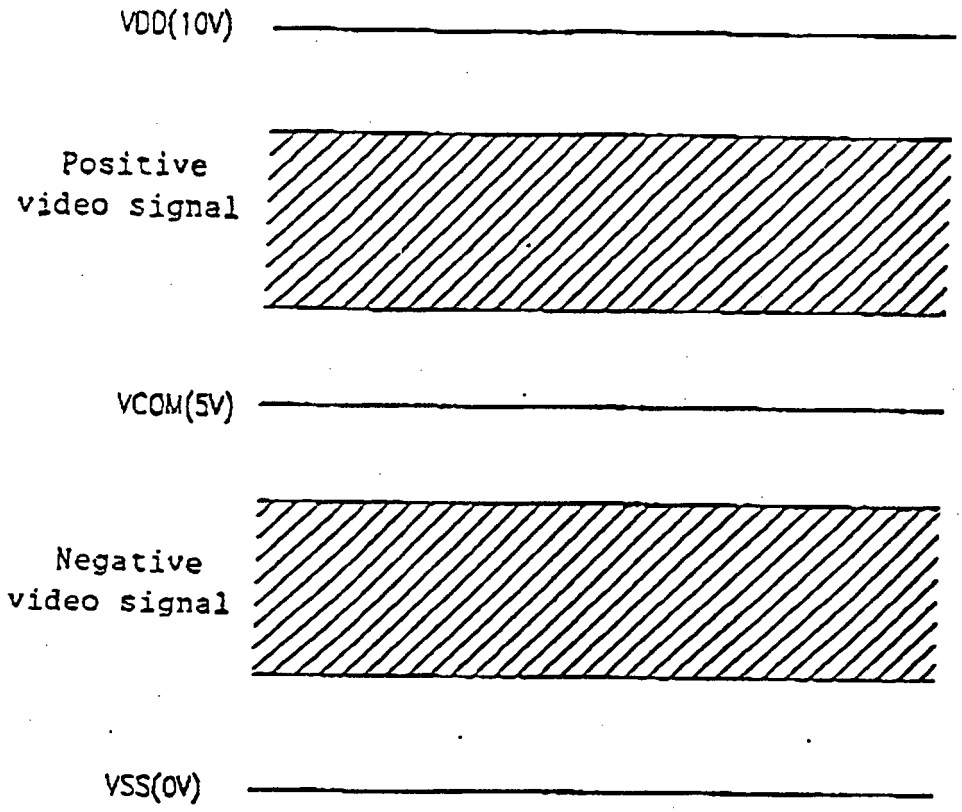

VDD(10V)
Positive video signal
VCOM(5V)
Negative video signal
VSS(0V)

FIG.5A

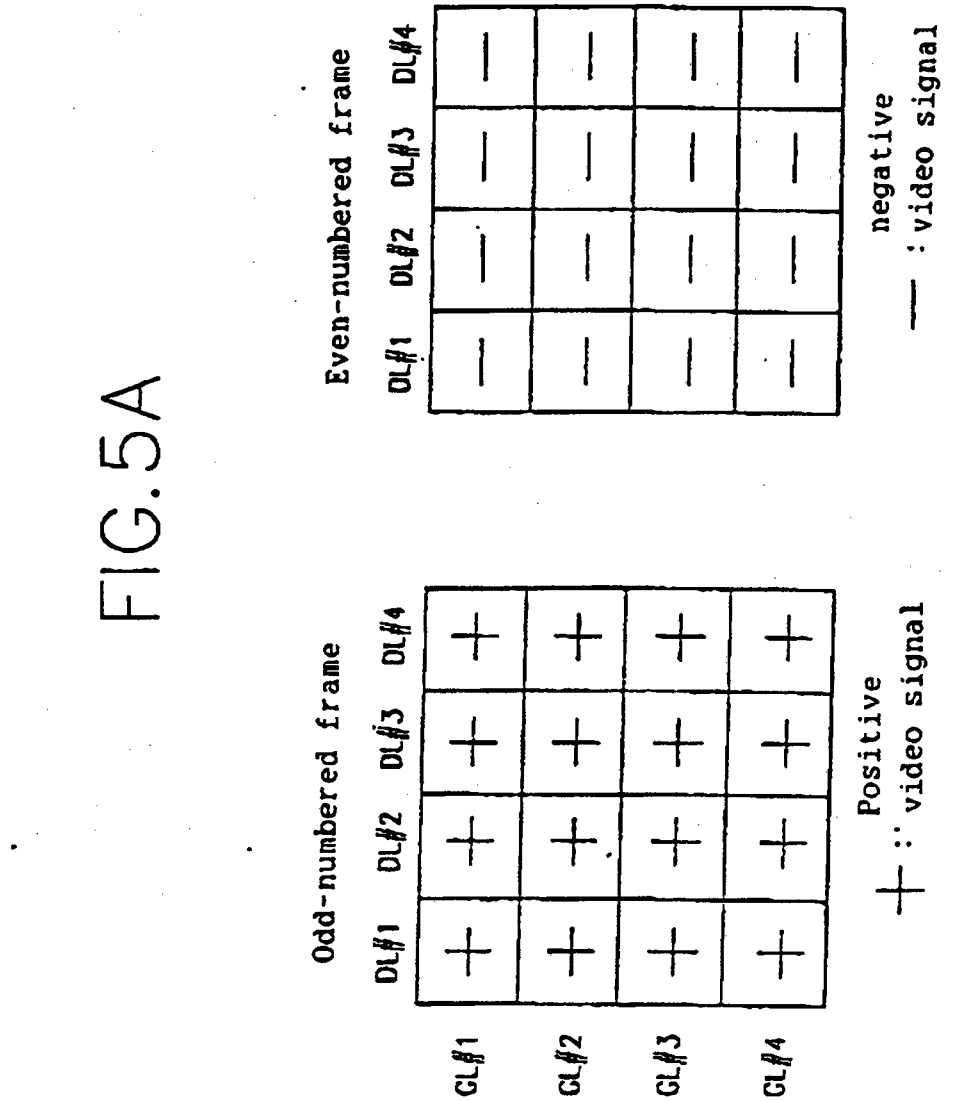

Odd-numbered frame
DL#1
DL#2
DL#3
DL#4
GL#1
GL#2
GL#3
GL#4
Positive
+ : video signal
Even-numbered frame
DL#1
DL#2
DL#3
DL#4
negative
— : video signal

FIG.5B

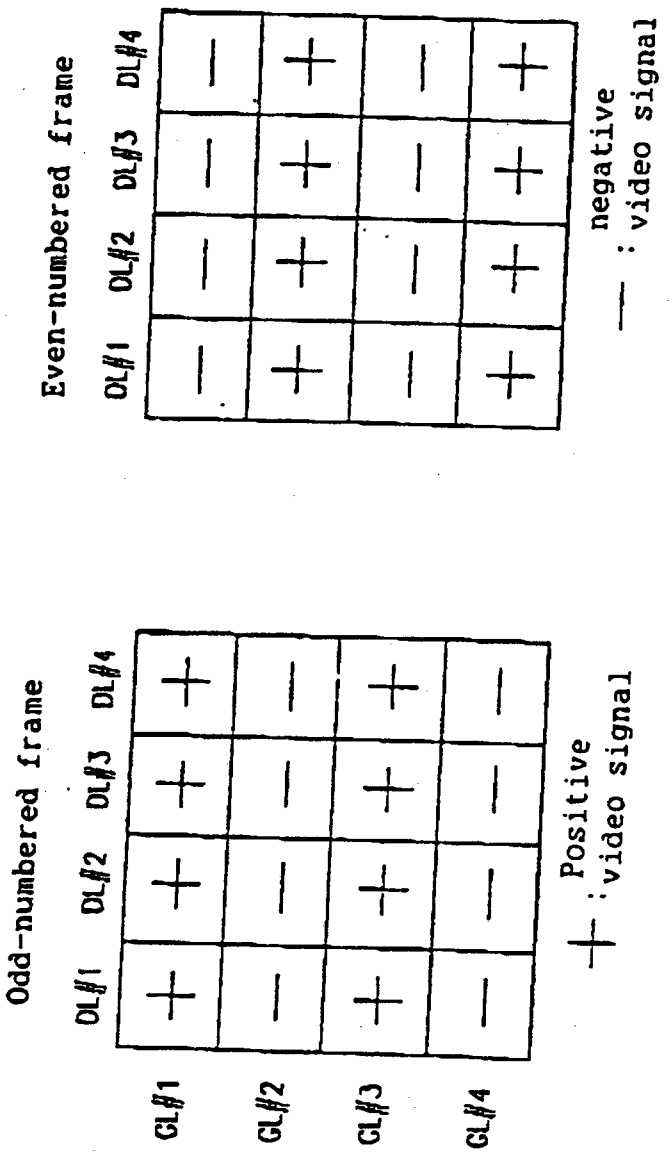

Even-numbered frame
DL#1
DL#2
DL#3
DL#4
Odd-numbered frame
GL#1
GL#2
GL#3
GL#4
+ : Positive video signal
— : negative video signal

FIG.5C

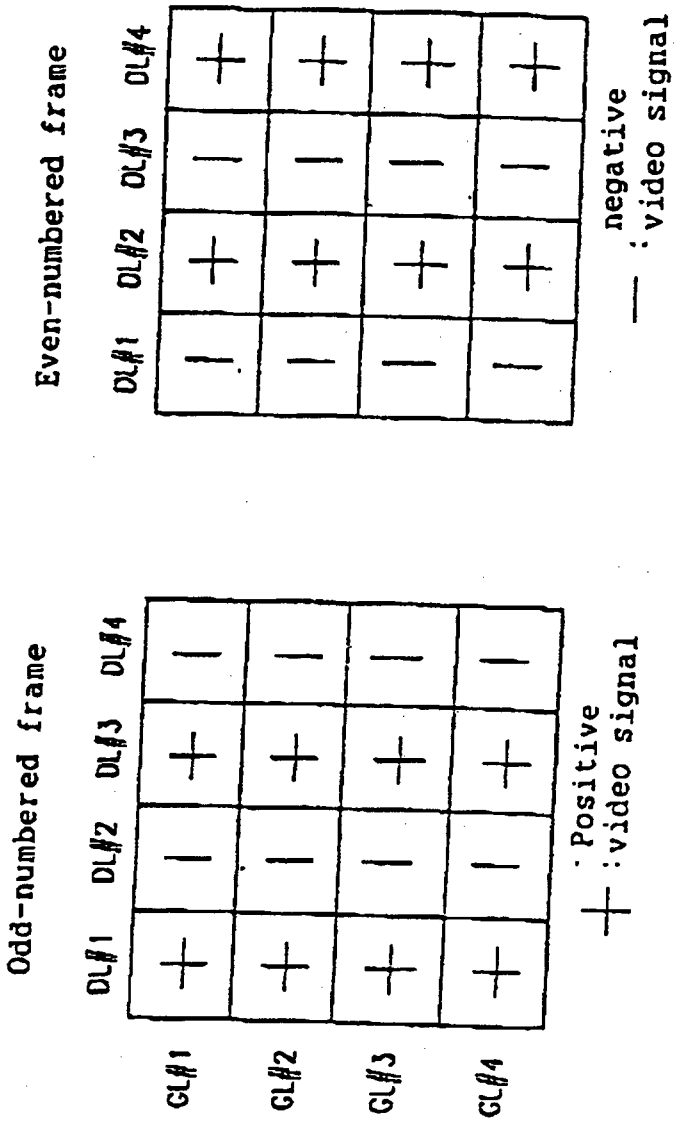

Odd-numbered frame
Even-numbered frame
DL#1
DL#2
DL#3
DL#4
GL#1
GL#2
GL#3
GL#4
+ : Positive video signal
— : negative video signal

FIG.5D

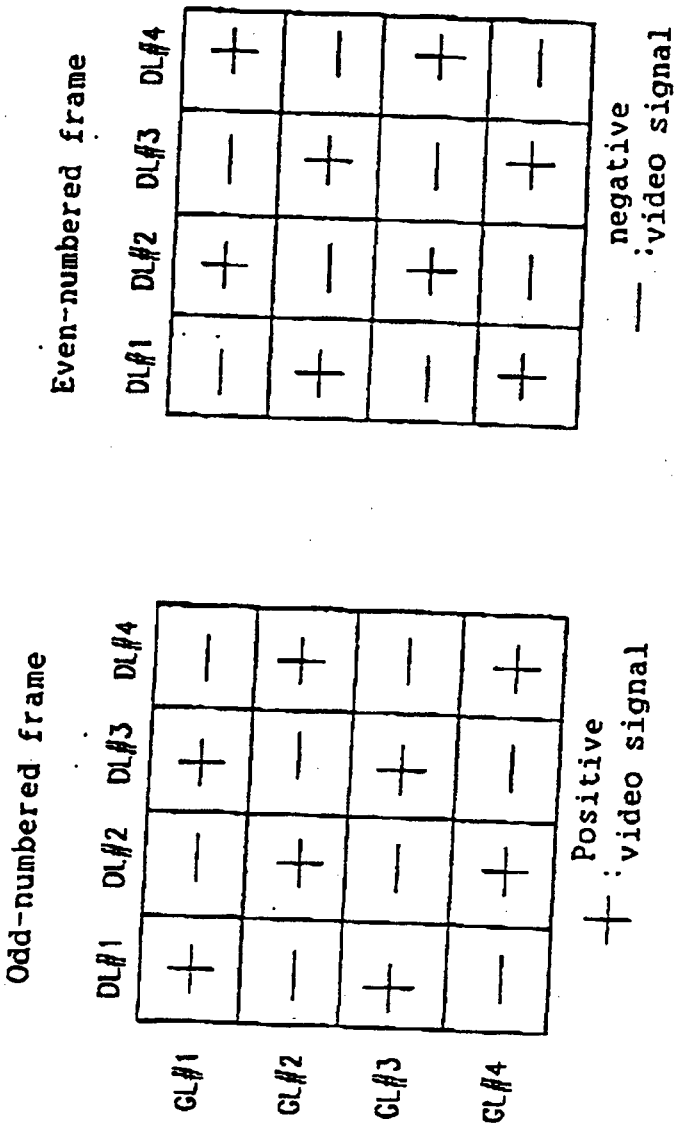

Even-numbered frame
DL#1 DL#2 DL#3 DL#4
GL#1 + − − +
GL#2 − + + −
GL#3 + − − +
GL#4 − + + −
− : negative video signal
Odd-numbered frame
DL#1 DL#2 DL#3 DL#4
GL#1 + − + −
GL#2 − + − +
GL#3 + − + −
GL#4 − + − +
+ : Positive video signal

FIG.6

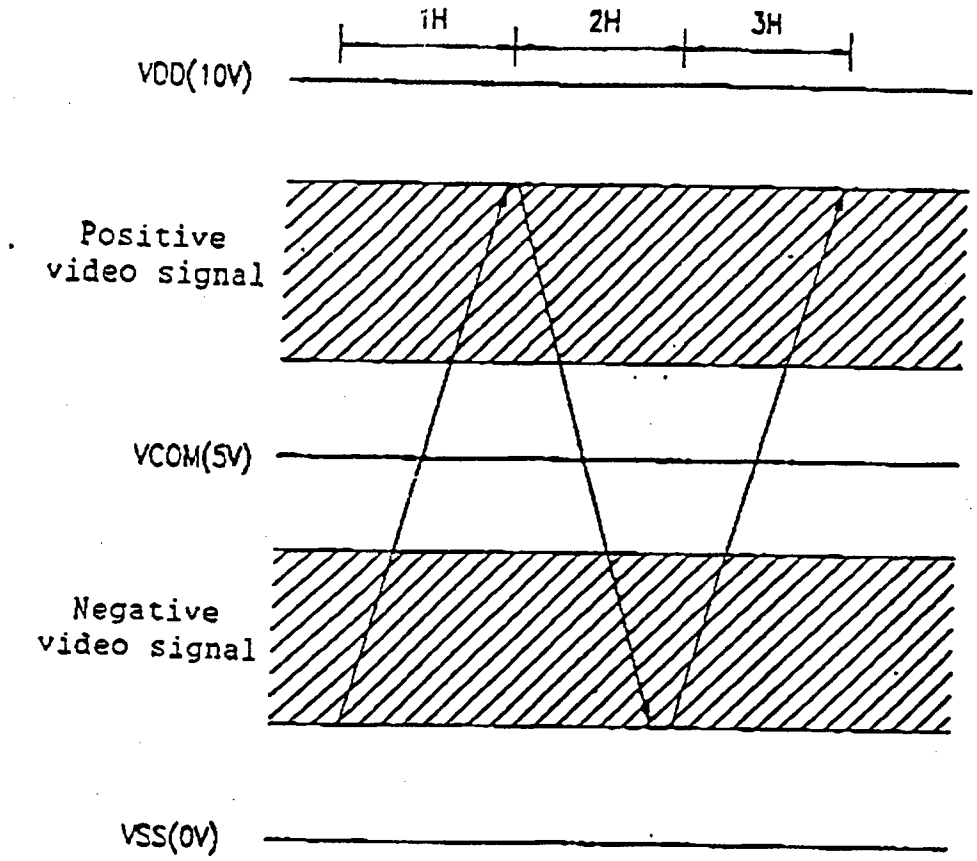

1H
2H
3H
VDD(10V)
Positive video signal
VCOM(5V)
Negative video signal
VSS(0V)

FIG. 7

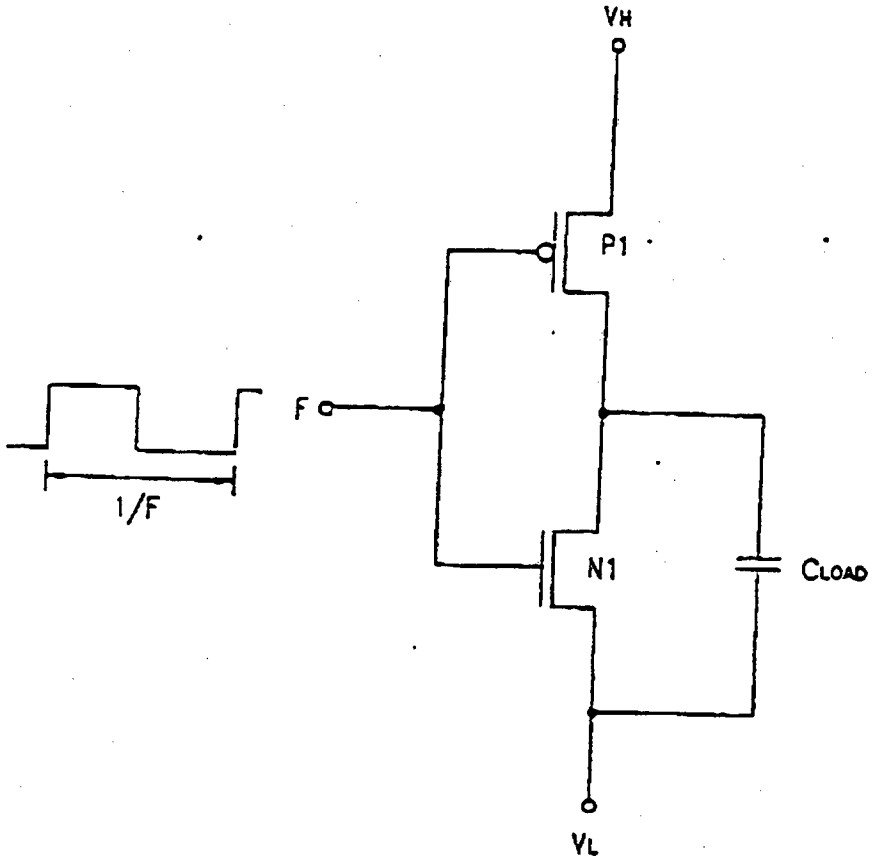


FIG.8

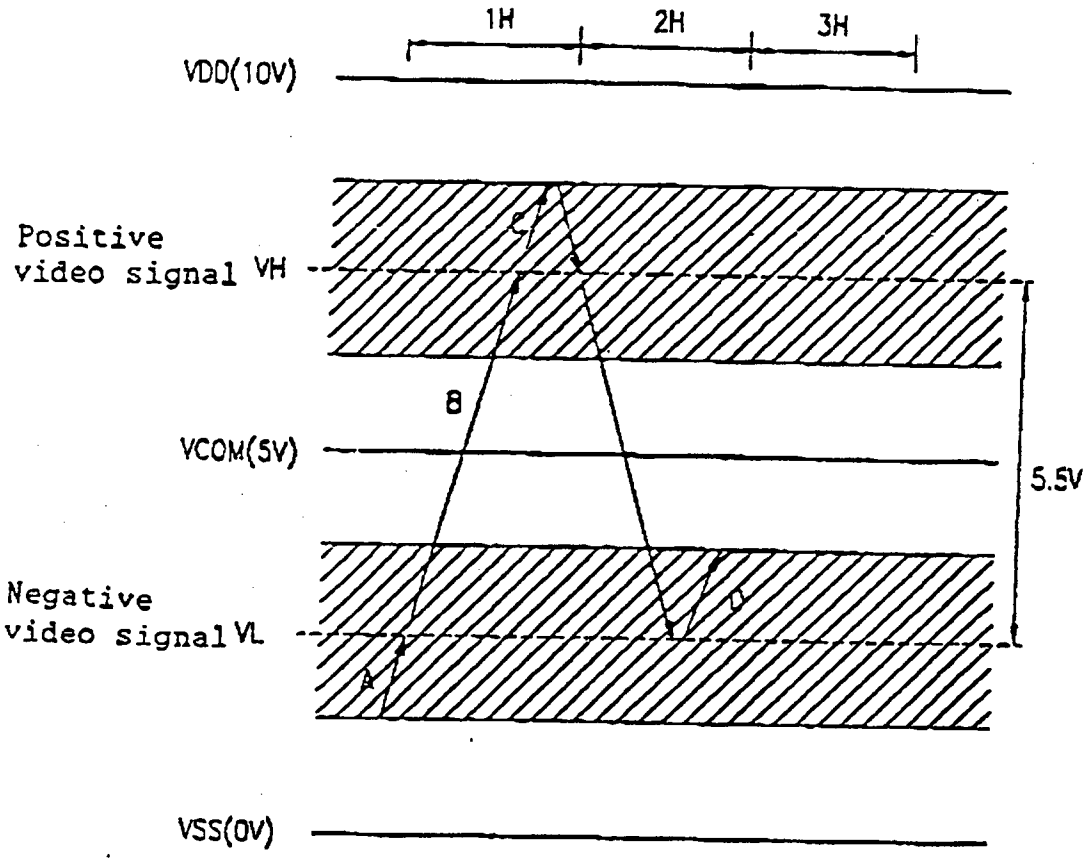

1H
2H
3H
VDD(10V)
Positive
video signal VH
C
B
VCOM(5V)
5.5V
Negative
video signal VL
D
A
VSS(0V)

FIG.9A

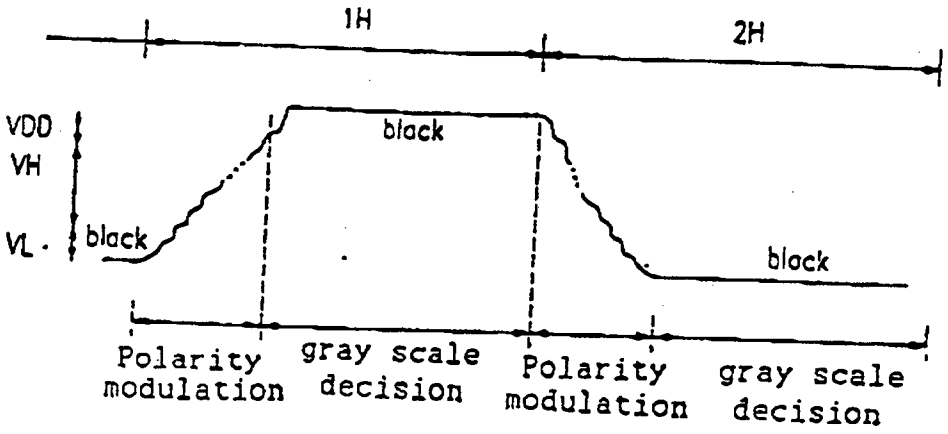

1H
2H
VDD
VH
VL
black
black
black
Polarity modulation
gray scale decision
Polarity modulation
gray scale decision

FIG.9B

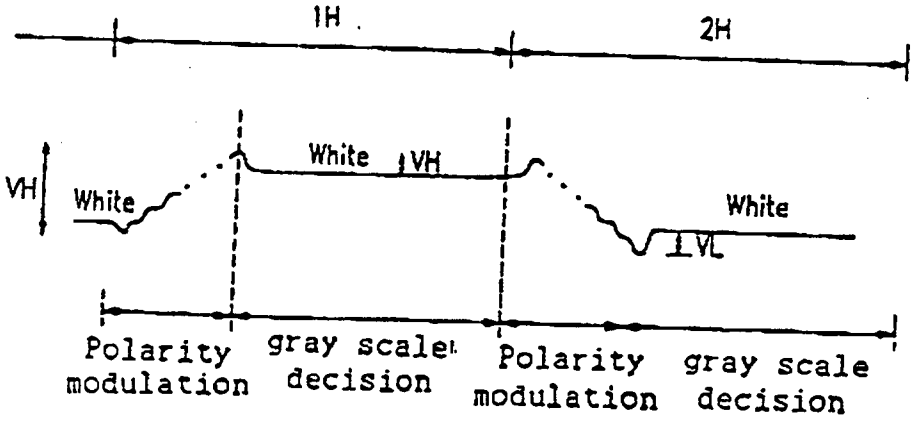

1H
2H
VH
White
White
VH
White
VL
Polarity modulation
gray scale decision
Polarity modulation
gray scale decision

FIG.10A

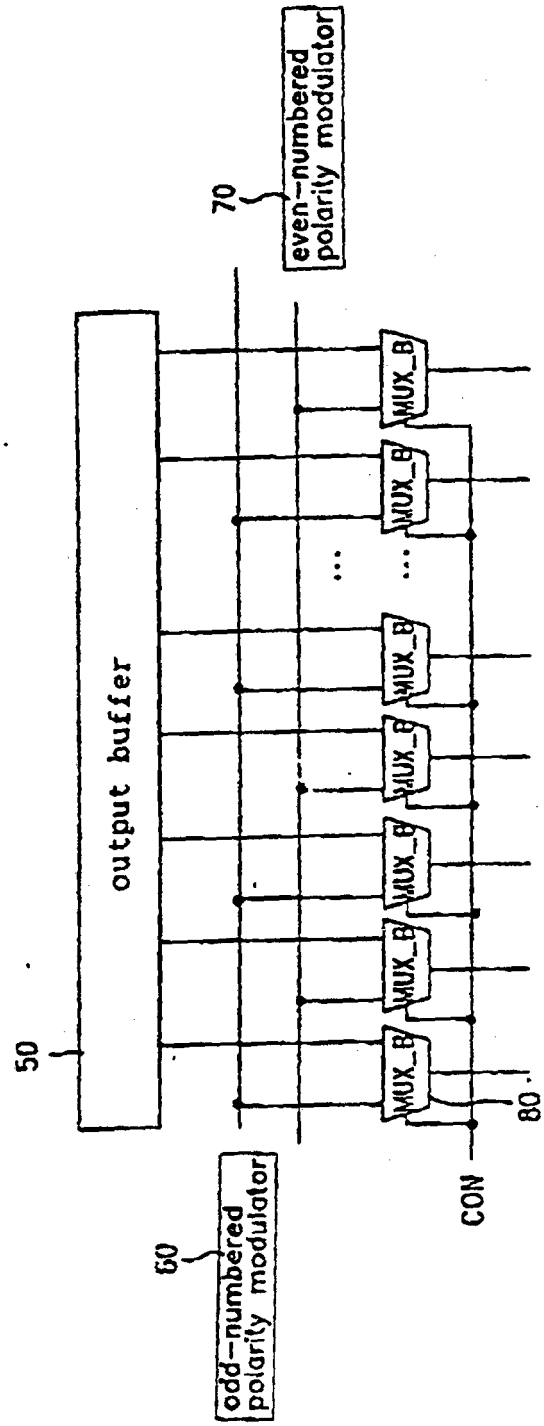

70
even-numbered polarity modulator
output buffer
50
MUX_B
60
odd-numbered polarity modulator
80
CON

FIG.10B

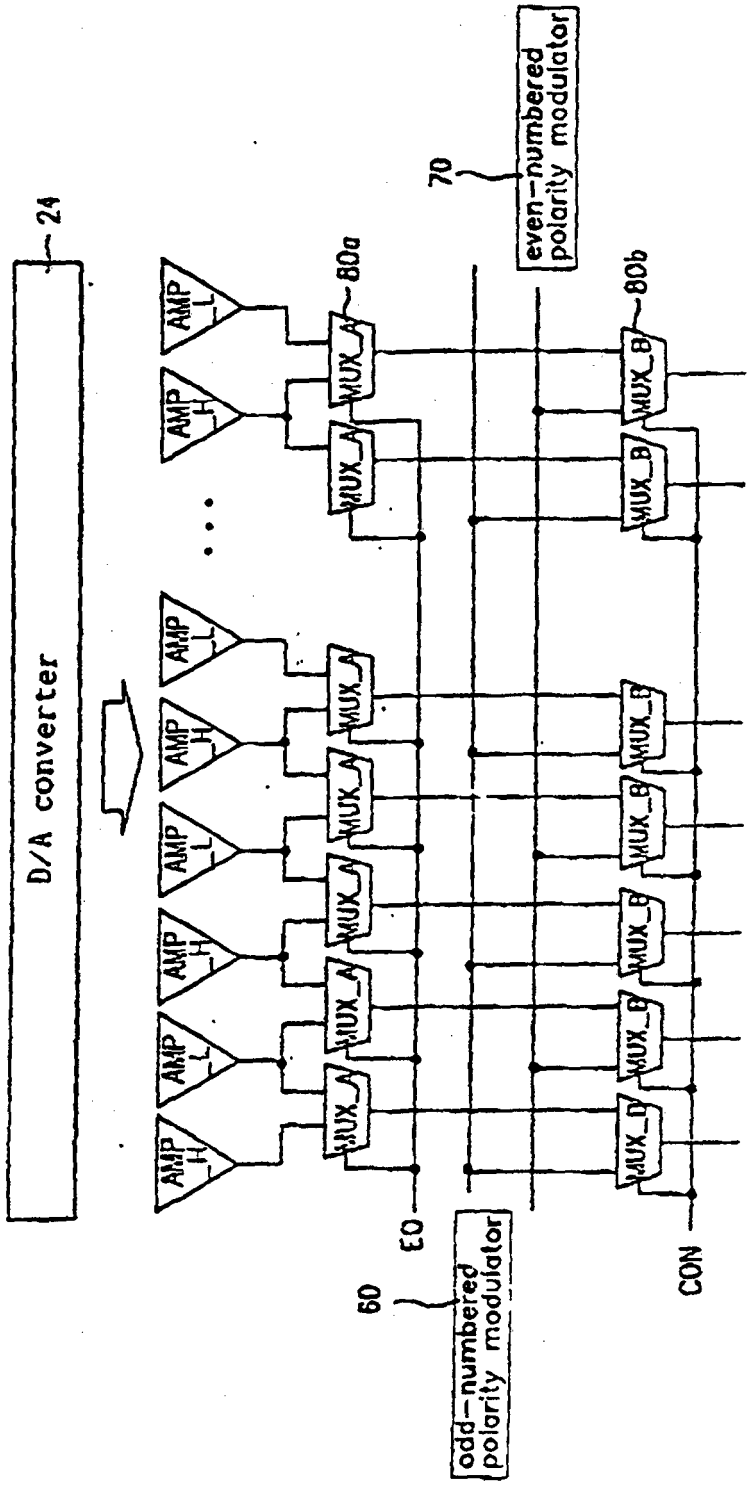

D/A converter
24
AMP_H
AMP_L
MUX_A
MUX_B
80a
80b
70
even-numbered polarity modulator
odd-numbered polarity modulator
60
EO
CON

FIG.10C

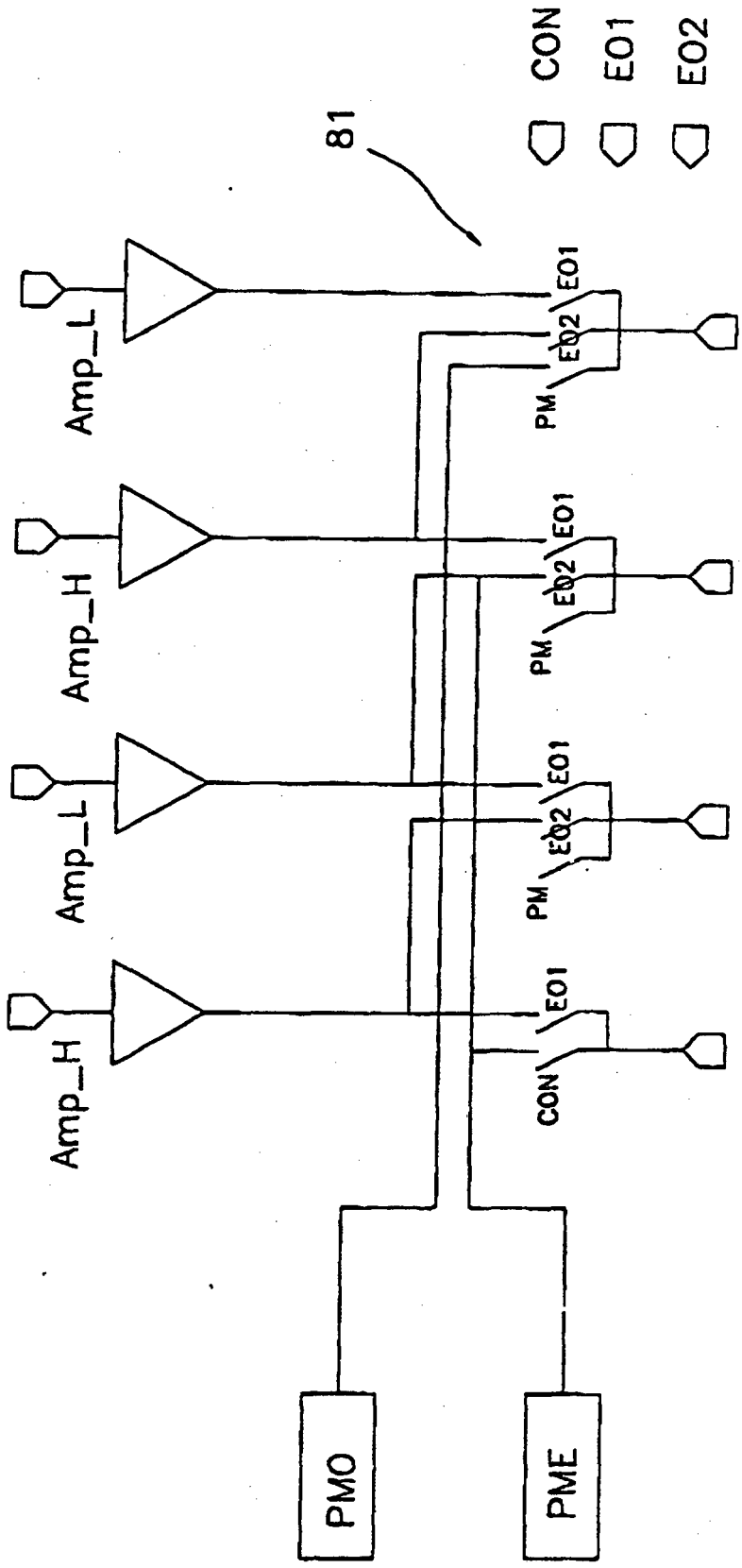
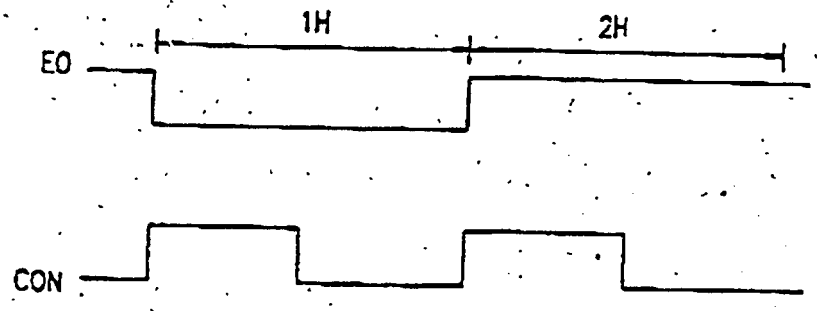


FIG.11A



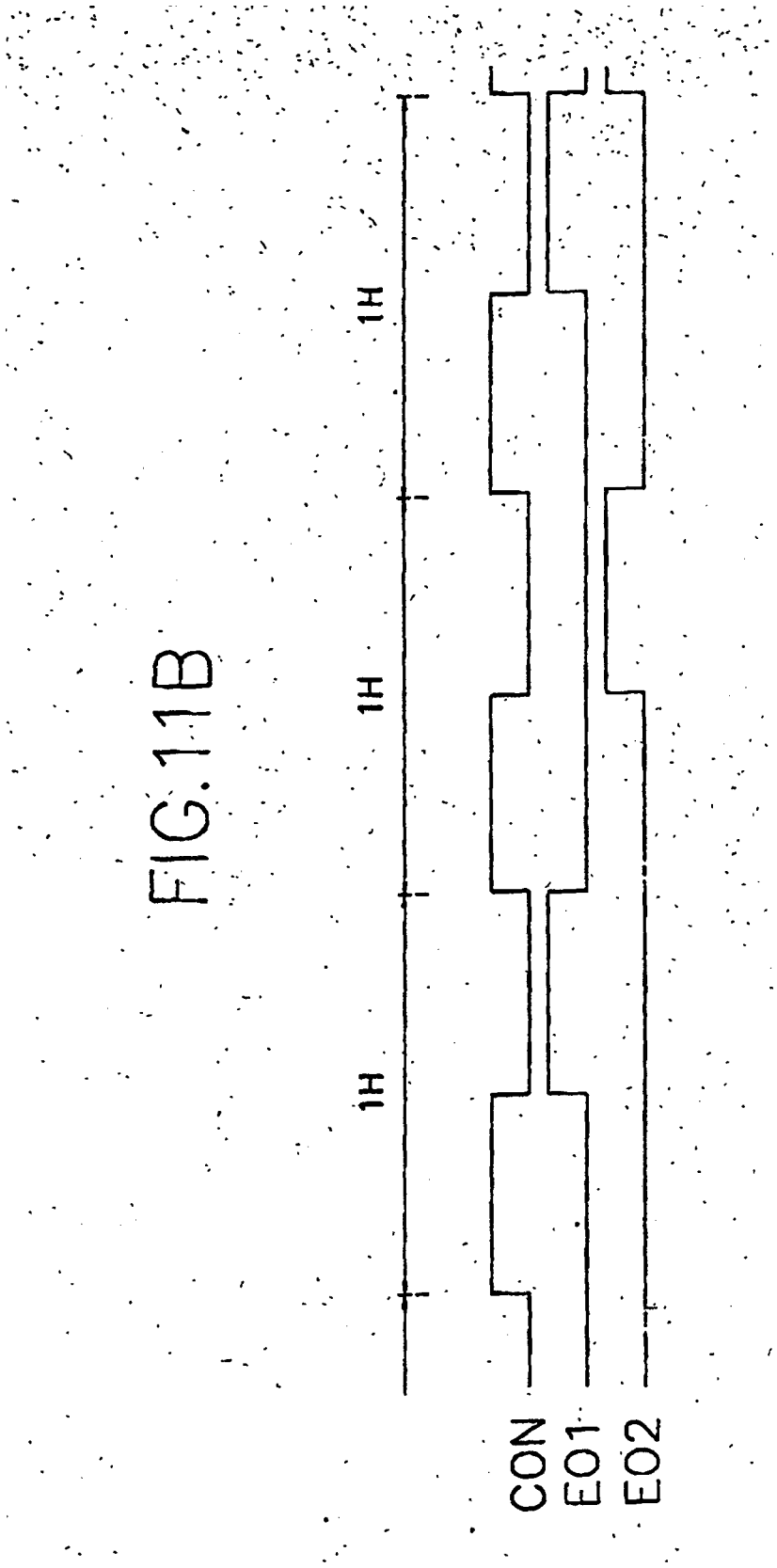


FIG.11B

FIG.12A

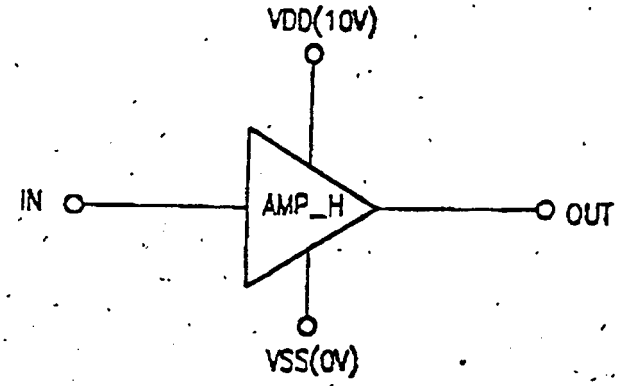


FIG.12B

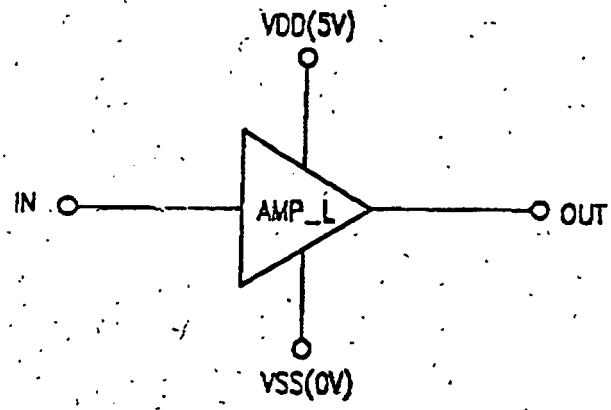


FIG.13

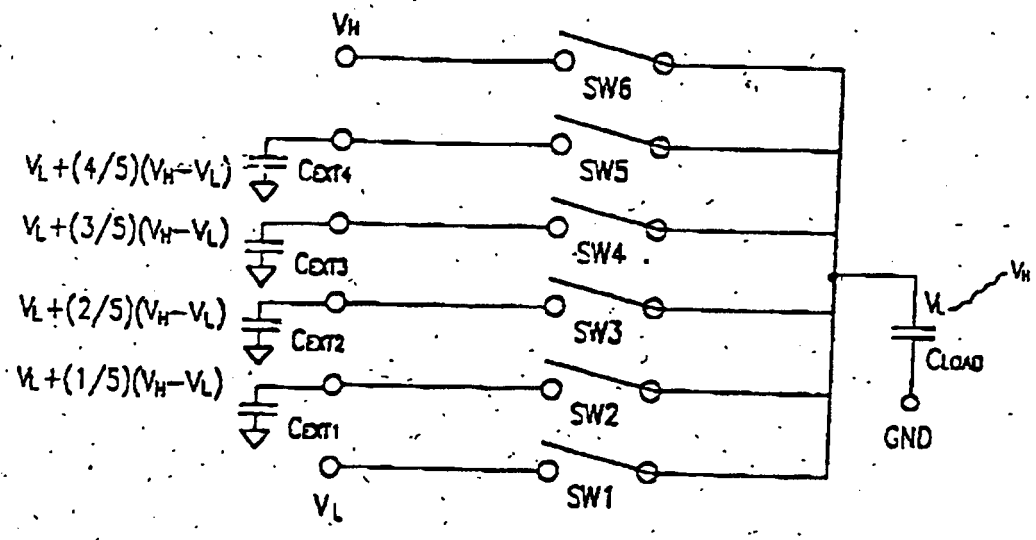

VH
SW6
VL+(4/5)(VH−VL)
CEXT4
SW5
VL+(3/5)(VH−VL)
CEXT3
SW4
VL+(2/5)(VH−VL)
CEXT2
SW3
VL+(1/5)(VH−VL)
CEXT1
SW2
VL
SW1
VH
VL
CLOAD
GND

FIG.14

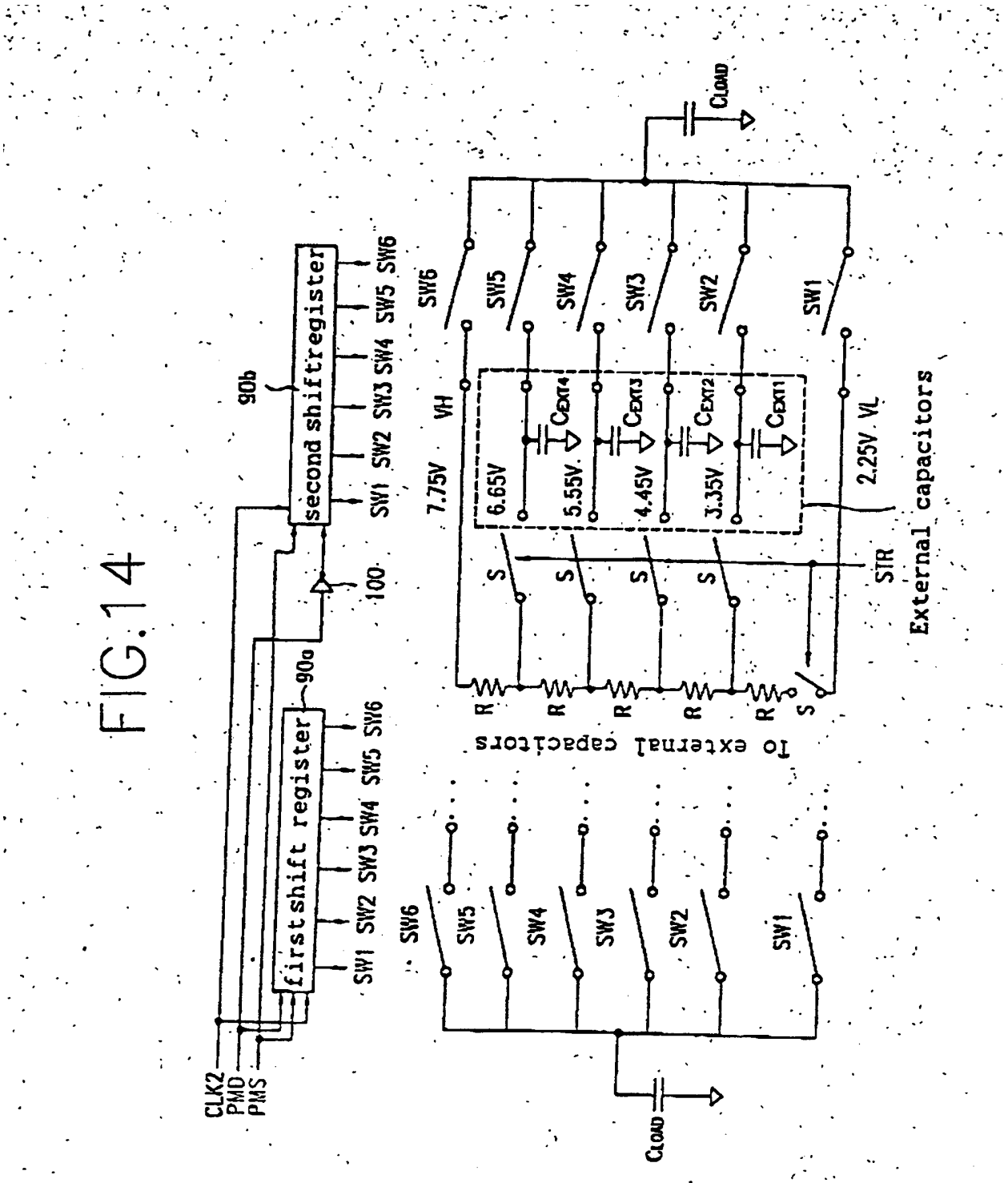

CLK2
PMD
PMS
first shift register
second shiftregister
90a
90b
100
SW1 SW2 SW3 SW4 SW5 SW6
CLOAD
VH
7.75V
6.65V
5.55V
4.45V
3.35V
2.25V VL
CEXT1
CEXT2
CEXT3
CEXT4
STR
S
R
External capacitors
To external capacitors

FIG.15

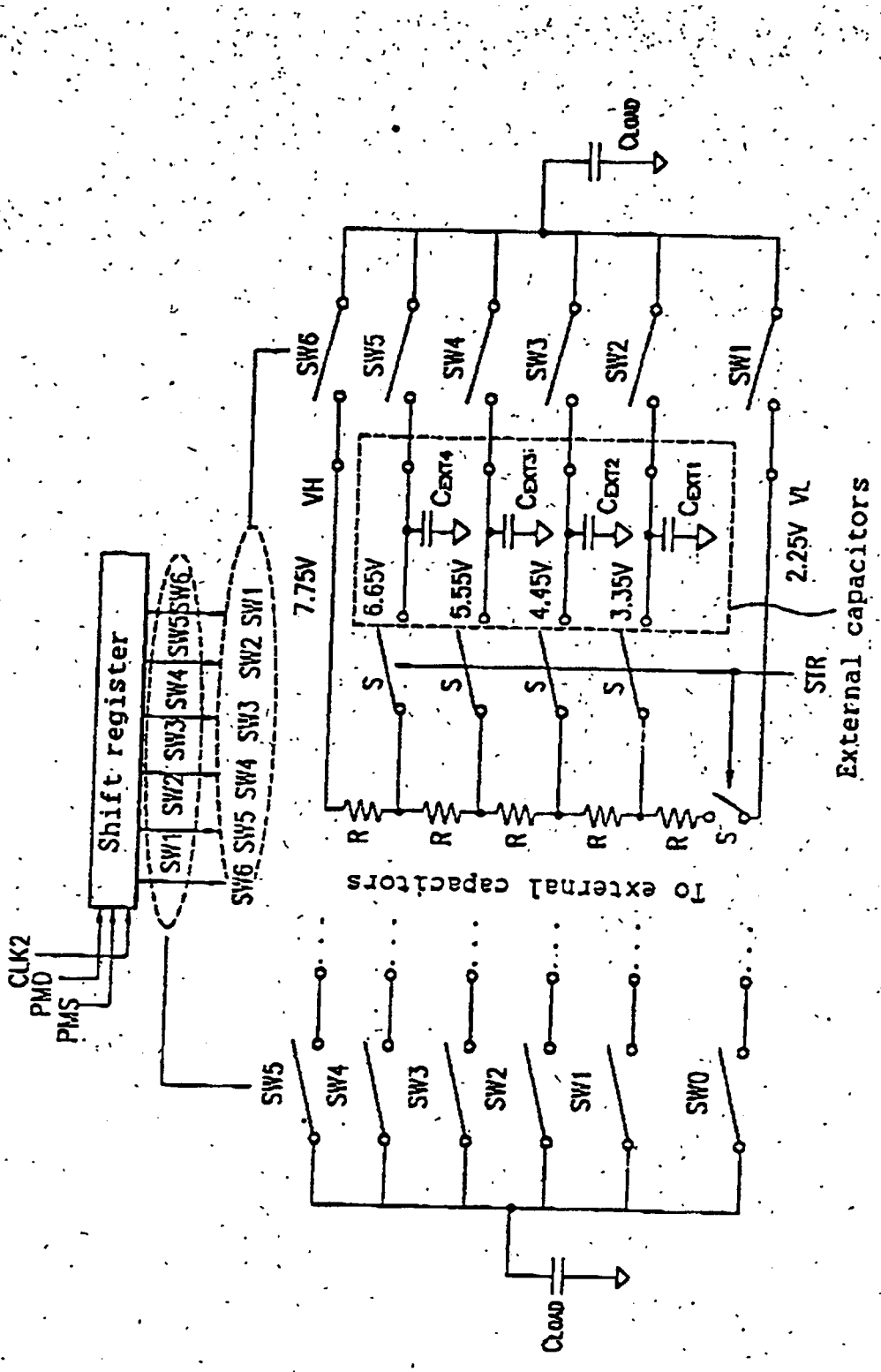

Shift register
CLK2
PMD
PMS
SW1 SW2 SW3 SW4 SW5 SW6
SW6 SW5 SW4 SW3 SW2 SW1
SW5 SW4 SW3 SW2 SW1 SW0
VH
7.75V
6.65V
5.55V
4.45V
3.35V
2.25V VL
CEXT4
CEXT3
CEXT2
CEXT1
External capacitors
STR
S
R
To external capacitors
CLOAD

FIG.16

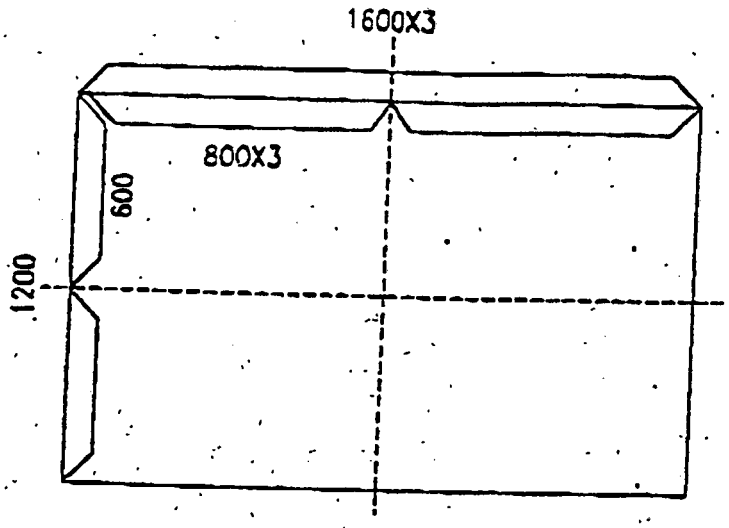

1600X3
800X3
600
1200

FIG.17

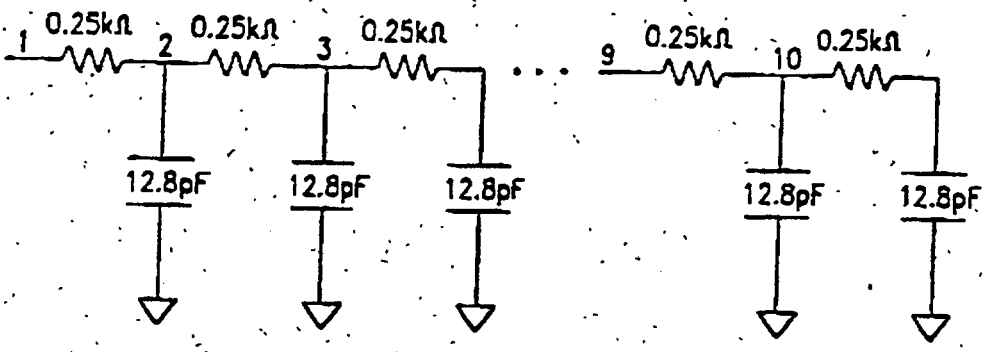

1
0.25kΩ
2
0.25kΩ
3
0.25kΩ
9
0.25kΩ
10
0.25kΩ
12.8pF
12.8pF
12.8pF
12.8pF
12.8pF

FIG.18

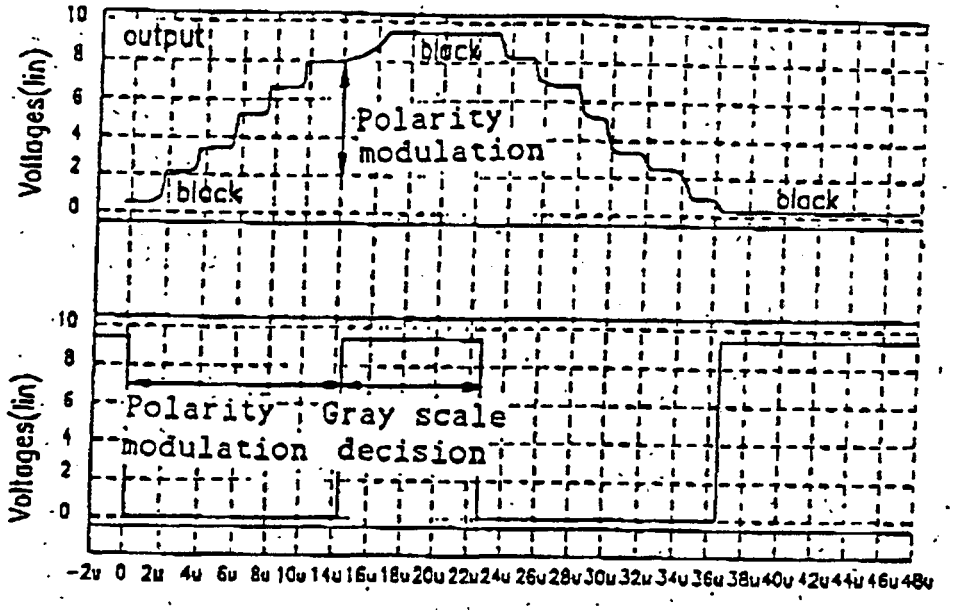
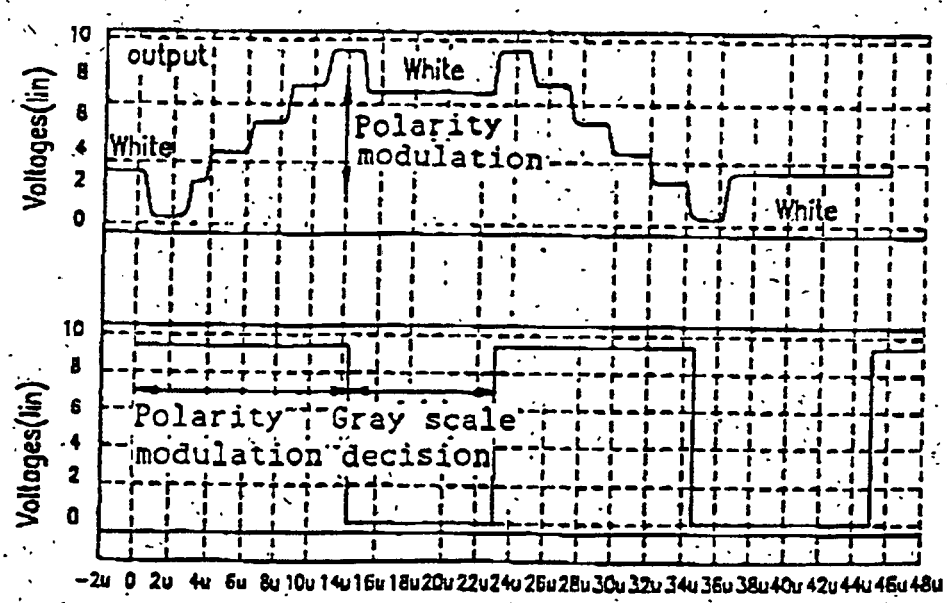

output
black
Polarity
modulation
black
black
Voltages(lin)
Polarity
Gray scale
modulation decision
Voltages(lin)
-2u 0 2u 4u 6u 8u 10u 14u 16u 18u 20u 22u 24u 26u 28u 30u 32u 34u 36u 38u 40u 42u 44u 46u 48u

FIG.19


output
White
Polarity
modulation
White
White
Voltages(lin)
Polarity
Gray scale
modulation decision
Voltages(lin)
-2u 0 2u 4u 6u 8u 10u 14u 16u 18u 20u 22u 24u 26u 28u 30u 32u 34u 36u 38u 40u 42u 44u 46u 48u

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- JP 10153986 A **[0022]**
- EP 0747748 A **[0023]**

专利名称(译)	用于驱动液晶显示器中的源极线的电路和方法		
公开(公告)号	EP1074966B1	公开(公告)日	2014-10-01
申请号	EP2000116569	申请日	2000-08-01
[标]申请(专利权)人(译)	NTEK RES		
申请(专利权)人(译)	NTEK RESEARCH CO.，LTD.		
当前申请(专利权)人(译)	SAMSUNG ELECTRONICS CO.，LTD.		
[标]发明人	KWON OH KYONG		
发明人	KWON, OH-KYONG		
IPC分类号	G09G3/36 G02F1/133 G09G3/20 H04N5/66		
CPC分类号	G09G3/2011 G09G3/3614 G09G3/3677 G09G3/3688 G09G2310/0248 G09G2310/0297 G09G2320/0247 G09G2330/023		
优先权	1019990032152 1999-08-05 KR		
其他公开文献	EP1074966A1		
外部链接	Espacenet		

摘要(译)

在液晶显示器中提供了一种源驱动电路和方法，其将负视频信号和正视频信号施加到液晶显示器的源极线，包括第一和第二板以及插入其间的液晶，其中每个视频信号是应用时，其电压分为极性调制和灰度决定两个阶段。通过逐步充电和放电完成极性调制。