

(19)



(11)

EP 2 879 126 B1

(12)

EUROPEAN PATENT SPECIFICATION

(45) Date of publication and mention of the grant of the patent:
31.07.2019 Bulletin 2019/31

(51) Int Cl.:
G09G 3/36^(2006.01) G11C 19/28^(2006.01)
H03K 17/687^(2006.01)

(21) Application number: **12881530.5**

(86) International application number:
PCT/CN2012/084688

(22) Date of filing: **15.11.2012**

(87) International publication number:
WO 2014/015580 (30.01.2014 Gazette 2014/05)

(54) GATE DRIVING CIRCUIT, METHOD AND LIQUID CRYSTAL DISPLAY

GATE-TREIBERSCHALTUNG, VERFAHREN UND FLÜSSIGKRISTALLANZEIGE

CIRCUIT D'ATTAQUE DE GRILLE, PROCÉDÉ ASSOCIÉ ET UNITÉ D'AFFICHAGE À CRISTAUX LIQUIDES

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR

- **XUE, Hailin**
Beijing 100176 (CN)
- **XUE, Yanna**
Beijing 100176 (CN)
- **LI, Yue**
Beijing 100176 (CN)
- **WANG, Xuelu**
Beijing 100176 (CN)

(30) Priority: **24.07.2012 CN 201210258201**

(43) Date of publication of application:
03.06.2015 Bulletin 2015/23

(73) Proprietors:
• **Beijing BOE Optoelectronics Technology Co., Ltd.**
Beijing 100176 (CN)
• **BOE Technology Group Co., Ltd.**
Beijing 100015 (CN)

(74) Representative: **Brötz, Helmut et al**
Rieder & Partner mbB
Patentanwälte - Rechtsanwalt
Corneliusstrasse 45
42329 Wuppertal (DE)

(72) Inventors:
• **CHEN, Xiaochuan**
Beijing 100176 (CN)

(56) References cited:
EP-A1- 2 400 481 CN-A- 101 527 170
CN-A- 101 587 700 CN-A- 101 882 470
US-A1- 2008 279 327 US-A1- 2011 019 118
US-A1- 2011 115 834

EP 2 879 126 B1

Note: Within nine months of the publication of the mention of the grant of the European patent in the European Patent Bulletin, any person may give notice to the European Patent Office of opposition to that patent, in accordance with the Implementing Regulations. Notice of opposition shall not be deemed to have been filed until the opposition fee has been paid. (Art. 99(1) European Patent Convention).

Description

TECHNICAL FIELD

[0001] The present disclosure relates to the technology of gate driving, and in particular to a gate driving circuit, a gate driving method, and a liquid crystal display (LCD).

BACKGROUND ART

[0002] At present, LCDs are commonly used flat panel displays, wherein Thin Film Transistor Liquid Crystal Display (TFT-LCD) is the mainstream product. With the increasingly fierce competition of TFT-LCD products, manufacturers have to reduce costs of products by means of adopting new technologies one after another, so as to enhance market competitiveness of products. The Gate on Array (GOA) technology refers to integrating gate drivers of the TFT-LCD on an array substrate, thus forming scan driving to the panel. As compared with the conventional techniques of Chip On Flex/Film (COF) and Chip On Glass (COG), the GOA technology not only can save costs, but also can achieve symmetry on both sides of the panel, which beautifies the design and leaves out a bonding area and a fan-out wiring space of the gate integrated circuit (Gate IC), thus achieving the design of a narrow frame; meanwhile, since the technique of gate direction bonding can be saved, it also facilitates improving productivity and yield.

[0003] Currently, the GOA circuit commonly used in the gate driving circuit adopts a 10T1C mode, in which one GOA unit in the gate driving circuit can drive only one row of gates and ten TFTs are needed to drive each row of gates. However, a display device with a small size will have an extremely small dot pitch under a resolution with a high number of Pixel Per Inch (PPI), less than $30 \times 90 \mu\text{m}$ sometimes, if ten TFTs are disposed on a space of $90 \mu\text{m}$, these ten TFTs need to be arranged in a row, in this way, a quite large sealing area is required. From EP 2 400 481 A1 it is known a shift register and an architecture of same on a display panel.

SUMMARY OF THE INVENTION

[0004] In view of the above, a primary object of the present disclosure is to provide a gate driving circuit, a gate driving method, and a display that can reduce the space occupied by the GOA circuit, and thereby reduce the sealing area of the display device.

[0005] The present invention is defined by the independent claims.

[0006] To achieve the above object, the technical solutions of the present disclosure are implemented as follows:

The present disclosure provides a gate driving circuit defined by claim 1.

[0007] The present disclosure also provides a liquid crystal display, comprising the gate driving circuit de-

scribed above.

[0008] The present disclosure also provides a gate driving method for driving the gate driving circuit described above, the method is defined by claim 3.

[0009] One GOA unit in the gate driving circuit of the present disclosure can output two gate driving signals, thus, two rows of pixels are driven by one GOA unit, as compared with the conventional GOA circuit, less TFTs are required to drive two rows of pixels, thus the space for disposing TFTs is saved, the sealing area of the LCD is reduced, and the narrow frame of the LCD is achieved.

BRIEF INTRODUCTION TO THE DRAWINGS

[0010]

Fig. 1 is a schematic diagram of functional configuration of each GOA unit in a gate driving circuit of the present disclosure;

Fig. 2 is a schematic diagram of architecture of specific components of a GOA unit in a gate driving circuit of a first embodiment of the present invention;

Fig. 3 is a time sequence diagram of input and output signals of a GOA unit in a gate driving circuit of the first embodiment of the present invention;

Fig. 4 is a flow chart of implementation of a gate driving method in a second embodiment of the present invention;

Fig. 5 is a schematic diagram of architecture of specific components of a GOA unit in a gate driving circuit of a third embodiment of the present invention; and

Fig. 6 is a schematic diagram of architecture of specific components of a GOA unit in a gate driving circuit of a fourth embodiment of the present invention.

SPECIFIC MODES FOR CARRYING OUT THE INVENTION

[0011] With respect to the LCD of the present disclosure, its array substrate comprises p (p is an integer not less than one) data driving lines and q (q is an integer not less than one) gate driving lines, pixels are set on areas where the data driving lines and the gate driving lines are interleaved, that is to say, pixels of p rows and q columns are set on the array substrate of the LCD, a gate driving circuit of the LCD outputs a gate driving signal to the pixels through the gate driving lines, and thereby drives the pixels to open, so that the respective pixels can receive a data signal output by the data driving circuit through the data driving lines, and thereby an image is displayed based on the data signal.

[0012] The gate driving circuit of the LCD comprises GOA units of multiple stages, each GOA unit can drive two adjacent rows of pixels, to be specific, the GOA unit of each stage drives two adjacent rows of pixels through two gate driving lines, when the GOA unit outputs a signal at a high level, the corresponding two adjacent rows of

pixels are driven to be opened through the corresponding gate driving lines, so that the corresponding two adjacent rows of pixels can receive a data signal; when the GOA unit outputs a signal at a low level, the corresponding two adjacent rows of pixels are closed to stop receiving the data signal. Thus, in one frame of picture, the GOA units of multiple stages in the gate driving circuit output a signal at a high level in sequence, and drive the pixels one by one with two adjacent rows of pixels as a unit.

[0013] Each GOA unit has an input signal terminal (INPUT terminal), a reset signal input terminal (RESET input terminal), a low level (VSS) terminal, a first clock signal (CLK1) input terminal, a second clock signal (CLK2) input terminal, a third clock signal (CLK3) input terminal, a fourth clock signal (CLK4) input terminal, a first gate driving signal (OUTPUT_n) output terminal, and a second gate driving signal (OUTPUT_{n+1}) output terminal, wherein OUTPUT_n is a gate driving signal for the n-th row of pixels, OUTPUT_{n+1} is a gate driving signal for the n+1-th row of pixels (n is an integer not less than 1, n is not less than the total number p of rows of pixels, if n is the last row of pixels, then the OUTPUT_{n+1} terminal can be useless). The GOA unit of any stage other than the first stage takes an output signal OUTPUT_{n-1} of a GOA unit of a previous stage as INPUT, and takes an output signal OUTPUT_{n+2} of a GOA unit of a next stage as RESET; in particular, as for the GOA unit of the first stage, it takes an STV signal (frame opening signal) as INPUT, as for the GOA unit of the last stage, usually a dummy GOA unit that is resultant and useless is designed to reset it.

[0014] Specifically, as shown in Fig. 1, the GOA unit of each stage comprises a pull-up module 11 and an output module 12. The pull-up module 11 outputs CLK2 to the output module 12 when INPUT is at a high level, the output module 12 is tuned on when CLK2 is at a high level, and outputs CLK3 as the first gate driving signal (OUTPUT_n), and outputs CLK4 as the second gate driving signal (OUTPUT_{n+1}) when being turned on, wherein CLK3 and CLK4 have opposite phases but the same cycle.

[0015] In addition, the pull-up module 11 is further for, when RESET is at a high level, stopping outputting CLK 2 to the output module 12, so that the output module 12 is able to quickly stop outputting the gate driving signal and complete a reset operation. Thus it can be known that, the output module 12, under the action of the pull-up module 11, can implement normally outputting and completing a shift within one cycle, and also can make the GOA unit reset according to the RESET signal and complete a reset operation in the operating process of the GOA unit.

[0016] The GOA unit of each stage further comprises a pull-down module 13 for pulling down voltage of the pull-up module 11, i.e., suppressing noise of the pull-up module 11.

First Embodiment

[0017] In this embodiment, the specific circuit structure of GOA unit of each stage is shown in Fig. 2, wherein the pull-up module 11 comprises a first switching device M1, a second switching device M2, a boosting device C1, and a third switching device M3, the source of M1 is taken as the INPUT terminal, the gate of M1 is connected to the source thereof, and the drain of M1 is connected to the source of M2, a connection point of the drain of M1 and the source of M2 is a pull up (PU) point, the drain of M2 is connected to a low level (VSS) terminal, the gate of M2 is connected to the RESET terminal, one end of the boosting device C1 is connected to the gate of M3 and to the PU point, the other end of C1 is connected to the drain of M3 and taken as an output terminal of the pull-up module 11, the source of M3 is taken as the second clock signal input terminal.

[0018] The output module 12 comprises a seventh switching device M7, an eleventh switching device M11, and a tenth switching device M10, wherein the gate of M7 is connected to the output terminal of the pull-up module 11, i.e., being connected to a connection point of C1 and the drain of M3, the source of M7 is taken as the CLK3 input terminal, and the drain of M7 is taken as the OUTPUT_n output terminal; the gate of M10 is connected to the output terminal of the pull-up module 11, i.e., being connected to a connection point of C1 and the drain of M3, the source of M10 is taken as the fourth clock signal input terminal, the drain of M10 is taken as the OUTPUT_{n+1} output terminal; the source of M11 is connected to the drain of M7, i.e., being connected to the OUTPUT_n output terminal, the gate of M11 is connected to the source of M10, i.e., being connected to the CLK4 input terminal, and the drain of M11 is connected to the VSS terminal.

[0019] The pull-down module 13 comprises a fourth switching device M4, the gate of M4 is connected to the RESET terminal, and the drain of M4 is connected to the drain of M3, i.e., the output terminal of the pull-up module 11, the source of M4 is connected to the VSS terminal. Voltage at the output terminal of the pull-up module 11 is pulled down according to the RESET signal.

[0020] The pull-down module 13 may further comprise a fifth switching device M5, a sixth switching device M6, an eighth switching device M8, a ninth switching device M9, and a twelfth switching device M12, wherein the source of M9 is taken as the CLK1 input terminal, the gate of M9 is connected to the source thereof, the drain of M9 is connected to the source of M8 and the gate of M5, this connection point is a pull down (PD) point; the gate of M8 is connected to the gate of M6 and to the PU point, the drain of M8 and the drain of M6 are connected to the VSS terminal, the source of M6 is connected to the drain of M5, and the source of M5 is connected to the source of M9.

[0021] The source of M12 is connected to the PU point, the gate of M12 is connected to the PD point of the pull-

down module, and the drain of M2 and the drain of M12 are connected to the low level (VSS) terminal.

[0022] The operating process of the GOA unit described above is as follows: when the gate driving signal output by the GOA unit of a previous stage is OUTPUT_{n-1}, that is, INPUT of the GOA unit of the current stage is at a high level, M1 is turned on to charge the PU point, C1 further pulls up the voltage at the PU point, i.e., charging the gate of M3, M3 is turned on; thereafter, CLK2 changes from a low level to a high level, since M3 is turned on, a high level signal of CLK2 is transmitted to the gate of M7 and the gate of M10 to make M7 and M10 be turned on, CLK3 is also at a high level, then the drain of M7, i.e., the OUTPUT_n output terminal, outputs CLK3 at a high level, that is, it outputs OUTPUT_n to drive the n-th row of pixels to open; thereafter, CLK3 changes from a high level to a low level, the OUTPUT_n output terminal stops outputting OUTPUT_n, CLK4 changes from a low level to a high level, since M10 is still in a turned-on state, the drain of M10, i.e., the OUTPUT_{n+1} output terminal, outputs CLK4 at a high level, that is, it outputs OUTPUT_{n+1} to drive the n+1-th row of pixels to open, M11 also is turned on to further pull down the OUTPUT_n output terminal, make the OUTPUT_n output terminal stop outputting OUTPUT_n, and thereby suppress the noise generated at the OUTPUT_n output terminal in this process. When CLK3 changes from a low level to a high level again and CLK4 changes from a high level to a low level, CLK2 changes from a high level to a low level, M7 and M10 are turned off, the OUTPUT_n output terminal and the OUTPUT_{n+1} output terminal are quickly pulled down to stop outputting.

[0023] When the GOA unit of a next stage outputs OUTPUT_{n+2}, that is, the RESET of the GOA unit of the current stage is at a high level, M2 is turned on to discharge the PU point, and pull down the voltage at the PU point, so that the voltage at the gate of M3 is pulled down, M3 is turned off, CLK2 cannot be transmitted to the gate of M7 and the gate of M10, which makes M7 and M10 remain in a turned-off state, the OUTPUT_n output terminal and the OUTPUT_{n+1} output terminal of the GOA unit of the current stage stop outputting.

[0024] In the above process, when CLK2 changes from a high level to a low level, CLK1 changes from a low level to a high level, M9 is turned on to charge the PD point, the voltage at the PD point is pulled up, M5 is turned on to charge the PD point to further pull up the voltage at the PD point, which makes M12 and M4 be turned on. M12 discharges the PU point when being turned on, and suppresses the noise generated by the pull-up module 11. M4 discharges the other end of C1, the drain of M3, the gate of M7, and the gate of M10 when being turned on, and suppresses the noise generated by the output module 12. When CLK2 is at a high level, that is, when the GOA unit of the current stage outputs normally, M6 and M8 are also turned on to suppress the noise generated by the pull-up module 11.

[0025] The time sequence of input and output signals

of the GOA unit as described above is as shown in Fig. 3, wherein CLK1 and CLK2 are two clock signals having opposite phases but the same cycle, CLK3 and CLK4 are two clock signals having opposite phases but the same cycle, the cycle of CLK2 is twice that of CLK3, the cycle of CLK4 and CLK3 is the time for which one row of pixels are opened, that is, 1/p of one frame of image, wherein p is the total number of rows of pixels. When CLK2 changes from a low level to a high level, CLK3 changes from a low level to a high level and CLK4 changes from a high level to a low level. In particular, CLK2 of the GOA unit of the current stage is the same as CLK1 of the GOA unit of an adjacent stage, CLK2 of the GOA unit of an adjacent stage is the same as CLK1 of the GOA unit of the current stage. That is, the adjacent GOA units are opposite in phase but the same in cycle in terms of CLK1 or CLK2.

[0026] From the above description with respect to the operating process, it can be known that, the function of C1 in the pull-up module 11 is, when CLK2 is at a high level, further pulling up the voltage at the PU point, and thereby reducing noise which is coupled to the PU point by CLK2 via a parasitic capacitor of M3, that is, the noise of the output module 11 will be reduced accordingly. M2 has a function similar to that of M12, it can pull down the voltage at the PU point when RESET is at a high level.

[0027] The pull-down module 13 is also optional. M6, M8, M5, and M9 are for controlling the voltage at PD point, the voltage at the PD point controls the turning-on of M12, which further controls to pull down the voltage at the PU point, and thereby accelerates the turning-off of M3, so that the CLK2 high level signal is not output to the output module 12. As will be appreciated that, the voltage at the PD point may be controlled by using other ways, M12 may be also controlled by a separate signal line, as long as the function of pulling down the voltage at the PU point by M12 in this embodiment can be achieved. Meanwhile, the voltage at the PD point also controls the turning-on of M4, which can pull down the voltage input by the pull-up module 11 to the output module 12, and pull down the voltage at the pull-up module 11, that is, it can be also considered as suppressing noise of the output module 12. Of course, M4 in this embodiment may also be controlled to be turned on by the RESET signal. Through the above analysis it can be known that, the pull-down module 13 can be divided into three shunts, that is, a first pull-down shunt M6, M8, M5, M9 and M12, a second pull-down shunt M6, M8, M5, M9 and M4, and a third pull-down shunt M4 (whose gate is connected to RESET), these three shunts may exist separately or in combination.

[0028] M11 is also optional in the output module 12. The function of M11 is, under the action of CLK4, further pulling down the OUTPUT_n output terminal, making the OUTPUT_n output terminal stop outputting OUTPUT_n, and thereby suppressing the noise generated by the OUTPUT_n output terminal in this process.

[0029] The above M1 to M12 may specifically be Metal-

Oxide-Semiconductor Field Effect Transistors (MOS-FET). C1 is a capacitor device. Since the manufacturing techniques of a source and a drain of the transistors are the same, the names of the source and the drain are interchangeable, and name change can be made according to the direction of the voltage.

Second Embodiment

[0030] This embodiment provides a gate driving method, as shown in Fig. 4, the method may mainly comprise the following steps:

Step 401: outputting, by a pull-up module, a second clock signal to an output module when an input signal is at a high level;

Step 402: turning on the output module when the second clock signal is at a high level, so as to output a third clock signal as a first gate driving signal and output a fourth clock signal as a second gate driving signal.

[0031] Herein, the third clock signal and the fourth clock signal have opposite phases but the same cycle, the cycle of the second clock signal is twice that of the third clock signal. In particular, when the second clock signal changes from a low level to a high level, the third clock signal changes from a low level to a high level and the fourth clock signal changes from a high level to a low level.

[0032] In the above method, after outputting the third clock signal as the first gate driving signal and prior to outputting the fourth clock signal as the second gate driving signal, the method may further comprise pulling down, by the output module, the first gate driving signal when the third clock signal changes from a low level to a high level and the fourth clock signal changes from a high level to a low level.

Third Embodiment

[0033] In this embodiment, the specific circuit structure of GOA unit of each stage is shown in Fig. 5, its architecture is substantially the same as that in the second embodiment, the difference lies in that a thirteenth switching device M13 is added, the gate of M13 is connected to the PD point, the source of M13 is connected to the output terminal of the pull-up module 11, i.e., being connected to a connection point of C1 and the drain of M3, and the drain of M13 is connected to the VSS terminal; the gate of M4 is connected to the RESET input terminal, the source of M4 is connected to the output of the pull-up module 11, i.e., being connected to a connection point of C1 and the drain of M3, the drain of M4 is connected to the VSS terminal; M4 at this time is controlled separately by the RESET signal, M13 is controlled separately by a voltage signal at the PD point. In this way, M13 pulls down the pull-up module under the control of

the PD point, and M4 pulls down the pull-up module under the control of the RESET, which makes M4 and M13 in common accomplish the function of M4 in the first embodiment, that is, M4 in the first embodiment does not need to be always in an operating status, which facilitates extending a service life.

Fourth Embodiment

[0034] In this embodiment, the specific circuit structure of GOA unit of each stage is shown in Fig. 6, its architecture is substantially the same as the GOA unit in the third embodiment, the difference lies in that a fourteenth switching device M14 is added additionally in the pull-down module, the gate of M14 is connected to the CLK1 input terminal, the source of M14 is connected to the output terminal of the pull-up module 11, that is, being connected to a connection point of C1 and the drain of M3, and the drain of M14 is connected to the VSS terminal, in this way, when CLK1 is at a high level, M14 can further pull down the pull-up module, and thereby further improve the noise elimination capability of the GOA unit.

[0035] In the prior art, one GOA unit can drive only one row of pixels, the space required to dispose TFT is relatively large; while in the gate driving circuit of the present disclosure, one GOA unit can drive two rows of pixels, which is implemented requiring less TFTs as compared with the prior art, thus the space for disposing TFTs is saved, the sealing area is reduced, and the narrow frame of the LCD is achieved.

[0036] The above described are merely preferred embodiments of the present invention, they are not intended to limit the scope of the present invention which is defined by the claims.

[0037] Explanation of Reference signs: M1, a first TFT switching device; M2, a second TFT switching device; M3, a third TFT switching device; M4, a fourth TFT switching device; M5, a fifth TFT switching device; M6, a sixth TFT switching device; M7, a seventh TFT switching device; M8, an eighth TFT switching device; M9, a ninth TFT switching device; M10, a tenth TFT switching device; M11, an eleventh TFT switching device; M12, a twelfth TFT switching device; M13, a thirteenth TFT switching device; M14, a fourteenth TFT switching device; C1, a boosting device; 11, a pull-up module; 12, an output module; and 13, a pull-down module.

Claims

1. A gate driving circuit comprising Gate on Array GOA units of multiple stages, the gate driving circuit is configured to drive a liquid crystal display comprising multiple rows of pixels, each of the GOA units is configured to drive two adjacent rows of pixels on an array substrate of the display, the GOA unit comprising:

a pull-up module (11) for receiving an input signal at an input signal terminal, receiving a second clock signal (CLK2) at a second clock signal input terminal and outputting the second clock signal (CLK2) to an output module (12) when the input signal is at a high level, wherein the pull-up module comprises a first switching device (M1), a second switching device (M2), a boosting device (C1), and a third switching device (M3), a gate and a source of the first switching device are both connected to the input signal terminal, and a drain of the first switching device is connected to a source of the second switching device, a connection point of the drain of the first switching device and the source of the second switching device is a pull up (PU) point, a drain of the second switching device is connected to a low level (VSS) terminal, a gate of the second switching device is connected to a reset signal input terminal, one end of the boosting device is connected to a gate of the third switching device and to the pull up point, the other end of the boosting device is connected to a drain of the third switching device, a connection point of the other end of the boosting device and the drain of the third switching device is an output terminal of the pull-up module, a source of the third switching device is connected to the second clock signal input terminal;

the output module (12) for receiving a third clock signal (CLK3) at a third clock signal input terminal, receiving a fourth clock signal (CLK4) at a fourth clock signal input terminal, and outputting the third clock signal (CLK3) as a first gate driving signal for driving a first row of the two adjacent rows of pixels and outputting the fourth clock signal (CLK4) as a second gate driving signal for driving a second row of the two adjacent rows of pixels when the second clock signal (CLK2) is at the high level; and

a pull-down module (13) for pulling down voltage of the pull-up module (11), wherein the pull-down module comprises a fourth switching device (M4), a gate of the fourth switching device is connected to the reset signal input terminal, a drain of the fourth switching device is connected to the output terminal of the pull-up module, a source of the fourth switching device is connected to the low level terminal;

characterized in that

the output module (12) comprises a seventh switching device (M7), a tenth switching device (M10) and an eleventh switching device (M11);

the gate of the seventh switching device (M7) is connected to the output terminal of the pull-up module (11), the source of the seventh switching device (M7) is connected

5

10

15

20

25

30

35

40

45

50

55

to the third clock signal input terminal, and the drain of the seventh switching device (M7) is connected to a first gate driving signal output terminal outputting the first gate driving signal;

the gate of the tenth switching device (M10) is connected to the output terminal of the pull-up module (11), the source of the tenth switching device (M10) is connected to the fourth clock signal input terminal, and the drain of the tenth switching device (M10) is connected to a second gate driving signal output terminal outputting the second gate driving signal;

the gate of the eleventh switching device (M11) is connected to the fourth clock signal input terminal, the source of the eleventh switching device (M11) is connected to the first gate driving signal output terminal, and the drain of the eleventh switching device (M11) is connected to the low level terminal, the eleventh switching device (M11) is turned on to pull down the first gate driving signal when the third clock signal (CLK3) changes from the high level to the low level and the fourth clock signal (CLK4) changes from the low level to the high level.

2. A liquid crystal display comprising the gate driving circuit according to claim 1.
3. A gate driving method for driving the gate driving circuit according to claim 1, comprising:

receiving, by the pull-up module (11), the input signal and the second clock signal (CLK2), and receiving, by the output module (12), the third clock signal (CLK3) and the fourth clock signal (CLK4);

outputting, by the pull-up module (11), the second clock signal (CLK2) to the output module (12) when the input signal is at the high level; and outputting, by the seventh switching device (M7) of the output module (12), the third clock signal (CLK3) as the first gate driving signal for driving the first row of pixels and outputting, by the tenth switching device (M10) of the output module (12), the fourth clock signal (CLK4) as the second gate driving signal for driving the second row of pixels when the second clock signal (CLK2) is at the high level;

pulling down, by the eleventh switching device (M11) of the output module (12), the first gate driving signal when the third clock signal (CLK3) changes from the high level to the low level and the fourth clock signal (CLK4) changes from the low level to the high level,

wherein the third clock signal (CLK3) and the

fourth clock signal (CLK4) have opposite phases but the same cycle, the cycle of the second clock signal (CLK2) is twice that of the third clock signal (CLK3), when the second clock signal (CLK2) changes from the low level to the high level, the third clock signal (CLK3) changes from the low level to the high level and the fourth clock signal (CLK4) changes from the high level to the low level,
 the second clock signals (CLK2) of adjacent GOA units have opposite phases but the same cycle.

Patentansprüche

1. Gate-Treiber-Schaltung, umfassend Gate-on-Array-GOA-Einheiten mehrerer Stufen, wobei die Gate-Treiber-Schaltung konfiguriert ist, um eine Flüssigkristallanzeige welche mehrere Reihen von Pixeln umfasst, anzusteuern, wobei jede der GOA-Einheiten konfiguriert ist, um zwei benachbarte Reihen von Pixeln auf einem Array-Substrat der Anzeige anzusteuern, und wobei die GOA-Einheit umfasst:

ein Pull-Up-Modul (11) zum Empfangen eines Eingangssignals an einem Eingangssignalsanschluss, zum Empfangen eines zweiten Taktsignals (CLK2) bei einem zweites-Taktsignal-Eingangsanschluss und zur Ausgabe des zweiten Taktsignals (CLK2) an ein Ausgangsmodul (12), wenn das Eingangssignal bei einem hohen Level ist, wobei das Pull-Up-Modul eine erste Schalteinrichtung (M1), eine zweite Schalteinrichtung (M2), eine erste Boost-Einrichtung (C1) und eine dritte Schalteinrichtung (M3) umfasst, wobei ein Gate und eine Source der ersten Schalteinrichtung beide an den Eingangssignalsanschluss angeschlossen sind, und wobei ein Drain der ersten Schalteinrichtung an eine Source der zweiten Schalteinrichtung angeschlossen ist, wobei ein Verbindungspunkt des Drains der ersten Schalteinrichtung und der Source der zweiten Schalteinrichtung ein Pull-Up-(PU)-Punkt ist, wobei ein Drain der zweiten Schalteinrichtung an einen Niedrig-Level-(VSS)-Anschluss angeschlossen ist, wobei ein Gate der zweiten Schalteinrichtung an einen RücksetzsignalEingangsanschluss angeschlossen ist, wobei ein Ende der Boost-Einrichtung an ein Gate der dritten Schalteinrichtung und an den Pull-Up-Punkt angeschlossen ist, wobei das andere Ende der Boost-Einrichtung an einen Drain der dritten Schalteinrichtung angeschlossen ist, wobei ein Verbindungspunkt des anderen Endes der Boost-Einrichtung und des Drains der dritten Schalteinrichtung ein Aus-

gangsanschluss des Pull-Up-Moduls ist, wobei eine Source der dritten Schalteinrichtung an den zweites-Taktsignal-Eingangsanschluss angeschlossen ist;

das Ausgangsmodul (12) zum Empfangen eines dritten Taktsignals (CLK3) bei einem drittes-Taktsignal-Eingangsanschluss, zum Empfangen eines vierten Taktsignals (CLK4) bei einem viertes-Taktsignal-Eingangsanschluss und zur Ausgabe des dritten Taktsignals (CLK3) als ein erstes Gate-Treibersignal zur Ansteuerung einer ersten Reihe von den zwei benachbarten Reihen von Pixeln und zur Ausgabe des vierten Taktsignals (CLK4) als ein zweites Gate-Treibersignal zur Ansteuerung einer zweiten Reihe von den zwei benachbarten Reihen von Pixeln, wenn das zweite Taktsignal (CLK2) bei dem hohen Level ist; und

ein Pull-Down-Modul (13) zum Herunterziehen von Spannung des Pull-Up-Moduls (11), wobei das Pull-Down-Modul eine vierte Schalteinrichtung (M4) umfasst, wobei ein Gate der vierten Schalteinrichtung an den Rücksetzsignal-Eingangsanschluss angeschlossen ist, wobei ein Drain der vierten Schalteinrichtung an den Ausgangsanschluss des Pull-Up-Moduls angeschlossen ist, und wobei eine Source der vierten Schalteinrichtung an den Niedrig-Level-Anschluss angeschlossen ist;

dadurch gekennzeichnet,

dass das Ausgangsmodul (12) eine siebte Schalteinrichtung (M7), eine zehnte Schalteinrichtung (M10) und eine elfte Schalteinrichtung (M11) umfasst;

dass das Gate der siebten Schalteinrichtung (M7) an den Ausgangsanschluss des Pull-Up-Moduls (11) angeschlossen ist, die Source der siebten Schalteinrichtung (M7) an den drittes-Taktsignal-Eingangsanschluss angeschlossen ist und der Drain der siebten Schalteinrichtung (M7) an einen ersten Gate-Treibersignal-Ausgangsanschluss, der das erste Gate-Treibersignal ausgibt, angeschlossen ist;

dass das Gate der zehnten Schalteinrichtung (M10) an den Ausgangsanschluss des Pull-Up-Moduls (11) angeschlossen ist, die Source der zehnten Schalteinrichtung (M10) an den viertes-Taktsignal-Eingangsanschluss angeschlossen ist, und der Drain der zehnten Schalteinrichtung (M10) an einen zweiten Gate-Treibersignal-Ausgangsanschluss, der das zweite Gate-Treibersignal ausgibt, angeschlossen ist;

dass das Gate der elften Schalteinrichtung (M11) an den viertes-Taktsignal-Eingangsanschluss angeschlossen ist, die Source der elften Schalteinrichtung (M11) an den ersten Gate-Treibersignal-Ausgangsanschluss angeschlossen ist, und der Drain der elften Schalteinrich-

tung (M11) an den Niedrig-Level-Anschluss angeschlossen ist, dass die elfte Schalteinrichtung (M11) eingeschaltet wird, um das erste Gate-Treiber-Signal herunterzuziehen, wenn das dritte Taktsignal (CLK3) sich von dem hohen Level zu dem niedrigen Level verändert und sich das vierte Taktsignal (CLK4) von dem niedrigen Level zu dem hohen Level verändert.

2. Flüssigkristallanzeige, umfassend die Gate-Treiberschaltung gemäß Anspruch 1.

3. Gate-Ansteuerungsverfahren zur Ansteuerung der Gate-Treiberschaltung gemäß Anspruch 1, umfassend:

mittels des Pull-Up-Moduls (11) Empfangen des Eingangssignals und des zweiten Taktsignals (CLK2) und mittels des Ausgangsmoduls (12) Empfangen des dritten Taktsignals (CLK3) und des vierten Taktsignals (CLK4);

mittels des Pull-Up-Moduls (11) Ausgeben des zweiten Taktsignals (CLK2) an das Ausgangssignal (12), wenn das Eingangssignal bei dem hohen Level ist; und

mittels der siebten Schalteinrichtung (M7) des Ausgangsmoduls (12) Ausgeben des dritten Taktsignals (CLK3) als das erste Gate-Treiber-Signal zur Ansteuerung der ersten Reihe von Pixeln, und mittels der zehnten Schalteinrichtung (M10) des Ausgangsmoduls (12) Ausgeben des vierten Taktsignals (CLK4) als das zweite Gate-Treibersignal zur Ansteuerung der zweiten Reihe von Pixeln, wenn das zweite Taktsignal (CLK2) bei dem hohen Level ist;

mittels der elften Schalteinrichtung (M11) des Ausgangsmoduls (12) Herunterziehen des ersten Gate-Treibersignals, wenn das dritte Taktsignal (CLK3) sich von dem hohen Level zu dem niedrigen Level ändert und sich das vierte Taktsignal (CLK4) von dem niedrigen Level zu dem hohen Level ändert,

wobei das dritte Taktsignal (CLK3) und das vierte Taktsignal (CLK4) entgegengesetzte Phasen aber die gleiche Periode besitzen, wobei die Periode des zweiten Taktsignals (CLK2) das Zweifache der des dritten Taktsignals (CLK3) beträgt, wenn sich das zweite Taktsignal (CLK2) von dem niedrigen Level zu dem hohen Level ändert, sich das dritte Taktsignal (CLK3) von dem niedrigen Level zu dem hohen Level ändert und sich das vierte Taktsignal (CLK4) von dem hohen Level zu dem niedrigen Level ändert, wobei die zweiten Taktsignale (CLK2) von benachbarten GOA-Einheiten entgegengesetzte Phasen aber die gleiche Periode besitzen.

Revendications

1. Un circuit de commande de grille(s) comprenant des unités de grille sur réseau GoA (*Gate on Array*) à plusieurs étages, le circuit de commande de grille(s) est configuré pour commander un dispositif d'affichage à cristaux liquides comprenant plusieurs rangées de pixels, chacune des unités GOA est configurée pour commander deux rangées adjacentes de pixels sur un substrat de réseau du dispositif d'affichage, l'unité GOA comprenant :

un module d'excursion haute (11) pour recevoir un signal d'entrée à une borne de signal d'entrée, recevoir un deuxième signal d'horloge (CLK2) à une deuxième borne d'entrée de signal d'horloge et fournir en sortie le deuxième signal d'horloge (CLK2) à un module de sortie (12) lorsque le signal d'entrée est à un niveau haut, dans lequel le module d'excursion haute comprend un premier dispositif de commutation (M1), un deuxième dispositif de commutation (M2), un dispositif de suralimentation (C1) et un troisième dispositif de commutation (M3), une grille et une source du premier dispositif de commutation sont tous deux reliées à la borne de signal d'entrée, et un drain du premier dispositif de commutation est relié à une source du deuxième dispositif de commutation, un point de connexion du drain du premier dispositif de commutation et de la source du deuxième dispositif de commutation est un point d'excursion haute (PU), un drain du deuxième dispositif de commutation est relié à une borne de niveau bas (VSS), une grille du deuxième dispositif de commutation est reliée à une borne d'entrée de signal de réinitialisation, une extrémité du dispositif de suralimentation est reliée à une grille du troisième dispositif de commutation et au point d'excursion haute, l'autre extrémité du dispositif de suralimentation est reliée à un drain du troisième dispositif de commutation, un point de raccordement de l'autre extrémité du dispositif de suralimentation et du drain du troisième dispositif de commutation est une borne de sortie du module d'excursion haute, une source du troisième dispositif de commutation est reliée à la borne d'entrée du deuxième signal d'horloge ;

le module de sortie (12) pour recevoir un troisième signal d'horloge (CLK3) à une troisième borne d'entrée de signal d'horloge, recevoir un quatrième signal d'horloge (CLK4) sur une quatrième borne d'entrée de signal d'horloge, et fournir en sortie le troisième signal d'horloge (CLK3) comme premier signal de commande de grille(s) pour commander une première rangée des deux rangées adjacentes de pixels et fournir en sortie le quatrième signal d'horloge (CLK4) comme

deuxième signal de commande de grille(s) pour commander une deuxième rangée des deux rangées adjacentes de pixels lorsque le deuxième signal d'horloge (CLK2) est au niveau haut ; et

un module d'excursion basse (13) pour tirer vers la bas la tension du module d'excursion haute (11), dans lequel le module d'excursion basse comprend un quatrième dispositif de commutation (M4), une grille du quatrième dispositif de commutation est reliée à la borne d'entrée du signal de réinitialisation, un drain du quatrième dispositif de commutation est relié à la borne de sortie du module d'excursion haute, une source du quatrième dispositif de commutation est reliée à la borne de niveau bas ;

caractérisé en ce que

le module de sortie (12) comprend un septième dispositif de commutation (M7), un dixième dispositif de commutation (M10) et un onzième dispositif de commutation (M11) ;

la grille du septième dispositif de commutation (M7) est reliée à la borne de sortie du module d'excursion haute (11), la source du septième dispositif de commutation (M7) est reliée à la borne d'entrée du troisième signal d'horloge, et le drain du septième dispositif de commutation (M7) est relié à une borne de sortie de premier signal de commande de grille(s) qui sort le premier signal de commande de grille(s) ;

la grille du dixième dispositif de commutation (M10) est reliée à la borne de sortie du module d'excursion haute (11), la source du dixième dispositif de commutation (M10) est reliée à la borne d'entrée du quatrième signal d'horloge, et le drain du dixième dispositif de commutation (M10) est relié à une deuxième borne de sortie de signal de commande de grille(s) qui sort le deuxième signal de commande de grille(s) ;

la grille du onzième dispositif de commutation (M11) est reliée à la borne d'entrée du quatrième signal d'horloge, la source du onzième dispositif de commutation (M11) est reliée à la première borne de sortie du signal de commande de grille(s), et le drain du onzième dispositif de commutation (M11) est relié à la borne de niveau bas, le onzième dispositif de commutation (M11) est activé pour tirer vers le bas le premier signal de commande de grille(s) lorsque le troisième signal d'horloge (CLK3) passe du niveau haut au niveau bas et le quatrième signal d'horloge (CLK4) passe du niveau bas au niveau haut.

2. Un dispositif d'affichage à cristaux liquides comprenant le circuit de commande de grille(s) selon la revendication 1.

3. Un procédé de commande de grille(s) pour comman-

der le circuit de commande de grille(s) selon la revendication 1, comprenant :

la réception, par le module d'excursion haute (11), du signal d'entrée et du deuxième signal d'horloge (CLK2), et la réception, par le module de sortie (12), du troisième signal d'horloge (CLK3) et du quatrième signal d'horloge (CLK4) ;

la sortie, par le module d'excursion haute (11), du deuxième signal d'horloge (CLK2) pour le module de sortie (12) lorsque le signal d'entrée est au niveau haut ; et

la sortie, par le septième dispositif de commutation (M7) du module de sortie (12), du troisième signal d'horloge (CLK3) comme premier signal de commande de grille(s) pour commander la première rangée de pixels et la sortie, par le dixième dispositif de commutation (M10) du module de sortie (12), du quatrième signal d'horloge (CLK4) comme deuxième signal de commande de grille(s) pour commander la deuxième rangée de pixels lorsque le deuxième signal d'horloge (CLK2) est au niveau haut ;

le tirage vers le bas, par le onzième dispositif de commutation (M11) du module de sortie (12), du premier signal de commande de grille(s) lorsque le troisième signal d'horloge (CLK3) passe du niveau haut au niveau bas et le quatrième signal d'horloge (CLK4) passe du niveau bas au niveau haut,

dans lequel le troisième signal d'horloge (CLK3) et le quatrième signal d'horloge (CLK4) ont des phases opposées mais le même cycle, le cycle du deuxième signal d'horloge (CLK2) est le double de celui du troisième signal d'horloge (CLK3), lorsque le deuxième signal d'horloge (CLK2) passe du niveau bas au niveau haut, le troisième signal d'horloge (CLK3) passe du niveau bas au niveau haut et le quatrième signal d'horloge (CLK4) passe du niveau haut au niveau bas,

les deuxième signaux d'horloge (CLK2) d'unités GOA adjacentes ont des phases opposées mais le même cycle.

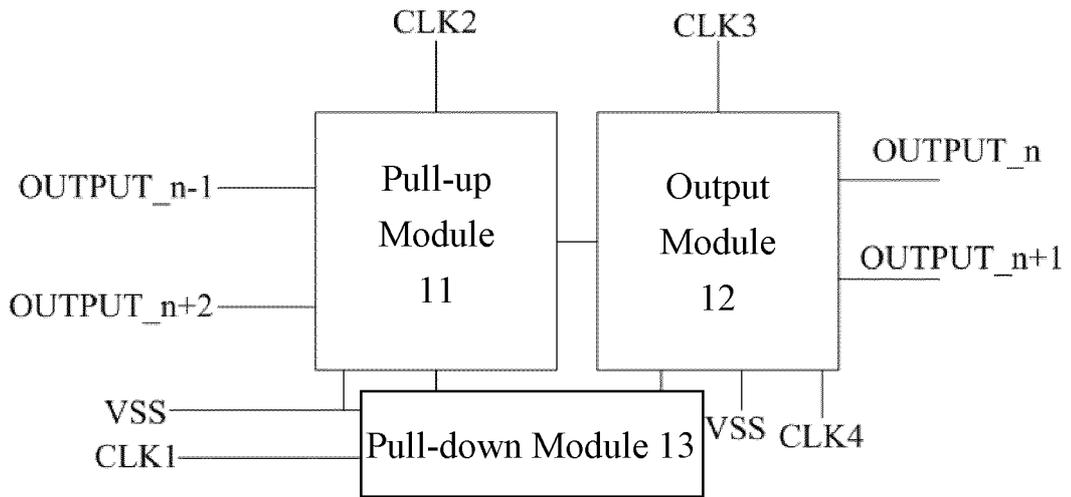


Fig.1

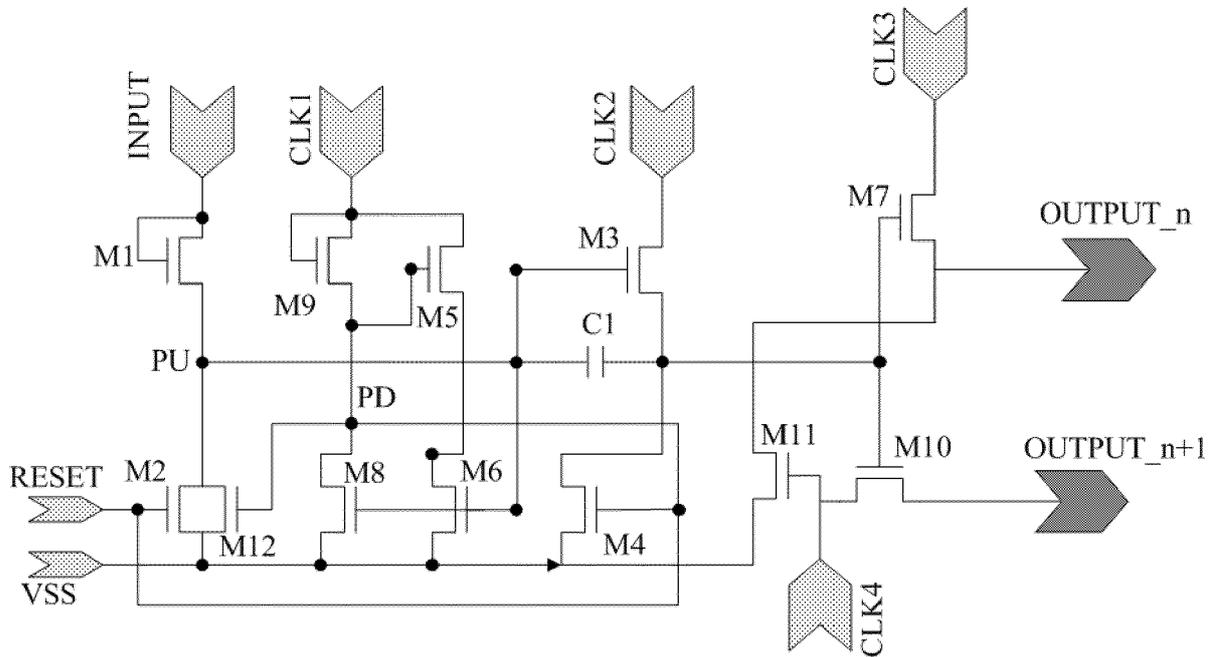


Fig.2

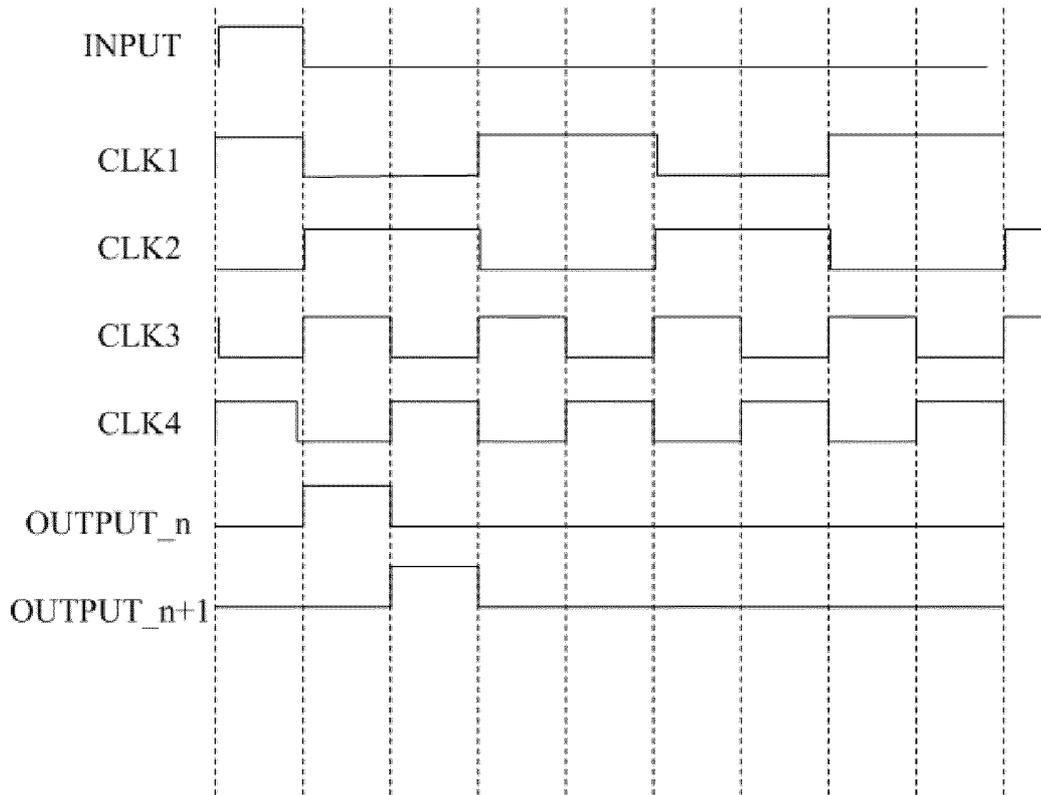


Fig.3

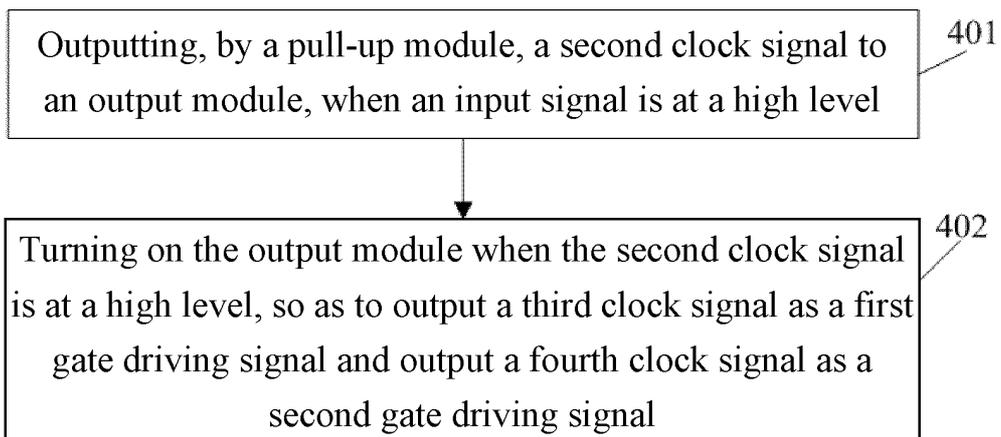


Fig.4

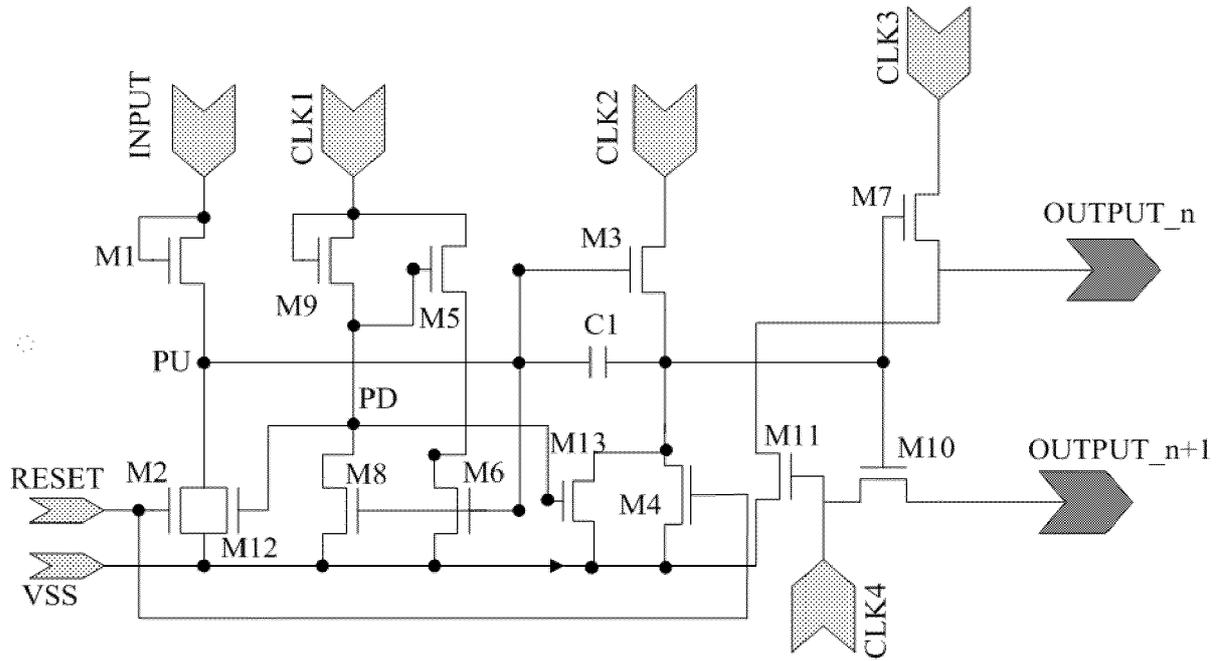


Fig.5

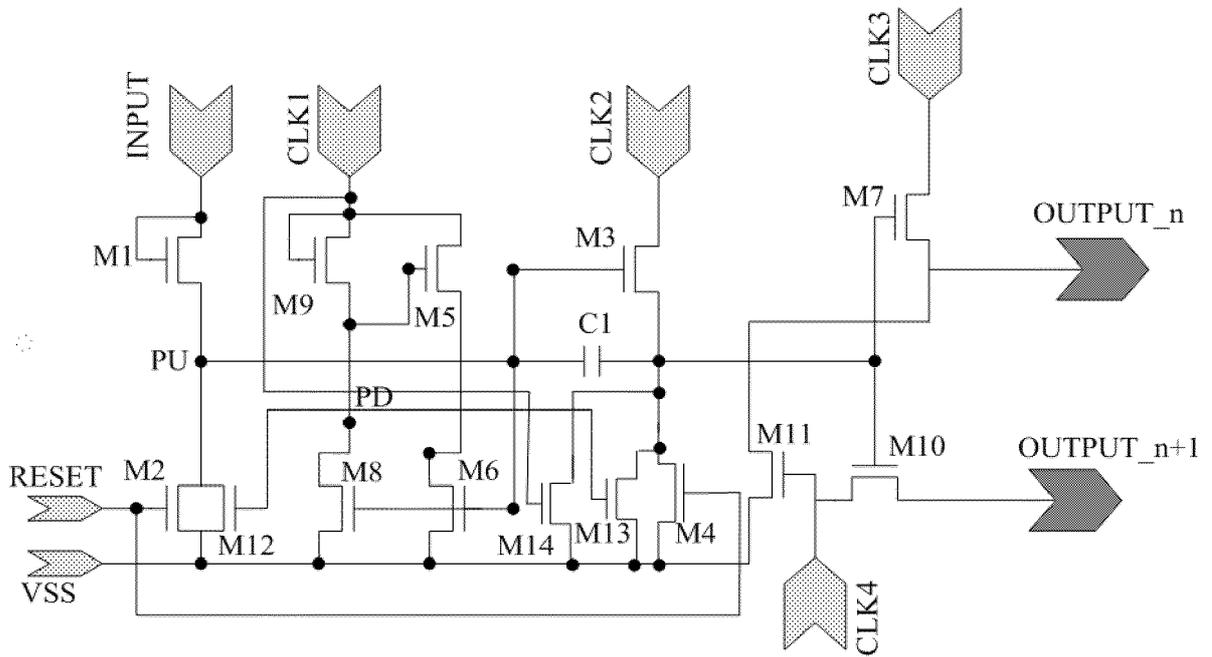


Fig.6

REFERENCES CITED IN THE DESCRIPTION

This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

Patent documents cited in the description

- EP 2400481 A1 [0003]

