(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) **EP 2 709 096 B1**

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
01.11.2017 Bulletin 2017/44

(21) Application number: **13180997.2**

(22) Date of filing: **20.08.2013**

(51) Int Cl.:
G09G 3/36 *(2006.01)* ***G11C 19/28*** *(2006.01)*

(54) Shift register unit circuit, shift register, array substrate and display apparatus

Schieberegistereinheitsschaltung, Schieberegister, Array-Substrat und Anzeigevorrichtung

Circuit d'unité de registre à décalage, registre à décalage, substrat de matrice et appareil d'affichage

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR

(30) Priority: **13.09.2012 CN 201220467195 U**

(43) Date of publication of application:
19.03.2014 Bulletin 2014/12

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EP 2 709 096 B1

Printed by Jouve, 75001 PARIS (FR)

Description

TECHNICAL FIELD OF THE DISCLOSURE

[0001] The present disclosure relates to a technical field of liquid crystal displaying, and particularly to a shift register unit circuit, a shift register, an array substrate and a display apparatus.

BACKGROUND

[0002] At present, in design of liquid crystal panel of mobile products, a shift register circuit capable of accomplishing bi-directional scanning has been widely used as a gate driving circuit and is integrated on an array substrate to achieve scanning and driving the panel, such that the cost may be saved and a design with two symmetric sides may be achieved for the panel. In addition, bonding area and fan-shaped wiring space for a gate circuit control chip may be omitted, such that a narrow frame design may be achieved, meanwhile a bonding process in the direction of gate may be omitted, which is advantageous for increasing the productivity and yield rate.

[0003] The bi-directional scanning shift register circuit includes a shift register unit circuit in a first row, a shift register unit circuit in a last row, and at least one shift register unit circuit in a middle row. A practicable shift register unit circuit in the first row is shown in Fig.1a and includes ten Thin Film Transistors and a capacitor, wherein a frame start signal (STV) input terminal is connected to a signal input terminal (INPUT). A shift register unit circuit in the last row is shown in Fig.1b, which is matched with the shift register unit circuit in the first row as shown in Fig.1a and includes ten Thin Film Transistors and a capacitor, a frame start signal input terminal is connected to a signal reset terminal (RESET). A shift register unit circuit in a middle row is shown in Fig.1c, which is matched with the shift register unit circuit in the first row as shown in Fig.1a and the shift register unit circuit in the last row as shown in Fig.1b and includes ten Thin Film Transistors and a capacitor.

[0004] When a forward scanning is performed, as shown in Fig.1d, an output signal of a shift register unit in a current row is used as an input signal of a shift register unit in a next row, and an output signal of the shift register unit in the next row is used as a reset signal of the shift register unit in the current row for resetting the shift register unit in the current row. When a reverse scanning is performed, as shown in Fig.1e, the output signal of the shift register unit in the next row is used as an input signal of the shift register of the current row, and the output signal of the shift register unit in the current row is used as a reset signal of the shift register unit in the next row for resetting the shift register unit in the next row. A timing waveform for the forward scanning is as shown in Fig.1f, in the forward scanning, when the frame start signal is at a high level, a forward clock signal (CLK) changes from a low level to a high level, the output terminal outputs a pulse of the forward clock signal; A timing waveform for the reverse scanning is as shown in Fig.1g, in the reverse scanning, when the frame start signal is at a high level, a reverse clock signal (CLKB) changes from a low level to a high level, the output terminal outputs a pulse of the reverse clock signal.

[0005] However, when the forward clock signal or the reverse clock signal changes from the low level to the high level, if the frame start signal is also at the high level, it tends to pull up the level at a node PU (pull up node) in Fig.1a, Fig.1b and Fig.1c. As shown in Fig.1h, since a size of a Thin Film Transistor TFT M01 is large, there is a large parasitic capacitance C02, and before the forward clock signal becomes the high level, the node PU keeps in the low level, as shown in Fig.1i; when the frame start signal is at the high level, the forward clock signal changes from the low level to the high level, the node PU also becomes the high level due to the parasitic capacitance of TFT M01, such that there occurs a little swell in the waveform of the node PU, also a little swell occurs in the output signal due to an coupling effect of a capacitor C01, such that a H-line defect is generated on a display screen.

[0006] In the prior art from CN 102629444 A it is known a circuit of gate drive on array, a shift register and a display screen. Further, US 2007/0248204 A1 discloses a shift register circuit and an image display apparatus equipped with the same.

SUMMARY

[0007] The invention is set forth in independent claim 1. Embodiments of the present disclosure provide a shift register unit circuit, a shift register, an array substrate and a display apparatus for removing the H-line defect of TFTs.

[0008] The embodiments of the present disclosure provide a shift register unit circuit, a shift register, an array substrate and a display apparatus, and relate to the technique of liquid crystal display. The first TFT is incorporated in the shift register unit circuit and is used to pull down the level of the node PU when the frame start signal is at the high level and the forward clock signal changes from the low level to the high level, such that the H-line defect generated in the output signal caused by the coupling effect of a coupling circuit can be avoided. In the shift register unit circuit, the shift register, the array substrate and the display apparatus provided in the embodiments of the present disclosure, it is avoided that a poor output signal is generated when the high level is output in the case that a bi-directional scanning is performed, which is advantageous for increasing productivity and yield rate of products.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] In order to explain the technical solutions in the embodiments of the present disclosure or in the prior art

more clearly, accompanying drawings required for describing the embodiments of the present disclosure or the prior art will be introduced. Obviously, the accompanying drawings below only show some embodiments of the present disclosure, and based on the accompanying drawings, other accompanying drawings can be obtained by those skilled in the art without paying inventive labor.

Fig.1a is a diagram of a shift register unit circuit in a first row in the prior art;

Fig.1b is a diagram of a shift register unit circuit in a last row in the prior art;

Fig.1c is a diagram of a shift register unit circuit in a middle row in the prior art;

Fig.1d is a diagram of a forward scanning logic circuit in the prior art;

Fig.1e is a diagram of a reverse scanning logic circuit in the prior art;

Fig.1f is a timing sequence diagram of a forward scanning in the prior art;

Fig.1g is a timing sequence diagram of a reverse scanning in the prior art;

Fig.1h is a diagram of a coupling circuit in which a parasitic capacitance exists in the prior art;

Fig.1i is a waveform diagram of a node PU in the shift register in the prior art;

Fig.2a is a diagram of a shift register unit circuit provided in embodiments of the present disclosure;

Fig.2b is a waveform diagram of a node PU in the shift register provided in the embodiments of the present disclosure;

Fig.2c is a diagram of a shift register unit circuit in a middle row provided in the embodiments of the present disclosure;

Fig.2d is a diagram of a shift register unit circuit in a first row provided in the embodiments of the present disclosure; and

Fig.2e is a diagram of a preferable shift register unit circuit in a last row provided in the embodiments of the present disclosure.

DETAILED DESCRIPTION

[0010] Descriptions will be made clearly and thoroughly for the technical solutions in the embodiments of the present disclosure below, in conjunction with the accompanying drawings of the embodiments of the present disclosure. Obviously, the described embodiments are only some but not all of the embodiments of the present disclosure. Other embodiments obtained by those skilled in the art based on the described embodiments without paying inventive labor shall belong to the scope sought for protection in the present disclosure.

[0011] Embodiments of the present disclosure relate to a technique of liquid crystal display, and provide a shift register unit circuit, a shift register, an array substrate and a display apparatus. A first TFT is incorporated in the shift register unit circuit and is used to pull down the level of a node PU when a frame start signal is at a high level and a forward clock signal changes from a low level to the high level, such that the H-line defect generated in an output signal due to the coupling effect of a coupling circuit can be avoided. In the shift register unit circuit, the shift register, the array substrate and the display apparatus provided in the embodiments of the present disclosure, it is avoided that a poor output signal is generated when a high level is output in the case that a bi-directional scanning is performed, which is advantageous for increasing productivity and yield rate of products.

[0012] As shown in Fig.2a, the shift register unit circuit provided in the embodiments of the present disclosure includes: a first Thin Film Transistor (TFT) M1 having a gate connected to a frame start signal input terminal, and a first electrode connected to a switching-off voltage signal input terminal, an operating voltage input terminal or a grounding voltage input terminal (in Fig.2a, taking a case that the first electrode is connected to the switching-off voltage signal input terminal as an example); a second TFT M2 having a gate connected to a second electrode of the first TFT M1, a second electrode connected to a forward clock signal input terminal and a first electrode connected to a signal output terminal; a third TFT M3 having a gate connected to a signal input terminal, a second electrode connected to the operating voltage input terminal and a first electrode connected to the second electrode of the first TFT M1; a fourth TFT M4 having a gate connected to a signal reset terminal, a second electrode connected to the first electrode of the third TFT M3 and a first electrode connected to the grounding voltage input terminal; a fifth TFT M5 having a gate connected to a reverse clock signal input terminal, a second electrode connected to a signal output terminal and a first electrode connected to the switching-off voltage signal input terminal; a capacitor C1 having a first electrode connected to the second electrode of the first TFT M1 and a second electrode connected to the signal output terminal.

[0013] The first TFT M1 performs a function of pulling down the level of a node PU when a frame start signal is at a high level and a forward clock signal changes from a low level to the high level, such that a H-line defect generated in an output signal due to the coupling effect of a coupling circuit will be avoided. The waveform of the node PU in the embodiments of the present disclosure is as shown in Fig.2b, when the frame start signal is at the high level, the level of the node PU is pulled down by the first TFT M1, such that the swell in the level of the node PU and the H-line defect in the output signal are suppressed.

[0014] Preferably, as shown in Fig.2a, the shift register unit circuit provided in the embodiments of the present disclosure further includes: a sixth TFT M6 having a second electrode connected to the reverse clock signal input terminal; a seventh TFT M7 having a gate connected to the first electrode of the capacitor C1, a second electrode connected to a first electrode of the sixth TFT M6 and a

first electrode connected to the switching-off voltage signal input terminal; an eighth TFT M8 having a gate connected to the first electrode of the capacitor C1 and a first electrode connected to the switching-off voltage signal input terminal; a ninth TFT M9 having a gate connected to the reverse clock signal input terminal, a second electrode connected to the reverse clock signal input terminal and a first electrode connected to a second electrode of the eighth TFT M8 and a gate of the sixth TFT M6; a tenth TFT M10 having a gate connected to the second electrode of the seventh TFT M7, a second electrode connected to the second electrode of the first TFT M1 and a first electrode connected to the switching-off voltage signal input terminal; an eleventh TFT M11 having a gate connected to the second electrode of the seventh TFT M7, a second electrode connected to the signal output terminal and a first electrode connected to the switching-off voltage signal input terminal.

[0015] A TFT shift register provided in the embodiments of the present disclosure includes at least three shift register unit circuits provided in the embodiments of the present disclosure. In the shift register unit circuit in a first row, the first electrode of the first TFT M1 is connected to the operating voltage input terminal; in the shift register unit circuit in a middle row, the first electrode of the first TFT M1 is connected to the switching-off voltage signal input terminal; and in the shift register unit circuit in a last row, the first electrode of the first TFT M1 is connected to the grounding voltage input terminal.

[0016] Preferably, as shown in Fig.2c, the shift register unit circuit in a middle row (hereinafter referred to as a middle-row shift register unit circuit) particularly includes: a middle-row first TFT M101 having a gate connected to the frame start signal input terminal, and a first electrode connected to the switching-off voltage signal input terminal, the operating voltage input terminal or the grounding voltage input terminal; a middle-row second TFT M102 having a gate connected to a second electrode of the middle-row first TFT M101, a second electrode connected to the forward clock signal input terminal and a first electrode connected to the signal output terminal; a middle-row third TFT M103 having a gate connected to the signal input terminal, a second electrode connected to the operating voltage input terminal and a first electrode connected to the second electrode of the middle-row first TFT M101; a middle-row fourth TFT M104 having a gate connected to the signal reset terminal, a second electrode connected to the first electrode of the middle-row third TFT M103 and a first electrode connected to the grounding voltage input terminal; a middle-row fifth TFT M105 having a gate connected to the reverse clock signal input terminal, a second electrode connected to the signal output terminal and a first electrode connected to the switching-off voltage signal input terminal; and a middle-row capacitor C101 having a first electrode connected to the second electrode of the middle-row first TFT M101 and a second electrode connected to the signal output terminal.

[0017] As shown in Fig.2d, the shift register unit circuit in a first row (hereinafter referred to as a first-row shift register unit circuit) particularly includes: a first-row first TFT M201 having a gate connected to the frame start signal input terminal, and a first electrode connected to the operating voltage input terminal; a first-row second TFT M202 having a gate connected to a second electrode of the first-row first TFT M201, a second electrode connected to the forward clock signal input terminal and a first electrode connected to the signal output terminal; a first-row third TFT M203 having a gate connected to the signal input terminal, a second electrode connected to the operating voltage input terminal and a first electrode connected to the second electrode of the first-row first TFT M201; a first-row fourth TFT M204 having a gate connected to the signal reset terminal, a second electrode connected to the first electrode of the first-row third TFT M203 and a first electrode connected to the grounding voltage input terminal; a first-row fifth TFT M205 having a gate connected to the reverse clock signal input terminal, a second electrode connected to the signal output terminal and a first electrode connected to the switching-off voltage signal input terminal; and a first-row capacitor C201 having a first electrode connected to the second electrode of the first-row first TFT M201 and a second electrode connected to the signal output terminal.

[0018] As shown in Fig.2e, the shift register unit circuit in a last row (hereinafter referred to as a last-row shift register unit circuit) particularly includes: a last-row first TFT M301 having a gate connected to the frame start signal input terminal, and a first electrode connected to the grounding voltage input terminal; a last-row second TFT M302 having a gate connected to a second electrode of the last-row first TFT M301, a second electrode connected to the forward clock signal input terminal and a first electrode connected to the signal output terminal; a last-row third TFT M303 having a gate connected to the signal input terminal, a second electrode connected to the operating voltage input terminal and a first electrode connected to the second electrode of the last-row first TFT M301; a last-row fourth TFT M304 having a gate connected to the signal reset terminal, a second electrode connected to the first electrode of the last-row third TFT M303 and a first electrode connected to the grounding voltage input terminal; a last-row fifth TFT M305 having a gate connected to the reverse clock signal input terminal, a second electrode connected to the signal output terminal and a first electrode connected to the switching-off voltage signal input terminal; and a last-row capacitor C301 having a first electrode connected to the second electrode of the last-row first TFT M301 and a second electrode connected to the signal output terminal.

[0019] In the first-row shift register unit circuit and the last-row shift register unit circuit provided in the embodiments of the present disclosure, the first electrode of the first-row first TFT M201 is connected to the operating voltage input terminal, the first electrode of the last-row first TFT M301 is connected to the grounding voltage

input terminal, thus ensuring that the whole TFT shift register can operate normally.

[0020] Since there are not any swells at the node PU in the first-row shift register unit circuit and the last-row shift register unit circuit, the following arrangements may be adopted in comparative examples not part of the invention:

a first-row shift register unit circuit without the first-row first TFT M201 being incorporated and a last-row shift register unit circuit without the last-row first TFT M301 being incorporated; a first-row shift register unit circuit with the first-row first TFT M201 being incorporated and a last-row shift register unit circuit without the last-row first TFT M301 being incorporated; a first-row shift register unit circuit without the first-row first TFT M201 being incorporated and a last-row shift register unit circuit with the last-row first TFT M301 being incorporated; or in an embodiment a first-row shift register unit circuit with the first-row first TFT M201 being incorporated and a last-row shift register unit circuit with the last-row first TFT M301 being incorporated.

[0021] Of course, those skilled in the art can set the first-row shift register unit circuit and the last-row shift register unit circuit by adopting other practical manners.

[0022] As shown in Fig.2c, the preferred middle-row shift register unit circuit provided in the embodiments of the disclosure includes: the middle-row first TFT M101 having the gate connected to the frame start signal input terminal, and the first electrode connected to the switching-off voltage signal input terminal; the middle-row second TFT M102 having the gate connected to the second electrode of the middle-row first TFT M101, the second electrode connected to the forward clock signal input terminal and the first electrode connected to the signal output terminal; the middle-row third TFT M103 having the gate connected to the signal input terminal, the second electrode connected to the operating voltage input terminal and the first electrode connected to the second electrode of the middle-row first TFT M101; the middle-row fourth TFT M104 having the gate connected to the signal reset terminal, the second electrode connected to the first electrode of the middle-row third TFT M103 and the first electrode connected to the grounding voltage input terminal; the middle-row fifth TFT M105 having the gate connected to the reverse clock signal input terminal, the second electrode connected to the signal output terminal and the first electrode connected to the switching-off voltage signal input terminal; and the middle-row capacitor C101 having the first electrode connected to the second electrode of the middle-row first TFT M101 and the second electrode connected to the signal output terminal.

[0023] The middle-row third TFT M103, the middle-row fourth TFT M104, the middle-row fifth TFT M105 and the middle-row second TFT M102, as well as the middle-row capacitor C101 achieve a basis shift register function together, particularly in the following manner: when the input signal is at the high level, the middle-row third TFT M103 is turned on to charge the node PU; when the forward clock signal is at the high level, the middle-row second TFT M102 is turned on, and the signal output terminal outputs a pulse of the forward clock signal, meanwhile a bootstrapping effect of the middle-row capacitor C101 further pulls up the level of the node PU; then the middle-row fourth TFT M104 and the middle-row fifth TFT M105 are turned on by the reset signal to discharge the node PU and the signal output terminal, thus achieving the basis shift register function. Of course, those skilled in the art can adopt other practical manner to achieve the basis register function.

[0024] Preferably, the middle-row shift register unit circuit further includes: a middle-row sixth TFT M106 having a second electrode connected to the reverse clock signal input terminal; a middle-row seventh TFT M107 having a gate connected to the first electrode of the middle-row capacitor C101, a second electrode connected to a first electrode of the middle-row sixth TFT M106 and a first electrode connected to the switching-off voltage signal input terminal; a middle-row eighth TFT M108 having a gate connected to the first electrode of the middle-row capacitor C101 and a first electrode connected to the switching-off voltage signal input terminal; a middle-row ninth TFT M109 having a gate connected to the reverse clock signal input terminal, a second electrode connected to the reverse clock signal input terminal and a first electrode connected to a second electrode of the middle-row eighth TFT M108 and a gate of the middle-row sixth TFT M106; a middle-row tenth TFT M110 having a gate connected to the second electrode of the middle-row seventh TFT M107, a second electrode connected to the second electrode of the middle-row first TFT M101 and a first electrode connected to the switching-off voltage signal input terminal; a middle-row eleventh TFT M111 having a gate connected to the second electrode of the middle-row seventh TFT M107, a second electrode connected to the signal output terminal and a first electrode connected to the switching-off voltage signal input terminal.

[0025] As shown in Fig.2d, the first-row shift register unit circuit provided in the embodiments of the present disclosure includes: the first-row first TFT M201 having the gate connected to the frame start signal input terminal, and the first electrode connected to the operating voltage input terminal; the first-row second TFT M202 having the gate connected to the second electrode of the first-row first TFT M201, the second electrode connected to the forward clock signal input terminal and the first electrode connected to the signal output terminal; the first-row third TFT M203 having the gate connected to the signal input terminal, the second electrode connected to the operating voltage input terminal and the first electrode connected to the second electrode of the first-row first TFT M201; the first-row fourth TFT M204 having the gate connected to the signal reset terminal, the second

electrode connected to the first electrode of the first-row third TFT M203 and the first electrode connected to the grounding voltage input terminal; the first-row fifth TFT M205 having the gate connected to the reverse clock signal input terminal, the second electrode connected to the signal output terminal and the first electrode connected to the switching-off voltage signal input terminal; and the first-row capacitor C201 having the first electrode connected to the second electrode of the first-row first TFT M201 and the second electrode connected to the signal output terminal.

[0026] The first-row third TFT M203, the first-row fourth TFT M204, the first-row fifth TFT M205 and the first-row second TFT M202, as well as the first-row capacitor C201 achieve a basis shift register function together, particularly in the following manner: when the input signal is at the high level, the first-row third TFT M203 is turned on to charge the node PU; when the forward clock signal is at the high level, the first-row second TFT M202 is turned on, and the signal output terminal outputs a pulse of the forward clock signal, meanwhile a bootstrapping effect of the first-row capacitor C201 further pulls up the level of the node PU; then the first-row fourth TFT M204 and the first-row fifth TFT M205 are turned on by the reset signal to discharge the node PU and the signal output terminal, thus achieving the basis shift register function. Of course, those skilled in the art can adopt other practical manners to achieve the basis register function.

[0027] Preferably, the first-row shift register unit circuit further includes: a first-row sixth TFT M206 having a second electrode connected to the reverse clock signal input terminal; a first-row seventh TFT M207 having a gate connected to the first electrode of the first-row capacitor C201, a second electrode connected to a first electrode of the first-row sixth TFT M206 and a first electrode connected to the switching-off voltage signal input terminal; a first-row eighth TFT M208 having a gate connected to the first electrode of the first-row capacitor C201 and a first electrode connected to the switching-off voltage signal input terminal; a first-row ninth TFT M209 having a gate connected to the reverse clock signal input terminal, a second electrode connected to the reverse clock signal input terminal and a first electrode connected to a second electrode of the first-row eighth TFT M208 and a gate of the first-row sixth TFT M206; a first-row tenth TFT M210 having a gate connected to the second electrode of the first-row seventh TFT M207, a second electrode connected to the second electrode of the first-row first TFT M201 and a first electrode connected to the switching-off voltage signal input terminal; a first-row eleventh TFT M211 having a gate connected to the second electrode of the first-row seventh TFT M207, a second electrode connected to the signal output terminal and a first electrode connected to the switching-off voltage signal input terminal.

[0028] As shown in Fig.2e, the last-row shift register unit circuit provided in the embodiments of the present disclosure includes: the last-row first TFT M301 having the gate connected to the frame start signal input terminal, and the first electrode connected to the grounding voltage input terminal; the last-row second TFT M302 having the gate connected to the second electrode of the last-row first TFT M301, the second electrode connected to the forward clock signal input terminal and the first electrode connected to the signal output terminal; the last-row third TFT M303 having the gate connected to the signal input terminal, the second electrode connected to the operating voltage input terminal and the first electrode connected to the second electrode of the last-row first TFT M301; the last-row fourth TFT M304 having the gate connected to the signal reset terminal, the second electrode connected to the first electrode of the last-row third TFT M303 and the first electrode connected to the grounding voltage input terminal; the last-row fifth TFT M305 having the gate connected to the reverse clock signal input terminal, the second electrode connected to the signal output terminal and the first electrode connected to the switching-off voltage signal input terminal; and the last-row capacitor C301 having the first electrode connected to the second electrode of the last-row first TFT M301 and the second electrode connected to the signal output terminal.

[0029] The last-row third TFT M303, the last-row fourth TFT M304, the last-row fifth TFT M305 and the last-row second TFT M302, as well as the last-row capacitor C301 achieve a basis shift register function together, particularly in the following manner: when the input signal is at the high level, the last-row third TFT M303 is turned on to charge the node PU; when the forward clock signal is at the high level, the last-row second TFT M302 is turned on, and the signal output terminal outputs a pulse of the forward clock signal, meanwhile a bootstrapping effect of the last-row capacitor C301 further pulls up the level of the node PU; then the last-row fourth TFT M304 and the last-row fifth TFT M305 are turned on by the reset signal to discharge the node PU and the signal output terminal, thus achieving the basis shift register function. Of course, those skilled in the art can adopt other practical manners to achieve the basis register function.

[0030] Preferably, the last-row shift register unit circuit further includes: a last-row sixth TFT M306 having a second electrode connected to the reverse clock signal input terminal; a last-row seventh TFT M307 having a gate connected to the first electrode of the last-row capacitor C301, a second electrode connected to a first electrode of the last-row sixth TFT M306 and a first electrode connected to the switching-off voltage signal input terminal; a last-row eighth TFT M308 having a gate connected to the first electrode of the last-row capacitor C301 and a first electrode connected to the switching-off voltage signal input terminal; a last-row ninth TFT M309 having a gate connected to the reverse clock signal input terminal, a second electrode connected to the reverse clock signal input terminal and a first electrode connected to a second electrode of the last-row eighth TFT M308 and a gate of the last-row sixth TFT M306; a last-row tenth TFT M310 having a gate connected to the second electrode of the

last-row seventh TFT M307, a second electrode connected to the second electrode of the last-row first TFT M301 and a first electrode connected to the switching-off voltage signal input terminal; and a last-row eleventh TFT M311 having a gate connected to the second electrode of the last-row seventh TFT M307, a second electrode connected to the signal output terminal and a first electrode connected to the switching-off voltage signal input terminal.

[0031] When the TFT shift register provided in the embodiments of the present disclosure performs a forward scanning, the operating voltage input terminal is connected to a positive electrode of a power supply, the grounding voltage input terminal is connected to a negative electrode of the power supply; when the TFT shift register provided in the embodiments of the present disclosure performs a reverse scanning, the operating voltage input terminal is connected to a negative electrode of a power supply, the grounding voltage input terminal is connected to a positive electrode of the power supply. In other words, the shift register provided in the embodiments of the present disclosure can perform a bi-directional driving by exchanging the polarities of the power supply connected to the operating voltage input terminal and the grounding voltage input terminal respectively.

[0032] The array substrate provided in the embodiment of the present disclosure includes the TFT shift register provided in the embodiments of the present disclosure.

[0033] The display apparatus provided in the embodiment of the present disclosure includes the TFT shift register provided in the embodiments of the present disclosure.

[0034] The embodiments of the present disclosure relate to the technique of liquid crystal display, and provide a shift register unit circuit, a shift register, an array substrate and a display apparatus. The first TFT is incorporated in the shift register unit circuit and is used to pull down the level of the node PU when the frame start signal is at the high level and the forward clock signal changes from the low level to the high level, such that the H-line defect generated in the output signal caused by the coupling effect of a coupling circuit can be avoided. In the shift register unit circuit, the shift register, the array substrate and the display apparatus provided in the embodiments of the present disclosure, it is avoided that a poor output signal is generated when the high level is output in the case that a bi-directional scanning is performed, which is advantageous for increasing productivity and yield rate of products.

[0035] The above descriptions are only for illustrating the embodiments of the present disclosure, and in no way limit the scope of the present disclosure. It will be obvious that those skilled in the art may make modifications, variations and equivalences to the above embodiments without departing the scope of the present invention as defined by the following claims. Such variations and modifications are intended to be included within the scope of the present invention.

Claims

1. A shift register for scanning a display device including at least three shift register unit circuits, wherein each of the at least three shift register unit circuits comprises:

   a first Thin Film Transistor TFT (M101; M201; M301) having a gate connected to a frame start signal input terminal (STV), a first electrode configured to be connected to a switching-off voltage signal input terminal (VGL), an operating voltage input terminal (VDD) or a grounding voltage input terminal (VSS) according to a position where the shift register unit circuit is located in the shift register, and a second electrode connected to a pull-up node (PU);
   a second TFT (M102 ;M202; M302) having a gate connected to a second electrode of the first TFT, a second electrode connected to a forward clock signal input terminal (CLK), and a first electrode connected to a signal output terminal (OUTPUT);
   a third TFT (M103; M203; M303) having a gate connected to a signal input terminal (INPUT), a second electrode connected to the operating voltage input terminal (VDD), and a first electrode connected to the second electrode of the first TFT;
   a fourth TFT (M104; M204; M304) having a gate connected to a signal reset terminal (RESET), a second electrode connected to the first electrode of the third TFT, and a first electrode connected to the grounding voltage input terminal (VSS);
   a fifth TFT (M105; M205; M305) having a gate connected to a reverse clock signal input terminal (CLKB), a second electrode connected to the signal output terminal (OUTPUT), and a first electrode connected to the switching-off voltage signal input terminal (VGL); and
   a capacitor (C101; C201; C301) having a first electrode connected to the second electrode of the first TFT and a second electrode connected to the signal output terminal (OUTPUT);
   wherein when the shift register unit circuit is located at a first position of the shift register, corresponding to a first row of the display device, the first electrode of the first TFT is connected to the operating voltage input terminal; when the shift register unit circuit is located at a middle position of the shift register, corresponding to a middle row of said display device, the first electrode of the first TFT is connected to the switching-off voltage signal input terminal; and when

the shift register unit circuit is located at a last position of the shift register, corresponding to a last row of said display device, the first electrode of the first TFT is connected to the grounding voltage input terminal.

2. The shift register of claim 1, wherein each of the at least three shift register unit circuits further comprises:

a sixth TFT (M106; M206; M306) having a second electrode connected to the reverse clock signal input terminal (CLKB);
a seventh TFT (M107; M207; M307) having a gate connected to the first electrode of the capacitor, a second electrode connected to a first electrode of the sixth TFT, and a first electrode connected to the switching-off voltage signal input terminal (VGL);
an eighth TFT (M108; M208; M308) having a gate connected to the first electrode of the capacitor and a first electrode connected to the switching-off voltage signal input terminal (VGL);
a ninth TFT (M109; M209; M309) having a gate connected to the reverse clock signal input terminal (CLKB), a second electrode connected to the reverse clock signal input terminal (CLKB), and a first electrode connected to a second electrode of the eighth TFT and a gate of the sixth TFT;
a tenth TFT (M110; M210; M310) having a gate connected to the second electrode of the seventh TFT, a second electrode connected to the second electrode of the first TFT, and a first electrode connected to the switching-off voltage signal input terminal (VGL); and
an eleventh TFT (M111; M211; M311) having a gate connected to the second electrode of the seventh TFT, a second electrode connected to the signal output terminal (OUTPUT), and a first electrode connected to the switching-off voltage signal input terminal (VGL).

3. The shift register of claim 1 or 2, wherein the first electrode of the TFTs is source and the second electrode of the TFTs is drain, and the first electrode of the capacitor is a positive electrode and the second electrode of the capacitor is a negative electrode.

4. The shift register of any one of claims 1-3, wherein when the shift register performs a forward scanning, the operating voltage input terminal is connected to a positive electrode of a power supply, the grounding voltage input terminal is connected to a negative electrode of the power supply; when the shift register performs a reverse scanning, the operating voltage input terminal is connected to the negative electrode of the power supply, the grounding voltage input terminal is connected to the positive electrode of the power supply.

5. An array substrate including the shift register of any of claims 1-4.

6. A display apparatus including the shift register of any of claims 1-4.

Patentansprüche

1. Schieberegister zum Scannen einer Anzeigevorrichtung, beinhaltend zumindest drei Schieberegistereinheitschaltungen, wobei jede der zumindest drei Schieberegistereinheitschaltungen umfasst:

einen ersten Dünnschichttransistor TFT (M101; M201; M301), aufweisend ein Gate, verbunden mit einem Frame-Startsignaleingabeanschluss (STV), eine erste Elektrode, die konfiguriert ist, um mit einem Ausschaltspannungssignaleingabeanschluss (VGL), einem Betriebsspannungseingabeanschluss (VDD) oder einem Erdungsspannungseingabeanschluss (VSS) verbunden zu sein, gemäß einer Position wo die Schieberegistereinheitschaltung in dem Schieberegister lokalisiert ist, und eine zweite Elektrode, die mit einem Pull-Up-Knoten (PU) verbunden ist;
einen zweiten TFT (M102; M202; M302), aufweisend ein Gate, das mit einer zweiten Elektrode des ersten TFTs verbunden ist, eine zweite Elektrode, die mit einem Vorwärtstaktsignaleingabeanschluss (CLK) verbunden ist, und eine erste Elektrode, die mit einem Signalausgabeanschluss (OUTPUT) verbunden ist;
einen dritten TFT (M103, M203; M303), aufweisend ein Gate, das mit einem Signaleingabeanschluss (INPUT) verbunden ist, eine zweite Elektrode, die mit dem Betriebsspannungseingabeanschluss (VDD) verbunden ist, und eine erste Elektrode, die mit der zweiten Elektrode des ersten TFTs verbunden ist;
einen vierten TFT (M104, M204; M304), aufweisend ein Gate, das mit einem Signalrücksetzanschluss (RESET) verbunden ist, eine zweite Elektrode, die mit der ersten Elektrode des dritten TFTs verbunden ist, und eine erste Elektrode, die mit dem Erdungsspannungseingabeanschluss (VSS) verbunden ist;
einen fünften TFT (M105; M205; M305), aufweisend ein Gate, das mit einem Umkehrtaktsignaleingabeanschluss (CLKB) verbunden ist, eine zweite Elektrode, die mit dem Signalausgabeanschluss (OUTPUT) verbunden ist, und eine erste Elektrode, die mit dem Ausschaltspannungssignaleingabeanschluss (VGL) verbun-

den ist; und
einen Kondensator (C101; C201; C301), aufweisend eine erste Elektrode, die mit der zweiten Elektrode des ersten TFTs verbunden ist, und eine zweite Elektrode, die mit dem Signalausgabeanschluss (OUTPUT) verbunden ist; wobei,
wenn die Schieberegistereinheitschaltung an einer ersten Position des Schieberegisters, entsprechend einer ersten Reihe der Anzeigevorrichtung, angeordnet ist, die erste Elektrode des ersten TFTs mit dem Betriebsspannungseingabeanschluss verbunden ist;
wenn die Schieberegistereinheitschaltung an einer mittleren Position des Schieberegisters, entsprechend einer mittleren Reihe der Anzeigevorrichtung, lokalisiert ist, die erste Elektrode des ersten TFTs mit dem Ausschaltspannungssignaleingabeanschluss verbunden ist; und
wenn die Schieberegistereinheitschaltung in einer letzten Position des Schieberegisters, entsprechend einer letzten Reihe der Anzeigevorrichtung, lokalisiert ist, die erste Elektrode des ersten TFTs mit dem Erdungsspannungseingabeanschluss verbunden ist.

2. Schieberegister gemäß Anspruch 1, wobei jede der zumindest drei Schieberegistereinheitschaltungen außerdem umfasst:

einen sechsten TFT (M106; M206; M306), aufweisend eine zweite Elektrode, die mit dem Umkehrtaktsignaleingabeanschluss (CLKB) verbunden ist;
einen siebten TFT (M107; M207; M307), aufweisend ein Gate, das mit der ersten Elektrode des Kondensators verbunden ist, eine zweite Elektrode, die mit einer ersten Elektrode des sechsten TFTs verbunden ist, und eine erste Elektrode, die mit dem Ausschaltspannungssignaleingabeanschluss (VGL) verbunden ist;
einen achten TFT (M108, M208; M308), aufweisend ein Gate, das mit der ersten Elektrode des Kondensators verbunden ist, und eine erste Elektrode, die mit dem Ausschaltspannungssignaleingabeanschluss (VGL) verbunden ist;
einen neunten TFT (M109; M209; M309), aufweisend ein Gate, das mit dem Umkehrtaktsignaleingabeanschluss (CLKB) verbunden ist, eine zweite Elektrode, die mit dem Umkehrtaktsignaleingabeanschluss (CLKB) verbunden ist, und eine erste Elektrode, die mit einer zweiten Elektrode des achten TFTs und einem Gate des sechsten TFTs verbunden ist;
einen zehnten TFT (M110; M210; M310), aufweisend ein Gate, das mit der zweiten Elektrode des siebten TFTs verbunden ist, eine zweite Elektrode, die mit der zweiten Elektrode des ersten TFTs verbunden ist, und eine erste Elektrode, die mit dem Ausschaltspannungssignaleingabeanschluss (VGL) verbunden ist; und
einen elften TFT (M111, M211M M311), aufweisend ein Gate, das mit der zweiten Elektrode des siebten TFTs verbunden ist, eine zweite Elektrode, die mit dem Signalausgabeanschluss (OUTPUT) verbunden ist, und eine erste Elektrode, die mit dem Ausschaltspannungssignaleingabeschluss (VGL) verbunden ist.

3. Schieberegister gemäß Anspruch 1 oder Anspruch 2, wobei die erste Elektrode des TFTs eine Source ist und wobei die zweite Elektrode des TFTs ein Drain ist, und wobei die erste Elektrode des Kondensators eine positive Elektrode ist und die zweite Elektrode des Kondensators eine negative Elektrode ist.

4. Schieberegister gemäß einem der Ansprüche 1 bis 3, wobei, wenn das Schieberegister einen Vorwärts-Scan ausführt, der Betriebsspannungseingabeanschluss verbunden ist mit einer positiven Elektrode der Energiezufuhr und der Erdungsspannungseingabeanschluss verbunden ist mit einer negativen Elektrode der Energiezufuhr; wenn das Schieberegister einen Rückwärts-Scan ausführt, der Betriebsspannungseingabeanschluss verbunden ist mit der negativen Elektrode der Energiezufuhr und der Erdungsspannungseingabeanschluss verbunden ist mit der positiven Elektrode der Energiezufuhr.

5. Array-Substrat, aufweisend das Schieberegister gemäß einem der Ansprüche 1 bis 4.

6. Anzeigevorrichtung, aufweisend das Schieberegister gemäß einem der Ansprüche 1 bis 4.

Revendications

1. Un registre à décalage pour balayer un dispositif d'affichage, comprenant au moins trois circuits d'unité de registre à décalage, dans lequel chacun des au moins trois circuits d'unité de registre à décalage comprend :

un premier transistor à film mince TFT (M101 ; M201 ; M301) ayant une grille connectée à une borne d'entrée de signal de début de trame (STV), une première électrode configurée pour être connectée à une borne d'entrée de signal de tension de coupure (VGL), une borne d'entrée de tension de fonctionnement (VDD) ou une borne d'entrée de tension de masse (VSS) selon une position à laquelle le circuit d'unité de registre à décalage est situé dans le registre à décalage, et une deuxième électrode connectée à un noeud d'excursion haute (PU) ;

un deuxième TFT (M102 ; M202 ; M302) ayant une grille connectée à une deuxième électrode du premier TFT, une deuxième électrode connectée à une borne d'entrée de signal d'horloge directe (CLK) et une première électrode connectée à une borne de sortie de signal (OUTPUT) ;
un troisième TFT (M103 ; M203 ; M303) ayant une grille connectée à une borne d'entrée de signal (INPUT), une deuxième électrode connectée à la borne d'entrée de tension de fonctionnement (VDD), et une première électrode connectée à la deuxième électrode du premier TFT ;
un quatrième TFT (M104 ; M204 ; M304) ayant une grille connectée à une borne de réinitialisation de signal (RESET), une deuxième électrode connectée à la première électrode du troisième TFT, et une première électrode connectée à la borne d'entrée de tension de masse (VSS) ;
un cinquième TFT (M105 ; M205 ; M305) ayant une grille connectée à une borne d'entrée de signal d'horloge inverse (CLKB), une deuxième électrode connectée à la borne de sortie de signal (OUTPUT), et une première électrode connectée à la borne d'entrée de signal de tension de coupure (VGL) ; et
un condensateur (C101 ; C201 ; C301) ayant une première électrode connectée à la deuxième électrode du premier TFT et une deuxième électrode connectée à la borne de sortie de signal (OUTPUT) ;
dans lequel lorsque le circuit d'unité de registre à décalage est situé à une première position du registre à décalage correspondant à une première colonne du dispositif d'affichage, la première électrode du premier TFT est connectée à la borne d'entrée de tension de fonctionnement ; lorsque le circuit d'unité de registre à décalage est situé à une position médiane du registre à décalage correspondant à une colonne médiane du dispositif d'affichage, la première électrode du premier TFT est connectée à la borne d'entrée de signal de tension de coupure ; et lorsque le circuit d'unité de registre à décalage est situé à une dernière position du registre à décalage correspondant à une dernière colonne du dispositif d'affichage, la première électrode du premier TFT est connectée à la borne d'entrée de tension de masse.

2. Le registre à décalage de la revendication 1, dans lequel chacun des au moins trois circuits d'unité de registre à décalage comprend en outre :

un sixième TFT (M106 ; M206 ; M306) ayant une deuxième électrode connectée à la borne d'entrée de signal d'horloge inverse (CLKB) ;
un septième TFT (M107 ; M207 ; M307) ayant une grille connectée à la première électrode du condensateur, une deuxième électrode connectée à une première électrode du sixième TFT, et une première électrode connectée à la borne d'entrée de signal de tension de coupure (VGL) ;
un huitième TFT (M108 ; M208 ; M308) ayant une grille connectée à la première électrode du condensateur et une première électrode connectée à la borne d'entrée de signal de tension de coupure (VGL) ;
un neuvième TFT (M109 ; M209 ; M309) ayant une grille connectée à la borne d'entrée de signal d'horloge inverse (CLKB), une deuxième électrode connectée à la borne d'entrée de signal d'horloge inverse (CLKB), et une première électrode connectée à une deuxième électrode du huitième TFT et une grille du sixième TFT ;
un dixième TFT (M110 ; M210 ; M310) ayant une grille connectée à la deuxième électrode du septième TFT, une deuxième électrode connectée à la deuxième électrode du premier TFT, et une première électrode connectée à la borne d'entrée de signal de tension de coupure (VGL) ; et
un onzième TFT (M111 ; M211 ; M311) ayant une grille connectée à la deuxième électrode du septième TFT, une deuxième électrode connectée à la borne de sortie de signal (OUTPUT), et une première électrode connectée à la borne d'entrée de signal de tension de coupure (VGL).

3. Le registre à décalage de la revendication 1 ou 2, dans lequel la première électrode des TFTs est une source et la deuxième électrode des TFTs est un drain, et la première électrode du condensateur est une électrode positive et la deuxième électrode du condensateur est une électrode négative.

4. Le registre à décalage de l'une quelconque des revendications 1 à 3, dans lequel lorsque le registre à décalage TFT effectue un balayage vers l'avant, la borne d'entrée de tension de fonctionnement est connectée à une électrode positive d'une alimentation électrique, la borne d'entrée de tension de masse est connectée à une électrode négative de l'alimentation électrique ; lorsque le registre à décalage effectue un balayage inverse, la borne d'entrée de tension de fonctionnement est connectée à l'électrode négative de l'alimentation électrique, la borne d'entrée de tension de masse est connectée à l'électrode positive de l'alimentation électrique.

5. Un substrat de réseau comprenant le registre à décalage de l'une quelconque des revendications 1 à 4.

6. Un appareil d'affichage comprenant le registre à décalage de l'une quelconque des revendications 1 à 4.

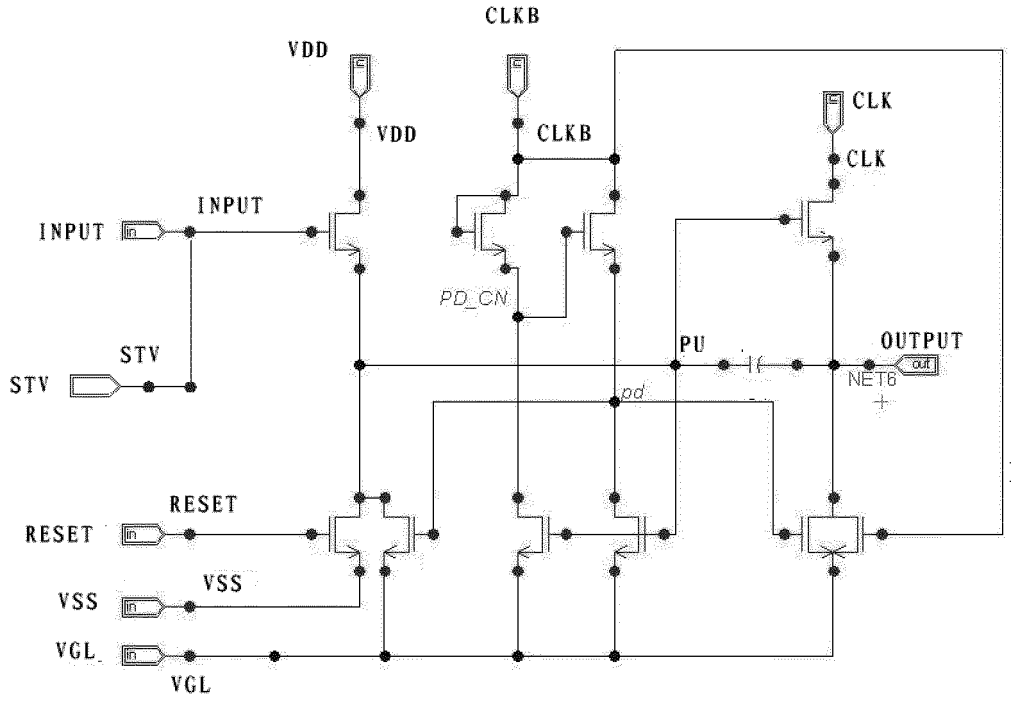
CLKB
VDD
VDD
CLKB
CLK
CLK
INPUT
INPUT
INPUT
PD_CN
STV
STV
PU
OUTPUT
NET6
pd
RESET
RESET
VSS
VSS
VGL
VGL

Fig.1a

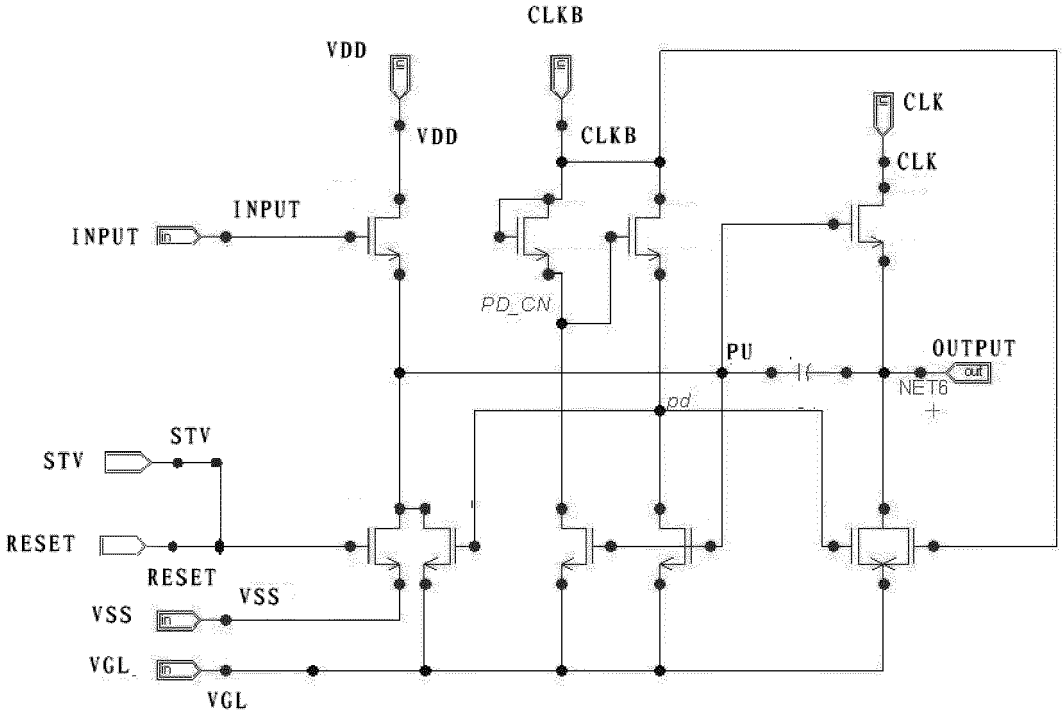
CLKB
VDD
VDD
CLKB
CLK
CLK
INPUT
INPUT
PD_CN
PU
OUTPUT
NET6
pd
STV
STV
RESET
RESET
VSS
VSS
VGL
VGL

Fig.1b

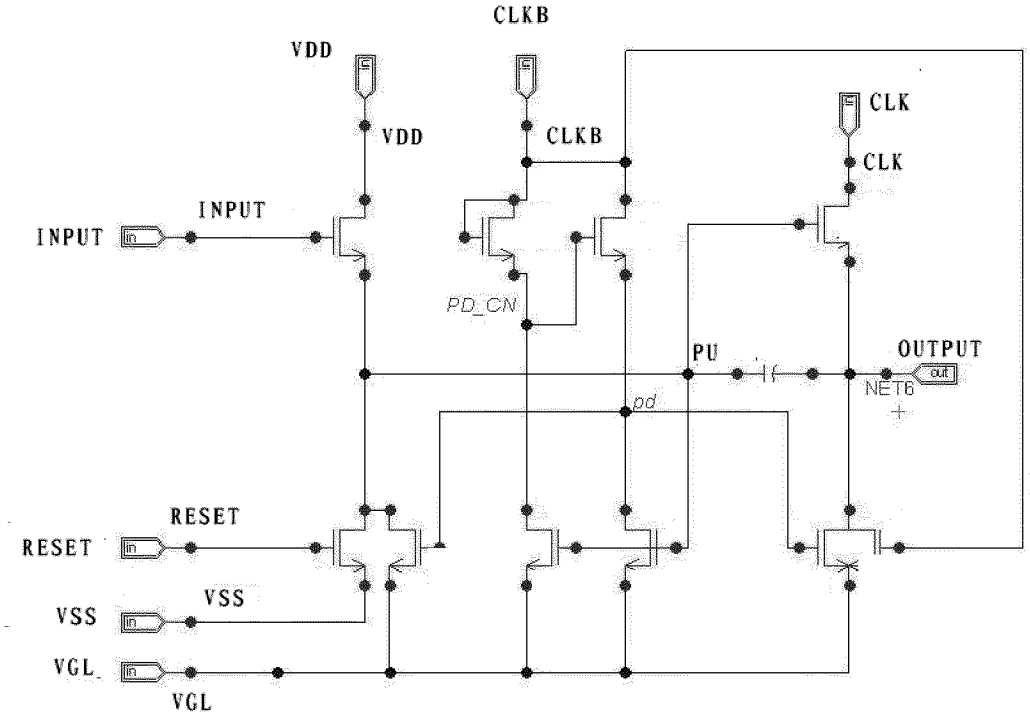
CLKB
VDD
VDD
CLKB
CLK
CLK
INPUT
INPUT
PD_CN
PU
OUTPUT
NET6
pd
RESET
RESET
VSS
VSS
VGL
VGL

Fig.1c

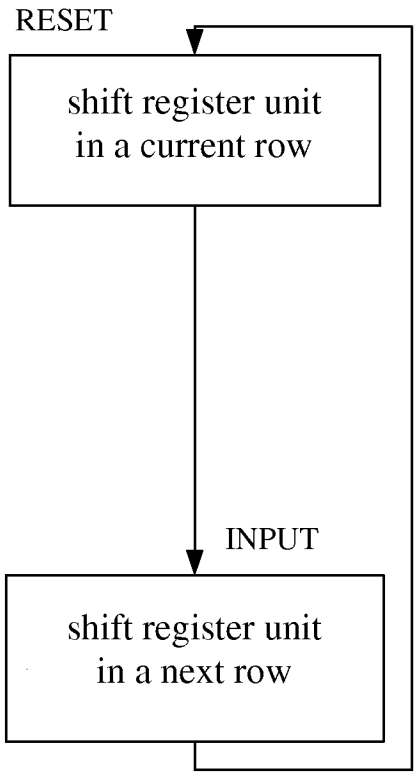
RESET
shift register unit in a current row
INPUT
shift register unit in a next row

Fig.1d

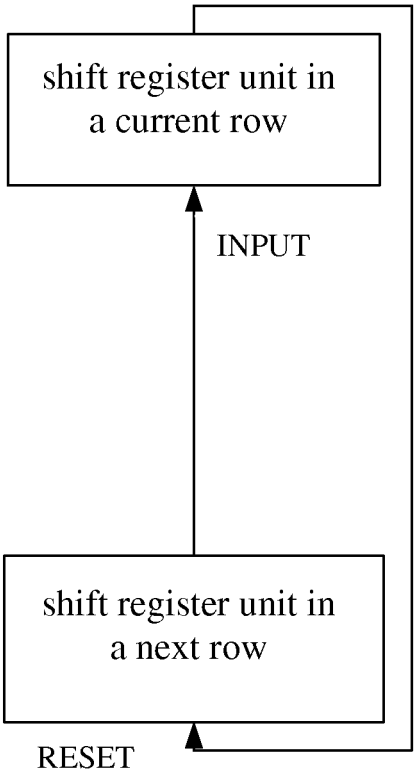
shift register unit in a current row
INPUT
shift register unit in a next row
RESET

Fig.1e

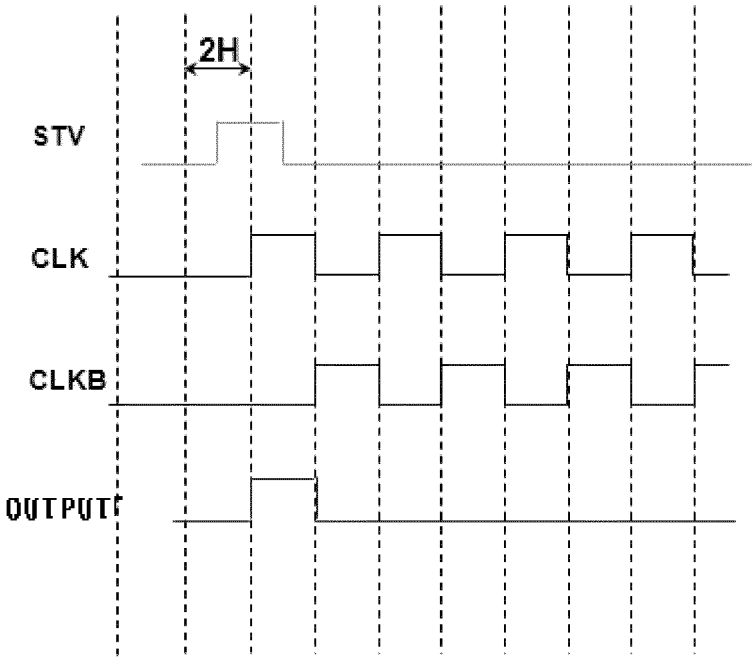
2H
STV
CLK
CLKB
OUTPUT

Fig.1f

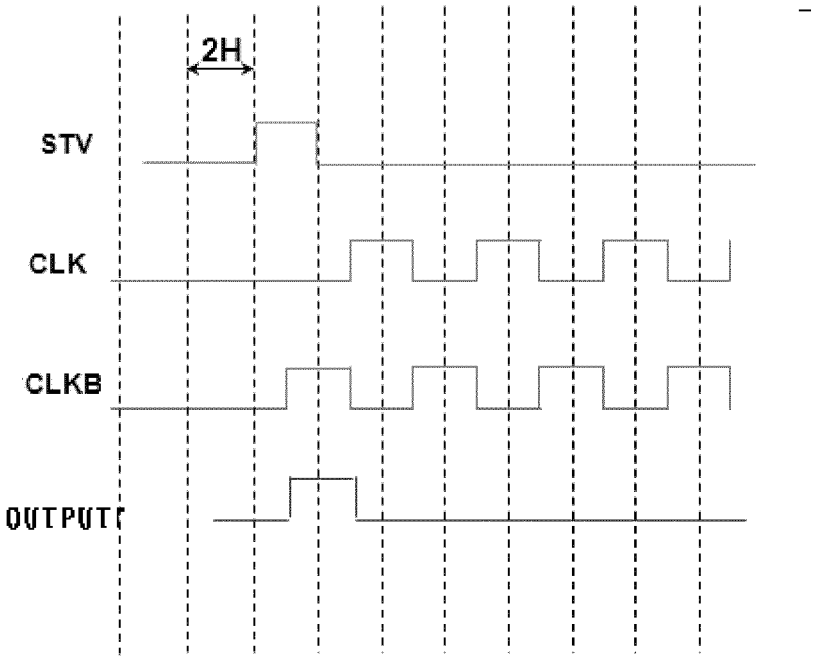

Fig.1g

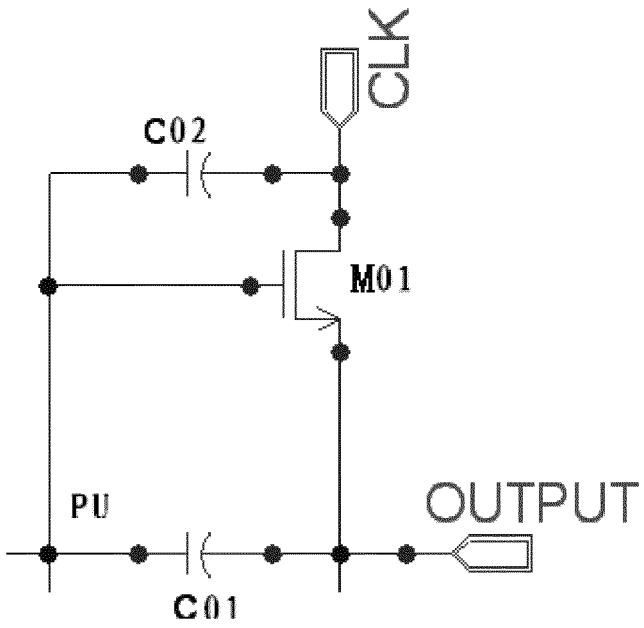

Fig.1h

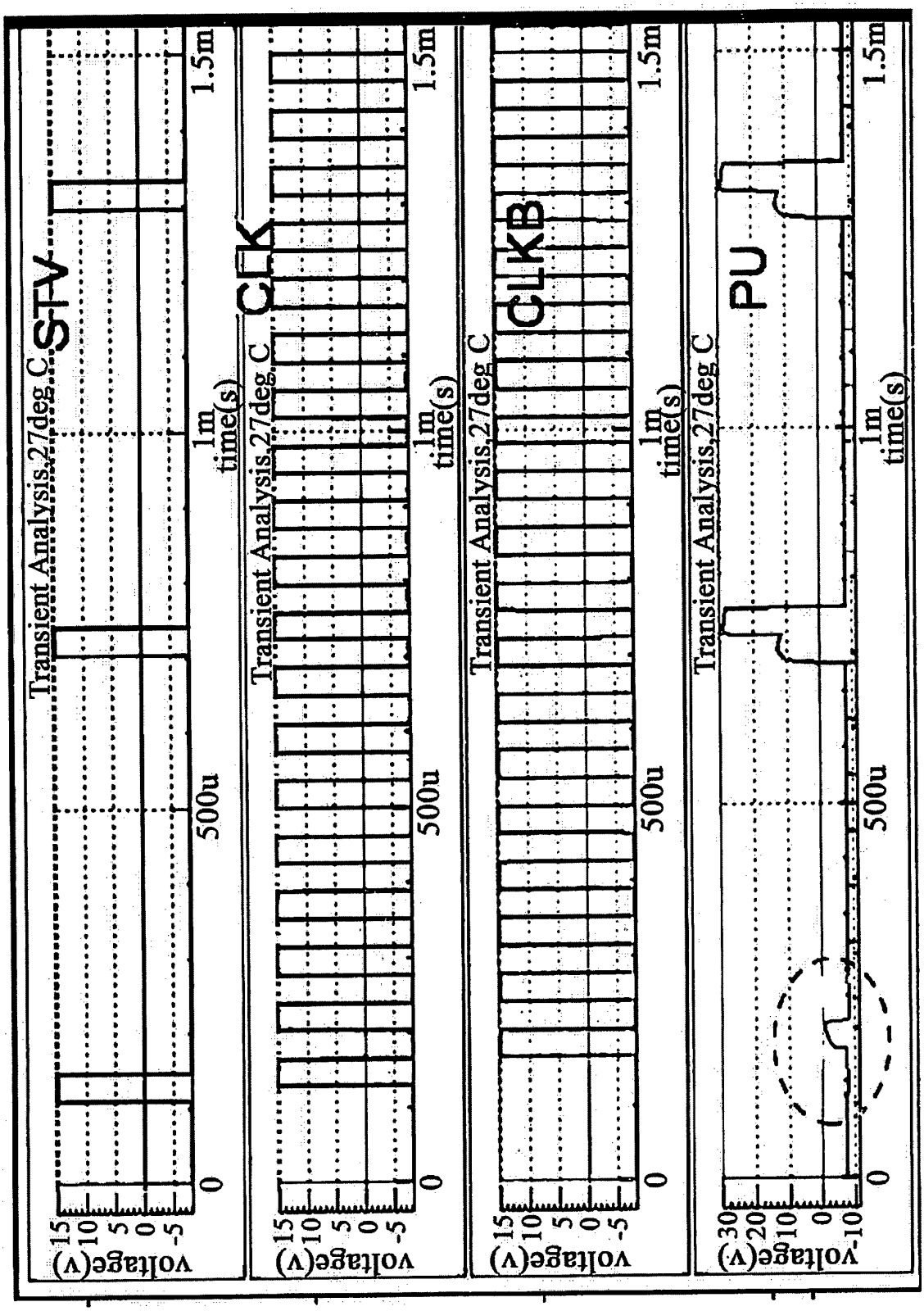
Transient Analysis,27deg C
STV
CLK
CLKB
PU
Voltage(V)
time(s)
0
500u
1m
1.5m
15
10
5
0
-5
30
20
10
0
-10

FIG. 1i

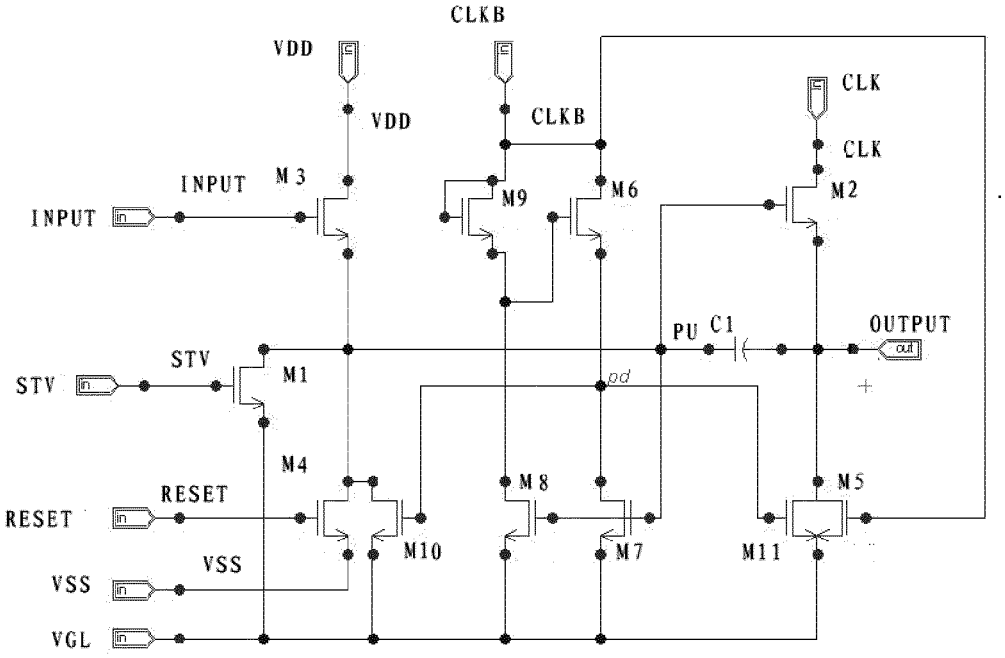
CLKB
VDD
CLK
VDD
CLKB
CLK
INPUT
M3
M9
M6
M2
INPUT
PU
C1
OUTPUT
STV
M1
STV
M4
M8
M5
RESET
RESET
M10
M7
M11
VSS
VSS
VGL

Fig.2a

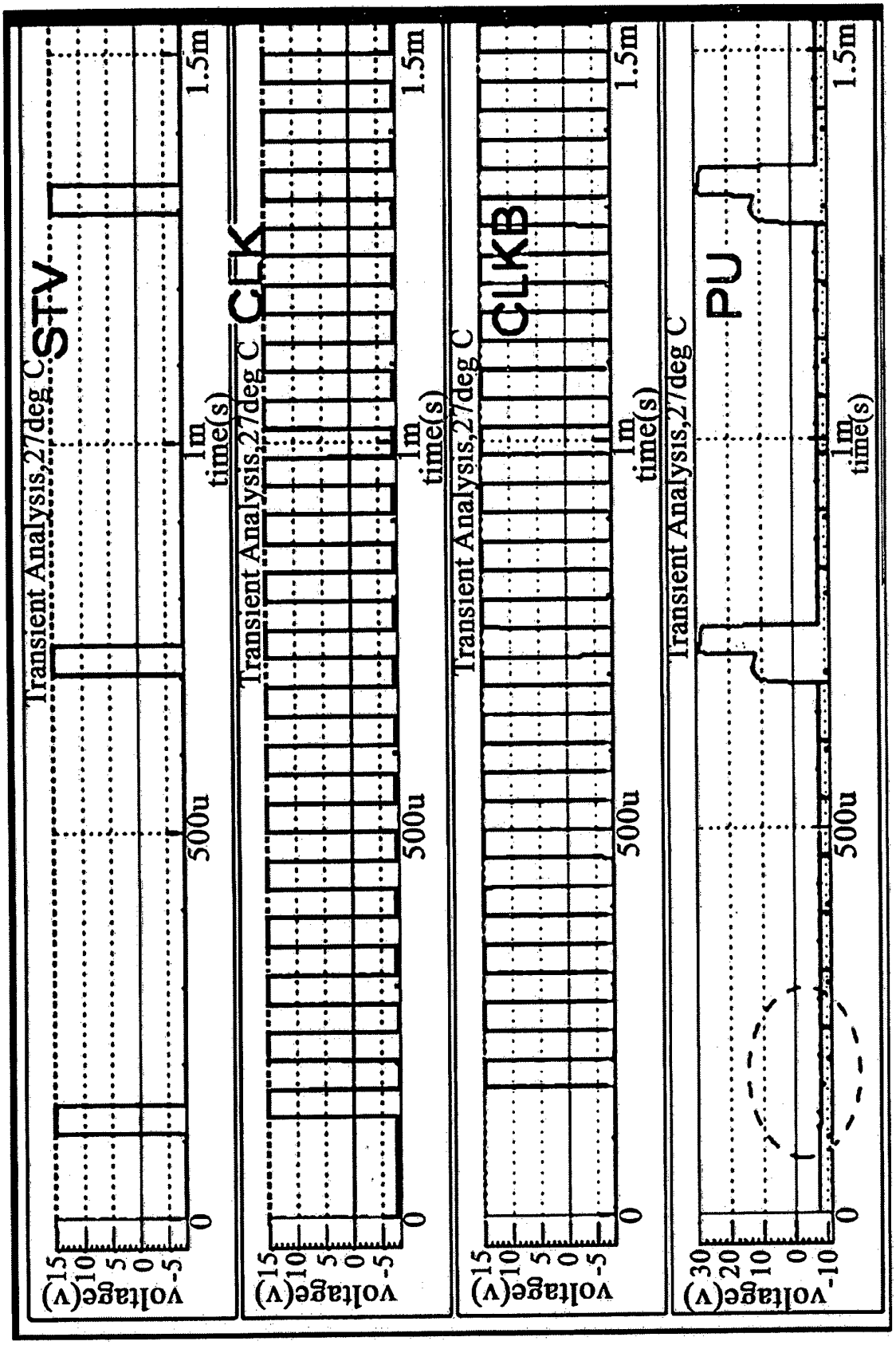
Transient Analysis,27deg C
STV
CLK
CLKB
PU
Voltage(V)
time(s)
0
500u
1m
1.5m
15
10
5
0
-5
30
20
10
0
-10

FIG. 2b

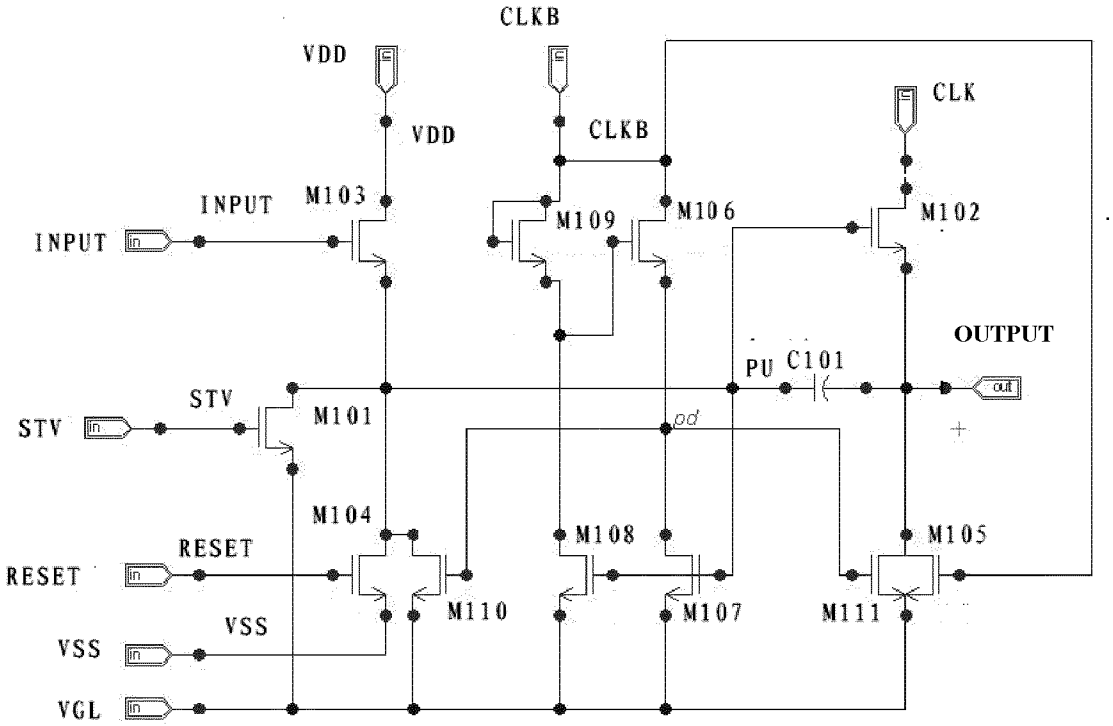
CLKB
VDD
CLK
VDD
CLKB
INPUT
M103
M109
M106
M102
INPUT
OUTPUT
PU
C101
STV
M101
STV
M104
M108
M105
RESET
RESET
M110
M107
M111
VSS
VSS
VGL

Fig.2c

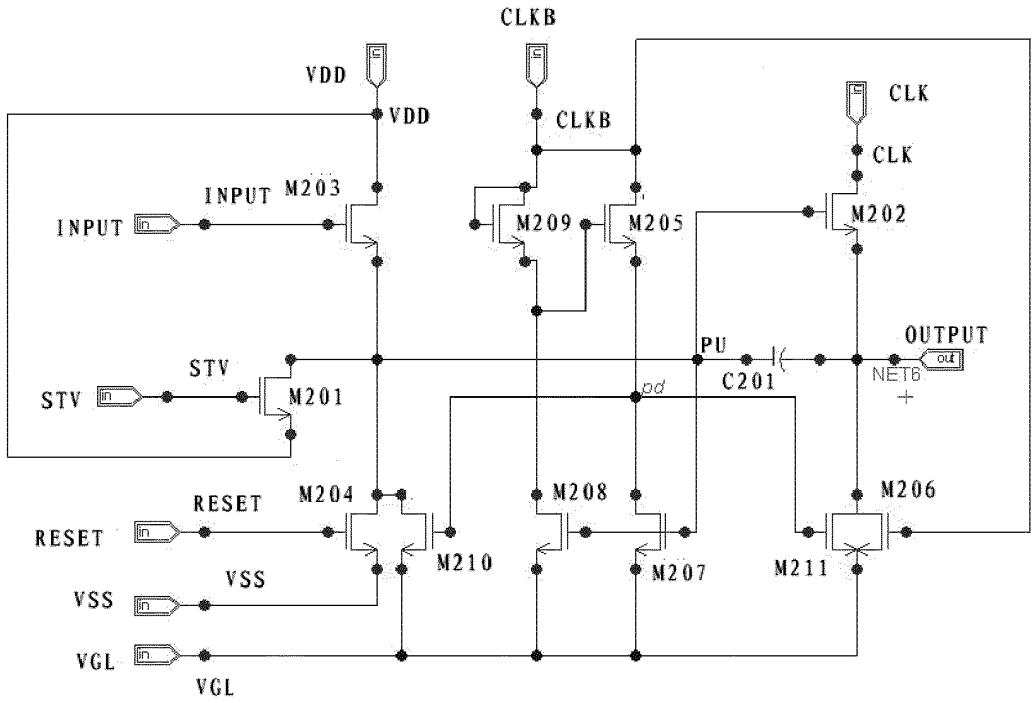
CLKB
VDD
VDD
CLKB
CLK
CLK
INPUT
M203
INPUT
M209
M205
M202
PU
OUTPUT
STV
STV
M201
pd
C201
NET6
RESET
M204
M208
M206
RESET
M210
M207
M211
VSS
VSS
VGL
VGL

Fig.2d

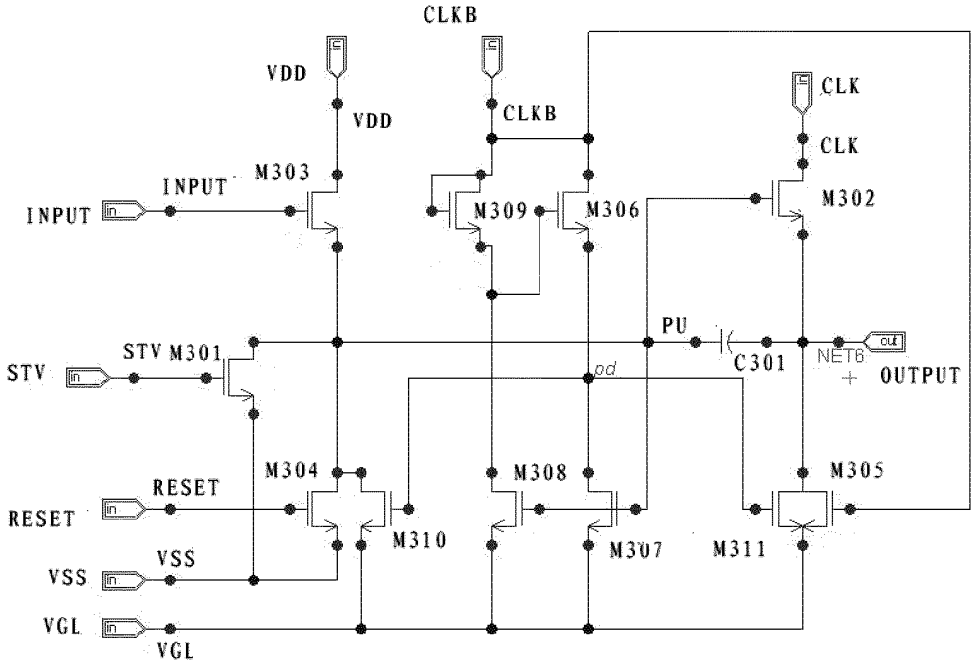
CLKB
VDD
VDD
CLKB
CLK
CLK
INPUT
M303
INPUT
M309
M306
M302
PU
STV
STV M301
pd
C301
NET6
OUTPUT
M304
M308
M305
RESET
RESET
M310
M307
M311
VSS
VSS
VGL
VGL

Fig.2e

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- CN 102629444 A **[0006]**
- US 20070248204 A1 **[0006]**

专利名称(译)	移位寄存器单元电路，移位寄存器，阵列基板和显示装置		
公开(公告)号	EP2709096B1	公开(公告)日	2017-11-01
申请号	EP2013180997	申请日	2013-08-20
[标]申请(专利权)人(译)	北京京东方光电科技有限公司		
申请(专利权)人(译)	北京京东方光电科技有限公司.LTD.		
当前申请(专利权)人(译)	北京京东方光电科技有限公司.		
[标]发明人	WANG SHIJUN		
发明人	WANG, SHIJUN		
IPC分类号	G09G3/36 G11C19/28		
CPC分类号	G09G3/3677 G09G2310/0283 G09G2310/0286 G11C19/28 G09G3/3611		
优先权	201220467195.7 2012-09-13 CN		
其他公开文献	EP2709096A2 EP2709096A3		
外部链接	Espacenet		

摘要(译)

本发明实施例涉及一种液晶显示技术，提供一种移位寄存器单元电路，移位寄存器，阵列基板和显示装置。在移位寄存器单元电路中添加第一TFT，并且当帧起始信号处于高电平并且正向时钟信号从低电平变为高电平时，用于下拉节点PU的电平，使得可以避免由耦合电路的耦合效应引起的输出信号中产生的H线缺陷，这有利于提高产品的生产率和产率。

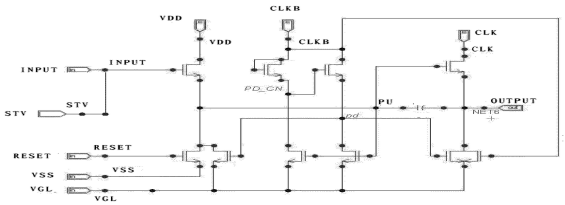

Fig.1a

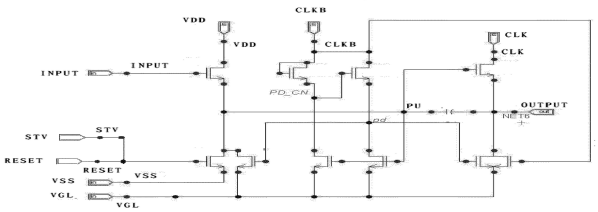

Fig.1b