(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 2 466 369 B1

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
21.05.2014 Bulletin 2014/21

(51) Int Cl.:
G02F 1/1362 *(2006.01)*

(21) Application number: **11174814.1**

(22) Date of filing: **21.07.2011**

(54) **Liquid crystal display to increase side view visibility**

Flüssigkristallanzeige zur Erhöhung der Seitenansichtssichtbarkeit

Écran à cristaux liquides pour augmenter la visibilité latérale

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR

(30) Priority: **14.12.2010 KR 20100127627**

(43) Date of publication of application:
20.06.2012 Bulletin 2012/25

(60) Divisional application:
14162266.2

(73) Proprietor: **Samsung Display Co., Ltd.**
Yongin-City, Gyeonggi-Do (KR)

(72) Inventors:
- **Chang, Hak Sun**
  103-203 Gyeonggi-do (KR)
- **Shin, Kyoung Ju**
  205-602 Gyeonggi-do (KR)
- **Shin, Yong Hwan**
  203-703 Gyeonggi-do (KR)

(74) Representative: **Dr. Weitzel & Partner**
Patent- und Rechtsanwälte mbB
Friedenstrasse 10
89522 Heidenheim (DE)

(56) References cited:
US-A1- 2006 023 137
US-A1- 2007 064 164
US-A1- 2008 273 131
US-A1- 2009 002 586
US-A1- 2010 253 869

EP 2 466 369 B1

Printed by Jouve, 75001 PARIS (FR)

Description

BACKGROUND

FIELD

[0001] The present invention relates to a liquid crystal display, and more particularly, to a liquid crystal display that has improved transmittance and visibility.

DISCUSSION OF THE BACKGROUND

[0002] Liquid crystal displays (LCD), may be composed of two display panels with field generating electrodes, such as a pixel electrode and a common electrode, and a liquid crystal layer between the display panels. LCDs display images by generating an electric field in the liquid crystal layer if voltage is applied to the field generating electrodes such that the liquid crystal molecules in the liquid crystal layer are aligned to control polarization of incident light.

[0003] The conventional liquid crystal displays may include switching elements connected to the pixel electrodes and multiple signal lines, such as gate lines and data lines, to apply voltage to the pixel electrodes by controlling the switching elements.

[0004] Further, in the conventional liquid crystal displays, a vertically aligned mode of liquid crystal display, in which the long axes of the liquid crystal molecules are arranged perpendicular to the display panel, without an electric field has been under the spotlight because of the large contrast ratio and the wide reference viewing angle. The reference viewing angle may imply a viewing angle under a contrast ratio of 1:10 or a luminance reverse limit angle between grays.

[0005] A method of dividing one pixel into two subpixels and applying different voltages to the subpixels to provide a difference in transmittance has been proposed in order to make the side visibility similar to the front visibility of the type of liquid crystal display. In this configuration, if different voltages are applied to the two subpixels through different data lines, double data driving circuits may be used. However, such a configuration may face cost increases in manufacturing.

[0006] A method of connecting the same data line to the two subpixels and reducing the voltage of one of the two subpixels by using a specific switching element and a capacitor has been proposed to solve the problem. However, the method has a problem of low transmittance to the same aperture ratio.

[0007] US2007/0064164 and US2006/0023137 disclose liquid crystal displays comprising three pixel electrodes per pixel and improving the grey level visibility at side viewing angles.

SUMMARY

[0008] The present invention has been made in an effort to provide a liquid crystal display having advantages of having high transmittance and improved visibility.

[0009] Additional features of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention.

[0010] It is to be understood that both foregoing general descriptions and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed. Other features and aspects will be apparent from the following detailed description, the drawings, and the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention, and together with the description serve to explain the principles of the invention.

[0012] FIG. 1 is an equivalent circuit diagram of one pixel a liquid crystal display not according to the invention.

[0013] FIG. 2 is a layout view of a lower display panel of the liquid crystal display not according to the invention.

[0014] FIG. 3 is a graph showing voltage of each electrode if the liquid crystal display is activated not according to the invention.

[0015] FIG. 4 is an equivalent circuit diagram of one pixel of a liquid crystal display not according the invention.

[0016] FIG. 5 is a layout view of a lower display panel of the liquid crystal display not according to the invention.

[0017] FIG. 6 is a layout view of a lower display panel of a liquid crystal display not according to the invention.

[0018] FIG. 7 is a cross-sectional view of the liquid crystal display not according to the invention, taken along the line VII-VII' of FIG. 6.

[0019] FIG. 8 is a cross-sectional view of the liquid crystal display not according to the invention, taken along the line VIII-VIII' of FIG. 6.

[0020] FIG. 9 is a cross-sectional view of a liquid crystal display not according to the invention, taken along the line VIII-VIII' of FIG. 6.

[0021] FIG. 10 is an equivalent circuit diagram of one pixel of a liquid crystal display not according to the invention.

[0022] FIG. 11 is a layout view of a lower display panel of the liquid crystal display not according to of the invention.

[0023] FIG. 12 is a cross-sectional view of a liquid crystal display not according to the invention, taken along the line XII-XII' of FIG. 11.

[0024] FIG. 13 is an equivalent circuit diagram of one pixel a liquid crystal display according to an exemplary embodiment of the invention.

[0025] FIG. 14 is a layout view of a lower display panel of the liquid crystal display according to an exemplary embodiment of the invention.

[0026] FIG. 15 is an equivalent circuit diagram of one pixel a liquid crystal display not according to the invention.

[0027] FIG. 16 is a graph showing a V-T curve at the front and the side of a liquid crystal display according to the related art.

[0028] FIG. 17 is a graph showing a V-T curve at the front and the side of a liquid crystal display according to an exemplary embodiment of the invention.

[0029] FIG. 18 is a graph showing a V-T curve at the front and the side of a liquid crystal display according to an exemplary embodiment of the invention.

[0030] FIG. 19 is a graph showing a V-T curve at the front and the side of a liquid crystal display according to an exemplary embodiment of the invention.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

[0031] The present invention will be described more fully hereinafter with reference to the accompanying drawings, in which exemplary embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, these exemplary embodiments are provided so that this disclosure is thorough, and will fully convey the scope of the invention to those skilled in the art. It will be understood that when an element is referred to as being "on" or "connected to" or "coupled to" another element, it can be directly on, directly connected to, or directly coupled to the other element, or intervening elements may be present. In contrast, if an element is referred to as being "directly on" or "directly connected to" or "directly coupled to" another element, no intervening elements are present. Throughout the drawings and the detailed description, unless otherwise described, the same drawing reference numerals are understood to refer to the same elements, features, and structures. The relative size and depiction of these elements may be exaggerated for clarity, illustration, and convenience.

[0032] A liquid crystal display according to a first exemple not according to the present invention is described first with reference to the accompanying drawings.

[0033] FIG. 1 is an equivalent circuit diagram of one pixel a liquid crystal display according to an exemple not according to the invention. FIG. 2 is a layout view of a lower display panel of the liquid crystal display according to an exemple not according to invention.

[0034] A liquid crystal display according to a first exemple not according to invention, as shown in FIG. 1, includes a first switching element Qa and a second switching element Qb, a first liquid crystal capacitor Clca connected to the first switching element Qa, a second liquid crystal capacitor Clcb connected to the second switching element Qb, a third switching element Qc connected to the second switching element Qb, and a third liquid crystal capacitor Clcc connected to the third switching element Qc.

[0035] The liquid crystal display according to the first exemple may further include a first gate line GLn, a second gate line GLn+1, and a data line DL. The first switching element Qa and the second switching element Qb may be three terminal elements of a thin film transistor etc., connected to the first gate line GLn to be switched by the same signal, and connected to the data line DL to receive the same data signal. The third switching element Qc is a three terminal element of a thin film transistor etc., and is connected to the second gate line GLn+1.

[0036] If gate-on voltage is applied to the first gate line GLn, the first switching element Qa and the second switching element Qb are turned on and the same data signal is applied through the data line DL, such that the first liquid crystal capacitor Clca and the second liquid crystal capacitor Clcb are charged with similar or near identical voltage. Thereafter, if gate-on voltage is applied to the second gate line GLn+1, which is the next gate line, the third switching element Qc is turned on and some of the charged voltage of the second liquid crystal capacitor Clcb are discharged to the third liquid crystal capacitor Clcc. Therefore, a difference in voltage is created between the first liquid crystal capacitor Clca and the second liquid crystal capacitor Clcb. As a result, the side visibility of the liquid crystal display can be improved.

[0037] In the structure of the liquid crystal display according to the first exemple, as shown in FIG. 2, one or more of first gate lines 121a and second gate lines 121b are provided on a first substrate (not shown). In an example, the first substrate may be made of transparent glass or plastic.

[0038] The first gate lines 121a and second gate lines 121b may transmit gate signals and may extend transversely. The first gate lines 121a and the second gate lines 121b may be alternately disposed and gate-on voltage may be sequentially applied to the first gate lines 121a and the second gate lines 121b.

[0039] The first gate line 121 a includes one or more of first gate electrodes 124a and second gate electrodes 124b, which protrude downward. The first gate electrode 124a and the second gate electrode 124b may be connected in one unit, such that they receive the same gate signal through the first gate line 121a. The second gate line 121b includes one or more of third gate electrodes 124c protruding upward.

[0040] A gate insulating layer (not shown) may be formed on the first gate lines 121a and second gate lines 121b. A semiconductor island (not shown) may be formed on the gate insulating layer. The semiconductor island may be disposed above the first gate electrode 124a, second gate electrode 124b, and third gate electrode 124c.

[0041] As shown further in FIG. 2, one or more data lines 171, a first source electrode 173a, a second source electrode 173b, a third source electrode 173c, a first drain electrode 175a, a second drain electrode 175b, and a third drain electrode 175c are formed on the semiconductor and the gate insulating layer.

[0042] The data line 171 transmits a data signal and may extend longitudinally to cross the first gate line 121a and second gate line 121b.

[0043] The first source electrode 173a and the second source electrode 173b protrude from the data line 171 and may be connected in one unit, such that they receive the similar or near identical data voltage through the data line 171. The first source electrode 173a is formed in a U-shape on the first gate electrode 124a and the second source electrode 173b is formed in a U-shaped on the second gate electrode 124b.

[0044] The first drain electrode 175a is spaced apart from the first source electrode 173a and has a bar-shaped end, with the first gate electrode 124a there between, in which the bar-shaped end is partially surrounded by the first source electrode 173a bending in a U-shape.

[0045] The second drain electrode 175b is spaced apart from the second source electrode 173b and has a bar-shaped end, with the second gate electrode 124b there between, in which the bar-shaped end is partially surrounded by the second source electrode 173b bending in a U-shape. The other end of the second drain electrode 175b is connected to the third source electrode 173c.

[0046] The third source electrode 173c extends from the second drain electrode 175b, in a U-shape on the third gate electrode 124c. The third drain electrode 175c is spaced apart from the third source electrode 173c and has a bar-shaped end, with the third gate electrode 124c there between, in which the bar-shaped end is partially surrounded by the third source electrode 173c bending in a U-shape.

[0047] The first source electrode 173a may be formed in an inverse U-shape, the second source electrode 173b in a U-shape open to the right, and the third source electrode 173c in a U-shape open to the right. Therefore, it may be possible to reduce a change in capacitance between the gate electrodes (first gate electrode 124a, second gate electrode 124b, and third gate electrode 124c) and the source electrodes (first source electrode 173a, second source electrode 173b, and third source electrode 173c), even if an error occurs in the positions of the source electrodes (first electrode 173a, second electrode 173b, and third source electrode 173c) due to a process deviation.

[0048] In an example, the first gate electrode 124a, the first source electrode 173a, and the first drain electrode 175a may constitute the first switching element (Qa in FIG. 1). The second gate electrode 124b, the second source electrode 173b, and the second drain electrode 175b may constitute the second switching element (Qb in FIG. 1). The third gate electrode 124c, the third source electrode 173c, the third drain electrode 175c may constitute the third switching element (Qc in FIG. 1).

[0049] A passivation layer (not shown) is formed on the data line 171, the first source electrode 173a, second source electrode 173b, and third source electrode 173c, first drain electrode 175a, second drain electrode 175b, and third drain electrode 175c. The passivation layer may be made of an inorganic insulator or organic insulator, with a flat surface. Further, the passivation layer may have a double layer structure including a lower layer, which may be an inorganic layer, and an upper layer, which may be an organic layer, in order to keep the high insulation of an organic layer, without damaging the exposed portion of the semiconductor.

[0050] A first contact hole 181a exposing a portion of the first drain electrode 175a, a second contact hole 181b exposing a portion of the second drain electrode 175b, and a third contact hole 181c exposing a portion of the third drain electrode 175c are formed on the passivation layer.

[0051] One or more first subpixel electrodes 191a, second subpixel electrodes 191b, and third subpixel electrodes 191c may be made of a transparent electrode material, such as an ITO (Indium Tin Oxide) or an IZO (Indium Zinc Oxide) on the passivation layer. The first subpixel electrode 191a is connected to the first drain electrode 175a through the first contact hole 181a, the second subpixel electrode 191b is connected to the second drain electrode 175b through the second contact hole 181b, and the third subpixel electrode 191c is connected to the third drain electrode 175c through the third contact hole 181c.

[0052] Although not shown, a common electrode may be provided on a second substrate assembled with the first substrate, and a liquid crystal layer may be provided between the first substrate and the second substrate.

[0053] The first subpixel electrode 191a and the second subpixel electrode 191b together with the common electrode on the second substrate and the liquid crystal layer there between respectively constitute first liquid crystal capacitors (Clca in FIG. 1) and second liquid crystal capacitor (Clcb in FIG. 1). The liquid crystal capacitors as described here may retain the applied voltage even after the first and second switching elements Qa and Qb are turned off

[0054] The third subpixel electrode 191c constitutes a third liquid crystal capacitor (Clcc in FIG. 1), together with the common electrode on the second substrate and the liquid crystal layer there between. Some of the voltage stored in the second liquid crystal capacitor Clcb may be discharged to the third liquid crystal capacitor Clcc, such that a difference in voltage may be created between the first liquid crystal capacitor Clca and the second liquid crystal capacitor Clcb.

[0055] In this configuration, the third subpixel electrode 191c is formed between the first gate line 121a and the second gate line 121b. A light blocking member is formed on the second substrate, corresponding to the first gate line 121a, second gate line 121b, first switching element Qa, second switching element Qb, and third switching element Qc, and the third subpixel electrode 191c. That is, the third subpixel electrode 191c may reduce the voltage of the second subpixel electrode 191b, but may not

display an image by transmitting light.

[0056] The liquid crystal display according to the first exemple may further include one or more of storage electrode lines 131 formed on the same layer as the first gate line 121a and second gate line 121b.

[0057] The storage electrode line 131 receives a reference voltage and may extend substantially in parallel with and at a reference distance from the first gate line 121a and second gate line 121b. The storage electrode line 131 may be positioned between the first gate line 121a of a first pixel and the second gate line 121b of a second pixel. The storage electrode line 131 may include a storage electrode 133, which may expand upward or downward. However, the shape and arrangement of the storage electrode line 131 and the storage electrodes 133 may be modified in various ways.

[0058] In the conventional technology, the third drain electrode 175c and the storage electrode 133 may be configured overlap to function as a capacitor that reduces the voltage of the second subpixel electrode 191b. However, this type of configuration may incur some problem in that the provided transmittance may be low, and the semiconductor is positioned between the third drain electrode 175c and the storage electrode 133 to possibly generate a surface residual image, if the liquid crystal display is formed through a four-time photolithography. Further, there may be a problem in that the first gate line 121a and the third drain electrode 175c overlap, which may possibly generate parasitic capacity, which may have an adverse effect on the image made by the second subpixel electrode 191b.

[0059] On the contrary the third subpixel electrode 191c may be formed such that the third liquid crystal capacitor (Clcc in FIG. 1) functions as a capacitor to reduce the voltage of the second subpixel electrode 191b. Accordingly, it may be possible to further improve the transmittance and reduce the surface residual image, in comparison to the related art. In an example, the transmittance may improve as much as 5%, if not more. Further, the first gate line 121a and the third drain electrode 175c may be configured so that do not overlap each other. As a result, it may be possible to prevent or reduce parasitic capacitance.

[0060] The first subpixel electrode 191a and second subpixel electrode 191b constitute a storage capacitor by overlapping the storage electrode 133, which may help the first liquid crystal capacitor Clca and second liquid crystal capacitor Clcb retain their voltage.

[0061] The voltage relationship that may be present if the liquid crystal display of the first exemple is activated is described hereafter.

[0062] FIG. 3 is a graph showing voltage of each electrode if the liquid crystal display is activated according to an exemple.

[0063] First, if a first gate signal V_GLn is supplied to the first gate line 121a, the voltage V_PX1 of the first subpixel electrode 191a and the voltage V_PX2 of the second subpixel electrode 191b may be charged to similar or near identical levels. If a second gate signal V_GLn+1 is supplied to the second gate line 121b, the voltage V_PX3 of the third subpixel electrode 191c may be increased to similar voltage level V_PX2 of the second subpixel electrode 191b, and the voltage V_PX2 of the second subpixel electrode 191b and the voltage V_PX3 of the third subpixel electrode 191 may be decreased to a voltage level below the voltage V_PX1 of the first subpixel electrode 191a.

[0064] It can be seen that the voltage V_PX2 of the second subpixel electrode 191 b and the voltage V_PX3 of the third subpixel electrode 191c are close at the point A, such that it can also be seen that the third subpixel electrode 191c may reduce the voltage V_PX2 of the second subpixel electrode 191b, and also display an image. Using the third subpixel electrode 191c to display an image, without covering it with a light blocking member, in the second exemple is described hereafter.

[0065] A liquid crystal display according to the second exemple not according to invention is described hereafter in detail with reference to FIG. 4 and FIG. 5.

[0066] FIG. 4 is an equivalent circuit diagram of one pixel of a liquid crystal display not according to the invention. FIG. 5 is a layout view of a lower display panel of the liquid crystal display not according to the invention.

[0067] As shown in FIG. 4, the liquid crystal display according to the second exemple may be similar in structure as illustrated in the circuit diagram as the liquid crystal display according to the first exemple, and as such will not described. However, the second exemple has a difference in the layout view from the first exemple, and this is described in more detail with reference to FIG. 5.

[0068] In the structure of the liquid crystal display according to the second exemple of the invention, one or more of first gate lines 121 a and second gate lines 121b are formed on a first substrate (not shown), which may made of transparent glass or plastic, as shown in FIG. 5.

[0069] The first gate line 121a and the second gate line 121b transmit gate signals and may extend transversely. The first gate line 121a and the second gate line 121b may be alternately disposed and gate-on voltage may be sequentially applied to the first gate line 121a and the second gate line 121b.

[0070] The first gate line 121a may include one or more first gate electrodes 124a and second gate electrodes 124b, which may protrude upward and downward, respectively. Also, the first gate electrode 124a and the second gate electrode 124b may receive the same gate signal through the first gate line 121a. The second gate line 121b may include one or more third gate electrodes 124c, which may protrude therefrom.

[0071] A gate insulating layer (not shown) may be further formed on the first gate lines 121a and the second gate lines 121b. A semiconductor island (not shown) may be formed on the gate insulating layer. The semiconductor island may further be disposed above the first gate electrode 124a, the second gate electrode 124b, and the third gate electrode 124c.

[0072] One or more data lines 171, a first source electrode 173a, a second source electrode 173b, a third source electrode 173c, a first drain electrode 175a, a second drain electrode 175b, and a third drain electrode 175c may be formed on the semiconductor and the gate insulating layer.

[0073] The data line 171 transmits a data signal and may extend longitudinally, crossing the first gate line 121a and the second gate line 121b.

[0074] The first source electrode 173a protrudes above the first gate electrode 124a from the data line 171, the second source electrode 173b protrudes above the second gate electrode 124b from the data line 171. Further, the first source electrode 173a and the second source electrode 173b may be connected in one unit, such that they may receive the same data voltage through the data line 171. The first source electrode 173a is formed in a U-shape on the first gate electrode 124a and the second source electrode 173b is formed in a U-shape on the second gate electrode 124b.

[0075] The first drain electrode 175a is spaced apart from the first source electrode 173a and has a bar-shaped end, with the first gate electrode 124a there between, in which the bar-shaped end is partially surrounded by the first source electrode 173a bending in a U-shape.

[0076] The second drain electrode 175b is spaced apart from the second source electrode 173b and has a bar-shaped end, with the second gate electrode 124b there between, in which the bar-shaped end is partially surrounded by the second source electrode 173b bending in a U-shape. The other end of the second drain electrode 175b is connected to the third source electrode 173c.

[0077] The third source electrode 173 extends from the second drain electrode 175b, in a U-shape on the third gate electrode 124c. The third drain electrode 175c is spaced apart from the third source electrode 173c and has a bar-shaped end, with the third gate electrode 124c there between, in which the bar-shaped end is partially surrounded by the third source electrode 173c bending in a U-shape.

[0078] In an example, the first gate electrode 124a, the first source electrode 173a, and the first drain electrode 175a may constitute the first switching element (Qa in FIG. 1). The second gate electrode 124b, the second source electrode 173b, and the second drain electrode 175b may constitute the second switching element (Qb in FIG. 1). The third gate electrode 124c, the third source electrode 173c, the third drain electrode 175c may constitute the third switching element (Qc in FIG. 1).

[0079] A passivation layer (not shown) may be formed on various components, including the data line 171, the first source electrode 173a, the second source electrode 173b, and the third source electrode 173c, the first drain electrode 175a, the second drain electrode 175b, and the third drain electrode 175c. The passivation layer may be made of an inorganic insulator or an organic insulator, with a flat surface. Further, the passivation layer may have a double layer structure composed of a lower layer, which may be an inorganic layer, and an upper layer, which may be an organic layer, in order to keep the high insulation of an organic layer and reducing the risk of damaging the exposed portion of the semiconductor.

[0080] A first contact hole 181a exposing a portion of the first drain electrode 175a, a second contact hole 181b exposing a portion of the second drain electrode 175b, and a third contact hole 181c exposing a portion of the third drain electrode 175c may be formed on the passivation layer.

[0081] One or more first subpixel electrode 191a, second subpixel electrodes 191b, and third subpixel electrodes 191c may be made of a transparent electrode material, such as an ITO (Indium Tin Oxide) or an IZO (Indium Zinc Oxide), and formed on the passivation layer. The first subpixel electrode 191a is connected to the first drain electrode 175a through the first contact hole 181a. The second subpixel electrode 191b is connected to the second drain electrode 175b through the second contact hole 181b. The third subpixel electrode 191c is connected to the third drain electrode 175 through the third contact hole 181c.

[0082] The first subpixel electrode 191a and the second subpixel electrode 191b are formed above and under the first gate line 121a, respectively. Further, the second subpixel electrode 191b and the third subpixel electrode 191c are formed above and under the second gate line 121b, respectively. That is, the second subpixel electrode 191b is formed between the first gate line 121a and the second gate line 121b. In this configuration, although the first subpixel electrode 191a, the second subpixel electrode 191b, the third subpixel electrode 191c are shown having the same size, it is not limited thereto and may make the size different.

[0083] Although not shown, a common electrode may be provided on a second substrate. Further, the second substrate may be assembled with the first substrate and a liquid crystal layer may be formed between the first substrate and the second substrate.

[0084] The first subpixel electrode 191a and the second subpixel electrode 191b, together with the common electrode on the second substrate and the liquid crystal layer there between, may constitute first liquid crystal capacitors (Clca in FIG. 4) and second liquid crystal capacitor (Clcb in FIG. 4). The liquid crystal capacitors as described here may retain the applied voltage even after the first and second switching elements Qa and Qb are turned off.

[0085] The third subpixel electrode 191a, together with the common electrode on the second substrate and the liquid crystal layer there between, may constitute a third liquid crystal capacitor (Clcc in FIG. 1). Some of the voltage stored in the second liquid crystal capacitor Clcb may be discharged to the third liquid crystal capacitor Clcc, such that a difference in voltage may be created between the first liquid crystal capacitor Clca and the second liquid

crystal capacitor Clcb. As a result, the voltage level of the second subpixel electrode 191b and the voltage level of the third subpixel electrode 191c may be similar.

[0086] The liquid crystal display according to the second exemple may further include one or more first electrode line 131a, second electrode line 131b, and third storage electrode line 131c that are formed on the same layer as the first gate line 121 a and the second gate line 121b.

[0087] The first storage electrode line 131a, the second electrode line 131b, and the third storage electrode line 131c may receive reference voltage and may extend substantially in parallel with and at a reference distance from the first gate lines 121a and the second gate line 121b. The storage electrode lines (first storage electrode line 131a, the second storage electrode line 131b, and the third storage electrode line 131c) may further include additional storage electrodes (first storage electrode 133a, second storage electrode 133b, third storage electrode 133c, and fourth storage electrode 133d,) which expand therefrom.

[0088] In an example, the first storage electrode line 131a may be formed above the first subpixel electrode 191a, the second storage electrode line 131b may overlap the center portion of the second subpixel electrode 191b, and the third storage electrode line 131c may be formed under the third subpixel electrode 191 c.

[0089] The first storage electrode 133a protrudes from the first storage electrode line 131a to partially overlap the left side and right side of the first subpixel electrode 191a.

[0090] The second storage electrode 133b may be formed in parallel with the first gate line 121a, overlapping the center portion of the first subpixel electrode 191a. The second storage electrode 133b connects the first storage electrode 133a with the first storage electrode 133a, which may be at the left side and the right side of the first subpixel electrode 191a, respectively.

[0091] The first storage electrode 133a may partially overlap one of the left side or the right side of the first subpixel electrode 191a. The second storage electrode 133b is connected to the first storage electrode 133a formed at any one side.

[0092] The third storage electrode 133c protrudes from the second storage electrode line 131b, partially overlapping the left and right sides of the second subpixel electrode 191b.

[0093] The fourth storage electrode 133d protrudes from the third storage electrode line 131c, overlapping the left and right sides of the third subpixel electrode 191 c.

[0094] Alternatively, the third storage electrode 133c and the fourth storage electrode 133d may respectively partially overlap only one of the left and right sides of the second subpixel electrode 191 b and third subpixel electrode 191 c.

[0095] Further, the shape and arrangement of the storage electrode lines (first storage electrode line 131a, second storage electrode line 131b, and third storage electrode line 131c) and the storage electrodes (first storage electrode 133a, second storage electrode 133b, third storage electrode 133c, and fourth storage electrode 133d) may be modified in various ways.

[0096] The data voltage applied to the data line 171 may continuously change with time, which influences the voltage of the first subpixel electrode 191a, the second subpixel electrode 191b, and the third subpixel electrode 191c. The first storage electrode 133a, the third storage electrode 133c, and the fourth storage electrode 133d may partially overlap the subpixel electrodes (first subpixel electrode 191a, second subpixel electrode 191b, and third subpixel electrode 191c,) adjacent to the data line, such that they can avoid the influence of the voltage.

[0097] In an example, an alignment layer may be formed on the first substrate and the second substrate of the liquid crystal layer, and it may be possible to align light in order to control the alignment direction and the alignment angle of the liquid crystal by radiating light to the alignment layers. Although it may be possible to increase the aperture ratio and improve the response speed of the liquid crystal by means of the light alignment, the alignment directions of the liquid crystal may be different at the interfaces of difference domains, such that texture may be generated at the interfaces.

[0098] The portion indicated by B in FIG. 5 is the region where the texture is generated, in which luminance may be larger than the other regions. However, it may be possible to reduce the influence caused by the generation of texture. In an example, if the liquid crystal is disposed at an angle of 0 degree at the longitudinal line portion crossing the center of the subpixel electrodes (first subpixel electrode 191a, the second subpixel electrode 191b, and third subpixel electrode 191c), the longitudinal line portion may be shown as if a luminance difference from the other regions is not large, if seen from the sides and the front. On the contrary, if the liquid crystal is disposed at an angle of 90 degrees at the transverse line portion crossing the centers of the subpixel electrodes (first subpixel electrode 191a, the second subpixel electrode 191b, and the third subpixel electrode 191c), the transverse line portion may be shown as if a luminance difference from the other regions is large, if seen from the sides.

[0099] Therefore, it may possible to reduce an influence of voltage due to texture by forming the second storage electrode 133b, the second storage electrode lines 131b to cover the transverse line portion crossing the centers of the subpixel electrodes (first subpixel electrode 191a, second subpixel electrode 191b, and third subpixel electrode 191c).

[0100] Unlike the first exemple, a light blocking member corresponding to the third pixel electrode 191c is not formed on the second substrate, in the second exemple . That is, the third subpixel electrode 191c may reduce the voltage of the second subpixel electrode 191 b, as well as display an image by transmitting light.

[0101] In the second exemple, the voltages of the second subpixel electrode 191b and the third subpixel electrode 191c may be similar or near identical, while the voltage of the first subpixel electrode 191a may be larger than the voltage of the second subpixel electrode 191 b and the third subpixel electrode 191 c. That is, although one pixel is divided in three subpixels, two subpixels may have the similar or near identical voltage, such that two grays may be implemented. In this configuration, the side visibility is further improved by applying three different voltages to the three subpixels, and a voltage difference in the second subpixel electrode 191b and the third subpixel electrode 191c is described hereafter with reference to the third exemple .

[0102] A liquid crystal display according to the third exemple not according to invention is described hereafter in detail with reference to FIG. 6, FIG. 7, FIG. 8, and FIG. 9.

[0103] FIG. 6 is a layout view of a lower display panel of a liquid crystal display not according to the invention. FIG. 7 is a cross-sectional view of the liquid crystal display not according to the invention, taken along the line VII-VII' of FIG. 6. FIG. 8 is a cross-sectional view of the liquid crystal display not according to the invention, taken along the line VIII-VIII' of FIG. 6. FIG. 9 is a cross-sectional view of a liquid crystal display not according to the invention, taken along the line VIII-VIII' of FIG. 6.

[0104] A large portion of the configuration of the liquid crystal display according the third exemple is similar to the liquid crystal display according to the second exemple, as shown in FIG. 6. Therefore, the detailed description is not provided and discussion will be directed towards the differences.

[0105] In the liquid crystal display according to the third exemple, a first subpixel electrode 191a and a second subpixel electrode 191b may be formed in the same way as in the liquid crystal display according to the second exemplary embodiment. One or more fine slits 193 may be provided in the third subpixel electrode 191 c. It is possible to make the voltage of the third subpixel electrode 191c lower than the voltage of the second subpixel electrode 191b by providing the fine slits 193.

[0106] As shown in FIG. 7, a gate insulating layer 140 and a passivation layer 180 are sequentially stacked on the first substrate 110 and the third subpixel electrode 191c is formed on the passivation layer 180. A common electrode 270 is formed on the second substrate 210 opposite to the first substrate 110.

[0107] The fine slits 193 may be provided at regular intervals with various widths. In an example, the width 'a' of the fine slit located on third subpixel electrode 191c between adjacent fine slits 193 may have a width range of 1 μm to 4 μm. Further, the width 'b' of the fine slit 193 may be in the range of 1 μm to 5 μm.

[0108] Further, as shown in FIG. 8, the thickness 'd' of the passivation layer 180 under the third subpixel electrode 191c may be larger than the thickness 'c' of the passivation layer under the first subpixel electrode 191a and the second subpixel electrode 191b. (Please note that only the second subpixel electrode 191b is illustrated in Fig. 8, since the structure around the first subpixel electrode 191a is the same as that around the second subpixel electrode 191b.) That is, it may be possible to form the passivation layers 180 to have different thicknesses in accordance with the positions. In an example, the thickness may be adjusted by using a slit mask of a halftone mask in the process of forming the passivation layers 180, even without using an additional mask.

[0109] It may be possible to further increase the difference in voltage between the third subpixel electrode 191c and the second subpixel electrode 191b by making the thickness of the passivation layer 180 irregular such that the cell gap between the first substrate 110 and the second substrate 210 is different in accordance with their positions, as described above. In this configuration, the cell gap 'f' at the portion where the third subpixel electrode 191c is formed may be smaller at 0.1 μm to 0.5 μm than the cell gap 'e' at the portion where the second subpixel electrode 191 b is formed.

[0110] As shown in FIG. 9, alignment layers 11a and 21 may be formed on the first substrate 110 and the second substrates 210 of the liquid crystal display according to the third exemple. Also, it may be possible to align light in order to control the alignment direction and the alignment angle of the liquid crystal by radiating light to the alignment layer.

[0111] The pretilt angle of the alignment layer 11b at the portion corresponding to the third subpixel electrode 191c may be smaller than the pretilt angle of the alignment layer 11a at the portion corresponding to the second subpixel electrode 191b. This difference in pretilt angles may allow further increases in the voltage difference between the third subpixel electrode 191c and the second subpixel electrode 191b. In an example, the pretilt angle of the alignment layer 11b at the portion corresponding to the third subpixel electrode 191c may be smaller at 0. 5 degrees to 2 degrees than the pretilt angle of the alignment layer 11a at the portion corresponding to the second subpixel electrode 191b.

[0112] In the liquid crystal display according to the third exemple, a method of providing the fine slits 193 in the third subpixel electrode 191c, a method of making the cell gap different by adjusting the height of the passivation layers 180 to be different, and a method of providing the pretilt angle different in light alignment has been described in order to making a difference in voltage between the second subpixel electrode 191 b and the third subpixel electrode 191c. One of the three methods may be used alone or in conjunction with the one or two of the other described methods.

[0113] In the liquid crystal display according to the third exemple, three grays may be implemented by making a difference in voltage between the second subpixel electrode 191 b and the third subpixel electrode 191c such that the subpixel electrodes (first subpixel electrode 191a, the second subpixel electrode 191b, and the third

subpixel electrodes 191c) have different voltages. As a result, the side visibility can be more improved over the second example having one pixel shown in two grays, if one pixel is shown with three grays, as in the third exemple.

[0114] A liquid crystal display according to a fourth exemple not according to invention is described hereafter in detail with FIG. 10, FIG. 11, and FIG. 12.

[0115] FIG. 10 is an equivalent circuit diagram of one pixel of a liquid crystal display not according to the invention. FIG. 11 is a layout view of a lower display panel of the liquid crystal display not according to the invention. FIG. 12 is a cross-sectional view of the liquid crystal display not according to the invention, taken along the line XII-XII' of FIG. 11.

[0116] A large portion of the configuration of the liquid crystal display according the fourth exemple is similar to the liquid crystal display according to the second exemple, as shown in FIG. 10. Therefore, the detailed description is not provided and the discussion will be directed towards the differences.

[0117] In the liquid crystal display according to the fourth exemple, the third liquid crystal capacitor Clcc is not directly connected to the third switching element Qc, but connected through a transforming capacitor Ct. That is, the liquid crystal display according to the fourth exemple may further include the transforming capacitor Ct, as compared with the liquid crystal display according to the second exemple. The transforming capacitor Ct is connected to the third switching element Qc and the third liquid crystal capacitor Clcc is connected to the transforming capacitor Ct.

[0118] If gate-on voltage is applied to the first gate line GLn, the first switching element Qa and the second switching element Qb are turned on. Also, the same data signal is applied through the data line DL, such that the first liquid crystal capacitor Clca and the second liquid crystal capacitor Clcb are charged with similar or near identical voltage. Thereafter, if gate-on voltage is applied to the second gate line GLn+1, which is the next gate line, the third switching element Qc is turned on and some of the charged voltage of the second liquid crystal capacitor Clcb are discharged to the transforming capacitor Ct and the third liquid crystal capacitor Clcc. Therefore, a difference in voltage is created between the first liquid crystal capacitor Clca and the second liquid crystal capacitor Clcb. Further, the voltage discharged from the second liquid crystal capacitor Clcb may be divided to the transforming capacitor Ct and the third liquid crystal capacitor Clcc, such that a difference in voltage is created between the second liquid crystal capacitor Clcb and the third liquid crystal capacitor Clcc. Accordingly, it may be possible to improve the side visibility of the liquid crystal display.

[0119] The structure of the liquid crystal display according to the fourth exemple, as shown in FIG. 11, has a large portion similar to the configuration of the liquid crystal display according to the second exemple. Therefore, the detailed description is not provided and the discussion will be directed towards the differences.

[0120] In the liquid crystal display according to the fourth exemple, unlike the second exemple, the third subpixel electrode 191c is not directly connected to the third drain electrode 175c.

[0121] As shown in FIG. 12, a gate insulating layer 140 is formed on the first substrate 110 and a third drain electrode 175c is formed on the gate insulating layer 140. A passivation layer 180 is provided between the third drain electrode 175c and the third subpixel electrode 191c to form the transforming capacitor Ct. A common electrode 270 is formed on the second substrate 210 opposite to the first substrate 110. A liquid crystal layer (not shown) is formed between the third subpixel electrode 191c and common electrode 270 to form the third liquid crystal capacitor Clcc.

[0122] The third drain electrode 175c may be formed to have a size above a reference level to function as the transforming capacitor Ct. Further, the third drain electrode 175c may generally be an opaque electrode, such that it is possible to reduce the aperture ratio of the third subpixel electrode 191c.

[0123] In this configuration, it may be possible to make the thickness 'h' of the passivation layer 180 (at the portion where the third drain electrode 175c and the third subpixel electrode 191c overlap) smaller than the thickness 'g' of the passivation layer 180 (at the portion where the third drain electrode 175c and the third subpixel electrode 191c do not overlap), in order to reduce the size of the third drain electrode 175c and increase the capacitance of the transforming capacitor Ct. That is, it may be possible to form the passivation layer 180 to have irregular thickness in accordance with their positions by using a slit mask or a halftone mask in the process of forming the passivation layer 180, even without using an additional mask.

[0124] In the liquid crystal display according to the fourth exemple, the side visibility may be improved by creating a difference in voltage levels between the second subpixel electrode 191b and the third subpixel electrode 191c. Such a difference in voltage levels may be provided using the transforming capacitor (Ct in FIG. 11) such that the first subpixel electrode 191a, the second subpixel electrode 191b, and the third subpixel electrode 191c have different voltages. As a result, three shades of grays may be implemented.

[0125] A liquid crystal display according to an exemplary embodiment of the invention is described hereafter in detail with FIG. 13 and FIG. 14.

[0126] FIG. 13 is an equivalent circuit diagram of one pixel a liquid crystal display according to an exemplary embodiment of the invention. FIG. 14 is a layout view of a lower display panel of the liquid crystal display according to an exemplary embodiment of the invention.

[0127] A large portion of the configuration of the liquid crystal display according the exemplary embodiment of the invention is similar to the liquid crystal display accord-

ing to the fourth exemple, as shown in FIG. 13. Therefore, the detailed description is not provided and discussion will be directed towards the differences.

[0128] In the liquid crystal display according to the exemplary embodiment of the invention, unlike the liquid crystal display according to the fourth exemple, the second gate line is not provided but the first gate line GLn is provided and connected to a first switching element Qa and a second switching element Qb. The first gate line GLn and the second gate line are not discriminated, such that the first gate line GLn will be described as a gate line.

[0129] As shown in FIG. 13, the third switching element Qc is not connected to a specific gate line, a control terminal N1 is floated, an input terminal N3 is connected to the second switching element Qb, and an output terminal N2 is connected to the transforming capacitor Ct. Further, the transforming capacitor Ct is connected to the third liquid crystal capacitor Clcc.

[0130] If gate-on voltage is applied to the first gate line GLn, the first switching element Qa and the second switching element Qb connected thereto are turned on. Further, the same data signal may be applied through the data line DL, such that the first liquid crystal capacitor Clca and the second liquid crystal capacitor Clcb are charged with similar or near identical voltages.

[0131] As positive data voltage is applied through the data line DL, the voltage of the control terminal N1 may increase while the input terminal N3 of the third switching element Qc is charged with positive data voltage. Accordingly, current flows from the input terminal N3 to the output terminal N2 of the third switching element Qc and the voltage of the output terminal N2 correspondingly may increase.

[0132] If gate-off voltage is applied to the first gate line GLn, the current continues flowing from the input terminal N3 to the output terminal N2, until the voltage of the output terminal N2, the voltage of the input terminal N3, and the voltage of the control terminal N1 become the similar or near identical in the third switching element Qc. Accordingly, the voltage of the input terminal N3 may decrease and the voltage of the output terminal N2 may increase. As a result, the voltage of the second liquid crystal capacitor Clcb connected to the input terminal N3 of the third switching element Qc decreases under the positive data voltage that has been applied, such that it decreases under the voltage of the first liquid crystal capacitor Clca. Further, the voltage discharged from the second liquid crystal capacitor Clcb is divided to the transforming capacitor Ct and the third liquid crystal capacitor Clcc, such that a difference in voltage is generated between the second liquid crystal capacitor Clcb and the third liquid crystal capacitor Clcc. Accordingly, it may be possible to improve the side visibility of the liquid crystal display.

[0133] The structure of the liquid crystal display according to the exemplary embodiment of the invention, as shown in FIG. 14, has a large portion similar to the configuration of the liquid crystal display according to the fourth exemple; therefore, the detailed description is not provided and discussion will be directed towards the differences.

[0134] In the liquid crystal display according to the exemplary embodiment of the invention, unlike the fourth exemple, the second gate line is not specifically provided and but the first gate line 121a is provided.

[0135] The third gate electrode 124c is floated between the second subpixel electrode 191b and the third subpixel electrode 191c, without being connected to a specific gate line.

[0136] Further, similar to the fourth exemple, it is possible to make the thickness of the passivation layer 180 at the portion where the third drain electrode 175c and the third subpixel electrode 191c overlap smaller than the other portions.

[0137] In the liquid crystal display according to the exemplary embodiment, it may be possible to improve the side visibility by making a difference in voltage between the second subpixel electrode 191b and the third subpixel electrode 191c. Such a difference may be created using the third switching element (Qc in FIG. 13) with the control terminal floating and the transforming capacitor (Ct in FIG. 13) such that the subpixel electrodes (first subpixel electrode 191a, second subpixel electrode 191b, and third subpixel electrode 191c) have different voltages and three grays are implemented as a result.

[0138] A liquid crystal display according to a fifth exemple not according to invention is described hereafter in detail with reference to FIG. 15.

[0139] FIG. 15 is an equivalent circuit diagram of one pixel a liquid crystal display not according to the invention.

[0140] A liquid crystal display according to the fifth exemple, as shown in FIG. 15, includes a first switching element Qa and a second switching element Qb, a first liquid crystal capacitor Clca connected to the first switching element Qa, a second liquid crystal capacitor Clcb and a third liquid crystal capacitor Clcc connected to the second switching element Qb, and a third switching element Qc connected to the second switching element Qb.

[0141] Further, a first transforming capacitor Ct1 may be further formed between the second switching element Qb and the third liquid crystal capacitor Clcc. Also, a second transforming capacitor Ctz connected to the third switching element may be further formed.

[0142] The liquid crystal display according to the fifth exemple further includes a first gate line GLn, a second gate line GLn+1, and a data line DL. The first switching element Qa and the second switching element Qb may be three terminal elements of a thin film transistor etc., connected to the first gate line GLn to be switched by the same signal, and connected to the data line DL to receive the same data signal. The third switching element Qc may be a three terminal element of a thin film transistor etc., and connected to the second gate line GLn+1.

[0143] If gate-on voltage is applied to the first gate line (GLn), the first switching element Qa and the second switching element Qb are turned on and the same data

signal is applied through the data line DL, such that the first liquid crystal capacitor Clca and the second liquid crystal capacitor Clcb are charged with the similar or near identical voltage. The third liquid crystal capacitor Clcc is charged with voltage lower than the first liquid crystal capacitor Clca and second liquid crystal capacitor Clcb, due to the first transforming capacitor Ct1.

[0144] Thereafter, if gate-on voltage is applied to the second gate line GLn+1, which is the next gate line, the third switching element Qc is turned on and some of the charged voltage of the second liquid crystal capacitors Clcb and third liquid crystal capacitor Clcc is discharged to the second transforming capacitor Ctz. Therefore, the voltage of the second liquid crystal capacitor Clcb decreases under the voltage of the first liquid crystal capacitor Clca and the voltage of the third liquid crystal capacitor Clcb decreases under the voltage of the second liquid crystal capacitor Clcb. Accordingly, it may be possible to improve the side visibility of the liquid crystal display.

[0145] Although the structure of the liquid crystal display according to the fifth exemple is not shown, it may include a first substrate, one or more first gate lines and second gate lines and one or more data lines formed on the first substrate, a first switching element and a second switching element connected to the first gate line and the data line, a first subpixel electrode connected to the first switching element, a second subpixel electrode and a third subpixel electrode connected to the second switching element, a first transforming capacitor formed between the second switching element and the third subpixel electrode, a third switching element connected to the second switching element and switched by the second gate line, and a second transforming capacitor connected to the third switching element.

[0146] Further, it may further include a second substrate opposite to the first substrate, a common electrode formed on the second substrate, and a liquid crystal layer formed between the first substrate and the second substrate.

[0147] In the liquid crystal displays according to the third to fifth exemples and according to the exemplary embodiment of the invention, the first subpixel electrode 191a, the second subpixel electrode 191b, and the third subpixel electrode 191c have different voltages and three grays may be implemented as a result, thereby improving the side visibility.

[0148] Hereinafter, the maximum area ratio and voltage ratio of the subpixel electrodes (first subpixel electrode 191a, second subpixel electrode 191b, and third subpixel electrode 191c) for improving the side visibility of the liquid crystal displays according to the third to fifth examples and according to the exemplary embodiment of the invention are described with reference to FIG. 16, FIG. 17, FIG. 18, and FIG. 19.

[0149] FIG. 16 is a graph showing a V-T curve at the front and the side of a liquid crystal display according to the related art. FIG. 17 is a graph showing a V-T curve at the front and the side of a liquid crystal display according to an exemplary embodiment of the invention. FIG. 18 is a graph showing a V-T curve at the front and the side of a liquid crystal display according to an exemplary embodiment of the invention. FIG. 19 at the front and the side of a liquid crystal display according to an exemplary embodiment of the invention.

[0150] In FIG. 16, FIG. 17, FIG. 18 and FIG. 19, the horizontal axis represents data voltage, the vertical axis represents transmittance, the solid line represents the front visibility, and the dotted line represents the side visibility.

[0151] A liquid crystal display according to the related art may have a problem in that, as shown in FIG. 16, bumping may be generated at a time when a pixel electrode where voltage showing a low gray is applied is turned on, if the difference between the voltage showing a high gray and the voltage showing a low gray is large in the method of dividing one pixel in two subpixels and applying different voltages thereto.

[0152] In the liquid crystal display according to an exemplary embodiment of the invention, as shown in FIG. 17, FIG. 18 and FIG. 19, the section where the bumping period, as shown in FIG. 16, is removed by dividing one pixel in three subpixels with different voltages.

[0153] FIG. 17, FIG. 18, and FIG. 19 show several typical experimental examples, in which the voltage ratio of the first subpixel electrode, second subpixel electrode, and third subpixel electrode may be 1: 0.6 to 0.85 : 0.4 to 0.7. Further, the area ratio of the first subpixel electrode, second subpixel electrode, and third subpixel electrode may be 1: 1 to 2 : 1 to 2. While the voltage ratio and the area ratio may not be limited to the exemplary ratios provided,

[0154] It will be apparent to those skilled in the art that various modifications and variation can be made in the present invention without departing from scope of the invention as defined in the appended claims. Thus, it is intended that the present invention cover the modifications and variations of this invention provided within the scope of the appended claims.

Claims

1. A liquid crystal display having three subpixel electrodes, comprising:

a first substrate;
a second substrate;
a common electrode formed on the second substrate; and
a liquid crystal layer formed between the first substrate and the second substrate;
a gate line (GLn) and a data line (DL) formed on the first substrate;
a first gate electrode (124a), a first source electrode (173a), and a first drain electrode (175a) constituting a first switching element (Qa);

a second gate electrode (124b), a second source electrode (173b), and a second drain electrode (175b) constituting a second switching element (Qb);
a third gate electrode (124c), a third source electrode (173c), and a third drain electrode (175c) constituting a third switching element (Qc);
the first switching element (Qa) and the second switching element (Qb) are formed on the first substrate and configured to be switched by the same signal
wherein the first gate electrode (124a) of the first switching element (Qa) and the second gate electrode (124b) of the second switching element (Qb) are connected to the gate line (GLn), and the first source electrode (173a) of the first switching element (Qa) and the second source electrode (173b) of the second switching element (Qb) are connected to the data line (DL), and the third source electrode (173c) of the third switching element (Qc) is connected to the second drain electrode (175b) of the second switching element (Qb);
a first subpixel electrode (191a) is connected to the first drain electrode (175a) of the first switching element (Qa);
a second subpixel electrode (191b) is connected to the second drain electrode (175b) of the second switching element (Qb);
a third subpixel electrode (191c) is connected to the third drain electrode (175c) of the third switching element (Qc);
characterized in that:
the third gate electrode (124c) is floated between the second subpixel electrode (191b) and the third subpixel electrode (191c) without being connected to a specific gate line (GLn).

2. The liquid crystal display of claim 1 arranged so that the voltage of the first subpixel electrode (191a) is higher than the voltage of the second subpixel electrode (191b), and the voltage of the second subpixel electrode (191b) is higher than the voltage of the third subpixel electrode (191c) in response to the first and second switching elements (Qa, Qb) being switched by a signal received from the gate line (GLn).

3. The liquid crystal display of claim 2, arranged so that a voltage ratio of the first subpixel electrode (191a) to the second subpixel electrode (191b) is 1: 0.6 - 0.85, and a voltage ratio of the first subpixel electrode (191a) to the third subpixel electrode (191c) is 1: 0.4 - 0.7.

4. The liquid crystal display of claim 2, wherein an area ratio of the first subpixel electrode (191a) to the second subpixel electrode (191b) is 1 : 1 - 2, and an area ratio of the first subpixel electrode (191a) to the third subpixel electrode (191c) is 1:1-2.

Patentansprüche

1. Flüssigkristallanzeige mit drei Subpixel-Elektroden, umfassend:

ein erstes Substrat;
ein zweites Substrat;
eine gemeinsame Elektrode, die auf dem zweiten Substrat gebildet ist;
und
eine Flüssigkristallschicht, die zwischen dem ersten Substrat und dem zweiten Substrat gebildet ist;
eine Gate-Leitung (GLn) und eine Datenleitung (DL), die auf dem ersten Substrat gebildet sind;
eine erste Gate-Elektrode (124a), eine erste Source-Elektrode (173a) und
eine erste Drain-Elektrode (175a), die ein erstes Schaltelement (Qa) bilden;
eine zweite Gate-Elektrode (124b), eine zweite Source-Elektrode (173b) und eine zweite Drain-Elektrode (175b), die ein zweites Schaltelement (Qb) bilden;
eine dritte Gate-Elektrode (124c), eine dritte Source-Elektrode (173c) und
eine dritte Drain-Elektrode (175c), die ein drittes Schaltelement (Qc) bilden;
wobei das erste Schaltelement (Qa) und das zweite Schaltelement (Qb) auf dem ersten Substrat gebildet sind und dafür ausgelegt sind, durch das gleiche Signal geschaltet zu werden;
wobei die erste Gate-Elektrode (124a) des ersten Schaltelements (Qa) und
die zweite Gate-Elektrode (124b) des zweiten Schaltelements (Qb) mit der Gate-Leitung (GLn) verbunden sind, und wobei die erste Source-Elektrode (173a) des ersten Schaltelements (Qa) und die zweite Source-Elektrode (173b) des zweiten Schaltelements (Qb) mit der Datenleitung (DL) verbunden sind, und wobei die dritte Source-Elektrode (173c) des dritten Schaltelements (Qc) mit der zweiten Drain-Elektrode (175b) des zweiten Schaltelements (Qb) verbunden ist;
wobei eine erste Subpixel-Elektrode (191a) mit der ersten Drain-Elektrode (175a) des ersten Schaltelements (Qa) verbunden ist;
wobei eine zweite Subpixel-Elektrode (191b) mit der zweiten Drain-Elektrode (175b) des zweiten Schaltelements (Qb) verbunden ist;
wobei eine dritte Subpixel-Elektrode (191c) mit der dritten Drain-Elektrode (175c) des dritten Schaltelements (Qc) verbunden ist;
dadurch gekennzeichnet, dass

sich die dritte Gate-Elektrode (124c) floatend zwischen der zweiten Subpixel-Elektrode (191b) und der dritten Subpixel-Elektrode (191c) befindet, ohne mit einer spezifischen Gate-Leitung (GLn) verbunden zu sein.

2. Flüssigkristallanzeige nach Anspruch 1, derart angeordnet, dass die Spannung der ersten Subpixel-Elektrode (191a) höher als die Spannung der zweiten Subpixel-Elektrode (191b) ist und dass die Spannung der zweiten Subpixel-Elektrode (191b) höher als die Spannung der dritten Subpixel-Elektrode (191c) ist, wenn die ersten und zweiten Schaltelemente (Qa, Qb) durch ein von der Gate-Leitung (GLn) eingehendes Signal geschaltet werden.

3. Flüssigkristallanzeige nach Anspruch 2, derart angeordnet, dass ein Spannungsverhältnis der ersten Subpixel-Elektrode (191a) zur zweiten Subpixel-Elektrode (191b) 1 : 0,6 - 0,85 beträgt und ein Spannungsverhältnis der ersten Subpixel-Elektrode (191a) zur dritten Subpixel-Elektrode (191c) 1 : 0,4 - 0,7 beträgt.

4. Flüssigkristallanzeige nach Anspruch 2, wobei ein Flächenverhältnis der ersten Subpixel-Elektrode (191a) zur zweiten Subpixel-Elektrode (191b) 1 : 1 - 2 beträgt und ein Flächenverhältnis der ersten Subpixel-Elektrode (191a) zur dritten Subpixel-Elektrode (191c) 1 : 1 - 2 beträgt.

Revendications

1. Un écran à cristaux liquides ayant trois électrodes de sous-pixel comprenant :

Un premier substrat ;
Un deuxième substrat ;
Une électrode ordinaire formée sur le deuxième substrat ; et
Une couche de cristaux liquides formée entre le premier substrat et le deuxième substrat ;
Une ligne de grille (GLn) et une ligne de données (DL) formée sur le premier substrat ;
Une première électrode de grille (124a), une première électrode source (173a) et une première électrode déversoir (175a) constituant un premier élément de commutation (Qa) ;
Une deuxième électrode de grille (124b), une deuxième électrode source (173b) et une deuxième électrode déversoir (175b) constituant un deuxième élément de commutation (Qb) ;
Une troisième électrode de grille (124c), une troisième électrode source (173c) et une troisième électrode déversoir (175c) constituant un troisième élément de commutation (Qc) ;
Le premier élément de commutation (Qa) et le deuxième élément de commutation (Qb) sont formés sur le premier substrat et configurés pour être commutés par le même signal,
Où la première électrode de grille (124a) du premier élément de commutation (Qa) et la deuxième électrode de grille (124b) du deuxième élément de commutation (Qb) sont connectées à la ligne de grille (GLn),
et la première électrode source (173a) du premier élément de commutation (Qa) et la deuxième électrode source (173b) du deuxième élément de commutation (Qb) sont connectées à la ligne de données (DL), et la troisième électrode source (173c) du troisième élément de commutation (Qc) est connectée à la deuxième électrode déversoir (175b) du deuxième élément de commutation (Qb) ;
Une première électrode de sous-pixel (191a) est connectée à la première électrode déversoir (175a) du premier élément de commutation (Qa) ;
Une deuxième électrode sous-pixel (191b) est connectée à la deuxième électrode déversoir (175b) du deuxième élément de commutation (Qb) ;
Une troisième électrode sous-pixel (191c) est connectée à la troisième électrode déversoir (175c) du troisième élément de commutation (Qc) ;
Caractérisé en ce que :

La troisième électrode de grille (124c) oscille entre la deuxième électrode sous-pixel (191b) et la troisième électrode sous-pixel (191c) sans être connectée à une ligne de grille (GLn) spécifique.

2. L'écran à cristaux liquides de la revendication 1 disposé de sorte que la tension de la première électrode sous-pixel (191a) soit supérieure à la tension de la deuxième électrode sous-pixel (191b) et la tension de la deuxième électrode sous-pixel (191b) soit supérieure à la tension de la troisième électrode sous-pixel (191c) en réponse au premier et au deuxième éléments de commutation (Qa, Qb) étant commutés par un signal reçu à partir de la ligne de grille (GLn).

3. L'écran à cristaux liquides de la revendication 2, disposé de sorte que le rapport de tension de la première électrode sous-pixel (191a) à la deuxième électrode sous-pixel (191b) soit 1 :0,6 - 0,85, et un rapport de tension de la première électrode sous-pixel (191a) à la troisième électrode sous-pixel (191c) soit 1 :0,4 - 0,7.

4. L'écran à cristaux liquides de la revendication 2, où un rapport de section de la première électrode sous-

pixel (191a) à la deuxième électrode sous-pixel (191b) est 1 : 1 - 2, et un rapport de section de la première électrode sous-pixel (191a) à la troisième électrode sous-pixel (191c) est 1 : 1 - 2.

FIG. 1

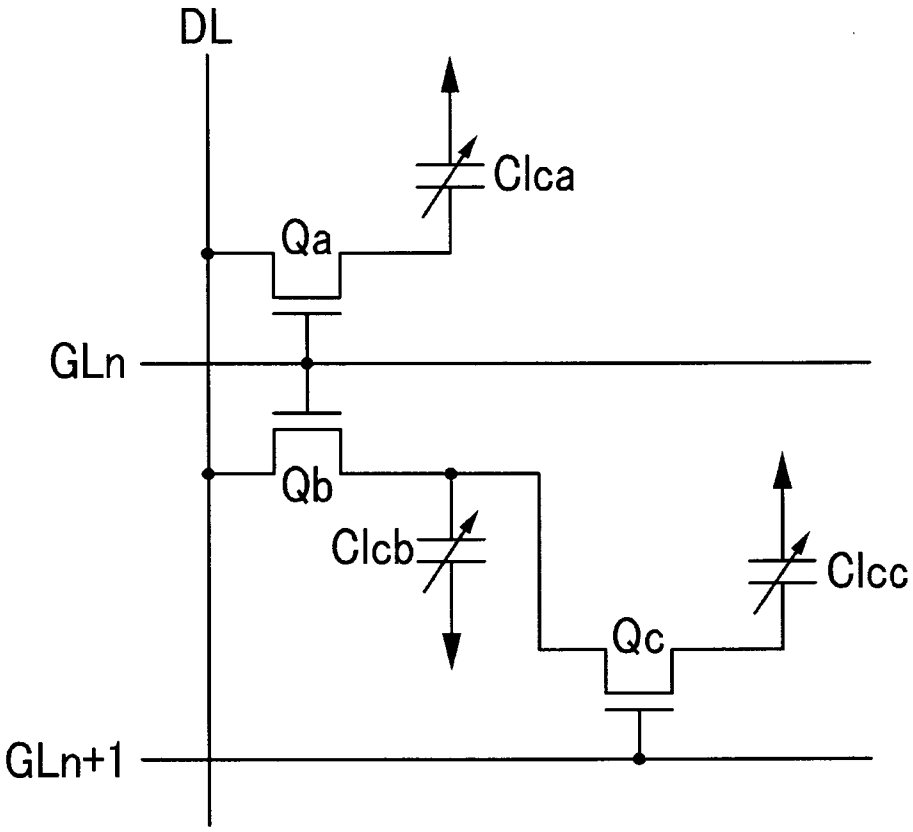


FIG. 2

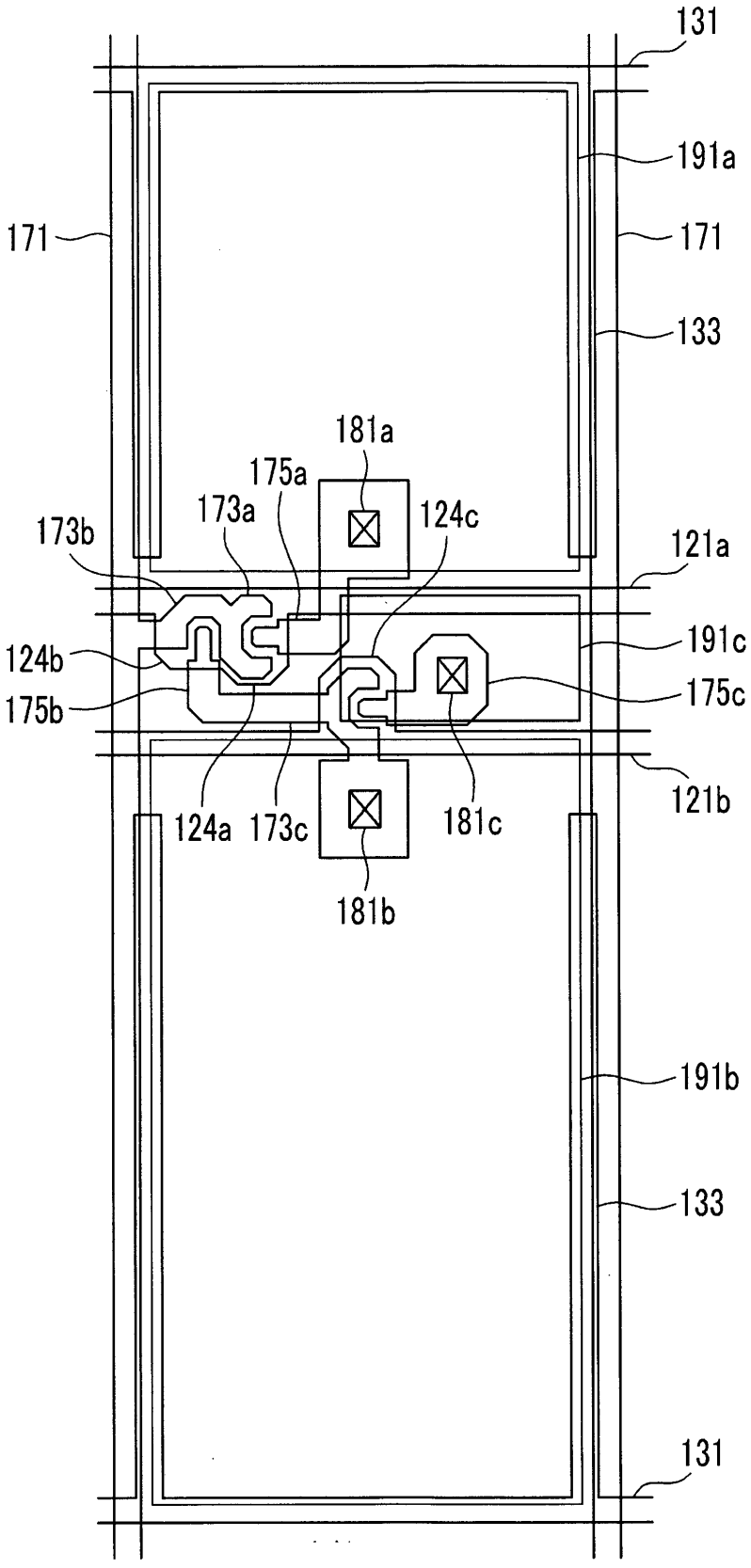

131
191a
171
171
133
181a
175a
173a
124c
173b
121a
191c
124b
175b
175c
121b
124a
173c
181c
181b
191b
133
131

FIG.3

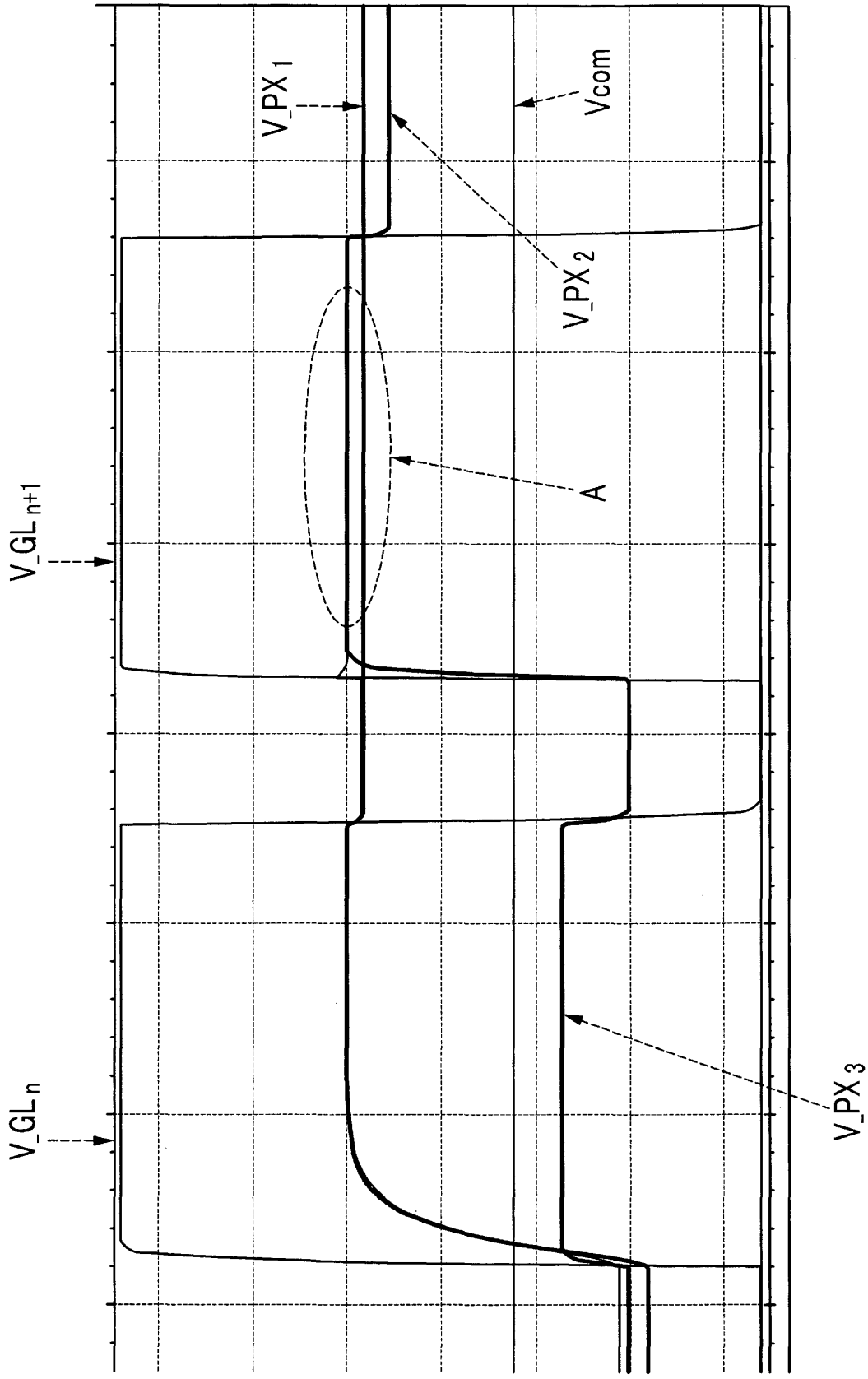


FIG. 4

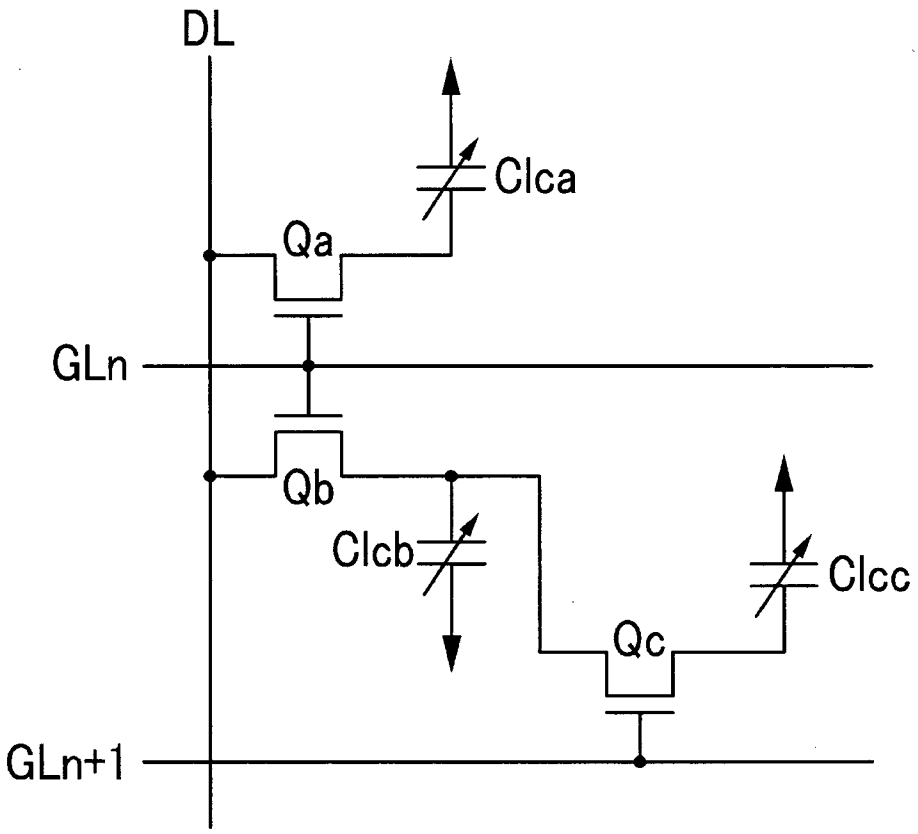


FIG.5

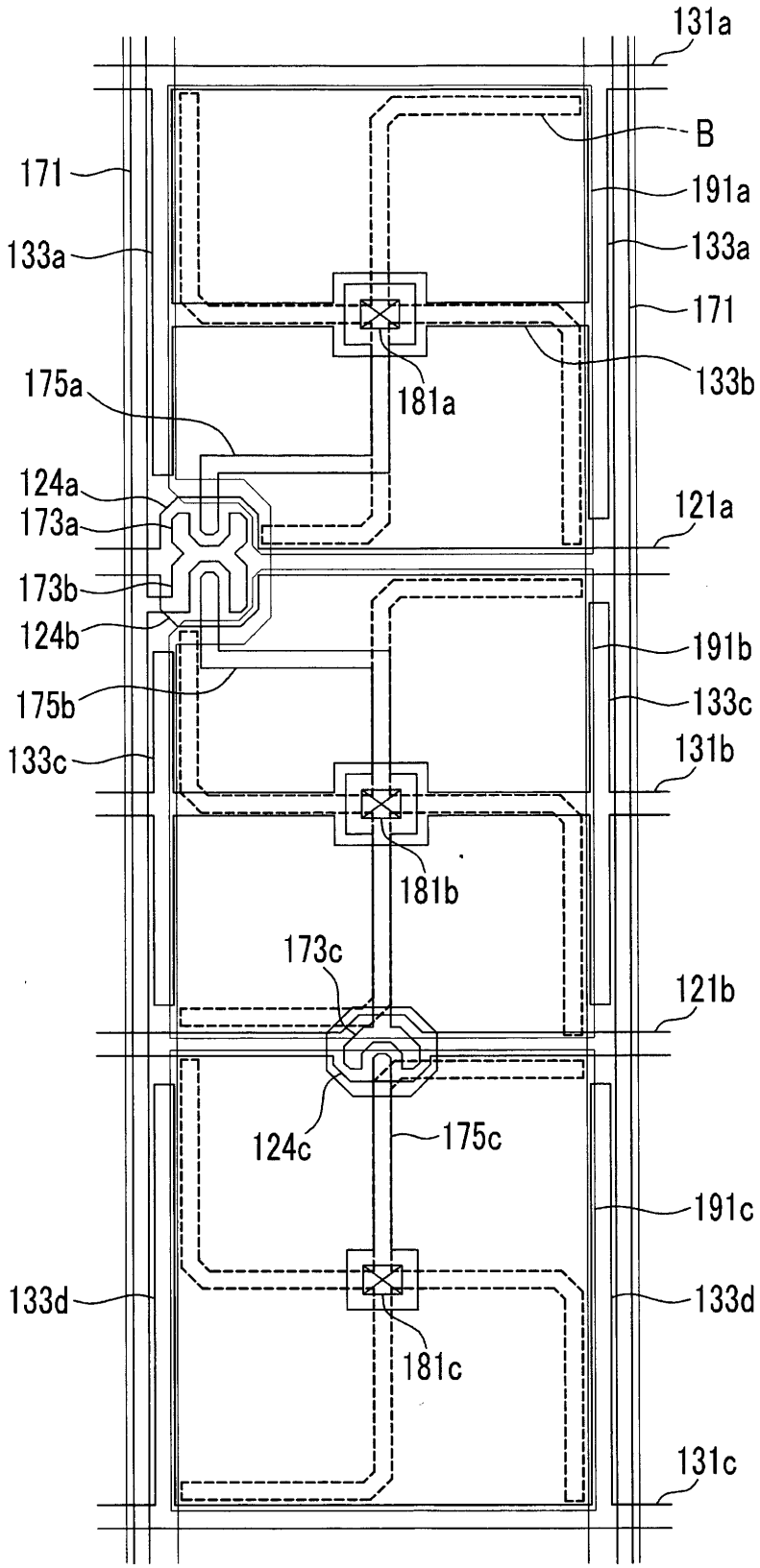

131a
B
171
191a
133a
133a
171
181a
133b
175a
124a
173a
121a
173b
124b
191b
175b
133c
133c
131b
181b
173c
121b
124c
175c
191c
133d
133d
181c
131c

FIG. 6

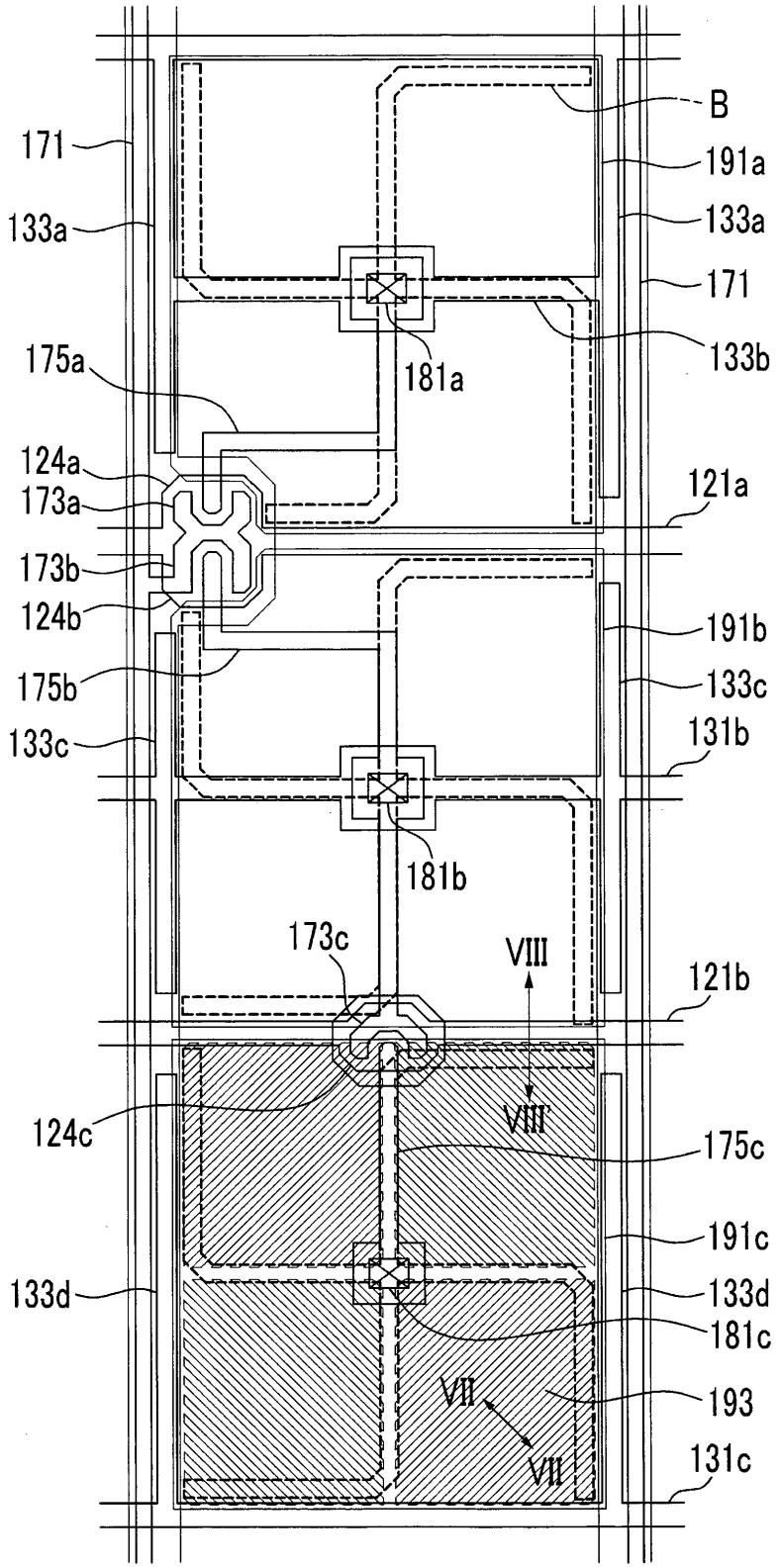

B
171
191a
133a
133a
171
181a
133b
175a
124a
173a
121a
173b
124b
191b
175b
133c
133c
131b
181b
173c
VIII
121b
124c
VIII'
175c
191c
133d
133d
181c
VII
193
VII
131c

FIG. 7

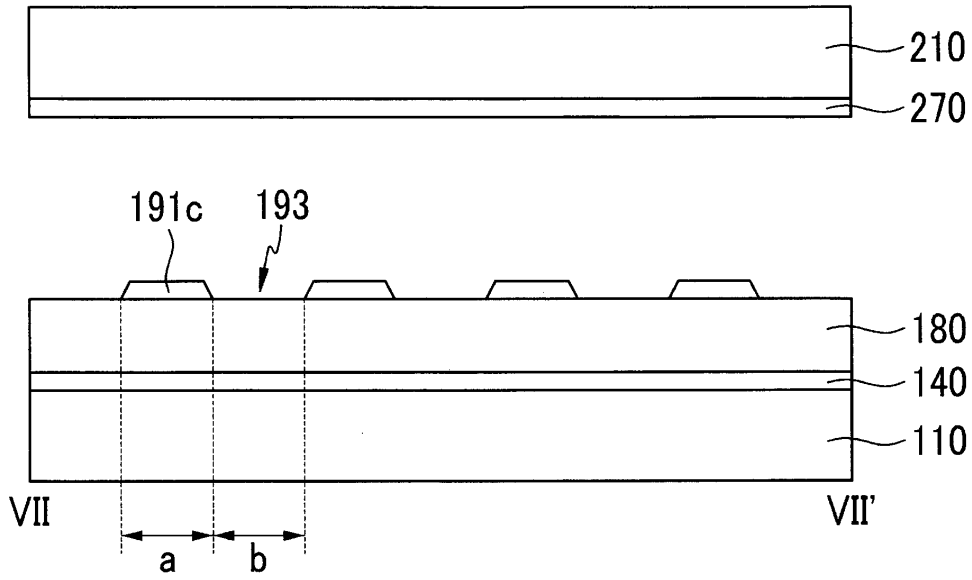

210
270
191c
193
180
140
110
VII
VII'
a
b

FIG. 8

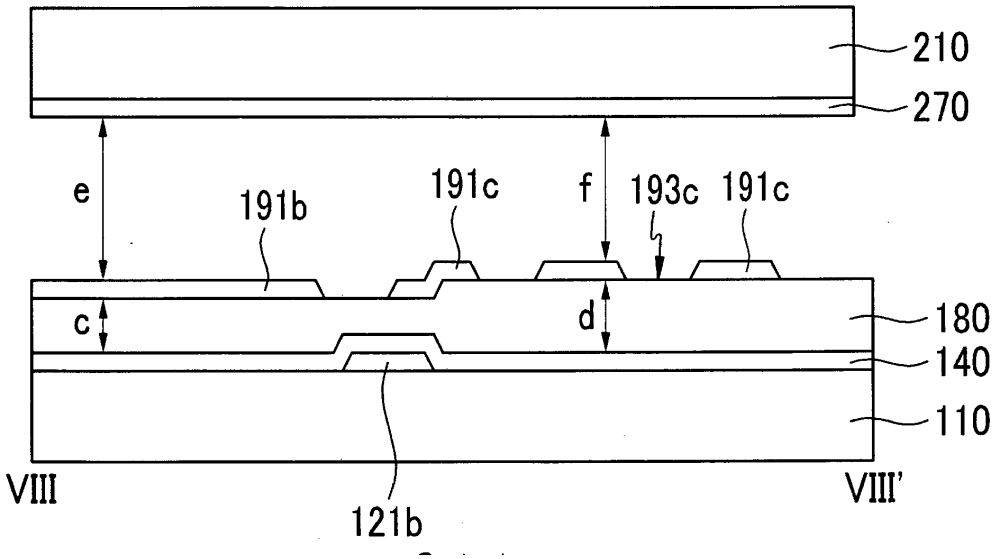

210
270
e
191b
191c
f
193c
191c
c
d
180
140
110
VIII
VIII'
121b

FIG. 9

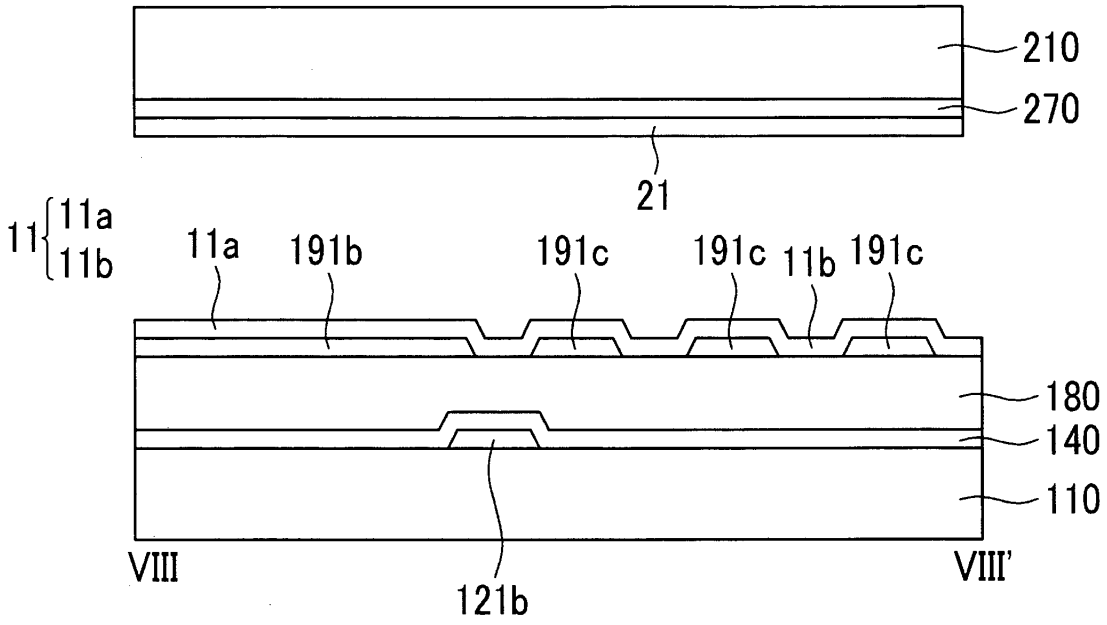

210
270
21
11
11a
11b
11a
191b
191c
191c
11b
191c
180
140
110
VIII
VIII'
121b

FIG. 10

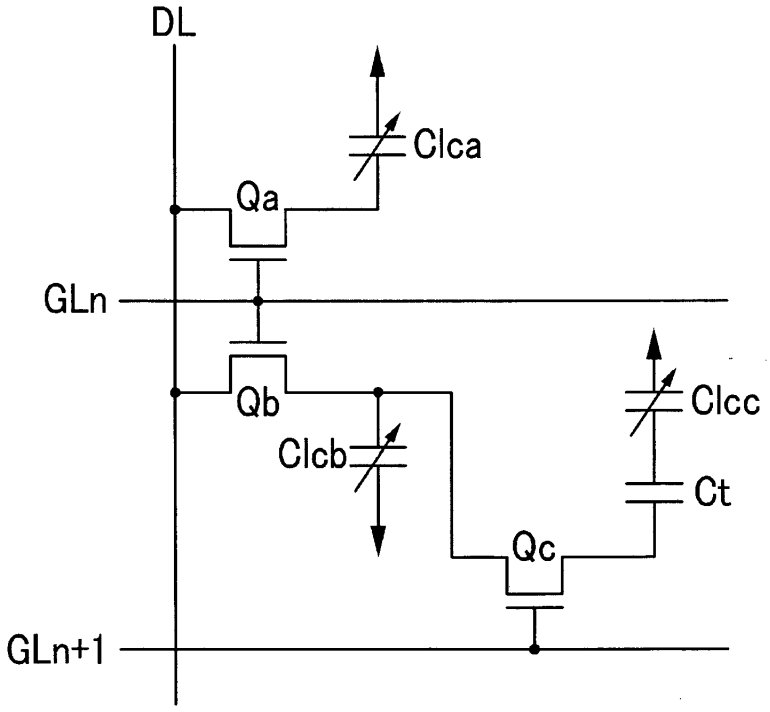

DL
Clca
Qa
GLn
Qb
Clcb
Clcc
Ct
Qc
GLn+1

FIG.11

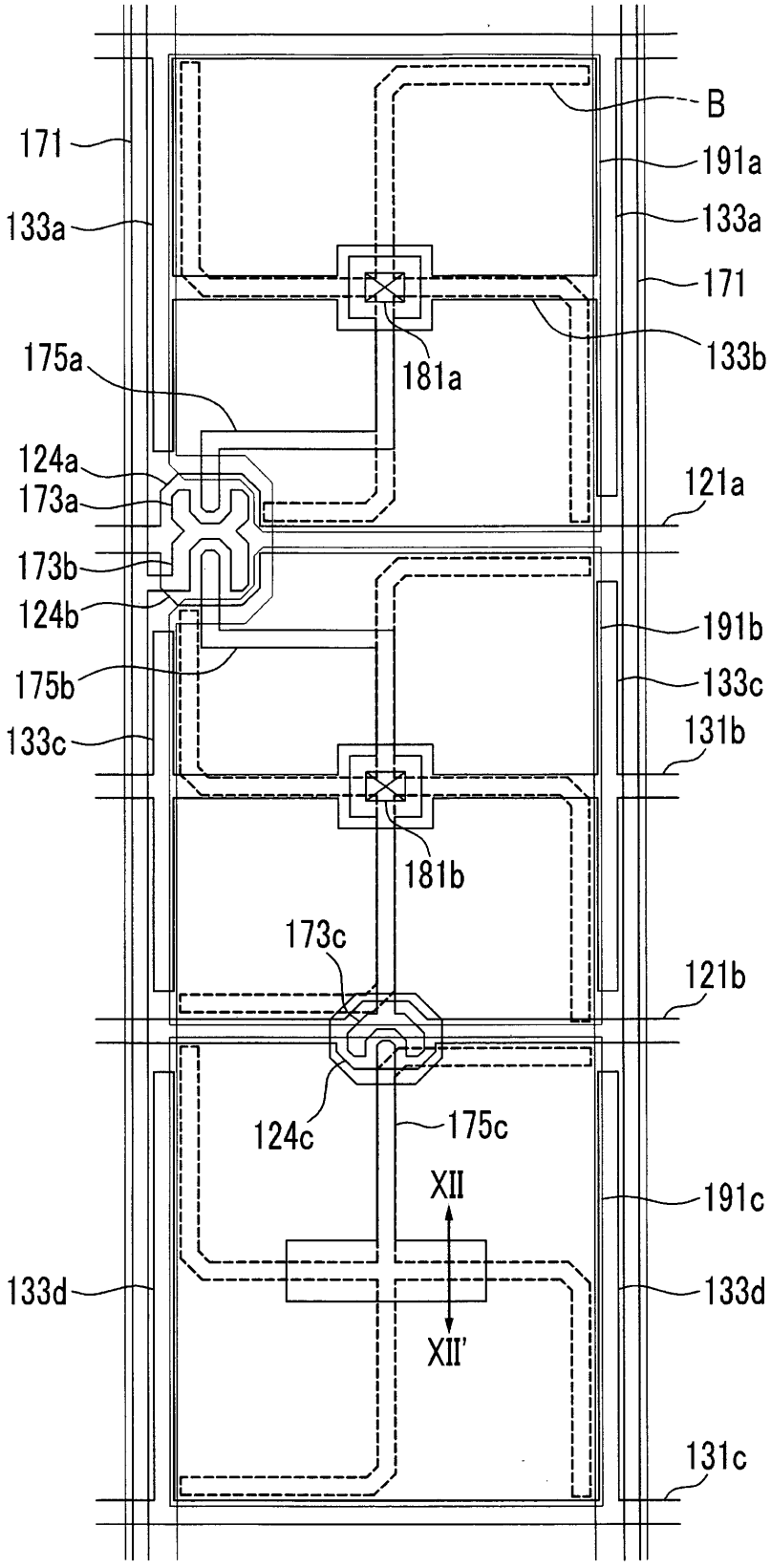

B
171
191a
133a
133a
171
181a
133b
175a
124a
173a
121a
173b
124b
191b
175b
133c
133c
131b
181b
173c
121b
124c
175c
XII
191c
133d
133d
XII'
131c

FIG. 12

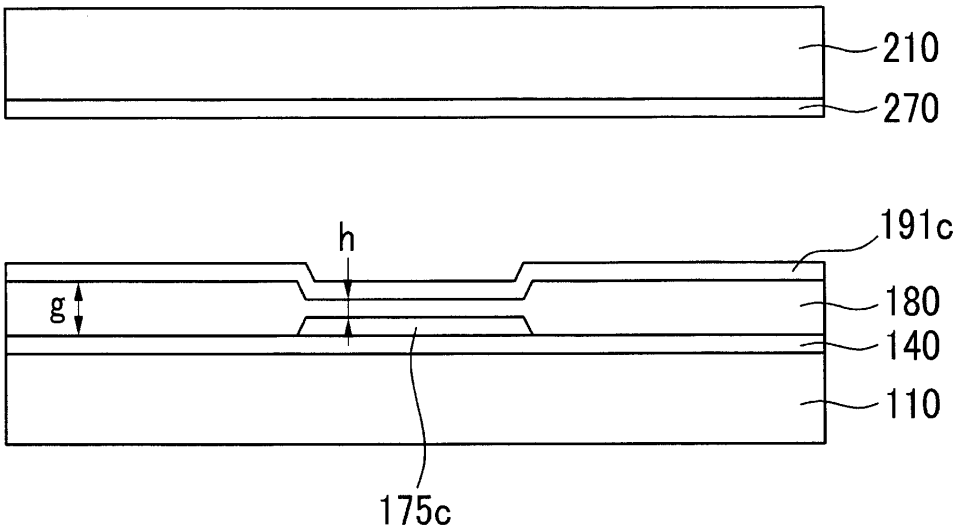

210
270
h
191c
g
180
140
110
175c

FIG. 13

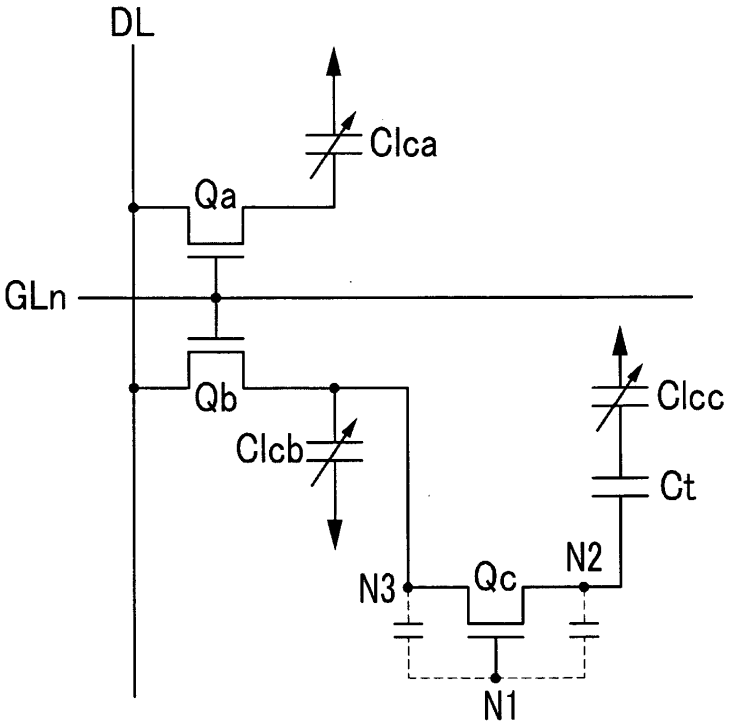

DL
Clca
Qa
GLn
Qb
Clcb
Clcc
Ct
N3
Qc
N2
N1

FIG. 14

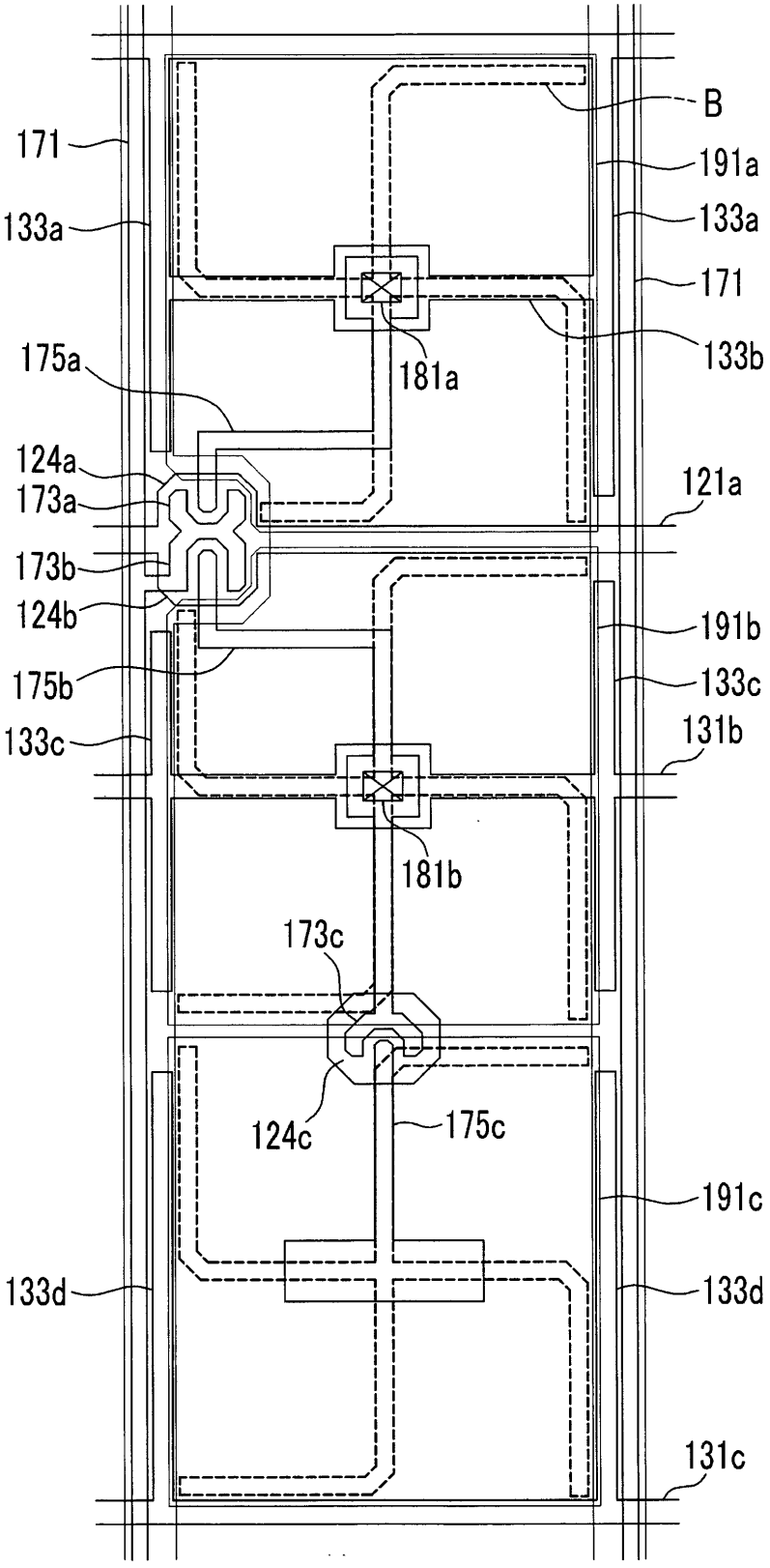

B
171
191a
133a
133a
171
181a
133b
175a
124a
173a
121a
173b
124b
191b
175b
133c
133c
131b
181b
173c
124c
175c
191c
133d
133d
131c

FIG.15

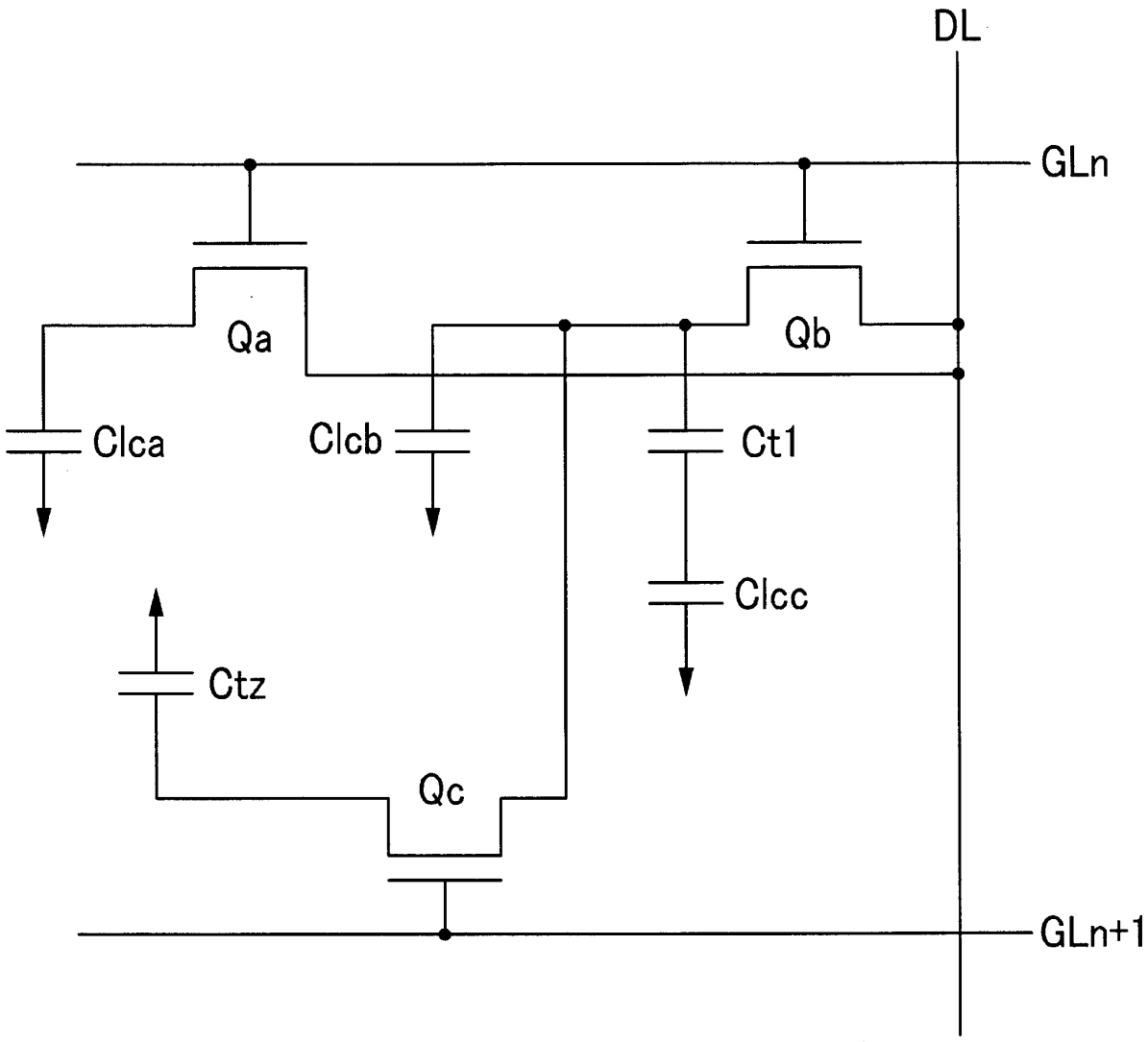


FIG.16

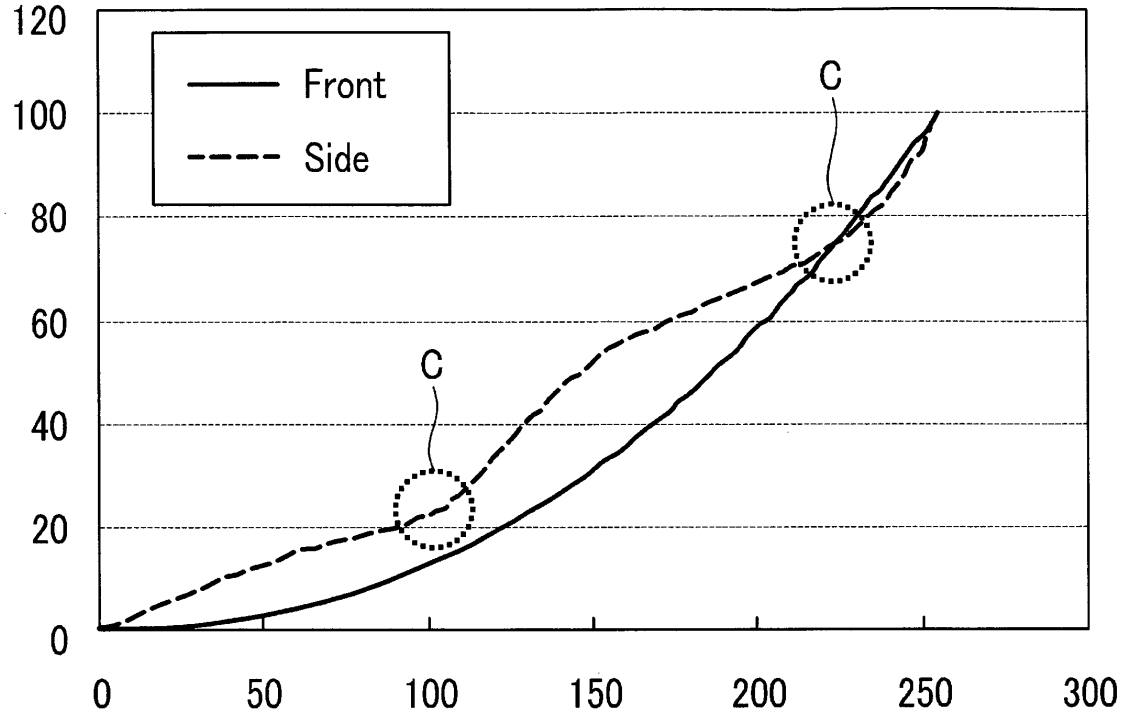

120
100
80
60
40
20
0
0
50
100
150
200
250
300
Front
Side
C
C

FIG.17

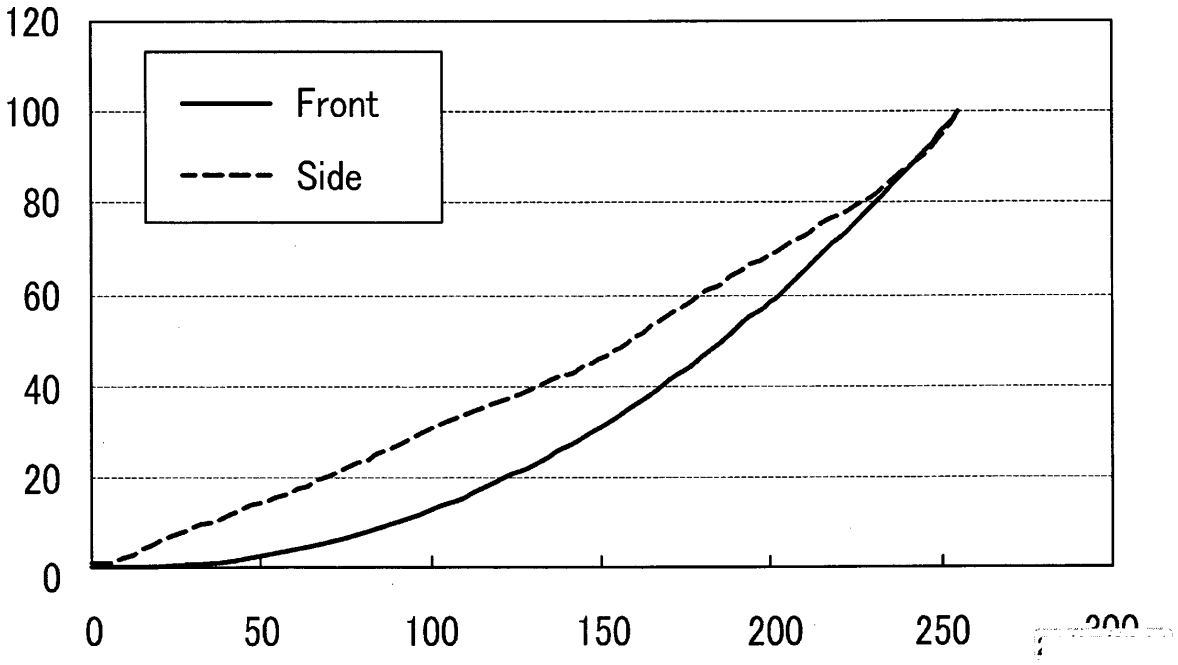

120
100
80
60
40
20
0
0
50
100
150
200
250
Front
Side

FIG.18

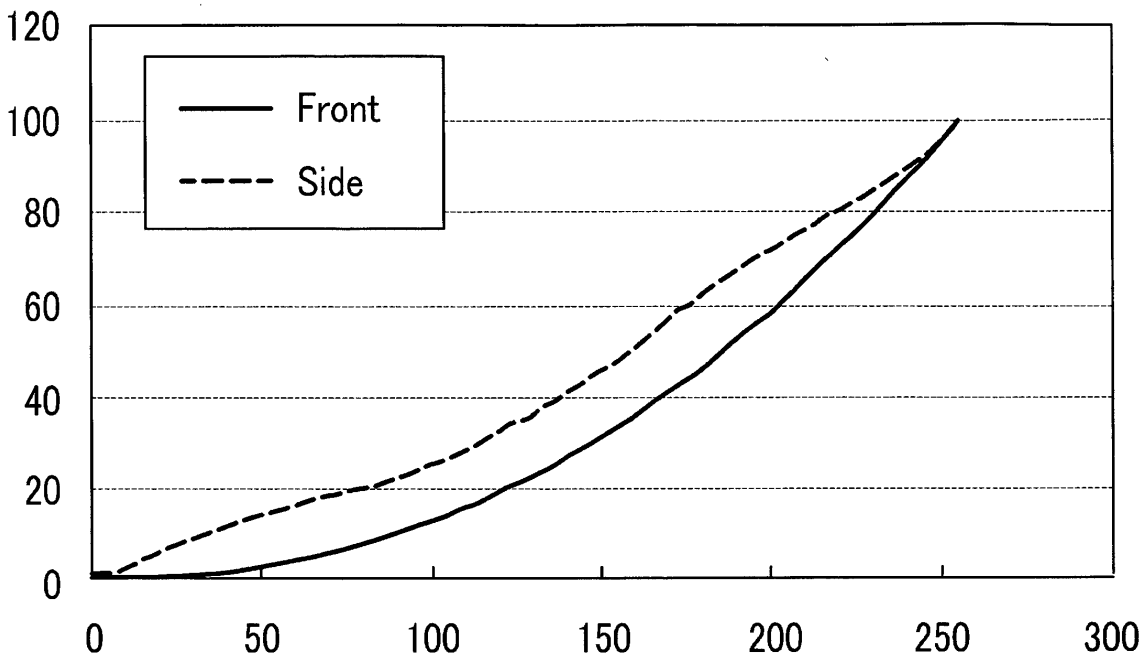
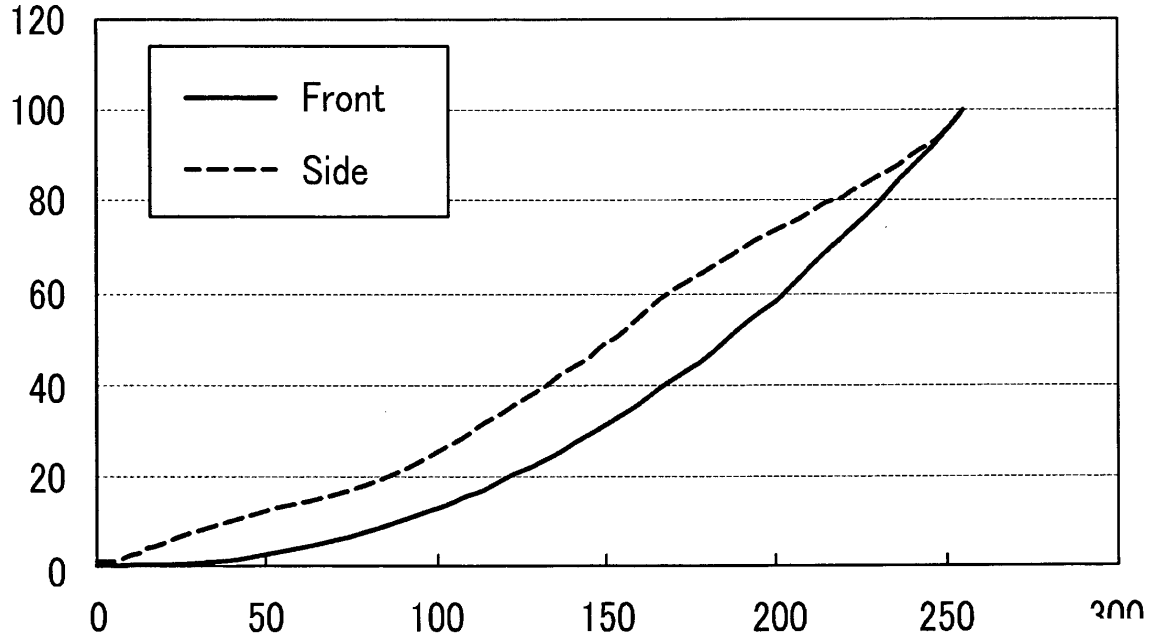

120
100
80
60
40
20
0
Front
Side
0
50
100
150
200
250
300

FIG.19


120
100
80
60
40
20
0
Front
Side
0
50
100
150
200
250
300

REFERENCES CITED IN THE DESCRIPTION

This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

Patent documents cited in the description

- US 20070064164 A **[0007]**
- US 20060023137 A **[0007]**

专利名称(译)	液晶显示器增加侧视能见度		
公开(公告)号	EP2466369B1	公开(公告)日	2014-05-21
申请号	EP2011174814	申请日	2011-07-21
[标]申请(专利权)人(译)	三星电子株式会社		
申请(专利权)人(译)	SAMSUNG ELECTRONICS CO.，LTD.		
当前申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
[标]发明人	CHANG HAK SUN SHIN KYOUNG JU SHIN YONG HWAN		
发明人	CHANG, HAK SUN SHIN, KYOUNG JU SHIN, YONG HWAN		
IPC分类号	G02F1/1362		
CPC分类号	G02F1/133371 G02F1/133707 G02F1/133753 G02F1/13624 G02F2001/134345 G02F2201/40 G02F1/134309 G02F1/136213 G02F1/136286 G02F1/1368		
代理机构(译)	DR.威猛和合作伙伴		
优先权	1020100127627 2010-12-14 KR		
其他公开文献	EP2466369A1		
外部链接	Espacenet		

摘要(译)

提供一种液晶显示器，其提供改善的透射率和可见度，包括第一基板;第一开关元件和第二开关元件，形成在第一基板上，被配置为通过相同的信号进行开关;第一子像素电极，连接到第一开关元件;第二子像素电极，连接到第二开关元件;第三开关元件，连接到第二开关元件;第三子像素电极，连接到第三开关元件;第二基板;形成在第二基板上的公共电极;以及在第一基板和第二基板之间形成的液晶层。

FIG. 1