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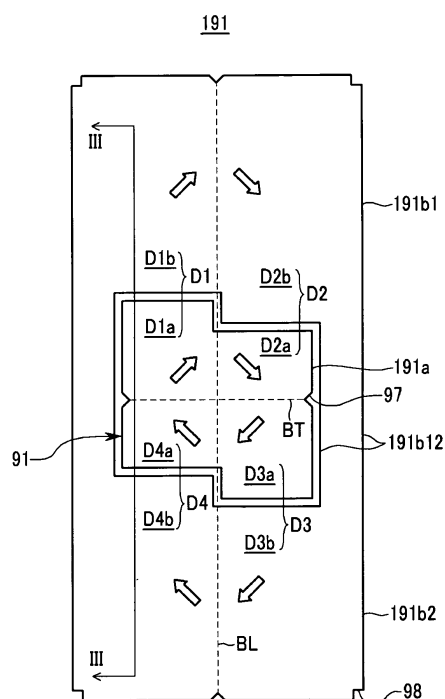
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(54) **Liquid crystal display and panel thereof**

(57) A liquid crystal panel according to an exemplary embodiment of the present invention includes a substrate, and a pixel electrode arranged on the substrate. The pixel electrode (191) includes a first subpixel electrode (191a) and a second subpixel electrode (191b) separated from each other, and the second subpixel electrode includes a first electrode part disposed above the first subpixel electrode and a second electrode part disposed below the first subpixel electrode and connected to the first electrode part. At least one first notch (97) is arranged on at least one edge of the first subpixel electrode or the second subpixel electrode.

FIG. 2



## Description

### BACKGROUND OF THE INVENTION

#### [0001] FIELD OF THE INVENTION

[0002] The present invention relates to a liquid crystal display and a display panel thereof.

#### [0003] DISCUSSION OF THE BACKGROUND

[0004] A liquid crystal display (LCD) is one of the most widely used flat panel displays, and includes a pair of panels provided with field-generating electrodes, such as pixel electrodes and a common electrode, and a liquid crystal (LC) layer interposed between the two panels. The LCD displays images by applying voltages to the field-generating electrodes, which generate an electric field in the LC layer that determines the orientations of LC molecules therein to adjust polarization of incident light.

[0005] Among LCDs, a vertical alignment (VA) mode LCD, which aligns LC molecules such that the long axes of the LC molecules are perpendicular to the panels in the absence of an electric field, is of interest because of its high contrast ratio and wide reference viewing angle.

[0006] In the VA mode LCD, a wide viewing angle may be obtained by forming a plurality of domains having different alignment directions of the liquid crystal in one pixel.

[0007] The plurality of domains in one pixel can be realized by forming cutouts in the field-generating electrodes. In this method, a plurality of domains may be formed by aligning the LC molecules vertically with respect to the fringe field generated between the edges of the cutout and the field generating electrodes facing the edges.

[0008] However, the aperture ratio is decreased in this structure. Also, while the LC molecules disposed near the cutouts are easily aligned vertically with respect to the fringe field, the LC molecules disposed in the central portions of the domains far from the cutouts are affected by a random motion such that the response speed becomes slow and a domain of the opposite direction is formed such that an instant afterimage may appear.

[0009] As another means for forming the plurality of domains in one pixel, there is a light alignment method in which the alignment direction of the LC molecules and the alignment angle are controlled by irradiating light on the alignment layer. In the light alignment method, it is not necessary to form cutouts in the field generating electrode, so the aperture ratio may be increased and the response time of the LC molecules may be improved by a pretilt angle generated under the light alignment.

[0010] On the other hand, a VA mode LCD may have lower side visibility than front visibility, so one pixel is divided into two subpixels and different voltages are applied to the subpixels to solve this problem.

[0011] However, when the light alignment method is applied to the structure having two divided subpixels, the alignment direction determined by the light alignment

may be different from the alignment direction of the LC molecules determined by the fringe field generated at a gap between the two subpixels of the LCD such that texture may be generated. The texture decreases transmittance and may appear as a stain such that the display characteristics of the LCD may be deteriorated.

### SUMMARY OF THE INVENTION

[0012] The present invention provides a liquid crystal display and a display panel thereof.

[0013] Additional features of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention.

[0014] The present invention discloses a liquid crystal panel that includes a substrate and a pixel electrode disposed on the substrate. The pixel electrode includes a first subpixel electrode and a second subpixel electrode, wherein the second subpixel electrode includes a first electrode part disposed above the first subpixel electrode, and a second electrode part disposed below the first subpixel electrode and connected to the first subpixel electrode. At least one first notch is arranged on at least one edge of the first subpixel electrode or the second subpixel electrode.

[0015] The present invention also discloses a liquid crystal display that includes a first substrate, a pixel electrode disposed on the first substrate. The pixel electrode includes a first subpixel electrode and a second subpixel electrode separated from each other, a second substrate facing the first substrate, a common electrode arranged on the second substrate, and a liquid crystal layer interposed between the pixel electrode and the common electrode, wherein the second subpixel electrode includes a first electrode part disposed on the first subpixel electrode, a second electrode part disposed under the first subpixel electrode and connected to the first subpixel electrode, and a plurality of connection pieces connecting the first electrode part and the second electrode part on right and left sides of the first subpixel electrode, and wherein first notches are arranged near a center of an upper edge and a lower edge of the first subpixel electrode, and near a center of a left edge and a right edge of the second subpixel electrode.

[0016] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

### BRIEF DESCRIPTION OF THE DRAWINGS

[0017] FIG. 1 is an equivalent circuit diagram of one pixel of the liquid crystal display according to an exemplary embodiment of the present invention.

[0018] FIG. 2 is a layout view of a pixel electrode in a liquid crystal display according to an exemplary embodiment of the present invention.

**[0019]** FIG. 3 is a cross-sectional view of the liquid crystal display including the pixel electrode shown in FIG. 2, taken along line III-III of FIG. 2.

**[0020]** FIG. 4, FIG. 5, and FIG. 6 are layout views of a pixel electrode according to another exemplary embodiment of the present invention.

**[0021]** FIG. 7 is a layout view of a liquid crystal display according to an exemplary embodiment of the present invention.

**[0022]** FIG. 8 is a layout view of a pixel electrode of the liquid crystal display shown in FIG. 7.

**[0023]** FIG. 9 is a layout view of a storage electrode line of the liquid crystal display shown in FIG. 7.

**[0024]** FIG. 10 is a layout view showing an alignment direction of liquid crystal molecules over the pixel electrode in the liquid crystal display of FIG. 7.

**[0025]** FIG. 11 is a cross-sectional view of the liquid crystal display shown in FIG. 7 taken along line XI-XI of FIG. 7.

#### DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

**[0026]** The invention is described more fully hereinafter with reference to the accompanying drawings, in which embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure is thorough, and will fully convey the scope of the invention to those skilled in the art. In the drawings, the size and relative sizes of layers and regions may be exaggerated for clarity. Like reference numerals in the drawings denote like elements.

**[0027]** It will be understood that when an element or layer is referred to as being "on" or "connected to" another element or layer, it can be directly on or directly connected to the other element or layer, or intervening elements or layers may be present. In contrast, when an element is referred to as being "directly on" or "directly connected to" another element or layer, there are no intervening elements or layers present.

**[0028]** First, a liquid crystal display according to an exemplary embodiment of the present invention will be described with reference to FIG. 1, FIG. 2, and FIG. 3.

**[0029]** FIG. 1 is an equivalent circuit diagram of one pixel of the liquid crystal display according to an exemplary embodiment of the present invention, FIG. 2 is a layout view of a pixel electrode in a liquid crystal display according to an exemplary embodiment of the present invention, FIG. 3 is a cross-sectional view of the liquid crystal display including the pixel electrode shown in FIG. 2 and taken along line III-III of FIG. 2, and FIG. 4, FIG. 5, and FIG. 6 are layout views of a pixel electrode according to another exemplary embodiment of the present invention.

**[0030]** Referring to FIG. 1, a liquid crystal display according to an exemplary embodiment of the present in-

vention includes a plurality of signal lines 121, 131, 171a, and 171b, and pixels PX connected thereto. Referring to FIG. 2 and FIG. 3, the liquid crystal display according to the present exemplary embodiment includes a lower panel 100 and an upper panel 200 facing each other, and a liquid crystal layer 3 interposed therebetween. Pixel electrodes 191 are formed on the lower panel 100, a common electrode 270 is formed on the upper panel 200, and alignment layers 11 and 21 are respectively formed on the pixel electrodes 191 and the common electrode 270. A pixel electrode 191 includes first and second subpixel electrodes 191a and 191b that are separated from each other.

**[0031]** The signal lines 121, 131, 171a, and 171b are provided on the lower panel 100, and include a gate line 121 to transmit a gate signal, a pair of data lines 171a and 171b to transmit data voltages, and a storage electrode line 131, which receives a storage voltage.

**[0032]** Each pixel PX includes a pair of subpixels PXa and PXb (see FIG. 1), and the subpixels PXa and PXb respectively include a switching element Qa and Qb, a liquid crystal capacitor Clea and Cleb, and a storage capacitor Csta and Cstb.

**[0033]** Each switching element Qa and Qb is a three terminal element including a control terminal, an input terminal, and an output terminal, wherein the control terminal is connected to the gate line 121, the input terminal is connected to the corresponding data line 171a and 171b, and the output terminal is connected to the corresponding liquid crystal capacitor Clea and Cleb and storage capacitor Csta and Cstb.

**[0034]** The liquid crystal capacitors Clea and Cleb respectively include the subpixel electrodes 191a and 191b of the lower panel 100 and the common electrode 270 of the upper panel 200 as its two terminals. The liquid crystal layer 3, which is disposed between the subpixel electrodes 191a and 191b and common electrode 270, functions as a dielectric material. The subpixel electrodes 191a and 191b are connected to the switching elements Qa and Qb, respectively, and the common electrode 270 is formed on the whole surface of the upper panel 200 and receives a common voltage Vcom.

**[0035]** The storage capacitors Csta and Cstb, which serve as auxiliaries to the liquid crystal capacitors Clea and Cleb, respectively, are formed where the storage electrode line 131 and the pixel electrodes 191a and 191b overlap each other via an insulator interposed therebetween. The storage capacitors Csta and Cstb may be omitted if necessary.

**[0036]** Referring to FIG. 2, the pixel electrode 191 has a rectangular shape that extends in a longitudinal direction, and the first subpixel electrode 191a is enclosed by the second subpixel electrode 191b.

**[0037]** The first subpixel electrode 191a has a shape of two identical rectangles, which extend in the longitudinal direction and are longitudinally offset from and connected to each other. Thus, if the two rectangles are symmetrically aligned and combined, an approximate square

may be formed. However, the ratio of the longitudinal length to a transverse length of the first subpixel electrode 191a may be changed.

**[0038]** The second subpixel electrode 191b encloses the first sub-pixel electrode 191a with a gap 91 having a uniform width therebetween, except that the width is not uniform in an area that notches 97 are disposed. The second subpixel electrode 191b includes an upper electrode part 191b1 disposed above the first subpixel electrode 191a, a lower electrode part 191b2 disposed therebelow, and connection pieces 191b12 connecting the two electrode parts 191b1 and 191 b2 on the right and left sides of the first subpixel electrode 191 a.

**[0039]** The second subpixel electrode 191b is larger than the first subpixel electrode 191 a, and a desired ratio of areas thereof may be embodied by controlling the ratio of the longitudinal length of the first subpixel electrode 191a to that of the second subpixel electrode 191b. For example, when the area of the second subpixel electrode 191b may be about two times the area of the first subpixel electrode 191a, the first subpixel electrode 191a, the upper electrode part 191b1, and the lower electrode part 191b2 all may have the same area.

**[0040]** A plurality of notches 97 are formed near the center of the left edge and the right edge of the first subpixel electrode 191a, and near the center of the upper edge and the lower edge of the second subpixel electrode 191b. The notches 97 shown in FIG. 2 have a shape of a triangle, however they may have a shape of a quadrangle, a trapezoid, or a semicircle, as shown in FIG. 4, FIG. 5, and FIG. 6. Further, it is possible for the notches 97 to have various shapes such as a curved line, a slit and a protrusion shape protruding outside. The number and the size of the notches 97 may be changed.

**[0041]** Notches 98 are formed at the corners of the pixel electrode 191 and may have a quadrangular shape.

**[0042]** The liquid crystal layer 3 has negative dielectric anisotropy and is aligned in the longitudinal direction with respect to the panels 100 and 200. Polarizers (not shown) are provided on outer surfaces of the substrates 110 and 210, and polarization axes of the two polarizers may cross each other and form an angle of about 45 degrees with respect to the longitudinal and transverse directions.

**[0043]** In the absence of an electric field applied to the liquid crystal layer 3, that is, when a difference between voltages of the pixel electrode 191 and the common electrode 270 equals zero, liquid crystal molecules 31 of the liquid crystal layer 3 may be perpendicular to or slightly inclined from a perpendicular state with respect to the surface of the alignment layers 11 and 21.

**[0044]** If a potential difference is generated between the pixel electrode 191 and the common electrode 270, an electric field that is substantially perpendicular to the surface of the display panels 100 and 200 is generated in the liquid crystal layer 3. Then, the liquid crystal molecules 31 of the liquid crystal layer 3 are aligned such that the long axes thereof are inclined vertically to the direction of the electric field in response to the electric

field, and the polarization of light that is incident to the liquid crystal layer 3 is changed according to the inclination degree of the liquid crystal molecules 31. The change of the polarization appears as a change of light transmittance by the polarizers, and thereby images are displayed by the liquid crystal display.

**[0045]** The inclination directions of the liquid crystal molecules 31 are dependent on the characteristics of the alignment layers 11 and 21. For example, the alignment layers 11 and 21 may be irradiated by ultraviolet rays having different polarization directions or may be obliquely irradiated so as to determine the inclination directions of the liquid crystal molecules 31.

**[0046]** A portion of the liquid crystal layer 3 disposed over the pixel electrode 191 is divided into four regions: left-upper D1, right-upper D2, right-lower D3, and left-lower D4, according to the inclination directions of the liquid crystal molecules 31. The boundaries of these regions D1 through D4 are the transverse central line BT and the longitudinal central line BL bisecting the pixel electrode 191, and the areas of the regions D1 through D4 are almost the same. The inclination directions of the liquid crystal molecules 31 disposed in neighboring regions D1 through D4 in the transverse and longitudinal directions form an angle of about 90 degrees with each other, and the inclination directions of the liquid crystal molecules 31 disposed in neighboring regions in the diagonal direction are opposite to each other.

**[0047]** The arrows in FIG. 2 indicate the inclination directions of the liquid crystal molecules 31. The liquid crystal molecules 31 are inclined in the right-upper direction in the left-upper region D1, in the right-lower direction in the right-upper region D2, in the left-lower direction in the right-lower region D3, in the left-upper direction in the left-lower region D4.

**[0048]** However, the inclination directions in the four regions D1, D2, D3, and D4 are not limited thereto and may be variously changed. Further, there may be greater than or fewer than four inclination directions of the liquid crystal molecules 31, if necessary.

**[0049]** Here, the notch 97 is disposed near the central lines BT and BL, and it may be disposed within 10 $\mu$ m from the central lines BT and BL. If the notch 97 is disposed outside of this range, sizes of the regions D1, D2, D3, and D4 differ from each other such that an imbalance of the viewing angle may be generated. The notch 97 accelerates the determination of the inclination direction of the liquid crystal molecules 31. In other words, if the notch 97 does not exist, boundaries of the four regions D1, D2, D3, and D4 in which the liquid crystal molecules are inclined may not be clear, or the boundary determination may become retarded when an electric field is applied. However, if the notch 97 exists, it functions as a singular point such that the inclination direction of the liquid crystal molecules 31 may be quickly changed with the boundaries of the notch 97. The notch 98 disposed at the corners of the pixel electrode 191 may help to quickly determine the inclination directions of the liquid crystal

molecules 31 such that the arrangements of liquid crystal molecules 31 may be quickly stabilized. The size of the notches 97 and 98 may be in the range of about 3  $\mu\text{m}$  by 3  $\mu\text{m}$  to 15  $\mu\text{m}$  by 1  $\mu\text{m}$ . However, when the size is greater than or less than these values, the notches 97 and 98 may not function as a singular point.

**[0050]** The viewing angle of the liquid crystal display is widened by varying the inclined directions of the liquid crystal molecules.

**[0051]** On the other hand, if different voltages are applied to the first subpixel electrode 191a and the second subpixel electrode 191b, the magnitude of the relative voltage of the first subpixel electrode 191a is larger than the magnitude of the relative voltage of the second subpixel electrode 191b with respect to the common voltage Vcom. The inclination angles of the liquid crystal molecules 31 may be changed according to the intensity of the electric field, and thus, the inclination angles of the liquid crystal molecules 31 that are disposed on the first subpixel electrode 191a and the second subpixel electrode 191b may be different since the voltages of the two subpixel electrodes 191a and 191b are different from each other.

**[0052]** Therefore, each of the regions D1, D2, D3, and D4 of the liquid crystal layer 3 are further divided into first subregions D1a, D2a, D3a, and D4a disposed on the first subpixel electrode 191a, and second subregions D1b, D2b, D3b, and D4b disposed on the second subpixel electrode 191b. As shown in FIG. 3, since the relative voltage of the first subpixel electrode 191a is higher than that of the second subpixel electrode 191b, the liquid crystal molecules 31 in the first subregions D1a, D2a, D3a, and D4a are more inclined than the liquid crystal molecules 31 of the second subregions D1b, D2b, D3b, and D4b.

**[0053]** Therefore, the luminances of the two subpixels PXa and PXb differ from each other, and the sum of the luminances thereof is equal to the luminance of the pixel PX. Accordingly, the voltages applied to the two subpixel electrodes 191a and 191b are determined to be a value corresponding to the desired luminance of the pixel PX. That is, the voltages applied to the two subpixel electrodes 191a and 191b are provided from an image signal for one pixel PX.

**[0054]** Further, if the voltages of the first subpixel electrode 191a and the second subpixel electrode 191b are appropriately controlled, the images shown at the side may be approximate to the image shown at the front, thereby improving the side visibility and increasing the transmittance of the liquid crystal display.

**[0055]** Next, a liquid crystal display according to another exemplary embodiment of the present invention will be described with reference to FIG. 7, FIG. 8, FIG. 9, FIG. 10, and FIG. 11.

**[0056]** FIG. 7 is a layout view of a liquid crystal display according to an exemplary embodiment of the present invention, FIG. 8 is a layout view of a pixel electrode of the liquid crystal display shown in FIG. 7, FIG. 9 is a

layout view of a storage electrode line of the liquid crystal display shown in FIG. 7, FIG. 10 is a layout view showing an alignment direction of liquid crystal molecules over the pixel electrode in the liquid crystal display of FIG. 7, and FIG. 11 is a cross-sectional view of the liquid crystal display shown in FIG. 7 taken along the line XI-XI.

**[0057]** Referring to FIG. 7, FIG. 8, FIG. 9, FIG. 10, and FIG. 11, a liquid crystal display according to the present exemplary embodiment includes a lower panel (thin film transistor array panel) 100, an upper panel (common electrode panel) 200, and a liquid crystal layer 3.

**[0058]** First, the thin film transistor array panel 100 will be described.

**[0059]** A gate conductor including a plurality of gate lines 121 and a plurality of storage electrode lines 131 are formed on an insulation substrate 110.

**[0060]** The gate lines 121 extend mainly in a transverse direction, and each gate line 121 includes a plurality of first and second gate electrodes 124a and 124b that protrude upward, and a wide end portion 129.

**[0061]** The storage electrode lines 131 extend mainly in the transverse direction and are disposed between two gate lines 121.

**[0062]** Referring to FIG. 9, each storage electrode line 131 includes a storage electrode 137 with a shape of an open-quadrangle belt, and a connection 136 connected to the storage electrode 137. The storage electrode 137 includes transverse electrodes 133, 134a, and 134b, and longitudinal electrodes 135, and the transverse electrodes 133, 134a, and 134b have a greater width than that of the longitudinal electrode 135. The transverse electrodes 133, 134a, and 134b include an upper electrode 133, a right lower electrode 134a, and a left lower electrode 134b. One end of the upper electrode 133 and one end of the right lower electrode 134a are connected by one longitudinal electrode 135, and the other end of the upper electrode 133 and one end of the left lower electrode 134b are connected by the other longitudinal electrode 135. The other end of the right lower electrode 134a and the other end of the left lower electrode 134b are separated from each other by a predetermined distance, thereby forming the open-quadrangle. The connection 136 is connected substantially to the center of the longitudinal electrode 135.

**[0063]** A gate insulating layer 140 is formed on the gate conductors 121 and 131.

**[0064]** A plurality of first and second semiconductor stripes 151a and 151b (in the drawing, only "151a" appears, and "151b" is not shown, but "151b" is used for convenience) are formed on the gate insulating layer 140. The first and second semiconductor stripes 151a and 151b extend in the longitudinal direction, and include first and second protrusions 154a and 154b extending toward the first and second gate electrodes 124a and 124b, respectively.

**[0065]** A plurality of first ohmic contact stripes 161a and first ohmic contact islands 165a are formed on the first semiconductor stripes 151a. The first ohmic contact

stripes 161a include a plurality of first protrusions 163a, and the first protrusion 163a and the first ohmic contact island 165a are disposed as a pair on each first protrusion 154a.

**[0066]** A plurality of second ohmic contact stripes (not shown) and second ohmic contact islands (not shown) are formed on the second semiconductor stripes 151b (not shown). The second ohmic contact stripes also include a plurality of protrusions (not shown), and the protrusion and the second ohmic contact island are disposed as a pair on each second protrusion 154b.

**[0067]** A plurality of first data lines 171a are formed on the first ohmic contact stripes 161a, and a plurality of first drain electrodes 175a are formed on the first ohmic contact islands 165a. A plurality of second data lines 171b are formed on the second ohmic contact stripes, and a plurality of second drain electrodes 175b are formed on the second ohmic contact islands.

**[0068]** The first and second data lines 171a and 171b extend substantially in the longitudinal direction, thereby crossing the gate lines 121 and the connections 136 of the storage electrode lines 131. The first and second data lines 171a and 171b include a plurality of first and second source electrodes 173a and 173b extending toward the first and second gate electrodes 124a and 124b, and end portions 179a and 179b, respectively.

**[0069]** The first and second drain electrodes 175a and 175b start from one end enclosed by the curved portions of the first and second source electrodes 173a and 173b on the first and second gate electrodes 124a and 124b, respectively, and extend upward.

**[0070]** The ohmic contacts 161a and 165a only exist between the semiconductor stripes 151a thereunder, and the first data lines 171a and the first drain electrodes 175a thereabove, and reduce contact resistance between them. The second ohmic contacts only exist between the underlying second semiconductor stripes 151b and the overlying second data lines 171b and second drain electrodes 175b, thereby reducing contact resistance therebetween. The first semiconductor stripes 151a have substantially the same planar shape as the first data lines 171a, the first drain electrodes 175a, and the first ohmic contacts 161a and 165a. The second semiconductor stripes 151b have substantially the same planar shape as the second data lines 171b, the second drain electrodes 175b, and the second ohmic contacts. However, the semiconductor stripes 151a and 151b have portions that are exposed without being covered by the data lines 171a and 171b and the drain electrodes 175a and 175b, such as the portions between the source electrodes 173a and 173b and the drain electrodes 175a and 175b.

**[0071]** A passivation layer 180 is formed on the first and second data lines 171a and 171b, the first and second drain electrodes 175a and 175b, and the exposed semiconductor stripes 151a and 154b. The passivation layer 180 includes a lower layer 180p made of an inorganic insulator such as silicon nitride or silicon oxide, and

an upper layer 180q. At least one of the lower layer 180p and the upper layer 180q may be omitted.

**[0072]** The passivation layer 180 has a plurality of contact holes 182a and 182b exposing the end portions 179a and 179b of the data lines 171a and 171b, respectively, and a plurality of contact holes 185a and 185b exposing the wide end portions of the drain electrodes 175a and 175b, respectively, and the passivation layer 180 and the gate insulating layer 140 have a plurality of contact holes 181 exposing the end portions 129 of the gate lines 121.

**[0073]** A plurality of color filters 230 are formed between the lower layer 180p and the upper layer 180q.

**[0074]** The color filters 230 have a plurality of through holes 235a and 235b through which the contact holes 185a and 185b pass, respectively, and the through holes 235a and 235b are larger than the contact holes 185a and 185b. The color filters 230 also include a plurality of openings 233a, 233b, 234a, and 234b disposed on the storage electrodes 137. The openings 233a and 233b are disposed on the upper electrode 133, and the openings 234a and 234b are respectively disposed on the right lower electrode 134a and the left lower electrode 134b.

**[0075]** A plurality of pixel electrodes 191 and a plurality of contact assistants 81, 82a, and 82b are formed on the upper layer 180q of the passivation layer 180.

**[0076]** As shown in FIG. 8, the pixel electrodes 191 according to the present exemplary embodiment have substantially the same shape as the pixel electrode 191 shown in FIG. 2. The pixel electrode 191 includes a first subpixel electrode 191a and a second subpixel electrode 191b that are opposite to each other via a gap 91, and notches 97 and 98 are formed on the edge and corners of the first subpixel electrode 191a and the second subpixel electrode 191b, respectively.

**[0077]** The gap 91 between the first subpixel electrode 191a and the second subpixel electrode 191b overlaps the storage electrode 137. The storage electrode 137 blocks light leakage between the first subpixel electrode 191a and the second subpixel electrode 191b, and simultaneously blocks texture caused by the light alignment. The texture caused by the light alignment is generated in regions toward which the liquid crystal molecules 31 incline with respect to the gap. For example, in FIG. 10, the positions where textures are generated are the left-upper portion and the right-lower portion of the first subpixel electrode 191a, and the right-upper portion and the left-lower portion of the second subpixel electrode 191b. Accordingly, if the left-half portion of the first subpixel electrode 191a is moved up and the right-half portion thereof is moved down, the texture generation region of the first subpixel electrode 191a and the texture generation region of the second subpixel electrode 191b are disposed on the same straight line. Accordingly, the storage electrode 137 having a simple shape and a small area may effectively cover the texture generation regions.

**[0078]** The pixel electrodes 191 also overlap the stor-

age electrodes 137 to form a storage capacitor. That is, the first subpixel electrode 191a overlaps the upper electrode 133 and the right lower electrode 134a thereby forming the storage capacitor Csta, and the second subpixel electrode 191b overlaps the upper electrode 133 and the left lower electrode 134b thereby forming the storage capacitor Cstb. Here, the pixel electrode 191 and the storage electrode 137 overlap only via the passivation layer 180 in the openings 233a and 234a of the color filters 230, so that the capacitance of the storage capacitor may be increased

**[0079]** The first and second gate electrodes 124a and 124b, the first and second protrusions 154a and 154b of the first and second semiconductor stripes 151a and 151b, respectively, the first and second source electrodes 173a and 173b, and the first and second drain electrodes 175a and 175b form the first and second thin film transistors Qa and Qb, respectively. The first and second drain electrodes 175a and 175b are connected to the first and second subpixel electrodes 191a and 191b through the contact holes 185a and 185b, respectively.

**[0080]** The contact assistants 81, 82a, and 82b are connected to the end portions 129, 179a, and 179b of the gate lines 121 and the data lines 171a and 171b, respectively. The contact assistants 81, 82a, and 82b complement adhesion of the end portions 129 of the gate lines 121 and the end portions 179a and 179b of the data lines 171a and 171 b with an external device such as a driver IC, and protect them.

**[0081]** Next, the common electrode panel 200 will be described.

**[0082]** A plurality of light blocking members 220 are formed on an insulating substrate 210, an overcoat 250 is formed on the light blocking members 220, and a common electrode 270 is formed on the overcoat 250. However, in FIG. 7, the light blocking member 220 is not shown for convenience of distinction between elements.

**[0083]** Alignment layers 11 and 21 are formed on the facing surfaces of the thin film transistor array panel 100 and the common electrode panel 200.

**[0084]** According to embodiments of the present invention, the pixel electrode may include notches such that liquid crystal molecules of each alignment region may be quickly stabilized.

**[0085]** Also, textures generated at a region where the alignment direction determined by the light alignment and the alignment direction of the liquid crystal molecules by the fringe field at a gap between two subpixels may be effectively covered such that transmittance may be improved and the textures may be prevented from appearing as a stain. Thereby, display characteristics may be improved. It will be apparent to those skilled in the art that various modifications and variation can be made in the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

## Claims

### 1. A liquid crystal panel, comprising:

- 5 a substrate; and  
a pixel electrode disposed on the substrate, the pixel electrode comprising a first subpixel electrode and a second subpixel electrode separated from each other,  
10 wherein the second subpixel electrode comprises  
a first electrode part disposed above the first subpixel electrode, and  
a second electrode part disposed below the first subpixel electrode and connected to the first electrode part, and  
15 at least one first notch is arranged on at least one edge of the first subpixel electrode or the second subpixel electrode.
- 20 2. The liquid crystal panel of claim 1, wherein at least one first notch is disposed within 10 $\mu$ m of a transverse central line or a longitudinal central line substantially bisecting the pixel electrode.
- 25 3. The liquid crystal panel of claim 2, wherein the at least one first notch is disposed on the transverse central line or the longitudinal central line.
- 30 4. The liquid crystal panel of claim 1, wherein the at least one first notch has a size in a range of 3 $\mu$ m by 3 $\mu$ m to 15 $\mu$ m by 15 $\mu$ m.
- 35 5. The liquid crystal panel of claim 1, wherein the second subpixel electrode further comprises a first connection piece connecting the first electrode part and the second electrode part on a right side of the first subpixel electrode and a second connection piece connecting the first electrode part and the second electrode part on a left side of the first subpixel electrode.
- 40 6. The liquid crystal panel of claim 5, wherein the first subpixel electrode is enclosed by the second subpixel electrode with a gap between the first subpixel electrode and the second subpixel electrode.
- 45 7. The liquid crystal panel of claim 6, wherein a boundary between the first subpixel electrode and the first electrode part and a boundary between the first subpixel electrode and the second electrode part each have a step shape.
- 50 8. The liquid crystal panel of claim 7, wherein The step shape of the boundary between the first subpixel electrode and the first electrode part and the step shape of the boundary between the first subpixel electrode and the second electrode part is dis-
- 55

posed on a longitudinal central line substantially bisecting the pixel electrode.

9. The liquid crystal panel of claim 7, wherein the at least one first notch comprises:

a second notch disposed within 10 $\mu$ m of a transverse central line substantially bisecting the pixel electrode, and arranged in a longitudinal edge of the first subpixel electrode, and  
a third notch disposed within 10 $\mu$ m of a longitudinal central line substantially bisecting the pixel electrode, and arranged in a transverse edge of the second subpixel electrode.

10. The liquid crystal panel of claim 6, further comprising a storage electrode overlapping the gap.

11. A liquid crystal display, comprising:

a first substrate;  
a pixel electrode arranged on the first substrate and comprising a first subpixel electrode and a second subpixel electrode separated from each other;  
a second substrate facing the first substrate;  
a common electrode arranged on the second substrate; and  
a liquid crystal layer interposed between the pixel electrode and the common electrode,

wherein the second subpixel electrode comprises:

a first electrode part disposed above the first subpixel electrode,  
a second electrode part disposed below the first subpixel electrode and connected to the first electrode part, and  
a first connection piece connecting the first electrode part and the second electrode part on the right side of the first subpixel electrode, and a second connection piece connecting the first electrode part and the second electrode part on the left side of the first subpixel electrode, and  
wherein first notches are arranged in an upper edge and a lower edge of the second subpixel electrode, and in a left edge and a right edge of the first subpixel electrode.

12. The liquid crystal display of claim 11, wherein the liquid crystal layer comprises four regions having different alignment directions from each other, the four regions being divided by a boundary near lines connecting the first notches opposing each other.

13. The liquid crystal display of claim 12, wherein the first notches are within 10 $\mu$ m from the boundary of the regions of the liquid crystal layer.

14. The liquid crystal display of claim 12, wherein a second notch is arranged at a corner of the pixel electrode.

15. The liquid crystal display of claim 12, wherein a boundary between the first subpixel electrode and the first electrode part and a boundary between the first subpixel electrode and the second electrode part each have a step shape.

FIG. 1

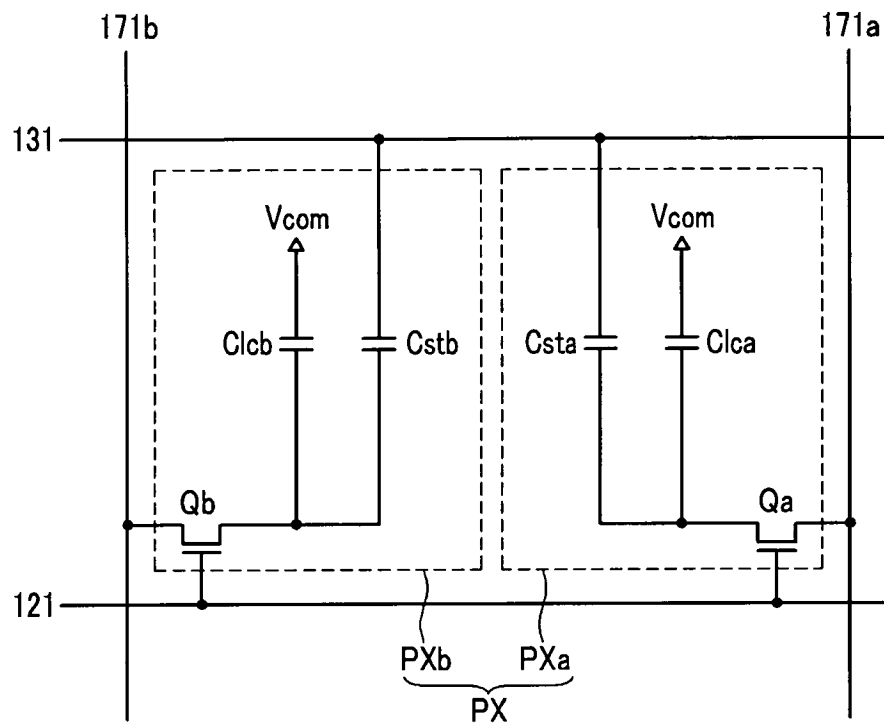


FIG. 2

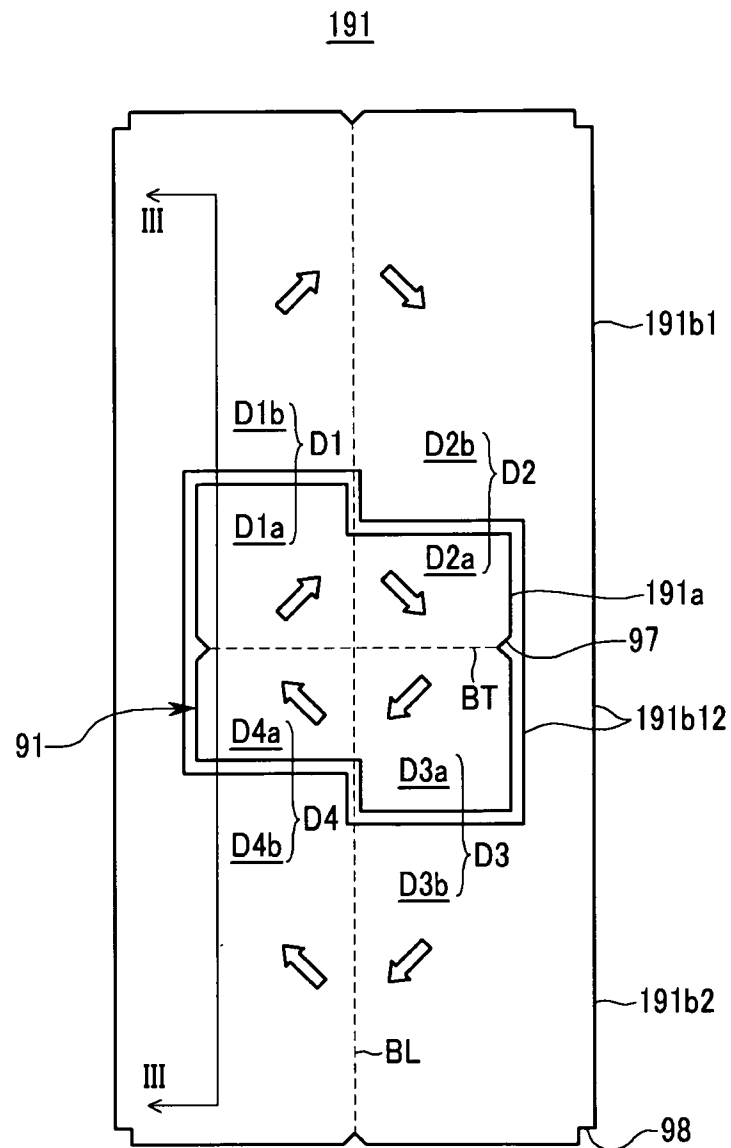


FIG. 3

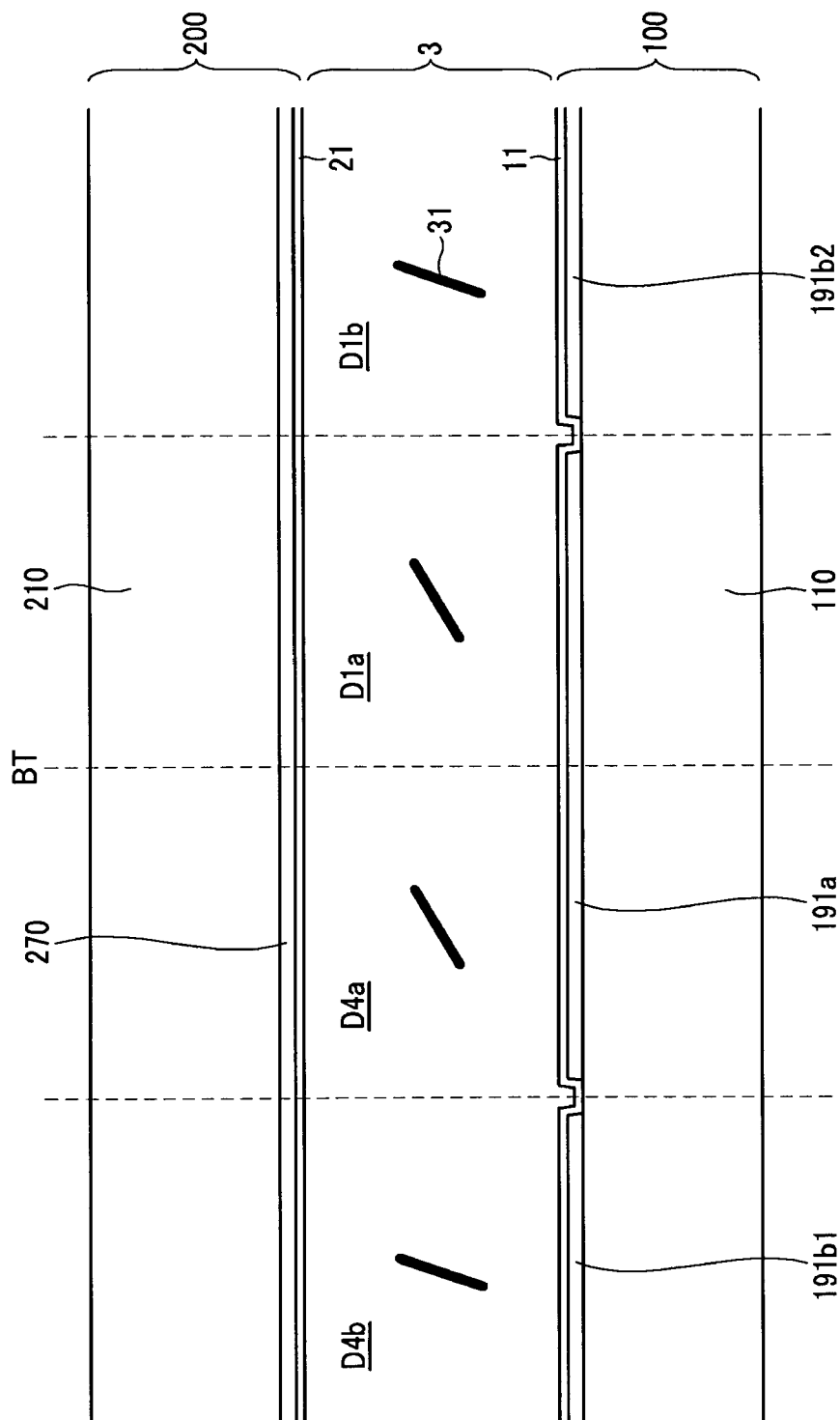


FIG. 4

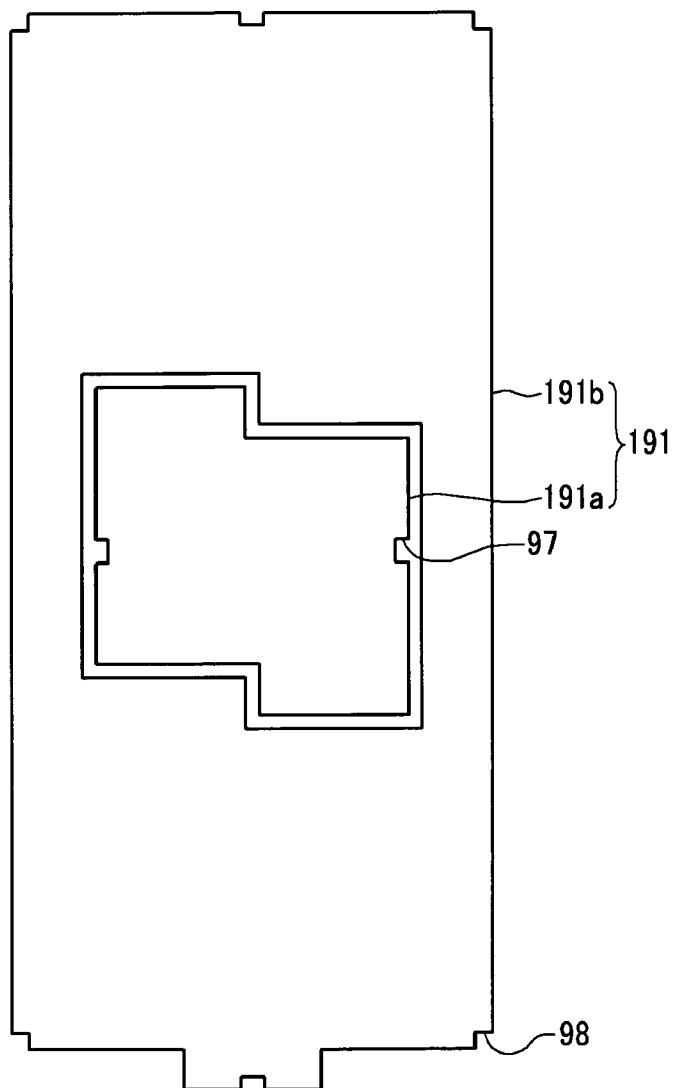


FIG. 5

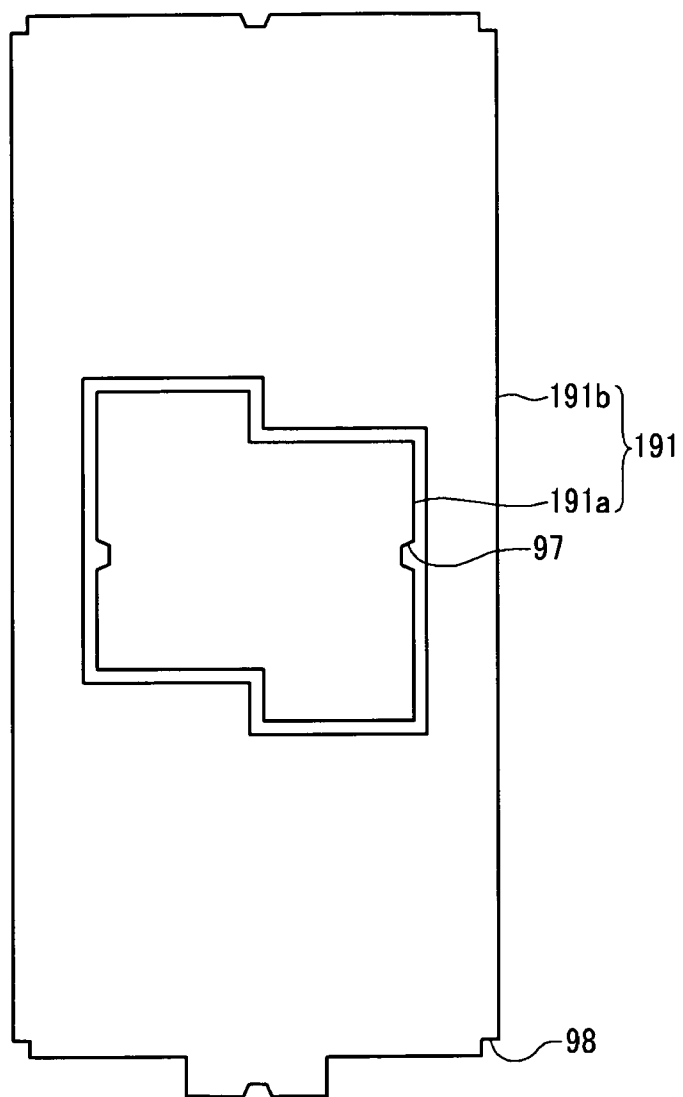


FIG. 6

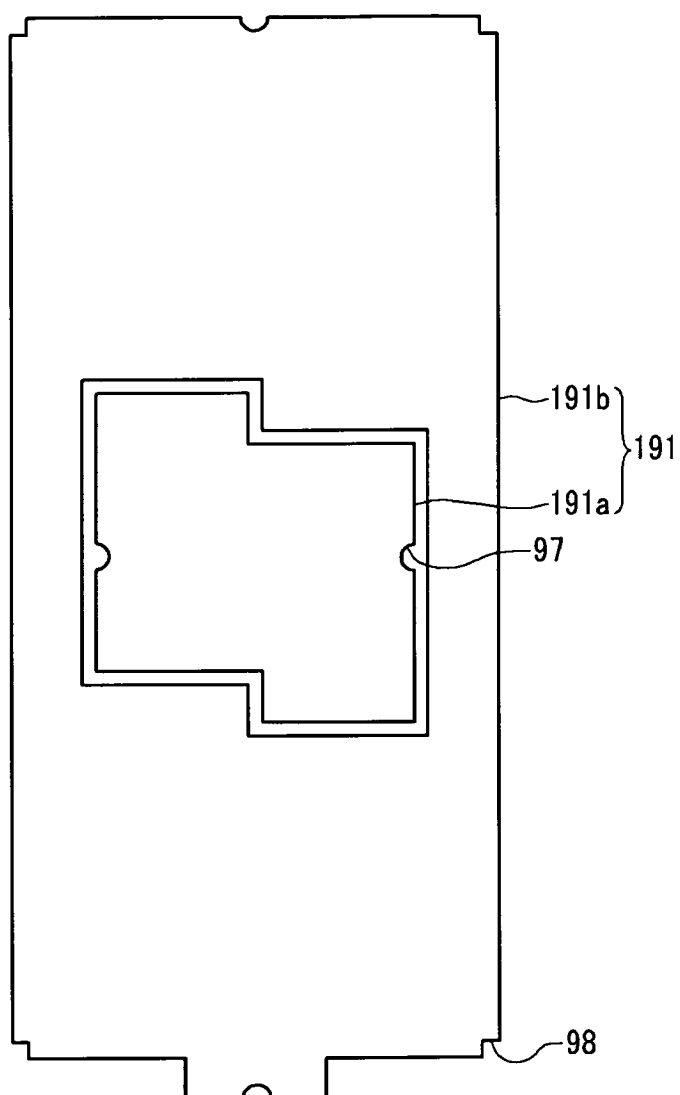


FIG. 7

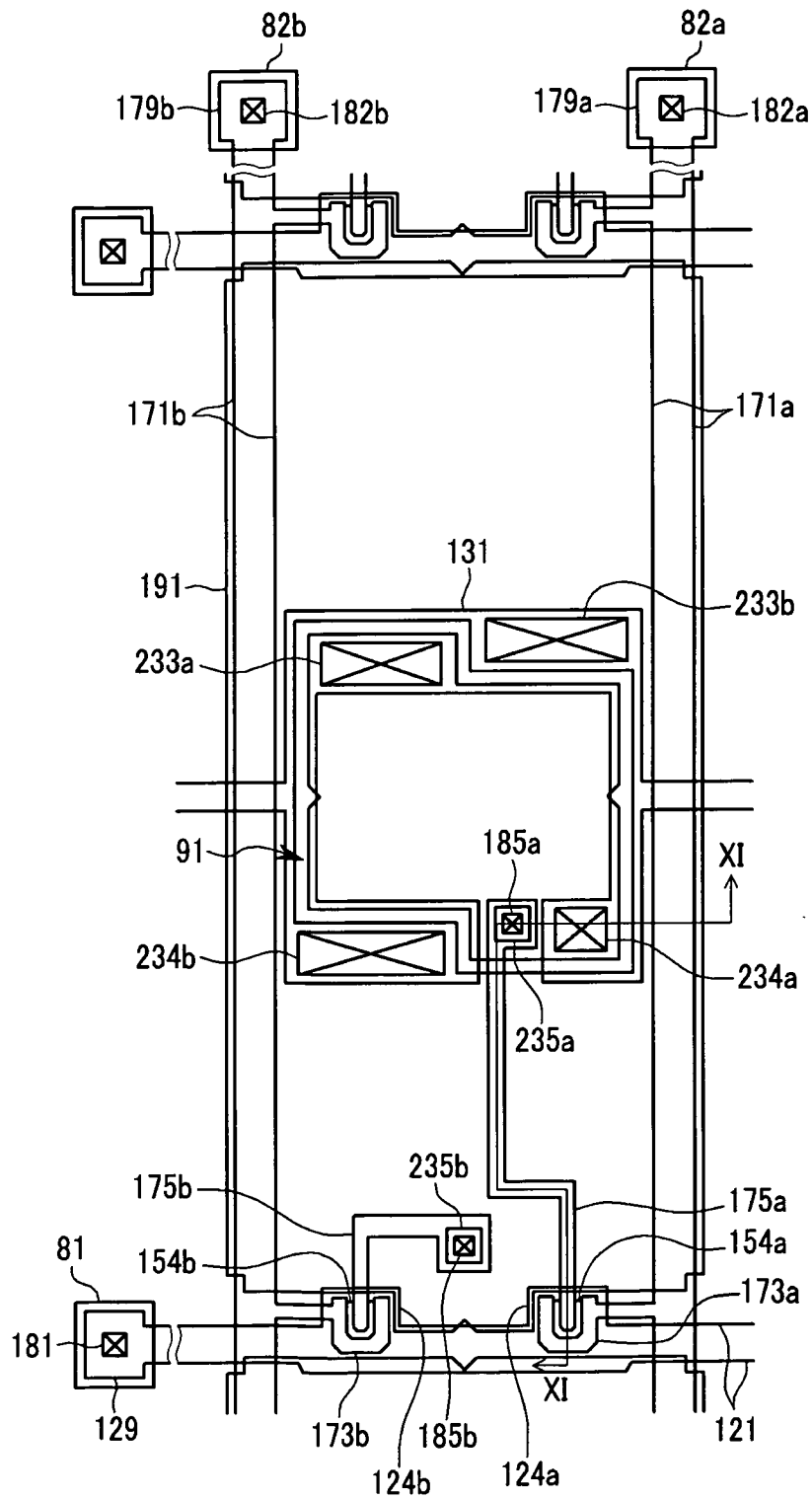


FIG. 8

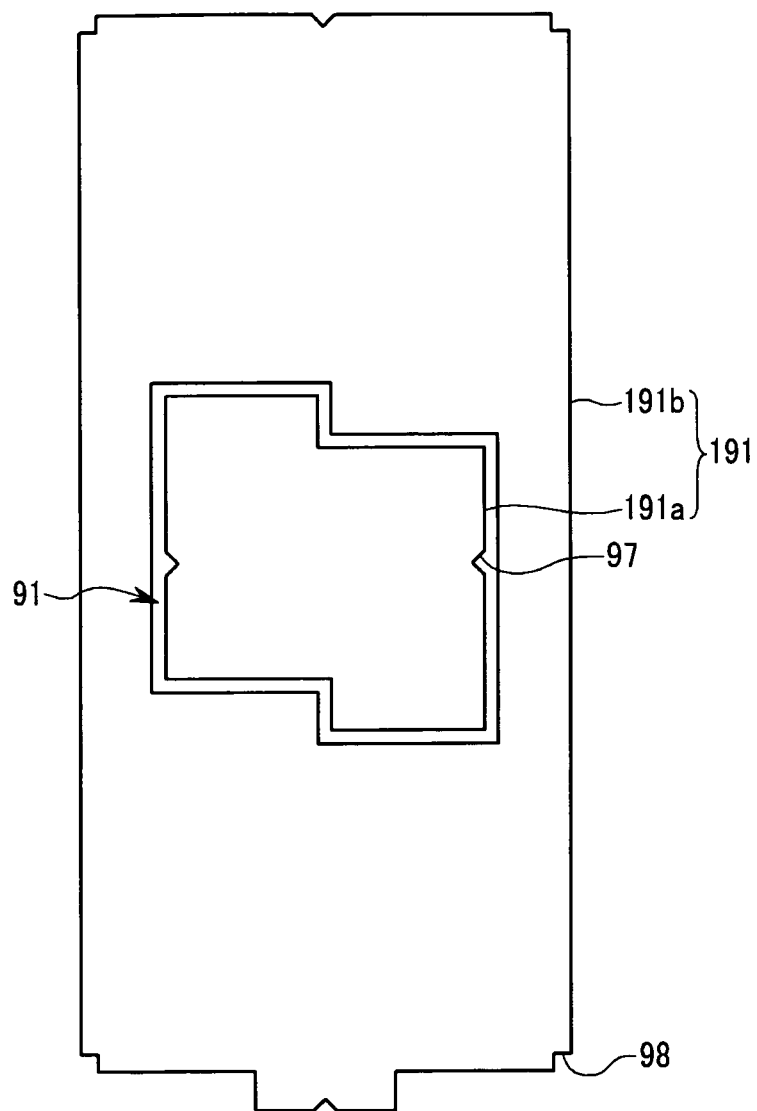


FIG. 9

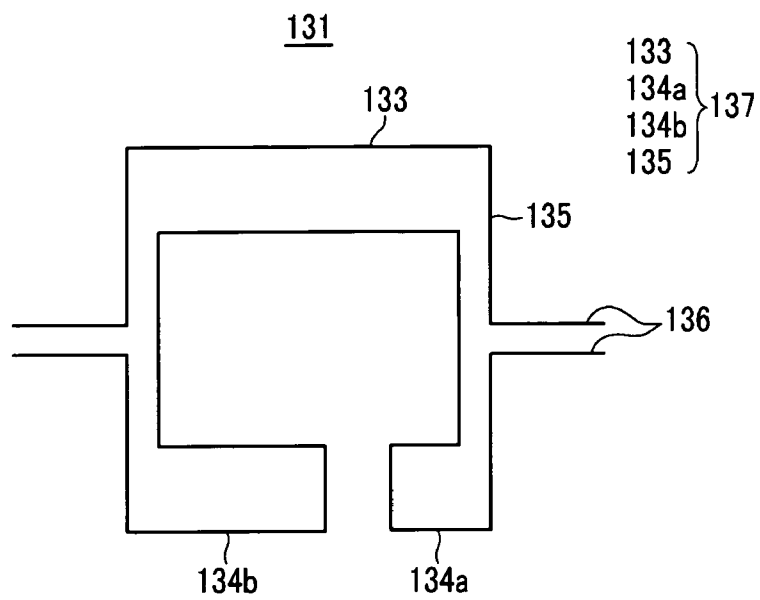


FIG. 10

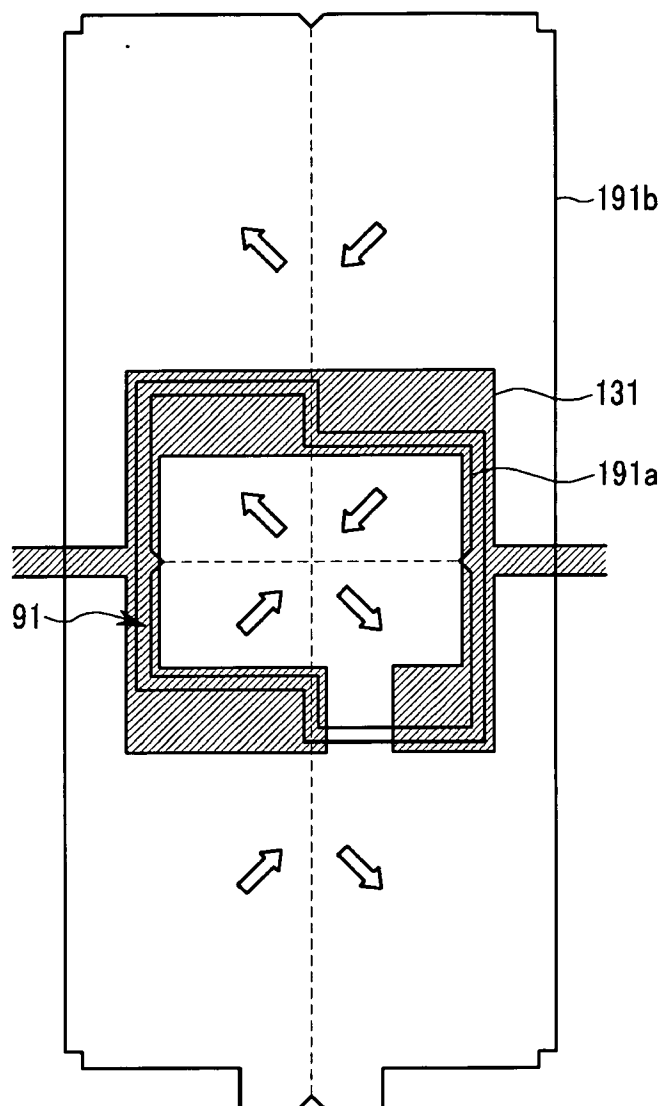
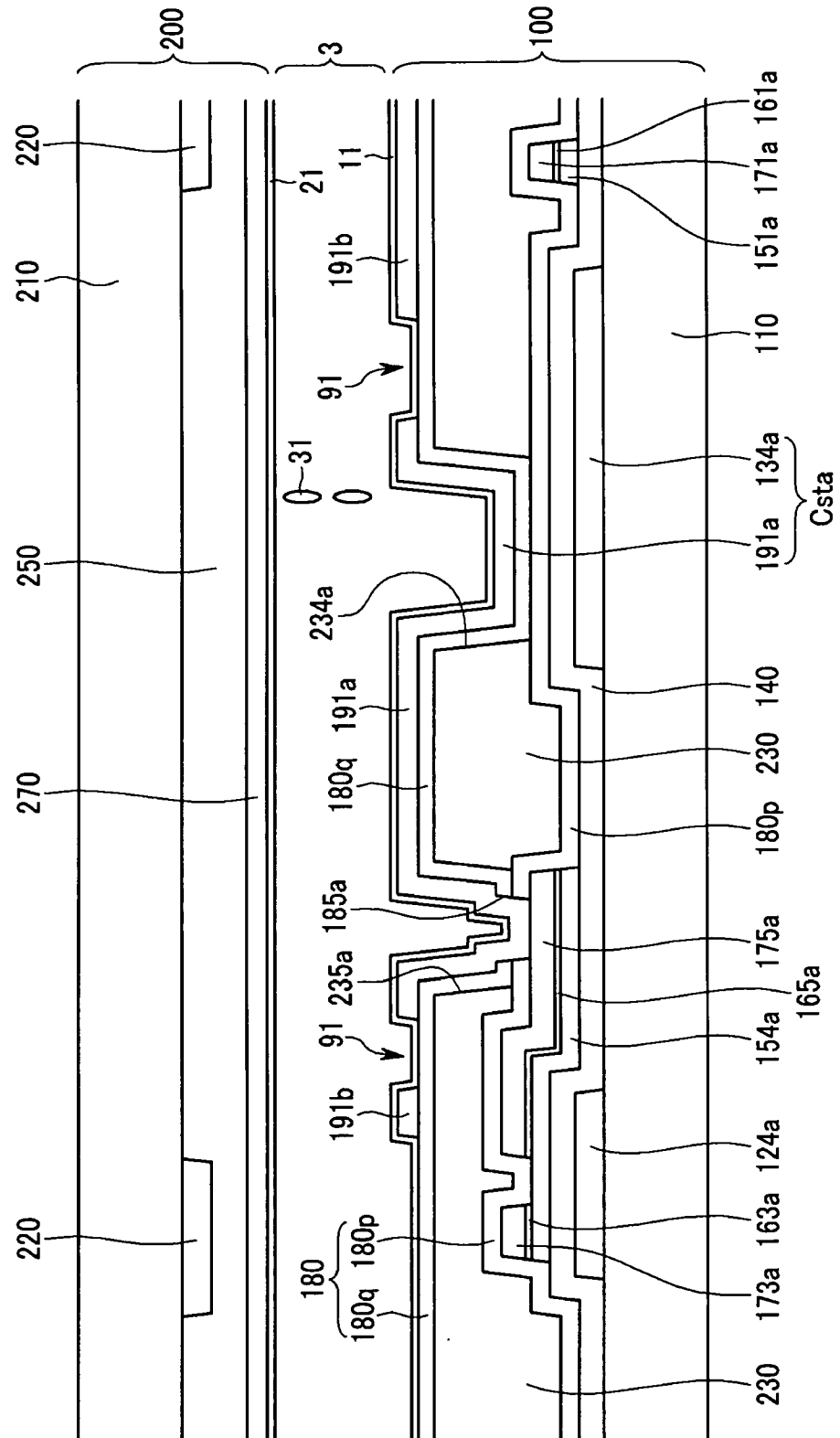


FIG. 11



|                |                                                                                                      |         |            |
|----------------|------------------------------------------------------------------------------------------------------|---------|------------|
| 专利名称(译)        | 液晶显示器及其面板                                                                                            |         |            |
| 公开(公告)号        | <a href="#">EP2148239A2</a>                                                                          | 公开(公告)日 | 2010-01-27 |
| 申请号            | EP2009002617                                                                                         | 申请日     | 2009-02-25 |
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| IPC分类号         | G02F1/1337 G02F1/1343 G02F1/13363                                                                    |         |            |
| CPC分类号         | G02F1/133634 G02F2001/133637                                                                         |         |            |
| 代理机构(译)        | DR.威猛和合作伙伴                                                                                           |         |            |
| 优先权            | 1020080072385 2008-07-24 KR                                                                          |         |            |
| 其他公开文献         | EP2148239B1<br>EP2148239A3                                                                           |         |            |
| 外部链接           | <a href="#">Espacenet</a>                                                                            |         |            |

#### 摘要(译)

根据本发明示例性实施例的液晶面板包括基板和布置在基板上的像素电极。像素电极 ( 191 ) 包括彼此分离的第一子像素电极 ( 191a ) 和第二子像素电极 ( 191b ) , 第二子像素电极包括设置在第一子像素电极上方的第一电极部分和设置在下方的第二电极部分第一子像素电极并连接到第一电极部分。至少一个第一凹口 ( 97 ) 布置在第一子像素电极或第二子像素电极的至少一个边缘上。

FIG. 2

