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(54) **ARRAY SUBSTRATE, METHOD FOR CORRECTING THE SAME, AND LIQUID CRYSTAL DISPLAY**

MATRIX SUBSTRAT, VERFAHREN ZUM REPARIEREN DESSELBEN UND FLÜSSIGKRISTALLANZEIGE

SUBSTRAT DE RÉSEAU, PROCÉDÉ POUR CORRIGER CELUI-CI ET AFFICHEUR À CRISTAUX LIQUIDES

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(56) References cited:
JP-A- 02 108 028
JP-A- 03 242 625
JP-A- 05 002 184
JP-A- 2007 010 824
US-A- 5 943 106
US-B1- 6 822 701

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Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to an array substrate having an auxiliary capacitance line and a correction method of the array substrate.

2. Description of the Related Art

[0002] In recent years, liquid crystal display devices are widely used as display units of household electrical appliances such as computers and televisions. A liquid crystal display device generally comprises an array substrate and a color filter substrate, which are facing to each other with a narrow gap therebetween and bonded together at their peripheral portions, and a liquid crystal filled in the gap. On the array substrate, scanning lines and signal lines are arranged perpendicular to each other in a reticular pattern. In each of pixel regions partitioned by the scanning lines and the signal lines, a pixel electrode is arranged. The pixel electrode and the signal line are connected via a switching element which is on/off controlled by the scanning line. In addition, on the array substrate, an auxiliary capacitance line is arranged overlapping the pixel electrode so that the electric charge which is supplied from the scanning line and stored in the pixel electrode is maintained longer.

[0003] Although the electric charge stored in the pixel electrode gradually leaks via the liquid crystal layer and the switching element and therefore decreases by the next application of signal voltage through the scanning line, the decrease is suppressed by the auxiliary capacitance line arranged overlapping the pixel electrode. In general, when the overlapping area of the pixel electrode and the auxiliary capacitance line is larger, the ability to maintain the electric charge stored in the pixel electrode is greater. However, a larger overlapping area results in a lower aperture ratio of the pixel electrode.

[0004] This type of liquid crystal display device is disclosed in Japanese Patent Application Unexamined Publication No. 2004-53752. As shown in Fig. 6, an auxiliary capacitance line 51 of an array substrate 50 of this type of liquid crystal display device has a line trunk 51a arranged parallel to a scanning line 52 and line branches 51b extending from the line trunk 51a. The line branches 51b are used to increase the ability to maintain the electric charge stored in a pixel electrode 53. The line branches 51b are arranged along signal lines 54 which are shielded from light by black matrixes of a color filter substrate, thereby suppressing decrease in the aperture ratio.

[0005] However, providing the auxiliary capacitance line 51 with the line branches 51b results in interposing a foreign matter such as a conductive foreign matter and causing a short circuit between the pixel electrode 53 and the auxiliary capacitance line 51. Accordingly, the possibility of point defect is increased. When a point defect occurs, the short circuit can be corrected by applying a laser beam to the short-circuited line branch 51b in order to cut it at some midpoint. However, if the insulating layer between the pixel electrode 53 and the auxiliary capacitance line 51 is thin, the laser beam is also applied to the pixel electrode 53.

[0006] Although there is another correction method in which the short-circuited area is isolated from the other area of the pixel electrode 53 by applying a laser beam to the pixel electrode 53, this method is difficult to perform because it is difficult to completely isolate and insulate the short-circuited area from the other area of the pixel electrode 53 and thus some area tends to remain connected.

[0007] Hence, the present invention aims to provide an array substrate, a correction method of the array substrate, and a liquid crystal display device which can easily correct the above defect.

SUMMARY OF THE INVENTION

[0008] In order to overcome the problems described above, an array substrate according to the present invention is as defined in claim 1.

[0009] The line branch of the auxiliary capacitance line may intersect with the aperture having the slit shape at an angle of between 80 degrees and 100 degrees. A plurality of the apertures of the pixel electrode may be arranged along the length direction of the line branch of the auxiliary capacitance line and the line branch of the auxiliary capacitance line may be arranged along the signal line.

[0010] A correction method of such an array substrate may comprise cutting the line branch of the auxiliary capacitance line using the aperture of the pixel electrode when there is a short circuit between the pixel electrode and the line branch of the auxiliary capacitance line.

[0011] A liquid crystal display device may comprise the above array substrate, a substrate which is arranged facing to the array substrate and has a common electrode, and a crystal filled between the array substrate and the substrate.

[0012] Because the array substrate has the above configuration, in which the auxiliary capacitance line comprises the line trunk arranged substantially parallel to the scanning line and the line branch extending from the line trunk, and the pixel electrode is provided with the aperture which crosses the line branch of the auxiliary capacitance line, even when there is a short circuit between the pixel electrode and the line branch due to an interposed foreign matter such as a conductive foreign matter, the short circuit can be readily corrected by separating the line branch short-circuited with the pixel electrode using the aperture formed on the pixel electrode. In addition, because it is possible to cut the line branch at the position of the aperture, the pixel electrode is prevented from being radiated by a laser beam for cutting even when the

insulating layer between the pixel electrode and the auxiliary capacitance line is thin.

[0013] If the aperture of the pixel electrode has a slit shape, it is easy to cut the line branch by applying light energy such as a laser beam, and the decrease in the overlapping area of the pixel electrode and the line branch by the area of the apertures can be suppressed. In addition, if the line branch of the auxiliary capacitance line intersects with the aperture having the slit shape at an angle of between 80 degrees and 100 degrees, the aperture and the line branch are efficiently arranged.

[0014] If a plurality of the apertures of the pixel electrode are arranged along the length direction of the line branch of the auxiliary capacitance line, it is possible to select the most appropriate aperture for cutting depending on the position of the short circuit between the pixel electrode and the line branch, thereby limiting the effect of the cutting of the line branch. In addition, if the line branch of the auxiliary capacitance line is arranged along the signal line, the decrease in the aperture ratio of the pixel can be suppressed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] Fig. 1 is a schematic enlarged view of one pixel of a liquid crystal display device.

[0016] Fig. 2 is a sectional view of the A-A section in Fig. 1.

[0017] Fig. 3 is a view showing a correction method of an array substrate.

[0018] Fig. 4 is a view showing a modified example of the pixel of a liquid crystal display device shown in Fig. 1.

[0019] Fig. 5 is a view showing a preferred embodiment of the present invention shown in Fig. 1.

[0020] Fig. 6 is a view showing the schematic configuration of a conventional array substrate.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0021] A detailed description will now be given with reference to the accompanying drawings. In the drawings, the same configurations are provided with the same reference signs, and overlapping explanation is omitted. Fig. 1 is a schematic enlarged view of one pixel of a liquid crystal display device and Fig. 2 is a sectional view of the A-A section in Fig. 1.

[0022] As shown in Fig. 2, in a liquid crystal display device 1, a liquid crystal layer 40 is provided between a glass substrate (an array substrate) 10 and a glass substrate (a color filter substrate) 30 which are facing to each other. In addition, pixel electrodes 17 are arranged in a reticular pattern on the lower glass substrate 10.

[0023] First, a description of the glass substrate (the array substrate) 10 is given. As shown in Fig. 1, scanning lines 11 and signal lines 12 which are perpendicular to each other are arranged around the pixel electrode 17 in a reticular pattern. The scanning line 11 and the signal line 12 intersect with each other such that the signal line 12 is placed over the scanning line 11. Additionally, the scanning line 11 and the signal line 12 are electronically insulated from each other at the intersection.

[0024] At the intersection of the scanning line 11 which is arranged below the pixel electrode 17 in Fig. 1 and the signal line 12 which is arranged on the left side of the pixel electrode 17 in Fig.1, a TFT (a thin film transistor) 13 is formed as a switching element connected to a gate electrode 11a which is a part of the scanning line 11. In addition, an auxiliary capacitance line 16 made of aluminum or other material is arranged under the substantially center of the pixel electrode 17. The auxiliary capacitance line 16 comprises a line trunk 16a arranged parallel to the scanning line 11 and line branches 16b to 16e extending vertically from the line trunk 16a along the right and left ends of the pixel electrode 17. The line branches 16b to 16e are arranged to increase the ability to maintain the electric charge stored in the pixel electrode 17. Because the line branches 16b to 16e are shielded from light by black matrixes 31 of the color filter substrate 30 (to be described later), the decrease in the aperture ratio is suppressed (see Fig. 2).

[0025] The scanning line 11 and the auxiliary capacitance line 16 are arranged in the same line layer (a first line layer). That is, the scanning line 11 and the auxiliary capacitance line 16 are formed by applying patterning to the same conductive film. In addition, the scanning line 11 and the auxiliary capacitance line 16 are covered by a gate insulator 15 made of silicon nitride or other material (see Fig. 2).

[0026] At a position on the gate insulator 15 corresponding to the TFT 13, a semiconductor layer (not shown) made of amorphous silicon or other material is arranged overlapping a gate electrode 11a. A source electrode 12a and a drain electrode 14, which are parts of the signal line 12, are separately placed on the both sides of the semiconductor layer arranged on the gate electrode 11a. The signal line 12, the source electrode 12a, and the drain electrode 14 are formed in the same line layer (a second line layer) on the gate insulator 15.

[0027] The signal line 12 and the TFT 13 are covered by an interlayer insulator 19 which is formed on the gate insulator 15. The interlayer insulator 19 is made of a photosensitive acrylic resin (a photosensitive organic film) material and is arranged between constituents such as the TFT 13 and the first and second line layers (e.g., the scanning line 11 and the signal line 12) and the pixel electrode 17 in order to insulate the electric conductors from each other (see Fig. 2).

[0028] In each of pixel regions on the interlayer insulator 19, the pixel electrode 17 is provided. The pixel electrode 17 is made of a transparent electric conductor such as an ITO (indium-tin oxide) material.

[0029] The TFT 13 is on/off controlled by scanning signal voltage supplied from the gate electrode 11a of the scanning line 11. Display signal voltage supplied from the source electrode 12a of the signal line 12 is supplied

to the pixel electrode 17 via a contact hole portion 17a of the pixel electrode 17.

[0030] In the pixel electrode 17, apertures 17b to 17d are formed along the line branches 16b to 16e of the auxiliary capacitance line 16. The apertures 17b to 17d, which have a slit shape and cross the line branches 16b to 16e, are used when the branches 16b to 16e placed under the apertures 17b to 17d are cut by applying light energy such as a laser beam. In addition, a lower alignment layer 21 is formed on the pixel electrode 17. The lower alignment layer 21 is made of, for example, polyimide resin.

[0031] A description of a method to manufacture the above array substrate 10 is given. First, a single-layer or multi-layer conductor film made of materials such as tungsten, titanium, aluminum, and chromium is formed on the glass substrate 10. This conductor film can be formed using a known method such as sputtering. The formed conductor film is then formed into a predetermined pattern using a method such as photolithography. As a result, the scanning line 11 and the auxiliary capacitance line 16 are formed in the predetermined pattern.

[0032] Then, the gate insulator 15 is formed. The gate insulator 15 is made of, for example, silicon nitride and is formed by a method such as a plasma CVD method. The semiconductor layer of the TFT 13 is made of, for example, n+ type amorphous silicon and is formed by a method such as a plasma CVD method. On the gate insulator 15, the signal line 12, the source electrode 13a, and the drain electrode 14 are formed in the same manner as the scanning line.

[0033] Then, the interlayer insulating film 19 made of a photosensitive acrylic resin (a photosensitive organic film) material is formed, and a contact hole is formed on the formed interlayer insulating film 19 by a method such as photolithography. On the interlayer insulating film 19, a transparent conductive film made of an ITO material is formed using a method such as sputtering. The formed ITO film is then formed into a predetermined pattern using a method such as photolithography in order to obtain the pixel electrode 17 and the contact hole portion 17a in the predetermined pattern.

[0034] After the pixel electrode 17 is formed, the lower alignment layer 21 is formed. A liquid alignment material consisting of polyamide or other material is applied using a cylinder printing press and an inkjet printing press and is then baked by heating the substrate using a device such as a baking system. Accordingly, the solid-state lower alignment layer 21 is formed on the pixel electrode 17. The array substrate 10 is formed through the processes described above.

[0035] Next, the glass substrate (the color filter substrate) 30 is described. As shown in Fig. 2, the black matrixes 31 are arranged under the glass substrate 30. The areas on the glass substrate 10 where the scanning line 11, the signal line 12, and the TFT 13 are arranged are shielded from light by the black matrixes 31. Under the glass substrate 30, a color layer 32 having one color among red (R), green (G), and blue (B) is arranged in each pixel. In the preferred embodiment of the present invention, the red (R), green (G), and blue (B) color layers 32 are repeatedly arranged in order in the horizontal direction, while the color layers 32 having the same color are arranged in the vertical direction.

[0036] Under the color layer 32, a common electrode 33 common to each pixel is arranged. The common electrode 33 is also made of a transparent electric conductor such as an ITO material. Under the common electrode 33, an upper alignment layer 36 made of, for example, polyimide resin is formed.

[0037] The liquid crystal layer 40 is arranged between the glass substrate (the array substrate) 10 and the glass substrate (the color filter substrate) 30. In addition, polarizing plates (not shown) are arranged under the glass substrate 10 and on the glass substrate 30.

[0038] A description of a method to manufacture the above color filter substrate 30 will be given. First, a BM resist (a photosensitive resin composition including a black coloring agent) or other material is applied on the glass substrate 30. The applied BM resist is formed into a predetermined pattern by a method such as photolithography in order to obtain the black matrixes 31 in the predetermined pattern.

[0039] Then a color ink made of a red, green, or blue coloring photoresist material (a solution in which a pigment of a certain color is dispersed in photosensitive resin) is applied and formed into a predetermined pattern by a method such as photolithography to obtain the color layer 32 in the predetermined pattern. On the color layer 32, the transparent conductive film made of the ITO material is formed using a method such as sputtering to obtain the common electrode 33.

[0040] The upper alignment layer 36 is then formed on the common electrode 33. A liquid alignment material consisting of polyamide or other material is applied using a cylinder printing press or an inkjet printing press and is then baked by heating the substrate using a device such as a baking system. Accordingly, the solid-state upper alignment layer 36 is formed on the common electrode 33. The array substrate 30 is formed through the processes described above.

[0041] A description of a method to correct a point defect when there is a short circuit between the pixel electrode 17 and one of the line branches 16b to 16e of the auxiliary capacitance line 16 in the array substrate 10 shown in Fig. 1 due to an interposed foreign matter such as a conductive foreign matter will be given referring to Fig. 3.

[0042] Fig. 3A shows a correction method to be used when the pixel electrode 17 and the line branch 16d are short-circuited due to a foreign matter 25 present at the tip of the line branch 16d of the auxiliary capacitance line 16. In this case, the short-circuited portion is separated to correct the short circuit with the pixel electrode 17 by cutting the line branch 16d at a cutting portion 22 using the aperture 17b being the closest aperture to the short-

circuited portion among the three apertures 17b to 17d which are arranged between the short-circuited portion and the line trunk 16a.

[0043] Fig. 3B shows a correction method to be used when the pixel electrode 17 and the line branch 16d are short-circuited due to the foreign matter 25 present at a position closer to the tip than the middle of the line branch 16d of the auxiliary capacitance line 16. In this case, the short-circuited portion is separated to correct the short circuit with the pixel electrode 17 by cutting the line branch 16d at a cutting portion 23 using the aperture 17c being the closer aperture to the short-circuited portion of the two apertures 17c and 17d which are arranged between the short-circuited portion and the line trunk 16a.

[0044] Fig. 3C shows a correction method to be used when the pixel electrode 17 and the line branch 16d are short-circuited due to the foreign matter 25 present at a position closer to the base end than the middle of the line branch 16d of the auxiliary capacitance line 16. In this case, the short-circuited portion is separated to correct the short circuit with the pixel electrode 17 by cutting the line branch 16d at a cutting portion 24 using the aperture 17d arranged between the short-circuited portion and the line trunk 16a.

[0045] The foregoing cutting is performed by applying light energy to the cutting portions 22 to 24 of the line branch 16d, which are located in the apertures 17b to 17d, from the side of the pixel electrode 17 of the array substrate 10. Various laser beams can be used as the light energy. When the light energy is applied, the line branch 16d is cut because the conductor which composes the line branch 16d and is situated at the position radiated by the light energy is dissipated by the heat.

[0046] Even when the pixel electrode 17 and the line branch 16d are short-circuited due to the interposed conductive foreign matter 25, the short circuit can be readily corrected by separating the line branch 16d being short-circuited with the pixel electrode 17 using the apertures 17b to 17d formed on the pixel electrode 17 as described above. In addition, because it is possible to cut the line branch 16d at the positions of the apertures 17b to 17d by applying a laser beam, the pixel electrode 17 is not radiated by the laser beam for cutting even when the insulating layer (the interlayer insulating film 19 in the preferred embodiment of the present invention) between the pixel electrode 17 and the auxiliary capacitance line 16 is thin.

[0047] Because the apertures 17b to 17d of the pixel electrode 17 have a slit shape and cross the line branches 16b to 16d of the auxiliary capacitance line 16, it is easy to cut the line branches 16b to 16e by applying the laser beam. In addition, the decrease in the overlapping area of the pixel electrode and the line branches by the area of the apertures is suppressed when the apertures has the slit shape, as compared with when the apertures have, for example, a circular shape.

[0048] In addition, because a plurality of apertures 17b to 17d of the pixel electrode 17 are arranged along the length direction of the line branches 16b to 16e, it is possible to select the most appropriate aperture for cutting depending on the position of the short-circuited portion between the pixel electrode 17 and the line branches 16b to 16e, thereby limiting the effect of the cutting of the line branch.

[0049] The line branches 16b to 16e may also be arranged along the signal lines 12; however, line branches 16f and 16g extending vertically from the line trunk 16a may be formed in the center of the pixel electrode 17, and apertures 17e to 17g are formed in the line branches 16f and 16g as shown in Fig. 4.

[0050] The preferred embodiment of the present invention is represented by the configuration shown in Fig. 5 may be used. An array substrate 42 shown in Fig. 5 is used for a vertical alignment liquid crystal display device having liquid crystal molecules with negative dielectric anisotropy. In addition to being used to correct a short circuit between the pixel electrode 17 and line branches 16h to 16k due to an interposed conductive foreign matter, apertures 17h to 17k can also be used to improve viewing angle characteristics by generating an oblique electric field (a fringe field) when voltage is applied to the pixel electrode 17 and thereby controlling the alignment of the liquid crystal molecules (not shown). As shown in Fig. 5, the apertures 17h to 17k have an oblique slit shape and are arranged symmetrically with respect to the line trunk 16a such that they cross the line branches 16h to 16k in the layer below. The correction method shown in Fig. 3 is of course applicable to this array substrate 42.

Claims

1. An array substrate (42) comprising a pixel electrode (17) connected to a switching element arranged near an intersection between a scanning line (11) and a signal line (12) and an auxiliary capacitance line (16) arranged in a layer below the pixel electrode (17), wherein the auxiliary capacitance line (16) comprises a line trunk (16a) arranged substantially parallel to the scanning line (11) and a line branch (16h to 16k) extending from the line trunk (16a), and the pixel electrode (17) is provided with an aperture (17h to 17k) which crosses the line branch (16h to 16k) of the auxiliary capacitance line (16),
characterized in that the line branch (16h to 16k) is arranged obliquely with regard to the line trunk (16a) and that
the apertures (17h to 17k) of the pixel electrode (17) have a slit shape and are arranged obliquely with respect to the line trunk (16a).

2. The array substrate (42) according to claim 1, wherein the line branch (16h to 16k) of the auxiliary capacitance line (16) intersects with the aperture (17h to 17k) having the slit shape at an angle of between 80 degrees and 100 degrees.

3. A correction method of the array substrate (42) according to claim 1 or 2 comprising cutting the line branch (16b to 16e) of the auxiliary capacitance line (16) using the aperture (17h to 17k) of the pixel electrode (17) when there is a short circuit between the pixel electrode (17) and the line branch (16h to 16k) of the auxiliary capacitance line (16).

4. A liquid crystal display device comprising the array substrate (42) according to claim 1 or 2, a substrate which is arranged facing to the array substrate (42) and has a common electrode, and a crystal filled between the array substrate (42) and the substrate.

Patentansprüche

1. Matrixsubstrat (42), mit einer Pixelelektrode (17), die mit einem Schaltelement verbunden ist, das in der Nähe eines Schnittpunkts zwischen einer Abtastleitung (11) und eine Signalleitung (12) angeordnet ist, und mit einer Hilfskapazitätsleitung (16), die in einer Schicht unter der Pixelelektrode (17) angeordnet ist, wobei die Hilfskapazitätsleitung (16) eine Verbindungsleitung (16a), die im Wesentlichen parallel zu der Abtastleitung (11) angeordnet ist, und eine Zweigleitung (16h bis 16k), die sich von der Verbindungsleitung (16a) erstreckt, aufweist, wobei die Pixelelektrode (17) mit einer Öffnung (17h bis 17k) versehen ist, die die Zweigleitung (16h bis 16k) der Hilfskapazitätsleitung (16) kreuzt,
dadurch gekennzeichnet, dass die Zweigleitung (16h bis 16k) in Bezug auf die Verbindungsleitung (16a) schräg angeordnet ist und dass
die Öffnungen (17h bis 17k) der Pixelelektrode (17) eine Schlitzform haben und in Bezug auf die Verbindungsleitung (16a) schräg angeordnet sind.

2. Matrixsubstrat (42) nach Anspruch 1, wobei die Zweigleitung (16h bis 16k) der Hilfskapazitätsleitung (16) die Öffnung (17h bis 17k) mit der Schlitzform unter einem Winkel im Bereich von 80 Grad bis 100 Grad schneidet.

3. Verfahren zum Korrigieren des Matrixsubstrats (42) nach Anspruch 1 oder 2, das das Durchtrennen der Zweigleitung (16b bis 16e) der Hilfskapazitätsleitung (16) unter Verwendung der Öffnung (17h bis 17k) der Pixelelektrode (17) enthält, wenn zwischen der Pixelelektrode (17) und der Zweigleitung (16h bis 16k) der Hilfskapazitätsleitung (16) ein Kurzschluss besteht.

4. Flüssigkristallanzeigevorrichtung, die das Matrixsubstrat (42) nach Anspruch 1 oder 2, ein Substrat, das so angeordnet ist, dass es dem Matrixsubstrat (42) zugewandt ist, und eine gemeinsame Elektrode besitzt, und einen Kristall, der zwischen das Matrixsubstrat (42) und das Substrat gefüllt ist, enthält.

Revendications

1. Substrat de réseau (42), comportant une électrode de pixel (17) reliée à un élément de commutation disposé à proximité d'une intersection entre une ligne de balayage (11) et une ligne de signal (12), et une ligne de capacité auxiliaire (16), disposée dans une couche située au-dessous de l'électrode de pixel (17), dans lequel la ligne de capacité auxiliaire (16) comporte une interconnexion de ligne (16a), disposée de manière sensiblement parallèle à la ligne de balayage (11), et une branche de ligne (16h à 16k) se prolongeant à partir de l'interconnexion de ligne (16a), et l'électrode de pixel (17) possède une ouverture (17h à 17k) coupant la branche de ligne (16h à 16k) de la ligne de capacité auxiliaire (16),
caractérisé en ce que la branche de ligne (16h à 16k) est disposée selon une orientation oblique par rapport à l'interconnexion de ligne (16a), et **en ce que**
les ouvertures (17h à 17k) de l'électrode de pixel (17) possèdent une forme de fente et sont disposées selon une orientation oblique par rapport à l'interconnexion de ligne (16a).

2. Substrat de réseau (42) selon la revendication 1, dans lequel la branche de ligne (16h à 16k) de la ligne de capacité auxiliaire (16) coupe l'ouverture (17h à 17k) en forme de fente selon un angle compris entre 80 degrés et 100 degrés.

3. Procédé de correction de substrat de réseau (42) selon la revendication 1 ou 2, comportant le coupage de la branche de ligne (16b à 16e) de la ligne de capacité auxiliaire (16) en utilisant l'ouverture (17h à 17k) de l'électrode de pixel (17) lorsqu'il existe un court-circuit entre l'électrode de pixel (17) et la branche de ligne (16h à 16k) de la ligne de capacité auxiliaire (16).

4. Dispositif d'affichage à cristaux liquides, comportant le substrat de réseau (42) selon la revendication 1 ou 2, un substrat disposé en opposition au substrat de réseau (42) et possédant une électrode commune, et des cristaux liquides introduits entre le substrat de réseau (42) et le substrat.

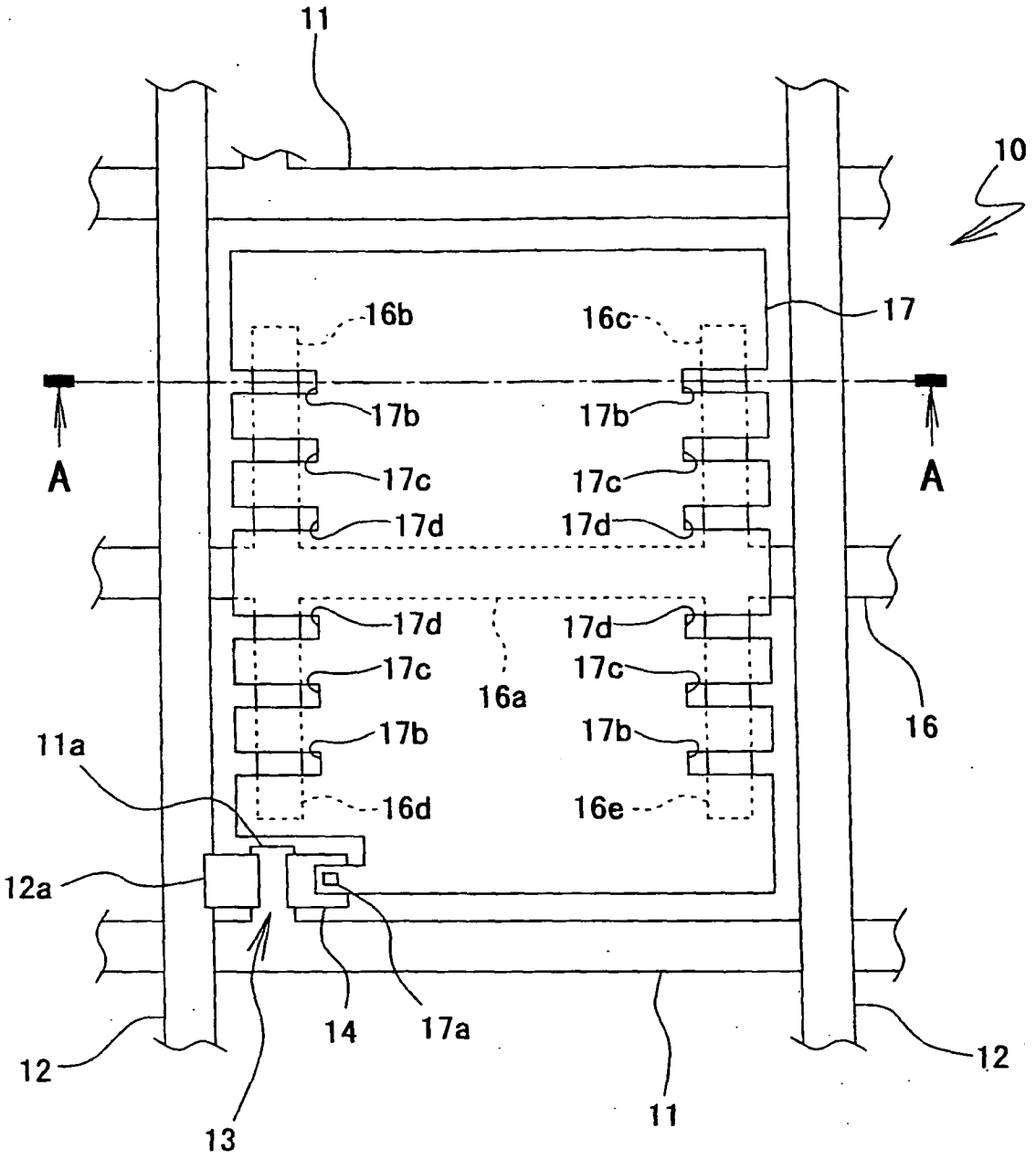

11
10
16b
16c
17
17b
17b
A
A
17c
17c
17d
17d
17d
17d
17c
17c
16a
16
11a
17b
17b
16d
16e
12a
14
17a
12
12
13
11

FIG. 1

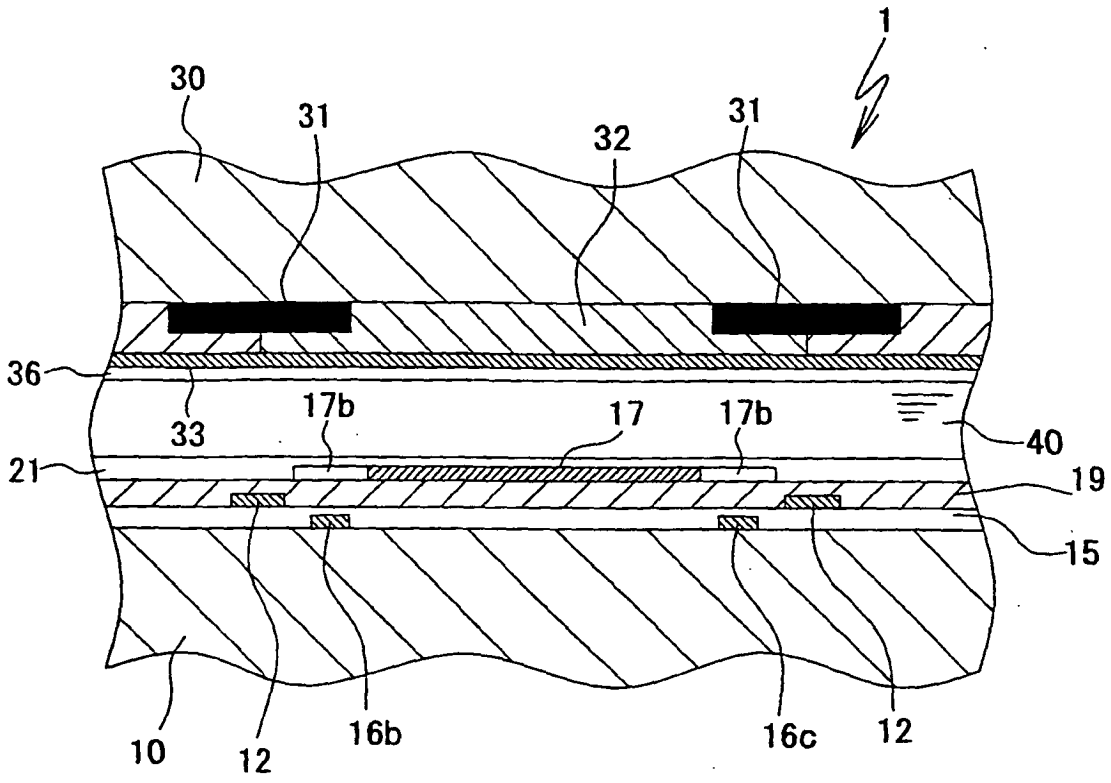


FIG. 2

FIG. 3A

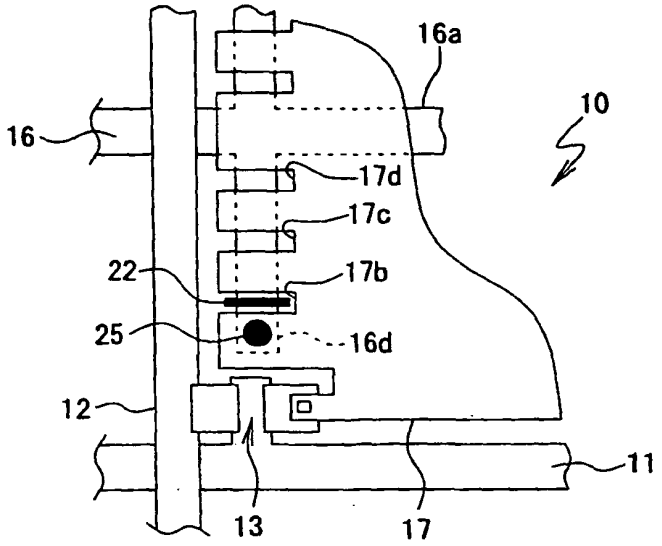


FIG. 3B

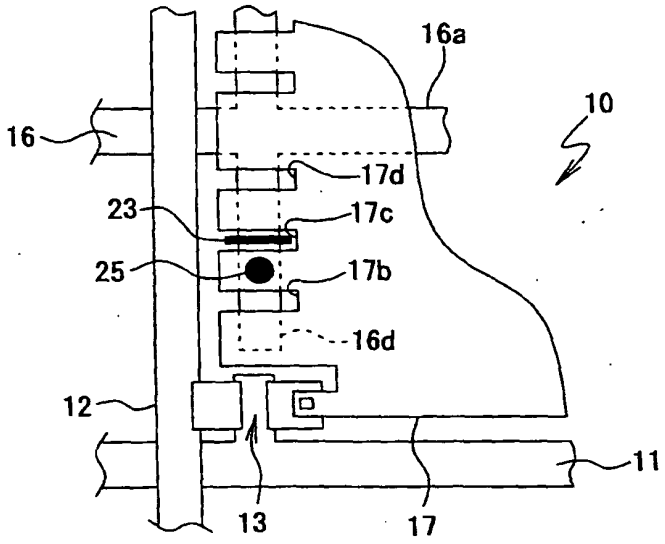
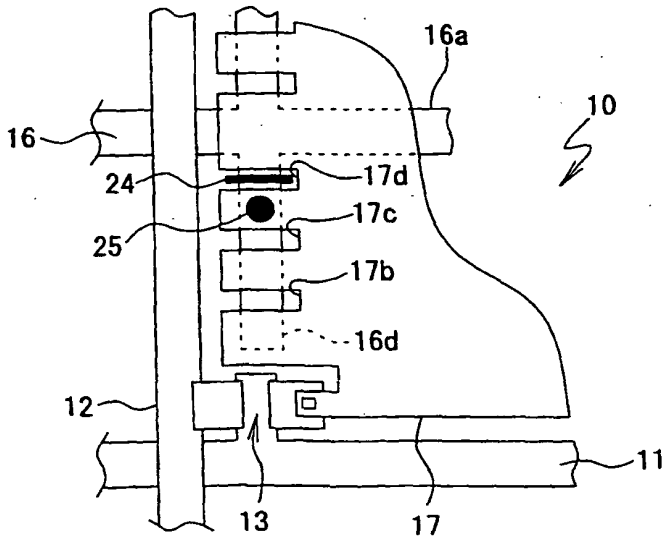


FIG. 3C



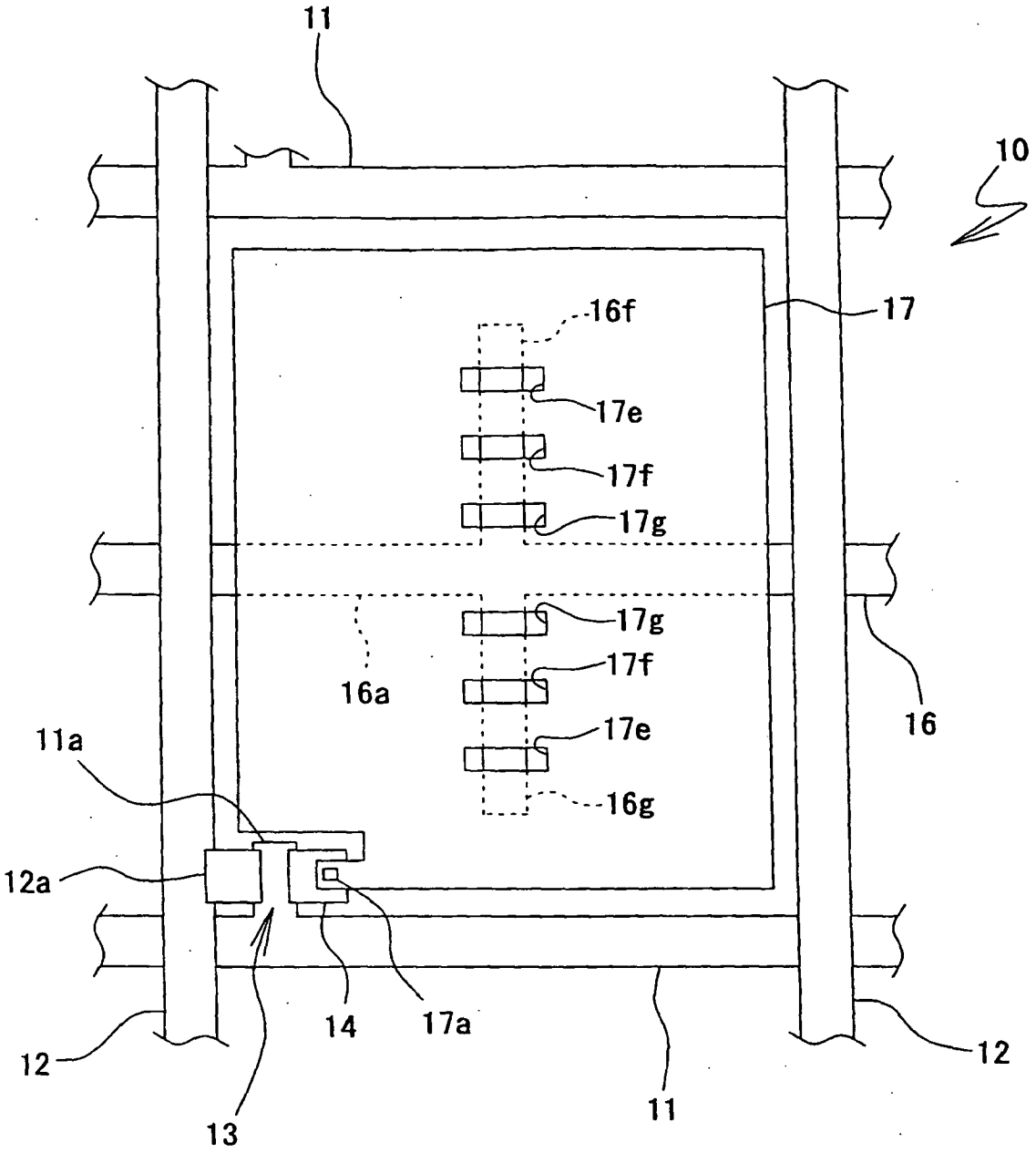

11
10
16f
17
17e
17f
17g
17g
17f
17e
16g
16a
16
11a
12a
12
13
14
17a
11
12

FIG. 4

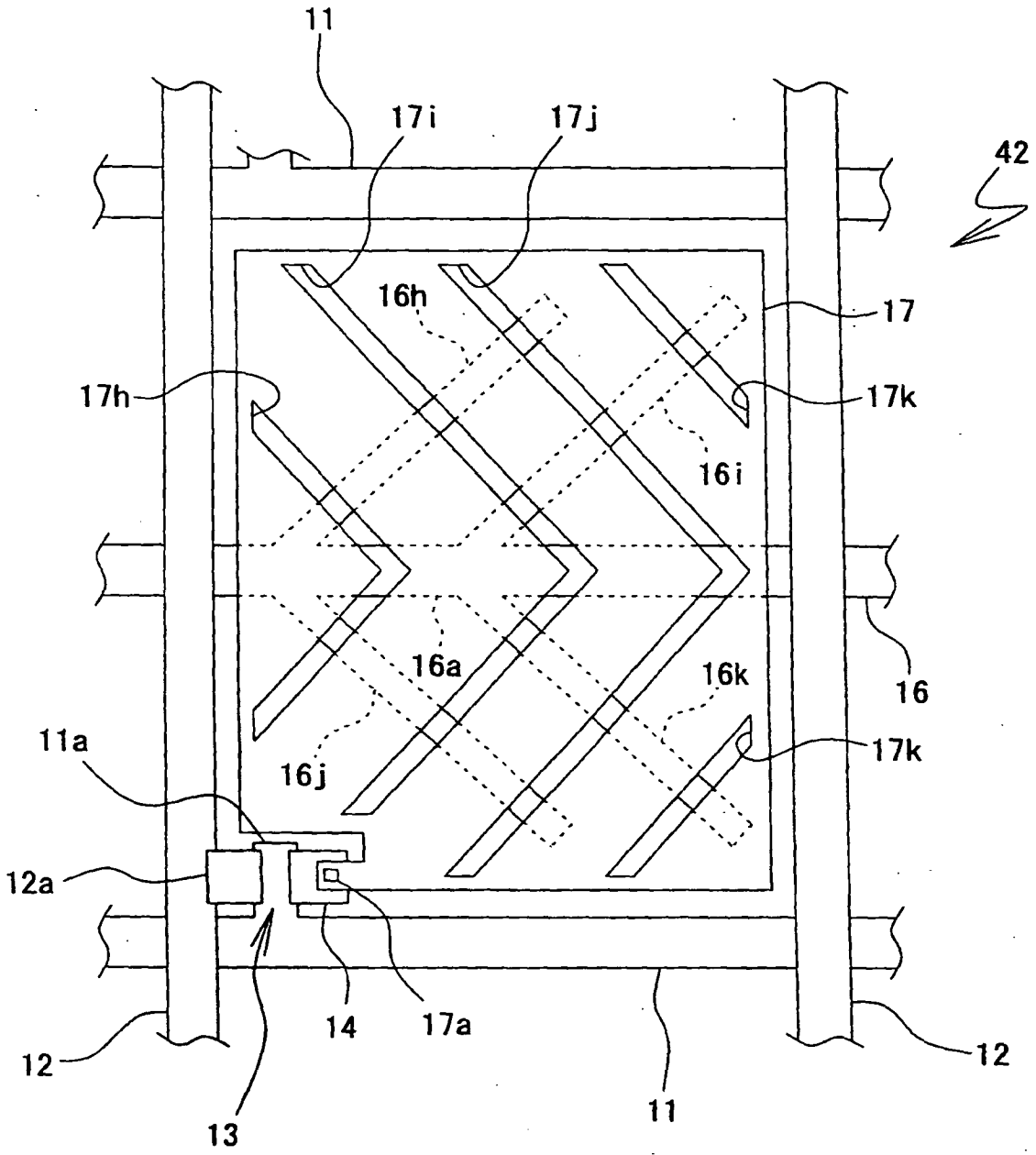

11
17i
17j
42
16h
17
17h
17k
16i
16a
16k
16
11a
16j
17k
12a
14
17a
12
12
13
11

FIG. 5

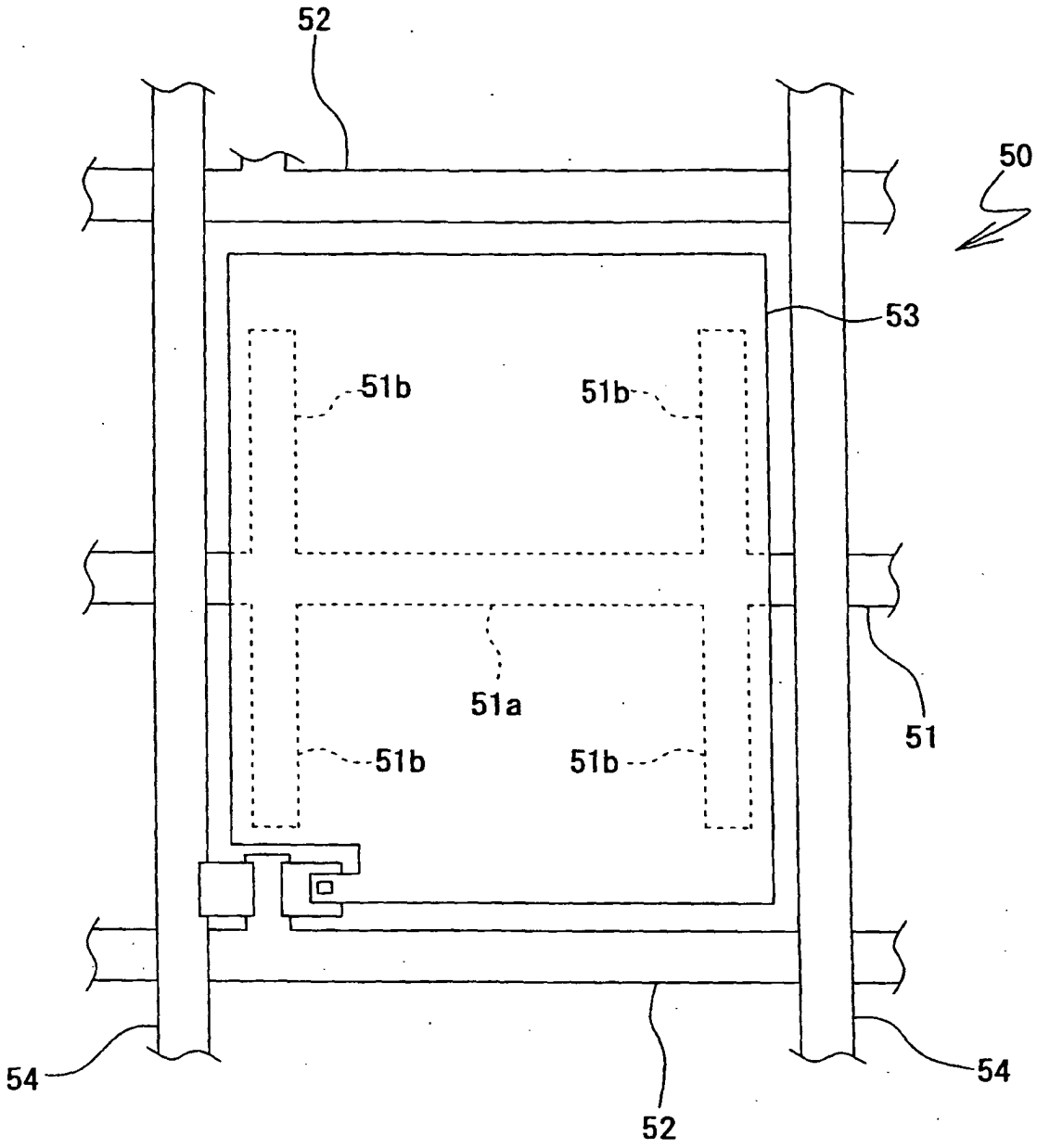


FIG. 6

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- JP 2004053752 A **[0004]**

专利名称(译)	阵列基板，用于校正阵列基板的方法和液晶显示器		
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摘要(译)

其中可以容易地校正辅助电容线的线分支和像素电极之间的短路的阵列基板包括连接到布置在扫描线和信号线之间的交叉点附近的开关元件的像素电极和辅助电容布置在像素电极下方的层中的线，其中辅助电容线包括基本上平行于扫描线布置的线主干和从线主干延伸的线分支，并且像素电极设置有穿过线分支的孔辅助电容线。