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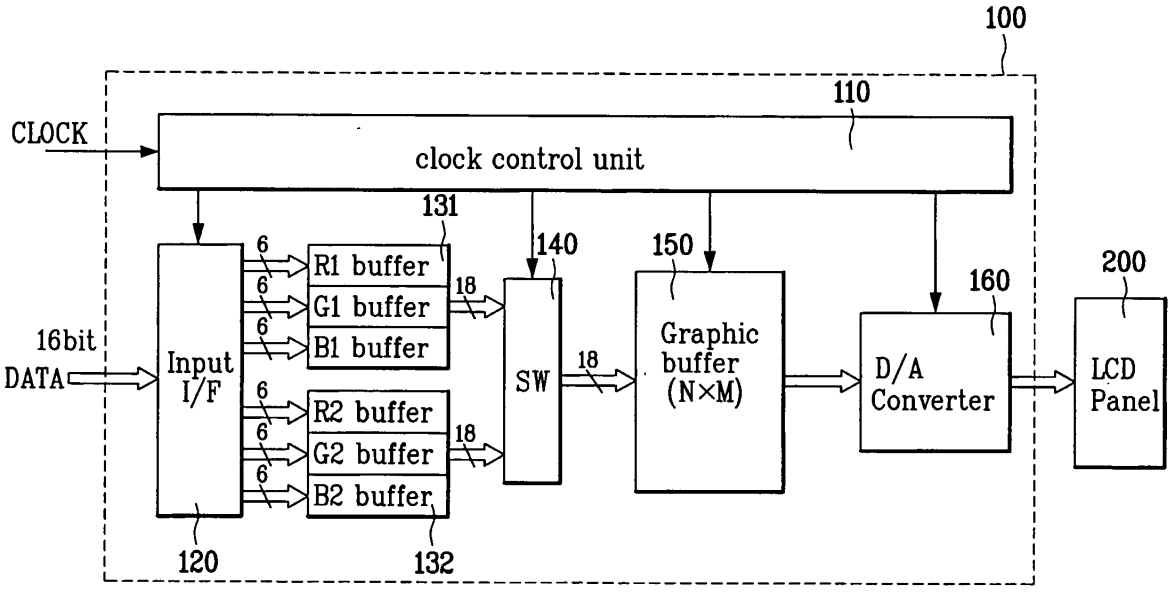
## (54) Apparatus for controlling color liquid crystal display and method thereof

(57) An apparatus for controlling a color liquid crystal display and method thereof are disclosed, by which data transfer efficiency is raised in a manner of changing an input interface type of an LCD controller, by which a same-sized video can be outputted with a smaller number of clocks, and by which practical applicability of CPU is enhanced. The present invention includes a clock control unit providing a clock for operating each module, an interface unit receiving 16-bit data each clock according to a control signal of the clock control unit, a pair of 18-bit RGB buffers storing data transferred via the interface unit, a graphic buffer storing graphic data provided from a pair of the RGB buffers, a switching block storing data signals provided from a pair of the RGB buffers in the graphic buffer, and a digital/analog converting unit converting digital R/G/B data stored in the graphic buffer to an analog signal to output.

FIG. 4

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## Description

**[0001]** This application claims the benefit of the Korean Patent Application No. 10-2004-0071328, filed on September 7, 2004, which is hereby incorporated by reference as if fully set forth herein.

## BACKGROUND OF THE INVENTION

### Field of the Invention

**[0002]** The present invention relates to a color liquid crystal display, and more particularly, to an apparatus for controlling a color liquid crystal display and method thereof. Although the present invention is suitable for a wide scope of applications, it is particularly suitable for reducing a processing time of a central processing unit having a 16-bit interface.

### Discussion of the Related Art

**[0003]** Generally, a liquid crystal display (hereinafter abbreviated LCD) is an instrument displaying a color video by receiving three kinds of signals R (red), G (green) and B (blue). An LCD widely used for a commercial portable terminal normally supports a 5:6:5 mode or 6:6:6 mode. The 5:6:5-mode LCD represents R, G and B with 5-, 6- and 5-bits, respectively to represent about 65,000 colors. And, the 6:6:6-mode LCD represents R, G and B with 6-bits each to represent about 260,000 colors.

**[0004]** An LCD interfaces can be classified into a parallel type and a serial type. The parallel type interface can be further classified into an 8-bit type, a 16-bit type and an 18-bit type. And, the interface widely used for the commercial portable terminal is the 16-bit parallel type interface. This is because a CPU controlling a portable terminal provides the 16-bit type interface. In case of representing 65,000 colors (5:6:5 mode) in an LCD using the 16-bit parallel type interface, one CPU clock is needed to transfer data of one pixel. Hence, in order to represent an overall video on an LCD having a size of 'N x M', 'N x M' clocks are needed. Yet, in case of representing 260,000 colors (6:6:6 mode) by the LCD using the 16-bit parallel type interface, CPU clocks, which are twice more than are needed to represent the 5:6:5 mode, are needed to transfer data of one pixel. Namely, '2 x N x M' clocks are needed to represent one video on the LCD having a size of 'N X M'. And, it takes a data transfer time twice longer than is needed to represent 65,000 colors.

**[0005]** FIG. 1 is a block diagram of an LCD controller according to a related art, in which a 16-bit parallel type interface is used.

**[0006]** Referring to FIG. 1, an LCD controller 10 consists of a clock control unit 11, an input interface 12, an RGB buffer 13, a graphic buffer 14 and a D/A converter 15.

**[0007]** The clock control unit 11 provides a basic clock to operate each of the modules 12, 13, 14 and 15. The input interface 12 plays a role in storing 16-bit data inputted to the LCD module in the RGB buffer 13. The RGB buffer 13 temporarily stores RGB data configured with six bits each. The graphic buffer 14 stores overall video data to be outputted to an LCD panel 20. A size of the graphic buffer 14 corresponds to 'N x M' and each pixel is represented by 18-bits. And, the D/A converter 15 converts digital RGB data to an analog voltage to output. The LCD panel 20 is a final output end that outputs a video.

**[0008]** FIG. 2 is a diagram of an LCD controller input data format according to a related art.

**[0009]** Referring to FIG. 2, 16-bit data is inputted via the input interface 12 of the LCD controller each clock. The data inputted for two clocks configure one pixel of an 'N x M' sized video. Namely, the data inputted for '2 x N x M' clocks configure one video.

**[0010]** The RGB data inputted in the format shown in FIG. 2 are stored in the RGB buffer as shown in FIG. 3A and FIG. 3B and are stored in the graphic buffer by a control of the clock control unit.

**[0011]** FIG. 3A is an exemplary diagram of a 16-bit data format of a first clock in FIG. 2.

**[0012]** Referring to FIG. 3A, when data configuring one pixel are inputted to the LCD controller, 6-bit data between D5~D0 among the 16-bit data inputted for the first clock indicates a brightness of R.

**[0013]** FIG. 3B is an exemplary diagram of a 16-bit data format of a second clock in FIG. 2.

**[0014]** Referring to FIG. 3B, 6-bit data between D15~D10 among the 16-bit data inputted for the second clock indicates a brightness of G and 6-bit data between D5~D0 indicates a brightness of B. Namely, the rest of bit information failing to be explained in the above description among the overall 32-bit data inputted for two clocks is not used (Don't care).

**[0015]** All kind of pixel information repeatedly inputted according to the above process is stored in the graphic buffer to configure one video. Videos stored in the graphic buffer 14 are converted to an analog voltage via the D/A converter 15. And, the analog voltage finally drives the LCD panel 20.

**[0016]** However, in the related art system, since the data between D15~D10 of the 16-bit data inputted for the first clock are not used in receiving the data configuring one pixel, efficiency of data transfer is degraded. For this reason, '2 x N x M' CPU clocks are used in transferring the overall video of the 'N x M' size to the LCD module, a corresponding data transfer time is increased.

## SUMMARY OF THE INVENTION

**[0017]** Accordingly, the present invention is directed to an apparatus for controlling a color liquid crystal display and method thereof that substantially obviate one or more problems due to limitations and disadvantages of the related art.

**[0018]** An object of the present invention is to provide

an apparatus for controlling a color liquid crystal display and method thereof, by which data transfer efficiency is raised in a manner of changing an input interface type of an LCD controller.

**[0019]** Another object of the present invention is to provide an apparatus for controlling a color liquid crystal display and method thereof, by which a same-sized video can be outputted with a smaller number of clocks.

**[0020]** A further object of the present invention is to provide an apparatus for controlling a color liquid crystal display and method thereof, by which practical applicability of CPU is enhanced.

**[0021]** Additional advantages, objects, and features of the invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from practice of the invention. The objectives and other advantages of the invention may be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

**[0022]** To achieve these objects and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, a method of controlling a color liquid crystal display according to the present invention includes the steps of receiving 16-bit video data each clock and processing data of two pixels each three clocks to represent 260,000 colors.

**[0023]** In another aspect of the present invention, a method of controlling a color liquid crystal display includes the steps of receiving 16-bit video data each clock, temporarily storing R, G and B data represented by six bits each in a pair of 18-bit buffers, selecting the data stored in a pair of the 18-bit buffers according to a control signal of a clock control unit, storing the selected data in a graphic buffer, and driving a color liquid crystal using the video data stored in the graphic buffer.

**[0024]** In another aspect of the present invention, an apparatus for controlling a color liquid crystal display includes a clock control unit providing a clock for operating each module, an interface unit receiving 16-bit data each clock according to a control signal of the clock control unit, a pair of 18-bit RGB buffers storing data transferred via the interface unit, a graphic buffer storing graphic data provided from a pair of the RGB buffers, a switching block storing data signals provided from a pair of the RGB buffers in the graphic buffer, and a digital/analog converting unit converting digital R/G/B data stored in the graphic buffer to an analog signal to output.

**[0025]** And, a method of controlling a color liquid crystal display is characterized in receiving 16-bit data each clock, configuring two pixels each three clocks, and transferring video data for '(3/2) x N x M' clocks.

**[0026]** It is to be understood that both the foregoing general description and the following detailed description of the present invention are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0027]** The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this application, illustrate embodiment(s) of the invention and together with the description serve to explain the principle of the invention. In the drawings:

**[0028]** FIG. 1 is a block diagram of an LCD controller according to a related art;

**[0029]** FIG. 2 is a diagram of an LCD controller input data format according to a related art;

**[0030]** FIG. 3A is an exemplary diagram of a 16-bit data format of a first clock in FIG. 2;

**[0031]** FIG. 3B is an exemplary diagram of a 16-bit data format of a second clock in FIG. 2;

**[0032]** FIG. 4 is a block diagram of an LCD controller according to the present invention;

**[0033]** FIG. 5 is a diagram of an input data format of an LCD controller according to the present invention;

**[0034]** FIG. 6A is an exemplary diagram of a 16-bit data format of a first clock in FIG. 5;

**[0035]** FIG. 6B is an exemplary diagram of a 16-bit data format of a second clock in FIG. 5; and

**[0036]** FIG. 6C is an exemplary diagram of a 16-bit data format of a third clock in FIG. 5.

## DETAILED DESCRIPTION OF THE INVENTION

**[0037]** Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

**[0038]** An apparatus for controlling an LCD and method thereof according to the present invention are explained with reference to the attached drawings as follows.

**[0039]** FIG. 4 is a block diagram of an LCD controller according to the present invention.

**[0040]** Referring to FIG. 4, an LCD controller 100 according to the present invention includes a clock control unit 110 providing a clock to operate each module, an interface unit 120 receiving 16-bit data each clock, a pair of 18-bit RGB buffers 131 and 132 storing data transferred via the interface unit 120, a graphic buffer 150 storing graphic data provided from a pair of the RGB buffers 131 and 132, a switching block 140 alternately reading data signals provided from a pair of the RGB buffers 131 and 132 according to the clock provided from the clock control unit to store in the graphic buffer 150, and a digital/analog converting unit 160 converting digital R/G/B data stored in the graphic buffer 150 to an analog signal to output.

**[0041]** The LCD controller according to the present invention differs from the related art LCD controller in including a pair of the RGB buffers and in using the switch-

ing block additionally. A pair of the RGB buffers 131 and 132 are used in storing pixel data temporarily. Each of the RGB buffers 131 and 132 includes an 18-bit buffer to store R, G and B data, each of which is represented by 6-bits. The switching block 140 plays a role in selecting data of R1, G1 and B1 buffers or data of R2, G2 and B2 buffers according to a control signal of the clock control unit 110.

**[0042]** FIG. 5 is a diagram of an input data format of an LCD controller according to the present invention.

**[0043]** Referring to FIG. 5, 16-bit data is inputted each clock via the input interface of the LCD controller. And, data inputted for three clocks configure two pixels. For instance, it is assumed that pixel data of coordinates (Xn, Ym) and pixel data of coordinates (Xn+1, Ym) are inputted. 6-bit data between D13~D8 of the 16-bit data inputted for a first clock, as shown in FIG. 6A, indicate a brightness of R configuring a pixel of the coordinates (Xn, Ym) and 6-bit data between D5~D0 indicate a brightness of G configuring the pixel of the coordinates (Xn, Ym). 6-bit data between D13~D8 of the 16-bit data inputted for a second clock, as shown in FIG. 6B, indicate the brightness of B configuring the pixel of the coordinates (Xn, Ym) and 6-bit data between D5~D0 indicate a brightness of R configuring a pixel of the coordinates (Xn+1, Ym). And, 6-bit data between D13~D8 of the 16-bit data inputted for a third clock, as shown in FIG. 6C, indicate a brightness of G configuring the pixel of the coordinates (Xn+1, Ym) and 6-bit data between D5~D0 indicate a brightness of B configuring the pixel of the coordinates (Xn+1, Ym).

**[0044]** 16-bit data inputted after the third clock follow the repetitions of the input formats of the previous three clocks. Hence, '(3/2) x N x M' clocks are needed to transfer one video data completely.

**[0045]** The above-inputted RGB data are alternately stored in a pair of the 18-bit buffers (R1/G1/B1 buffer and R2/G2/B2 buffer), respectively. And, data of the two RGB buffers 131 and 132 are alternately read by the switch block 140 to be stored in the graphic buffer 150. Finally, the video data stored in the graphic buffer 150 is converted to a voltage via the D/A converter 160. By the voltage, an LCD panel 200 is then driven. Besides, synchronization between the input interface unit 120 and the switching block 140 is controlled by the clock control unit 110.

**[0046]** Accordingly, the LCD controller of the present invention is capable of transferring the same-sized video with the number of clocks smaller than the related art number of clocks, thereby bringing about speed enhancement.

**[0047]** And, the present invention enables the CPU to do a different work for a saved time, thereby enhancing the practical applicability of the CPU.

**[0048]** It will be apparent to those skilled in the art that various modifications and variations can be made in the present invention without departing from the spirit or scope of the inventions. Thus, it is intended that the present invention covers the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

## Claims

1. A method of controlling a color liquid crystal display, comprising the steps of:

   receiving 16-bit video data each clock; and
   processing data of two pixels each three clocks to represent 260,000 colors.

2. A method of controlling a color liquid crystal display, comprising the steps of:

   receiving 16-bit video data each clock;
   temporarily storing R, G and B data represented by six bits each in a pair of 18-bit buffers;
   selecting the data stored in a pair of the 18-bit buffers according to a control signal of a clock control unit;
   storing the selected data in a graphic buffer; and
   driving a color liquid crystal using the video data stored in the graphic buffer.

3. The method of claim 2, wherein the R, G and B data of the received 16-bit video data are alternately stored in a pair of RGB buffers.

4. The method of claim 2, wherein data of a pair of RGB buffers are alternately read according to a clock provided from the clock control unit to be stored in the graphic buffer.

5. The method of claim 2, wherein if n is an integer greater than zero, the data stored in the graphic buffer indicates brightnesses of R and G of an odd pixel for a $(3n+1)^{th}$ clock, a brightness of B of an odd pixel and a brightness of G of an even pixel for a $(3n+2)^{th}$ clock, or brightnesses of G and B of an even pixel for a $3n^{th}$ clock.

6. The method of claim 5, wherein 6-bit data between D13~D8 include either brightnesses of R and B of the odd pixel or a brightness of G of the even pixel and wherein 6-bit data between D5~D0 include either a brightness of G of the odd pixel or brightnesses of R and B of the even pixel.

7. An apparatus for controlling a color liquid crystal display, comprising:

   a clock control unit providing a clock for operating each module;
   an interface unit receiving 16-bit data each clock according to a control signal of the clock control unit;

a pair of 18-bit RGB buffers storing data transferred via the interface unit;
a graphic buffer storing graphic data provided from a pair of the RGB buffers;
a switching block storing data signals provided from a pair of the RGB buffers in the graphic buffer; and
a digital/analog converting unit converting digital R/G/B data stored in the graphic buffer to an analog signal to output.

**8.** The apparatus of claim 7, the interface unit alternately stores R, G and B data of the received 16-bit data in a pair of the RGB buffers.

**9.** The apparatus of claim 7, wherein the switching block alternately reads the data of a pair of the RGB buffers according to the clock provided from the clock control unit and stores the read data in the graphic buffer.

**10.** The apparatus of claim 7, wherein if n is an integer greater than zero, the data stored in the graphic buffer indicates brightnesses of R and G of an odd pixel for a $(3n+1)^{th}$ clock, a brightness of B of an odd pixel and a brightness of G of an even pixel for a $(3n+2)^{th}$ clock, or brightnesses of G and B of an even pixel for a $3n^{th}$ clock.

**11.** The apparatus of claim 10, wherein 6-bit data between D13~D8 include either brightnesses of R and B of the odd pixel or a brightness of G of the even pixel and wherein 6-bit data between D5~D0 include either a brightness of G of the odd pixel or brightnesses of R and B of the even pixel.

FIG. 1

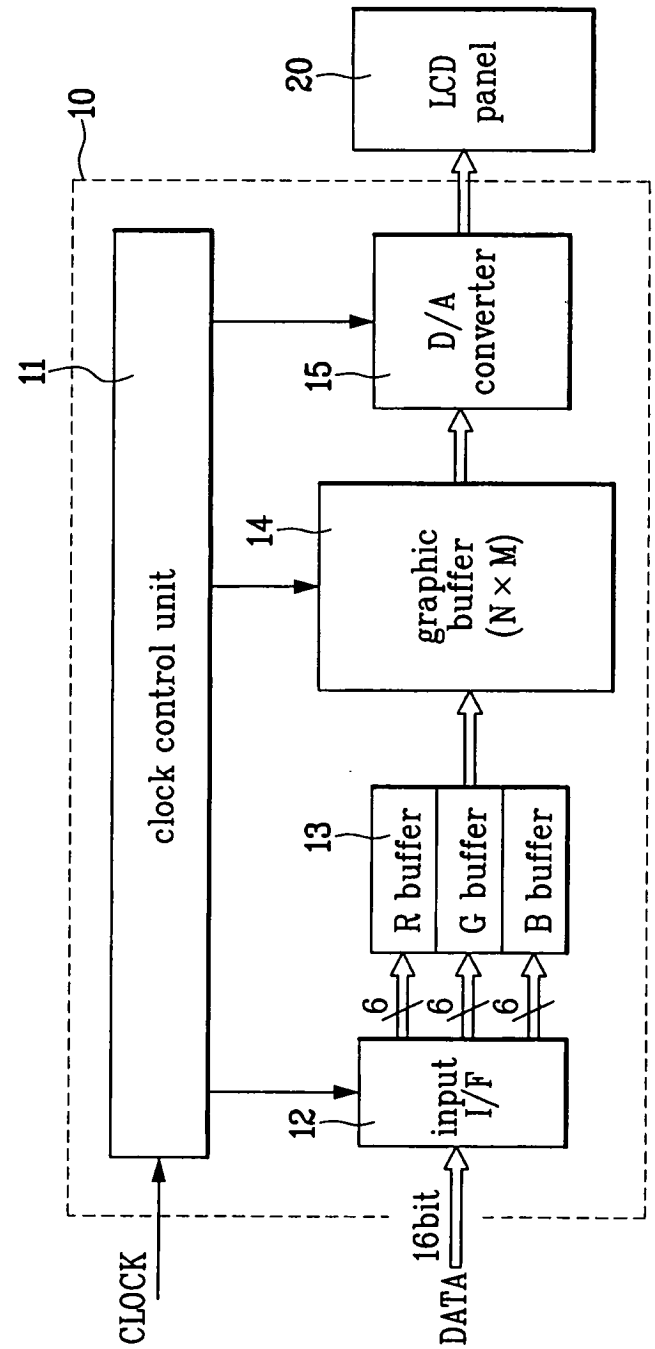
20
LCD panel
10
11
clock control unit
15
D/A converter
14
graphic buffer (N × M)
13
R buffer
G buffer
B buffer
6
6
6
12
input I/F
CLOCK
16bit
DATA

FIG. 2

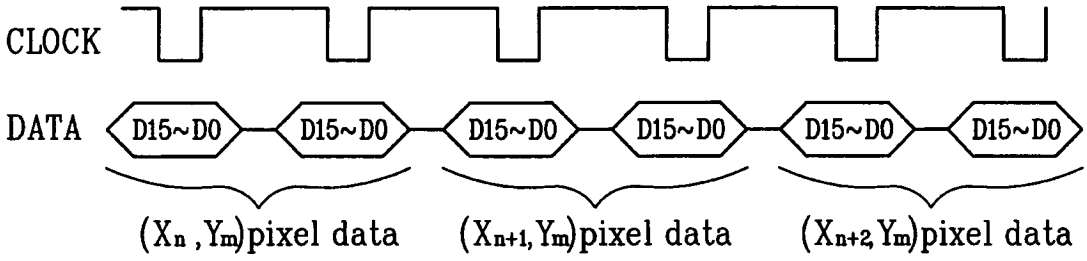


FIG. 3A

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Don't Care | | | | | | | | Don't Care | | R($X_n$ , $Y_m$) | | | | | |

FIG. 3B

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Don't Care | | G($X_n$ , $Y_m$) | | | | | | Don't Care | | B($X_n$ , $Y_m$) | | | | | |

FIG. 4

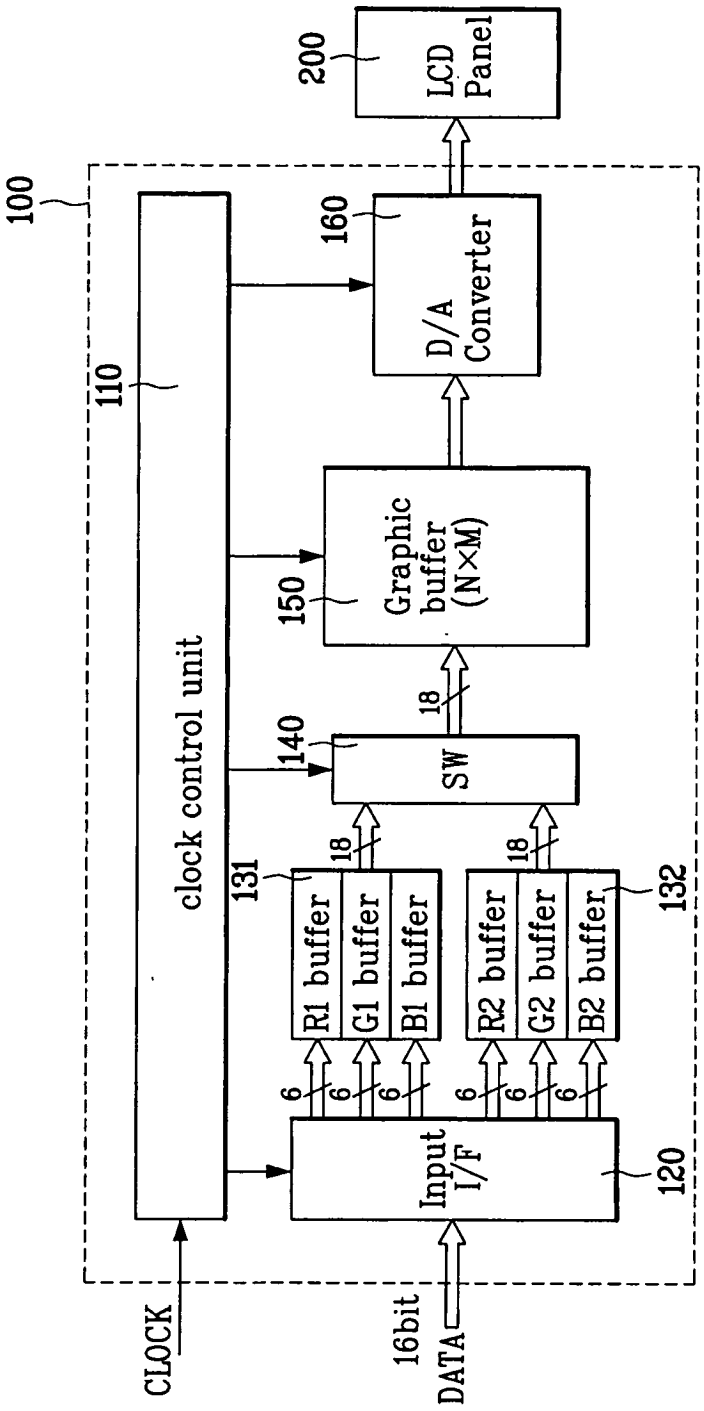
200
LCD Panel
100
160
D/A Converter
110
clock control unit
Graphic buffer (N×M)
150
18
140
SW
18
18
131
R1 buffer
G1 buffer
B1 buffer
R2 buffer
G2 buffer
B2 buffer
132
6
6
6
6
6
6
Input I/F
120
CLOCK
16bit DATA

FIG. 5

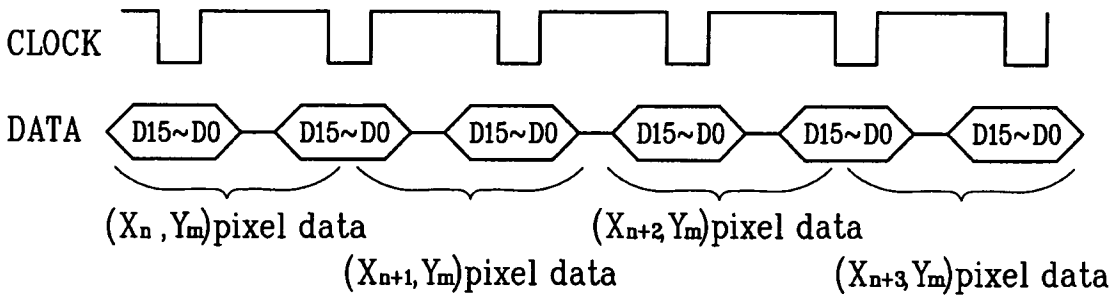
CLOCK
DATA
D15~D0
D15~D0
D15~D0
D15~D0
D15~D0
D15~D0
(Xn , Ym)pixel data
(Xn+1, Ym)pixel data
(Xn+2, Ym)pixel data
(Xn+3, Ym)pixel data

FIG. 6A

| D15 D14 | D13 D12 D11 D10 D9 D8 | D7 D6 | D5 D4 D3 D2 D1 D0 |
|---|---|---|---|
| Don't Care | $R(X_n, Y_m)$ | Don't Care | $G(X_n, Y_m)$ |

FIG. 6B

| D15 D14 | D13 D12 D11 D10 D9 D8 | D7 D6 | D5 D4 D3 D2 D1 D0 |
|---|---|---|---|
| Don't Care | $B(X_n, Y_m)$ | Don't Care | $R(X_{n+1}, Y_m)$ |

FIG. 6C

| D15 D14 | D13 D12 D11 D10 D9 D8 | D7 D6 | D5 D4 D3 D2 D1 D0 |
|---|---|---|---|
| Don't Care | $G(X_{n+1}, Y_m)$ | Don't Care | $B(X_{n+1}, Y_m)$ |

| | | | |
|---|---|---|---|
| 专利名称(译) | 用于控制彩色液晶显示器的装置及其方法 | | |
| 公开(公告)号 | EP1632931A2 | 公开(公告)日 | 2006-03-08 |
| 申请号 | EP2005019113 | 申请日 | 2005-09-02 |
| 申请(专利权)人(译) | LG电子株式会社. | | |
| 当前申请(专利权)人(译) | LG电子株式会社. | | |
| [标]发明人 | YOUNG JIN CHOI | | |
| 发明人 | YOUNG-JIN, CHOI | | |
| IPC分类号 | G09G3/36 G09G5/02 G09G5/39 | | |
| CPC分类号 | G09G5/02 G06F3/147 G09G3/2096 G09G3/3611 G09G5/006 G09G5/393 G09G2310/027 G09G2370/045 | | |
| 优先权 | 1020040071328 2004-09-07 KR | | |
| 其他公开文献 | EP1632931A3 | | |
| 外部链接 | Espacenet | | |


摘要(译)

公开了一种用于控制彩色液晶显示器的装置及其方法，通过改变LCD控制器的输入接口类型来提高数据传输效率，通过该输入接口类型可以以较小的数量输出相同大小的视频。时钟，以及增强CPU的实际适用性。本发明包括：时钟控制单元，提供用于操作每个模块的时钟;接口单元，根据时钟控制单元的控制信号，每个时钟接收16位数据;一对18位RGB缓冲器，存储通过接口单元，存储从一对RGB缓冲器提供的图形数据的图形缓冲器，存储从图形缓冲器中的一对RGB缓冲器提供的数据信号的切换块，以及转换数字R / G /的数字/模拟转换单元B数据存储在图形缓冲器中，以模拟信号输出。


FIG. 4