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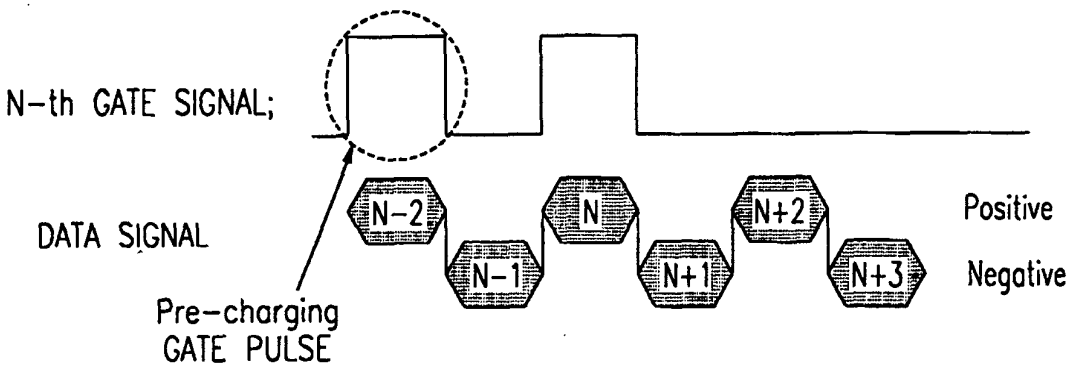
(54) Method and device for driving a LCD display

(57) Disclosed are an LCD capable of realizing a pre-charging method even in the random data-enable mode, and an apparatus and method for driving the same. In the LCD driving apparatus, a timing controller outputs a vertical sync start signal based on a data-enable signal having an irregular output interval to control the output of the image data. A gate driver sequentially applies both first and second gate-on voltages to a same gate line based on the vertical sync start signal. The first gate-on voltage is to drive a previous line being most adjacent to and having the same polarity as the current line, and the second gate-on voltage is to drive the current line. An LCD panel is firstly charged with the first gate-on voltage supplied from the gate driver, and secondly charged with the second gate-on voltage, so that it can display analog image data received from the data driver during the second charging.

FIG. 1



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Description

BACKGROUND OF THE INVENTION

(a) Field of the Invention

[0001] The present invention relates to a liquid crystal display and an apparatus and method for driving the same. More specifically, the present invention relates to a liquid crystal display capable of realizing a pre-charging method even in the random data-enable mode, and an apparatus and method for driving the same.

(b) Description of the Related Art

[0002] In general, a liquid crystal display (LCD) is a display device in which an electric field is applied to a liquid crystal layer having anisotropic dielectric constant permitivity sandwiched between two substrates, said electric field being adjusted to control the amount of light incident upon the substrates and thereby obtaining a desired image. Such LCDs, including a flat panel type display (FPD) that is very handy to carry, and a thin film transistor (TFT) LCD using a TFT as a switching element are, inter alia, widely used.

[0003] An increased resolution of the LCD has lead to a rapid reduction of the pixel charging time needed. Use is made of a pre-charging method as illustrated in FIG. 1 in order to compensate for the reduced charging time. The term "pre-charging method" as used herein refers to a method of charging a specific pixel over time that involves previously charging a corresponding pixel with data of an adjacent pixel having the same polarity as the corresponding pixel so as to invert the polarity of the pixel and thereafter charging the adjacent pixel with the data of the corresponding pixel.

[0004] A conventional gate signal usually appears every frame. However, as illustrated in FIG. 1, the typical pre-charging method compensates for the charging time in such a manner that an additional pre-charging gate pulse is used to previously charge the N-th pixel with the data of the (N-1)-th pixel having the same polarity as the N-th pixel prior to charging with the data of the N-th pixel.

[0005] More specifically, two vertical sync start signals STV have to be fed into the gate driver in order to generate a pre-charging gate pulse. For this purpose, use is made of a method of previously generating the vertical sync start signals STV at a designated position using a counter for a frame blank interval.

[0006] The data-enable (DE) mode makes the data-enable (DE) signal 'high' only during the interval having effective data, but no problem must arise in driving the LCD even with an irregular interval of the effective data. However, the conventional method using the counter is problematic in that it does not display an image when the interval of the effective data is irregular.

[0007] When the output interval of the effective data is irregular, i.e., in the random DE mode, the blank intervals of data-enable signals (for example, t1 and t2) are not conformable with each other with the consequence of a failure in obtaining a normal display of the LCD image.

SUMMARY OF THE INVENTION

[0008] It is an object of the present invention to solve the above problem and to provide an LCD capable of displaying all data even though a data-enable signal is randomly input.

[0009] It is another object of the present invention to provide an apparatus for driving the LCD.

[0010] It is further another object of the present invention to provide a method for driving the LCD.

[0011] In one aspect of the present invention, to achieve the first object, there is provided an LCD including: a timing controller for receiving external image data, and outputting a vertical sync start signal based on a data-enable signal having an irregular output interval to control the output of the image data, the vertical sync start signal having a generation interval associated with a blank interval of the data-enable signal; a data driver for converting the image data; a gate driver for sequentially applying both first and second gate-on voltages to a same gate line, wherein the first gate-on voltage is to drive a previous line being most adjacent to and having the same polarity as a current line, and the second gate-on voltage is to drive the current line; and an LCD panel being firstly charged with the first gate-on voltage supplied from the gate driver, and secondly charged with the second gate-on voltage, wherein the LCD panel displays the image data received from the data driver during the second charging.

[0012] In another aspect of the present invention, to achieve the second object, there is provided an apparatus for driving an LCD that includes an LCD panel having a plurality of data and gate lines, which charges a specific pixel by firstly charging the data of an adjacent pixel having the same polarity as the specific pixel to change the polarity of the corresponding pixel, and secondly by charging the data of the specific pixel, the LCD including: a timing controller for receiving external image data, and outputting a vertical sync start signal based on a data-enable signal having an irregular output interval to control the output of the image data, the vertical sync start signal having a generation interval associated with a blank interval of the data-enable signal; a data driver for converting the image data and outputting the converted image data to the data line of the LCD panel; and a gate driver for applying a first gate-on voltage to the gate line of the LCD panel to perform a first charging, and a second gate-on voltage to the gate line to perform a second charging, based on the vertical sync start signal, and controlling display of the converted image data supplied from the data driver during the second charging, wherein the first gate-on voltage is to drive a

previous line being most adjacent to and having the same polarity as the current line, and the second gate-on voltage is to drive the current line.

[0013] In still another aspect of the present invention to achieve the above and other objects, the timing controller preferably includes: an internal data-enable converter for receiving the data-enable signal having an irregular output interval, and outputting an internal data-enable signal shifted by a predetermined number of lines; a counter for counting the number of data-enable signals applied to the internal data-enable converter to output first and second switching signals; a control signal generator for receiving the internal data-enable signal shifted by the predetermined number of lines to output a control signal for driving the LCD panel; a first switch having one input path and a plurality of output paths, for determining the output path of the image data signal based on the first switching signal; a memory section having a plurality of memories for respectively storing image data received via the first switch, and outputting the stored image data as the image data of the next line is applied; and a second switch having a plurality of input paths and one output path, for determining the input path of the image data received from the memory section based on the second switching signal, and outputting the image data to the data driver.

[0014] In still another aspect of the present invention, to achieve the third object, there is provided a method for driving an LCD that includes an LCD panel having a plurality of data and gate lines, which charges a specific pixel by firstly charging the data of an adjacent pixel having the same polarity as the specific pixel to change the polarity of the corresponding pixel, and secondly by charging the data of the specific pixel, the method including: (a) receiving image data from an external image signal source and a data-enable signal for controlling output of the image data; (b) checking whether the data-enable signal has been received, sequentially recording the image data on a predetermined number of built-in memories upon receiving the data-enable signal, sequentially extracting the recorded image data, and generating an internal data-enable signal upon extraction of the image data to output a vertical sync start signal having a generation interval associated with a blank interval of the data-enable signal; (c) applying a voltage corresponding to the image data to the data lines; and (d) sequentially applying both first and second gate-on voltages based on the vertical sync start signal, wherein the first gate-on voltage is to drive a previous line being most adjacent to and having the same polarity as the current line, and the second gate-on voltage is to drive the current line.

[0015] Preferably, the data extraction based on the output of the vertical sync start signal in step (b) includes: (b-11) initializing a line count value and an internal flag; (b-12) checking whether the data-enable signal is present; (b-13) increasing the line count value by one and checking whether the updated line count value is greater than a first number of lines, which is the number of gate lines plus one, when the data-enable signal exists in step (b-12); (b-14) returning to step (b-12) when the updated line count value is equal to or less than the first number of lines, and generating a memory extraction flag signal to extract the data when the updated line count value is greater than the first number of lines; (b-15) checking whether the updated line count value is equal to the number of gate lines, and if not, returning to step (b-12); (b-16) generating an internal flag signal and increasing an internal flag count value by one, when the updated line count value is equal to the number of gate lines in step (b-15) or when the data-enable signal does not exist in step (b-12); and (b-17) comparing the updated interval flag count value with the first number of lines, ending the flow of the method when the internal flag count value is greater than the first number of lines, and returning to step (b-16) when the internal flag count value is equal to or less than the first number of lines.

[0016] Preferably, the data recording based on the output of the vertical sync start signal in step (b) includes: (b-21) initializing a line count value; (b-22) checking whether the data-enable signal is present, ending the flow of the method when the data-enable signal does not exist, and increasing the line count value by one when the data-enable signal exists; (b-23) generating a memory recording flag signal to record the data; and (b-24) checking whether the updated line count value in step (b-22) is equal to the number of vertically arranged gate lines, ending the flow of the method when the updated line count value is equal to the number of gate lines, and returning to step (b-22) when the updated line count value is not equal to the number of gate lines.

[0017] The LCD and the apparatus and method for driving the same use a built-in counter based on input data-enable signals to output an LCD control signal to a proper position in spite of the irregular positions of the input data-enable signals, which allows a normal display of all data in the presence of random inputs of the data-enable signals.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate an embodiment of the invention, and, together with the description, serve to explain the principles of the invention:

FIG. 1 is a waveform diagram illustrating a pre-charging gate pulse;

FIG. 2 is a waveform diagram illustrating the blank interval of a data-enable signal in the random DE mode;

FIG. 3 is a diagram illustrating an LCD using the pre-charging method in accordance with an embodiment of the present invention;

FIG. 4 is a detailed diagram of the timing controller shown in FIG. 3;

FIG. 5 is a waveform diagram illustrating a vertical sync start signal for pre-charging in the random DE mode in accordance with an embodiment of the present invention;

FIG. 6 is a flow chart illustrating generation of the vertical sync start signal when extracting data from a memory in accordance with an embodiment of the present invention; and

FIG. 7 is a flow chart illustrating generation of the vertical sync start signal when recording data in a memory in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0019] In the following detailed description, only the preferred embodiment of the invention has been shown and described, simply by way of illustration of the best mode contemplated by the inventor(s) of carrying out the invention. As will be realized, the invention is capable of modification in various obvious respects, all without departing from the invention. Accordingly, the drawings and description are to be regarded as illustrative in nature, and not restrictive.

[0020] FIG. 3 is a diagram illustrating an LCD using the pre-charging method in accordance with an embodiment of the present invention.

[0021] Referring to FIG. 3, the LCD using the pre-charging method in accordance with the embodiment of the present invention, comprises a timing controller 100, a data driver 200, a gate driver 300, and an LCD panel 400.

[0022] The timing controller 100 receives an RGB data signal DATA and a data-enable signal DE from an external graphic controller (not shown) and outputs to the data driver 200 the corresponding RGB data signal, a horizontal start signal STH for RGB data transmission, and a TP (or LOAD) signal for starting the output to a data driver IC after the completion of the RGB data transmission.

[0023] The timing controller 100, receiving the RGB data signal DATA and the data-enable signal DE from the external graphic controller (not shown), also outputs to the gate driver 300 a gate clock signal CPV for selection of the next gate line, a vertical sync start signal STV for selection of the first gate line, and an output enable signal OE for controlling the output of the gate drive IC.

[0024] In particular, the vertical sync start signal STV output from the timing controller 100 according to the present invention includes not only a gate pulse for substantially driving the gate lines but also a gate pulse for pixel data applied to a most adjacent gate line (e.g., the (N-2)'th gate line) having the same polarity as the current gate line (e.g., the N'th gate line), namely, a pre-charging gate pulse.

[0025] The data driver 200 comprises a plurality of data driver IC's to generate a plurality of data signals STH and TP for the LCD panel 400 based on a plurality of control signals received from the timing controller 100. The data driver 200, for example, latches the individual RGB data sequentially received in accord with the applied TP signal to change a dot-at-a-time scanning timing system to a line-at-a-time scanning system, and outputs a plurality of data signals D_1, D_2, ..., D_{m-1} and D_m to the data lines of the LCD panel 400.

[0026] The gate driver 300 comprises a plurality of gate driver IC's and sequentially applies a gate-on signal to gate lines based on the control signals CPV, STV and OE received from the timing controller 100, turning on the TFT.

[0027] In particular, since the vertical sync start signal STV output from the timing controller 100 according to the present invention includes a control signal to apply a gate pulse for pixel data to a most adjacent gate line having the same polarity as the current gate line, as well as a control signal to apply a gate pulse to the current gate line, the gate-on voltage output from the gate driver 300 includes two gate lines for every frame to perform a previous charging with a gate pulse of the most adjacent previous line and thereafter substantially drive the gate lines of the LCD panel with the gate pulse of the current line.

[0028] The most adjacent line may be the first, the second, or the third previous line, or the like, that has the same polarity as the current line.

[0029] The LCD panel 400 has a plurality of gate lines for transmission of a gate-on signal supplied from the gate driver 300, and a plurality of data lines for transmission of a data voltage from the data driver 200. The regions surrounded with the gate and data lines form the respective pixels, each of which includes a thin film transistor (TFT) (not shown) with gate and source electrodes connected to the gate and data lines, respectively, and pixel and storage capacitors (not shown) connected to the drain electrode of the TFT, thus displaying specific image information.

[0030] In particular, according to the present invention, the gate-on signal applied from the gate driver 300 has two gate pulses every frame to previously perform charging with the gate pulse of the most adjacent line having the same polarity as the data applied to the current gate line for driving the current frame and for displaying RGB image data applied from the data driver 200 for driving the current line.

[0031] FIG. 4 is a detailed diagram of the timing controller shown in FIG. 3, and FIG. 5 is a waveform diagram illustrating a vertical sync start signal for pre-charging in the random DE mode in accordance with an embodiment of the present invention.

[0032] Referring to FIG. 4, the timing controller 100 according to the embodiment of the present invention includes an internal DE converter 110, a counter 120, a control signal generator 130, a first switch 140, a first

memory 150, a second memory 160, a third memory 170, and a second switch 180.

[0033] The internal DE converter 110 receives a data-enable signal DE supplied from the graphic controller (not shown), more specifically a random DE signal, and outputs a two-line shifted internal data-enable signal DE' to the control signal generator 130. The output of the internal data-enable signal DE' is associated with the counting operation of the counter 120. The internal data-enable signal DE' is output in synchronization with the rising of the input DE from the third line of the random DE signal.

[0034] The counter 120 checks the input of the random DE signal applied to the internal DE converter 110, and when applying every frame, outputs a first switching signal to the internal DE converter 110 and the first switch 140 and a second switching signal associated with the first switching signal to the second switch 180.

[0035] The counter 120 further outputs the first switching signal to the internal DE converter 110 to control the output of the internal data-enable signal, and automatically generates the internal data-enable signal corresponding to the last two lines to compensate for the internal data-enable signal of the two missing lines.

[0036] The blank interval of the internal data-enable signal thus generated automatically may be the interval of a specific internal data-enable signal (for example, the internal data-enable signal copied in correspondence to the just previous line) or an interval that is usually defined.

[0037] The control signal generator 130 receives the two-line shifted internal enable signal DE' from the internal DE generator 110 and outputs control signals STH, TP, CPV, STV and OE for driving the LCD panel 400, to the data driver 200 and the gate driver 300.

[0038] In particular, the vertical sync start signal STV for realizing the pre-charging method according to an embodiment of the present invention applies a control signal to the gate driver 300 to output the gate pulse for the pixel data corresponding to the line prior to two lines from the current line as well as a control signal to output the gate pulse to the current line.

[0039] The first switch 140 comprises one port input terminal and three port output terminals and sequentially outputs the RGB image data signals applied from the graphic controller (not shown) to the first, second and third memories 150, 160 and 170 via any one of the three port output terminals in response to the first switching signal from the counter 120.

[0040] The first, second and third memories 150, 160 and 170 sequentially store the RGB image data received via the first switch 140 and output the stored RGB image data to the second switch 180 when the RGB image data of the next line are applied.

[0041] More specifically, in the case where the first, second and third memories 150, 160 and 170 comprise dual port memories that simultaneously perform read and write operations, the first, second and third image data are stored in the first, second and third memories 150, 160 and 170, respectively, and the first image data are output from the first memory 150 when the fourth image data are stored in the first memory 150.

[0042] On the other hand, in the case where the first, second and third memories 150, 160 and 170 comprise signal port memories that differently perform read and write operations, the first and third image data are stored in the first and second memories 150 and 160, respectively, and the first image data are output from the first memory 150 when the third image data are stored in the third memory 170.

[0043] The memory as used herein is a line memory capable of simultaneously applying RGB image data stored in every gate line.

[0044] The second switch 180 comprises three port input terminals and one port output terminal and sequentially outputs the RGB image data signals applied from the first, second and third memories 150, 160 and 170 to the data driver 200 in response to the second switching signal from the counter 120.

[0045] Now, a description will be given as to the generation algorithm of the vertical sync start signal STV for realizing the pre-charging method in the random DE mode according to the present invention as described above.

[0046] First, the three line memories 150, 160 and 170 are sequentially used to store RGB image data such that RGB image data for two lines (i.e., k-th and (k+1)-th lines) are stored in the first and second memories 150 and 160, respectively.

[0047] Sequentially, the data stored in the first memory 150 two lines prior are output to the data driver 200 while storing the RGB image data for the third line (i.e., (k+2)-th line) in the third line memory 170.

[0048] The internal DE signal DE' is generated in synchronization with the rising of the input DE signal from the third line of the input DE signal, because all LCD control signals STH, HCLK, OE and CPV are generated based on the DE signal and the internal DE signal DE' has to be generated after the two lines.

[0049] It is, however, impossible to generate the internal DE signals corresponding to the last two lines if the internal data-enable signal DE' is generated in such a way. To solve this problem, the counter 120 is used to determine which internal DE is generated for the current input data and to automatically generate an internal data-enable signal DE' corresponding to the last two lines. The blank width of the internal data-enable signal DE' is that of the normal data-enable signal.

[0050] Now, descriptions will be given as to a method for extracting data from a line memory and a method for recording data on the line memory based on the above-mentioned vertical sync start signal generating algorithm for realizing the pre-charging method in the random DE mode.

[0051] FIG. 6 is a flow chart illustrating generation of the vertical sync start signal when extracting data from

a line memory in accordance with an embodiment of the present invention.

[0052] Referring to FIG. 6, a line count value and an internal flag are first initialized at zero ('0'), in step s110. The internal flag is a signal used to form an extraction part of the memory in the interval destitute of a data-enable signal DE.

[0053] Subsequently, it is checked in step s120 whether the data-enable signal DE is present. If so, one ('1') is added to the line count value in step s130 and it is checked in step s140 whether the line count value is greater than the number of gate lines plus one, i.e., N+1. The number of gate lines represents an interval between the two vertical sync start signals STV.

[0054] If the line count value is not greater than N+1, the flow of the procedure returns to the routine of step s120. Otherwise, if the line value is greater than N+1, a memory extraction flag signal is generated to extract the data, in step s150.

[0055] It is then checked in step s160 whether the line count value is equal to the number of vertical lines. If not, the flow of the procedure returns to the routine of step s120.

[0056] If the line count value is equal to the number of vertical lines in step s160, or if there is no data-enable signal DE in step s120, the internal flag signal is generated and one ('1') is added to the internal flag count value, in step s170.

[0057] It is then checked in step s180 whether the internal flag count value is greater than the number of gate lines plus one, i.e., N+1. If not, the flow of the procedure goes to step s170; and otherwise, the flow ends.

[0058] FIG. 7 is a flow chart illustrating generation of the vertical sync start signal when recording data on a line memory in accordance with an embodiment of the present invention.

[0059] Referring to FIG. 7, a line count value is first initialized at zero ('0'), in step s210. It is then checked in step s220 whether a data-enable signal DE is present. If so, one ('1') is added to the line count value, in step s230, and a memory recording flag signal is generated to record the data, in step s240.

[0060] Subsequently, it is checked in step s250 whether the line count value is equal to the number of vertical lines. If not, the flow of the procedure goes to step s220; and otherwise, the flow ends.

[0061] As described above, even through the data-enable signal to control the output of the RGB image data in the LCD using the pre-charging method is randomly applied, the internal data-enable signal is generated in synchronization with the rising of the data-enable signal input after two lines for the input data-enable signal, so that the generation interval of the LCD control signals can be changed to produce a normal display of an image.

[0062] The internal data-enable signals corresponding to the last two lines are automatically generated using a built-in counter to compensate for the missing internal data-enable signals of the two lines. Preferably, the blank interval of the internal data-enable signals automatically generated is constant at all times.

[0063] While this invention has been described in connection with what is presently considered to be the most practical and preferred embodiment, it is to be understood that the invention is not limited to the disclosed embodiments, but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims.

[0064] As described above, the present invention uses a built-in counter based on input data-enable signals supplied from an external graphic controller so that an LCD control signal can be generated in spite of the irregular positions of the input data-enable signals. This allows a normal display of all data even though the data-enable signals are randomly input.

[0065] Where technical features mentioned in any claim are followed by reference signs, those reference signs have been included for the sole purpose of increasing the intelligibility of the claims and accordingly, such reference signs do not have any limiting effect on the scope of each element identified by way of example by such reference signs.

Claims

1. A liquid crystal display (LCD) comprising:

a timing controller for receiving external image data, and outputting a vertical sync start signal based on a data-enable signal having an irregular output interval to control the output of the image data, the vertical sync start signal having a generation interval associated with a blank interval of the data-enable signal;
a data driver for converting the image data and outputting the same;
a gate driver for sequentially applying both first and second gate-on voltages to a same gate line, wherein the first gate-on voltage is to drive a previous line being most adjacent to and having the same polarity as a current line, and the second gate-on voltage is to drive the current line; and
an LCD panel being firstly charged with the first gate-on voltage supplied from the gate driver, and secondly charged with the second gate-on voltage, wherein the LCD panel displays the image data received from the data driver during the second charging.

2. The LCD as claimed in claim 1, wherein the vertical sync start signal comprises a signal for generating the first gate-on voltage and a signal for generating the second gate-on voltage.

3. The LCD as claimed in claim 1, wherein the timing controller comprises:

an internal data-enable converter for receiving the data-enable signal having an irregular output interval, and outputting an internal data-enable signal after being shifted by a predetermined number of lines;
a counter for counting the number of data-enable signals applied to the internal data-enable converter to output first and second switching signals;
a control signal generator for receiving the internal data-enable signal shifted by the predetermined number of lines to output a control signal for driving the LCD panel;
a first switch having one input path and a plurality of output paths, for determining the output path of the image data signal based on the first switching signal;
a memory section having a plurality of memories for respectively storing image data received via the first switch, and outputting the stored image data when the image data of the next line is applied; and
a second switch having a plurality of input paths and one output path, for determining the input path of the image data received from the memory section based on the second switching signal, and outputting the image data to the data driver.

4. The LCD as claimed in claim 3, wherein the predetermined number of lines is at least one.

5. The LCD as claimed in claim 3, wherein the internal data-enable signal is generated in synchronization with the input data-enable signal shifted by a predetermined number of lines, the internal data-enable signal having the same polarity as the input data-enable signal.

6. The LCD as claimed in claim 3, wherein the memory comprises a line memory.

7. An apparatus for driving an LCD, which includes an LCD panel having a plurality of data and gate lines, and which charges a specific pixel by firstly charging the data of an adjacent pixel having the same polarity as the specific pixel to change the polarity of the corresponding pixel, and secondly, by charging the data of the specific pixel,

the LCD comprising:

a timing controller for receiving external image data, and outputting a vertical sync start signal based on a data-enable signal having an irregular output interval to control the output of the image data, the vertical sync start signal having a generation interval associated with a blank interval of the data-enable signal;
a data driver for converting the image data and outputting the converted image data to the data line of the LCD panel; and
a gate driver for applying a first gate-on voltage to the gate line of the LCD panel to perform a first charging, and a second gate-on voltage to the gate line to perform a second charging, based on the vertical sync start signal, and controlling display of the converted image data supplied from the data driver during the second charging, wherein the first gate-on voltage is to drive a previous line being most adjacent to and having the same polarity as the current line, and the second gate-on voltage is to drive the current line.

8. The apparatus as claimed in claim 7, wherein the vertical sync start signal comprises a signal for generating the first gate-on voltage and a signal for generating the second gate-on voltage.

9. The apparatus as claimed in claim 7, wherein the timing controller comprises:

an internal data-enable converter for receiving the data-enable signal having an irregular output interval, and outputting an internal data-enable signal shifted by a predetermined number of lines;
a counter for counting the number of data-enable signals applied to the internal data-enable converter to output first and second switching signals;
a control signal generator for receiving the internal data-enable signal shifted by the predetermined number of lines to output a control signal for driving the LCD panel;
a first switch having one input path and a plurality of output paths, for determining the output path of the image data signal based on the first switching signal;
a memory section having a plurality of memories for respectively storing image data received via the first switch, and outputting the stored image data as the image data of the next line is applied; and
a second switch having a plurality of input paths and one output path, for determining the input path of the image data received from the memory section based on the second switching signal, and outputting the image data to the data driver.

10. The apparatus as claimed in claim 9, wherein the predetermined number of lines is at least one.

11. The apparatus as claimed in claim 9, wherein the internal data-enable signal is generated in synchronization with the input data-enable signal shifted by a predetermined number of lines, the internal data-enable signal having the same polarity as the input data-enable signal.

12. The apparatus as claimed in claim 9, wherein the memory comprises a line memory.

13. A method for driving an LCD that includes an LCD panel having a plurality of data and gate lines, which charges a specific pixel by firstly charging the data of an adjacent pixel having the same polarity as the specific pixel to change the polarity of the corresponding pixel, and secondly by charging the data of the specific pixel,

the method comprising:

(a) receiving image data from an external image signal source and a data-enable signal for controlling output of the image data;
(b) checking whether the data-enable signal has been received, sequentially recording the image data on a predetermined number of built-in memories upon receiving the data-enable signal, sequentially extracting the recorded image data, and generating an internal data-enable signal upon extraction of the image data to output a vertical sync start signal having a generation interval associated with a blank interval of the data-enable signal;
(c) applying a voltage corresponding to the image data to the data lines; and
(d) sequentially applying both first and second gate-on voltages based on the vertical sync start signal, wherein the first gate-on voltage is to drive a previous line being most adjacent to and having the same polarity as the current line, and the second gate-on voltage is to drive the current line.

14. The method as claimed in claim 13, wherein the memories comprise a line memory.

15. The method as claimed in claim 13, wherein the vertical sync start signal comprises a signal for generating the first gate-on voltage and a signal for generating the second gate-on voltage.

16. The method as claimed in claim 13, wherein the predetermined number is at least one.

17. The method as claimed in claim 16, wherein the internal data-enable signal is generated in synchronization with the input data-enable signal shifted by a predetermined number of lines, the internal data-enable signal having the same polarity as the input data-enable signal.

18. The method as claimed in claim 13, wherein the output of the vertical sync start signal when extracting the data in step (b) comprises:

(b-11) initializing a line count value and an internal flag;
(b-12) checking whether the data-enable signal is present;
(b-13) increasing the line count value by one and checking whether the updated line count value is greater than a first number of lines, which is the number of gate lines plus one, when the data-enable signal exists in step (b-12);
(b-14) returning to step (b-12) when the updated line count value is equal to or less than the first number of lines, and generating a memory extraction flag signal to extract the data when the updated line count value is greater than the first number of lines;
(b-15) checking whether the updated line count value is equal to the number of gate lines, and if not, returning to step (b-12);
(b-16) generating an internal flag signal and increasing an internal flag count value by one, when the updated line count value is equal to the number of gate lines in step (b-15) or when the data-enable signal does not exist in step (b-12); and
(b-17) comparing the updated interval flag count value with the first number of lines, ending the flow of the method when the internal flag count value is greater than the first number of lines, and returning to step (b-16) when the internal flag count value is equal to or less than the first number of lines.

19. The method as claimed in claim 13, wherein the output of the vertical sync start signal when recording the data in step (b) comprises:

(b-21) initializing a line count value;
(b-22) checking whether the data-enable signal is present, ending the flow of the method when the data-enable signal does not exist, and increasing the line count value by one when the data-enable signal exists;
(b-23) generating a memory-recording flag signal to record the data; and
(b-24) checking whether the updated line count value in step (b-22) is equal to the number of vertically arranged gate lines, ending the flow of the method when the updated line count value is equal to the number of gate lines, and returning to step (b-22) when the updated line count value is not equal to the number of gate lines.

FIG. 1

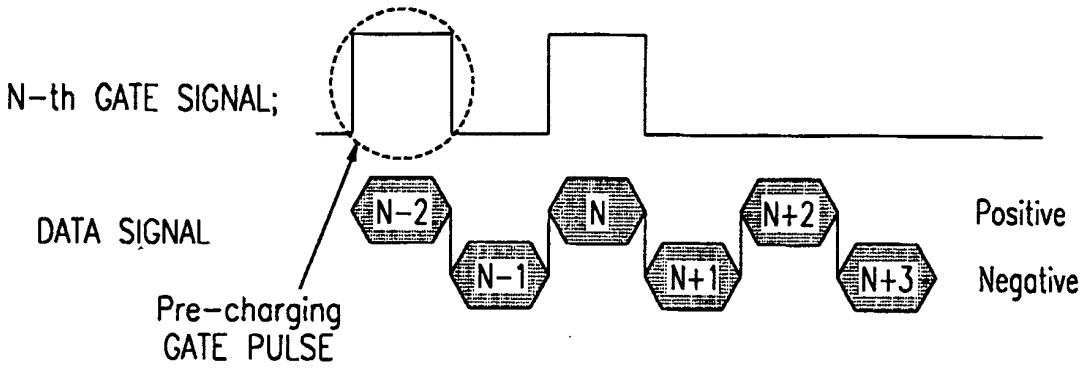

N-th GATE SIGNAL;
DATA SIGNAL
Pre-charging
GATE PULSE
N-2
N-1
N
N+1
N+2
N+3
Positive
Negative

FIG. 2

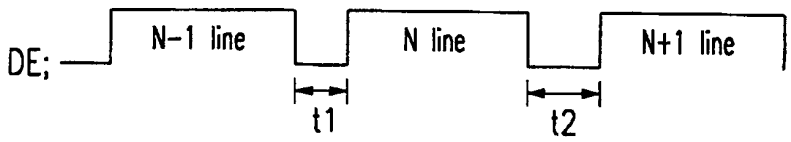

DE;
N-1 line
N line
N+1 line
t1
t2

FIG. 3

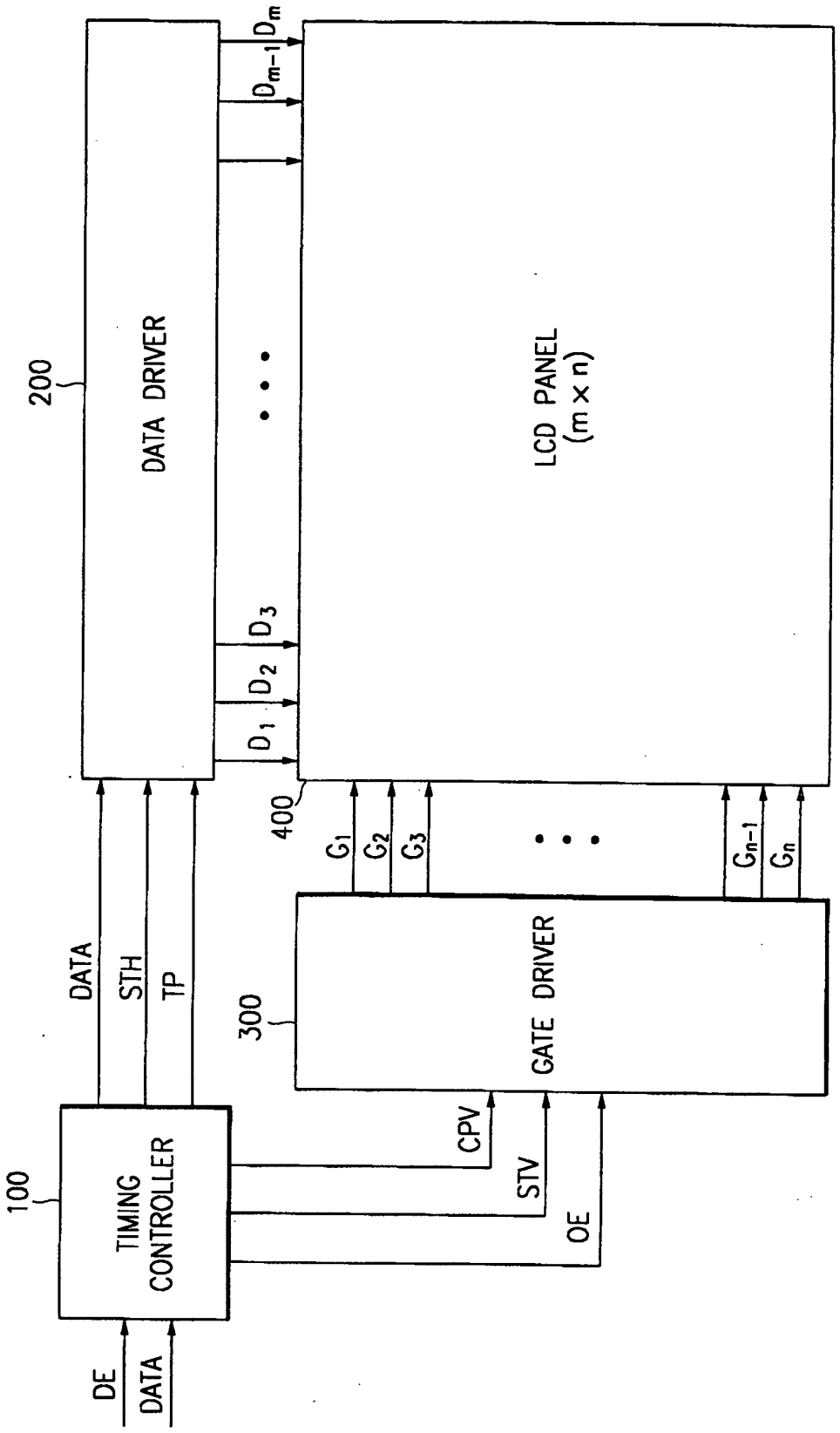

DE
DATA
100
TIMING CONTROLLER
DATA
STH
TP
200
DATA DRIVER
D_1
D_2
D_3
D_{m-1}
D_m
400
LCD PANEL
(m x n)
300
GATE DRIVER
CPV
STV
OE
G_1
G_2
G_3
G_{n-1}
G_n

FIG. 4

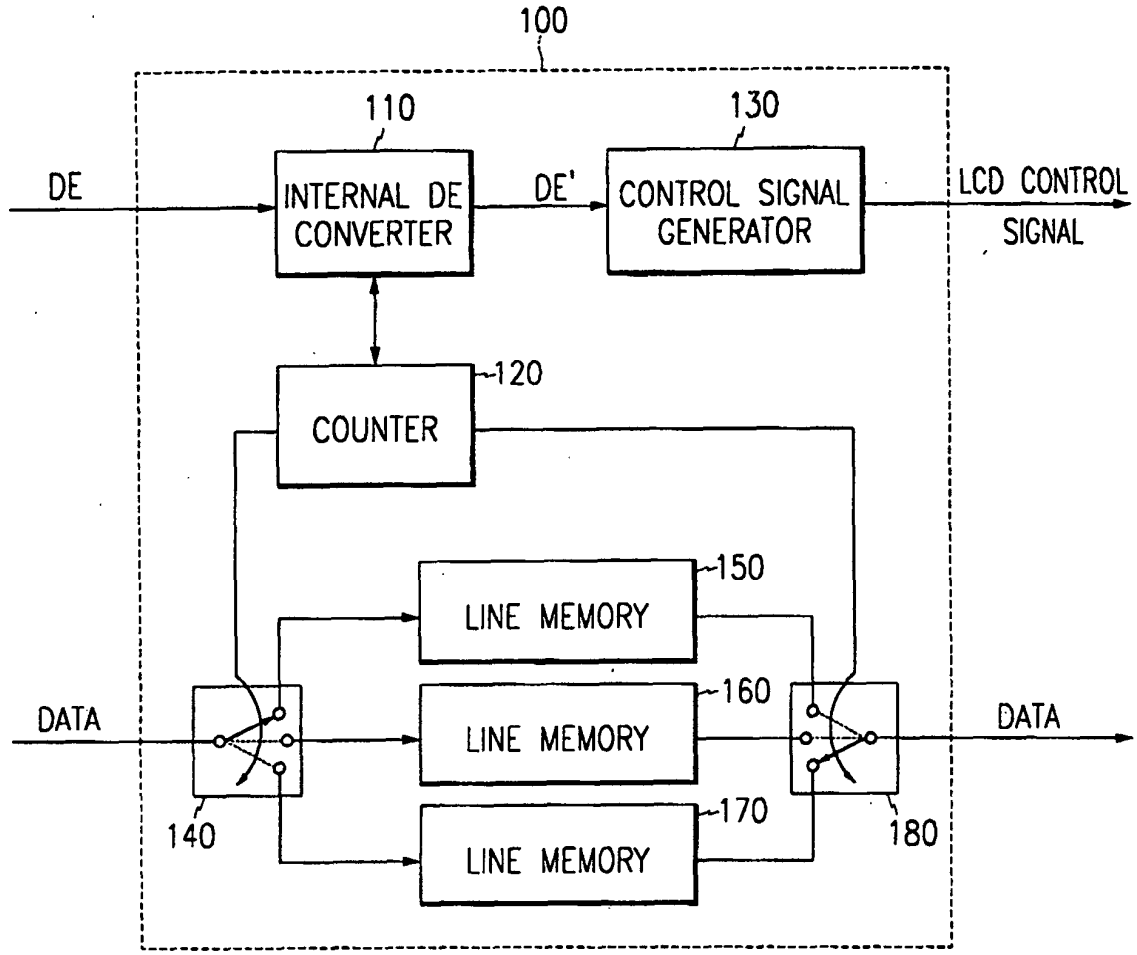

100
110
130
DE
INTERNAL DE CONVERTER
DE'
CONTROL SIGNAL GENERATOR
LCD CONTROL SIGNAL
120
COUNTER
150
LINE MEMORY
160
LINE MEMORY
170
LINE MEMORY
DATA
DATA
140
180

FIG. 5

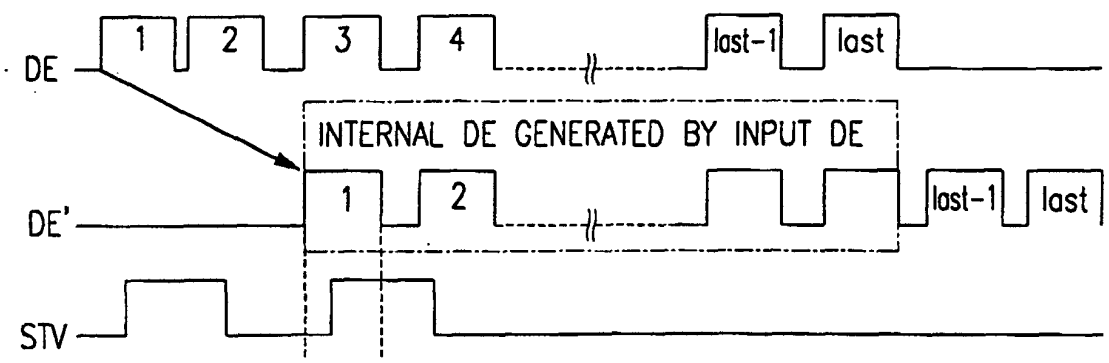

DE
1
2
3
4
last-1
last
INTERNAL DE GENERATED BY INPUT DE
DE'
1
2
last-1
last
STV

FIG. 6

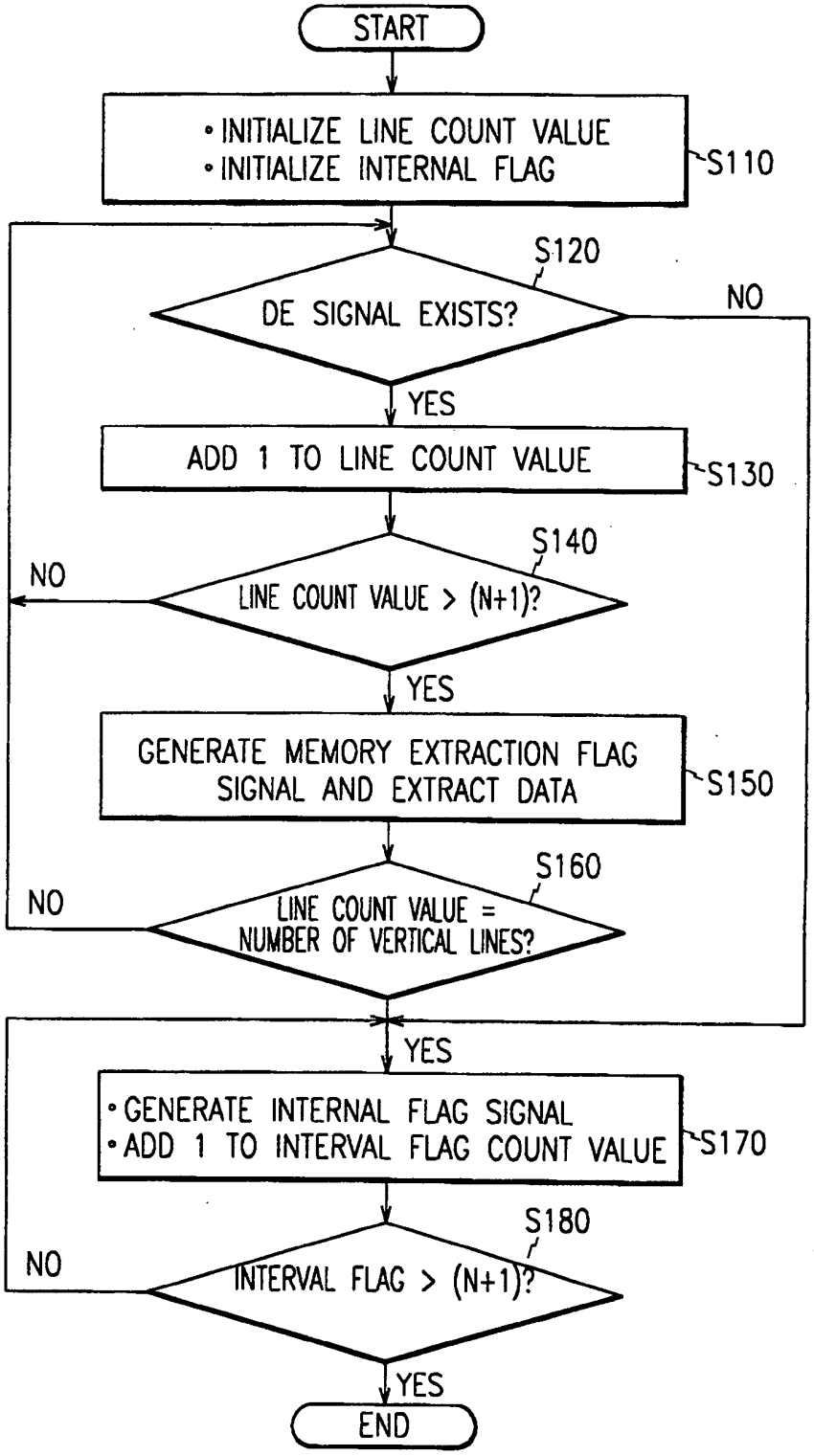
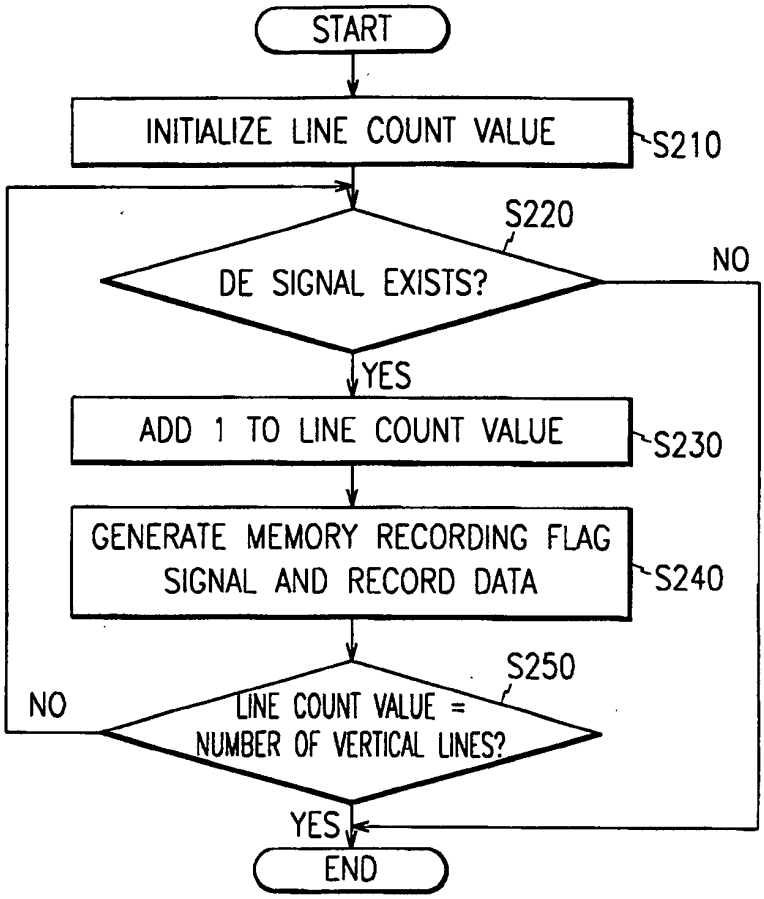

START
• INITIALIZE LINE COUNT VALUE
• INITIALIZE INTERNAL FLAG
S110
S120
DE SIGNAL EXISTS?
NO
YES
ADD 1 TO LINE COUNT VALUE
S130
S140
NO
LINE COUNT VALUE > (N+1)?
YES
GENERATE MEMORY EXTRACTION FLAG SIGNAL AND EXTRACT DATA
S150
S160
NO
LINE COUNT VALUE = NUMBER OF VERTICAL LINES?
YES
• GENERATE INTERNAL FLAG SIGNAL
• ADD 1 TO INTERVAL FLAG COUNT VALUE
S170
S180
NO
INTERVAL FLAG > (N+1)?
YES
END

FIG. 7


START
INITIALIZE LINE COUNT VALUE
S210
S220
DE SIGNAL EXISTS?
NO
YES
ADD 1 TO LINE COUNT VALUE
S230
GENERATE MEMORY RECORDING FLAG SIGNAL AND RECORD DATA
S240
S250
NO
LINE COUNT VALUE = NUMBER OF VERTICAL LINES?
YES
END

专利名称(译)	用于驱动LCD显示器的方法和设备		
公开(公告)号	EP1233400A2	公开(公告)日	2002-08-21
申请号	EP2002002092	申请日	2002-02-12
[标]申请(专利权)人(译)	三星电子株式会社		
申请(专利权)人(译)	SAMSUNG ELECTRONICS CO.，LTD.		
当前申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
[标]发明人	LEE SEUNG WOO CHEON MAN BOK KWON SU HYUN		
发明人	LEE, SEUNG-WOO CHEON, MAN-BOK KWON, SU-HYUN		
IPC分类号	G02F1/133 G09G3/36 G09G3/20 G09G5/12		
CPC分类号	G09G3/3677 G09G2310/0251 G09G2320/0252 G09G2340/16		
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其他公开文献	EP1233400B1 EP1233400A3		
外部链接	Espacenet		

摘要(译)

公开了一种即使在随机数据使能模式下也能够实现预充电方法的LCD，以及用于驱动该方法的装置和方法。在LCD驱动装置中，定时控制器基于具有不规则输出间隔的数据使能信号输出垂直同步开始信号，以控制图像数据的输出。栅极驱动器基于垂直同步开始信号顺序地将第一和第二栅极导通电压施加到同一栅极线。第一栅极导通电压用于驱动与电流线最接近并具有相同极性的前一条线，并且第二栅极导通电压用于驱动电流线。 LCD面板首先用从栅极驱动器提供的第一栅极导通电压充电，然后用第二栅极导通电压充电，以便它可以在第二次充电期间显示从数据驱动器接收的模拟图像数据。