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(54) Liquid crystal display and manufacturing method thereof

Flüssigkristallanzeige und Herstellungsverfahren dafür

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Description

BACKGROUND

(a) Technical Field

[0001] The present invention is related to a liquid crystal display (i.e., liquid crystal display device) and a manufacturing method thereof.

(b) Description of the Related Art

[0002] A liquid crystal display typically includes two panels with field generating electrodes (such as a pixel electrode and a common electrode) and a liquid crystal layer interposed between the panels.

[0003] The liquid crystal display may generate an electric field in the liquid crystal layer by applying voltage to the field generating electrodes. The electric field may determine the direction of liquid crystal molecules of the liquid crystal layer, thereby controlling polarization of incident light so as to control displayed images.

[0004] A liquid crystal display manufacturing process may include the following steps: forming a sacrificial layer with a photoresist, removing the sacrificial layer by an etching process after coating a support member thereon, and filling liquid crystal through an injection hole into an empty space that is resulted from removing the sacrificial layer. Typically, a height of the empty space is not large. If the liquid crystal injection hole is partially blocked by another constituent element formed below the empty space, the liquid crystal injection may be substantially difficult and time-consuming.

[0005] The above information disclosed in this Background section is for enhancement of understanding of the background of the invention. A Liquid crystal display device as specified in the preamble of claim 1 is known from EP 0 294 900.

SUMMARY

[0006] Embodiments of the present invention may enable efficient formation of a liquid crystal layer in manufacturing a liquid crystal display device, thereby minimizing the manufacturing time and/or minimizing the manufacturing cost. Embodiments of the present invention may effectively seal liquid crystal material in liquid crystal display devices to ensure optimal performance of the liquid crystal display devices.

[0007] The present invention is related to a liquid crystal display device as defined in claim 1.

[0008] The first light-blocking element may be formed after the formation of the liquid crystal layer; therefore, the first light-blocking element may not obstruct the formation of the liquid crystal layer. Advantageously, the liquid crystal layer may be efficiently formed, and therefore the manufacturing time and/or the manufacturing cost of the liquid crystal display device may be minimized. The first light-blocking element may prevent light leakage and may seal the liquid crystal injection hole to prevent liquid crystal leakage. Advantageously, the performance of the liquid crystal display device may be optimized.

[0009] In one or more embodiments, the liquid crystal display device may include a transistor electrically connected to the pixel electrode. The liquid crystal display device may further include a gate line electrically connected to the transistor and configured to transmit a gate signal to the transistor. The first light-blocking element extends parallel to the gate line and overlaps the transistor.

[0010] In one or more embodiments, the first light-blocking element is disposed between a first portion of the liquid crystal layer and a second portion of the liquid crystal layer.

[0011] In one or more embodiments, a portion of the liquid crystal layer is disposed between the first light-blocking element and the substrate.

[0012] In one or more embodiments, the first light-blocking element directly contacts the liquid crystal layer.

[0013] In one or more embodiments, the liquid crystal display device may include a capping layer that is made of a material (e.g., a transparent material) different from a material of the first light-blocking element. A first portion of the capping layer is disposed inside the liquid crystal injection hole and is disposed between the first light-blocking element and the liquid crystal layer.

[0014] In one or more embodiments, the first light-blocking element is disposed between a second portion of the capping layer and a third portion of the capping layer.

[0015] In one or more embodiments, the second portion of the capping layer and the third portion of the capping layer are disposed between a first portion of the common electrode and a second portion of the common electrode.

[0016] In one or more embodiments, the liquid crystal display device may include a second light-blocking element. The second light-blocking element is directly connected to the first light-blocking element and extending substantially perpendicular to the first light-blocking element.

[0017] In one or more embodiments, the liquid crystal display device may include a second light-blocking element.

The first light-blocking element is disposed at a first side with respect to the liquid crystal layer. The second light-blocking element is disposed at a second side with respect to the liquid crystal layer and extends substantially perpendicular to the first light-blocking element in a plan view of the liquid crystal display device.

[0018] The present invention is further related to a method for manufacturing a liquid crystal display device as defined in claim 11.

[0019] Since the first light-blocking element is provided after the liquid crystal has been injected, the first light-blocking element may not obstruct the injection of the liquid crystal. Advantageously, the liquid crystal layer may be efficiently formed, and therefore the manufacturing time and/or the manufacturing cost of the liquid crystal display device may be minimized. The first light-blocking element may prevent light leakage and may seal the liquid crystal injection hole to prevent liquid crystal leakage. Advantageously, the performance of the liquid crystal display device may be optimized.

[0020] In one or more embodiments the method may include the following steps: providing a photoresist pattern that partially overlaps the common electrode; using the photoresist pattern as a mask in the forming the liquid crystal injection hole; and removing the photoresist pattern when performing the removing the sacrificial layer.

[0021] In one or more embodiments the method may include the following steps: providing a transistor that is electrically connected to the pixel electrode; and providing a gate line that is electrically connected to the transistor and is configured to transmit a gate signal to the transistor, wherein the first light-blocking element extends parallel to the gate line and overlaps the transistor.

[0022] In one or more embodiments the method may include the following step: disposing the first light-blocking element between a first portion of the liquid crystal layer and a second portion of the liquid crystal layer.

[0023] In one or more embodiments the method may include the following step: disposing the first light-blocking element such that a portion of the liquid crystal layer is disposed between the first light-blocking element and the substrate.

[0024] In one or more embodiments the method may include the following step: disposing the first light-blocking element such that the first light-blocking element directly contacts the liquid crystal layer.

[0025] In one or more embodiments the method may include the following steps: forming a capping layer using a material that is different from a material of the first light-blocking element; disposing a first portion of the capping layer inside the liquid crystal injection hole; and disposing the first light-blocking element such that the first portion of the capping layer is disposed between the first light-blocking element and the liquid crystal layer.

[0026] In one or more embodiments the method may include the following step: disposing the first light-blocking element such that the first light-blocking element is disposed between a second portion of the capping layer and a third portion of the capping layer.

[0027] In one or more embodiments the method may include the following step:

forming a second light-blocking element when forming the first light-blocking element, the second light-blocking element being directly connected to the first light-blocking element and extending substantially perpendicular to the first light-blocking element.

[0028] In one or more embodiments the method may include the following step: forming a second light-blocking element before the forming the liquid crystal layer, wherein the first light-blocking element is disposed at a first side with respect to the liquid crystal layer, and wherein the second light-blocking element is disposed at a second side with respect to the liquid crystal layer and extends substantially perpendicular to the first light-blocking element in a plan view of the liquid crystal display device.

[0029] Advantageously, the time required for the liquid crystal injection may be minimized, and the liquid crystal material may sufficiently fill the microcavity. In one or more embodiments, the photoresist and the sacrificial layer may be removed in a same process step. Advantageously, manufacturing may be simplified, and manufacturing time and/or manufacturing cost may be saved.

BRIEF DESCRIPTION OF THE DRAWINGS

[0030]

FIG. 1 is a plan view illustrating a liquid crystal display according to one or more embodiments of the present invention.
FIG. 2 is a cross-sectional view taken along line II-II indicated in FIG. 1.
FIG. 3 is a cross-sectional view taken along line III-III indicated in FIG. 1.
FIGS. 4, 5, and 6 are diagrams sequentially illustrating a manufacturing method of the liquid crystal display of FIG. 1 according to one or more embodiments of the present invention.
FIG. 7 is a cross-sectional view illustrating a liquid crystal display according to one or more embodiments of the present invention.
FIGS. 8, 9, 10, and 11 are diagrams sequentially illustrating a manufacturing method of the liquid crystal display of

FIG. 7 according to one or more embodiments of the present invention.

FIGS. 12 and 13 are cross-sectional views illustrating a liquid crystal display according to one or more embodiments of the present invention.

FIG. 14 is a plan view illustrating positions of a first black matrix and a second black matrix in the liquid crystal display of FIGS. 12 and 13 according to one or more embodiments of the present invention.

DETAILED DESCRIPTION OF EMBODIMENTS

[0031] Embodiments of the present invention will be described more fully hereinafter with reference to the accompanying drawings. As those skilled in the art would realize, the described embodiments may be modified in various ways, all without departing from the scope of the present invention as defined in the claims.

[0032] In the drawings, the thickness of layers, films, panels, regions, etc., may be exaggerated for clarity. Like reference numerals may designate like elements in the specification. It will be understood that when an element such as a layer, film, region, or substrate is referred to as being "on" another element, it can be directly on the other element, or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements present (except environmental elements such as air).

[0033] Although the terms first, second, etc. may be used herein to describe various signals, elements, components, regions, layers, and/or sections, these signals, elements, components, regions, layers, and/or sections should not be limited by these terms. These terms may be used to distinguish one signal, element, component, region, layer, or section from another signal, region, layer or section. Thus, a first signal, element, component, region, layer, or section discussed below may be termed a second signal, element, component, region, layer, or section without departing from the teachings of the present invention. The description of an element as a "first" element may not require or imply the presence of a second element or other elements. The terms first, second, etc. may also be used herein to differentiate different categories of elements. For conciseness, the terms first, second, etc. may represent first-type (or first-category), second-type (or second-category), etc., respectively.

[0034] Hereinafter, a liquid crystal display (i.e., a liquid crystal display device) according to one or more embodiments of the present invention will be described in detail with reference to FIGS. 1 to 3.

[0035] FIG. 1 is a plan view illustrating a liquid crystal display according to one or more embodiments of the present invention, FIG. 2 is a cross-sectional view taken along line II-II indicated in FIG. 1, and FIG. 3 is a cross-sectional view taken along line III-III indicated in FIG. 1.

[0036] In the liquid crystal display, gate line 121 (for transmitting a gate signal) and a storage voltage line 131 are formed on an insulation substrate 110 made of transparent glass, transparent plastic, or a different transparent substrate material. The gate line 121 includes a first gate electrode 124a, a second gate electrode 124b, and a third gate electrode 124c. The storage voltage line 131 includes storage electrodes 135a and 135b and a protrusion 134 protruding in the gate line 121 direction (i.e., the horizontal direction). The storage electrodes 135a and 135b may form a structure that surrounds a first subpixel electrode 192h and a second subpixel electrode 1921 of a front pixel. A horizontal portion of the storage electrode 135b may be one wiring which is not separated from the horizontal portion of the front pixel.

[0037] A gate insulating layer 140 is formed on the gate line 121 and the storage voltage line 131. A semiconductor 151 positioned below a data line 171 (for transmitting image signals), portions of a semiconductor 155 positioned below one or more drain electrodes (e.g., a drain electrode 175b), and a semiconductor 154 positioned at a channel part of a thin film transistor are formed on the gate insulating layer 140.

[0038] A plurality of ohmic contacts may be respectively formed on the semiconductors 151, 154, and 155 and between the data line 171 and the one or more source electrodes and/or the one or more drain electrodes, the ohmic contacts being omitted in the drawings.

[0039] On the semiconductors 151, 154, and 155 and the gate insulating layer 140, a set of data conductors that includes a plurality of data lines 171 including a first source electrode 173a and a second source electrode 173b, a first drain electrode 175a, a second drain electrode 175b, a third source electrode 173c, and a third drain electrode 175c is formed.

[0040] The first gate electrode 124a, the first source electrode 173a, and the first drain electrode 175a form a first thin film transistor together with the semiconductor 154, and a channel of the thin film transistor is formed at the semiconductor portion 154 between the first source electrode 173a and the first drain electrode 175a. Analogously, the second gate electrode 124b, the second source electrode 173b, and the second drain electrode 175b form a second thin film transistor together with the semiconductor 154, and a channel of the thin film transistor is formed at the semiconductor portion 154 between the second source electrode 173b and the second drain electrode 175b. The third gate electrode 124c, the third source electrode 173c, and the third drain electrode 175c form a third thin film transistor together with the semiconductor 154, and a channel of the thin film transistor is formed at the semiconductor portion 154 between the third source electrode 173c and the third drain electrode 175c.

[0041] The data line 171 may have a structure with a narrow width in a thin film transistor formation region around (or near) an extension 175c' of the third drain electrode 175c. This structure is for keeping a distance from the adjacent wiring and reducing signal interference. In one or more embodiments, the structure may not be required.

[0042] A first passivation layer 180 is formed on the data conductors 171, 173c, 175a, 175b, and 175c and the exposed semiconductor 154 portion. The first passivation layer 180 may include an inorganic insulator, such as at least one of silicon nitride (SiNx) and silicon oxide (SiOx), or an organic insulator.

[0043] A color filter 230 is formed on the first passivation layer 180. The color filter 230 having the same color is formed in adjacent pixels in a vertical direction (i.e., the data line direction). Adjacent pixels in a horizontal direction (i.e., the gate line direction) have color filters 230 and 230' having different colors, and two color filters 230 and 230' may be substantially simultaneously formed and may overlap each other over the data line 171. Each of the color filters 230 and 230' may display one color of a set of primary colors, such as a set of three primary colors of red, green, and blue. In one or more embodiments, each of the color filters 230 and 230' may display one color of cyan, magenta, yellow, and white-based colors.

[0044] A first black matrix 220, i.e., a black matrix portion or light-blocking portion which is defined as the second light-blocking element in the claims, overlapping and/or covering a data line, is formed on the color filters 230 and 230' and overlaps at least a portion of each of the color filters 230 and 230'. The first black matrix 220 is made of a non-transmissive material for blocking light. The first black matrix 220 is formed based on a region where the data line 171 is formed to extend in a vertical direction and is not formed in a 'transistor formation regions', a region where the gate line 121, the storage voltage line 131, and one or more thin film transistors are formed, such that the first black matrix 220 may not overlap the gate line 121, the storage voltage line 131, or the one or more thin film transistors. A black matrix 225 may overlap the transistor formation region and may block light in the transistor formation region. The second black matrix 225, i.e., a black matrix disposed in a liquid crystal injection hole 335 and being defined as the first light-blocking element in the claims, is formed after liquid crystal molecules have been injected in a microcavity (e.g., microcavity 305 illustrated in FIG. 5). This will be described below.

[0045] A second passivation layer 185 may cover the color filter 230 and the black matrix 220 and may be formed on the color filter 230 and the black matrix 220. The second passivation layer 185 may contain an inorganic insulator, such as at least one of silicon nitride (SiNx) and silicon oxide (SiOx), or an organic insulator. As illustrated in cross-sectional views of FIGS. 2 and 3, in the case where a step occurs due to a thickness difference and/or thickness variation associated with the color filter 230 and/or the black matrix 220, the second passivation layer 185 may reduce or compensate the thickness difference and/or the thickness variation; the second passivation layer 185 may server as a planarization layer disposed over the color filter 230 and the black matrix 220.

[0046] A first contact hole 186a and a second contact hole 186b, which expose the first drain electrode 175a and an extension 175b' of the second drain electrode 175b, respectively, are formed in (and/or are formed through) one or more of the color filter 230, the first black matrix 220, and the passivation layers 180 and 185. A third contact hole 186c, which exposes a protrusion 134 of the storage voltage line 131 and the extension 175c' of the third drain electrode 175c, is formed in (and/or is formed through) on or more of the color filter 230, the first black matrix 220, and the passivation layers 180 and 185.

[0047] In one or more embodiments, the contact holes 186a, 186b, and 186c are formed in (and/or are formed through) the first black matrix 220 and the color filter 230, even if etching the first black matrix 220 and the color filter 230 may be more difficult than etching the passivation layers 180 and 185 because of material properties. In one or more embodiments, the material used for forming the first black matrix 220 or the color filter 230 may not be formed at positions corresponding to the contact holes 186a, 186b, and 186c before etching of the black matrix 220 or the color filter 230.

[0048] In one or more embodiments, the color filter 230 and the passivation layers 180 and 185 may be etched, and a position of the first black matrix 220 may be changed, in order to form the contact holes 186a, 186b, and 186c.

[0049] On the second passivation layer 185, a pixel electrode 192 including the first subpixel electrode 192h and the second subpixel electrode 1921 is formed. The pixel electrode 192 may be made of a transparent conductive material, such as ITO or IZO.

[0050] The first subpixel electrode 192h and the second subpixel electrode 1921 are adjacent to each other in a column direction. Each of the first subpixel electrode 192h and the second subpixel electrode 1921 may have an overall quadrangular shape and may include a cross stem structure having a horizontal stem and a vertical stem crossing the horizontal stem. Each of the first subpixel electrode 192h and the second subpixel electrode 1921 may be divided into four subregions by the horizontal stem and the vertical stem, and each subregion may include a plurality of minute branches.

[0051] The minute branches of the first subpixel electrode 192h and the second subpixel electrode 1921 form an angle in a range of approximately 40 to 45 degrees with the gate line 121 or the horizontal stem. The minute branches of two adjacent subregions may be perpendicular to each other. A width of the minute branch may be gradually increased. Distances between the minute branches may be different from each other.

[0052] The first subpixel electrode 192h and the second subpixel electrode 1921 are physically and electrically connected with the first drain electrode 175a and the second drain electrode 175b through the contact holes 186a and 186b and receive data voltage from the first drain electrode 175a and the second drain electrode 175b.

[0053] A connecting member 194 electrically connects the extension 175c' of the third drain electrode 175c and the protrusion 134 of the storage voltage line 131 through the third contact hole 186c. As a result, a part of the data voltage applied to the second drain electrode 175b is divided through the third source electrode 173c, and a magnitude of the voltage applied to the second subpixel electrode 1921 may be smaller than a magnitude of the voltage applied to the first subpixel electrode 192h.

[0054] An area of the second subpixel electrode 1921 may be in a range of 1 to 2 times an area of the first subpixel electrode 192h.

[0055] An opening for collecting gas discharged from the color filter 230 and a cover for covering the opening may be formed in the second passivation layer 185. The cover may be formed of the same material as the pixel electrode 192. The opening and the cover may prevent gas discharged from the color filter 230 from being transferred to other elements. In one or more embodiments, the opening and the cover may not be required.

[0056] A microcavity 305 (see FIG. 5) is positioned on the second passivation layer 185 and the pixel electrode 192 (and is positioned between the second passivation layer 185 and a common electrode 270), and the liquid crystal layer 3 is formed in the microcavity. An alignment layer (not illustrated) may be formed between the second passivation layer 185 and the liquid crystal layer 3 in order to align the liquid crystal molecules injected in the microcavity 305. The alignment layer may contain at least one of polyamic acid, polysiloxane, and polyimide, which are generally used in a liquid crystal alignment layer.

[0057] The liquid crystal layer 3 is formed in the microcavity 305 (and on the alignment layer). The liquid crystal molecules 310 are initially aligned by the alignment layer and the alignment direction is changed according to the applied electric field. A height of the liquid crystal layer 3 corresponds to a height of the microcavity 305. A thickness of the liquid crystal layer 3 may be in a range of 2.0 μm to 3.6 μm.

[0058] The liquid crystal material for forming the liquid crystal layer 3 may be injected into the microcavity 305 using capillary force in a liquid crystal injection hole 335. The alignment layer may be formed using capillary force.

[0059] The common electrode 270 is positioned above the microcavity 305 and the liquid crystal layer 3 with the microcavity 305 and the liquid crystal layer 3 being disposed between the common electrode 270 and the second passivation layer 185. The common electrode 270 may have a curved structure including a protrusion portion (illustrated in FIG. 2) that is disposed above a data line 171 and protrudes (and is convex) toward the data line 171. At least a portion of the first black matrix 220 may be disposed between the protrusion portion and the data line 171. The protrusion portion may directly contact the second passivation layer 185. A portion of the roof material 312 and a portion of the lower insulating layer 311 may be disposed inside a recess structure of the protrusion portion. The common electrode 270 is not formed in the liquid crystal injection hole 335 portion (which corresponds to the transistor formation region); the liquid crystal injection hole 335 may be disposed between two portions of the common electrode 270, as illustrated in FIG. 3. The common electrode 270 may extend in a gate line direction (i.e., the horizontal direction).

[0060] The common electrode 270 is made of a transparent conductive material, such as ITO or IZO, and serves to generate an electric field together with the pixel electrode 192 to control an alignment direction of the liquid crystal molecules.

[0061] A lower insulating layer 311 is positioned on the common electrode 270. The lower insulating layer 311 may contain an inorganic insulating material, such as silicon nitride (SiNx).

[0062] A roof layer 312 is formed on the lower insulating layer 311. The roof layer 312 may serve to support a space (microcavity 305) to be formed between the pixel electrode 192 and the common electrode 270. The roof layer 312 according to one or more embodiments serves to support the microcavity 305 above the common electrode 270 at a predetermined thickness.

[0063] An upper insulating layer 313 is formed on the roof layer 312. The upper insulating layer 313 may contain an inorganic insulating material, such as silicon nitride (SiNx).

[0064] The liquid crystal injection hole 335 may be formed through the lower insulating layer 311, the roof layer 312, and the upper insulating layer 313 in the transistor formation region, wherein a liquid crystal may be injected through the liquid crystal injection hole 335 into the microcavity 305. The liquid crystal injection hole 335 may be used for removing the sacrificial layer 300 of FIG. 4 in the process of forming the microcavity 305.

[0065] The lower insulating layer 311 and the upper insulating layer 313 may be laminated with portions disposed in the transistor formation region corresponding to a position for forming the liquid crystal injection hole 335. In one or more embodiments, the roof layer 312 may not be formed in the transistor formation region; therefore, the liquid crystal injection hole 335 may be formed by removing portions of the lower insulating layer 311 and upper insulating layer 313 in the transistor formation region without removing portions of the roof layer 312. The sacrificial layer 300 may be exposed through the liquid crystal injection hole 335 after a portion of the common electrode 270 that is positioned in the transistor formation region has been removed.

[0066] In one or more embodiments, the roof layer 312, the upper insulating layer 313, and the lower insulating layer 311 are etched in a same etching process in the transistor formation region to form the liquid crystal injection hole 335.

[0067] In one or more embodiments, the lower insulating layer 311 and the upper insulating layer 313 may not be required.

[0068] A second black matrix 225, i.e., a black matrix portion or light-blocking portion for covering the transistor formation region, is formed in the transistor formation region and is formed inside the liquid crystal injection hole 335. The second black matrix 225 is formed of a non-transmissive material for blocking light. In one or more embodiments of the present invention, the second black matrix 225 is formed by injecting the material using an inkjet method. According to the invention, at least a portion of the second black matrix 225 is positioned inside the liquid crystal injection hole 335. In one or more embodiments, a part of the second black matrix 225 may be positioned outside the liquid crystal injection hole 335. Since the second black matrix 225 covers the transistor formation region, light passing through the transistor formation region is blocked, and thus the transistor formation region is not recognized by a viewer of the liquid crystal display. The second black matrix 225 may seal (and/or cap) the liquid crystal injection hole 335 so that the liquid crystal layer 3 may not leak through the liquid crystal injection hole 335 after the liquid crystal layer 3 has been injected through the liquid crystal injection hole 335 into the microcavity 305.

[0069] In one or more embodiments, as illustrated in FIG. 3, a portion of the liquid crystal layer 3 may be disposed between the second passivation layer 185 and the second black matrix 225. In one or more embodiments, the second black matrix 225 may directly contact the second passivation layer 185 and thus may separate a first portion of the liquid crystal layer 3 from a second portion of the liquid crystal layer 3.

[0070] The second black matrix 225 extends in a horizontal direction along the transistor formation region.

[0071] As illustrated in the plan view of FIG. 1, the first black matrix 220 (which include portions extending in the vertical direction) and the second black matrix 225 (which include portions extending in the horizontal direction) may form a lattice structure having openings. A substantial portion of the pixel electrode 192, a substantial portion of the color filter 230, and a substantial portion of the liquid crystal layer 3 may be positioned at one or more corresponding openings.

[0072] A lower polarizer (not illustrated) may be positioned below the insulation substrate 110, and an upper polarizer may be positioned above the upper insulating layer 313. Each of the polarizers may include a polarized element for generating polarization and a tri-acetyl-cellulose (TAC) layer for ensuring durability. In one or more embodiments, directions in transmissive axes of the upper polarizer and the lower polarizer may be vertical or parallel to each other.

[0073] A process for forming the microcavity 305 and for injecting and capping the liquid crystal layer 3 is described with reference to FIGS. 4 to 6.

[0074] FIGS. 4 to 6 are diagrams sequentially illustrating a manufacturing method of the liquid crystal display of FIG. 1 according to one or more embodiments of the present invention.

[0075] FIG. 4 illustrates that the liquid crystal injection hole 335 is formed to expose the microcavity 305. Steps preceding the formation of the liquid crystal injection hole 335 are described below with reference to FIGS. 1 to 3.

[0076] The gate line 121 and the storage voltage line 131 are formed on the insulation substrate 110 made of transparent glass, transparent plastic, or a different transparent substrate material. The gate line 121 and the storage voltage line 131 may be substantially simultaneously formed of the same material using the same mask. The gate line 121 includes a first gate electrode 124a, a second gate electrode 124b, and a third gate electrode 124c. The storage voltage line 131 includes storage electrodes 135a and 135b and a protrusion 134 protruding in the gate line 121 direction. The storage electrodes 135a and 135b have a structure surrounding a first subpixel electrode 192h and a second subpixel electrode 1921 of a front pixel. Since a gate voltage is to be applied to the gate line 121 and a storage voltage is to be applied to the storage voltage line 131, the gate line 121 and the storage voltage line 131 are electrically insulated from each other. The storage voltage may have a constant voltage level or may have a swing (or variable) voltage level.

[0077] A gate insulating layer 140 covering the gate line 121 and the storage voltage line 131 is formed on the gate line 121 and the storage voltage line 131.

[0078] Thereafter, the semiconductors 151, 154, and 155, the data line 171, the source electrodes 173a, 173b, and 173c, and the drain electrodes 175a, 175b, and 175c are formed on the gate insulating layer 140.

[0079] The semiconductors 151, 154, and 155, the data line 171, and the source electrodes and drain electrodes may be formed by separate processes or substantially simultaneously formed using one mask. In one or more embodiments, for forming the semiconductors 151, 154, and 155, the data line 171, and the source electrodes and drain electrodes using a same mask, materials for forming the semiconductors and material for forming the data line, the source electrodes, and the drain electrodes are sequentially laminated. Thereafter, two patterns are substantially simultaneously formed through one process of exposure, developing, and etching using one mask (e.g., a slit mask or a transflective mask). In one or more embodiments, in order to prevent the semiconductor 154 positioned at the channel part of the thin film transistor from being etched, the corresponding portion is exposed through the slit or transflective region of the mask.

[0080] A plurality of ohmic contacts may be formed on the semiconductors 151, 154, and 155 and between the data line 171 and the source electrodes and/or the drain electrodes.

[0081] The first passivation layer 180 is formed all over the data conductors 171, 173a, 173b, 173c, 175a, 175b, and 175c and the exposed semiconductor 154 portion. The first passivation layer 180 may contain an inorganic insulator, such as at least one of silicon nitride (SiNx) and silicon oxide (SiOx), or an organic insulator.

[0082] Thereafter, the color filter 230 and the first black matrix 220 are formed on the first passivation layer 180. The color filter 230 is formed before the first black matrix 220 is formed. The color filter 230 for each color may be formed by a separate process. Portions of the color filter 230 that correspond to the positions of the contact holes 186a, 186b, and 186c may be removed during etching of the color filter 230.

[0083] The first black matrix 220 is formed on the color filter 230 and is formed of a non-transmissive material for blocking light. The first black matrix 220may extend in a vertical direction and may overlap the data line 171 without overlapping the transistor formation region.

[0084] Thereafter, the second passivation layer 185 is formed all over the color filter 230 and the black matrix 220. The second passivation layer 185 may contain an inorganic insulator, such as at least one of silicon nitride (SiNx) and silicon oxide (SiOx), or an organic insulator.

[0085] Thereafter, a first contact hole 186a and a second contact hole 186b exposing the first drain electrode 175a and the extension 175b' of the second drain electrode 175b, respectively, are formed in (and/or are formed through) the color filter 230, the black matrix 220, and the passivation layers 180 and 185. Further, in (and/or through) the color filter 230, the black matrix 220, and the passivation layers 180 and 185, the third contact hole 186c exposing the protrusion 134 of the storage voltage line 131 and the extension 175c' of the third drain electrode 175c is formed.

[0086] Thereafter, the pixel electrode 192 including the first subpixel electrode 192h and the second subpixel electrode 1921 is formed on the second passivation layer 185. The pixel electrode 192 may be made of a transparent conductive material, such as ITO or IZO. The first subpixel electrode 192h and the second subpixel electrode 1921 are physically and electrically connected with the first drain electrode 175a and the second drain electrode 175b through the contact holes 186a and 186b, respectively. The connecting member 194 that electrically connects the extension 175c' of the third drain electrode 175c and the protrusion 134 of the storage voltage line 131 through the third contact hole 186c is formed. As a result, a part of the data voltage applied to the second drain electrode 175b is divided through the third source electrode 173c, and a magnitude of the voltage applied to the second subpixel electrode 1921 may be smaller than a magnitude of the voltage applied to the first subpixel electrode 192h.

[0087] Thereafter, the sacrificial layer 300 (illustrated in FIG. 4) is formed. The sacrificial layer 300 may be made of an organic material, such as a photoresist material. The organic material is exposed, developed, and etched using a mask after the organic material has been laminated on the second passivation layer 185 and the pixel electrode 192, to form the sacrificial layer 300. The sacrificial layer 300 may have an opening above the data line 171 such that the sacrificial layer 300 may not substantially overlap the data line. The sacrificial layer 300 may extend in the data line 171 direction. At the opening, the sacrificial layer 300 may have a tapered side wall analogous to the tapered side wall of the liquid crystal layer 3 illustrated in FIG. 2.

[0088] Thereafter, the common electrode 270 and the lower insulating layer 311 are sequentially formed on the sacrificial layer 300, the sidewalls of the opening of the sacrificial layer 300, and the exposed portion of the second passivation layer 185 that is exposed at the opening. In one or more embodiments, after a transparent conductive material, such as ITO or IZO, has been laminated throughout the entire panel (on the top surfaces of the sacrificial layer 300, the sidewalls, the exposed portion of the second passivation layer 185, etc.), a lower insulating layer forming material containing an inorganic insulating material, such as silicon nitride (SiNx), is laminated throughout the entire panel. As a result, the lower insulating layer 311 covers the common electrode 270.

[0089] Thereafter, the roof layer 312 is formed on the lower insulating layer 311. The roof layer 312 may contain an organic material. The roof layer 312 may not be formed in the transistor formation region, which may correspond to the location for the liquid crystal injection hole 335, i.e., the roof layer 312 may have an opening at the transistor formation region. The lower insulating layer 311 is exposed by the roof layer 312 opening in the transistor formation region. The roof layer 312 is exposed and developed using a mask after a roof layer material (containing an organic material) has been laminated in the entire panel area and after a portion of the roof layer material corresponding to the transistor formation region has been removed. Therefore, the sacrificial layer 300, the common electrode 270, and the lower insulating layer 311, but not the roof layer 312, are formed in the transistor formation region, and the sacrificial layer 300, the common electrode 270, the lower insulating layer 311, and the roof layer 312 are laminated in regions of the panel other than the transistor formation region.

[0090] Thereafter, the upper insulating layer 313, which may be formed of the inorganic insulating material, such as silicon nitride (SiNx), may be laminated on the entire display panel. As a result, the upper insulating layer 313 is formed on the roof layer 312 and formed on the exposed lower insulating layer 311 in the transistor formation region.

[0091] Thereafter, a photoresist pattern PR having an opening in the transistor formation region is formed on the upper insulating layer 313. The upper insulating layer 313, the lower insulating layer 311, and the common electrode 270 are etched using the photoresist pattern PR as a mask. As a result, the sacrificial layer 300 is exposed by the liquid crystal injection hole 335, as illustrated in FIG. 4. The etching process for forming the liquid crystal injection hole 335 may be performed through dry etching and/or wet etching.

[0092] Thereafter, as illustrated in FIG. 5, the sacrificial layer 300 exposed through the liquid crystal injection hole 335 is removed to form the microcavity 305. In one or more embodiments, the sacrificial layer 300 is made of the photoresist material used for forming the photoresist pattern PR, and the process of removing the photoresist pattern PR formed on the upper insulating layer 313 may be performed when removing the sacrificial layer 300. That is, the photoresist pattern PR formed on the upper insulating layer 313 and the sacrificial layer 300 may be substantially simultaneously wet-etched and removed by immersing the structure illustrated in FIG. 4 in an etchant (for example, a photo resist stripper). Advantageously, the manufacturing process may be substantially shortened and simplified. In one or more embodiments, the sacrificial layer 300 may be formed of a material that is different from the material of the photoresist pattern PR, and two separate process steps may be performed for removing the sacrificial layer 300 and the photo resist pattern PR. In one or more embodiments, the sacrificial layer 300 may be removed through dry etching, alternative or in addition to wet etching.

[0093] Thereafter, an alignment layer (not illustrated) and/or the liquid crystal layer 3 (illustrated in FIG. 6) are injected in the microcavity 305 using capillary force. As illustrated in FIG. 5, the microcavity 305 and the liquid crystal injection hole 335 are connected without obstacles. The black matrix to be positioned in the transistor formation region is not formed before the injection of the liquid crystal, and thus the liquid crystal injection may be substantially easy and efficient.

[0094] After the liquid crystal material for forming the liquid crystal layer 3 has been injected into the microcavity 305, a capping process for preventing the liquid crystal layer 3 from flowing out through the liquid crystal injection hole 335 is performed. As illustrated in FIG. 3, the second black matrix 225 is formed in the liquid crystal injection hole 335 to prevent transmission of light in the transistor formation region and to cap (and/or seal) the liquid crystal layer 3 so as to prevent leakage of liquid crystal of the liquid crystal layer 3.

[0095] The second black matrix 225 is formed of a non-transmissive material in the transistor formation region and in the liquid crystal injection hole 335. In one or more embodiments of the present invention, the second black matrix 225 is formed by injecting the non-transmissive material using an inkjet method. At least a portion of the second black matrix 225 is positioned in the liquid crystal injection hole 335. According to one or more embodiments, a part of the second black matrix 225 may be positioned outside the liquid crystal injection hole 335. Since the second black matrix 225 covers the transistor formation region, light passing through the transistor formation region is blocked, and thus the transistor formation region is not recognized by a viewer of the liquid crystal display. The second black matrix 225 may also seal the liquid crystal layer 3 so as to prevent the liquid crystal layer 3 from leaking through the liquid crystal injection hole 335 after the liquid crystal layer 3 has been injected through the liquid crystal injection hole 335 into the microcavity 305. The second black matrix 225 extends in a horizontal direction along the transistor formation region.

[0096] As illustrated in the plan view of FIG. 1, the first black matrix 220 (which include portions extending in the vertical direction) and the second black matrix 225 (which include portions extending in the horizontal direction) may form a lattice structure having openings. A substantial portion of the pixel electrode 192, a substantial portion of the color filter 230, and a substantial portion of the liquid crystal layer 3 may be positioned at one or more corresponding openings.

[0097] According to one or more embodiments, the lower insulating layer 311 and the upper insulating layer 313 may not be required.

[0098] A lower polarizer (not illustrated) may be disposed below the insulation substrate 110, and an upper polarizer may be disposed above the upper insulating layer 313. Each of the polarizers may include a polarized element for generating polarization and a tri-acetyl-cellulose (TAC) layer for ensuring durability. In one or more embodiments, directions in transmissive axes of the upper polarizer and the lower polarizer may be vertical or parallel to each other.

[0099] As can be appreciated from the foregoing discussion, the second black matrix 225 is formed after the liquid crystal layer 3 has been injected into the microcavity 305. Therefore, the second black matrix 225 may not block the injection of liquid crystal for forming the liquid crystal layer 3. Advantageously, the liquid crystal layer 3 may be substantially easily and efficiently formed.

[0100] In one or more embodiments, the second black matrix 225 seals the liquid crystal layer 3 to serve as a capping layer so as to prevent the liquid crystal layer 3 from leaking through the liquid crystal injection hole 335.

[0101] In one or more embodiments, an additional or alternative capping layer may be formed, as illustrated in FIGS. 7 to 11.

[0102] FIG. 7 is a cross-sectional view illustrating a liquid crystal display, e.g., the liquid crystal display of FIG. 1, according to one or more embodiments of the present invention. For example, FIG. 7 may be a cross-sectional view taken line III-III indicated in FIG. 1. The liquid crystal display may include a capping layer 350.

[0103] Referring to FIG. 1, In the liquid crystal display, a gate line 121 and a storage voltage line 131 are formed on an insulation substrate 110 made of transparent glass, transparent plastic, or a different transparent substrate material. The gate line 121 includes a first gate electrode 124a, a second gate electrode 124b, and a third gate electrode 124c. The storage voltage line 131 includes storage electrodes 135a and 135b and a protrusion 134 protruding in the gate line 121 direction (i.e., the horizontal direction). The storage electrodes 135a and 135b may form a structure that surrounds a first subpixel electrode 192h and a second subpixel electrode 1921 of a front pixel. A horizontal portion of the storage electrode 135b may be one wiring which is not separated from the horizontal portion of the front pixel.

[0104] A gate insulating layer 140 is formed on the gate line 121 and the storage voltage line 131. A semiconductor 151 positioned below a data line 171, portions of a semiconductor 155 positioned below one or more drain electrodes (e.g., a drain electrode 175b), and a semiconductor 154 positioned at a channel part of a thin film transistor are formed on the gate insulating layer 140.

[0105] A plurality of ohmic contacts may be respectively formed on the semiconductors 151, 154, and 155 and between the data line 171 and the one or more source electrodes and/or the one or more drain electrodes, is the ohmic contacts being omitted in the drawings.

[0106] On the semiconductors 151, 154, and 155 and the gate insulating layer 140, a set of data conductors that includes a plurality of data lines 171 including a first source electrode 173a and a second source electrode 173b, a first drain electrode 175a, a second drain electrode 175b, a third source electrode 173c, and a third drain electrode 175c is formed.

[0107] The first gate electrode 124a, the first source electrode 173a, and the first drain electrode 175a form a first thin film transistor together with the semiconductor 154, and a channel of the thin film transistor is formed at the semiconductor portion 154 between the first source electrode 173a and the first drain electrode 175a. Analogously, the second gate electrode 124b, the second source electrode 173b, and the second drain electrode 175b form a second thin film transistor together with the semiconductor 154, and a channel of the thin film transistor is formed at the semiconductor portion 154 between the second source electrode 173b and the second drain electrode 175b. The third gate electrode 124c, the third source electrode 173c, and the third drain electrode 175c form a third thin film transistor together with the semiconductor 154, and a channel of the thin film transistor is formed at the semiconductor portion 154 between the third source electrode 173c and the third drain electrode 175c.

[0108] The data line 171 of may have a structure with a narrow width in a thin film transistor formation region around (or near) an extension 175c' of the third drain electrode 175c. This structure is for keeping a distance from the adjacent wiring and reducing signal interference. In one or more embodiments, the structure may not be required.

[0109] A first passivation layer 180 is formed on the data conductors 171, 173c, 175a, 175b, and 175c and the exposed semiconductor 154 portion. The first passivation layer 180 may include an inorganic insulator, such as at least one of silicon nitride (SiNx) and silicon oxide (SiOx), or an organic insulator.

[0110] A color filter 230 is formed on the first passivation layer 180. The color filter 230 having the same color is formed in adjacent pixels in a vertical direction (i.e., the data line direction). Adjacent pixels in a horizontal direction (i.e., the gate line direction) have color filters 230 and 230' having different colors, and two color filters 230 and 230' may be substantially simultaneously formed and may overlap each other over the data line 171. Each of the color filters 230 and 230' may display one color of a set of primary colors such as three primary colors of red, green, and blue. In one or more embodiments, each of the color filters 230 and 230' may display one color of cyan, magenta, yellow, and white-based colors.

[0111] A first black matrix 220, i.e., a black matrix portion overlapping and/or covering a data line, is formed on the color filters 230 and 230' and overlaps at least a portion of each of the color filters 230 and 230'. The first black matrix 220 is made of a non-transmissive material for blocking light. The first black matrix 220 is formed based on a region where the data line 171 is formed to extend in a vertical direction and is not formed in a 'transistor formation regions', a region where the gate line 121, the storage voltage line 131, and one or more thin film transistors are formed, such that the first black matrix 220 may not overlap the gate line 121, the storage voltage line 131, or the one or more thin film transistors. A black matrix 225 may overlap the transistor formation region and may block light in the transistor formation region. The second black matrix 225, i.e., a black matrix disposed in a liquid crystal injection hole 335, may be formed after liquid crystal molecules have been injected in a microcavity (e.g., microcavity 305 illustrated in FIG. 5). This will be described below.

[0112] A second passivation layer 185 may cover the color filter 230 and the black matrix 220 and may be formed on the color filter 230 and the black matrix 220. The second passivation layer 185 may contain an inorganic insulator, such as at least one of silicon nitride (SiNx) and silicon oxide (SiOx), or an organic insulator. As illustrated in cross-sectional views of FIGS. 2 and 3, in the case where a step occurs due to a thickness difference and/or thickness variation associated with the color filter 230 and/or the black matrix 220, the second passivation layer 185 may reduce or compensate the thickness difference and/or the thickness variation; the second passivation layer 185 may server as a planarization layer disposed over the color filter 230 and the black matrix 220.

[0113] A first contact hole 186a and a second contact hole 186b which expose the first drain electrode 175a and an extension 175b' of the second drain electrode 175b, respectively, are formed in (and/or are formed through) one or more of the color filter 230, the first black matrix 220, and the passivation layers 180 and 185. A third contact hole 186c, which exposes a protrusion 134 of the storage voltage line 131 and the extension 175c' of the third drain electrode 175c is formed in (and/or is formed through) on or more of the color filter 230, the first black matrix 220, and the passivation layers 180 and 185.

[0114] In one or more embodiments, the contact holes 186a, 186b, and 186c are formed in (and/or are formed through) the first black matrix 220 and the color filter 230, even if etching the first black matrix 220 and the color filter 230 may be more difficult than etching the passivation layers 180 and 185 because of material properties. In one or more embodiments, the material used for forming the first black matrix 220 or the color filter 230 may not be formed at positions corresponding to the contact holes 186a, 186b, and 186c before etching of the black matrix 220 or the color filter 230.

[0115] In one or more embodiments, the color filter 230 and the passivation layers 180 and 185 may be etched, and a position of the first black matrix 220 may be changed, in order to form the contact holes 186a, 186b, and 186c.

[0116] On the second passivation layer 185, a pixel electrode 192 including the first subpixel electrode 192h and the second subpixel electrode 1921 is formed. The pixel electrode 192 may be made of a transparent conductive material such as ITO or IZO.

[0117] The first subpixel electrode 192h and the second subpixel electrode 1921 are adjacent to each other in a column direction. Each of the first subpixel electrode 192h and the second subpixel electrode 1921 may have an overall quadrangular shape, and include a cross stem configured by a horizontal stem and a vertical stem crossing the horizontal stem. Each of the first subpixel electrode 192h and the second subpixel electrode 1921 may be divided into four subregions by the horizontal stem and the vertical stem, and each subregion may include a plurality of minute branches.

[0118] The minute branches of the first subpixel electrode 192h and the second subpixel electrode 1921 form an angle in a range of approximately 40 to 45 degrees with the gate line 121 or the horizontal stem. The minute branches of two adjacent subregions may be perpendicular to each other. A width of the minute branch may be gradually increased. Distances between the minute branches may be different from each other.

[0119] The first subpixel electrode 192h and the second subpixel electrode 1921 are physically and electrically connected with the first drain electrode 175a and the second drain electrode 175b through the contact holes 186a and 186b and receive data voltage from the first drain electrode 175a and the second drain electrode 175b.

[0120] A connecting member 194 electrically connects the extension 175c' of the third drain electrode 175c and the protrusion 134 of the storage voltage line 131 through the third contact hole 186c. As a result, a part of the data voltage applied to the second drain electrode 175b is divided through the third source electrode 173c, and a magnitude of the voltage applied to the second subpixel electrode 1921 may be smaller than a magnitude of the voltage applied to the first subpixel electrode 192h.

[0121] An area of the second subpixel electrode 1921 may be in a range of 1 to 2 times an area of the first subpixel electrode 192h.

[0122] An opening for collecting gas discharged from the color filter 230 and a cover for covering the opening may be formed in the second passivation layer 185. The cover may be formed of the same material as the pixel electrode 192. The opening and the cover may prevent gas discharged from the color filter 230 from being transferred to other elements. In one or more embodiments, the opening and the cover may not be required.

[0123] A microcavity 305 is positioned on the second passivation layer 185 and the pixel electrode 192 (and is positioned between the second passivation layer 185 and a common electrode 270), and the liquid crystal layer 3 is formed in the microcavity. An alignment layer (not illustrated) may be formed between the second passivation layer 185 and the liquid crystal layer 3 in order to align the liquid crystal molecules injected in the microcavity 305. The alignment layer may contain at least one of polyamic acid, polysiloxane, and polyimide, which are generally used in a liquid crystal alignment layer.

[0124] The liquid crystal layer 3 is formed in the microcavity 305 (and on the alignment layer). The liquid crystal molecules 310 are initially aligned by the alignment layer and the alignment direction is changed according to the applied electric field. A height of the liquid crystal layer 3 corresponds to a height of the microcavity 305. A thickness of the liquid crystal layer 3 may be in a range of 2.0 μm to 3.6 μm.

[0125] Liquid crystal material for forming the liquid crystal layer 3 may be injected into the microcavity 305 using capillary force in a liquid crystal injection hole 335. The alignment layer may be formed capillary force.

[0126] The common electrode 270 is positioned above the microcavity 305 and the liquid crystal layer 3 with the microcavity 305 and the liquid crystal layer 3 being disposed between the common electrode 270 and the second passivation layer 185. The common electrode 270 may have a curved structure including a protrusion portion (illustrated in FIG. 2) that is disposed above a data line 171 and protrudes (and is convex) toward the data line 171. At least a portion of the first black matrix 220 may be disposed between the protrusion portion and the data line 171. The protrusion portion may directly contact the second passivation layer 185. A portion of the roof material 312 and a portion of the lower insulating layer 311 may be disposed inside a recess structure of the protrusion portion. The common electrode 270 is not formed in the liquid crystal injection hole 335 portion (which corresponds to the transistor formation region); the liquid crystal injection hole 335 may be disposed between two portions of the common electrode 270, as illustrated in FIG. 3. The common electrode 270 may extend in a gate line direction (i.e., the horizontal direction).

[0127] The common electrode 270 is made of a transparent conductive material, such as ITO or IZO, and serves to generate an electric field together with the pixel electrode 192 to control an alignment direction of the liquid crystal molecules.

[0128] A lower insulating layer 311 is positioned on the common electrode 270. The lower insulating layer 311 may contain an inorganic insulating material such as silicon nitride (SiNx).

[0129] A roof layer 312 is formed on the lower insulating layer 311. The roof layer 312 may serve to support a space (microcavity 305) to be formed between the pixel electrode 192 and the common electrode 270. The roof layer 312 according to one or more embodiments serves to support the microcavity 305 above the common electrode 270 at a predetermined thickness.

[0130] An upper insulating layer 313 is formed on the roof layer 312. The upper insulating layer 313 may contain an inorganic insulating material, such as silicon nitride (SiNx).

[0131] The liquid crystal injection hole 335 may be formed through the lower insulating layer 311, the roof layer 312, and the upper insulating layer 313 in the transistor formation region, wherein a liquid crystal may be injected through the liquid crystal injection hole 335 into the microcavity 305. The liquid crystal injection hole 335 may be used for removing the sacrificial layer 300 of FIG. 4 in the process of forming the microcavity 305..

[0132] The lower insulating layer 311 and the upper insulating layer 313 may be laminated with portions disposed in the transistor formation region corresponding to a position for forming the liquid crystal injection hole 335. In one or more embodiments, the roof layer 312 may not be formed in the transistor formation region; therefore, the liquid crystal injection hole 335 may be formed by removing portions of the lower insulating layer 311 and upper insulating layer 313 in the transistor formation region without removing portions of the roof layer 312. The sacrificial layer 300 may be exposed through the liquid crystal injection hole 335 after a portion of the common electrode 270 that is positioned in the transistor formation region has been removed.

[0133] According to one or more embodiments, the roof layer 312, the upper insulating layer 313, and the lower insulating layer 311 are etched in the transistor formation region to form the liquid crystal injection hole 335.

[0134] According to one or more embodiments, the lower insulating layer 311 and the upper insulating layer 313 may be omitted.

[0135] A capping layer 350 is formed on the liquid crystal injection hole 335 and the upper insulating layer 313. The capping layer 350 is made of a transparent material and may contain an organic insulating material or an inorganic insulating material, such as silicon nitride (SiNx). The capping layer 350, as illustrated in FIG. 7, may be formed throughout the entire display panel. In one or more embodiments, the capping layer 350 may be formed only near the liquid crystal injection hole 335. The capping layer 350 serves to seal the liquid crystal injection hole 335 after the liquid crystal material of the liquid crystal layer 3 has been injected into the microcavity 305 so as to prevent the liquid crystal layer 3 from leaking through the liquid crystal injection hole 335.

[0136] In one or more embodiments, as illustrated in FIG. 7, a portion of the liquid crystal layer 3 may be disposed between the second passivation layer 185 and the capping layer 350. In one or more embodiments, the capping layer 350 may directly contact the second passivation layer 185 and thus may separate a first portion of the liquid crystal layer 3 from a second portion of the liquid crystal layer 3.

[0137] The second black matrix 225 is formed on the capping layer 350, formed in the transistor formation region, formed in the liquid crystal injection hole 335. At least a portion of the capping layer 350 may be disposed between the second black matrix 225 and the second passivation layer 185 and may be disposed between the second black matrix 225 and a portion of the liquid crystal layer 3. At least a portion of the capping layer 350 (e.g., a portion that is substantially perpendicular to the substrate 110) may be disposed between the second black matrix 225 and at least a portion of one or more of the upper insulating layer 313, the roof layer 312, the lower insulating layer 311, the common electrode 270, and the liquid crystal layer 3. In one or more embodiments of the present invention, the second black matrix 225 is formed by injecting the material using an inkjet method. According to the invention, at least a portion of the second black matrix 225 is positioned inside the liquid crystal injection hole 335. According to one or more embodiments, a part of the second black matrix 225 may be positioned outside the liquid crystal injection hole 335. The second black matrix 225 is formed of a non-transmissive material. Since the second black matrix 225 covers the transistor formation region, light passing through the transistor formation region is blocked, and thus the transistor formation region is not recognized by a viewer of the liquid crystal display. The second black matrix 225 extends in a horizontal direction along the transistor formation region.

[0138] As illustrated in the plan view of FIG. 1, the first black matrix 220 (which include portions extending in the vertical direction) and the second black matrix 225 (which include portions extending in the horizontal direction) may form a lattice structure having openings. A substantial portion of the pixel electrode 192, a substantial portion of the color filter 230, and a substantial portion of the liquid crystal layer 3 may be positioned at one or more corresponding openings.

[0139] A lower polarizer (not illustrated) may be positioned below the insulation substrate 110, and an upper polarizer may be positioned above the upper insulating layer 313. Each of the polarizers may include a polarized element for generating polarization and a tri-acetyl-cellulose (TAC) layer for ensuring durability. In one or more embodiments, directions in transmissive axes of the upper polarizer and the lower polarizer may be vertical or parallel to each other.

[0140] A process for forming the microcavity 305 and for injecting and capping the liquid crystal layer 3 is described with reference to FIGS. 8 to 11.

[0141] FIGS. 8 to 11 are diagrams sequentially illustrating a manufacturing method of the liquid crystal display of FIGS. 1 and 7 according to one or more embodiments of the present invention.

[0142] FIG. 8 illustrates that the liquid crystal injection hole 335 is formed to expose the microcavity 305. Steps preceding the formation of the liquid crystal injection hole 335 are described below with reference to at least some of

FIGS. 1 to 7.

[0143] The gate line 121 and the storage voltage line 131 are formed on the insulation substrate 110 made of transparent glass, transparent plastic, or a different transparent substrate material. The gate line 121 and the storage voltage line 131 may be substantially simultaneously formed of the same material using the same mask. The gate line 121 includes a first gate electrode 124a, a second gate electrode 124b, and a third gate electrode 124c. The storage voltage line 131 includes storage electrodes 135a and 135b and a protrusion 134 protruding in the gate line 121 direction. The storage electrodes 135a and 135b have a structure surrounding a first subpixel electrode 192h and a second subpixel electrode 1921 of a front pixel. Since a gate voltage is to be applied to the gate line 121 and a storage voltage is to be applied to the storage voltage line 131, the gate line 121 and the storage voltage line 131 are electrically insulated from each other. The storage voltage may have a constant voltage level or may have a swing (or variable) voltage level.

[0144] A gate insulating layer 140 covering the gate line 121 and the storage voltage line 131 is formed on the gate line 121 and the storage voltage line 131.

[0145] Thereafter, the semiconductors 151, 154, and 155, the data line 171, the source electrodes 173a, 173b, and 173c, and the drain electrodes 175a, 175b, and 175c are formed on the gate insulating layer 140.

[0146] The semiconductors 151, 154, and 155, the data line 171, and the source electrodes and drain electrodes may be formed by separate processes or substantially simultaneously formed using one mask. In one or more embodiments, for forming the semiconductors 151, 154, and 155, the data line 171, and the source electrodes and drain electrodes using a same mask, materials for forming the semiconductors and material for forming the data line, the source electrodes, and the drain electrodes are sequentially laminated. Thereafter, two patterns are substantially simultaneously formed through one process of exposure, developing, and etching using one mask (e.g., a slit mask or a transflective mask). In one or more embodiments, in order to prevent the semiconductor 154 positioned at the channel part of the thin film transistor from being etched, the corresponding portion is exposed through the slit or transflective region of the mask.

[0147] A plurality of ohmic contacts may be formed on the semiconductors 151, 154, and 155 and between the data line 171 and the source electrodes and/or the drain electrodes.

[0148] The first passivation layer 180 is formed all over the data conductors 171, 173a, 173b, 173c, 175a, 175b, and 175c and the exposed semiconductor 154 portion. The first passivation layer 180 may contain an inorganic insulator, such as at least one of silicon nitride (SiNx) and silicon oxide (SiOx), or an organic insulator.

[0149] Thereafter, the color filter 230 and the first black matrix 220 are formed on the first passivation layer 180. The color filter 230 is formed before the first black matrix 220 is formed. The color filter 230 for each color may be formed by a separate process. Portions of the color filter 230 that correspond to the positions of the contact holes 186a, 186b, and 186c may be removed during etching of the color filter 230.

[0150] The first black matrix 220 is formed on the color filter 230 and is formed of a non-transmissive material for blocking light. The first black matrix 220may extend in a vertical direction and may overlap the data line 171 without overlapping the transistor formation region.

[0151] Thereafter, the second passivation layer 185 is formed all over the color filter 230 and the black matrix 220. The second passivation layer 185 may contain an inorganic insulator, such as at least one of silicon nitride (SiNx) and silicon oxide (SiOx), or an organic insulator.

[0152] Thereafter, a first contact hole 186a and a second contact hole 186b exposing the first drain electrode 175a and the extension 175b' of the second drain electrode 175b, respectively are formed in (and/or are formed through) the color filter 230, the black matrix 220, and the passivation layers 180 and 185. Further, in (and/or through) the color filter 230, the black matrix 220, and the passivation layers 180 and 185, the third contact hole 186c exposing the protrusion 134 of the storage voltage line 131 and the extension 175c' of the third drain electrode 175c is formed.

[0153] Thereafter, the pixel electrode 192 including the first subpixel electrode 192h and the second subpixel electrode 1921 is formed on the second passivation layer 185. The pixel electrode 192 may be made of a transparent conductive material, such as ITO or IZO. The first subpixel electrode 192h and the second subpixel electrode 1921 are physically and electrically connected with the first drain electrode 175a and the second drain electrode 175b through the contact holes 186a and 186b, respectively. The connecting member 194 that electrically connects the extension 175c' of the third drain electrode 175c and the protrusion 134 of the storage voltage line 131 through the third contact hole 186c is formed. As a result, a part of the data voltage applied to the second drain electrode 175b is divided through the third source electrode 173c, and a magnitude of the voltage applied to the second subpixel electrode 1921 may be smaller than a magnitude of the voltage applied to the first subpixel electrode 192h.

[0154] Thereafter, the sacrificial layer 300 (illustrated in FIG. 8) is formed. The sacrificial layer 300 may be made of an organic material, such as a photoresist material. The organic material is exposed, developed, and etched using a mask after the organic material has been laminated on the second passivation layer 185 and the pixel electrode 192, to form the sacrificial layer 300. The sacrificial layer 300 may have an opening above the data line 171 such that the sacrificial layer 300 may not substantially overlap the data line. The sacrificial layer 300 may extend in the data line 171 direction. At the opening, the sacrificial layer 300 may have a tapered side wall analogous to the tapered side wall of the liquid crystal layer 3 illustrated in FIG. 2.

[0155] Thereafter, the common electrode 270 and the lower insulating layer 311 are sequentially formed on the sacrificial layer 300, the sidewalls of the opening of the sacrificial layer 300, and the exposed portion of the second passivation layer 185 that is exposed at the opening. In one or more embodiments, after a transparent conductive material, such as ITO or IZO, has been laminated throughout the entire panel (on the top surfaces of the sacrificial layer 300, the sidewalls, the exposed portion of the second passivation layer 185, etc.), a lower insulating layer forming material containing an inorganic insulating material, such as silicon nitride (SiNx), is laminated throughout the entire panel. As a result, the lower insulating layer 311 covers the common electrode 270.

[0156] Thereafter, the roof layer 312 is formed on the lower insulating layer 311. The roof layer 312 may contain an organic material. The roof layer 312 may not be formed in the transistor formation region, which may correspond to the location for the liquid crystal injection hole 335, i.e., the roof layer 312 may have an opening at the transistor formation region. The lower insulating layer 311 is exposed by the roof layer 312 opening in the transistor formation region. The roof layer 312 is exposed and developed using a mask after a roof layer material (containing an organic material) has been laminated in the entire panel area and after a portion of the roof layer material corresponding to the transistor formation region has been removed. Therefore, the sacrificial layer 300, the common electrode 270, and the lower insulating layer 311, but not the roof layer 312, are formed in the transistor formation region, and the sacrificial layer 300, the common electrode 270, the lower insulating layer 311, and the roof layer 312 are laminated in regions of the panel other than the transistor formation region.

[0157] Thereafter, the upper insulating layer 313, which may be formed of the inorganic insulating material, such as silicon nitride (SiNx), may be laminated on the entire display panel. As a result, the upper insulating layer 313 is formed on the roof layer 312 and formed on the exposed lower insulating layer 311 in the transistor formation region.

[0158] Thereafter, a photoresist pattern PR having an opening in the transistor formation region is formed on the upper insulating layer 313. The upper insulating layer 313, the lower insulating layer 311, and the common electrode 270 are etched using the photoresist pattern PR as a mask. As a result, the sacrificial layer 300 is exposed by the liquid crystal injection hole 335, as illustrated in FIG. 8. The etching process for forming the liquid crystal injection hole 335 may be performed through dry etching and/or wet etching.

[0159] Thereafter, as illustrated in FIG. 9, the sacrificial layer 300 exposed through the liquid crystal injection hole 335 is removed to form the microcavity 305. In one or more embodiments, the sacrificial layer 300 is made of the photoresist material used for forming the photoresist pattern PR, and the process of removing the photoresist pattern PR formed on the upper insulating layer 313 may be performed when removing the sacrificial layer 300. That is, the photoresist pattern PR formed on the upper insulating layer 313 and the sacrificial layer 300 may be substantially simultaneously wet-etched and removed by immersing the structure illustrated in FIG. 4 in an etchant (for example, a photo resist stripper). Advantageously, the manufacturing process may be substantially shortened and simplified. In one or more embodiments, the sacrificial layer 300 may be formed of a material that is different from the material of the photoresist pattern PR, and two separate process steps may be performed for removing the sacrificial layer 300 and the photo resist pattern PR. In one or more embodiments, the sacrificial layer 300 may be removed through dry etching, alternative or in addition to wet etching.

[0160] Thereafter, an alignment layer (not illustrated) and/or the liquid crystal layer 3 (illustrated in FIG. 10) are injected in the microcavity 305 using capillary force. As illustrated in FIG. 9, the microcavity 305 and the liquid crystal injection hole 335 are connected without obstacles. The black matrix to be positioned in the transistor formation region is not formed before the injection of the liquid crystal, and thus the liquid crystal injection may be substantially easy and efficient.

[0161] After the liquid crystal material for forming the liquid crystal layer 3 has been injected into the microcavity 305, a capping process for preventing the liquid crystal layer 3 from flowing out through the liquid crystal injection hole 335 is performed. In one or more embodiments, as illustrated in FIG. 7, the capping layer 350 is formed to seal the liquid crystal injection hole 335 such that leakage of the liquid crystal layer 3 may be prevented.

[0162] The capping layer 350 is formed in the liquid crystal injection hole 335 and is formed on the upper insulating layer 313. The capping layer 350 is made of a transparent material and may contain an organic insulating material or an inorganic insulating material, such as silicon nitride (SiNx). In one or more embodiments, the capping layer 350 is formed throughout the entire display panel. According to one or more embodiments, the capping layer 350 may be formed only near the liquid crystal injection hole 335. The capping layer 350 serves to seal the liquid crystal injection hole 335 after the liquid crystal material of the liquid crystal layer 3 has been injected into the microcavity 305 so as to prevent the liquid crystal layer 3 from leaking through the liquid crystal injection hole 335.

[0163] Thereafter, as illustrated in FIG. 7, the second black matrix 225, which is formed of a non-transmissive material, may be formed on the capping layer 350, formed in the transistor formation region, and formed in the liquid crystal injection hole 335. In one or more embodiments of the present invention, the second black matrix 225 is formed by injecting the material using an inkjet method. According to the invention, at least a portion of the second black matrix 225 is positioned inside the liquid crystal injection hole 335. According to one or more embodiments, a part of the second black matrix 225 may be positioned outside the liquid crystal injection hole 335. Since the second black matrix 225 covers the transistor formation region, light passing through the transistor formation region is blocked and thus the transistor formation region is not recognized by a viewer of the liquid crystal display. The second black matrix 225 extends in a horizontal direction along the transistor formation region.

[0164] As illustrated in the plan view of FIG. 1, the first black matrix 220 (which include portions extending in the vertical direction) and the second black matrix 225 (which include portions extending in the horizontal direction) may form a lattice structure having openings. A substantial portion of the pixel electrode 192, a substantial portion of the color filter 230, and a substantial portion of the liquid crystal layer 3 may be positioned at one or more corresponding openings.

[0165] According to one or more embodiments, the lower insulating layer 311 and the upper insulating layer 313 may not be required.

[0166] A lower polarizer (not illustrated) may be disposed below the insulation substrate 110, and an upper polarizer may be disposed above the upper insulating layer 313. Each of the polarizers may include a polarized element for generating polarization and a tri-acetyl-cellulose (TAC) layer for ensuring durability. In one or more embodiments, directions in transmissive axes of the upper polarizer and the lower polarizer may be vertical or parallel to each other.

[0167] As can be appreciated from the foregoing discussion, the capping layer 350 and the second black matrix 225 may be formed after the liquid crystal layer 3 has been injected into the microcavity 305. Therefore, the second black matrix 225 may not block the injection of liquid crystal for forming the liquid crystal layer 3. Advantageously, the liquid crystal layer 3 may be substantially easily and efficiently formed.

[0168] In one or more embodiments, as illustrated in FIG. 7, the liquid crystal layer 3 may not leak through the liquid crystal injection hole 335, which is sealed by at least the capping layer 350. In one or more embodiments, if the material of the second black matrix 225 directly contacts the liquid crystal layer 3, the material of the second black matrix 225 may cause contamination and/or deterioration to the liquid crystal layer 3 during or after a manufacturing process of the second black matrix 225, and the capping layer 350, which is disposed between the liquid crystal layer 3 and the second black matrix 225 may prevent such contamination and/or deterioration.

[0169] As can be appreciated from the foregoing, the formation process of liquid crystal layer 3 may be performed between the formation process of the first black matrix 220 and the formation process of the second black matrix 225, such that the formation of the liquid crystal layer 3 may not be obstructed by the second black matrix 225. The first black matrix 220 and the second black matrix 225 may be formed in two separate processes and may be located at two different layers in the liquid crystal display.

[0170] In one or more embodiments, as discussed with reference to FIGS. 12 to 14, a first black matrix 220 and a second black matrix 225, i.e., two portions of a combined black matrix, may be substantially simultaneously formed in one process.

[0171] FIGS. 12 and 13 are cross-sectional views illustrating a liquid crystal display, e.g., the liquid crystal display of FIG. 1, according to one or more embodiments of the present invention, and FIG. 14 is a plan view illustrating positions of a first black matrix and a second black matrix in the liquid crystal display of FIGS. 12 and 13.

[0172] FIGS. 12 and 13 may be cross-sectional views taken along a cross-sectional line II-II indicated in FIG. 1 and a cross-sectional line III-III indicated in FIG. 1, respectively. As can be appreciated from FIGS. 12 and 13, both the first black matrix 220 and the second black matrix 225 may be positioned at the upper side (i.e., a same side) with respect to the liquid crystal layer 3. In one or more embodiments, the second black matrix 225 may be configured to seal the liquid crystal injection hole 335. In one or more embodiments, an additional capping layer may be formed to seal the liquid crystal injection hole 335.

[0173] In the liquid crystal display, gate line 121 and a storage voltage line 131 are formed on an insulation substrate 110 made of transparent glass, transparent plastic, or a different transparent substrate material. The gate line 121 includes a first gate electrode 124a, a second gate electrode 124b, and a third gate electrode 124c. The storage voltage line 131 includes storage electrodes 135a and 135b and a protrusion 134 protruding in the gate line 121 direction (i.e., the horizontal direction). The storage electrodes 135a and 135b may form a structure that surrounds a first subpixel electrode 192h and a second subpixel electrode 1921 of a front pixel. A horizontal portion of the storage electrode 135b may be one wiring which is not separated from the horizontal portion of the front pixel.

[0174] A gate insulating layer 140 is formed on the gate line 121 and the storage voltage line 131. A semiconductor 151 positioned below a data line 171, portions of a semiconductor 155 positioned below one or more drain electrodes (e.g., a drain electrode 175b), and a semiconductor 154 positioned at a channel part of a thin film transistor are formed on the gate insulating layer 140.

[0175] A plurality of ohmic contacts may be respectively formed on the semiconductors 151, 154, and 155 and between the data line 171 and the one or more source electrodes and/or the one or more drain electrodes, the ohmic contacts being omitted in the drawings.

[0176] On the semiconductors 151, 154, and 155 and the gate insulating layer 140, a set of data conductors that includes a plurality of data lines 171 including a first source electrode 173a and a second source electrode 173b, a first drain electrode 175a, a second drain electrode 175b, a third source electrode 173c, and a third drain electrode 175c is formed.

[0177] The first gate electrode 124a, the first source electrode 173a, and the first drain electrode 175a form a first thin film transistor together with the semiconductor 154, and a channel of the thin film transistor is formed at the semiconductor portion 154 between the first source electrode 173a and the first drain electrode 175a. Analogously, the second gate electrode 124b, the second source electrode 173b, and the second drain electrode 175b form a second thin film transistor together with the semiconductor 154, and a channel of the thin film transistor is formed at the semiconductor portion 154 between the second source electrode 173b and the second drain electrode 175b. The third gate electrode 124c, the third source electrode 173c, and the third drain electrode 175c form a third thin film transistor together with the semiconductor 154, and a channel of the thin film transistor is formed at the semiconductor portion 154 between the third source electrode 173c and the third drain electrode 175c.

[0178] The data line 171 of may have a structure with a narrow width in a thin film transistor formation region near an extension 175c' of the third drain electrode 175c. This structure is for keeping a distance from the adjacent wiring and reducing signal interference. In one or more embodiments, the structure may not be required. A first passivation layer 180 is formed on the data conductors 171, 173c, 175a, 175b, and 175c and the exposed semiconductor 154 portion. The first passivation layer 180 may include an inorganic insulator, such as at least one of silicon nitride (SiNx) and silicon oxide (SiOx), or an organic insulator.

[0179] A color filter 230 is formed on the first passivation layer 180. The color filter 230 having the same color is formed in adjacent pixels in a vertical direction (i.e., the data line direction). Adjacent pixels in a horizontal direction (i.e., the gate line direction) have color filters 230 and 230' having different colors, and two color filters 230 and 230' may be substantially simultaneously formed and may overlap each other over the data line 171. Each of the color filters 230 and 230' may display one color of a set of primary colors such as three primary colors of red, green, and blue. In one or more embodiments, each of the color filters 230 and 230' may display one color of cyan, magenta, yellow, and white-based colors.

[0180] A second passivation layer 185 may cover the color filter 230 and may be formed on the color filter 230. The second passivation layer 185 may contain an inorganic insulator, such as at least one of silicon nitride (SiNx) and silicon oxide (SiOx), or an organic insulator. As illustrated in cross-sectional views of FIGS. 12 and 13, in the case where a step occurs due to a thickness difference and/or thickness variation associated with the color filter 230, the second passivation layer 185 may reduce or compensate the thickness difference and/or the thickness variation; the second passivation layer 185 may server as a planarization layer disposed over the color filter 230.

[0181] A first contact hole 186a and a second contact hole 186b which expose the first drain electrode 175a and an extension 175b' of the second drain electrode 175b, respectively, are formed in (and/or are formed through) one or more of the color filter 230 and the passivation layers 180 and 185. A third contact hole 186c which exposes a protrusion 134 of the storage voltage line 131 and the extension 175c' of the third drain electrode 175c is formed in (and/or is formed through) on or more of the color filter 230 and the passivation layers 180 and 185.

[0182] In one or more embodiments, the contact holes 186a, 186b, and 186c are formed in (and/or are formed through) the color filter 230, even if etching the color filter 230 may be more difficult than etching the passivation layers 180 and 185 because of material properties. In one or more embodiments, the material used for forming the color filter 230 may be formed at position corresponding to the contact holes 186a, 186b, and 186c before etching the color filter 230.

[0183] On the second passivation layer 185, a pixel electrode 192 including the first subpixel electrode 192h and the second subpixel electrode 1921 is formed. The pixel electrode 192 may be made of a transparent conductive material, such as ITO or IZO.

[0184] The first subpixel electrode 192h and the second subpixel electrode 1921 are adjacent to each other in a column direction. Each of the first subpixel electrode 192h and the second subpixel electrode 1921 may have an overall quadrangular shape, and may include a cross stem structure having a horizontal stem and a vertical stem crossing the horizontal stem. Each of the first subpixel electrode 192h and the second subpixel electrode 1921 may be divided into four subregions by the horizontal stem and the vertical stem, and each subregion may include a plurality of minute branches.

[0185] The minute branches of the first subpixel electrode 192h and the second subpixel electrode 1921 form an angle of approximately in a range of 40 to 45 degrees with the gate line 121 or the horizontal stem. The minute branches of two adjacent subregions may be perpendicular to each other. A width of the minute branch may be gradually increased. Distances between the minute branches may be different from each other.

[0186] The first subpixel electrode 192h and the second subpixel electrode 1921 are physically and electrically connected with the first drain electrode 175a and the second drain electrode 175b through the contact holes 186a and 186b and receive data voltage from the first drain electrode 175a and the second drain electrode 175b.

[0187] A connecting member 194 electrically connects the extension 175c' of the third drain electrode 175c and the protrusion 134 of the storage voltage line 131 through the third contact hole 186c. As a result, a part of the data voltage applied to the second drain electrode 175b is divided through the third source electrode 173c, and a magnitude of the voltage applied to the second subpixel electrode 1921 may be smaller than a magnitude of the voltage applied to the first subpixel electrode 192h.

[0188] An area of the second subpixel electrode 1921 may be in a range of 1 to 2 times an area of the first subpixel electrode 192h.

[0189] An opening for collecting gas discharged from the color filter 230 and a cover for covering the opening may be formed in the second passivation layer 185. The cover may be formed of the same material as the pixel electrode 192. The opening and the cover may prevent gas discharged from the color filter 230 from being transferred to other elements. In one or more embodiments, the opening and the cover may not be required.

[0190] A microcavity 305 is positioned on the second passivation layer 185 and the pixel electrode 192 (and is positioned between the second passivation layer 185 and a common electrode 270), and the liquid crystal layer 3 is formed in the microcavity. An alignment layer (not illustrated) may be formed between the second passivation layer 185 and the liquid crystal layer 3 in order to align the liquid crystal molecules injected in the microcavity 305. The alignment layer may contain at least one of polyamic acid, polysiloxane, and polyimide, which are generally used in a liquid crystal alignment layer.

[0191] The liquid crystal layer 3 is formed in the microcavity 305 (and on the alignment layer). The liquid crystal molecules 310 are initially aligned by the alignment layer and the alignment direction is changed according to the applied electric field. A height of the liquid crystal layer 3 corresponds to a height of the microcavity 305. A thickness of the liquid crystal layer 3 may be in a range of 2.0 μm to 3.6 μm.

[0192] The liquid crystal material for forming the liquid crystal layer 3 may be injected into the microcavity 305 using capillary force in a liquid crystal injection hole 335. The alignment layer may be formed using capillary force.

[0193] The common electrode 270 is positioned above the microcavity 305 and the liquid crystal layer 3 with the microcavity 305 and the liquid crystal layer 3 being disposed between the common electrode 270 and the second passivation layer 185. The common electrode 270 may have a curved structure including a protrusion portion (illustrated in FIG. 2) that is disposed above a data line 171 and protrudes (and is convex) toward the data line 171. At least a portion of the first black matrix 220 may be disposed between the protrusion portion and the data line 171. The protrusion portion may directly contact the second passivation layer 185. A portion of the roof material 312 and a portion of the lower insulating layer 311 may be disposed inside a recess structure of the protrusion portion. The common electrode 270 is not formed in the liquid crystal injection hole 335 portion (which corresponds to the transistor formation region); the liquid crystal injection hole 335 may be disposed between two portions of the common electrode 270, as illustrated in FIG. 3. The common electrode 270 may extend in a gate line direction (i.e., the horizontal direction).

[0194] The common electrode 270 is made of a transparent conductive material, such as ITO or IZO, and serves to generate an electric field together with the pixel electrode 192 to control an alignment direction of the liquid crystal molecules.

[0195] A lower insulating layer 311 is positioned on the common electrode 270. The lower insulating layer 311 may contain an inorganic insulating material such as silicon nitride (SiNx).

[0196] A roof layer 312 is formed on the lower insulating layer 311. The roof layer 312 may serve to support a space (microcavity 305) to be formed between the pixel electrode 192 and the common electrode 270. The roof layer 312 according to one or more embodiments serves to support the microcavity 305 above the common electrode 270 at a predetermined thickness.

[0197] An upper insulating layer 313 is formed on the roof layer 312. The upper insulating layer 313 may contain an inorganic insulating material such as silicon nitride (SiNx).

[0198] The liquid crystal injection hole 335 may be formed through the lower insulating layer 311, the roof layer 312, and the upper insulating layer 313 in the transistor formation region, wherein a liquid crystal may be injected through the liquid crystal injection hole 335 into the microcavity 305. The liquid crystal injection hole 335 may be used for removing the sacrificial layer 300 of FIG. 4 in the process of forming the microcavity 305.

[0199] The lower insulating layer 311 and the upper insulating layer 313 may be laminated with portions disposed in the transistor formation region corresponding to a position for forming the liquid crystal injection hole 335. In one or more embodiments, the roof layer 312 may not be formed in the transistor formation region; therefore, the liquid crystal injection hole 335 may be formed by removing portions of the lower insulating layer 311 and upper insulating layer 313 in the transistor formation region without removing portions of the roof layer 312. The sacrificial layer 300 may be exposed through the liquid crystal injection hole 335 after a portion of the common electrode 270 that is positioned in the transistor formation region has been removed.

[0200] According to one or more embodiments, the roof layer 312, the upper insulating layer 313, and the lower insulating layer 311 are etched in a same etching process in the transistor formation region to form the liquid crystal injection hole 335.

[0201] According to one or more embodiments, the lower insulating layer 311 and the upper insulating layer 313 may not be required.

[0202] The first black matrix 220 and the second black matrix 225 are formed on the liquid crystal layer 3, wherein the first black matrix 220 may be formed on the upper insulating layer 313, and wherein the second black matrix 225 may be formed in the transistor formation region and formed in the liquid crystal injection hole 335. The first black matrix 220 and the second black matrix 225 may be made of one or more same non-transmissive materials and may be substantially simultaneously formed in a same process step using a same mask.

[0203] The first black matrix 220 may overlap the data line 171 and may extend in a vertical direction, wherein at least a portion of one or more of the upper insulating layer 313, the roof layer 312, the lower insulating layer 311, the common electrode 270, the second passivation layer 185, and the first passivation layer 180 may be disposed between the first black matrix 220 and the data line 171. The second black matrix 225 may have a portion positioned inside the liquid crystal injection hole and may extend in a horizontal direction in the transistor formation region.

[0204] As illustrated in the plan views of FIG. 14, the first black matrix 220 (which include portions extending in the vertical direction) and the second black matrix 225 (which include portions extending in the horizontal direction) may form a lattice structure having openings. A substantial portion of the pixel electrode 192, a substantial portion of the color filter 230, and a substantial portion of the liquid crystal layer 3 may be positioned at one or more corresponding openings.

[0205] In one or more embodiments, as discussed with reference to FIGS. 1 to 7, the first black matrix 220 and the second black matrix 225 may be formed at different layers in a liquid crystal display. In one or more embodiments, as discussed with reference to FIG. 1 and FIGS. 12 to 14, the first black matrix 220 and the second black matrix 225 may be connected to each other at a same layer in a liquid crystal display.

[0206] The second black matrix 225 may seal (and/or cap) the liquid crystal injection hole 335 so that the liquid crystal layer 3 may not leak through the liquid crystal injection hole 335 after the liquid crystal layer 3 has been injected through the liquid crystal injection hole 335 into the microcavity 305.

[0207] In one or more embodiments, as illustrated in FIG. 3, a portion of the liquid crystal layer 3 may be disposed between the second passivation layer 185 and the second black matrix 225. In one or more embodiments, the second black matrix 225 may directly contact the second passivation layer 185 and thus may separate a first portion of the liquid crystal layer 3 from a second portion of the liquid crystal layer 3.

[0208] A lower polarizer (not illustrated) may be positioned below the insulation substrate 110, and an upper polarizer may be positioned above the upper insulating layer 313. Each of the polarizers may include a polarized element for generating polarization and a tri-acetyl-cellulose (TAC) layer for ensuring durability. In one or more embodiments, directions in transmissive axes of the upper polarizer and the lower polarizer may be vertical or parallel to each other.

[0209] The manufacturing method of the liquid crystal display discussed with reference to FIGS. 12 to 14 may include steps that are substantially similar to steps in the manufacturing process discussed with reference to one or more of FIGS. 1 to 7. Nevertheless, as can be appreciated from the discussion association with FIGS. 12-14, the first black matrix 220 may not be formed immediately after the formation of the color filter 230; instead, the first black matrix 220 may be formed when the second black matrix 225 is formed. Advantageously, total formation time for the first black matrix 220 and the second black matrix 225 may be minimized.

[0210] While this invention has been described in connection with what is presently considered to be practical embodiments, it is to be understood that the invention is not limited to the disclosed embodiments. The invention is intended to cover various modifications and equivalent arrangements included within the scope of the appended claims.

<Description of symbols>

110: Insulation substrate	121: Gate line
124: Gate electrode	131: Storage voltage line
140: Gate insulating layer	151,152, and 155: Semiconductor
171: Data line	173: Source electrode
175: Drain electrode	180,185: Passivation layer
186: Contact hole	192: Pixel electrode
194: Connecting member	220: First black matrix
225: Second black matrix	230: Color filter
270: Common electrode	3: Liquid crystal layer
305: Microcavity	300: Sacrificial layer
311: Lower insulating layer	312: Roof layer
313: Upper insulating layer	335: Liquid crystal injection hole
350: Capping layer	

Claims

1. A liquid crystal display device comprising:

a substrate (110);

a pixel electrode (192) disposed on the substrate (110);
a common electrode (270) overlapping the pixel electrode (192), wherein a liquid crystal injection hole (335) is formed through at least the common electrode (270);
a microcavity (305) disposed between the pixel electrode (192) and the common electrode (270); and
a liquid crystal (3) filled in the microcavity (305) through the liquid crystal injection hole (335), wherein
the pixel electrode (192), the common electrode (270) and the microcavity (305) are disposed on same substrate,
characterized in that
a first light-blocking element (225) is disposed inside the liquid crystal injection hole (335).

2. The liquid crystal display device of claim 1, further comprising:

a transistor electrically connected to the pixel electrode (192); and
a gate line (121) electrically connected to the transistor and configured to transmit a gate signal to the transistor, wherein the first light-blocking element (225) extends parallel to the gate line (121) and overlaps the transistor.

3. The liquid crystal display device of claim 1, wherein the first light-blocking element (225) is disposed between a first portion of the liquid crystal layer (3) and a second portion of the liquid crystal layer (3).

4. The liquid crystal display device of claim 1, wherein a portion of the liquid crystal layer (3) is disposed between the first light-blocking element (225) and the substrate (110).

5. The liquid crystal display device of claim 1, wherein the first light-blocking S element (225) directly contacts the liquid crystal layer (3).

6. The liquid crystal display device of claim 1, further comprising a capping layer (350) that is made of a material different from a material of the first light-blocking element (225), wherein a first portion of the capping layer (350) is disposed inside the liquid crystal injection hole (335) and is disposed between the first light-blocking element (225) and the liquid crystal layer (3).

7. The liquid crystal display device of claim 6, wherein the first light-blocking element (225) is disposed between a second portion of the capping layer (350) and a third portion of the capping layer (350).

8. The liquid crystal display device of claim 7, wherein the second portion of the capping layer (350) and the third portion of the capping layer (350) are disposed between a first portion of the common electrode (270) and a second portion of the common electrode (270).

9. The liquid crystal display device of claim 1, further comprising a second light-blocking element (220), the second light-blocking element (220) being directly connected to the first light-blocking element (225) and extending substantially perpendicular to the first light-blocking element (225).

10. The liquid crystal display device of claim 1, further comprising a second light-blocking element (220), wherein the first light-blocking element (225) is disposed at a first side with respect to the liquid crystal layer (3), and wherein the second light-blocking element (220) is disposed at a second side with respect to the liquid crystal layer (3) and extends substantially perpendicular to the first light-blocking element (225) in a plan view of the liquid crystal display device.

11. A method for manufacturing a liquid crystal display device, the method comprising:

providing a pixel electrode (192) on a substrate (110);
providing a sacrificial layer (300) on the pixel electrode (192);
providing a common electrode (270) on the sacrificial layer (300);
forming a liquid crystal injection hole (335) through at least the common electrode (270);
removing the sacrificial layer (300) through the liquid crystal injection hole (335) for forming a microcavity (305) between the pixel electrode (192) and the common electrode (270);
injecting liquid crystal through the liquid crystal injection hole (335) into the microcavity (305) for forming a liquid crystal layer (3); wherein
the pixel electrode (192), the common electrode (270) and the microcavity (305) are disposed on same substrate;
characterized in that

after the injecting, a first light-blocking element (225) is provided in the liquid crystal injection hole (335). disposed on same substrate;

12. The method of claim 11, further comprising:

    providing a photoresist pattern (PR) that partially overlaps the common electrode (270);
    using the photoresist pattern (PR) as a mask in the forming the liquid crystal injection hole (335); and
    removing the photoresist pattern (PR) when performing the removing the sacrificial layer (300).

13. The method of claim 11, further comprising:

    providing a transistor electrically that is connected to the pixel electrode (192); and
    providing a gate line (121) that is electrically connected to the transistor and is configured to transmit a gate signal to the transistor,
    wherein the first light-blocking element (225) extends parallel to the gate line (121) and overlaps the transistor.

14. The method of claim 11, further comprising: disposing the first light-blocking element (225) between a first portion of the liquid crystal layer (3) and a second portion of the liquid crystal layer (3).

15. The method of claim 11, further comprising: disposing the first light-blocking element (225) such that a portion of the liquid crystal layer (3) is disposed between the first light-blocking element (225) and the substrate (110).

Patentansprüche

1. Flüssigkristall-Anzeigevorrichtung, umfassend:

    ein Substrat (110);
    eine Pixelelektrode (192), die auf dem Substrat (110) angeordnet ist;
    eine gemeinsame Elektrode (270), welche die Pixelelektrode (192) überlappt, wobei ein Flüssigkristall-Injektionsloch (335) durch wenigstens die gemeinsame Elektrode (270) gebildet ist;
    eine Mikrokavität (305), die zwischen der Pixelelektrode (192) und der gemeinsamen Elektrode (270) angeordnet ist; und
    einen Flüssigkristall (3), der durch das Flüssigkristall-Injektionsloch (335) in die Mikrokavität (305) eingefüllt wird; wobei
    die Pixelelektrode (192), die gemeinsame Elektrode (270) und die Mikrokavität (305) auf dem gleichen Substrat angeordnet sind,
    dadurch gekennzeichnet, dass
    ein erstes lichtblockierendes Element (225) in dem Flüssigkristall-Injektionsloch (335) angeordnet ist.

2. Flüssigkristall-Anzeigevorrichtung nach Anspruch 1, ferner umfassend:

    einen Transistor, der mit der Pixelelektrode (192) elektrisch verbunden ist;
    und
    eine Gate-Leitung (121), die mit dem Transistor elektrisch verbunden ist und dafür ausgelegt ist, ein Gate-Signal zum Transistor zu übertragen, wobei sich das erste lichtblockierende Element (225) parallel zur Gate-Leitung (121) erstreckt und den Transistor überlappt.

3. Flüssigkristall-Anzeigevorrichtung nach Anspruch 1, wobei das erste lichtblockierende Element (225) zwischen einem ersten Abschnitt der Flüssigkristallschicht (3) und einem zweiten Abschnitt der Flüssigkristallschicht (3) angeordnet ist

4. Flüssigkristall-Anzeigevorrichtung nach Anspruch 1, wobei ein Abschnitt der Flüssigkristallschicht (3) zwischen dem ersten lichtblockierenden Element (225) und dem Substrat (110) angeordnet ist.

5. Flüssigkristall-Anzeigevorrichtung nach Anspruch 1, wobei das erste lichtblockierende Element (225) die Flüssigkristallschicht (3) direkt berührt.

6. Flüssigkristall-Anzeigevorrichtung nach Anspruch 1, ferner umfassend eine Verkappungsschicht (350), die aus einem Material hergestellt ist, das sich von dem Material des ersten lichtblockierenden Elements (225) unterscheidet, wobei ein erster Abschnitt der Verkappungsschicht (350) innerhalb des Flüssigkristall-Injektionslochs (335) angeordnet ist und zwischen dem ersten lichtblockierenden Element (225) und der Flüssigkristallschicht (3) angeordnet ist.

7. Flüssigkristall-Anzeigevorrichtung nach Anspruch 6, wobei das erste lichtblockierende Element (225) zwischen einem zweiten Abschnitt der Verkappungsschicht (350) und einem dritten Abschnitt der Verkappungsschicht (350) angeordnet ist.

8. Flüssigkristall-Anzeigevorrichtung nach Anspruch 7, wobei der zweite Abschnitt der Verkappungsschicht (350) und der dritte Abschnitt der Verkappungsschicht (350) zwischen einem ersten Abschnitt der gemeinsamen Elektrode (270) und einem zweiten Abschnitt der gemeinsamen Elektrode (270) angeordnet sind.

9. Flüssigkristall-Anzeigevorrichtung nach Anspruch 1, ferner umfassend ein zweites lichtblockierendes Element (220), wobei das zweite lichtblockierende Element (220) direkt mit dem ersten lichtblockierenden Element (225) verbunden ist und sich im Wesentlichen senkrecht zu dem ersten lichtblockierenden Element (225) erstreckt.

10. Flüssigkristall-Anzeigevorrichtung nach Anspruch 1, ferner umfassend ein zweites lichtblockierendes Element (220), wobei das erste lichtblockierende Element (225) an einer ersten Seite in Bezug auf die Flüssigkristallschicht (3) angeordnet ist und wobei das zweite lichtblockierende Element (220) an einer zweiten Seite in Bezug auf die Flüssigkristallschicht (3) angeordnet ist und sich in Draufsicht auf die Flüssigkristall-Anzeigevorrichtung im Wesentlichen senkreicht zu dem ersten lichtblockierenden Element (225) erstreckt.

11. Verfahren zur Herstellung einer Flüssigkristall-Anzeigevorrichtung, wobei das Verfahren Folgendes umfasst:

Bereitstellen einer Pixelelektrode (192) auf einem Substrat (110);
Bereitstellen einer Opferschicht (300) auf der Pixelelektrode (192);
Bereitstellen einer gemeinsamen Elektrode (270) auf der Opferschicht (300);
Bilden eines Flüssigkristall-Injektionslochs (335) durch wenigstens die gemeinsame Elektrode (270);
Entfernen der Opferschicht (300) durch das Flüssigkristall-Injektionsloch (335), um eine Mikrokavität (305) zwischen der Pixelelektrode (192) und der gemeinsamen Elektrode (270) zu bilden;
Injizieren von Flüssigkristall durch das Flüssigkristall-Injektionsloch (335) in die Mikrokavität (305), um eine Flüssigkristallschicht (3) zu bilden;
wobei
die Pixelelektrode (192), die gemeinsame Elektrode (270) und die Mikrokavität (305) auf dem gleichen Substrat angeordnet sind,
dadurch gekennzeichnet, dass
nach dem Injizieren ein erstes lichtblockierendes Element (225) in dem Flüssigkristall-Injektionsloch (335) bereitgestellt wird.

12. Verfahren nach Anspruch 11, ferner umfassend:

Bereitstellen eines Fotolackmusters (PR), das die gemeinsame Elektrode (270) teilweise überlappt;
Verwenden des Fotolackmusters (PR) als Maske bei der Bildung des Flüssigkristall-Injektionslochs (335); und
Entfernen des Fotolackmusters (PR), wenn die Entfernung der Opferschicht (300) durchgeführt wird.

13. Verfahren nach Anspruch 11, ferner umfassend:

Bereitstellen eines Transistors, der mit der Pixelelektrode (192) elektrisch verbunden ist; und
Bereitstellen einer Gate-Leitung (121), die mit dem Transistor elektrisch verbunden ist und dafür ausgelegt ist, ein Gate-Signal zum Transistor zu übertragen,
wobei sich das erste lichtblockierende Element (225) parallel zur Gate-Leitung (121) erstreckt und den Transistor überlappt.

14. Verfahren nach Anspruch 11, ferner umfassend: Anordnen des ersten lichtblockierenden Elements (225) zwischen einem ersten Abschnitt der Flüssigkristallschicht (3) und einem zweiten Abschnitt der Flüssigkristallschicht (3).

15. Verfahren nach Anspruch 11, ferner umfassend: Anordnen des ersten lichtblockierenden Elements (225), so dass ein Abschnitt der Flüssigkristallschicht (3) zwischen dem ersten lichtblockierenden Element (225) und dem Substrat (110) angeordnet ist.

Revendications

1. Un dispositif d'affichage à cristaux liquides comprenant :

   Un substrat (110) ;
   Une électrode de pixel (192) disposée sur le substrat (110) ;
   Une électrode commune (270) chevauchant l'électrode de pixel (192), où un trou d'injection de cristaux liquides (335) est formé au moins au travers de l'électrode commune (270) ;
   Une microcavité (305) disposée entre l'électrode de pixel (192) et l'électrode commune (270) ; et
   Un cristal liquide (3) versé dans la microcavité (305) au travers du trou d'injection de cristaux liquides (335), où L'électrode de pixel (192), l'électrode commune (270), et la microcavité (305) sont disposées sur le même substrat,
   Caractérisé en ce que
   Un premier élément bloquant la lumière (225) est disposé à l'intérieur du trou d'injection du cristal liquide (335).

2. Le dispositif d'affichage à cristaux liquides de la revendication 1, comprenant de plus :

   Un transistor électriquement connecté à l'électrode de pixel (192) ; et
   Une ligne de porte (121) électriquement connectée au transistor et configurée pour transmettre un signal de porte au transistor,
   Où le premier élément bloquant la lumière (225) s'étend de façon parallèle à la ligne de porte (121) et chevauche le transistor.

3. Le dispositif d'affichage à cristaux liquides de la revendication 1, où le premier élément bloquant la lumière (225) est disposé entre une première portion de la couche de cristaux liquides (3) et une deuxième portion de la couche de cristaux liquides (3).

4. Le dispositif d'affichage à cristaux liquides de la revendication 1, où une portion de la couche de cristaux liquides (3) est disposée entre le premier élément bloquant la lumière (225) et le substrat (110).

5. Le dispositif d'affichage à cristaux liquides de la revendication 1, où le premier élément bloquant la lumière (225) contacte directement la couche de cristaux liquides (3).

6. Le dispositif d'affichage à cristaux liquides de la revendication 1, comprenant de plus une sous-couche (350) qui est fabriquée dans un matériau différent d'un matériau du premier élément bloquant la lumière (225), où une première portion de la sous-couche (350) est disposée à l'intérieur du trou d'injection du cristal liquide (335) et est disposée entre le premier élément bloquant la lumière (225) et la couche de cristaux liquides (3).

7. Le dispositif d'affichage à cristaux liquides de la revendication 6, où le premier élément bloquant la lumière (225) est disposé entre une deuxième portion de la sous-couche (350) et une troisième portion de la sous-couche (350).

8. Le dispositif d'affichage à cristaux liquides de la revendication 7, où la deuxième portion de la sous-couche (350) et la troisième portion de la sous-couche (350) sont disposées entre une première portion de l'électrode commune (270) et une deuxième portion de l'électrode commune (270).

9. Le dispositif d'affichage à cristaux liquides de la revendication 1, comprenant de plus un deuxième élément bloquant la lumière (220), le deuxième élément bloquant la lumière (220) étant directement connecté au premier élément bloquant la lumière (225) et s'étendant substantiellement perpendiculaire au premier élément bloquant la lumière (225).

10. Le dispositif d'affichage à cristaux liquides de la revendication 1, comprenant de plus un deuxième élément bloquant la lumière (220), où le premier élément bloquant la lumière (225) est disposé sur un premier côté par rapport à la couche de cristaux liquides (3), et où le deuxième élément bloquant la lumière (220) est disposé sur un deuxième côté par rapport à la couche de cristaux liquides (3) et s'étend substantiellement perpendiculaire au premier élément

bloquant la lumière (225) dans une vue plan du dispositif d'affichage à cristaux liquides.

11. Une méthode pour fabriquer un dispositif d'affichage à cristaux liquides, la méthode comprenant :

L'apport d'une électrode de pixel (192) sur un substrat (110) ;
L'apport d'une couche sacrificielle (300) sur l'électrode de pixel (192) ;
L'apport d'une électrode commune (270) sur la couche sacrificielle (300) ;
La formation d'un trou d'injection de cristal liquide (335) au travers au moins de l'électrode commune (270) ;
Le retrait de la couche sacrificielle (300) au travers du trou d'injection de cristal liquide (335) pour former une microcavité (305) entre l'électrode de pixel (192) et
l'électrode commune (270) ;
L'injection de cristaux liquides au travers du trou d'injection de cristal liquide (335) dans la microcavité (305) pour former une couche de cristaux liquides (3) ;
où
L'électrode de pixel (192), l'électrode commune (270) et la microcavité (305) sont disposées sur le même substrat ;
Caractérisée en ce que
Après l'injection, un premier élément bloquant la lumière (225) est fourni dans le trou d'injection de cristal liquide (335).

12. La méthode de la revendication 11, comprenant de plus :

L'apport d'un modèle en résine photosensible (PR) qui chevauche partiellement l'électrode commune (270) ;
Utilisant le modèle en résine photosensible (PR) comme un masque dans la formation du trou d'injection du cristal liquide (335) ; et
Le retrait du modèle en résine photosensible (PR) lors de la réalisation du retrait de la couche sacrificielle (300).

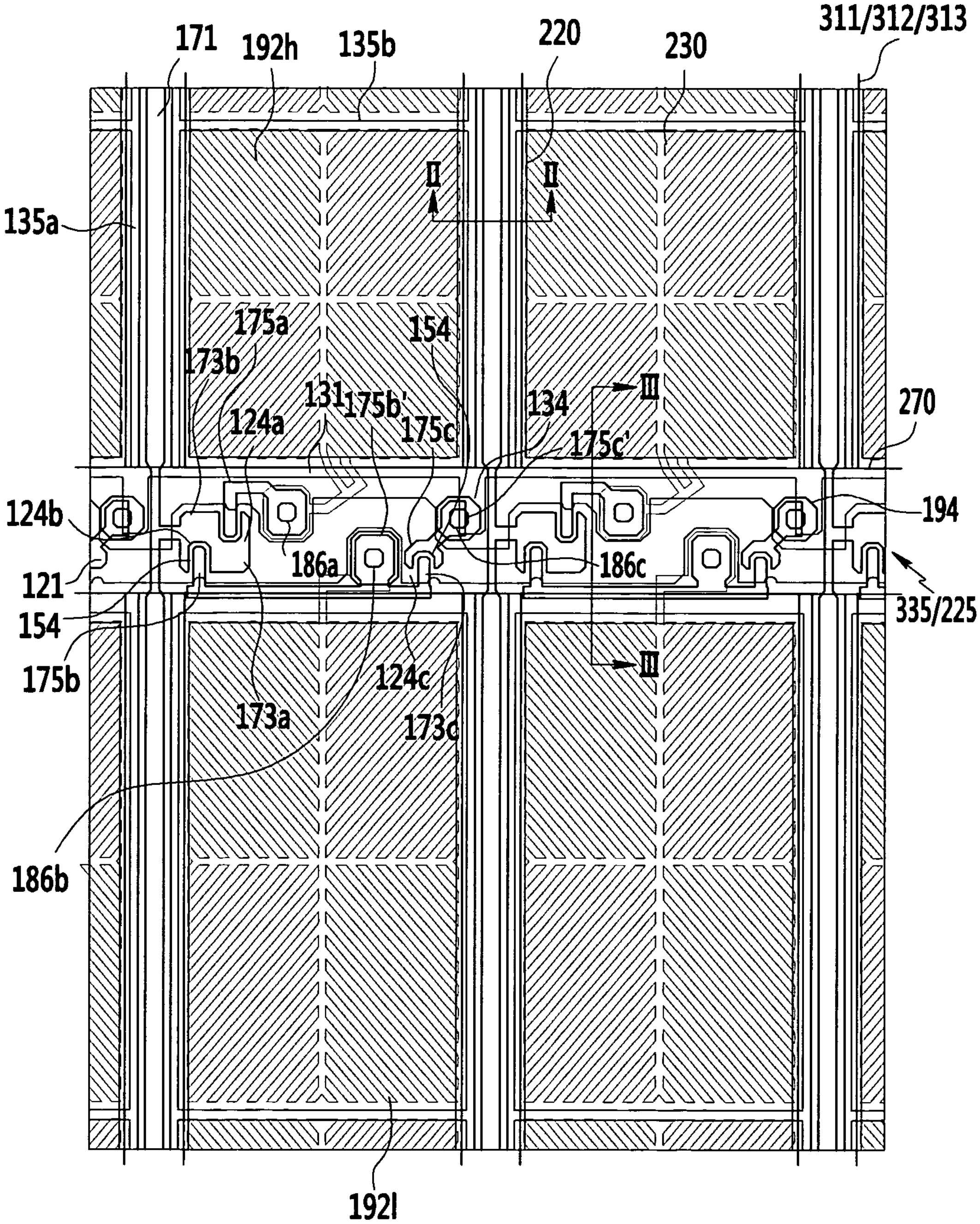
13. La méthode de la revendication 11, comprenant de plus :

L'apport d'un transistor électriquement connecté à l'électrode de pixel (192) ;
Et
L'apport d'une ligne de porte (121) qui est électriquement connectée au transistor et qui est configurée pour transmettre un signal de porte au transistor,
Où le premier élément bloquant la lumière (225) s'étend parallèlement à la ligne de porte (121) et chevauche le transistor.

14. La méthode de la revendication 11, comprenant de plus : la disposition du premier élément bloquant la lumière (225) entre une première portion de la couche de cristaux liquides (3) et une deuxième portion de la couche de cristaux liquides (3).

15. La méthode de la revendication 11, comprenant de plus: la disposition du premier élément bloquant la lumière (225) de façon à ce qu'une portion de la couche de cristaux liquides (3) est disposée entre le premier élément bloquant la lumière (225) et le substrat (110).

FIG. 1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220
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II
II
175a
154
173b
131
175b'
134
III
270
124a
175c
175c'
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194
121
186a
186c
335/225
154
175b
124c
173a
173c
III
186b
192l

FIG. 2

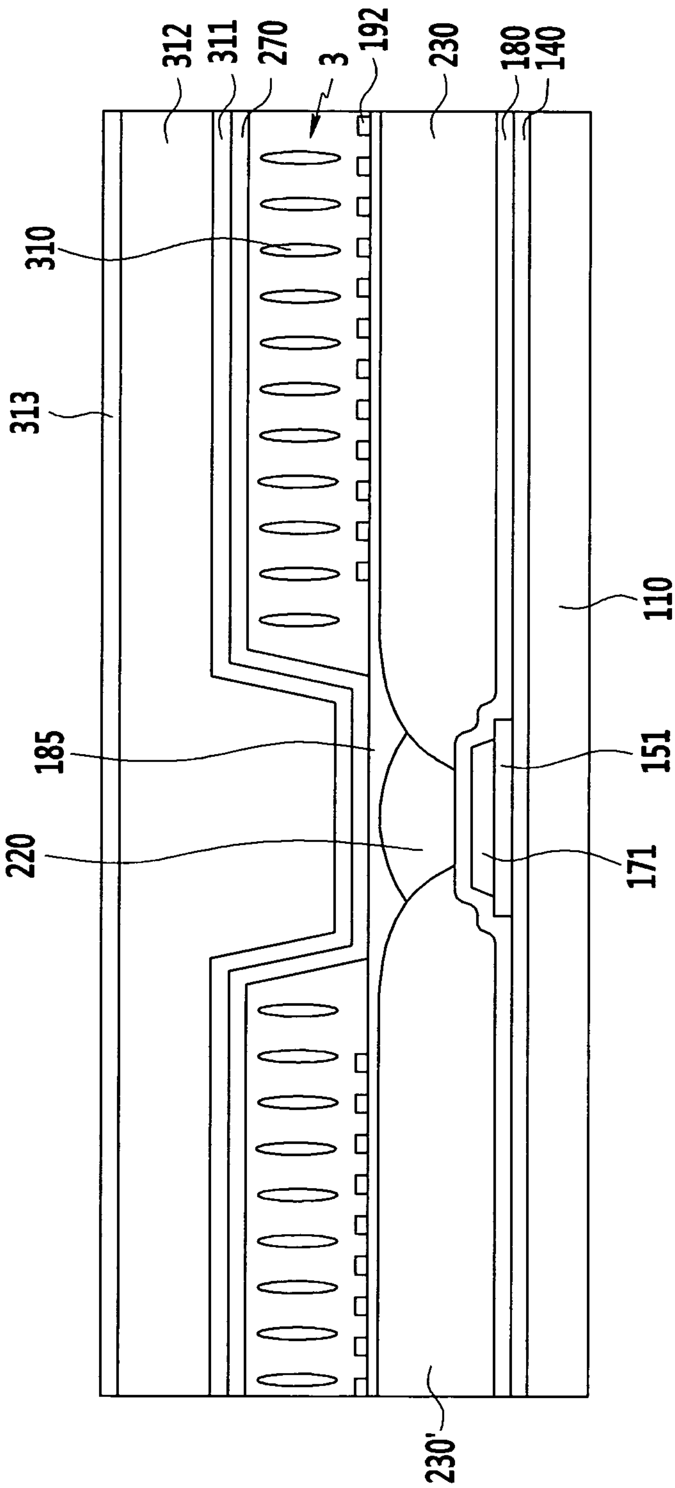
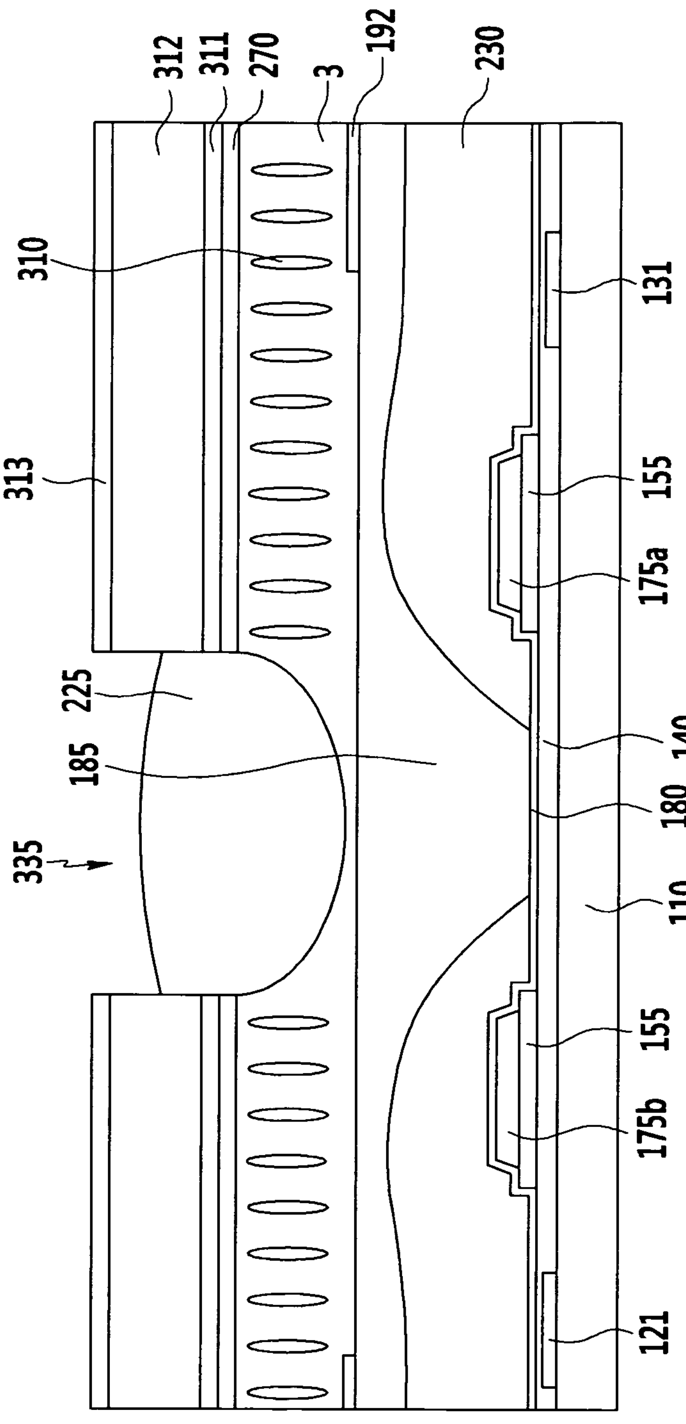


FIG. 3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175b
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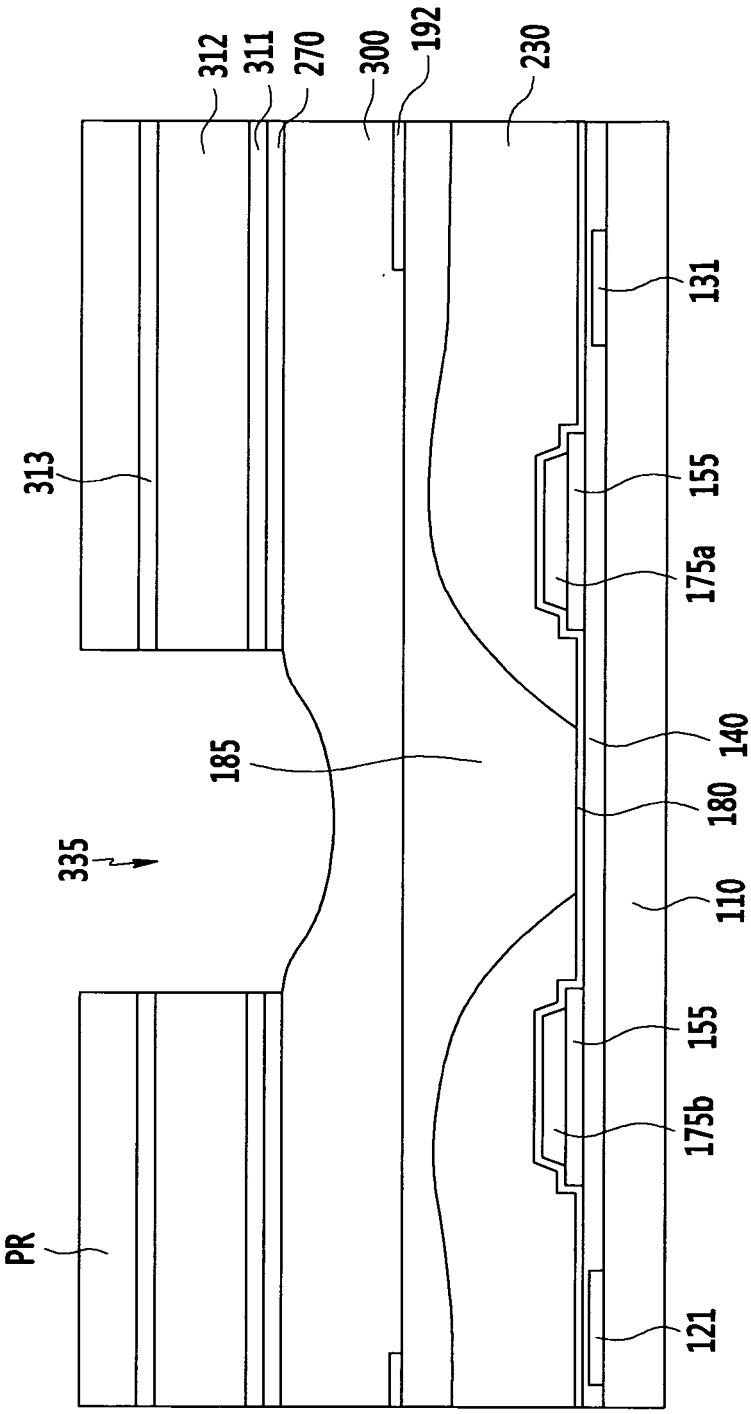
FIG. 4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PR
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FIG. 5

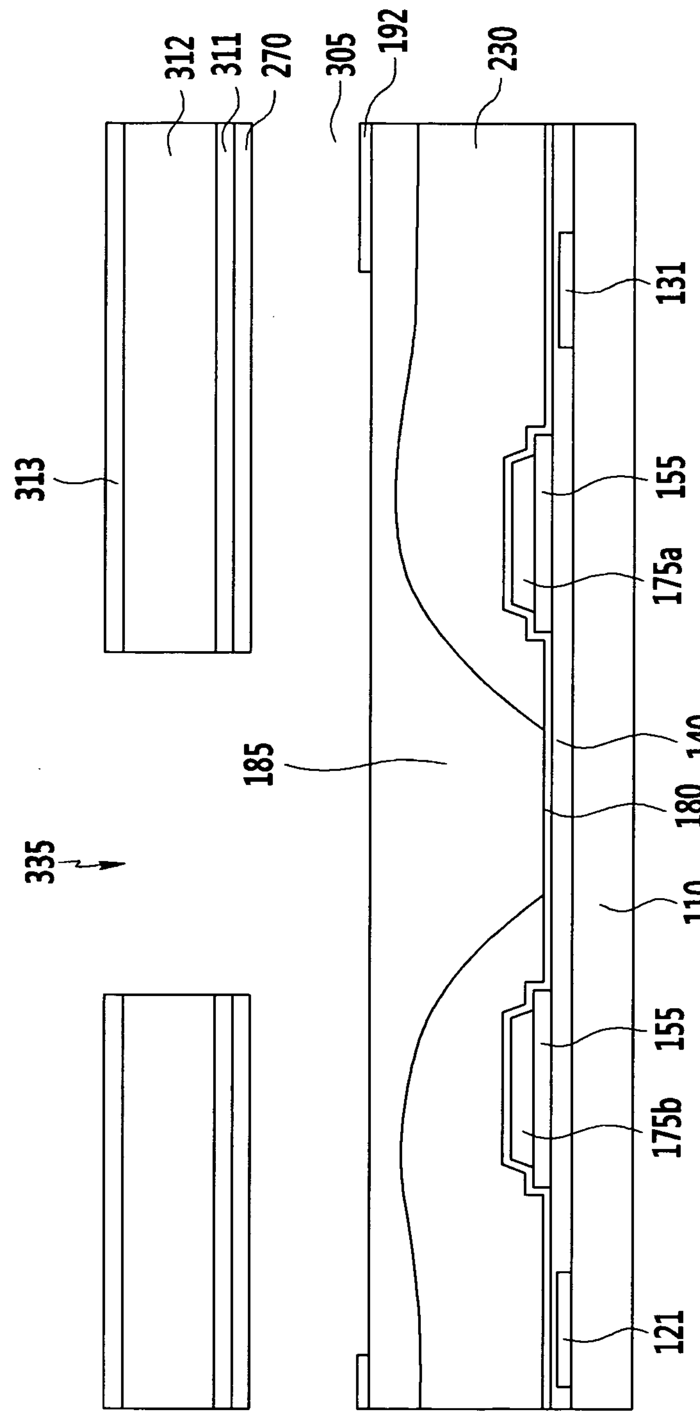
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FIG. 6

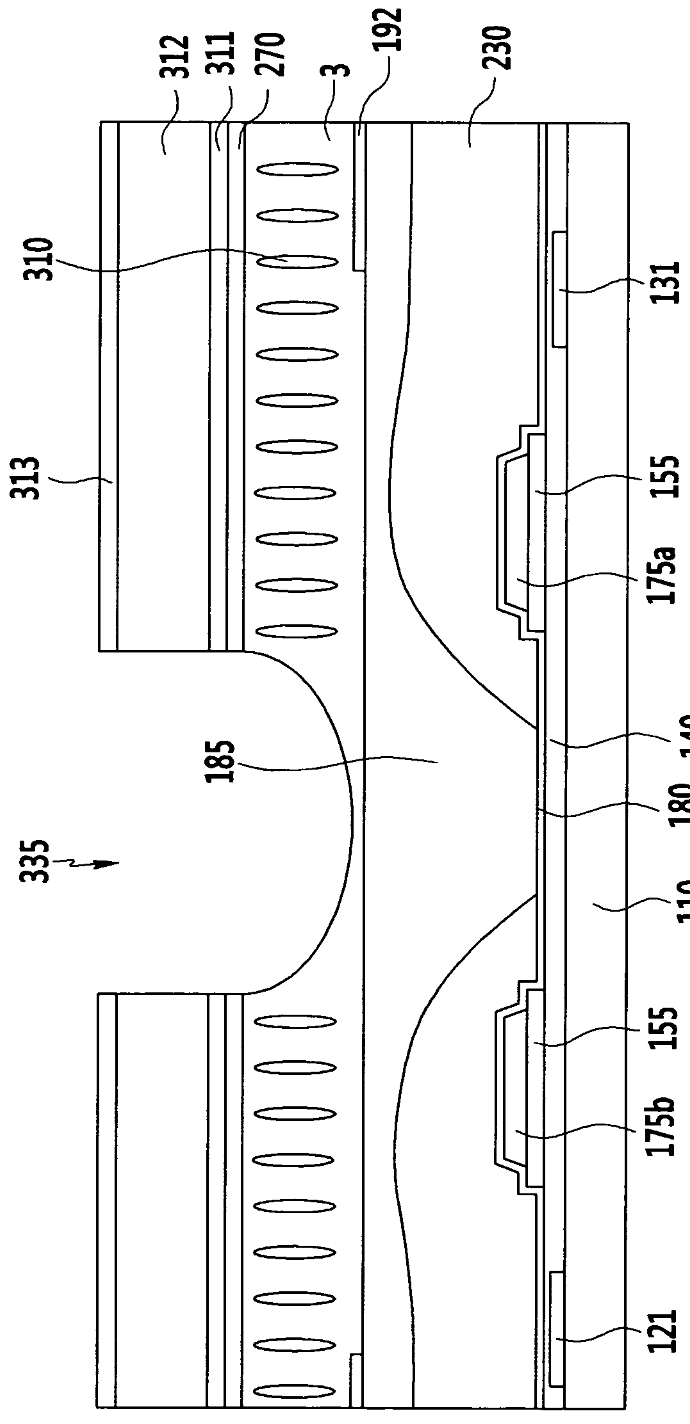
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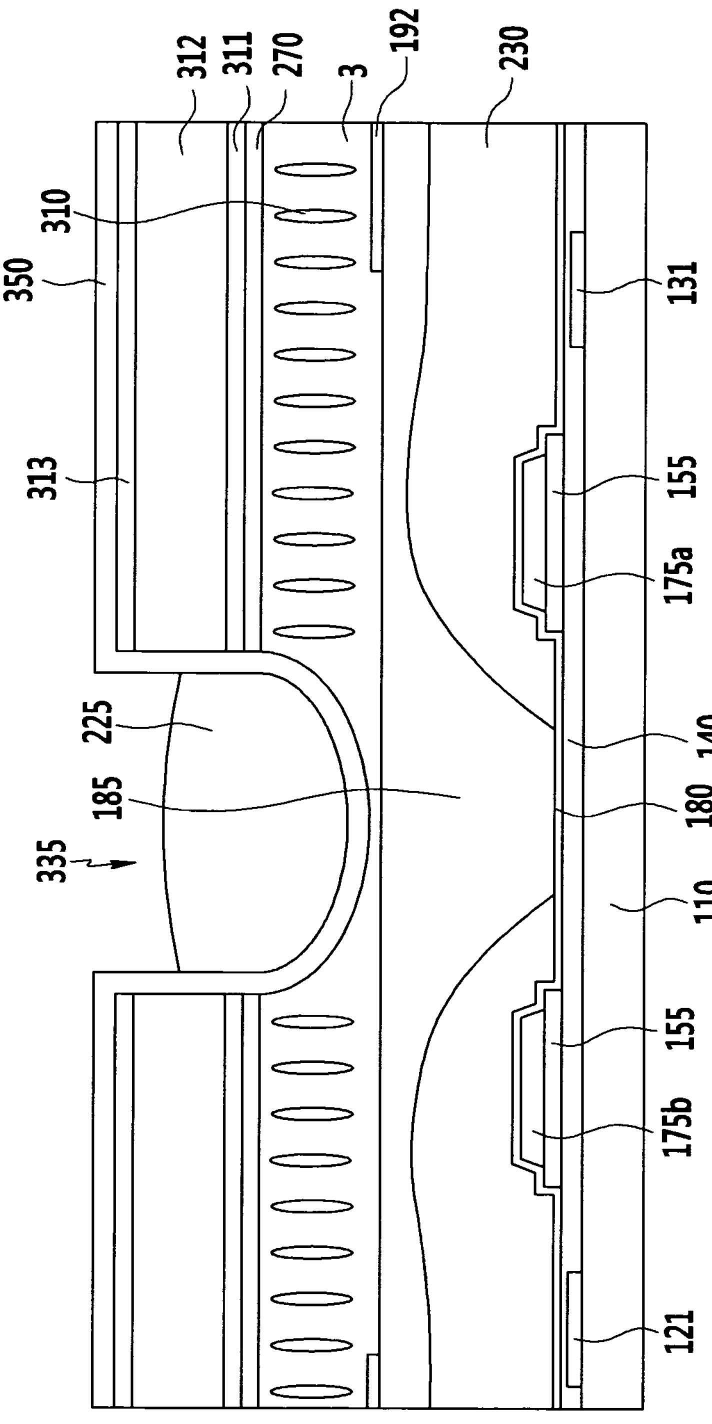
FIG. 7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121

FIG. 8

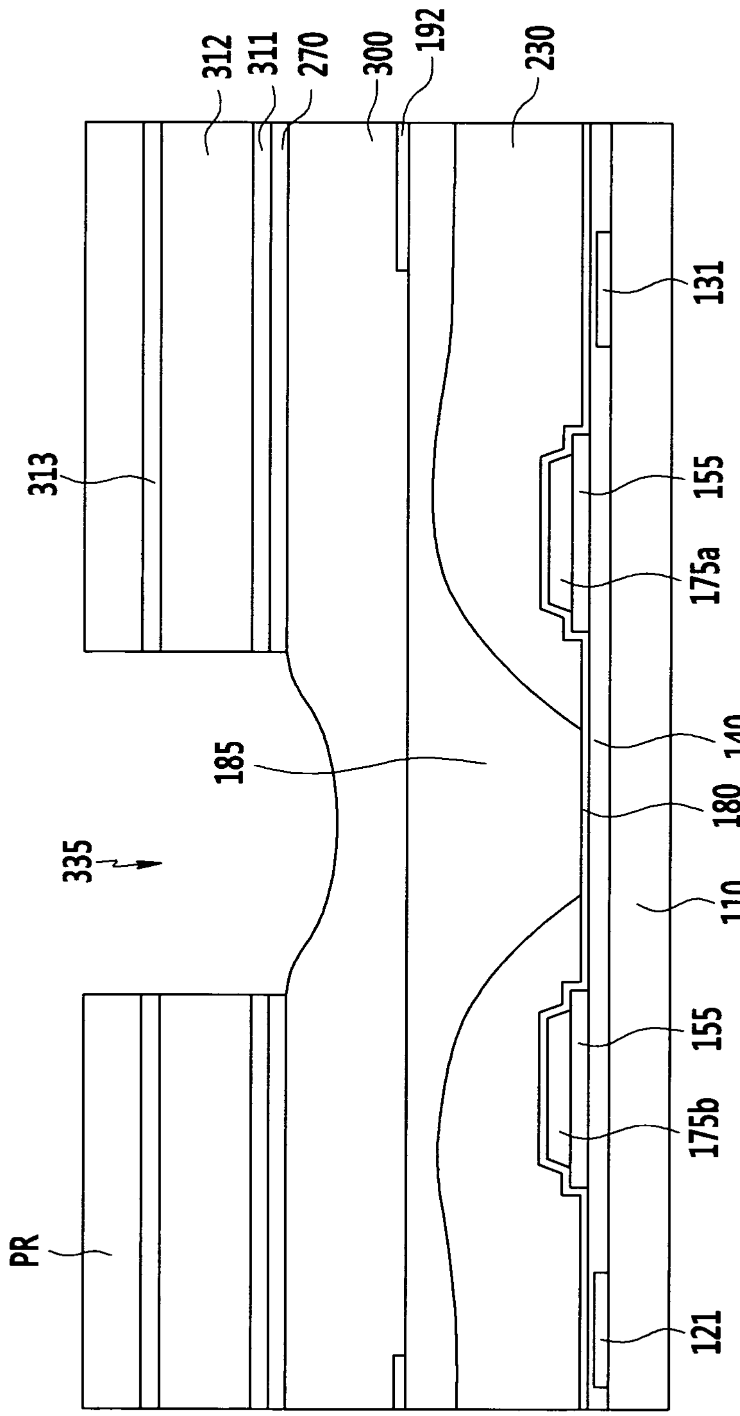
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FIG. 9

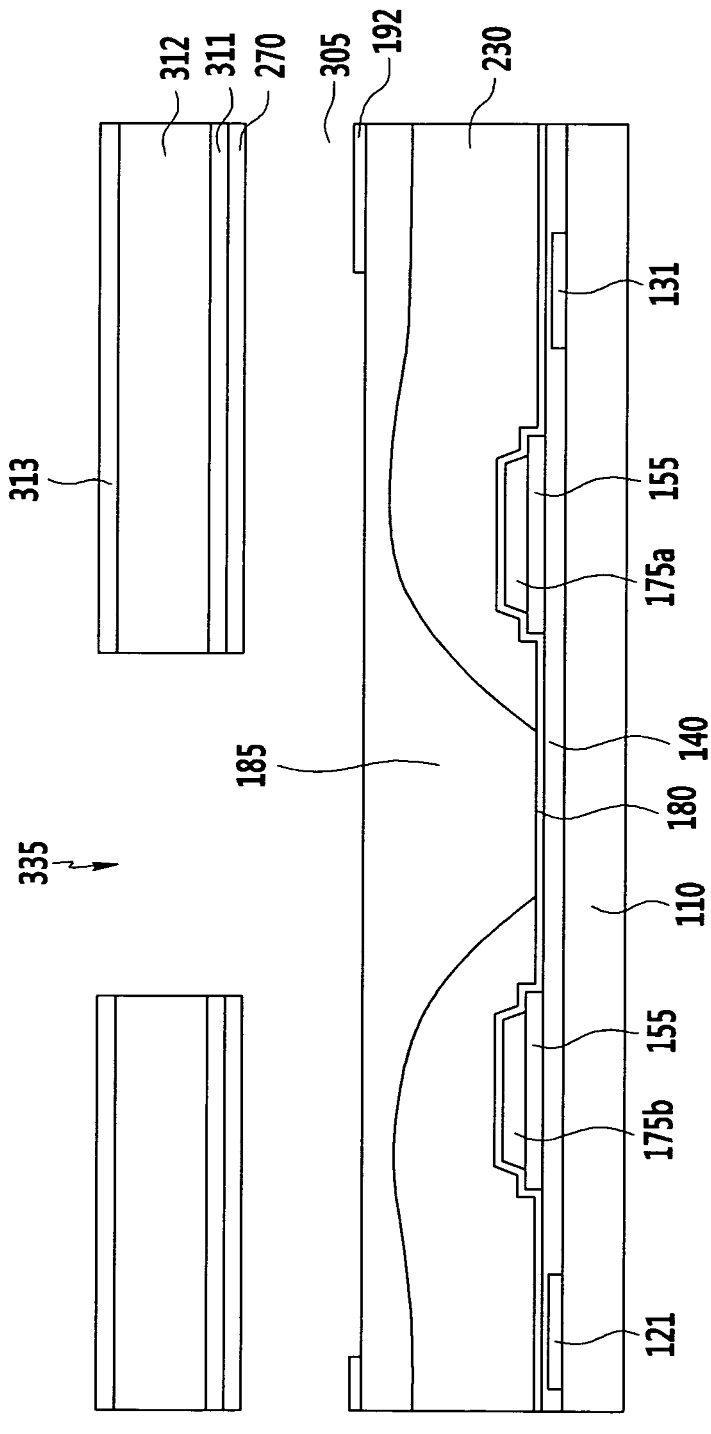
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FIG. 10

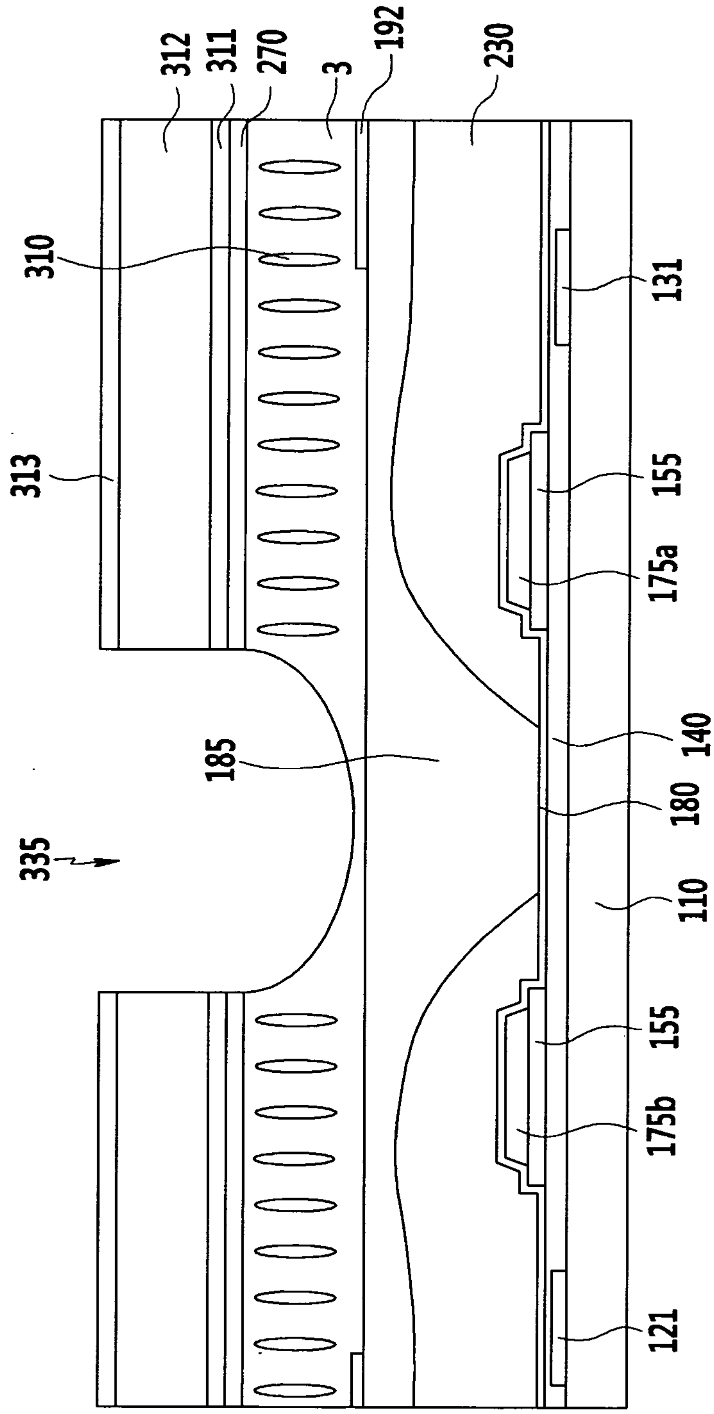
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FIG. 11

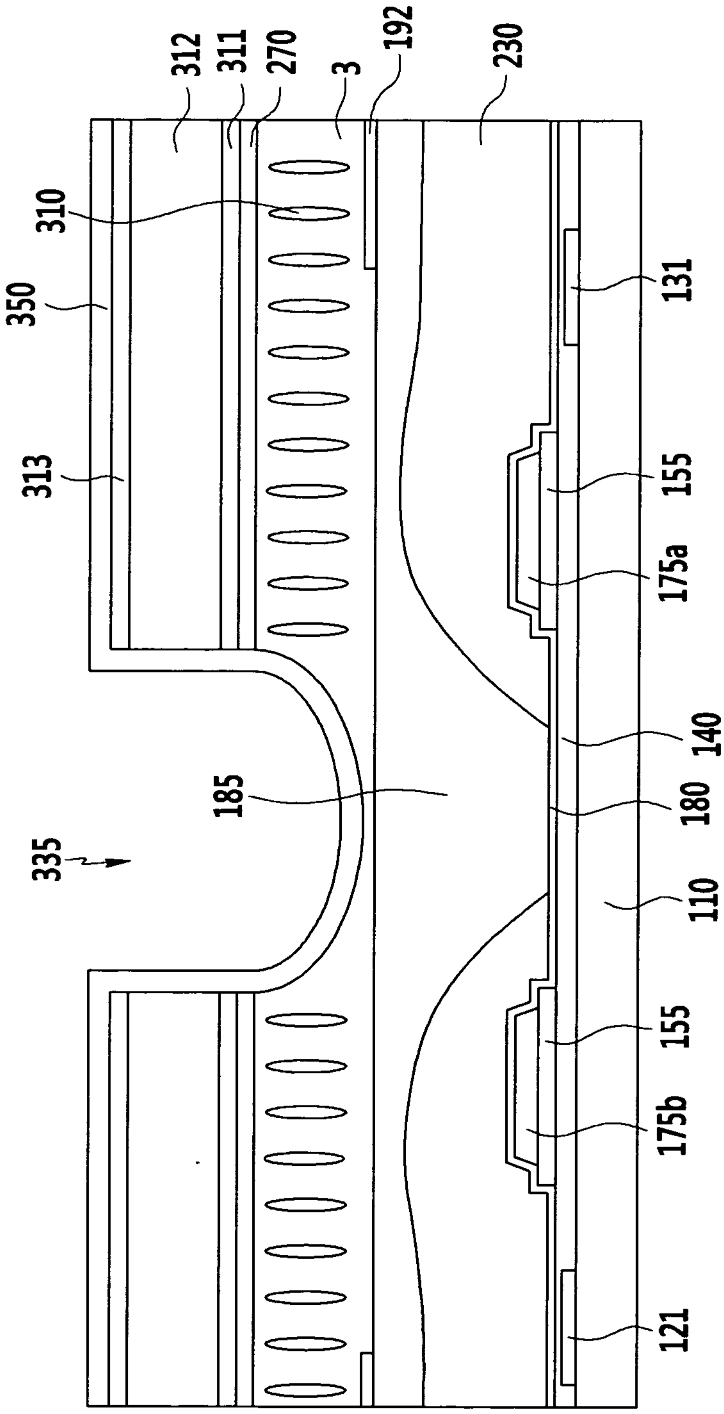
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FIG. 12

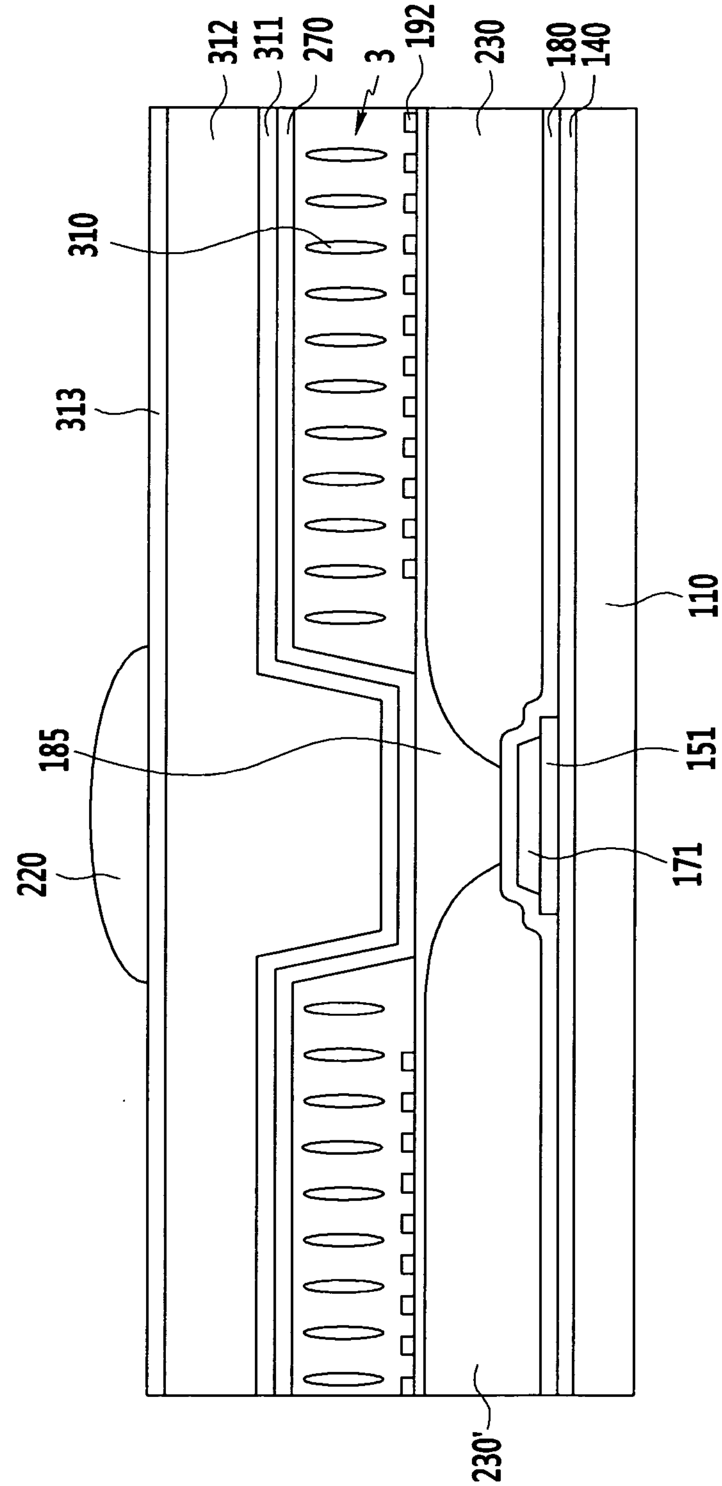

FIG. 13

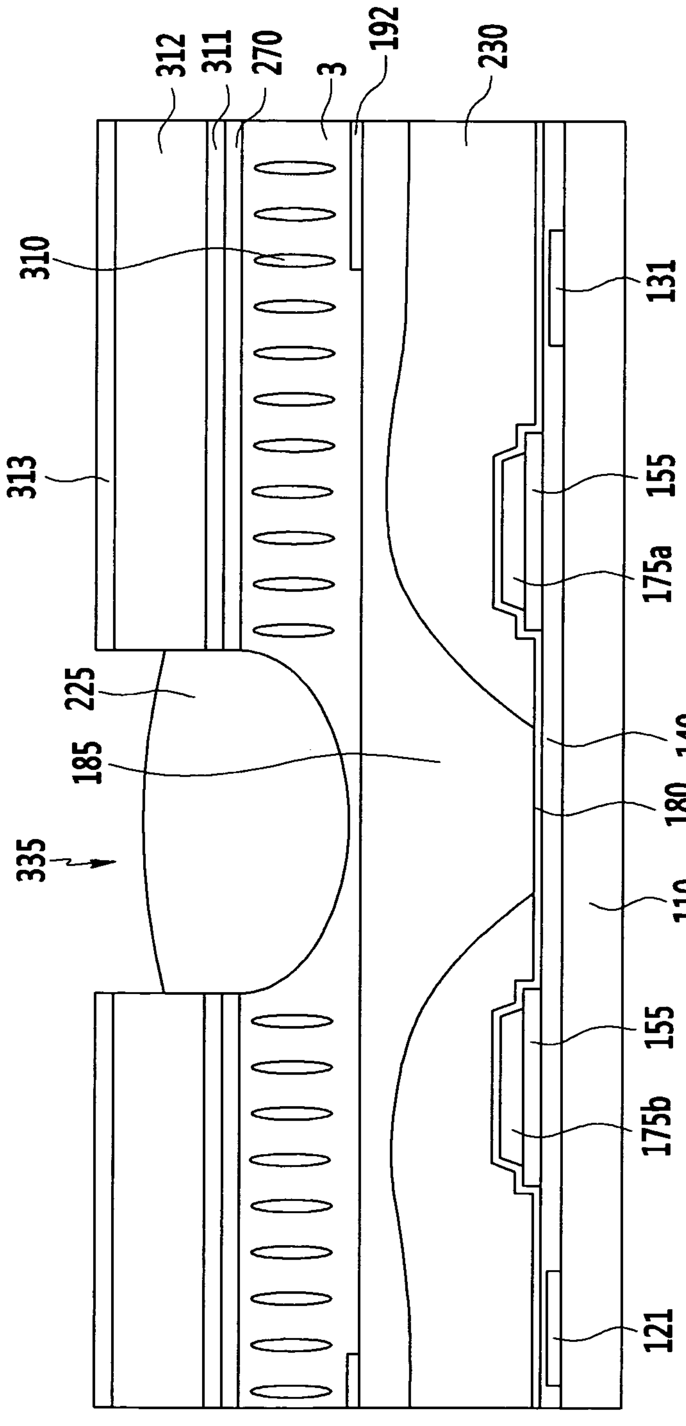
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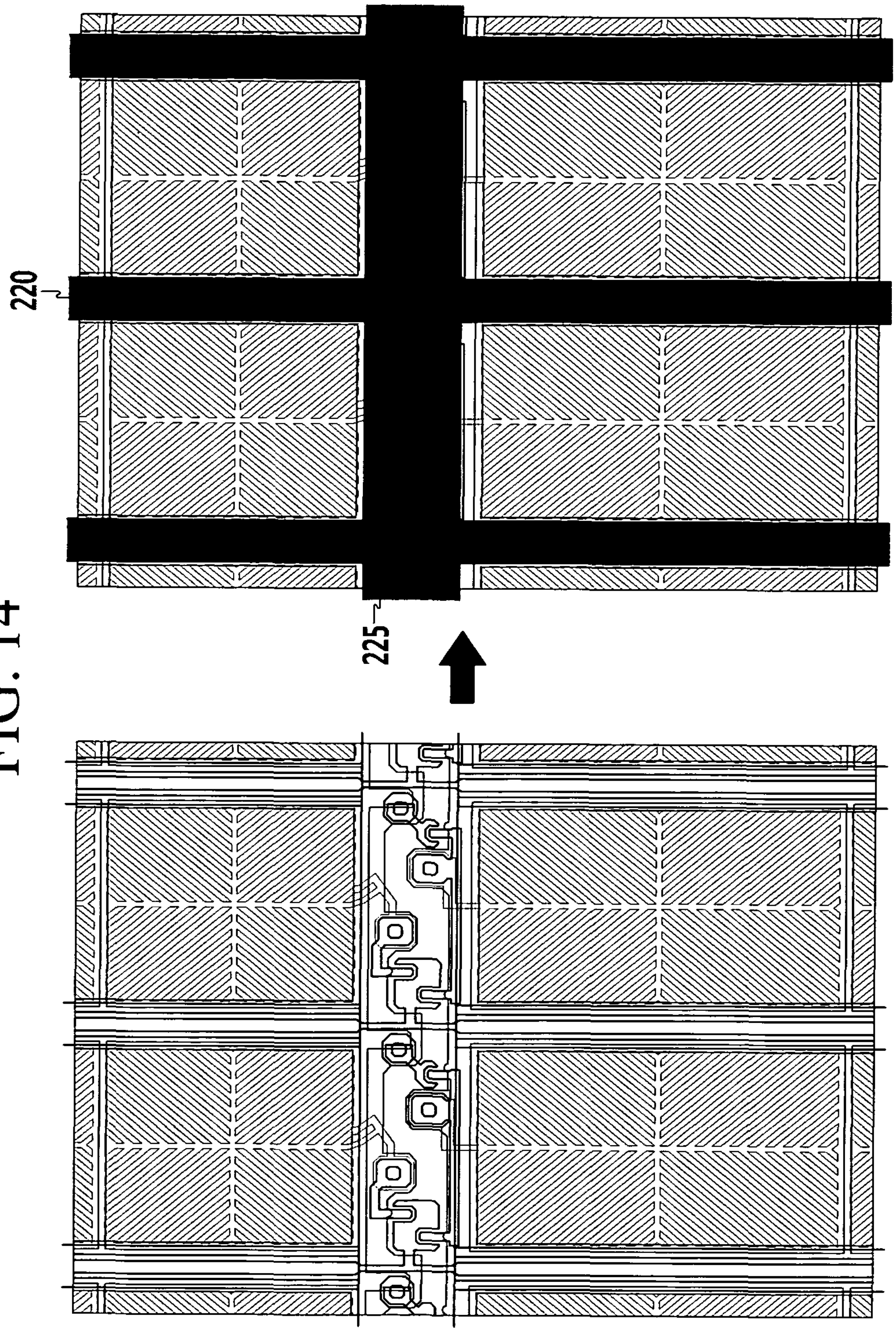
FIG. 14



REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- EP 0294900 A **[0005]**

专利名称(译)	液晶显示器及其制造方法		
公开(公告)号	EP2728402B1	公开(公告)日	2016-07-06
申请号	EP2013160558	申请日	2013-03-22
[标]申请(专利权)人(译)	三星显示有限公司		
申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
当前申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
[标]发明人	HONG KI PYO KIM SWAE HYUN PARK JAE HWA PARK JE HYEONG SONG YOUNG GOO		
发明人	HONG, KI PYO KIM, SWAE-HYUN PARK, JAE HWA PARK, JE HYEONG SONG, YOUNG GOO		
IPC分类号	G02F1/1341 G02F1/1335 G02F1/1362		
CPC分类号	G02F1/1333 G02F1/133377 G02F1/1341 G02F1/136209 G02F1/133512		
代理机构(译)	DR.威猛和合作伙伴		
优先权	1020120124720 2012-11-06 KR		
其他公开文献	EP2728402A1		
外部链接	Espacenet		

摘要(译)

在像素电极（192）和公共电极（270）之间具有液晶层（3）的液晶显示装置，其具有光阻挡元件（225），该光阻挡元件设置在通过所述液晶注入孔（335）形成的液晶注入孔（335）内部。公共电极（270）。

FIG. 1