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(54) **Liquid crystal display device**

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Dispositif d'affichage à cristaux liquides

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EP 2 407 823 B1

Description

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

[0001] Exemplary embodiments of the present invention relate to a liquid crystal display device (LCD). More particularly, exemplary embodiments of the present invention relate to an LCD capable of preventing light from being leaked.

DISCUSSION OF THE BACKGROUND

[0002] An LCD device is one of the most widely used types of flat panel display devices. The LCD device includes a display substrate on which electric field generating electrodes such as a first pixel electrode and a second pixel electrode are formed and an opposite substrate opposite to the display substrate. Moreover, the LCD device includes a liquid crystal (LC) layer interposed between the display substrate and the opposite substrate.

[0003] The LCD device displays images by applying voltages to the electric field generating electrodes to generate an electric field in the LC layer, which controls an orientation of LC molecules in the LC layer to affect a polarization of light passing therethrough.

[0004] The LC molecules of the LC layer may be operated in a vertical alignment (VA) mode due to an electric field formed between the first pixel electrode and the second pixel electrode. For example, the LCD panel displays a black image when the electric field is not formed between the first and second pixel electrodes, and the LCD panel displays images of various gradations when a horizontal electric field is formed between the first and second pixel electrodes.

[0005] However, since different voltages are applied to a first pixel part, which includes the first pixel electrode and the second pixel electrode, and a second pixel part formed adjacent to the first pixel part, light leakage may be generated between the first pixel part and the second pixel part.

[0006] US 2010/103085 A1 discloses a horizontal electric field LCD device wherein the in-plane pixel and counter electrodes of each pixel are both actively driven by respective thin film transistors in order to compensate a voltage level shift while driving the LCD with a dot inversion driving scheme. The counter pixel electrodes of neighboured pixels of a row are both connected to a data line Dj centred between adjacent data lines Dj-1 and Dj+1 to which the respective pixel electrodes of said neighboured pixels are connected. Dot inversion is achieved in US 2010/103085 A1 by frame-wise inverting the polarity of the data lines Dj-1 and Dj+1 relative to the constant reference potential applied via the intermediate data power line Dj to the counter electrodes of directly adjacent pixels in a row.

[0007] US 2006/290863 A1 discloses an in-plane-switching LCD device wherein the in-plane pixel and counter electrodes of a pixel are both actively driven by respective thin film transistors in order to minimise flicker caused by the voltage level shift while driving the LCD with a conventional dot inversion driving scheme wherein the polarity of the data signals are frame-wise inverted.

[0008] US 2009/262061 A1 discloses another in-plane-switching LCD device with a dot inversion driving scheme involving two common voltage bus lines set to common potentials of mutually opposite polarities, the counter electrodes of the pixels of the same row being alternately connected to the two common voltage bus lines so that the polarity of the counter electrodes alternates along the pixel rows. The counter electrodes are not actively switched, and the common voltage bus lines extend in a meander-form in the row direction.

SUMMARY OF THE INVENTION

[0009] Exemplary embodiments of the present invention provide a liquid crystal display (LCD) device capable of preventing light from being leaked.

[0010] Additional features of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention.

[0011] An exemplary embodiment of the present invention discloses an LCD device according to appended independent claim 1.

[0012] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention, and together with the description serve to explain the principles of the invention.

[0014] FIG. 1 is a plan view illustrating a liquid crystal display ("LCD") device according to an exemplary embodiment of the present invention.

[0015] FIG. 2 is a schematic diagram of the LCD panel of FIG. 1.

[0016] FIG. 3 is a plan view illustrating the LCD panel of FIG. 1.

[0017] FIG. 4 is a cross-sectional view taken along line I-I' of FIG. 3.

[0018] FIG. 5A, FIG. 5B, FIG. 5C and FIG. 5D are plan views explaining a method of manufacturing the display substrate of FIG. 4.

[0019] FIG. 6 is a plan view illustrating an LCD panel according to another exemplary embodiment of the present invention.

[0020] FIG. 7 is a cross-sectional view taken along line II-II' of FIG. 6.

[0021] FIG. 8A, FIG. 8B, FIG. 8C and FIG. 8D are plan views explaining a method of manufacturing the display substrate of FIG. 7.

[0022] FIG. 9 is a schematic diagram illustrating an LCD panel according to another exemplary embodiment of the present invention.

[0023] FIG. 10 is a plan view showing the LCD panel of FIG. 9.

[0024] FIG. 11 is a cross-sectional view taken along line III-III' of FIG. 9.

[0025] FIG. 12A, FIG. 12B and FIG. 12C are plan views explaining a method of manufacturing the display substrate of FIG. 11;

[0026] FIG. 13 is a schematic diagram illustrating an LCD panel according to another exemplary embodiment of the present invention.

[0027] FIG. 14 is a plan view showing the LCD panel of FIG. 13.

[0028] FIG. 15 is a plan view showing an LCD panel according to another exemplary embodiment of the present invention.

[0029] FIG. 16 is a schematic diagram illustrating an LCD panel according to another exemplary embodiment of the present invention.

[0030] FIG. 17 is a plan view illustrating the LCD panel of FIG. 16.

[0031] FIG. 18 is a schematic diagram illustrating an LCD panel according to another exemplary embodiment of the present invention.

[0032] FIG. 19 is a schematic diagram illustrating an LCD panel according to another exemplary embodiment of the present invention.

[0033] FIG. 20 is a schematic diagram illustrating an LCD panel according to another exemplary embodiment of the present invention.

[0034] FIG. 21 is a schematic diagram illustrating an LCD panel according to another exemplary embodiment of the present invention.

[0035] FIG. 22 is a schematic diagram illustrating an LCD panel not according to the present invention.

[0036] FIG. 23 is a plan view illustrating the LCD panel of FIG. 22.

[0037] FIG. 24 is a cross-sectional view taken along line IV-IV' of FIG. 23.

[0038] FIG. 25 is a plan view illustrating an LCD panel not according to the present invention.

[0039] FIG. 26 is a plan view illustrating an LCD panel not according to the present invention.

[0040] FIG. 27 is a plan view illustrating an LCD panel not according to the present invention.

[0041] FIG. 28 is a plan view illustrating an LCD panel not according to the present invention.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

[0042] The invention is described more fully hereinafter with reference to the accompanying drawings, in which embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure is thorough, and will fully convey the scope of the invention to those skilled in the art. In the drawings, the size and relative sizes of layers and regions may be exaggerated for clarity. Like reference numerals in the drawings denote like elements.

[0043] It will be understood that when an element or layer is referred to as being "on" or "connected to" another element or layer, it can be directly on or directly connected to the other element or layer, or intervening elements or layers may be present. In contrast, when an element or layer is referred to as being "directly on" or "directly connected to" another element or layer, there are no intervening elements or layers present.

[0044] Hereinafter, the present invention will be explained in detail with reference to the accompanying drawings.

[0045] FIG. 1 is a plan view illustrating a liquid crystal display ("LCD") device according to an exemplary embodiment of the present invention.

[0046] Referring to FIG. 1, the LCD device includes an LCD panel 1000, a gate driving part 1010 for driving the LCD panel 1000 and a data driving part 1030 for driving the LCD panel 1000.

[0047] The LCD panel 1000 includes a display substrate 100, an opposite substrate 200 (i.e., a color filter substrate) coupled with the display substrate 100, and a liquid crystal (not shown) disposed between the display substrate 100 and the opposite substrate 200. In this case, the LCD panel 1000 may include a display area DA, a first peripheral area PA1 and a second peripheral area PA2. The first and second peripheral areas PA1 and PA2 border perimeters of and may surround the display area DA.

[0048] A data line DL transmitting a data signal and a gate line GL transmitting a gate signal are formed in the display area DA. The data line DL is extended in a first direction DI1, and the gate line GL is extended in a second direction DI2 crossing the first direction DI1.

[0049] In this case, the first peripheral area PA1 is positioned at a first end portion of the data line DL, and the second peripheral area PA2 is positioned at a first end portion of the gate line GL. In FIG. 1, the second peripheral area PA2 is disposed at a left side of the display area DA when viewed on a plan view. Alternatively, the second peripheral area PA2 may be disposed at a right side of the display area DA.

[0050] The gate driving part 1010 includes a shift register in which plural stages are connected one after another to each other, and sequentially outputs the gate

signal to the gate lines GLs. In this case, the gate driving part 1010 includes at least one gate driving chip 1011. The gate driving part 1010 is formed on the second peripheral area PA2. Alternatively, the gate driving part 1010 may include a plurality of thin-film transistors formed at the second peripheral area PA2 by a manufacturing process identical to a process for forming a thin-film transistor formed in the display area DA. That is, the gate driving part 1010 may be integrated on the second peripheral area PA2 of the display panel 1000 without the gate line driving chip. Thus, a mounting space for components is not required, so that a slim type display device may be realized.

[0051] Moreover, the gate driving chip 1011 may be attached on a tape carrier package (TCP) positioned between a printed circuit board (not shown) and an LCD panel 1000.

[0052] The data driving part 1030 outputs an analog type data signal to the data line DL in synchronization with the gate signal. The data driving part 1030 may include at least one data driving chip 1031.

[0053] The data driving chip 1031 may be directly attached on the first peripheral area PA1 of the LCD panel 1000 in a chip on glass ("COG") type panel. The data driving chips 1031 may be mounted on a flexible film 1070, and then may be attached on the LCD panel 1000. The flexible film 1070 may include a power line 1050. The power line 1050 may deliver voltages applied to a first bus line and a second line. Moreover, the power line 1050 may deliver voltage provided to the gate driving part 1010.

[0054] FIG. 2 is a schematic diagram illustrating the LCD panel 1000 of FIG. 1.

[0055] Referring to FIGS. 1 and 2, the LCD panel 1000 includes a pad part 400, a plurality of data lines DL1, DL2, DL3, DL4, DL5 and DL6, a first bus line BL1, a second bus line BL2, a first power line VL1, a second power line VL2, a gate line GL and a plurality of pixel parts P1, P2, P3, P4, P5, P6 and P7.

[0056] The pad part 400 includes plural pads 410, 420, 430, 440, 450 and 460 receiving plural data voltages outputted from the data driving part 1030, respectively. A first pad 410 is connected to a first data line DL1, a second pad 420 is connected to a second data line DL2, and a third pad 430 is connected to a third data line DL3. A fourth pad 440 is connected to a fourth data line DL4, a fifth pad 450 is connected to a fifth data line DL5, and a sixth pad 460 is connected to a sixth data line DL6.

[0057] The first to sixth data lines DL1, DL2, DL3, DL4, DL5 and DL6 are extended in the first direction DI1, and are arranged in the second direction D12.

[0058] The first bus line BL1 may be extended in the second direction DI2 to be disposed on the first peripheral area PA1. The second bus line BL2 may be extended in the second direction DI2 to be disposed on the first peripheral area PA1 adjacent to the first bus line BL1.

[0059] The first power line VL1 is connected to the first bus line BL1 to be extended in the first direction DI1. The second power line VL2 is connected to the second bus line BL2 to be extended in the first direction DI1. A plurality of pixel parts P4, P5 and P6 is arranged between the first and second power lines VL1 and VL2. Each of the first and second power lines VL1 and VL2 provides voltage to a plurality of pixel parts P1, P2 and P3, and P4, P5 and P6, respectively.

[0060] The gate line GL is extended in the second direction DI2.

[0061] The plural pixel parts P1, P2, P3, P4, P5 and P6 include primary color pixels. The primary color pixels may be a red pixel, a green pixel and a blue pixel.

[0062] A first pixel part P1 includes a first pixel electrode PE1, a second pixel electrode PE2, a first switching element T1 and a second switching element T2. The first pixel electrode PE1 is connected to the first data line DL1 and the gate line GL through the first switching element T1. The second pixel electrode PE2 is spaced apart from the first pixel electrode PE1 to be connected to the first power line VL1 and the gate line GL through the second switching element T2. The second switching element T2 is connected to the first power line VL1 through a first connection line CL1. A polarity of a voltage applied to the first pixel electrode PE1 and a polarity of a voltage applied to the second pixel electrode PE2 may be opposite to each other with respect to a reference voltage. For example, when a polarity of a voltage applied to the first pixel electrode PE1 is positive with respect to the reference voltage, a polarity of a voltage applied to the second pixel electrode PE2 may be negative.

[0063] A second pixel part P2 includes a third pixel electrode PE3, a fourth pixel electrode PE4, a third switching element T3 and a fourth switching element T4. The third pixel electrode PE3 is connected to the second data line DL2 and the gate line GL through the third switching element T3. The fourth pixel electrode PE4 is spaced apart from the third pixel electrode PE3 to be connected to the first power line VL1 and the gate line GL through the fourth switching element T4. The fourth switching element T4 is connected to the first power line VL1 through the first connection line CL1. A polarity of a voltage applied to the third pixel electrode PE3 and a polarity of a voltage applied to the fourth pixel electrode PE4 may be opposite to each other with respect to a reference voltage.

[0064] A third pixel part P3 includes a fifth pixel electrode PE5, a sixth pixel electrode PE6, a fifth switching element T5 and a sixth switching element T6. The fifth pixel electrode PE5 is connected to the third data line DL3 and the gate line GL through the fifth switching element T5. The sixth pixel electrode PE6 is spaced apart from the fifth pixel electrode PE5 to be connected to the first power line VL1 and the gate line GL through the sixth switching element T6. The sixth switching element T6 is connected to the first power line VL1 through the first connection line CL1. A polarity of a voltage applied to the fifth pixel electrode PE5 and a polarity of a voltage applied to the sixth pixel electrode PE6 may be opposite to each

other with respect to a reference voltage.

[0065] A fourth pixel part P4 includes a seventh pixel electrode PE7, an eighth pixel electrode PE8, a seventh switching element T7 and an eighth switching element T8. The seventh pixel electrode PE7 is connected to the fourth data line DL4 and the gate line GL through the seventh switching element T7. The eighth pixel electrode PE8 is spaced apart from the seventh pixel electrode PE7 to be connected to the second power line VL2 and the gate line GL through the eighth switching element T8. The eighth switching element T8 is connected to the second power line VL2 through a second connection line CL2. A polarity of a voltage applied to the seventh pixel electrode PE7 and a polarity of a voltage applied to the eighth pixel electrode PE8 may be opposite to each other with respect to a reference voltage.

[0066] A fifth pixel part P5 includes a ninth pixel electrode PE9, a tenth pixel electrode PE10, a ninth switching element T9 and a tenth switching element T10. The ninth pixel electrode PE9 is connected to the fifth data line DL5 and the gate line GL through the ninth switching element T9. The tenth pixel electrode PE10 is spaced apart from the ninth pixel electrode PE9 to be connected to the second power line VL2 and the gate line GL through the tenth switching element T10. The tenth switching element T10 is connected to the second power line VL2 through the second connection line CL2. A polarity of a voltage applied to the ninth pixel electrode PE9 and a polarity of a voltage applied to the tenth pixel electrode PE10 may be opposite to each other with respect to a reference voltage.

[0067] A sixth pixel part P6 includes an eleventh pixel electrode PE11, a twelfth pixel electrode PE12, an eleventh switching element T11 and a twelfth switching element T12. The eleventh pixel electrode PE11 is connected to the sixth data line DL6 and the gate line GL through the eleventh switching element T11. The twelfth pixel electrode PE12 is spaced apart from the eleventh pixel electrode PE 11 to be connected to the second power line VL2 and the gate line GL through the twelfth switching element T12. The twelfth switching element T12 is connected to the second power line VL2 through the second connection line CL2. A polarity of a voltage applied to the eleventh pixel electrode PE11 and a polarity of a voltage applied to the twelfth pixel electrode PE12 may be opposite to each other with respect to a reference voltage.

[0068] A first voltage is applied to the first bus line BL1, and a second voltage is applied to the second bus line BL2. Voltages, which are inversed per frame unit with respect to an intermediated voltage between the first voltage and the second voltage, are applied to the first and second bus lines BL1 and BL2, respectively. For example, when a minimum voltage is applied to the first bus line BL1 and a maximum voltage is applied to the second bus line BL2 during a current frame, the maximum voltage is applied to the first bus line BL1 and the minimum voltage is applied to the second bus line BL2 during a next frame.

[0069] The first power line VL1 is electrically connected to the first bus line BL1 to receive a voltage that is substantially equal to a voltage applied to the first bus line BL1. The second power line VL2 is electrically connected to the second bus line BL2 to receive a voltage that is substantially equal to a voltage applied to the second bus line BL2. For example, the maximum voltage is applied to the first power line VL1, and the minimum voltage is applied to the second power line VL2. Thus, a voltage of a second polarity (+) that is higher than the minimum voltage with respect to the minimum voltage is applied to the first bus line BL1, and a voltage of a first polarity (-) that is lower than the maximum voltage with respect to the maximum voltage is applied to the second bus line BL2.

[0070] According to the present exemplary embodiment, one power line is shared by three pixel parts and the same polarity data voltage is applied to one power line, so that a generation of a light leakage in a black state may be minimized. Moreover, the number of the power lines is decreased, so that an aperture ratio of a display substrate may be enhanced.

[0071] Hereinafter, as an example, a pixel structure and a manufacturing method of a display substrate 100 according to the present exemplary embodiment will be explained by using the third pixel part P3 of FIG. 2.

[0072] FIG. 3 is a plan view illustrating the LCD panel 1000 of FIG. 1. FIG. 4 is a cross-sectional view taken along line I-I' of FIG. 3.

[0073] Referring to FIGS. 2, 3 and 4, the LCD panel 1000 includes a display substrate 100, an opposite substrate 200 and a liquid crystal layer 300.

[0074] The display substrate 100 includes a first base substrate 101, a first metal pattern, a second metal pattern and a transparent electrode pattern. The display substrate 100 may further include a gate insulation layer 102 covering the first metal pattern, a data insulation layer covering the second metal pattern and a first alignment layer 11 covering the transparent electrode pattern. For example, the data insulation layer may be formed in a multiple layer structure in which a protection insulation layer 103 and an organic insulation layer 104 are formed. For another example, the data insulation layer may be formed in a single layer structure in which a protection insulation layer 103 is formed.

[0075] The first metal pattern includes the gate line GL, a fifth gate electrode GE5, a sixth gate electrode GE6, a first shield part SH1 and a second shield part SH2. The second metal pattern includes a first power line VL1, a third data line DL3, a fifth source electrode SE5, a fifth drain electrode DE5, a sixth source electrode SE6 and a sixth drain electrode DE6. The transparent electrode pattern includes a fifth pixel electrode PE5, a sixth pixel electrode PE6 and a first connection line CL1.

[0076] The gate line GL is extended in the second direction D12. The fifth and sixth gate electrodes GE5 and GE6 are protruded from the gate line GL when viewed in a plan view.

[0077] The first shield part SH1 is disposed adjacent to a self data line delivering a data voltage to the third pixel part P3, that is, the third data line DL3. The first shield part SH1 blocks an electric field of the third data line DL3 from passing through the first base substrate 101, and also blocks light. The first shield part SH1 includes a first upper shield SU1 and a first lower shield SD1 that are spaced apart from each other. The first upper shield SU1 is disposed on an upper area of a pixel area defining the third pixel part P3 adjacent to the third data line DL3, and the first lower shield SD1 is disposed on a lower area of a pixel area defining the third pixel part P3 adjacent to the third data line DL3.

[0078] The second shield part SH2 is disposed adjacent to a first power line VL1. The second shield part SH2 blocks an electric field of the first power line VL1 from leaking through the first base substrate 101, and also blocks light. The second shield part SH2 includes a second upper shield SU2, a second lower shield SD2 spaced apart from the second upper shield SU2, and a connection shield SC connecting the first lower shield SD1 and the second upper shield SU2. Moreover, the second shield part SH2 may be disposed adjacent to a neighboring data line which delivers a data voltage to a neighboring pixel part. For example, in a case of the second pixel part P2 shown in FIG. 2, the second shield part SH2 is disposed adjacent to the third data line DL3 delivering a data voltage to the third pixel part P3. An end portion of the first upper shield SU1 is extended along the second direction DI2 to be disposed adjacent to the second upper shield SU2, and an end portion of the first lower shield SD1 is extended along the second direction DI2 to be disposed adjacent to the second lower shield SD2.

[0079] The first upper shield SU1 is electrically connected to the sixth pixel electrode PE6 through a seventh contact hole C7 to overlap with the sixth pixel electrode PE6, and the second lower shield SD2 is electrically connected to the sixth pixel electrode PE6 through a fifth contact hole C5 to overlap with the sixth pixel electrode PE6. The first upper shield SU1 blocks a light leakage generated between the third data line DL3 and the sixth pixel electrode PE6, and the second lower shield SD2 blocks a light leakage generated between the first power line VL1 and the sixth pixel electrode PE6.

[0080] The first lower shield SD1 is electrically connected to the fifth pixel electrode PE5 through a second contact hole C2 to overlap with the fifth pixel electrode PE5, and the second upper shield SU2 is electrically connected to the fifth pixel electrode PE5 through a sixth contact hole C6 to overlap with the fifth pixel electrode PE5. The first lower shield SD1 blocks a light leakage generated between the third data line DL3 and the fifth pixel electrode PE5, and the second upper shield SU2 blocks a light leakage generated between the first power line VL1 and the fifth pixel electrode PE5.

[0081] The third data line DL3 is extended in the first direction DI1. The fifth source electrodes SE5 is protruded from the third data line DL3 under a plan view, and is disposed on the fifth gate electrode GE5. The fifth drain electrode DE5 is spaced apart from the fifth source electrode SE5 to be electrically connected to the fifth pixel electrode PE5 through a first contact hole C1.

[0082] The sixth source electrode SE6 is electrically connected to the first connection line CL1 through a third contact hole C3, and is disposed on the sixth gate electrode GE6. The first connection line CL1 is electrically connected to the first power line VL1. The sixth drain electrode DE6 is spaced apart from the sixth source electrode SE6 to be electrically connected to the sixth pixel electrode PE6 through a fourth contact hole C4.

[0083] The display substrate 100 may further include a semiconductor layer 150. The semiconductor layer 150 may include a first amorphous silicon layer 151 and a second amorphous silicon layer 152 doped with impurities. For example, the first amorphous silicon layer 151 may have amorphous silicon (a-Si:H), and the second amorphous silicon layer 152 may have n+ amorphous silicon (n+ a-Si:H) that is heavily doped with an n-type impurity. The source electrode and the drain electrode may be positioned on the semiconductor layer 150. A channel of a switching element may be defined by the semiconductor layer 150 exposed between the source electrode and the drain electrode. The fifth and sixth pixel electrodes PE5 and PE6 are disposed in an alternating arrangement to receive the different voltages from the third data line DL3 and the first power line VL1, respectively. Thus, liquid crystal molecules of the liquid crystal layer 300 are arranged by a horizontal electric field formed between the fifth and sixth pixel electrodes PE5 and PE6, so that a gradation may be realized.

[0084] Each of the fifth and sixth pixel electrodes PE5 and PE6 includes a stem portion E 1 overlapping with the data line or the power line and a branch portion E2 inclinedly extending from the stem portion E 1 toward a pixel area by an angle of about 45 degrees (or about -45 degrees). The stem portion E 1 overlaps with the data line or the power line, so that it prevents an electric field of the data line or the power line from being leakage toward an upper portion of the display substrate 100. Moreover, this overlap prevents light from being leaked between the pixel electrode and the data line (or the power line). The potential light leakage may be greater between the third pixel part P3 and the fourth pixel part P4, and between the sixth pixel part P6 and the seventh pixel part P7 in which the polarity of the data voltages is varied, so that light leakages between the third pixel part P3 and the fourth pixel part P4, and between the sixth pixel part P6 and the seventh pixel part P7, as examples, will hereinafter be described.

[0085] For example, a plurality of pixel rows is arranged on the display area DA in the first direction DI1. When frames are altered, a data voltage having a different polarity to a previous data voltage may be sequentially provided to the pixel parts in the first direction DI1. Since a first polarity data voltage is applied to an upper pixel row of the display area DA in an initial frame interval and a

second polarity data voltage is applied to a lower pixel row of the display area DA in a following frame interval, more light leakage may be generated at each right portion of the third pixel part P3 and the sixth pixel part P6 in the upper pixel row and more light leakage may be generated at each left portion of the fourth pixel part P4 and the seventh pixel part P7 in the lower pixel row. Similar to the above, a similar number of light leakage positions may be generated at a left portion and a right portion of each pixel part positioned at a middle portion of the display area DA. Thus, a right width of a stem portion of the pixel electrode corresponding to the middle portion of the display area DA may be substantially equal to a left width of the stem portion of the pixel electrode corresponding to the middle portion of the display area DA.

[0086] Thus, in order to effectively prevent light leakage at each portion of the display area DA, on an upper pixel row of the display area DA, stem portions of pixel electrodes corresponding to a right portion of the third and sixth pixel parts P3 and P6 may be formed to have a wider width, and stem portions of pixel electrodes corresponding to a left portion of the fourth and seventh pixel parts P4 and P7 may be formed to have a narrower width. In a lower pixel row of the display area DA, stem portions of pixel electrodes corresponding to a right portion of the third and sixth pixel parts P3 and P6 may be formed to have a narrower width, and stem portions of pixel electrodes corresponding to a left portion of the fourth and seventh pixel parts P4 and P7 may be formed to have a wider width. As a result, since widths of the stem portions of the pixel parts are different from each other or equal to each other according to which portion of the display area DA the pixel part is positioned in, when data voltages inverted at every frame interval are applied thereto, a light leakage may be effectively prevented, which would otherwise be locally generated at some area as the data voltages are applied to the upper and lower portions of the display area DA at different points of time to have a time interval therebetween.

[0087] Referring to FIG. 3, interval distances between the fifth and sixth pixel electrodes PE5 and PE6 branch portions E2 corresponding to a first area A1 are substantially less than interval distances between the fifth and sixth pixel electrodes PE5 and PE6 branch portions E2 corresponding to a second area A2 of the third pixel part P3. For example, the first area A1 includes a center portion (i.e., a portion on which the connection shield SC is disposed) of the pixel area, a right portion (i.e., a portion proximate a portion through which the sixth contact hole C6 is formed) of the pixel area, and a lower portion of the pixel area, and the second area A2 is the remaining area excluding the first area of the pixel area. Accordingly, the pixel area may be divided into multi-domains to be driven.

[0088] The first alignment layer 11 is formed on the transparent electrode pattern including the fifth and sixth pixel electrodes PE5 and PE6 to vertically align liquid crystal molecules of the liquid crystal layer 300.

[0089] The opposite substrate 200 includes a second base substrate 201. A light-blocking pattern 220, a color filter 230, an overcoating layer 250 and a second alignment layer 21 may be formed on the second base substrate 201.

[0090] The light-blocking pattern 220 may be disposed in correspondence with an area on which the first metal pattern and the second metal pattern are formed, and the light-blocking pattern 220 may block light. For example, the light-blocking pattern 220 is disposed on an area on which the third data line DL3, the first power line VL1, the gate line GL and the switching elements T5 and T6 are formed.

[0091] The color filter 230 is disposed in correspondence with the pixel area on which the fifth and sixth pixel electrodes PE5 and PE6 are formed. The color filter 230 may include a red filter, a green filter and a blue filter. For example, the first pixel part P1 includes a red filter, the second pixel part P2 includes a green filter, and the third pixel part P3 includes a blue filter.

[0092] The overcoating layer 250 is formed on the second base substrate 201 to cover the color filter 230 and the light-blocking pattern 220. The overcoating layer 250 may include an insulation material. The overcoating layer 250 may prevent the color filter 230 from being exposed and provide a planarization surface. The overcoating layer 250 may be omitted.

[0093] In this exemplary embodiment, the light-blocking pattern 220 and the color filter 230 are formed on the opposite substrate 200. Alternatively, the light-blocking pattern 220 and the color filter 230 may be formed on the display substrate 100.

[0094] The second alignment layer 21 is formed on the overcoating layer 250 to vertically align the liquid crystal molecules of the liquid crystal layer 300.

[0095] The liquid crystal layer 300 is disposed between the display substrate 100 and the opposite substrate 200. The liquid crystal layer 300 may have an anisotropy of permittivity. When an electric field is not applied to the liquid crystal molecules of the liquid crystal layer 300, long axes of the liquid crystal molecules may be aligned to be perpendicular with facing surfaces of the two substrates 100 and 200.

[0096] An arrangement of the liquid crystal molecules of the liquid crystal layer 300 is altered by an electric field formed between the fifth pixel electrode PE5 and the sixth pixel electrode PE6. As a result, a transmissivity of the liquid crystal layer 300 may be altered in accordance with the strength of the electrical field.

[0097] For example, when an electric potential difference between the fifth pixel electrode PE5 and the sixth pixel electrode PE6 is maximum, a horizontal electric field may be generated at a surface of the display substrate 100 and the opposite substrate 200 so that a white mode is realized. In contrast, when an electric potential difference between the fifth pixel electrode PE5 and the sixth pixel electrode PE6 is minimum, an electric field may be not generated at a surface of the display substrate 100 and the opposite substrate 200 so that a black mode is

realized.

[0098] That is, liquid crystal molecules of the liquid crystal layer 300 are vertically aligned with respect to a surface of the display substrate 100 and the opposite substrate 200 in response to an electric field, so that long axes of the liquid crystal molecules are horizontally inclined with respect to a direction of the electric field. Thus, a polarizing degree of an incident light is altered in accordance with an inclined degree of the liquid crystal molecules. The polarizing degree represents as a transmittance varying by a polarizer, so that the LCD panel may display images due to the varied transmittance.

[0099] Accordingly, when vertically aligned liquid crystal molecules are used in the LCD device, a contrast ratio of the LCD device may be increased and a wide viewing angle may be realized. Moreover, two voltages having different polarities are applied to one pixel part, so that a driving voltage may be increased and a response speed may be enhanced.

[0100] FIGS. 5A to 5D are plan views explaining a method of manufacturing the display substrate of FIG. 3.

[0101] Referring to FIGS. 3, 4 and 5A, a first metal layer is formed on the first base substrate 101, and then the first metal layer is patterned to form a first metal pattern. The first metal pattern includes the gate line GL, the fifth gate electrode GE5, the sixth gate electrode GE6, the first shield part SH1 and the second shield part SH2.

[0102] The gate line GL is extended in the second direction DI2. The fifth and sixth gate electrodes GE5 and GE6 are protruded from the gate line GL toward the pixel area in a plan view.

[0103] The first shield part SH1 includes the first upper shield SU1 and the first lower shield SD1 that are extended along the first direction DI1. The upper end portion of the first upper shield SU1 is extended in the second direction DI2, and the lower end portion of the first lower shield SD1 is extended in the second direction DI2.

[0104] The second shield part SH2 includes the second upper shield SU2 and the second lower shield SU2 that are extended along the first direction DI1. The second shield part SH2 may further include a connection shield SC extended in the second direction DI2 to connect the first lower shield SD 1 and the second upper shield SU2.

[0105] A gate insulation layer 102 is formed on the first base substrate 101 on which the first metal pattern is formed to cover the first metal pattern. The gate insulation layer 102 may have a multiple layer structure in which a silicon oxide (SiOx) and a silicon nitride (SiNx) are deposited. Alternatively, the gate insulation layer 102 may have a single layer structure in which a silicon oxynitride (SiON) is formed. In this case, the silicon oxynitride (SiON) layer may have an oxide concentration in accordance with a deposition direction thereof. The oxide concentration may be higher when the silicon oxynitride (SiON) layer is closer to a semiconductor pattern.

[0106] Referring to FIGS. 3, 4 and 5B, a semiconductor layer 150 and a second metal layer are formed on the gate insulation layer 102, and then the semiconductor layer 150 and the second metal layer are patterned to form a second metal pattern. The semiconductor layer 150 may include the first amorphous silicon layer 151 and the second amorphous silicon layer 152 doped with impurities. For example, the first amorphous silicon layer 151 may have amorphous silicon (a-Si:H), and the second amorphous silicon layer 152 may have n+ amorphous silicon (n+ a-Si:H) that is heavily doped with an n-type impurity.

[0107] Moreover, the semiconductor layer 150 may include an oxide semiconductor material. The oxide semiconductor material may include amorphous oxide including at least one of indium (In), zinc (Zn), gallium (Ga), tin (Sn) and hafnium (Hf). For one example, the oxide semiconductor material may include amorphous oxide including indium (In), zinc (Zn) and gallium (Ga). For another example, the oxide semiconductor material may include amorphous oxide including indium (In), zinc (Zn) and hafnium (Hf). The oxide semiconductor may include an oxide material such as indium zinc oxide (InZnO), indium gallium oxide (InGaO), indium tin oxide (InSnO), zinc tin oxide (ZnSnO), gallium tin oxide (GaSnO), gallium zinc oxide (GaZnO), etc. In addition, the oxide semiconductor may further include at least one of elements of the Group III, elements of the Group IV, elements of the Group V, and transition elements in order to enhance the oxide material characteristics. The oxide semiconductor layer has a higher effective mobility than a hydrogen amorphous silicon by about two times to a hundred times and has an on-off current ratio of about 10:5 to about 10:8, so that the oxide semiconductor layer has superior semiconductor characteristics in comparison with the hydrogen amorphous silicon. Moreover, since a band gap of the oxide semiconductor is about 3.0 eV to about 3.5 eV, a leakage current for a visible light is not generated. Thus, a light-blocking layer is not formed below a switching element including the oxide semiconductor layer, so that an aperture ratio may be increased.

[0108] Alternatively, before the second metal layer is formed, a semiconductor layer may be formed on the gate insulation layer 102 by using an additional mask to form a semiconductor pattern only on the gate electrodes.

[0109] The second metal pattern includes the third data line DL3, the fifth source electrode SE5, the fifth drain electrode DE5, the sixth source electrode SE6, the sixth drain electrode DE6 and the first power line VL1.

[0110] The third data line DL3 is extended in the first direction DI1, and is formed adjacent to the first shield part SH1. For example, the third data line DL3 is formed adjacent to the first upper shield SU1 and the first lower shield SD1.

[0111] The first power line VL1 is extended in the first direction DI1, and is formed adjacent to the second shield part SH2. For example, the first power line VL1 is formed adjacent to the second upper shield SU2 and the second lower shield SD2.

[0112] The fifth source electrode SE5 is protruded from the third data line DL3 to be formed on the fifth gate electrode GE5 under a plan view. The fifth drain electrode DE5 is spaced apart from the fifth source electrode SE5 to be formed on the fifth gate electrode GE5. The fifth drain electrode DE5 is extended to have a predetermined length. The sixth source electrode SE6 is formed on the sixth gate electrode GE6, and the sixth drain electrode DE6 is spaced apart from the sixth source electrode SE6 to be formed on the sixth gate electrode GE6. The sixth source electrode SE6 is extended to have a predetermined length.

[0113] Referring to FIGS. 3 and 5C, the protection insulation layer 103 is formed on the first base substrate 101 on which the second metal pattern is formed. The protection insulation layer 103 may have a multiple layer structure including a silicon oxide (SiOx) and a silicon nitride (SiNx) or a single layer structure. The protection layer 103 is disposed to cover the semiconductor layer, so that deterioration of a thin-film transistor is prevented.

[0114] The protection insulation layer 103 and the gate insulation layer 102 are etched to form the first contact hole C1, the second contact hole C2, the third contact hole C3, the fourth contact hole C4, the fifth contact hole C5, the sixth contact hole C6, the seventh contact hole C7 and an eighth contact hole C8. Then, the organic insulation layer 104 is formed on the first base substrate 101 having the first to eighth contact holes C1, C2, C3, C4, C5, C6, C7 and C8 formed thereon. The organic insulation layer 104 is patterned to remove the organic insulation layer 104 in correspondence with the first to eighth contact holes C1, C2, C3, C4, C5, C6, C7 and C8.

[0115] As a result, the first metal pattern and the second metal pattern are partially exposed through the first to eighth contact holes C1, C2, C3, C4, C5, C6, C7 and C8.

[0116] Referring to FIGS. 3 and 5D, a transparent conductive layer is formed on the first base substrate 101 having the first to eighth contact holes C1, C2, C3, C4, C5, C6, C7 and C8 formed thereon, and then the transparent conductive layer is patterned to form a transparent conductive pattern. The transparent conductive layer may include an optically transparent and electrically conductive material such as indium tin oxide (ITO), indium zinc oxide (IZO), etc.

[0117] The transparent electrode pattern includes the fifth pixel electrode PE5, the sixth pixel electrode PE6 and the first connection line CL1.

[0118] The fifth pixel electrode PE5 is electrically connected to the fifth drain electrode DE5 of the fifth switching element T5 through the first contact hole C1, and the sixth pixel electrode PE6 is electrically connected to the sixth drain electrode DE6 of the sixth switching element T6 through the fourth contact hole C4. Each of the fifth and sixth pixel electrodes PE5 and PE6 includes a stem portion E1 and a branch portion E2. The stem portions E1 may partially overlap with the third data line DL3 and the first power line VL1. The branch portions E2 may be inclinedly extended from the respective stem portion E1 toward the pixel area by an angle of about 45 degrees (or about -45 degrees). The branch portion E2 of the fifth pixel electrode PE5 and the branch portion E2 of the sixth pixel electrode PE6 may be disposed in an alternating arrangement.

[0119] The fifth pixel electrode PE5 is electrically connected to the first lower shield SD1 through the second contact hole C2, and is electrically connected to the second upper shield SU2 through the sixth contact hole C6. The sixth pixel electrode PE6 is electrically connected to the second lower shield SD2 through the fifth contact hole C5, and is electrically connected to the first upper shield SU1 through the seventh contact hole C7.

[0120] The first connection line CL1 is electrically connected to the first power line VL1 through the eighth contact hole C8 to be extended in the second direction DI2. The first connection line CL1 is protruded toward the sixth source electrode SE6 to be electrically connected to the sixth source electrode SE6 through the third contact hole C3. Thus, the sixth switching element T6 may deliver a voltage applied to the first connection line CL1 to the sixth pixel electrode PE6.

[0121] The first alignment layer 11 is formed on the first base substrate 101 having the transparent electrode pattern formed thereon.

[0122] FIG. 6 is a plan view illustrating an LCD panel 1000A according to another exemplary embodiment of the present invention. FIG. 7 is a cross-sectional view taken along line II-II' of FIG. 6.

[0123] Referring to FIGS. 2, 6 and 7, the LCD panel 1000A includes a display substrate 100A, an opposite substrate 200 and a liquid crystal layer 300. The LCD panel 1000A according to the present exemplary embodiment may be substantially the same as the LCD device of FIG. 1 except for a first shield part SH1, a second shield part SH2 and a connection electrode pattern CEP, and thus any repetitive detailed explanation will hereinafter be omitted or simplified.

[0124] Each of the first and second shield parts SH1 and SH2 includes a trench structure in which the gate insulation layer 102, the protection insulation layer 103 and the organic insulation layer 104 are removed.

[0125] The connection electrode pattern CEP may be included in the first metal pattern. The connection electrode pattern CEP is extended from a center portion of the pixel area along the second direction DI2 to electrically connect the fifth pixel electrode PE5 disposed in the lower pixel area and the fifth pixel electrode PE5 disposed in the upper pixel area under a plan view. The connection electrode CEP is electrically connected to the fifth pixel electrode PE5 partially overlapped with the third data line DL3 through a ninth contact hole C9, and is electrically connected to the fifth pixel electrode PE5 partially overlapped with the first power line VL1 through a tenth contact hole C10.

[0126] The first shield part SH1 is disposed adjacent to a self data line, that is, the third data line DL3, which

delivers a data voltage to the third pixel part P3. The first shield part SH1 includes a first upper trench TU1 and a first lower trench TD1. The gate insulation layer 102, the protection insulation layer 103 and the organic insulation layer 104 are removed to form the first upper trench TU1 and the first lower trench TD1. The sixth pixel electrode PE6 partially overlapped with an upper portion of the third data line DL3 is formed through the first upper trench TUl, and the fifth pixel electrode PE5 partially overlapped with a lower portion of the third data line DL3 is formed through the first lower trench TD1.

[0127] The second shield part SH2 is disposed adjacent to the first power line VL1. Alternatively, the second shield part SH2 may be disposed adjacent to a neighboring data line delivering a data voltage to a neighboring pixel part. The second shield part SH2 includes a second upper trench TU2 and a second lower trench TD2. The gate insulation layer 102, the protection insulation layer 103 and the organic insulation layer 104 are removed to form the second upper trench TU2 and the second lower trench TD2. The fifth pixel electrode PE5 partially overlapped with an upper portion of the first power line VL1 is formed through the second upper trench TU2, and the sixth pixel electrode PE6 partially overlapped with a lower portion of the first power line VL1 is formed through the second lower trench TD2.

[0128] As shown in FIG. 6, the first upper trench TU1 may extend along the second direction DI2 at an upper portion of the pixel area adjacent to the second upper trench TU2 in a plan view, and the first lower trench TD 1 may extend along the second direction DI2 at a lower portion of the pixel area adjacent to the second lower trench TD2 in a plan view.

[0129] Similar to the previous embodiment described in connection with FIGS. 1 to 4, the first and second shield parts SH1 and SH2 may prevent an electric field of the data line or the power line from being leaked, and may prevent a light leakage from being generated between the power line and the pixel electrode or between the data line and the pixel electrode. In addition, the first and second shield parts SH1 and SH2 have a structure in which the pixel electrode is formed through a trench, so that an aperture ratio of the display substrate may be enhanced in comparison with the display substrate according to the previous embodiment described in connection with FIGS. 1 to 4.

[0130] FIGS. 8A to 8D are plan views explaining a method of manufacturing the display substrate of FIG. 7. Hereinafter, the same reference numerals will be used to refer to the same or like parts as those described in the previous exemplary embodiment of FIG. 1 and any repetitive detailed explanation concerning the above elements will be omitted or simplified.

[0131] Referring to FIGS. 7 and 8A, a first metal layer is formed on the first base substrate 101, and then the first metal layer is patterned to form a first metal pattern. The first metal pattern includes the gate line GL, a fifth gate electrode GE5, a sixth gate electrode GE6 and the connection electrode pattern CEP.

[0132] The gate line GL is extended in the second direction DI2. The fifth and sixth gate electrodes GE5 and GE6 are protruded from the gate line GL toward the pixel area on a plan view.

[0133] The connection electrode pattern CEP is extended at a center portion of the pixel area toward the second direction DI2. The connection electrode pattern CEP may divide the pixel area into an upper portion and a lower portion. The pixel area is an area on which the fifth and sixth pixel electrodes PE5 and PE6 are formed by the following process.

[0134] The gate insulation layer 102 covering the first metal pattern is formed on the first base substrate 101 on which the first metal pattern is formed.

[0135] Referring to FIGS. 7 and 8B, a semiconductor layer and a second metal layer are formed on the gate insulation layer 102, and then the semiconductor layer and the second metal layer are patterned to form a second metal pattern.

[0136] The second metal pattern includes the third data line DL3, a fifth source electrode SE5, a fifth drain electrode DE5, a sixth source electrode SE6, a sixth drain electrode DE6 and the first power line VL1.

[0137] Referring to FIGS. 7 and 8C, the protection insulation layer 103 is formed on the first base substrate 101 on which the second metal pattern is formed to cover the second metal pattern.

[0138] The protection insulation layer 103 and the gate insulation layer 102 are etched to form a first, third, fourth, eighth, ninth and tenth contact holes C1, C3, C4, C8, C9 and C10. Moreover, the protection insulation layer 103 and the gate insulation layer 102 are etched to form the first upper trench TU1 and the first lower trench TD1 on the pixel area adjacent to the third data line DL3, and to form the second upper trench TU2 and the second lower trench TD2 on the pixel area adjacent to the first power line VL1.

[0139] Then, the organic insulation layer 104 is formed on the first base substrate 101 on which the contact holes C1, C3, C4, C8, C9 and C10 and the trenches TU1, TD1, TU2 and TD2 are formed. The organic insulation layer 104 is patterned, so that the organic insulation layer 104 corresponding to the contact holes C1, C3, C4, C8, C9 and C10 and the trenches TU1, TD1, TU2 and TD2 is removed.

[0140] As a result, the first metal pattern and the second metal pattern are partially exposed through the contact holes C1, C3, C4, C8, C9 and C10, and the first base substrate 101 is exposed through the trenches TU1, TD 1, TU2 and TD2.

[0141] Referring to FIGS. 7 and 8D, a transparent conductive layer is formed on the first base substrate 101 having the contact holes C1, C3, C4, C8, C9 and C10 and the trenches TU1, TD1, TU2 and TD2 formed thereon, and then the transparent conductive layer is patterned to form a transparent electrode pattern.

[0142] The transparent electrode pattern includes the

fifth pixel electrode PE5, the sixth pixel electrode PE6 and a first connection line CL1.

[0143] The fifth pixel electrode PE5 is electrically connected to the fifth drain electrode DE5 of the fifth switching element T5 through the first contact hole C1, and the sixth pixel electrode PE6 is electrically connected to the sixth drain electrode DE6 of the sixth switching element T6. Each of the fifth and sixth pixel electrodes PE5 and PE6 includes a stem portion E1 and a branch portion E2. The stem portions E1 may partially overlap with the third data line DL3 and the first power line VL1. The branch portions E2 may inclinedly extend from the respective stem portions E1 toward the pixel area by an angle of about 45 degrees (or about -45 degrees). The branch portion E2 of the fifth pixel electrode PE5 and the branch portion E2 of the sixth pixel electrode PE6 may be disposed in an alternating arrangement.

[0144] The fifth pixel electrode PE5 which is formed at a lower portion of the pixel area with respect to the connection electrode pattern CEP is electrically connected to the connection electrode pattern CEP through the ninth contact hole C9. In addition, the fifth pixel electrode PE5 which is formed at an upper portion of the pixel area with respect to the connection electrode pattern CEP is electrically connected to the connection electrode pattern CEP through the tenth contact hole C10. Thus, the fifth pixel electrode PE5 formed at the upper portion of the pixel area may be electrically connected to the fifth pixel electrode PE5 formed at the lower portion of the pixel area. The sixth pixel electrode PE6 is formed at the upper portion and the lower portion of the pixel area.

[0145] The sixth pixel electrode PE6 which partially overlaps with an upper portion of the third data line DL3 is formed through the first upper trench TU1 of the first shield part SH1, and the fifth pixel electrode PE5 which partially overlaps with a lower portion of the third data line DL3 is formed through the first lower trench TD1 of the first shield part SH1. The fifth pixel electrode PE5 which overlaps with an upper portion of the first power line VL1 is formed through the second upper trench TU2 of the second shield part SH2, and the sixth pixel electrode PE6 which overlaps with a lower portion of the first power line VL1 is formed through the second lower trench TD2 of the second shield part SH2.

[0146] The first connection line CL1 is electrically connected to the first power line VL1 through the eighth contact hole C8, and is extended in the second direction DI2. The first connection line CL1 is protruded toward the sixth source electrode SE6 to be electrically connected to the sixth source electrode SE6 through the third contact hole C3 on a plan view.

[0147] According to the present exemplary embodiment, the first and second shield parts SH1 and SH2 have trenches having the pixel electrodes formed therethrough, so that an aperture ratio of the LCD panel may be enhanced.

[0148] FIG. 9 is a schematic diagram illustrating an LCD panel 1000B according to another exemplary embodiment of the present invention.

[0149] Referring to FIG. 9, an LCD device includes the LCD panel 1000B. The LCD panel 1000B may further include a storage line STL in comparison with the LCD panel 1000 of FIGS. 1 to 3.

[0150] The storage line STL is extended in the second direction DI2, and is disposed adjacent to the gate line GL. A storage voltage is applied to the storage line STL. The storage voltage may be a direct current (DC) having a predetermined level in spite of a frame. A reference voltage is applied to the storage line STL. A voltage of a first polarity (for example, a negative (-) polarity) with respect to the reference voltage is applied to the first power line VL1, and a voltage of a second polarity (for example, a positive (+) polarity) with respect to the reference voltage is applied to the second power line VL2. In accordance with the above, a voltage of a second polarity (a positive (+) polarity) having a level higher than a voltage applied to the first power line VL1 is applied to the first, second and third data lines DL1, DL2 and DL3, and a voltage of a first polarity (for example, a negative (-) polarity) having a level lower than a voltage applied to the second power line VL2 is applied to the fourth, fifth and sixth data lines DL4, DL5 and DL6.

[0151] For example, the storage line STL partially overlaps with extending portions of switching elements included on the first, second, third, fourth, fifth and sixth pixel parts P1, P2, P3, P4, P5 and P6, so that storage capacitors may be defined. A variation of a voltage applied to the pixel parts P1, P2, P3, P4, P5 and P6 is decreased by the storage capacitors, so that display quality may be enhanced.

[0152] Hereinafter, as an example, a pixel structure and a manufacturing method according to the present exemplary embodiment will be explained by using the third pixel part P3 of FIG. 9.

[0153] FIG. 10 is a plan view showing the LCD panel of FIG. 9. FIG. 11 is a cross-sectional view taken along line III-III' of FIG. 10.

[0154] Referring to FIGS. 10 and 11, the LCD panel 1000B includes a display substrate 100B, an opposite substrate 200 and a liquid crystal layer 300. The LCD panel 1000B according to the present exemplary embodiment may be substantially the same as the LCD panel 1000 of FIG. 1, and thus any repetitive detailed explanation will hereinafter be omitted or simplified. Moreover, the display substrate 100B according to the present exemplary embodiment may be substantially the same as the display substrate 100 of FIG. 1, and thus any repetitive detailed explanation will hereinafter be simplified.

[0155] The display substrate 100B includes a first base substrate 101, the gate line GL, the storage line STL, a first shield part SH1, a second shield part SH2, the third data line DL3, the first power line VL1, the fourth data line DL4, a fifth pixel electrode PE5, a sixth pixel electrode PE6, a seventh pixel electrode PE7, an eighth pixel electrode PE8, and a first connection line CL1.

[0156] The gate line GL is extended in the second di-

rection DI2. A fifth gate electrode GE5 and a sixth gate electrode GE6 are protruded from the gate line GL in a plan view.

[0157] The storage line STL is extended in the second direction DI2, and is disposed adjacent to the gate line GL.

[0158] The first shield part SH1 is disposed adjacent to a self data line, that is, the third data line DL3, which delivers a data voltage to the third pixel part P3. The first shield part SH1 includes a first upper shield SU1 adjacent to an upper portion of the third data line DL3 and a first lower shield SD1 adjacent to a lower portion of the third data line DL3. The second shield part SH2 is disposed adjacent to the first power line VL1 (or a neighboring data line). The second shield part SH2 includes a second upper shield SU2 adjacent to an upper portion of the first power line VL1 and a second lower shield SD2 adjacent to a lower portion of the first power line VL1. The first and second shield parts SH1 and SH2 may be formed by the first upper trench TU1, the first lower trench TD1, the second upper trench TU2 and the second lower trench TD2, as described in FIGS. 6 and 7.

[0159] The third data line DL3 is extended in the first direction DI1. A fifth source electrode SE5 is protruded from the third data line DL3 to be disposed on the fifth gate electrode GE5 in a plan view. A fifth drain electrode DE5 is spaced apart from the fifth source electrode SE5 to partially overlap with the fifth gate electrode GE5, and is electrically connected to the fifth pixel electrode PE5 through a first contact hole C1. The fifth drain electrode DE5 includes an extending portion. The extending portion partially overlaps with the storage line STL to form a first storage capacitor CST1.

[0160] A sixth source electrode SE6 is electrically connected to the first connection line CL1 through a third contact hole C3, and is disposed on the sixth gate electrode GE6. The first connection line CL1 is electrically connected to the first power line VL1. A sixth drain electrode DE6 is spaced apart from the sixth source electrode SE6 to partially overlap with the sixth gate electrode GE6, and is electrically connected to the sixth pixel electrode PE6 through a fourth contact hole C4. The sixth drain electrode DE6 includes an extending portion. The extending portion partially overlaps with the storage line STL to form a second storage capacitor CST2.

[0161] The fourth data line DL4 is extended in the first direction DI1. A seventh pixel electrode PE7 is electrically connected to the fourth data line DL4 through a seventh switching element T7 (as shown in FIG. 9), and an eighth pixel electrode PE8 is electrically connected to a second connection line CL2 through an eighth switching element T8 (as shown in FIG. 9).

[0162] The third data line DL3 may overlap with a stem portion of the fifth pixel electrode PE5, and the fourth data line DL4 may overlap with a stem portion of the seventh pixel electrode PE7. Thus, a generation of a light leakage may be prevented, which is generated between the third and fourth pixel parts P3 and P4 having different polarities.

[0163] Moreover, the first power line VL1 and the fourth data line DL4 may be spaced apart from each other across an interval (gap). The interval between the first power line VL1 and the fourth data line DL4 may be about 7 μm to about 13 μm. Thus, a generation of a light leakage may be prevented, which would be generated between the third and fourth pixel parts P3 and P4 having different polarities.

[0164] The first connection line CL1 overlaps with the gate line GL (as shown in FIG. 10). Similarly, the second connection line CL2 (FIG. 9) overlaps with the gate line. Thus, an aperture ratio of the LCD panel may be enhanced.

[0165] FIGS. 12A to 12C are plan views explaining a method of manufacturing the display substrate of FIG. 11. Hereinafter, any repetitive detailed explanation about the identical elements of FIG. 1 will be omitted.

[0166] Referring to FIGS. 11 and 12A, a first metal layer is formed on the first base substrate 101, and then the first metal pattern is patterned to form a first metal pattern. The first metal pattern includes the gate line GL, the fifth gate electrode GE5, the sixth gate electrode GE6, the storage line STL, the first shield part SH1 and the second shield part SH2.

[0167] The storage line STL is extended in the second direction DI2, and is disposed adjacent to the gate line GL.

[0168] A gate insulation layer 102 is formed on the first base substrate 101 on which the first metal pattern is formed, so that the first metal pattern is covered by the gate insulation layer 102.

[0169] Referring to FIGS. 11 and 12B, a semiconductor layer and a second metal layer are formed on the gate insulation layer 102, and then the semiconductor layer and the second metal layer are patterned to form a second metal pattern. The second metal pattern includes the third data line DL3, the fourth data line DL4, the fifth source electrode SE5, the fifth drain electrode DE5, the sixth source electrode SE6, the sixth drain electrode DE6 and the first power line VL1.

[0170] The fifth drain electrode DE5 is spaced apart from the fifth source electrode SE5, and an extending portion of the fifth drain electrode DE5 is partially overlapped with the storage line STL. The sixth drain electrode DE6 is spaced apart from the sixth source electrode SE6, and an extending portion of the sixth drain electrode DE6 is partially overlapped with the storage line STL.

[0171] Referring to FIGS. 11 and 12C, a protection insulation layer 103 covering the second metal pattern is formed on the first base substrate 101 1 on which the second metal pattern is formed. The protection insulation layer 103 and the gate insulation layer 102 are etched to form the first contact hole C1, the second contact hole C2, the third contact hole C3, the fourth contact hole C4, a fifth contact hole C5, a sixth contact hole C6, a seventh contact hole C7 and an eighth contact hole C8. An organic insulation layer 104 is formed on the first base sub-

strate 101. The organic insulation layer 104 is patterned to remove the organic insulation layer 104 corresponding to the first to eighth contact holes C1, C2, C3, C4, C5, C6, C7 and C8. Although not shown in FIGS. 11 and 12C, the gate insulation layer 102, the protection insulation layer 103 and the organic insulation layer 104 may be removed from the first and second shield parts SH1 and SH2, so that a first upper trench TU1, a first lower trench TD1, a second upper trench TU2 and a second lower trench TD2 may be formed, in a similar manner to the exemplary embodiment described with reference to FIGS. 6 and 7.

[0172] A transparent conductive layer is formed on the first base substrate 101 1 having the first to eighth contact holes C1, C2, C3, C4, C5, C6, C7 and C8 formed therethrough, and then the transparent conductive layer is patterned to form a transparent electrode pattern. The transparent electrode pattern includes the fifth pixel electrode PE5, the sixth pixel electrode PE6, the seventh pixel electrode PE7, the eighth pixel electrode PE8 and the first connection line CL1.

[0173] A stem portion of the fifth pixel electrode PE5 may be formed to overlap with the third data line DL3, and a stem portion of the seventh pixel electrode PE7 may be formed to overlap with the fourth data line DL4.

[0174] The first connection line CL1 is formed on the gate line GL to overlap with the gate line GL.

[0175] According to the present exemplary embodiment, the storage line receiving a direct voltage of a uniform level is formed, so that voltage variation of a pixel part is decreased to enhance display quality. Moreover, a data line and a power line between pixel parts having different polarities are overlapped with an adjacent pixel electrode, so that light leakage may be prevented. Moreover, a connection line connecting the power line and a switching element is overlapped with a gate line, so that an aperture ratio may be enhanced.

[0176] FIG. 13 is a schematic diagram illustrating an LCD panel 1000C according to another exemplary embodiment of the present invention.

[0177] Referring to FIG. 13, the LCD panel 1000C includes plural data lines DL1, DL2, DL3, DL4, DL5, DL6, DL7, DL8, DL9, DL10, DL11 and DL12, a first bus line BL1, a second bus line BL2, a first power line VL1, a second power line VL2, a first gate line GL1, a second gate line GL2 and plural pixel parts P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11 and P12. The plural pixel parts P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11 and P12 include a primary color pixel.

[0178] As with the previous embodiment described in connection with FIGS. 1 to 4, the first to sixth pixel parts P1, P2, P3, P4, P5 and P6 include first to twelfth pixel electrodes PE1, PE2, ..., PE12. The first to twelfth pixel electrodes PE1, PE2, ..., PE12 are electrically connected to the first to sixth data lines DL1, DL2, DL3, DL4, DL5 and DL6, the power lines VL1 and VL2 and the first gate line GL1. In this exemplary embodiment, a detailed explanation for a connection structure concerning the first to sixth pixel parts P1, P2, P3, P4, P5 and P6 will be omitted.

[0179] The second gate line GL2 is extended in the second direction DI2.

[0180] As shown in FIG. 13, the first and second gate lines GL1 and GL2 may be connected to each other at a peripheral area of the LCD panel. In this case, a gate signal outputted from the gate driving part may be simultaneously applied to the first and second gate lines GL1 and GL2. Alternatively, the first and second gate lines GL1 and GL2 may be separated from each other. In this case, the gate driving part may simultaneously output the gate signal to each of the first and second gate lines GL1 and GL2. Accordingly, two pixel rows electrically connected to the first and second gate lines GL1 and GL2 may be simultaneously driven. The seventh pixel part P7 includes a thirteenth pixel electrode PE13, a fourteenth pixel electrode PE14, a thirteenth switching element T13 and a fourteenth switching element T14. The thirteenth pixel electrode PE13 is connected to the seventh data line DL7 and the second gate line GL2 through the thirteenth switching element T13. The seventh data line DL7 is disposed between the first and second data lines DL1 and DL2, and is disposed adjacent to the second data line DL2. The fourteenth pixel electrode PE14 is spaced apart from the thirteenth pixel electrode PE13, and is connected to the first power line VL1 and the second gate line GL2 through the fourteenth switching element T14. The fourteenth switching element T14 is connected to the first power line VL1 through a first connection line CL1.

[0181] The eighth pixel part P8 includes a fifteenth pixel electrode PE15, a sixteenth pixel electrode PE16, a fifteenth switching element T15 and a sixteenth switching element T16. The fifteenth pixel electrode PE15 is connected to the eighth data line DL8 and the second gate line GL2 through the fifteenth switching element T15. The eighth data line DL8 is disposed between the second and third data lines DL2 and DL3, and is disposed adjacent to the third data line DL3. The sixteenth pixel electrode PE16 is spaced apart from the fifteenth pixel electrode PE15 to be connected to the first power line VL1 and the second gate line GL2 through the sixteenth switching element T16. The sixteenth switching element T16 is connected to the first power line VL1 through the first connection line CL1.

[0182] The ninth pixel part P9 includes a seventeenth pixel electrode PE17, an eighteenth pixel electrode PE18, a seventeenth switching element T17 and an eighteenth switching element T18. The seventeenth pixel electrode PE17 is connected to the ninth data line DL9 and the second gate line GL2 through the seventeenth switching element T17. The ninth data line DL9 is disposed between the third data line DL3 and the first power line VL1, and is disposed adjacent to the first power line VL1. The eighteenth pixel electrode PE18 is spaced apart from the seventeenth pixel electrode PE17 to be connected to the first power line VL1 and the second gate

line GL2 through the eighteenth switching element T18. The eighteenth switching element T18 is connected to the first power line VL1 through the first connection line CL1.

[0183] The tenth pixel part P10 includes a nineteenth pixel electrode PE19, a twentieth pixel electrode PE20, a nineteenth switching element T19 and a twentieth switching element T20. The nineteenth pixel electrode PE19 is connected to the tenth data line DL10 and the second gate line GL2 through the nineteenth switching element T19. The tenth data line DL10 is disposed between the fourth and fifth data lines DL4 and DL5, and is disposed adjacent to the fifth data line DL5. The twentieth pixel electrode PE20 is spaced apart from the nineteenth pixel electrode PE19 to be connected to the second power line VL2 and the second gate line GL2 through the twentieth switching element T20. The twentieth switching element T20 is connected to the second power line VL2 through a second connection line CL2.

[0184] The eleventh pixel part P11 includes a twenty-first pixel electrode PE21, a twenty-second pixel electrode PE22, a twenty-first switching element T21 and a twenty-second switching element T22. The twenty-first pixel electrode PE21 is connected to the eleventh data line DL11 and the second gate line GL2 through the twenty-first switching element T21. The eleventh data line DL11 is disposed between the fifth and sixth data lines DL5 and DL6, and is disposed adjacent to the sixth data line DL6. The twenty-second pixel electrode PE22 is spaced apart from the twenty-first pixel electrode PE21 to be connected to the second power line VL2 and the second gate line GL2 through the twenty-second switching element T22. The twenty-second switching element T22 is connected to the second power line VL2 through the second connection line CL2.

[0185] The twelfth pixel part P12 includes a twenty-third pixel electrode PE23, a twenty-fourth pixel electrode PE24, a twenty-third switching element T23 and a twenty-fourth switching element T24. The twenty-third pixel electrode PE23 is connected to the twelfth data line DL12 and the second gate line GL2 through the twenty-third switching element T23. The twelfth data line DL12 is disposed between the sixth data line DL6 and a second power line VL2, and is disposed adjacent to the second power line VL2. The twenty-fourth pixel electrode PE24 is spaced apart from the twenty-third pixel electrode PE23 to be connected to the second power line VL2 and the second gate line GL2 through the twenty-fourth switching element T24. The twenty-fourth switching element T24 is connected to the second power line VL2 through the second connection line CL2.

[0186] A voltage of a first polarity (for example, a negative (-) polarity) with respect to a reference voltage is applied to the first power line VL1, and a voltage of a second polarity (for example, a positive (+) polarity) with respect to the reference voltage is applied to the second power line VL2. A voltage of a second polarity (a positive (+) polarity) having a level higher than a voltage applied to the first power line VL1 is applied to the first, second, third, seventh, eighth and ninth data lines DL1, DL2, DL3, DL7, DL8 and DL9, and a voltage of a first polarity (for example, a negative (-) polarity) having a level lower than a voltage applied to the second power line VL2 is applied to the fourth, fifth, sixth, tenth, eleventh and twelfth data lines DL4, DL5, DL6, DL10, DL11 and DL12.

[0187] According to the present exemplary embodiment, one pixel row receives a data voltage through two data lines, and two pixel columns receive one gate signal through two gate lines, so that two pixel columns may be driven for one horizontal period (1H). That is, the LCD panel 1000C may be driven at a high speed. Moreover, one power line is shared by three pixel parts and the same polarity data voltage is applied by the one power line, so that a generation of a light leakage in a black state may be minimized. Moreover, the number of power lines is decreased, so that an aperture ratio of a display substrate may be enhanced.

[0188] FIG. 14 is a plan view showing the LCD panel 1000C of FIG. 13. Hereinafter, any repetitive detailed explanation about the identical elements of FIG. 1 will be omitted or simplified.

[0189] Referring to FIGS. 13 and 14, the LCD panel 1000C includes the third data line DL3, the ninth data line DL9, the first power line VL1, the first gate line GL1 and the third pixel part P3.

[0190] The third data line DL3 and the ninth data line DL9 are extended along a first direction DI1, and the third pixel part P3 is disposed between the third and ninth data lines DL3 and DL9. The first power line VL1 is disposed adjacent to the ninth data line DL9.

[0191] The first gate line GL1 is extended along the second direction DI2.

[0192] The third pixel part P3 includes a fifth switching element T5, a fifth pixel electrode PE5, a sixth switching element T6, a sixth pixel electrode PE6, a first shield part SH1 and a second shield part SH2. The fifth switching element T5 includes a fifth gate electrode GE5 connected to the first gate line GL1, a fifth source electrode SE5 connected to the third data line DL3, and a fifth drain electrode DE5 spaced apart from the fifth source electrode SE5 to be connected to the fifth pixel electrode PE5 through a first contact hole C1.

[0193] The sixth switching element T6 includes a sixth gate electrode GE6 connected to the first gate line GL1, a sixth source electrode SE6 electrically connected to the first power line VL1 through the first connection line CL1, and a sixth drain electrode DE6 spaced apart from the sixth source electrode SE6 to be connected to the sixth pixel electrode PE6 through a fourth contact hole C4. The sixth source electrode SE6 is connected to the first connection line CL1 through a third contact hole C3.

[0194] The first shield part SH1 includes a first upper shield part SU1 and a first lower shield part SD1 to be disposed adjacent to a self data line, that is, the third data line DL3 delivering a data voltage to the third pixel part P3.

[0195] The second shield part SH2 includes a second

upper shield SU2 and a second lower shield SD2 to be disposed adjacent to a neighboring data line, that is, the ninth data line DL9 delivering a data voltage to the ninth pixel part P9 adjacent to the third pixel part P3 in the first direction DI1. The first and second shield parts SH1 and SH2 may be a metal pattern. For example, the first and second shield parts SH1 and SH2 may be a metal pattern formed from a metal layer identical to the first gate line GL1.

[0196] A method of manufacturing the display substrate according to the present exemplary embodiment is substantially the same as the method of manufacturing the display substrate described in FIGS. 5A to 5D. In this case, the ninth data line DL9 may be formed when the second metal pattern including the third data line DL3 is formed. Thus, any explanation for the method of manufacturing the display substrate according to the present exemplary embodiment will hereinafter be omitted.

[0197] FIG. 15 is a plan view showing an LCD panel 1000D according to another exemplary embodiment of the present invention.

[0198] Referring to FIGS. 13 and 15, the LCD panel 1000D may be substantially the same as the LCD panel 1000C of FIG. 13 except that first and second shield parts SH1 and SH2 have a trench structure as shown in FIG. 7.

[0199] The LCD panel 1000D includes the first shield part SH1, the second shield part SH2 and a connection electrode pattern CEP. The first and second shield parts SH1 and SH2 will be explained with reference to the previous embodiment described in connection with FIG. 7.

[0200] The first shield part SH1 includes a first upper trench TU1 and a first lower trench TD1 to be disposed adjacent to a self data line, that is, the third data line DL3 delivering a data voltage to the third pixel part P3. The gate insulation layer 102, the protection insulation layer 103 and the organic insulation layer 104 are removed to form the first upper trench TU1 and the first lower trench TD1. The sixth pixel electrode PE6 partially overlapped with an upper portion of the third data line DL3 is formed through the first upper trench TU1, and the fifth pixel electrode PE5 partially overlapped with a lower portion of the third data line DL3 is formed through the first lower trench TD 1.

[0201] The second shield part SH2 is disposed adjacent to a neighbor data line, that is the ninth data line DL9, which deliveries a data voltage to a ninth pixel part P9 neighboring the third pixel part P3 along the first direction DI1. The second shield part SH2 includes a second upper trench TU2 and a second lower trench TD2. The gate insulation layer 102, the protection insulation layer 103 and the organic insulation layer 104 are removed to form the second upper trench TU2 and the second lower trench TD2. The fifth pixel electrode PE5 partially overlapped with an upper portion of the ninth data line DL9 is formed through the second upper trench TU2, and the sixth pixel electrode PE6 partially overlapped with a lower portion of the ninth data line DL9 is formed through the second lower trench TD2.

[0202] The first metal pattern may include the connection electrode pattern CEP. The connection electrode pattern CEP is extended from a center portion of the pixel area along the second direction DI2 to be electrically connected to the fifth pixel electrode PE5 disposed in the lower pixel area and the fifth pixel electrode PE5 disposed in the upper pixel area in a plan view. The connection electrode CEP is electrically connected to the fifth pixel electrode PE5 partially overlapped with the third data line DL3 through a ninth contact hole C9, and is electrically connected to the fifth pixel electrode PE5 partially overlapped with the ninth data line DL9 through a tenth contact hole C10.

[0203] In a similar manner to the previous embodiment described in connection with FIGS. 1 to 4, the first and second shield parts SH1 and SH2 may prevent an electric field of the data line or the power line from being leaked, and may prevent a light leakage from being generated between the data line and the power line or between the data line and the pixel electrode. In addition, the first and second shield parts SH1 and SH2 have a structure in which the pixel electrode is formed through a trench, so that an aperture ratio of the display substrate may be enhanced in comparison with the display substrate according to the previous embodiment described in connection with FIGS. 1 to 4.

[0204] A method of manufacturing the display substrate according to the present exemplary embodiment is substantially the same as the method of manufacturing the display substrate described in FIGS. 8A to 8D. In this case, the ninth data line DL9 may be formed when the second metal pattern including the third data line DL3 is formed. Thus, any explanation for the method of manufacturing the display substrate according to the present exemplary embodiment will hereinafter be omitted.

[0205] FIG. 16 is a schematic diagram illustrating an LCD panel 1000E according to another exemplary embodiment of the present invention.

[0206] Referring to FIG. 16, the LCD panel 1000E further includes a first storage line STL1 and a second storage line STL2 in comparison with the LCD panel 1000C of FIG. 13.

[0207] The first storage line STL1 is extended in the second direction DI2 to be disposed adjacent to the first gate line GL1. The first storage line STL1 partially overlaps with extending portions of switching elements included in pixel parts corresponding to a pixel row electrically connected to the first gate line GL1, so that storage capacitors may be formed.

[0208] The second storage line STL2 is extended in the second direction DI2 to be disposed adjacent to the second gate line GL2. The second storage line STL2 partially overlaps with extending portions of switching elements included in pixel parts corresponding to a pixel row electrically connected to the second gate line GL2, so that storage capacitors may be formed. Each storage capacitor may decrease a voltage variation of the pixel part to enhance display quality.

[0209] As shown in FIG. 16, the first and second gate lines GL1 and GL2 may be connected to each other at a peripheral area of the LCD panel. In this case, a gate signal outputted from the gate driving part may be simultaneously applied to the first and second gate lines GL1 and GL2. Moreover, the first and second gate lines GL1 and GL2 may be separated from each other. In this case, the gate driving part may simultaneously output the gate signal to each of the first and second gate lines GL1 and GL2. Accordingly, two pixel rows electrically connected to the first and second gate lines GL1 and GL2 may be simultaneously driven.

[0210] A pixel part according to the present exemplary embodiment may include first and second shield parts SH1 and SH2 formed from the first metal pattern of FIGS. 1 to 4. Alternatively, a pixel part according to the present exemplary embodiment may include first and second shield parts SH1 and SH2 of a trench structure of FIGS. 6 to 8D.

[0211] FIG. 17 is a plan view illustrating an LCD panel 1000E of FIG. 16. Hereinafter, any repetitive detailed explanation about the identical elements of FIGS. 15, 16 and 17 will be omitted or simplified.

[0212] Referring to FIGS. 16 and 17, the LCD panel 1000E includes a third data line DL3, a ninth data line DL9, a first power line VL1, the first gate line GL1, the first storage line STL1 and a third pixel part P3.

[0213] The first gate line GL1 is extended in the second direction DI2.

[0214] The first storage line STL1 is extended in the second direction DI2 to be disposed adjacent to the first gate line GL1.

[0215] The third pixel part P3 includes a fifth switching element T5, a fifth pixel electrode PE5, a sixth switching element T6, a sixth pixel electrode PE6, a first shield part SH1 and a second shield part SH2.

[0216] The fifth switching element T5 includes a fifth gate electrode GE5 connected to the first gate line GL1, a fifth source electrode SE5 connected to the third data line DL3 and a fifth drain electrode DE5 spaced apart from the fifth source electrode SE5. An extending portion of the fifth drain electrode DE5 partially overlaps with the first storage line STL1 to be connected to the fifth pixel electrode PE5 through a first contact hole C1. The extending portion of the fifth drain electrode DE5, the first storage line STL1 partially overlapping with the extending portion and a gate insulation layer (not shown) disposed therebetween may define a first storage capacitor CST1.

[0217] The sixth switching element T6 includes a sixth gate electrode GE6 connected to the first gate line GL1, a sixth source electrode SE6 connected to the first power line VL1 through the first connection line CL1 and a sixth drain electrode DE6 spaced apart from the sixth source electrode SE6. An extending portion of the sixth drain electrode DE6 partially overlaps with the first storage line STL1 to be connected to the sixth pixel electrode PE6 through a fourth contact hole C4. The sixth source electrode SE6 is connected to the first connection line CL1 through a third contact hole C3. The extending portion of the sixth drain electrode DE6, the first storage line STL1 partially overlapping with the extending portion and a gate insulation layer (not shown) disposed therebetween may define a second storage capacitor CST2.

[0218] A method of manufacturing the display substrate according to the present exemplary embodiment is substantially the same as the method of manufacturing the display substrate described in FIGS. 12A to 12C. That is, a first metal pattern includes the first gate line GL1, the second gate line GL2, the first storage line STL1 and the second storage line STL2, and a second metal pattern includes the first to sixteenth data lines DL1, DL2, ..., DL16. Thus, any explanation for the method of manufacturing the display substrate according to the present exemplary embodiment will hereinafter be omitted.

[0219] FIG. 18 is a schematic diagram illustrating an LCD panel according to another exemplary embodiment of the present invention.

[0220] Referring to FIGS. 1 and 18, the LCD panel 1000F includes a pad part 400, a plurality of data lines DL1, DL2, DL3, DL4, DL5, DL6, DL7 and DL8, a first bus line BL1, a second bus line BL2, a first power line VL1, a second power line VL2, a gate line GL, and a plurality of pixel parts P1, P2, P3, P4, P5, P6, P7 and P8. Hereinafter, any repetitive detailed explanation about the identical elements of FIG. 1 will be omitted or simplified.

[0221] The pad part 400 includes a plurality of pads disposed at a first peripheral area PA1 of the LCD panel 1000F to be connected to respective data lines.

[0222] Each of the data lines DL1, DL2, DL3, DL4, DL5, DL6, DL7 and DL8 is extended in the first direction DI1, and is arranged in the second direction DI2.

[0223] The first bus line BL1 may be extended in the second direction DI2 to be disposed in the first peripheral area PA1 of the LCD panel 1000F. The second bus line BL2 may be extended in the second direction DI2 to be disposed in the first peripheral area PA1 adjacent to the first bus line BL1.

[0224] The first power line VL1 is connected to the first bus line BL1 to be extended in the first direction DI1. The second power line VL2 is connected to the second bus line BL2 to be extended in the first direction DI2. A plurality of pixel parts P5, P6, P7 and P8 is arranged between the first and second power lines VL1 and VL2. Each of the first and second power lines VL1 and VL2 provides the pixel parts P1, P2, P3 and P4, and P5, P6, P7 and P8 with a voltage, respectively.

[0225] The gate line GL is extended in the second direction DI2.

[0226] The plural pixel parts P1, P2, P3, P4, P5, P6, P7 and P8 include primary color pixels and a multi-primary color pixel. The primary color pixels may be a red pixel, a green pixel and a blue pixel, and the multi-primary color pixel may include a white pixel, a yellow pixel, a cyan pixel, a magenta pixel, etc. In the present exemplary embodiment, the multi-primary color pixel is a white pixel. When the LCD panel further includes the multi-primary

color pixel, a transmissivity of the LCD panel is enhanced and a range of color reproducibility (or a color range) is wider so that almost every color viewable by a viewer's eye may be reproduced. The first pixel part P1 includes a first pixel electrode PE1, a second pixel electrode PE2, a first switching element T1 and a second switching element T2. The first pixel electrode PE1 is connected to the first data line DL1 and the gate line GL through the first switching element T1. The second pixel electrode PE2 is spaced apart from the first pixel electrode PE1 to be connected to the first power line VL1 and the gate line GL through the second switching element T2. The second switching element T2 is connected to the first power line VL1 through a first connection line CL1.

[0227] The second pixel part P2 includes a third pixel electrode PE3, a fourth pixel electrode PE4, a third switching element T3 and a fourth switching element T4. The third pixel electrode PE3 is connected to the second data line DL2 and the gate line GL through the third switching element T3. The fourth pixel electrode PE4 is spaced apart from the third pixel electrode PE3 to be connected to the first power line VL1 and the gate line GL through the fourth switching element T4. The fourth switching element T4 is connected to the first power line VL1 through the first connection line CL1.

[0228] The third pixel part P3 includes a fifth pixel electrode PE5, a sixth pixel electrode PE6, a fifth switching element T5 and a sixth switching element T6. The fifth pixel electrode PE5 is connected to the third data line DL3 and the gate line GL through the fifth switching element T5. The sixth pixel electrode PE6 is spaced apart from the fifth pixel electrode PE5 to be connected to the first power line VL1 and the gate line GL through the sixth switching element T6. The sixth switching element T6 is connected to the first power line VL1 through the first connection line CL1.

[0229] The fourth pixel part P4 includes a seventh pixel electrode PE7, an eighth pixel electrode PE8, a seventh switching element T7 and an eighth switching element T8. The seventh pixel electrode PE7 is connected to the fourth data line DL4 and the gate line GL through the seventh switching element T7. The eighth pixel electrode PE8 is spaced apart from the seventh pixel electrode PE7 to be connected to the first power line VL1 and the gate line GL through the eighth switching element T8. The eighth switching element T8 is connected to the first power line VL1 through the first connection line CL1.

[0230] The fifth pixel part P5 includes a ninth pixel electrode PE9, a tenth pixel electrode PE10, a ninth switching element T9 and a tenth switching element T10. The ninth pixel electrode PE9 is connected to the fifth data line DL5 and the gate line GL through the ninth switching element T9. The tenth pixel electrode PE10 is spaced apart from the ninth pixel electrode PE9 to be connected to the second power line VL2 and the gate line GL through the tenth switching element T10. The tenth switching element T10 is connected to the second power line VL2 through a second connection line CL2.

[0231] The sixth pixel part P6 includes an eleventh pixel electrode PE11, a twelfth pixel electrode PE12, an eleventh switching element T11 and a twelfth switching element T12. The eleventh pixel electrode PE11 is connected to the sixth data line DL6 and the gate line GL through the eleventh switching element T11. The twelfth pixel electrode PE12 is spaced apart from the eleventh pixel electrode PE11 to be connected to the second power line VL2 and the gate line GL through the twelfth switching element T12. The twelfth switching element T12 is connected to the second power line VL2 through the second connection line CL2.

[0232] The seventh pixel part P7 includes a thirteenth pixel electrode PE13, a fourteenth pixel electrode PE14, a thirteenth switching element T13 and a fourteenth switching element T14. The thirteenth pixel electrode PE13 is connected to the seventh data line DL7 and the gate line GL through the thirteenth switching element T13. The fourteenth pixel electrode PE14 is spaced apart from the thirteenth pixel electrode PE13 to be connected to the second power line VL2 and the gate line GL through the fourteenth switching element T14. The fourteenth switching element T14 is connected to the second power line VL2 through the second connection line CL2.

[0233] The eighth pixel part P8 includes a fifteenth pixel electrode PE15, a sixteenth pixel electrode PE16, a fifteenth switching element T15 and a sixteenth switching element T16. The fifteenth pixel electrode PE15 is connected to the eighth data line DL8 and the gate line GL through the fifteenth switching element T15. The sixteenth pixel electrode PE16 is spaced apart from the fifteenth pixel electrode PE15 to be connected to the second power line VL2 and the gate line GL through the sixteenth switching element T16. The sixteenth switching element T16 is connected to the second power line VL2 through the second connection line CL2.

[0234] A voltage of a first polarity (for example, a negative (-) polarity) with respect to a reference voltage is applied to the first power line VL1, and a voltage of a second polarity (for example, a positive (+) polarity) with respect to the reference voltage is applied to the second power line VL2. A voltage of a second polarity (a positive (+) polarity) having a level higher than a voltage applied to the first power line VL1 is applied to the first, second, third and fourth data lines DL1, DL2, DL3 and DL4, and a voltage of a first polarity (for example, a negative (-) polarity) having a level lower than a voltage applied to the second power line VL2 is applied to the fifth, sixth, seventh and eighth data lines DL5, DL6, DL7 and DL8. For example, a level of the first polarity (-) may be lower than a level of the reference voltage, and a level of the second polarity (+) may be higher than a level of the reference voltage.

[0235] According to the present exemplary embodiment, one power line is shared by four pixel parts and the same polarity data voltage is applied via the one power line, so that a generation of a light leakage in a black state may be minimized. Moreover, the number of the

power lines is decreased, so that an aperture ratio of a display substrate may be enhanced.

[0236] A pixel structure of the fourth pixel part P4 according to the present exemplary embodiment may be substantially the same as that of the third pixel part P3 of FIG. 3. Similar to the previous embodiment described in connection with FIG. 3, the pixel part according to the present exemplary embodiment may include a first shield part SH1 and a second shield part SH2, and the first and second shield parts SH1 and SH2 may be formed from a metal pattern. In this case, a method of manufacturing the display substrate according to the present exemplary embodiment may be substantially the same as that of manufacturing the display substrate described in connection with FIGS. 5A to 5D. However, each of the first and second power lines VL1 and VL2 may be arranged in units of four pixel parts (FIG. 18).

[0237] Moreover, a pixel structure of the fourth pixel part P4 according to the present exemplary embodiment may be substantially the same as that of the third pixel part P3 of FIG. 6. Similar to the previous embodiment described in connection with FIG. 6, the pixel part according to the present exemplary embodiment may include a first shield part SH1 and a second shield part SH2, and the first and second shield parts SH1 and SH2 may be formed in a trench structure. In this case, a method of manufacturing the display substrate according to the present exemplary embodiment may be substantially the same as that of manufacturing the display substrate described in connection with FIGS. 8A to 8D. However, each of the first and second power lines VL1 and VL2 may be arranged in units of four pixel parts.

[0238] FIG. 19 is a schematic diagram illustrating an LCD panel according to another exemplary embodiment of the present invention.

[0239] Referring to FIG. 19, the LCD panel 1000G may further include a storage line STL in comparison with the LCD panel 1000F of FIG. 18.

[0240] The storage line STL is extended in the second direction DI2, and is disposed adjacent to the gate line GL. A storage voltage is applied to the storage line STL. The storage voltage may be a direct current (DC) having a predetermined level in spite of a frame.

[0241] For example, the storage line STL partially overlaps with extending portions of first to sixteenth switching elements T1, T2,..., T16 included in the first, second, third, fourth, fifth, sixth, seventh and eighth pixel parts P1, P2, P3, P4, P5, P6, P7 and P8, so that a plurality of storage capacitors may be defined. A variation of a voltage applied to the pixel parts P1, P2, P3, P4, P5, P6, P7 and P8 is decreased by the storage capacitors, so that display quality may be enhanced.

[0242] A pixel structure of the fourth pixel part P4 according to the present exemplary embodiment may be substantially the same as that of the third pixel part P3 of FIG. 10. Similar to the previous embodiment described in connection with FIG. 10, an extending portion of the seventh switching element of the fourth pixel part P4 according to the present exemplary embodiment may be partially overlapped with the storage line STL to form a first storage capacitor, and an extending portion of the eighth switching element may be partially overlapped with the storage line STL to form a second storage capacitor. In this case, a method of manufacturing the display substrate according to the present exemplary embodiment may be substantially the same as that of manufacturing the display substrate described in connection with FIGS. 12A to 12C. However, each of the first and second power lines VL1 and VL2 may be arranged in units of four pixel parts.

[0243] Moreover, similar to the previous embodiment described in connection with FIGS. 1 to 4, the pixel part according to the present exemplary embodiment may include first and second shield parts SH1 and SH2 of a metal pattern. In this case, a method of manufacturing the display substrate according to the present exemplary embodiment may be substantially the same as the method of manufacturing the display substrate described in FIGS. 5A to 5D.

[0244] Furthermore, similar to the previous embodiment described in connection with FIGS. 6 and 7, the pixel part according to the present exemplary embodiment may include first and second shield parts SH1 and SH2 of a trench structure. In this case, a method of manufacturing the display substrate according to the present exemplary embodiment may be substantially the same as the method of manufacturing the display substrate described in FIGS. 8A to 8D.

[0245] FIG. 20 is a schematic diagram illustrating an LCD panel according to another exemplary embodiment of the present invention.

[0246] Referring to FIG. 20, the LCD panel 1000H includes a plurality of data lines DL1, DL2, DL3, DL4, DL5, DL6, DL7, DL8, DL9, DL10, DL11, DL12, DL13, DL14, DL15 and DL16, a first bus line BL1, a second bus line BL2, a first power line VL1, a second power line VL2, a first gate line GL1, a second gate line GL2, and a plurality of pixel parts P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15 and P16. The plural pixel parts P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15 and P16 include primary color pixels and multi-primary color pixels. The primary color pixels may be a red pixel, a green pixel and a blue pixel, and the multi-primary color pixel may include a white pixel, a yellow pixel, a cyan pixel, a magenta pixel, etc. In the present exemplary embodiment the multi-primary color pixel is a white pixel.

[0247] As with the previous embodiment described in connection with FIG. 18, the first to eighth pixel parts P1, P2, P3, P4, P5, P6, P7 and P8 include first to sixteenth pixel electrodes PE1, PE2, ..., PE16. The first to sixteenth pixel electrodes PE1, PE2, ..., PE16 are electrically connected to the first to eighth data lines DL1, DL2, DL3, DL4, DL5, DL6, DL7 and DL8, the power lines VL1 and VL2 and the first gate line GL1. In this exemplary embodiment, a detailed explanation for a connection struc-

ture concerning the first to eighth pixel parts P1, P2, P3, P4, P5, P6, P7 and P8 will be omitted.

[0248] The second gate line GL2 is extended in the second direction DI2 to be electrically connected to the first gate line GL1. As shown in FIG. 20, the first and second gate lines GL1 and GL2 may be connected to each other at a peripheral area of the LCD panel. In this case, a gate signal outputted from a gate driving part may be simultaneously supplied to the first and second gate lines GL1 and GL2 that are connected to each other. Alternatively, the first and second gate lines GL1 and GL2 may be separated from each other. In this case, a gate driving part may output a gate signal to the first and second gate lines GL1 and GL2 at a same point of time. Thus, two pixel rows respectively and electrically connected to the first and second gate lines GL1 and GL2 may be simultaneously driven.

[0249] The ninth pixel part P9 includes a seventeenth pixel electrode PE17, an eighteenth pixel electrode PE18, a seventeenth switching element T17 and an eighteenth switching element T18. The seventeenth pixel electrode PE17 is connected to the ninth data line DL9 and the second gate line GL2 through the seventeenth switching element T17. The ninth data line DL9 is disposed between the first data line DL1 and the second data line DL2, and is disposed adjacent to the second data line DL2. The eighteenth pixel electrode PE18 is spaced apart from the seventeenth pixel electrode PE17 to be connected to the first power line VL1 and the second gate line GL2 through the eighteenth switching element T18. The eighteenth switching element T18 is connected to the first power line VL1 through a first connection line CL1.

[0250] The tenth pixel part P10 includes a nineteenth pixel electrode PE19, a twentieth pixel electrode PE20, a nineteenth switching element T19 and a twentieth switching element T20. The nineteenth pixel electrode PE19 is connected to the tenth data line DL10 and the second gate line GL2 through the nineteenth switching element T19. The tenth data line DL10 is disposed between the second and third data lines DL2 and DL3, and is disposed adjacent to the third data line DL3. The twentieth pixel electrode PE20 is spaced apart from the nineteenth pixel electrode PE 19 to be connected to the first power line VL1 and the second gate line GL2 through the twentieth switching element T20. The twentieth switching element T20 is connected to the first power line VL1 through the first connection line CL1.

[0251] The eleventh pixel part P11 includes a twenty-first pixel electrode PE21, a twenty-second pixel electrode PE22, a twenty-first switching element T21 and a twenty-second switching element T22. The twenty-first pixel electrode PE21 is connected to the eleventh data line DL11 and the second gate line GL2 through the twenty-first switching element T21. The eleventh data line DL11 is disposed between the third and fourth data lines DL3 and DL4, and is disposed adjacent to the fourth data line DL4. The twenty-second pixel electrode PE22 is spaced apart from the twenty-first pixel electrode PE21 to be connected to the first power line VL1 and the second gate line GL2 through the twenty-second switching element T22. The twenty-second switching element T22 is connected to the first power line VL1 through the first connection line CL1.

[0252] The twelfth pixel part P12 includes a twenty-third pixel electrode PE23, a twenty-fourth pixel electrode PE24, a twenty-third switching element T23 and a twenty-fourth switching element T24. The twenty-third pixel electrode PE23 is connected to the twelfth data line DL12 and the second gate line GL2 through the twenty-third switching element T23. The twelfth data line DL12 is disposed between the fourth data line DL4 and the first power line VL1, and is disposed adjacent to the first power line VL1. The twenty-fourth pixel electrode PE24 is spaced apart from the twenty-third pixel electrode PE23 to be connected to the first power line VL1 and the second gate line GL2 through the twenty-fourth switching element T24. The twenty-fourth switching element T24 is connected to the first power line VL1 through the first connection line CL1.

[0253] The thirteenth pixel part P13 includes a twenty-fifth pixel electrode PE25, a twenty-sixth pixel electrode PE26, a twenty-fifth switching element T25 and a twenty-sixth switching element T26. The twenty-fifth pixel electrode PE25 is connected to the thirteenth data line DL13 and the second gate line GL2 through the twenty-fifth switching element T25. The thirteenth data line DL13 is disposed between the fifth data line DL5 and the sixth data line DL6, and is disposed adjacent to the sixth data line DL6. The twenty-sixth pixel electrode PE26 is spaced apart from the twenty-fifth pixel electrode PE25 to be connected to the second power line VL2 and the second gate line GL2 through the twenty-sixth switching element T26. The twenty-sixth switching element T26 is connected to the second power line VL2 through a second connection line CL2.

[0254] The fourteenth pixel part P14 includes a twenty-seventh pixel electrode PE27, a twenty-eighth pixel electrode PE28, a twenty-seventh switching element T27 and a twenty-eighth switching element T28. The twenty-seventh pixel electrode PE27 is connected to the fourteenth data line DL14 and the second gate line GL2 through the twenty-seventh switching element T27. The fourteenth data line DL14 is disposed between the sixth data line DL6 and the seventh data line DL7, and is disposed adjacent to the seventh data line DL7. The twenty-eighth pixel electrode PE28 is spaced apart from the twenty-seventh pixel electrode PE27 to be connected to the second power line VL2 and the second gate line GL2 through the twenty-eighth switching element T28. The twenty-eighth switching element T28 is connected to the second power line VL2 through the second connection line CL2.

[0255] The fifteenth pixel part P15 includes a twenty-ninth pixel electrode PE29, a thirtieth pixel electrode PE30, a twenty-ninth switching element T29 and a thir-

tieth switching element T30. The twenty-ninth pixel electrode PE29 is connected to the fifteenth data line DL15 and the second gate line GL2 through the twenty-ninth switching element T29. The fifteenth data line DL15 is disposed between the seventh data line DL7 and the eighth data line DL8, and is disposed adjacent to the eighth data line DL8. The thirtieth pixel electrode PE30 is spaced apart from the twenty-ninth pixel electrode PE29 to be connected to the second power line VL2 and the second gate line GL2 through the thirtieth switching element T30. The thirtieth switching element T30 is connected to the second power line VL2 through the second connection line CL2.

[0256] The sixteenth pixel part P16 includes a thirty-first pixel electrode PE31, a thirty-second pixel electrode PE32, a thirty-first switching element T31 and a thirty-second switching element T32. The thirty-first pixel electrode PE31 is connected to the sixteenth data line DL16 and the second gate line GL2 through the thirty-first switching element T31. The sixteenth data line DL16 is disposed between the eighth data line DL8 and the second power line VL2, and is disposed adjacent to the second power line VL2. The thirty-second pixel electrode PE32 is spaced apart from the thirty-first pixel electrode PE31 to be connected to the second power line VL2 and the second gate line GL2 through the thirty-second switching element T32. The thirty-second switching element T32 is connected to the second power line VL2 through the second connection line CL2.

[0257] A voltage of a first polarity (for example, a negative (-) polarity) with respect to a reference voltage is applied to the first power line VL1, and a voltage of a second polarity (for example, a positive (+) polarity) with respect to the reference voltage is applied to the second power line VL2. A voltage of a second polarity (a positive (+) polarity) having a level higher than a voltage applied to the first power line VL1 is applied to the first, second, third, fourth, ninth, tenth, eleventh and twelfth data lines DL1, DL2, DL3, DL4, DL9, DL10, DL11 and DL12, and a voltage of a first polarity (for example, a negative (-) polarity) having a level lower than a voltage applied to the second power line VL2 is applied to the fifth, sixth, seventh, eighth, thirteenth, fourteenth, fifteenth and sixteenth data lines DL5, DL6, DL7, DL8, DL13, DL14, DL15 and DL16.

[0258] According to the present exemplary embodiment, one pixel row receives a data voltage through two data lines, and two pixel columns receive one gate signal through two gate lines, so that two pixel columns may be driven for one horizontal period (1H). That is, the LCD panel 1000H may be driven at a high speed. Moreover, one power line is shared by four pixel parts and the same polarity data voltage is applied via the one power line, so that a generation of a light leakage in a black state may be minimized. Moreover, the number of power lines is decreased, so that an aperture ratio of a display substrate may be enhanced.

[0259] A pixel structure of the fourth pixel part P4 according to the present exemplary embodiment may be substantially the same as that of the third pixel part P3 of FIG. 14. Similar to the previous embodiment described in connection with FIG. 14, the pixel part according to the present exemplary embodiment may include a first shield part SH1 and a second shield part SH2, and the first and second shield parts SH1 and SH2 may be formed from a metal pattern. In this case, a method of manufacturing the display substrate according to the present exemplary embodiment may be substantially the same as that of manufacturing the display substrate described in connection with FIGS. 5A to 5D. However, each of the first and second power lines VL1 and VL2 may be arranged in units of four pixel parts.

[0260] Moreover, a pixel structure of the fourth pixel part P4 according to the present exemplary embodiment may be substantially the same as that of the third pixel part P3 of FIG. 15. Similar to the previous embodiment described in connection with FIG. 15, the pixel part according to the present exemplary embodiment may include a first shield part SH1 and a second shield part SH2, and the first and second shield parts SH1 and SH2 may be formed in a trench structure. In this case, a method of manufacturing the display substrate according to the present exemplary embodiment may be substantially the same as that of manufacturing the display substrate described in connection with FIGS. 8A to 8D. However, each of the first and second power lines VL1 and VL2 may be arranged in units of four pixel parts.

[0261] FIG. 21 is a schematic diagram illustrating an LCD panel according to another exemplary embodiment of the present invention.

[0262] Referring to FIG. 21, the LCD panel 1000I may further include a first storage line STL1 and a second storage line STL2 in comparison with the LCD panel 1000H of FIG. 20.

[0263] The first storage line STL1 is disposed adjacent to the first gate line GL1 in parallel with the first gate line GL1. The first storage line STL1 partially overlaps with respective extending portions of switching elements included in pixel parts corresponding to a pixel row electrically connected to the first gate line GL1, so that a storage capacitor may be formed.

[0264] The second storage line STL2 is disposed adjacent to the second gate line GL2 in parallel with the second gate line GL2. The second storage line STL2 partially overlaps with respective extending portions of switching elements included in pixel parts corresponding to a pixel row electrically connected to the second gate line GL2, so that a storage capacitor may be formed.

[0265] The storage capacitors may decrease voltage variations of the pixel parts to enhance display quality.

[0266] As shown in FIG. 21, the first and second gate lines GL1 and GL2 may be connected to each other at a peripheral area of the LCD panel. In this case, a gate signal outputted from a gate driving part may be simultaneously applied to the first and second gate lines GL1 and GL2 that are connected to each other. Alternatively,

the first and second gate lines GL1 and GL2 may be separated from each other. In this case, the gate driving part may simultaneously output the gate signal to each of the first and second gate lines GL1 and GL2. Accordingly, two pixel rows electrically connected to the first and second gate lines GL1 and GL2 may be simultaneously driven.

[0267] Each of the pixel parts according to the present exemplary embodiment may include first and second shield parts SH1 and SH2 of the metal pattern described in FIGS. 1 to 5D. Alternatively, each of the pixel parts according to the present exemplary embodiment may include first and second shield parts SH1 and SH2 of the trench structure described in FIGS. 6 to 8D.

[0268] A method of manufacturing the display substrate according to the present exemplary embodiment is substantially the same as the method of manufacturing the display substrate described in FIGS. 12A to 12C. That is, a first metal pattern includes the first gate line GL1, the second gate line GL2, the first storage line STL1 and the second storage line STL2, and a second metal pattern includes the first to sixteenth data lines DL1, DL2, ..., DL16. Thus, any explanation for the method of manufacturing the display substrate according to the present exemplary embodiment will hereinafter be omitted.

[0269] FIG. 22 is a schematic diagram illustrating an LCD panel not according to the present invention.

[0270] Referring to FIGS. 1 and 22, the LCD panel 1000J includes a pad part 400, a first bus line BL1, a second bus line BL2, a plurality of first power lines VL11 and VL12, a plurality of second power lines VL21 and VL22, a plurality of data lines DL1, DL2, DL3, DL4, DL5 and DL6, a plurality of connection electrodes CT1 and CT2, a gate line GL and a plurality of pixel parts P1, P2, P3, P4, P5 and P6.

[0271] The pad part 400 includes plural pads 410, 420, 430, 440, 450 and 460 receiving plural data voltages outputted from the data driving part 1030, respectively.

[0272] The first bus line BL1 is extended in the second direction DI2. The first bus line BL1 may be disposed at a first peripheral area PA1 of the LCD panel 1000J. The second bus line BL2 is extended in the second direction DI2. The second bus line BL2 may be disposed at the first peripheral area PA1 adjacent to the first bus line BL1.

[0273] Each of the first power lines VL11 and VL12 is connected to the first bus line BL1 to be extended in the first direction DI1, respectively. Each of the first power lines VL11 and VL12 is electrically connected to two pixel parts to provide two pixel parts with a voltage. For example, the first power line VL11 is disposed between the first pixel part P1 and the second pixel part P2 adjacent to the first pixel part P1 along the second direction DI2 to provide the first and second pixel parts P1 and P2 with a voltage.

[0274] Each of the second power lines VL21 and VL22 is connected to the second bus line BL2 to be extended in the first direction DI1, respectively. Each of the second power lines VL21 and VL22 is electrically connected to one pixel part to provide one pixel part with a voltage. For example, the second power line VL21 is disposed between the third pixel part P3 and the fourth pixel part P4 adjacent to the third pixel part P3 along the second direction DI2 to provide the third pixel part P3 with a voltage.

[0275] The first to sixth data lines DL1, DL2, DL3, DL4, DL5 and DL6 are extended in the first direction DI1, and are arranged in the second direction DI2. The first data line DL1 is directly connected to the first pad 410, the second data line DL2 is connected to the third pad 430 through a first connection electrode CT1, and the third data line DL3 is connected to a second pad 420 through a second connection electrode CT2. The fourth data line DL4 is directly connected to the fourth pad 440, a fifth data line DL5 is connected to a sixth pad 460 through another first connection electrode CT1, and the sixth data line DL6 is connected to the fifth pad 450 through another second connection electrode CT2. The first and second connection electrodes CT1 and CT2 may be a transparent electrode pattern.

[0276] The gate line GL is extended in the second direction DI2.

[0277] The plural pixel parts P1, P2, P3, P4, P5 and P6 include primary color pixels. The primary color pixels may be a red pixel, a green pixel and a blue pixel.

[0278] The first pixel part P1 includes a first pixel electrode PE1, a second pixel electrode PE2, a first switching element T1 and a second switching element T2. The first pixel electrode PE1 is connected to the first data line DL1 and the gate line GL through the first switching element T1. The second pixel electrode PE2 is spaced apart from the first pixel electrode PE1, and is connected to the first power line VL11 and the gate line GL through the second switching element T2.

[0279] The second pixel part P2 includes a third pixel electrode PE3, a fourth pixel electrode PE4, a third switching element T3 and a fourth switching element T4. The third pixel electrode PE3 is connected to the first power line VL11 and the gate line GL through the third switching element T3. The fourth pixel electrode PE4 is spaced apart from the third pixel electrode PE3, and is connected to the second data line DL2 and the gate line GL through the fourth switching element T4.

[0280] The third pixel part P3 includes a fifth pixel electrode PE5, a sixth pixel electrode PE6, a fifth switching element T5 and a sixth switching element T6. The fifth pixel electrode PE5 is connected to the third data line DL3 and the gate line GL through the fifth switching element T5. The sixth pixel electrode PE6 is spaced apart from the fifth pixel electrode PE5, and is connected to the second power line VL21 and the gate line GL through the sixth switching element T6.

[0281] The fourth pixel part P4 includes a seventh pixel electrode PE7, an eighth pixel electrode PE8, a seventh switching element T7 and an eighth switching element T8. The seventh pixel electrode PE7 is connected to the fourth data line DL4 and the gate line GL through the

seventh switching element T7. The eighth pixel electrode PE8 is spaced apart from the seventh pixel electrode PE7, and is connected to the first power line VL12 and the gate line GL through the eighth switching element T8.

[0282] The fifth pixel part P5 includes a ninth pixel electrode PE9, a tenth pixel electrode PE10, a ninth switching element T9 and a tenth switching element T10. The ninth pixel electrode PE9 is connected to the first power line VL12 and the gate line GL through the ninth switching element T9. The tenth pixel electrode PE10 is spaced apart from the ninth pixel electrode PE9, and is connected to the fifth data line DL5 and the gate line GL through the tenth switching element T10.

[0283] The sixth pixel part P6 includes an eleventh pixel electrode PE11, a twelfth pixel electrode PE12, an eleventh switching element T11 and a twelfth switching element T12. The eleventh pixel electrode PE11 is connected to the sixth data line DL6 and the gate line GL through the eleventh switching element T11. The twelfth pixel electrode PE12 is spaced apart from the eleventh pixel electrode PE11, and is connected to the second power line VL22 and the gate line GL through the twelfth switching element T 12.

[0284] A voltage of a first polarity (for example, a negative (-) polarity) with respect to a reference voltage is applied to the first power lines VL11 and VL12, and a voltage of a second polarity (for example, a positive (+) polarity) with respect to the reference voltage is applied to the second power lines VL21 and VL22. A voltage of a second polarity (a positive (+) polarity) having a level higher than a voltage applied to the first power lines VL11 and VL12 is applied to the first, second and sixth data lines DL1, DL2 and DL6, and a voltage of a first polarity (for example, a negative (-) polarity) having a level lower than a voltage applied to the second power lines VL21 and VL22 is applied to the third, fourth and fifth data lines DL3, DL4 and DL5. For example, a level of the first polarity (-) may be lower than a level of the reference voltage, and a level of the second polarity (+) may be higher than a level of the reference voltage.

[0285] According to the present comparative example , the same polarity data voltage is applied to adjacent pixel parts, so that a generation of a light leakage in a black state may be minimized. Moreover, adjacent pixel parts share a power line, so that the number of the power lines is decreased so that an aperture ratio of a display substrate may be enhanced.

[0286] FIG. 23 is a plan view illustrating the LCD panel of FIG. 22. FIG. 24 is a cross-sectional view taken along line IV-IV' of FIG. 23.

[0287] Referring to FIGS. 23 and 24, the LCD panel 1000J includes a display substrate 100J, an opposite substrate 200 and a liquid crystal layer 300. The opposite substrate 200 and the liquid crystal layer 300 may be substantially the same as the opposite substrate 200 and the liquid crystal layer 300 described with reference to FIG. 1, and thus any repetitive detailed explanation may hereinafter be omitted.

[0288] The display substrate 100J includes a first base substrate 101, a first metal pattern, a second metal pattern and a transparent electrode pattern. The display substrate 100J further includes a gate insulation layer 102 covering the first metal pattern, a data insulation layer covering the second metal pattern and a first alignment layer 11 covering the transparent electrode pattern. For one example, the data insulation layer may be formed in a multiple layered structure including a protection insulation layer 103 and an organic insulation layer 104. For another example, the data insulation layer may be formed in a single layer structure including the protection insulation layer 103.

[0289] The first metal pattern includes the gate line GL, a plurality of control electrodes of switching elements T1, T2, T3, T4, T5 and T6 connected to the gate line GL, a first shield part SH1 and a second shield part SH2. The second metal pattern includes the data lines DL1, DL2 and DL3, input electrodes of the switching elements T1, T2, T3, T4, T5 and T6 connected to the data lines DL1, DL2 and DL3, output electrodes of the switching elements T1, T2, T3, T4, T5 and T6 that are spaced apart from the input electrodes, a first power line VL11 and a second power line VL21. The transparent electrode pattern includes a plurality of pixel electrodes PE1, PE2, PE3, PE4, PE5 and PE6, and the first and second connection electrodes CT1 and CT2 shown in FIG. 22.

[0290] Hereinafter, as an example, a pixel structure of the present comparative example will be explained by using the first pixel part P1.

[0291] The first pixel part P1 includes the first switching element T1, the first pixel electrode PE1, the second switching element T2, the second pixel electrode PE2, the first shield part SH1 and the second shield part SH2. The switching element T1 is connected to the first data line DL1 and the gate line GL, and is connected to the first pixel electrode PE1 through a first contact hole C1. The second switching element T2 is connected to the first power line VL11 and the gate line GL, and is connected to the second pixel electrode PE2 through a fourth contact hole C4.

[0292] The first and second pixel electrodes PE1 and PE2 are disposed in an alternating arrangement to receive different voltages from the first data line DL1 and the first power line VL11. Thus, when a horizontal electric field is formed between the first and second pixel electrodes PE1 and PE2, various gradations may be realized.

[0293] In a lower portion of the first pixel part P1, the first pixel electrode PE1 has a first stem portion extending to a center line to partially overlap with the first data line DL1. Moreover, the first pixel electrode PE1 has a first branch portion inclinedly extending from the first stem portion by an angle of about 45 degrees with respect to an extending direction of the gate line GL.

[0294] In the lower portion of the first pixel part P1, the second pixel electrode PE2 has a second stem portion extending to the center line to partially overlap with the first power line VL11. Moreover, the second pixel elec-

trode PE2 has a second branch portion inclinedly extending from the second stem portion by an angle of about -45 degrees with respect to an extending direction of the gate line GL.

[0295] In an upper portion of the first pixel part P1, the first pixel electrode PE1 has a third stem portion extending from the center line to an upper portion of the first pixel part P1 to partially overlap with the first power line VL11. Moreover, the first pixel electrode PE1 has a third branch portion inclinedly extended from the first branch portion by an angle of about 135 degrees with respect to an extending direction of the gate line GL or inclinedly extended from the third stem portion by an angle of about 135 degrees with respect to an extending direction of the gate line GL.

[0296] In an upper portion of the first pixel part P1, the second pixel electrode PE2 has a fourth stem portion extended from the center line to an upper portion of the first pixel part P1 to partially overlap with the first data line DL1. Moreover, the second pixel electrode PE2 has a fourth branch portion inclinedly extended from the second stem portion by an angle of about 135 degrees with respect to an extending direction of the gate line GL or inclinedly extended from the fourth stem portion by an angle of about -45 degrees with respect to an extending direction of the gate line GL.

[0297] Hereinafter, an area adjacent to the first peripheral area PA1 of FIG. 1 will be referred to as an upper portion of the display area DA.

[0298] On an upper portion of the display area DA, a plurality of stem portions of pixel electrodes formed on a first portion of each pixel part may be formed to have a first width, and a plurality of stem portions of pixel electrodes formed on a second portion of each pixel part may be formed to have a second width less than the first width. On a lower portion of the display area DA, a plurality of stem portions of pixel electrodes formed on a second portion of each pixel part may be formed to have a third width, and a plurality of stem portions of pixel electrodes formed on a first portion of each pixel part may be formed to have a fourth width less than the third width. The first and third widths may be the same and the second and fourth widths may be the same. Here, the first portions may be a right portion of each pixel part in the display area DA in a plan view, and the second portions may be a left portion of each pixel part in the display area DA in a plan view.

[0299] Referring again to FIG. 22, more light leakage may be generated between the second pixel part P2 and the third pixel part P3 and between the fifth pixel part P5 and the sixth pixel part P6 in which a polarity of a data voltage is varied, so that light leakage between the second pixel part P2 and the third pixel part P3 and between the fifth pixel part P5 and the sixth pixel part P6, as examples, will hereinafter be described.

[0300] For example, when a plurality of pixel rows (shown in FIG. 22) is arranged on the display area DA in the first direction DI1, a data voltage having a different polarity to a previous data voltage may be sequentially provided to the pixel parts in the first direction DI1 when frames are altered. Since a first polarity data voltage is applied to an upper pixel row of the display area DA in an initial frame interval and a second polarity data voltage is applied to a lower pixel row of the display area DA in a following frame interval, more light leakage may be generated at each right portion of the second pixel part P2 and the fifth pixel part P5 in the upper pixel row and more light leakage may be generated at each left portion of the third pixel part P3 and the sixth pixel parts P6 in the lower pixel row. Similar to the above, an amount of light leakage may be generated in a similar amount at a left portion and a right portion of each pixel part positioned at a middle portion of the display area DA.

[0301] Thus, in order to effectively prevent a light leakage at each portion of the display area DA, on an upper pixel row of the display area DA, stem portions of pixel electrodes corresponding to a right portion of the second and fifth pixel parts P2 and P5 may be formed to have a first width, and stem portions of pixel electrodes corresponding to a left portion of the third and sixth pixel parts P3 and P6 may be formed to have a second width less than the first width. On a lower pixel row of the display area DA stem portions of pixel electrodes corresponding to a right portion of the second and fifth pixel parts P2 and P5 may be formed to have a third width, and stem portions of pixel electrodes corresponding to a left portion of the third and sixth pixel parts P3 and P6 may be formed to have a fourth width greater than the third width.

[0302] As a result, since widths of the stem portions of each pixel electrode of each pixel part are different from each other in accordance with portions of the display area DA, when data voltages inverted at every frame interval are applied thereto, a light leakage may be effectively prevented, which would otherwise be locally generated at some area as the data voltages are applied to the upper and lower portions of the display area DA at a different point of time to have a time interval therebetween.

[0303] The first shield part SH1 is disposed adjacent to a data line electrically connected to a pixel electrode of a self pixel part, the second shield part SH2 is disposed adjacent to a power line electrically connected to a pixel electrode of the self pixel part, and the first and second shield parts SH1 and SH2 are electrically connected to pixel electrodes of the self pixel part.

[0304] For example, the first shield part SH1 is disposed adjacent to the first data line DL1 delivering a data voltage to the first pixel part P1 to include a first upper shield SU1 and a first lower shield SD1. The second shield part SH2 is disposed adjacent to the first power line VL11 delivering a voltage to the first pixel part P1 to include a second upper shield SU2, a second lower shield SD2 and a connection shield SC. The connection shield SC is extended along the second direction DI2 so as to connect the first lower shield SD1 and the second upper shield SU2, so that the first pixel part P1 is divided into

an upper portion and a lower portion.

[0305] The first upper shield SU1 partially overlaps with a fourth stem portion of the second pixel electrode PE2 overlapping with the first data line DL1, and the first lower shield SD1 partially overlaps with a first stem portion of the first pixel electrode PE1 overlapping with the first data line DL1. The second upper shield SU2 partially overlaps with a third stem portion of the first pixel electrode PE1 overlapping with the first power line VL11, and the second lower shield SD2 partially overlaps with a second stem portion of the second pixel electrode PE2 overlapping with the first power line VL11.

[0306] The first lower shield SD1 is connected to the first pixel electrode PE1 through a second contact hole C2, and the second upper shield SU2 is connected to the first pixel electrode PE1 through a sixth contact hole C6. The first upper shield SU1 is connected to the second pixel electrode PE2 through a seventh contact hole C7, and the second lower shield SD2 is connected to the second pixel electrode PE2 through a fifth contact hole C5.

[0307] The first lower shield SD1 overlaps with the first pixel electrode PE1 to receive a voltage equal to a voltage applied to the first pixel electrode PE1, so that it may block a light leakage generated between the first data line DL1 and the first pixel electrode PE1. Moreover, the first upper shield SU1 overlaps with the second pixel electrode PE2 to receive a voltage equal to a voltage applied to the second pixel electrode PE2, so that it may block a light leakage generated between the first data line DL1 and the second pixel electrode PE2. Furthermore, the second lower shield SD2 overlaps with the second pixel electrode PE2 to receive a voltage equal to a voltage applied to the second pixel electrode PE2, so that it may block a light leakage generated between the first power line VL11 and the second pixel electrode PE2. Furthermore, the second upper shield SU2 overlaps with the first pixel electrode PE1 to receive a voltage equal to a voltage applied to the first pixel electrode PE1, so that it may block a light leakage generated between the first power line VL11 and the first pixel electrode PE1.

[0308] Referring to FIG. 24, a metal pattern and a transparent electrode pattern that are formed on a boundary between the first pixel part P1 and the second pixel part P2 may be realized as follows. A first distance 'd11' that is a width of the second lower shield SD2, a second distance 'd12' that is a distance between the second lower shield SD2 and a semiconductor layer 150 formed below the first power line VL11, a third distance 'd13' that is a width of the semiconductor layer 150, a fourth distance 'd14' that is a distance between the semiconductor layer 150 and the first lower shield SD1, and a fifth distance 'd15' that is a width of the second lower shield SD2 may be about 5 μm, about 3 μm, about 9 μm, about 3 μm and about 5 μm, respectively. Moreover, a distance PD between the second pixel electrode PE2 and the fourth pixel electrode PE4 may be about 6.5 μm. Thus, a non-transparent width OA1 may be about 25 μm.

[0309] A metal pattern and a transparent electrode pattern that are formed on a boundary between the second pixel part P2 and the third pixel part P3 may be realized as follows. A first distance 'd21' that is a width of the second lower shield SD2, a second distance 'd22' that is a distance between the second lower shield SD2 and a semiconductor layer 150 formed below the second data line DL2, a third distance 'd23' that is a width of the semiconductor layer 150, a fourth distance 'd24' that is a distance between the semiconductor layers 150 that are formed below the second and third data lines DL2 and DL3, respectively, a fifth distance 'd25' that is a width of the semiconductor layer 150 formed below the third data line DL3, a sixth distance 'd26' that is a distance between the semiconductor layer 150 and the first lower shield SD1, and a seventh distance 'd27' that is a width of the first lower shield SD1 may be about 4 μm, about 2μ m, about 6 μm, about 6 μm, about 6 μm, about 2 μm and about 4 μm, respectively. Moreover, a distance PD between the third pixel electrode PE3 and the fifth pixel electrode PE5 may be about 6.5 μm. Thus, a non-transparent width OA2 may be about 30 μm.

[0310] In this case, when the second and third data lines DL2 and DL3 may be formed to have a greater thickness in a low resistively material such as copper (Cu), the non-transparent width OA1 may be maintained as about 25 μm.

[0311] According to the present comparative example, the first bus line BLI and the second bus line BL2 may be formed on a first peripheral area PA1 due to the first and second power lines VL11 and VL21 that are disposed between pixel rows.

[0312] Thus, a horizontal power line formed along a horizontal direction (or a second direction) is removed from the display area DA, so that an aperture ratio of the LCD panel may be increased. In addition, a voltage drop is generated by a line resistance of the horizontal power line, so that a charge decrease of a pixel electrode generated at a first side of the display area DA may be prevented.

[0313] Moreover, the first connection electrode CT1 which connects the second data line DL2 and the third pad 430 and the second connection electrode CT2 which connects the third data line DL3 and the second pad 420 are electrically separated from each other and cross with each other, so that the pixel parts adjacent to each other share the first power line VL11 and may receive the same polarity data voltages. Therefore, a generation of a light leakage in a black state may be minimized between adjacent pixel parts and the number of the first power lines VL11 is decreased, so that an aperture ratio of a display substrate may be enhanced.

[0314] FIG. 25 is a plan view illustrating an other LCD panel not according to the present invention.

[0315] Referring to FIG. 25, the LCD panel 1000K may be substantially the same as the LCD panel 1000J of FIGS. 22 and 23 except for a first shield part SH1, a second shield part SH2 and a connection electrode pat-

tern CEP. Hereinafter, any repetitive detailed explanation will hereinafter be omitted or simplified.

[0316] In a description of the first and second shield parts SH1 and SH2, the first pixel part P1 as an example will be described with reference to FIGS. 7, 24 and 25.

[0317] The first shield part SH1 includes a first upper trench TU1 and a first lower trench TD1 to be disposed adjacent to a self pixel part, that is, the first data line DL1 delivering a data voltage to the first pixel part P1. The gate insulation layer 102, the protection insulation layer 103 and the organic insulation layer 104 are removed to form the first upper trench TU1 and the first lower trench TD1. The second pixel electrode PE2 partially overlapped with an upper portion of the first data line DL1 is formed through the first upper trench TU1, and the first pixel electrode PE1 partially overlapped with a lower portion of the first data line DL1 is formed through the first lower trench TD1.

[0318] The second shield part SH2 is disposed adjacent to a first power line VL11 which delivers a voltage to the first pixel part P1. The second shield part SH2 includes a second upper trench TU2 and a second lower trench TD2. The gate insulation layer 102, the protection insulation layer 103 and the organic insulation layer 104 are removed to form the second upper trench TU2 and the second lower trench TD2. The first pixel electrode PE1 partially overlapped with an upper portion of the first power line VL11 is formed through the second upper trench TU2, and the second pixel electrode PE2 partially overlapped with a lower portion of the first power line VL11 is formed through the second lower trench TD2.

[0319] The connection electrode pattern CEP may be the first metal pattern. The connection electrode pattern CEP is extended from a center portion of the pixel area along the second direction DI2 to be electrically connected to the first pixel electrode PE1 disposed below the center portion of the pixel area and the first pixel electrode PE1 disposed above the center portion of the pixel area in a plan view. The connection electrode CEP is electrically connected to the first pixel electrode PE1 partially overlapped with the first data line DL1 through a ninth contact hole C9, and is electrically connected to the first pixel electrode PE1 partially overlapped with the first power line VL11 through a tenth contact hole C10.

[0320] Similar to the previous embodiment described in connection with FIGS. 1 to 4, the first and second shield parts SH1 and SH2 may prevent an electric field of the data line or the power line from being leaked, and may prevent a light leakage from being generated between the power line and the pixel electrode or between the data line and the pixel electrode. In addition, the first and second shield parts SH1 and SH2 have a structure in which the pixel electrode is formed through a trench, so that an aperture ratio of the display substrate may be enhanced in comparison with the display substrate according to the previous embodiment described in connection with FIGS. 1 to 4.

[0321] FIG. 26 is a plan view illustrating an other LCD panel 1000L not according to the present invention.

[0322] Referring to FIG. 26, the LCD panel 1000L further includes a storage line STL formed from a first metal pattern in comparison with the LCD panel 1000J of FIGS. 22 and 23.

[0323] The storage line STL is extended in the second direction DI2, and is disposed adjacent to the gate line GL. A storage voltage is applied to the storage line STL. The storage voltage may be a direct current (DC) having a predetermined level in spite of a frame.

[0324] For example, the storage line STL partially overlaps with extending portions extended from a drain electrode of the first switching element T1 included in the first pixel part P1 to form a first storage capacitor CST1, and partially overlaps with extending portions extended from a drain electrode of the second switching element T2 to form a second storage capacitor CST2. A variation of a voltage applied to the first pixel part P1 is decreased by the first and second storage capacitors, so that display quality may be enhanced.

[0325] The pixel part according to the present comparative example may include the first and second shield parts SH1 and SH2 formed as a first metal pattern, in a similar manner to an exemplary embodiment described in connection with FIGS. 1 to 4. Alternatively, the pixel part may include the first and second shield parts SH1 and SH2 of a trench structure, in a similar manner to another exemplary embodiment described in connection with FIGS. 6 and 7.

[0326] FIG. 27 is a plan view illustrating an other LCD panel 1000M not according to the present invention.

[0327] Referring to FIGS. 1 and 27, the LCD panel 1000M includes a pad part 400, a plurality of data lines DL1, DL2, DL3, DL4, DL5, DL6, DL7 and DL8, a first bus line BL1, a second bus line BL2, a first power line VL1, a second power line VL2, a first gate line GL1, a second gate line GL2, a third gate line GL3, a fourth gate line GL4 and a plurality of pixel parts P1, P2, P3, P4, P5, P6, P7 and P8. The plural pixel parts P1, P2, P3, P4, P5, P6, P7 and P8 include primary color pixels. The primary color pixels may be a red pixel, a green pixel and a blue pixel.

[0328] The pad part 400 includes a plurality of pads disposed at a first peripheral area PA1 of the LCD panel 1000M to be connected to respective data lines.

[0329] Each of the data lines DL1, DL2, DL3, DL4, DL5, DL6, DL7 and DL8 is extended in the first direction DI1, and is arranged in the second direction DI2.

[0330] The first bus line BL1 may be extended in the second direction DI2 to be disposed on the first peripheral area PA1 of the LCD panel 1000M. The second bus line BL2 may be extended in the second direction DI2 to be disposed on the first peripheral area PA1 adjacent to the first bus line BL1.

[0331] The first power line VL1 is connected to the first bus line BL1 to be extended in the first direction DI1. The second power line VL2 is connected to the second bus line BL2 to be extended in the first direction DI2. The first power line VL1 is disposed between two pixel rows ad-

jacent to each other to provide pixel parts P1 and P3 of the pixel rows with a voltage, and the second power line VL2 is disposed between two pixel rows adjacent to each other to provide pixel parts P5 and P7 of the pixel rows with a voltage.

[0332] The first, second, third and fourth gate lines GL1, GL2, GL3 and GL4 are extended in the second direction DI2 to be arranged in the first direction DI1. The first, second, third and fourth gate lines GL1, GL2, GL3 and GL4 are electrically connected to each other to receive the same gate signal. As shown in FIG. 27, the first to fourth gate lines GL1, GL2, GL3 and GL4 may be connected to each other at a peripheral area of the LCD panel 1000M. In this case, a gate signal outputted from the gate driving part may be simultaneously applied to the first, second, third and fourth gate lines GL1, GL2, GL3 and GL4. Alternatively, the first to fourth gate lines GL1, GL2, GL3 and GL4 may be separated from each other. In this case, the gate driving part may simultaneously output the gate signal to each of the first to fourth gate lines GL1, GL2, GL3 and GL4. Accordingly, two pixel rows electrically connected to the first to fourth gate lines GL1, GL2, GL3 and GL4 may be simultaneously driven.

[0333] The plural pixel parts P1, P2, P3, P4, P5, P6, P7 and P8 include primary color pixels. The primary color pixels may be a red pixel, a green pixel and a blue pixel.

[0334] The first pixel part P1 includes a first pixel electrode PE1, a second pixel electrode PE2, a first switching element T1 and a second switching element T2. The first pixel electrode PE1 is connected to the first data line DL1 and the first gate line GL1 through the first switching element T1. The second pixel electrode PE2 is spaced apart from the first pixel electrode PE1 to be connected to the first power line VL1 and the second gate line GL2 through the second switching element T2.

[0335] The second pixel part P2 is adjacent to the first pixel part P1 along the first direction DI1 to include a third pixel electrode PE3, a fourth pixel electrode PE4, a third switching element T3 and a fourth switching element T4. The third pixel electrode PE3 is connected to the second data line DL2 and the fourth gate line GL4 through the third switching element T3. The fourth pixel electrode PE4 is spaced apart from the third pixel electrode PE3 to be connected to the first power line VL1 and the third gate line GL3 through the fourth switching element T4.

[0336] The third pixel part P3 is adjacent to the first pixel part P1 along the second direction DI2 to include a fifth pixel electrode PE5, a sixth pixel electrode PE6, a fifth switching element T5 and a sixth switching element T6. The fifth pixel electrode PE5 is connected to the fourth data line DL4 and the first gate line GL1 through the fifth switching element T5. The sixth pixel electrode PE6 is spaced apart from the fifth pixel electrode PE5 to be connected to the first power line VL1 and the second gate line GL2 through the sixth switching element T6.

[0337] The fourth pixel part P4 is adjacent to the second pixel part P2 along the second direction DI2 to include a seventh pixel electrode PE7, an eighth pixel electrode PE8, a seventh switching element T7 and an eighth switching element T8. The seventh pixel electrode PE7 is connected to the third data line DL3 and the fourth gate line GL4 through the seventh switching element T7. The eighth pixel electrode PE8 is spaced apart from the seventh pixel electrode PE7 to be connected to the first power line VL1 and the third gate line GL3 through the eighth switching element T8.

[0338] The fifth pixel part P5 is adjacent to the third pixel part P3 along the second direction DI2 to include a ninth pixel electrode PE9, a tenth pixel electrode PE10, a ninth switching element T9 and a tenth switching element T10. The ninth pixel electrode PE9 is connected to the fifth data line DL5 and the first gate line GL1 through the ninth switching element T9. The tenth pixel electrode PE10 is spaced apart from the ninth pixel electrode PE9 to be connected to the second power line VL2 and the second gate line GL2 through the tenth switching element T10.

[0339] The sixth pixel part P6 is adjacent to the fifth pixel part P5 along the first direction DI1 to include an eleventh pixel electrode PE11, a twelfth pixel electrode PE12, an eleventh switching element T11 and a twelfth switching element T12. The eleventh pixel electrode PE11 is connected to the sixth data line DL6 and the fourth gate line GL4 through the eleventh switching element T11. The twelfth pixel electrode PE12 is spaced apart from the eleventh pixel electrode PE11 to be connected to the second power line VL2 and the third gate line GL3 through the twelfth switching element T 12.

[0340] The seventh pixel part P7 is adjacent to the fifth pixel part P5 along the second direction DI2 to include a thirteenth pixel electrode PE13, a fourteenth pixel electrode PE14, a thirteenth switching element T13 and a fourteenth switching element T14. The thirteenth pixel electrode PE13 is connected to the eighth data line DL8 and the first gate line GL1 through the thirteenth switching element T13. The fourteenth pixel electrode PE14 is spaced apart from the thirteenth pixel electrode PE13 to be connected to the second power line VL2 and the second gate line GL2 through the fourteenth switching element T14.

[0341] The eighth pixel part P8 is adjacent to the seventh pixel part P7 along the first direction DI1 to include a fifteenth pixel electrode PE15, a sixteenth pixel electrode PE16, a fifteenth switching element T15 and a sixteenth switching element T16. The fifteenth pixel electrode PE15 is connected to the seventh data line DL7 and the fourth gate line GL4 through the fifteenth switching element T15. The sixteenth pixel electrode PE16 is spaced apart from the fifteenth pixel electrode PE15 to be connected to the second power line VL2 and the third gate line GL3 through the sixteenth switching element T16.

[0342] A voltage of a first polarity (for example, a negative (-) polarity) with respect to a reference voltage is applied to the first power line VL1, and a voltage of a second polarity (for example, a positive (+) polarity) with

respect to the reference voltage is applied to the second power line VL2. A voltage of a second polarity (a positive (+) polarity) having a level higher than a voltage applied to the first power line VL1 is applied to the first, second, third and fourth data lines DL1, DL2, DL3 and DL4, and a voltage of a first polarity (for example, a negative (-) polarity) having a level lower than a voltage applied to the second power line VL2 is applied to the fifth, sixth, seventh and eighth data lines DL5, DL6, DL7 and DL8. For example, a level of the first polarity (-) may be lower than a level of the reference voltage, and a level of the second polarity (+) may be higher than a level of the reference voltage.

[0343] According to the present comparative example, one pixel row receives a data voltage through two data lines and two pixel columns receive one gate signal through four gate lines, so that two pixel columns may be driven for one horizontal period (1H). That is, the LCD panel 1000M may be driven at a high speed. Moreover, one power line is shared by two pixel parts and the same polarity data voltage is applied via the one power line, so that a generation of a light leakage in a black state may be minimized. Moreover, the number of the power lines is decreased, so that an aperture ratio of a display substrate may be enhanced.

[0344] The pixel parts according to the present comparative example may include the first and second shield parts SH1 and SH2 similar to an exemplary embodiment described in connection with FIGS. 1 to 4 and another exemplary embodiment described in connection with FIGS. 6 and 7. The first shield part SH1 is disposed adjacent to a data line electrically connected to a pixel electrode of a self pixel part, the second shield part SH2 is disposed adjacent to a power line electrically connected to a pixel electrode of the self pixel part, and the first and second shield parts SH1 and SH2 are electrically connected to pixel electrodes of the self pixel part. That is, in a similar manner to the previous exemplary embodiment described in connection with FIGS. 1 to 4, the first and second shield parts SH1 and SH2 may be formed from a first metal pattern. Alternatively, in a similar manner to the previous exemplary embodiment described in connection with FIGS. 6 and 7, the first and second shield parts SH1 and SH2 may be formed of a trench structure. The LCD panel 1000M according to the present comparative example may further include first to fourth storage lines adjacent to the first to fourth gate lines, respectively.

[0345] FIG. 28 is a plan view illustrating an other LCD panel 1000N not according to the present invention.

[0346] Referring to FIG. 28, the LCD panel 1000N includes a plurality of data lines DL1, DL2, DL3 and DL4, a gate line GL, a first power line VL1, a second power line VL2 and a plurality of pixel parts P1, P2 and P3.

[0347] The data lines DL1, DL2, DL3 and DL4 are extended in a first direction DI1, and are arranged in a second direction DI2 crossing the first direction DI1.

[0348] The gate line GL is extended in the second direction DI2.

[0349] The first power line VL1 is extended in the second direction DI2, and is disposed adjacent to the gate line GL.

[0350] The second power line VL2 is extended in the second direction DI2, and is disposed adjacent to the first power line VL1.

[0351] The first pixel part P1 includes a first pixel electrode PE1, a second pixel electrode PE2, a first switching element T1, a second switching element T2, a connection electrode pattern CEP, a first shield part SH1 and a second shield part SH2. The first pixel electrode PE1 is connected to the first data line DL1 and the gate line GL through the first switching element T1. The second pixel electrode PE2 is spaced apart from the first pixel electrode PE1, and is connected to the first power line VL1 and the gate line GL through the second switching element T2.

[0352] The connection electrode pattern CEP may be the first metal pattern. The connection electrode pattern CEP is extended in the second direction DI2 at a center portion of the pixel part area to electrically connect with a first pixel electrode PE1 disposed below the center portion of the pixel part area and the first pixel electrode PE1 disposed above the center portion of the pixel part area. The connection electrode pattern CEP is electrically connected to the first pixel electrode PE1 partially overlapped with the first data line DL1 through a ninth contact hole C9, and is electrically connected to the first pixel electrode PE1 partially overlapped with the second data line DL2 through a tenth contact hole C10.

[0353] Referring to FIG. 7, the first shield part SH1 is disposed adjacent to a self data line, that is, the first data line DL1, which delivers a data voltage to the first pixel part P1. The first shield part SH1 includes a first upper trench TU1 and a first lower trench TD1. The gate insulation layer 102, the protection insulation layer 103 and the organic insulation layer 104 are removed to form the first upper trench TU1 and the first lower trench TD1. The second pixel electrode PE2 partially overlapped with an upper portion of the first data line DL1 is formed through the first upper trench TU1, and the first pixel electrode PE1 partially overlapped with a lower portion of the first data line DL1 is formed through the first lower trench TD1. The second shield part SH2 is disposed adjacent to a neighboring data line, which is the second data line DL2, which delivers a data voltage to a neighboring pixel part P2. The second shield part SH2 includes a second upper trench TU2 and a second lower trench TD2. The gate insulation layer 102, the protection insulation layer 103 and the organic insulation layer 104 are removed to form the second upper trench TU2 and the second lower trench TD2. The first pixel electrode PE1 partially overlapped with an upper portion of the second data line DL2 is formed through the second upper trench TU2, and the second pixel electrode PE2 partially overlapped with a lower portion of the second data line DL2 is formed through the second lower trench TD2.

[0354] In a similar manner to the previous exemplary

embodiment described in connection with FIGS. 1 to 4, the first and second shield parts SH1 and SH2 may prevent an electric field of the data line or the power line from being leaked, and may prevent a light leakage from being generated between the power line and the pixel electrode or between the data line and the pixel electrode. In addition, the first and second shield parts SH1 and SH2 have a structure in which the pixel electrode is formed through a trench, so that an aperture ratio of the display substrate may be enhanced in comparison with the display substrate according to the previous exemplary embodiment described in connection with FIGS. 1 to 4.

[0355] As described above, according to exemplary embodiments of the present invention, pixel parts adjacent to each other in the display substrate have a same polarity, so that a light leakage may be prevented. Moreover, one power line is shared by the pixel parts adjacent to each other, so that an aperture ratio of a display substrate may be enhanced.

[0356] The foregoing is illustrative of the present invention and is not to be construed as limiting thereof. It will be apparent to those skilled in the art that various modifications and variations can be made in the present invention without departing from the scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims.

Claims

1. A liquid crystal display device, comprising:

a first substrate (100) and an opposed second substrate (200) with a liquid crystal layer (300) disposed between the opposed substrates (100, 200);
a gate line (GL) disposed on the first substrate (100);
a first data line (DL2), a second data line (DL3) and a first power line (VL1) that are disposed on the first substrate (100), insulated from the gate line (GL) and crossing the gate line (GL);
a first switching element (T3) electrically connected to the gate line (GL) and the first data line (DL2);
a second switching element (T4) electrically connected to the gate line (GL) and the first power line (VL1);
a third switching element (T5) electrically connected to the gate line (GL) and the second data line (DL3);
a fourth switching element (T6) electrically connected to the gate line (GL) and the first power line (VL1); and
a first pixel (P2) including a first pixel electrode (PE3) and a second pixel electrode (PE4) and a second pixel (P3) including a third pixel electrode (PE5) and a fourth pixel electrode (PE6), wherein the first to fourth pixel electrodes (PE3-PE6) are arranged in the same layer and are respectively connected to the first switching element (T3), the second switching element (T4), the third switching element (T5) and the fourth switching element (T6),
a first bus line (BL1) disposed in parallel with the gate line (GL) and connected to the first power line (VL1);
a third data line (DL4), a fourth data line (DL5) and a second power line (VL2) that are insulated from the gate line (GL) and cross the gate line (GL);
a fifth switching element (T7) electrically connected to the gate line (GL) and the third data line (DL4);
a sixth switching element (T8) electrically connected to the gate line (GL) and the second power line (VL2);
a seventh switching element (T9) electrically connected to the gate line (GL) and the fourth data line (DL5);
an eighth switching element (T10) electrically connected to the gate line (GL) and the second power line (VL2);
a third pixel (P4) including a fifth pixel electrode (PE7) and a sixth pixel electrode (PE8) and a fourth pixel (P5) including a seventh pixel electrode (PE9) and an eighth pixel electrode (PE10), wherein the fifth to eighth pixel electrodes (PE7-PE10) are arranged in the same layer and are respectively connected to the fifth switching element (T7), the sixth switching element (T8), the seventh switching element (T9) and the eighth switching element (T10); and
a second bus line (BL2) disposed in parallel with the gate line (GL) to be connected to the second power line (VL2),
wherein the first power line (VL1) is configured to receive from the first bus line (BL1) a voltage of a first polarity with respect to a reference voltage, and the second power line (VL2) is configured to receive from the second bus line (BL2) a voltage of a second polarity with respect to the reference voltage, the first voltage polarity being opposite to the second voltage polarity.

2. The liquid crystal display device of claim 1, further comprising a connection line (CL2) connected to the second power line (VL2),
wherein the sixth switching element (T8) is electrically connected to the second power line (VL2) through the connection line (CL2), and
the eighth switching element (T10) is electrically connected to the second power line (VL2) through the connection line (CL2).

3. The liquid crystal display device of claim 1, further comprising:

a first shield pattern (SD1, SC, SU2) electrically connected to the third pixel electrode (PES) for shielding electric fields and light; and
a second shield pattern (SU1, SD2) electrically connected to the fourth pixel electrode (PE6) for shielding electric fields and light.

4. The liquid crystal display device of claim 3, further comprising a connection line (CL1) connected to the first power line (VL1),
wherein a portion of the first shield pattern (SD1, SC, SU2) overlaps with the third pixel electrode (PE5).

5. The liquid crystal display device of claim 4, wherein the connection line (CL1) is disposed in the same layer as the first pixel electrode (PE3), the second pixel electrode (PE4), the third pixel electrode (PE5) and the fourth pixel electrode (PE6).

6. The liquid crystal display device of claim 1, further comprising a connection line (CL1) connected to the first power line (VL1),
wherein the connection line (CL1) is disposed in the same layer as the first pixel electrode (PE3), the second pixel electrode (PE4), the third pixel electrode (PE5) and the fourth pixel electrode (PE6).

7. The liquid crystal display device of claim 6, wherein the polarity of a voltage applied to the first pixel electrode (PE3) is different from the polarity of a voltage applied to the second pixel electrode (PE4) with respect to a reference voltage.

8. The liquid crystal display device of claim 3, wherein a portion of the first shield pattern (SD1, SC, SU2) overlaps with the third pixel electrode (PE5).

Patentansprüche

1. Flüssigkristallanzeige, umfassend:

ein erstes Substrat (100) und ein gegenüberliegendes zweites Substrat (200) mit einer zwischen den einander gegenüberliegenden Substraten (100, 200) angeordneten Flüssigkristallschicht (300);
eine Gate-Leitung (GL), die auf dem ersten Substrat (100) angeordnet ist;
eine erste Datenleitung (DL2), eine zweite Datenleitung (DL3) und eine erste Stromleitung (VL1), die auf dem ersten Substrat (100) angeordnet sind, von der Gate-Leitung (GL) isoliert sind und die Gate-Leitung (GL) kreuzen;
ein erstes Schaltelement (T3), das mit der Gate-Leitung (GL) und der ersten Datenleitung (DL2) elektrisch verbunden ist;
ein zweites Schaltelement (T4), das mit der Gate-Leitung (GL) und der ersten Stromleitung (VL1) elektrisch verbunden ist;
ein drittes Schaltelement (T5), das mit der Gate-Leitung (GL) und der zweiten Datenleitung (DL3) elektrisch verbunden ist;
ein viertes Schaltelement (T6), das mit der Gate-Leitung (GL) und der ersten Stromleitung (VL1) elektrisch verbunden ist;
ein erstes Pixel (P2), umfassend eine erste Pixelelektrode (PE3) und eine zweite Pixelelektrode (PE4), und ein zweites Pixel (P3), umfassend eine dritte Pixelelektrode (PE5) und eine vierte Pixelelektrode (PE6), wobei die ersten bis vierten Pixelelektroden (PE3-PE6) in der gleichen Schicht angeordnet sind und jeweils mit dem ersten Schaltelement (T3), dem zweiten Schaltelement (T4), dem dritten Schaltelement (T5) und dem vierten Schaltelement (T6) verbunden sind;
eine erste Busleitung (BL1), die parallel zur Gate-Leitung (GL) angeordnet ist und mit der ersten Stromleitung (VL1) verbunden ist;
eine dritte Datenleitung (DL4), eine vierte Datenleitung (DL5) und eine zweite Stromleitung (VL2), die von der Gate-Leitung (GL) isoliert sind und die Gate-Leitung (GL) kreuzen;
ein fünftes Schaltelement (T7), das mit der Gate-Leitung (GL) und der dritten Datenleitung (DL4) elektrisch verbunden ist;
ein sechstes Schaltelement (T8), das mit der Gate-Leitung (GL) und der zweiten Stromleitung (VL2) elektrisch verbunden ist;
ein siebentes Schaltelement (T9), das mit der Gate-Leitung (GL) und der vierten Datenleitung (DL5) elektrisch verbunden ist;
ein achtes Schaltelement (T10), das mit der Gate-Leitung (GL) und der zweiten Stromleitung (VL2) elektrisch verbunden ist;
ein drittes Pixel (P4), umfassend eine fünfte Pixelelektrode (PE7) und eine sechste Pixelelektrode (PE8), und ein viertes Pixel (P5), umfassend eine siebente Pixelelektrode (PE9) und eine achte Pixelelektrode (PE10), wobei die fünften bis achten Pixelelektroden (PE7-PE10) in der gleichen Schicht angeordnet sind und jeweils mit dem fünften Schaltelement (T7), dem sechsten Schaltelement (T8), dem siebenten Schaltelement (T9) und dem achten Schaltelement (T10) verbunden sind;
eine zweite Busleitung (BL2), die parallel zur Gate-Leitung (GL) angeordnet ist, um mit der zweiten Stromleitung (VL2) verbunden zu werden;
wobei die erste Stromleitung (VL1) dafür ausgelegt ist, von der ersten Busleitung (BL1) eine

Spannung mit einer ersten Polarität in Bezug auf eine Referenzspannung zu empfangen, und wobei die zweite Stromleitung (VL2) dafür ausgelegt ist, von der zweiten Busleitung (BL2) eine Spannung mit einer zweiten Polarität in Bezug auf die Referenzspannung zu empfangen, wobei die Polarität der ersten Spannung der Polarität der zweiten Spannung entgegengesetzt ist.

2. Flüssigkristallanzeige nach Anspruch 1, ferner umfassend eine Verbindungsleitung (CL2), die mit der zweiten Stromleitung (VL2) verbunden ist,
wobei das sechste Schaltelement (T8) über die Verbindungsleitung (CL2) mit der zweiten Stromleitung (VL2) elektrisch verbunden ist; und
das achte Schaltelement (T10) über die Verbindungsleitung (CL2) mit der zweiten Stromleitung (VL2) elektrisch verbunden ist.

3. Flüssigkristallanzeige nach Anspruch 1, ferner umfassend:

ein erstes Abschirmungsmuster (SD1, SC, SU2), das mit der dritten Pixelelektrode (PE5) elektrisch verbunden ist, um elektrische Felder und Licht abzuschirmen; und
ein zweites Abschirmungsmuster (SU1, SD2), das mit der vierten Pixelelektrode (PE6) elektrisch verbunden ist, um elektrische Felder und Licht abzuschirmen.

4. Flüssigkristallanzeige nach Anspruch 3, ferner umfassend eine Verbindungsleitung (CL1), die mit der ersten Stromleitung (VL1) verbunden ist,
wobei ein Teil des ersten Abschirmungsmusters (SD1, SC, SU2) die dritte Pixelelektrode (PE5) überlappt.

5. Flüssigkristallanzeige nach Anspruch 4, wobei die Verbindungsleitung (CL1) in der gleichen Schicht wie die erste Pixelelektrode (PE3), die zweite Pixelelektrode (PE4), die dritte Pixelelektrode (PE5) und die vierte Pixelelektrode (PE6) angeordnet ist.

6. Flüssigkristallanzeige nach Anspruch 1, ferner umfassend eine Verbindungsleitung (CL1), die mit der ersten Stromleitung (VL1) verbunden ist;
wobei die Verbindungsleitung (CL1) in der gleichen Schicht wie die erste Pixelelektrode (PE3), die zweite Pixelelektrode (PE4), die dritte Pixelelektrode (PE5) und die vierte Pixelelektrode (PE6) angeordnet ist.

7. Flüssigkristallanzeige nach Anspruch 6, wobei sich die Polarität einer an die erste Pixelelektrode (PE3) angelegten Spannung von der Polarität einer an die zweite Pixelelektrode (PE4) angelegten Spannung unter Bezugnahme auf eine Referenzspannung unterscheidet.

8. Flüssigkristallanzeige nach Anspruch 3, wobei ein Teil des ersten Abschirmungsmusters (SD1, SC, SU2) die dritte Pixelelektrode (PE5) überlappt.

Revendications

1. Un dispositif d'affichage à cristaux liquides comprenant :

Un premier substrat (100) et un deuxième substrat opposé (200) avec une couche de cristaux liquides disposée entre les substrats opposés (100, 200) ;
Une ligne de barrière (GL) disposée sur le premier substrat (100) ;
Une première ligne de données (DL2), une deuxième ligne de données (DL3) et une première ligne d'alimentation (VL1) qui sont disposées sur le premier substrat (100), isolée de la ligne de barrière (GL) et traversant la ligne de barrière (GL) ;
Un premier élément de commutation (T3) électriquement connecté à la ligne de barrière (GL) et à la première ligne de données (DL2) ;
Un deuxième élément de commutation (T4) électriquement connecté à la ligne de barrière (GL) et à la première ligne d'alimentation (VL1) ;
Un troisième élément de commutation (T5) électriquement connecté à la ligne de barrière (GL) et à la deuxième ligne de données (DL3) ;
Un quatrième élément de commutation (T6) électriquement connecté à la ligne de barrière (GL) et à la première ligne d'alimentation (VL1) ; et
Un premier pixel (P2) comprenant une première électrode de pixel (PE3) et une deuxième électrode de pixel (PE4) et un deuxième pixel (P3) comprenant une troisième électrode de pixel (PE5) et une quatrième électrode de pixel (PE6), où la première à la quatrième électrode de pixel (PE3-PE6) sont disposées dans la même couche et sont respectivement connectées au premier élément de commutation (T3), au deuxième élément de commutation (T4), au troisième élément de commutation (T5) et au quatrième élément de commutation (T6),
Une première ligne de bus (BL1) disposée en parallèle avec la ligne de barrière (GL) et connectée à la première ligne d'alimentation (VL1) ;
Une troisième ligne de données (DL4), une quatrième ligne de données (DL5) et une deuxième ligne d'alimentation (VL2) qui sont isolées de la ligne de barrière (GL) et traversent la ligne de barrière (GL) ;
Un cinquième élément de commutation (T7)

électriquement connecté à la ligne de barrière (GL) et à la troisième ligne de données (DL4) ;
Un sixième élément de commutation (T8) électriquement connecté à la ligne de barrière (GL) et à la deuxième ligne d'alimentation (VL2) ;
Un septième élément de commutation (T9) électriquement connecté à la ligne de barrière (GL) et à la quatrième ligne de données (DL5) ;
Un huitième élément de commutation (T10) électriquement connecté à la ligne de barrière (GL) et à la deuxième ligne d'alimentation (VL2) ;
Un troisième pixel (P4) comprenant une cinquième électrode de pixel (PE7) et une sixième électrode de pixel (PE8) et un quatrième pixel (P5) comprenant une septième électrode de pixel (PE9) et une huitième électrode de pixel (PE10), où les cinquième à huitième électrodes de pixel (PE7 - PE10) sont disposées dans la même couche et sont respectivement connectées au cinquième élément de commutation (T7), le sixième élément de commutation (T8), le septième élément de commutation (T9) et le huitième élément de commutation (T10) ; et
Une deuxième ligne de bus (BL2) disposée en parallèle avec la ligne de barrière (GL) pour être connectée à la deuxième ligne d'alimentation (VL2),
Où la première ligne d'alimentation (VL1) est configurée pour recevoir à partir de la première ligne de bus (BL1) une tension d'une première polarité par rapport à une tension de référence, et la deuxième ligne d'alimentation (VL2) est configurée pour recevoir à partir de la deuxième ligne de bus (BL2) une tension d'une deuxième polarité par rapport à la tension de référence, la polarité de la première tension étant opposée à la deuxième polarité de tension.

2. Le dispositif d'affichage à cristaux liquides de la revendication 1, comprenant de plus une ligne de connexion (CL2) connectée à la deuxième ligne d'alimentation (VL2),
Où le sixième élément de commutation (T8) est électriquement connecté à la deuxième ligne d'alimentation (VL2) au travers de la ligne de connexion (CL2), et
Le huitième élément de commutation (T10) est électriquement connecté à la deuxième ligne d'alimentation (VL2) au travers de la ligne de connexion (CL2).

3. Le dispositif d'affichage à cristaux liquides de la revendication 1, comprenant de plus :

Un premier modèle de protection (SD1, SC, SU2) électriquement connecté à la troisième électrode de pixel (PE5) pour protéger des champs électrique et de la lumière ; et
Un deuxième modèle de protection (SU1, SD2) électriquement connecté à la quatrième électrode de pixel (PE6) pour protéger des champs électriques et de la lumière.

4. Le dispositif d'affichage à cristaux liquides de la revendication 3, comprenant de plus une ligne de connexion (CL1) connectée à la première ligne d'alimentation (VL1),
Où une portion du premier modèle de protection (SD1, SC, SU2) chevauche la troisième électrode de pixel (PE5).

5. Le dispositif d'affichage à cristaux liquides de la revendication 4, où la ligne de connexion (CL1) est disposée dans la même couche que la première électrode à pixel (PE3), la deuxième électrode à pixel (PE4), la troisième électrode à pixel (PE5) et la quatrième électrode à pixel (PE6).

6. Le dispositif d'affichage à cristaux liquides de la revendication 1, comprenant de plus une ligne de connexion (CL1) connectée à la première ligne d'alimentation (VL1),
Où la ligne de connexion (CL1) est disposée dans la même couche que la première électrode de pixel (PE3), la deuxième électrode de pixel (PE4), la troisième électrode de pixel (PE5) et la quatrième électrode de pixel (PE6).

7. Le dispositif d'affichage à cristaux liquides de la revendication 6, où la polarité d'une tension appliquée à la première électrode de pixel (PE3) est différente de la polarité d'une tension appliquée à la deuxième électrode de pixel (PE4) par rapport à une tension de référence.

8. Le dispositif d'affichage à cristaux liquides de la revendication 3, où une portion du premier modèle de protection (SD1, SC, SU2) chevauche la troisième électrode de pixel (PE5).

FIG. 1

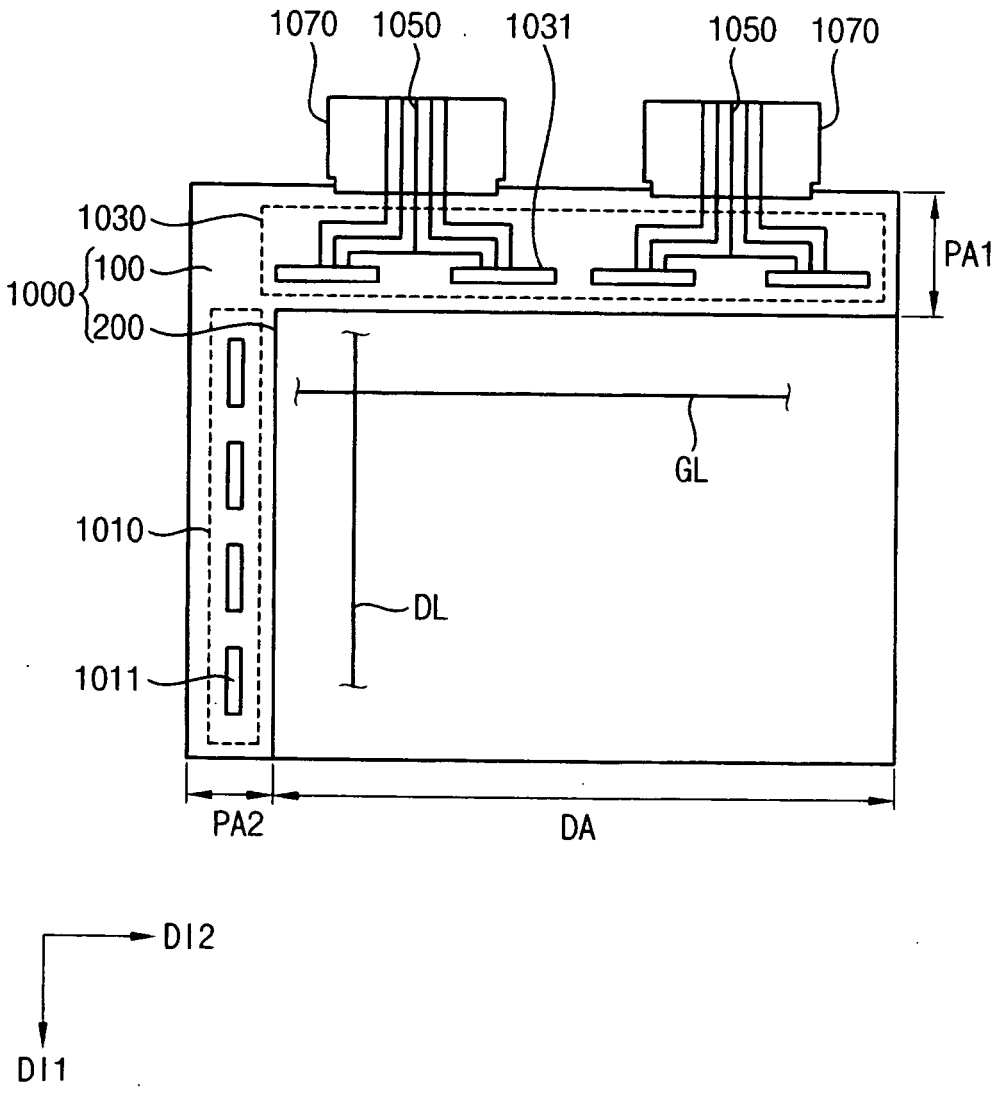

1070
1050
1031
1050
1070
1030
100
1000
200
PA1
GL
1010
DL
1011
PA2
DA
DI2
DI1

FIG. 2

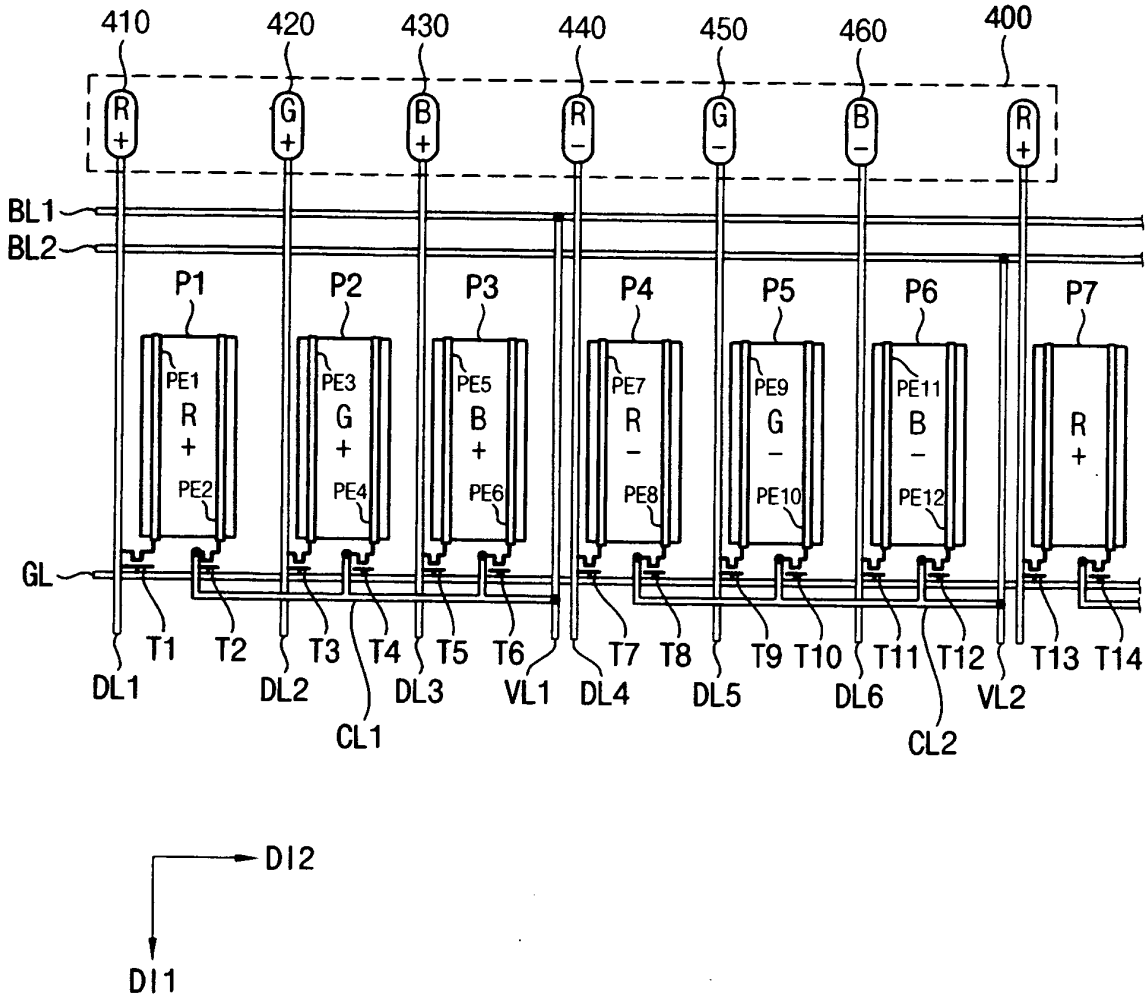

410
420
430
440
450
460
400
R +
G +
B +
R −
G −
B −
R +
BL1
BL2
P1
P2
P3
P4
P5
P6
P7
PE1
R
+
PE2
PE3
G
+
PE4
PE5
B
+
PE6
PE7
R
−
PE8
PE9
G
−
PE10
PE11
B
−
PE12
R
+
GL
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
T13
T14
DL1
DL2
CL1
DL3
VL1
DL4
DL5
DL6
CL2
VL2
DI2
DI1

FIG. 3

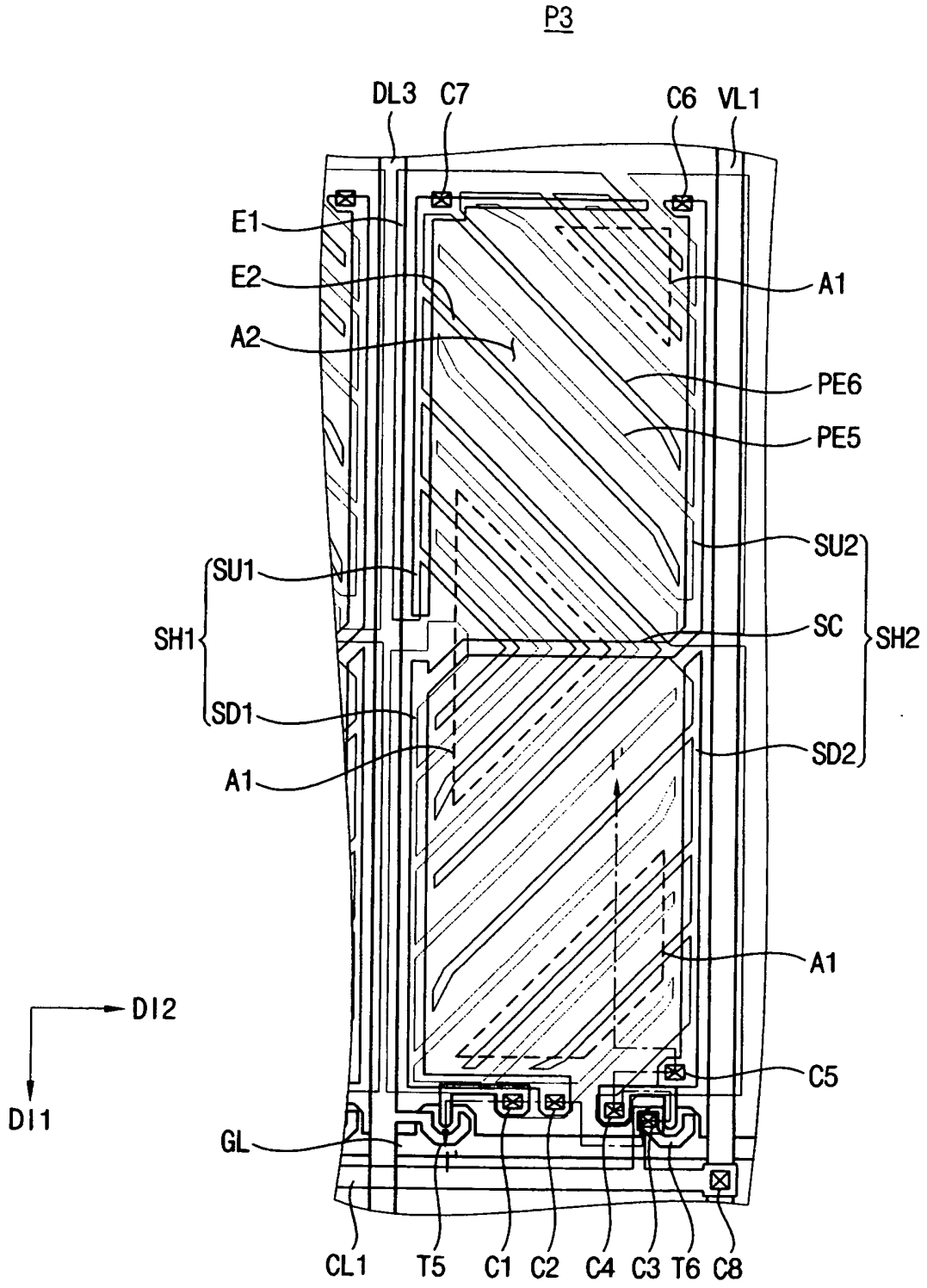

P3
DL3
C7
C6
VL1
E1
E2
A2
A1
PE6
PE5
SU2
SU1
SH1
SC
SH2
SD1
SD2
A1
A1
C5
DI2
DI1
GL
CL1
T5
C1
C2
C4
C3
T6
C8

FIG. 4

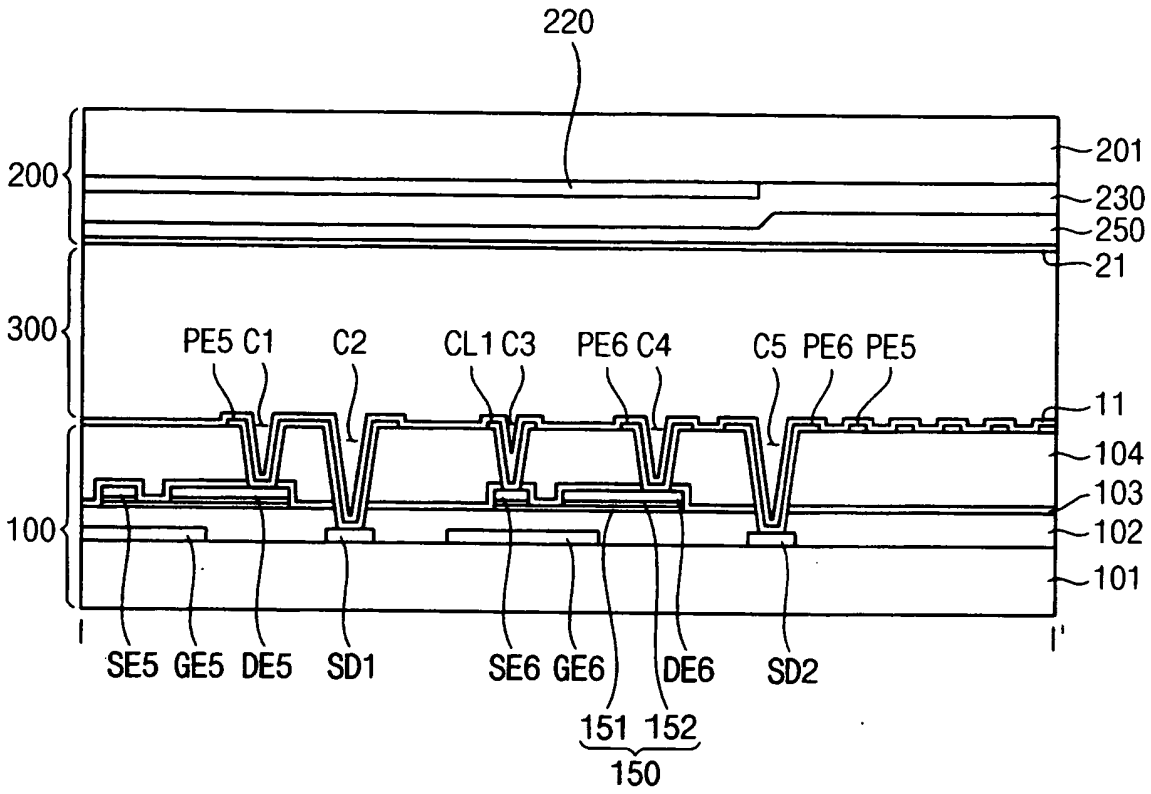

220
200
300
100
201
230
250
21
PE5 C1
C2
CL1 C3
PE6 C4
C5 PE6 PE5
11
104
103
102
101
SE5 GE5 DE5 SD1
SE6 GE6
DE6
SD2
151 152
150

FIG. 5A

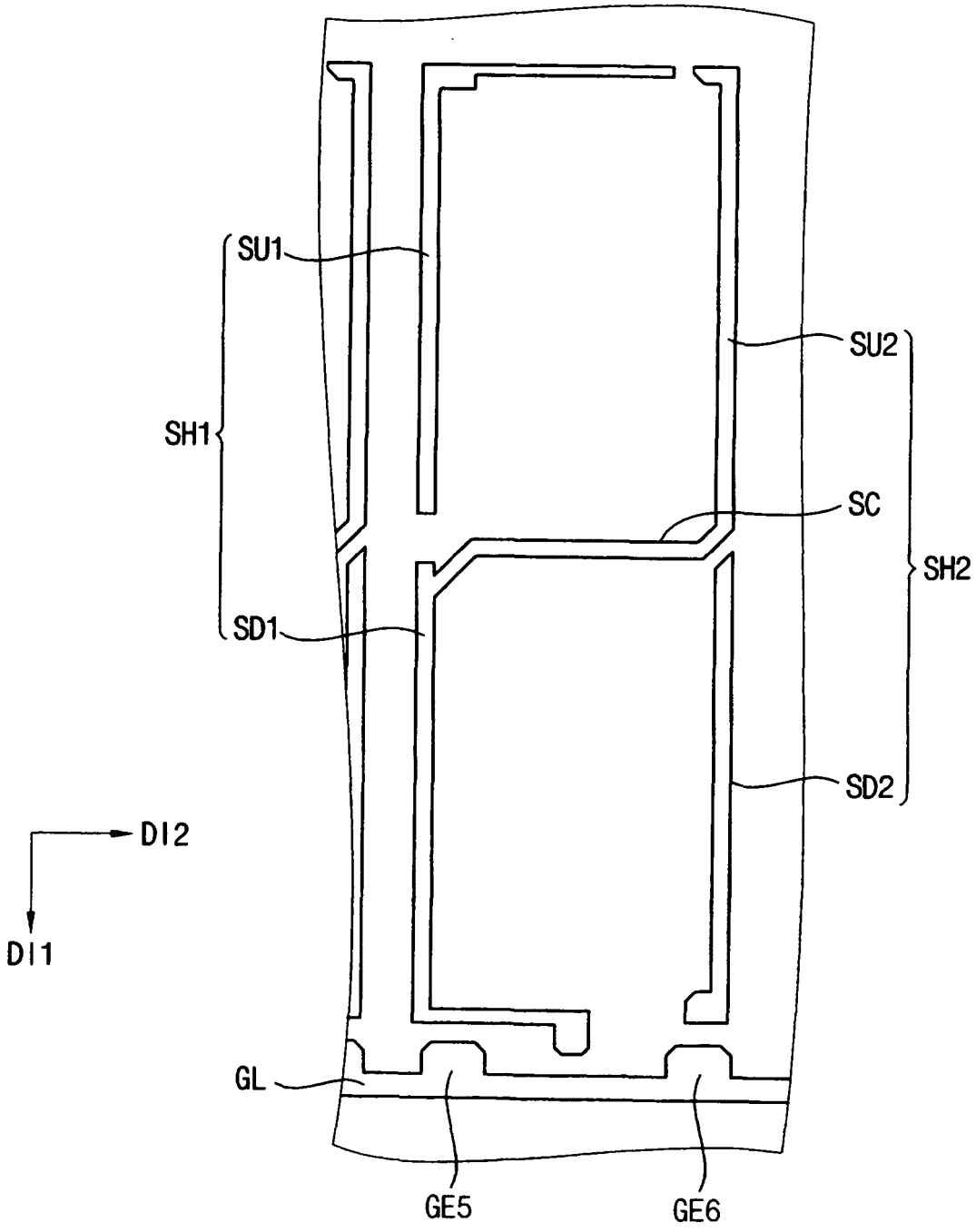


FIG. 5B

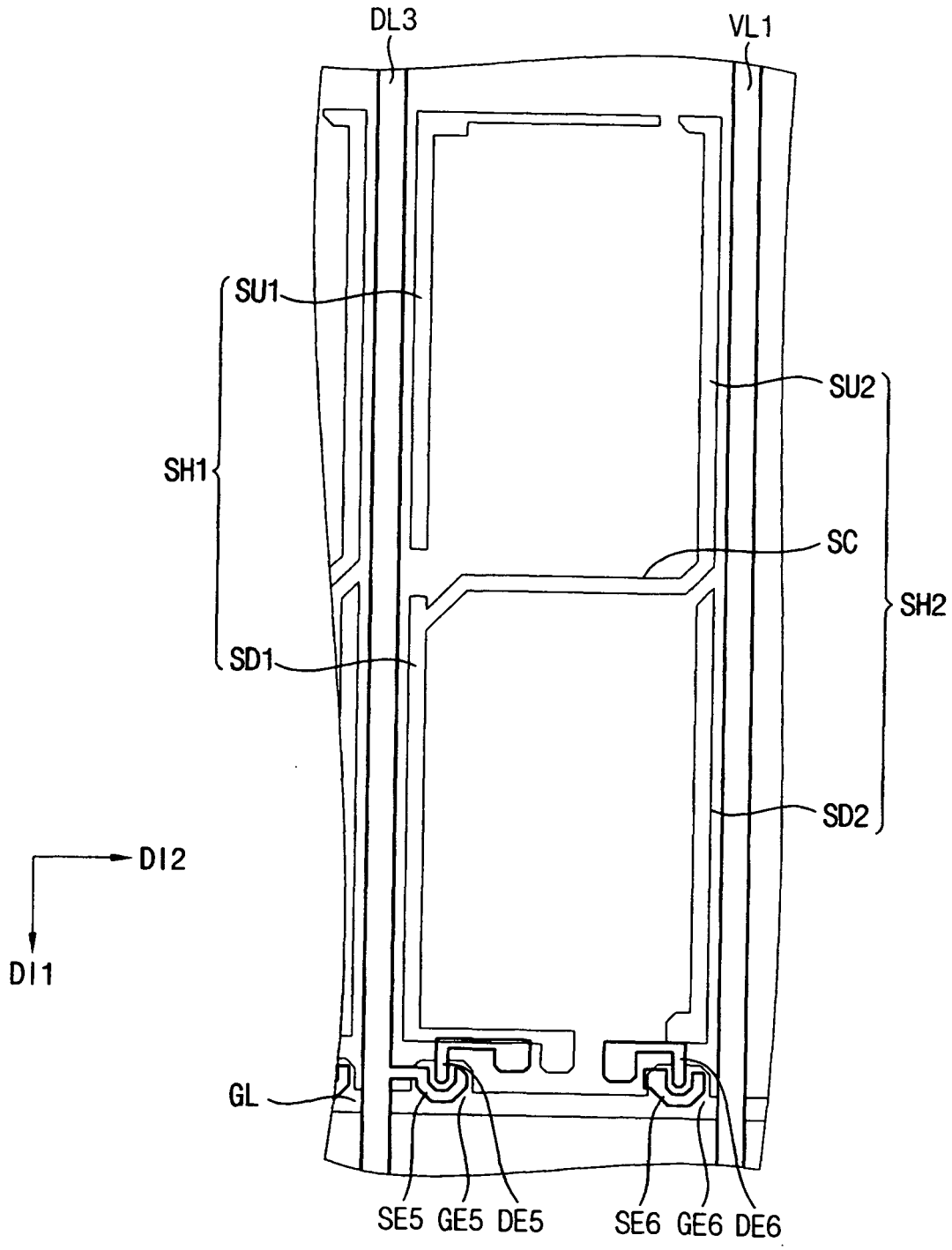

DL3
VL1
SU1
SU2
SH1
SC
SH2
SD1
SD2
DI2
DI1
GL
SE5 GE5 DE5
SE6 GE6 DE6

FIG. 5C

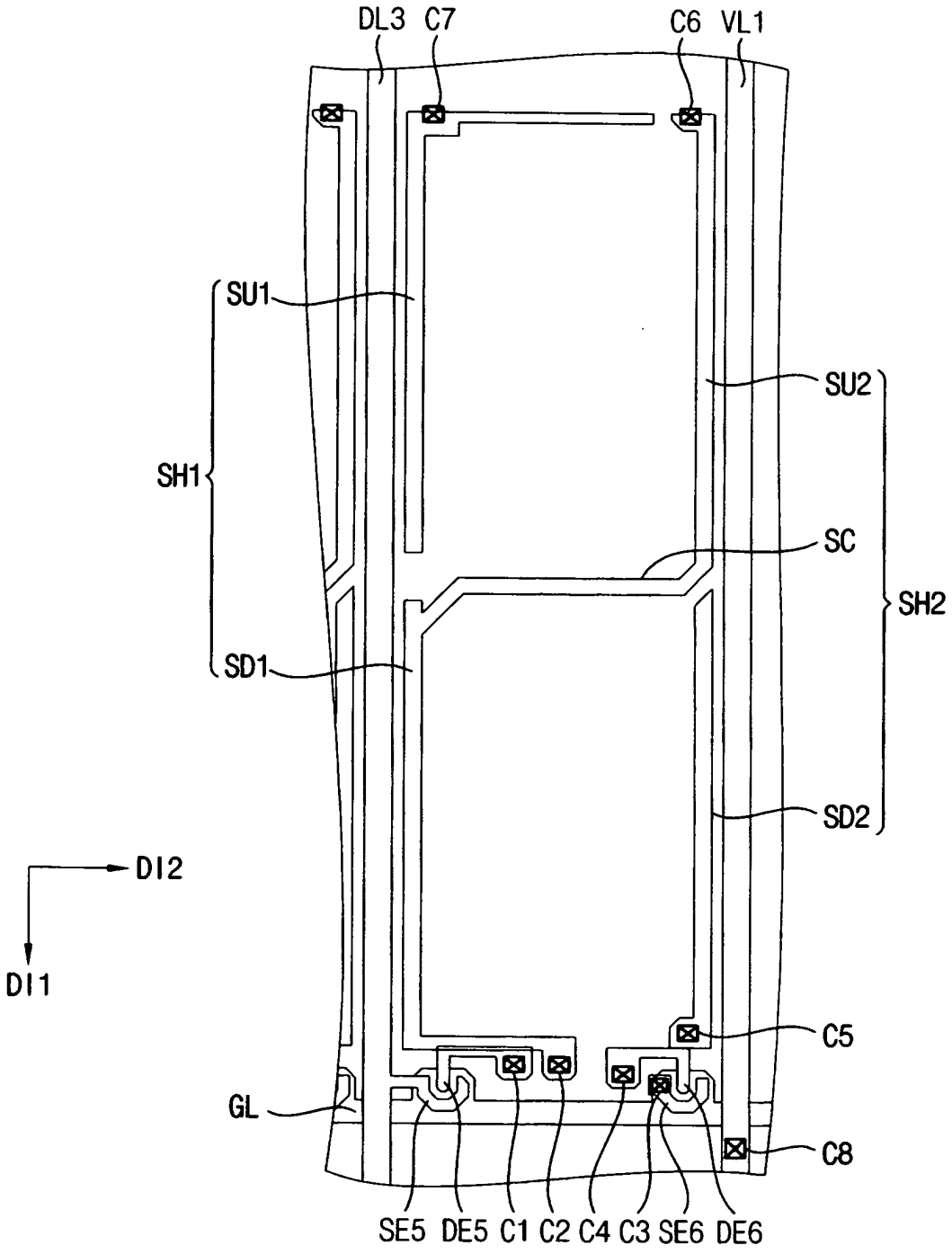

DL3
C7
C6
VL1
SU1
SU2
SH1
SC
SH2
SD1
SD2
DI2
DI1
C5
GL
C8
SE5
DE5
C1
C2
C4
C3
SE6
DE6

FIG. 5D

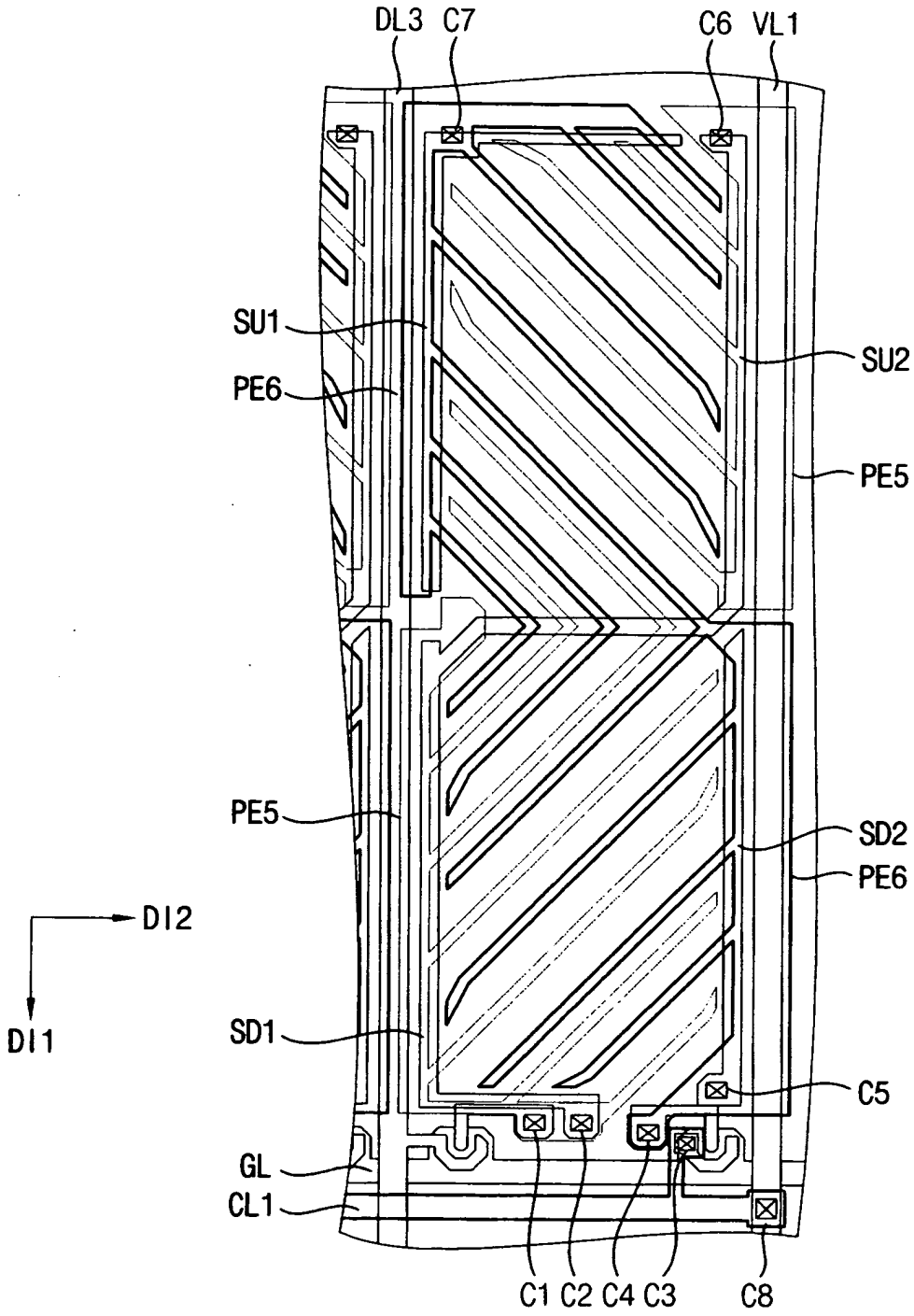

DL3
C7
C6
VL1
SU1
SU2
PE6
PE5
PE5
SD2
PE6
D12
D11
SD1
C5
GL
CL1
C1
C2
C4
C3
C8

FIG. 6

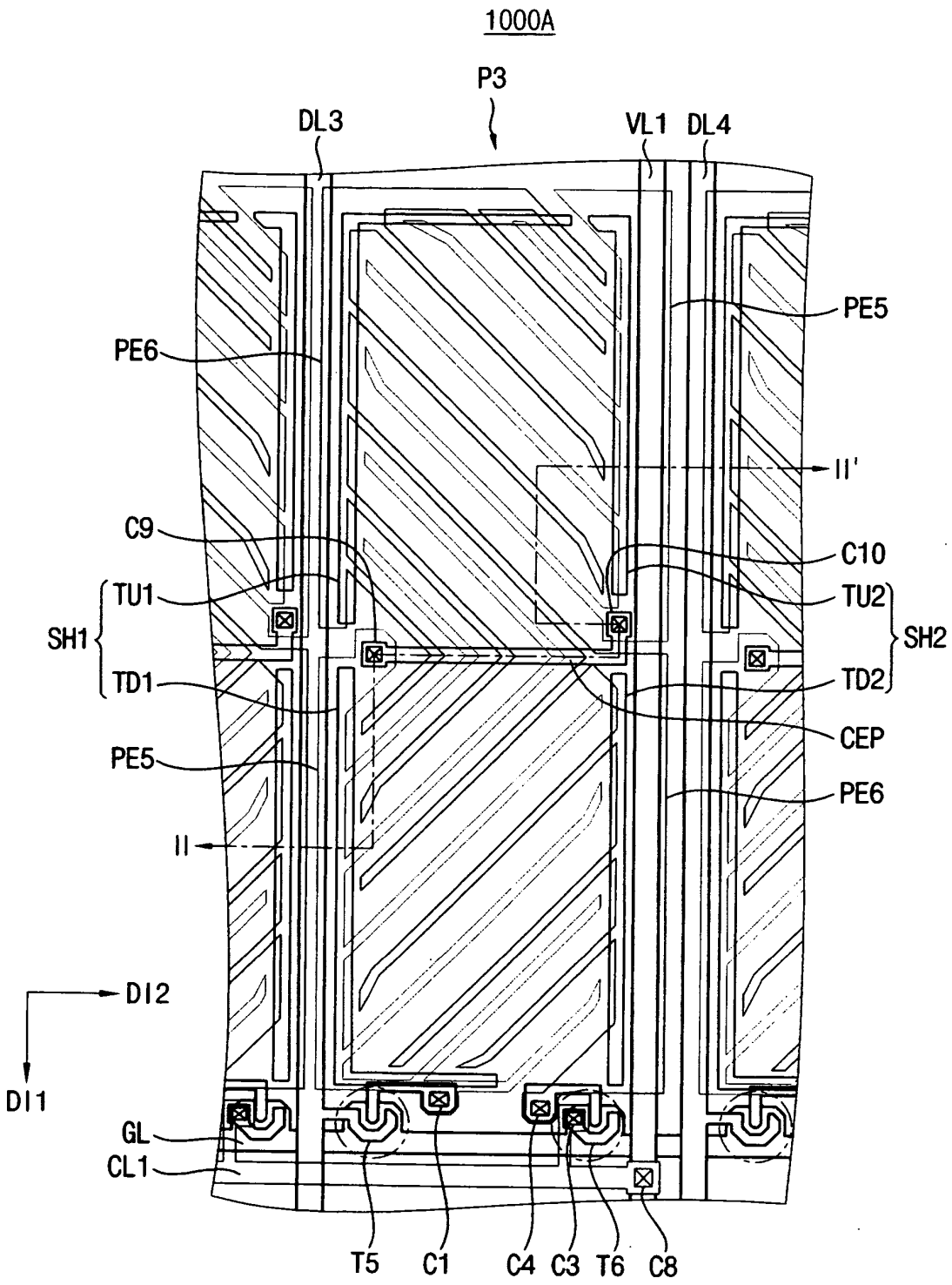

1000A
P3
DL3
VL1
DL4
PE5
PE6
II'
C9
C10
TU1
TU2
SH1
SH2
TD1
TD2
CEP
PE5
PE6
II
DI2
DI1
GL
CL1
T5
C1
C4
C3
T6
C8

FIG. 7

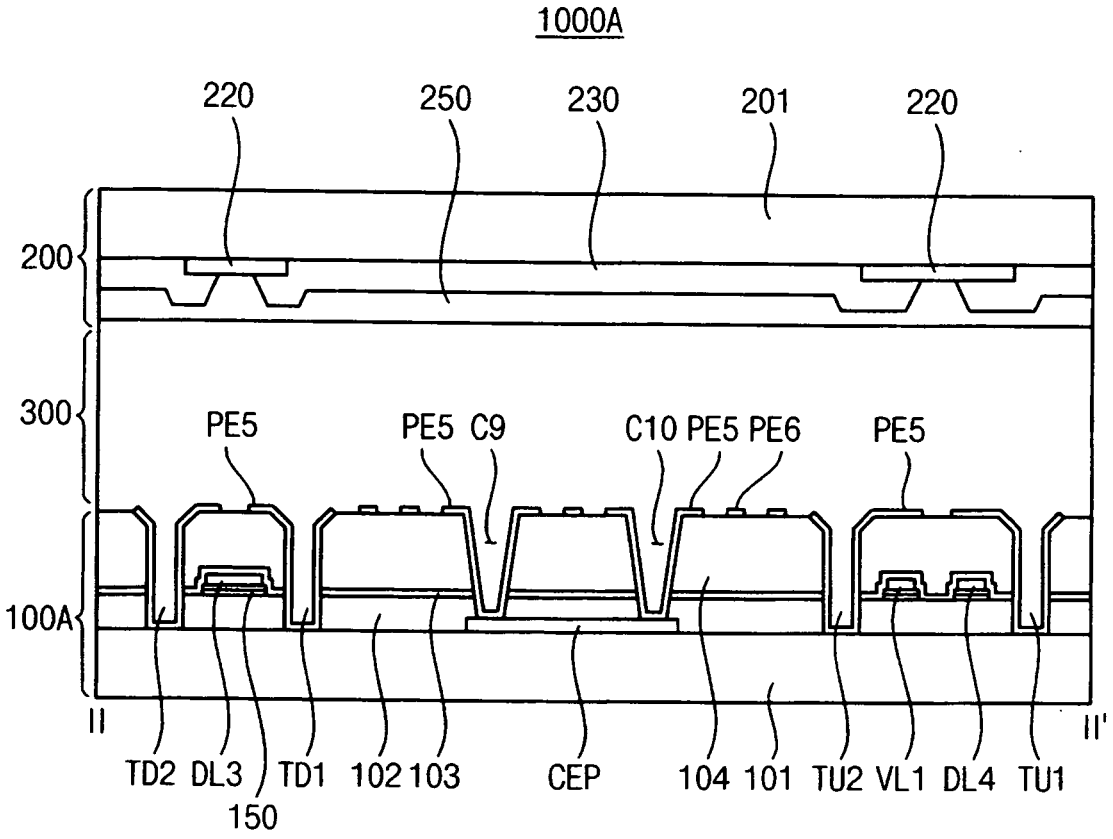

1000A
220
250
230
201
220
200
300
PE5
PE5
C9
C10
PE5
PE6
PE5
100A
II
II'
TD2
DL3
150
TD1
102
103
CEP
104
101
TU2
VL1
DL4
TU1

FIG. 8A

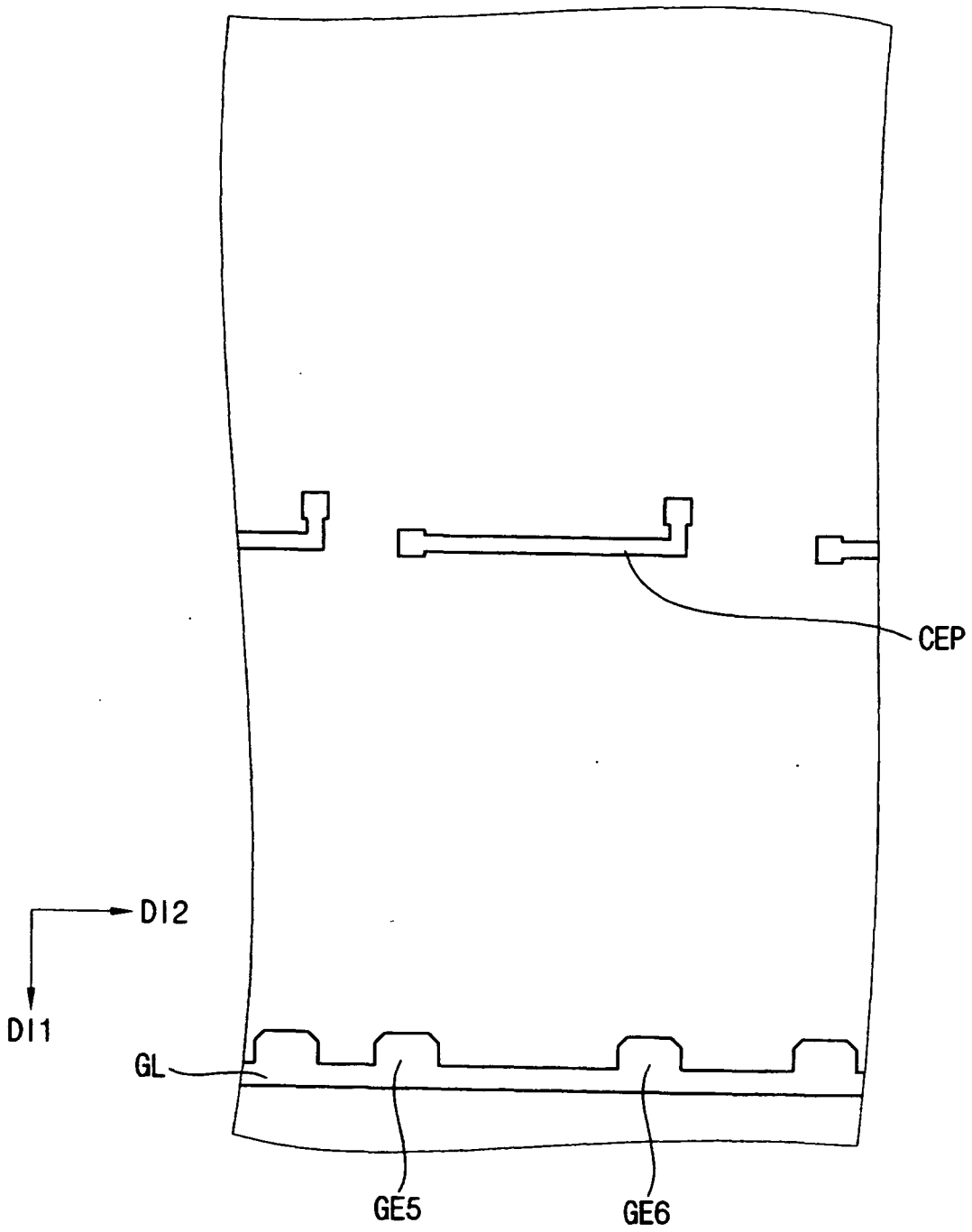


FIG. 8B

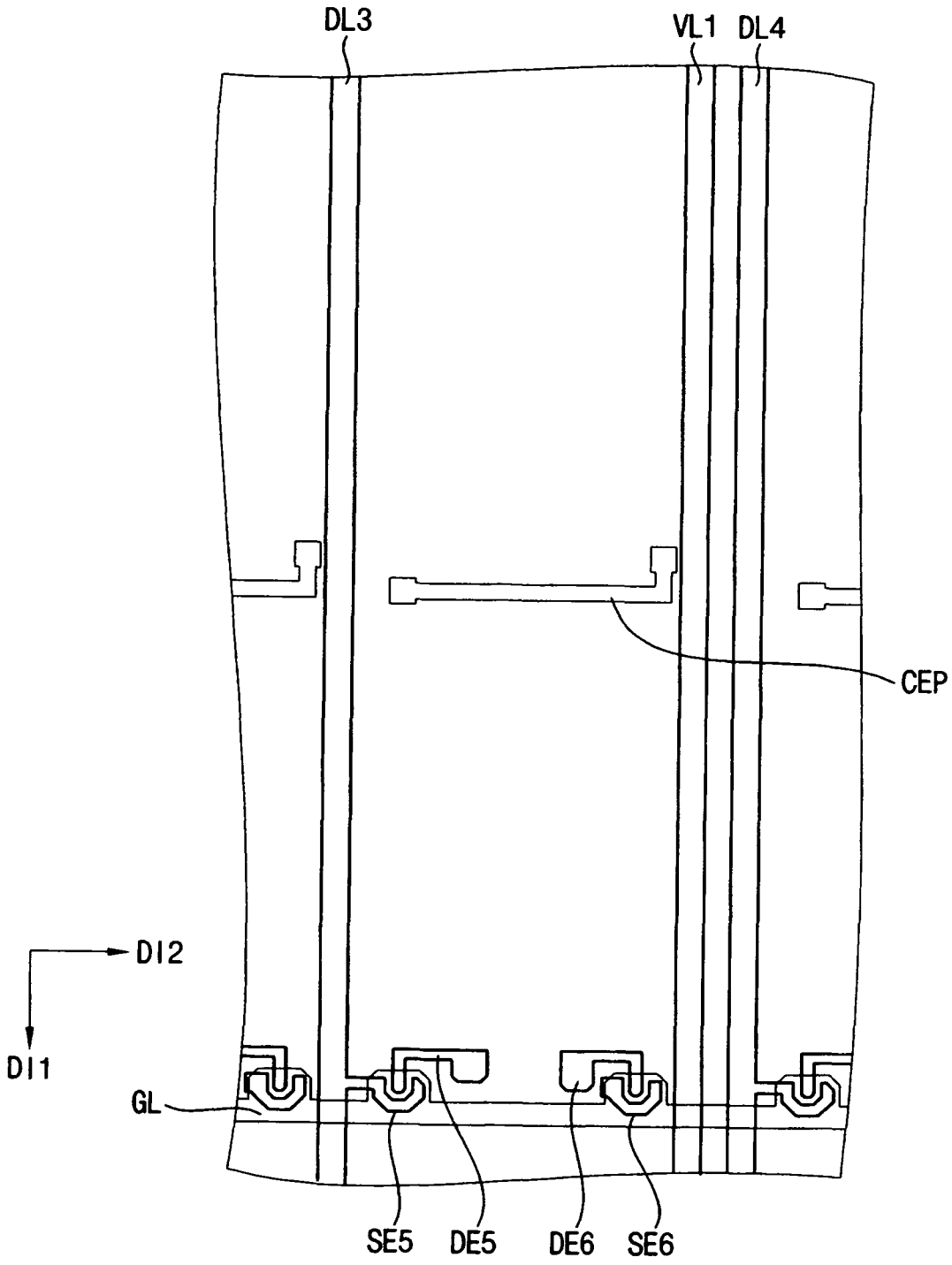


FIG. 8C

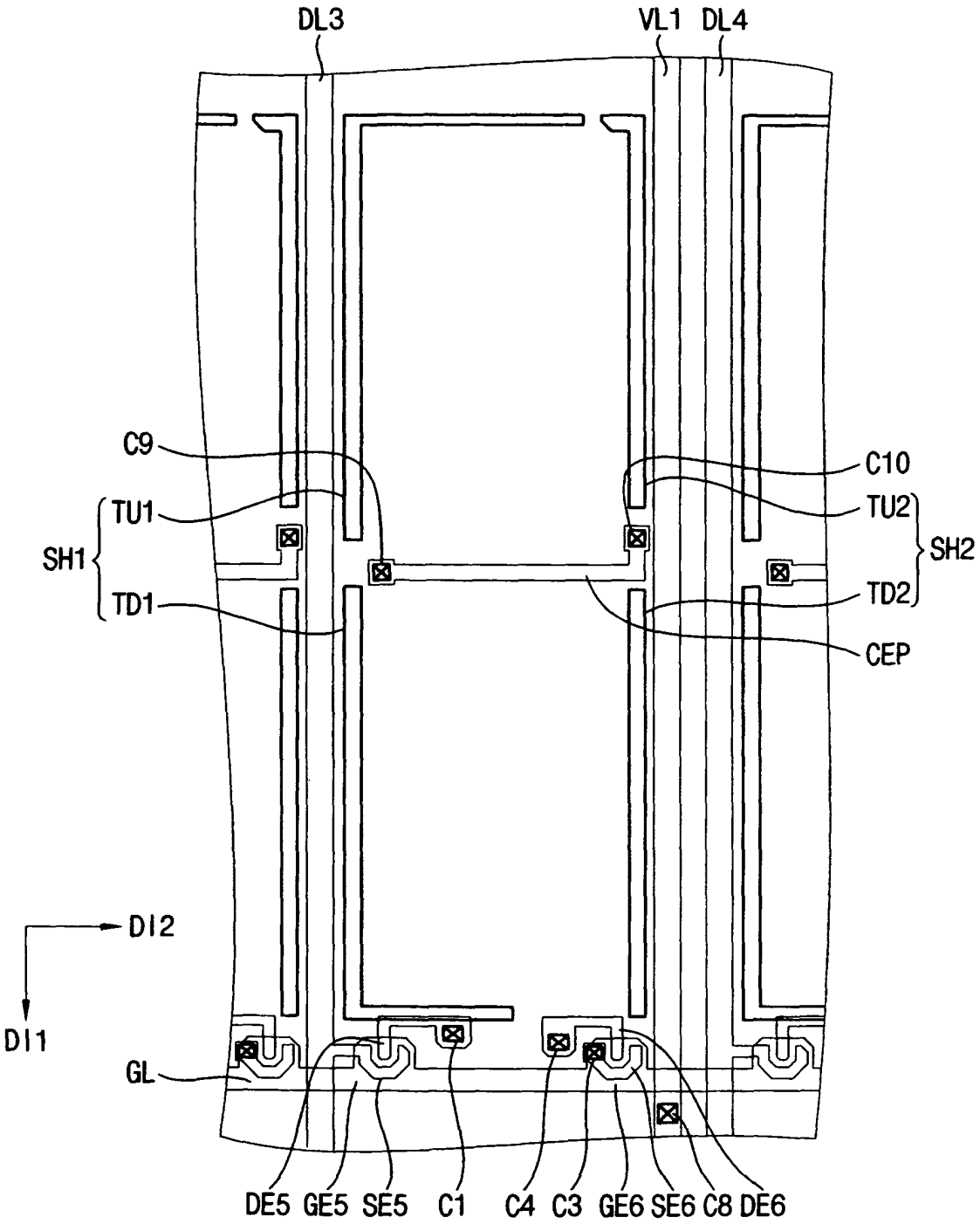

DL3
VL1
DL4
C9
C10
TU1
TU2
SH1
SH2
TD1
TD2
CEP
DI2
DI1
GL
DE5
GE5
SE5
C1
C4
C3
GE6
SE6
C8
DE6

FIG. 8D

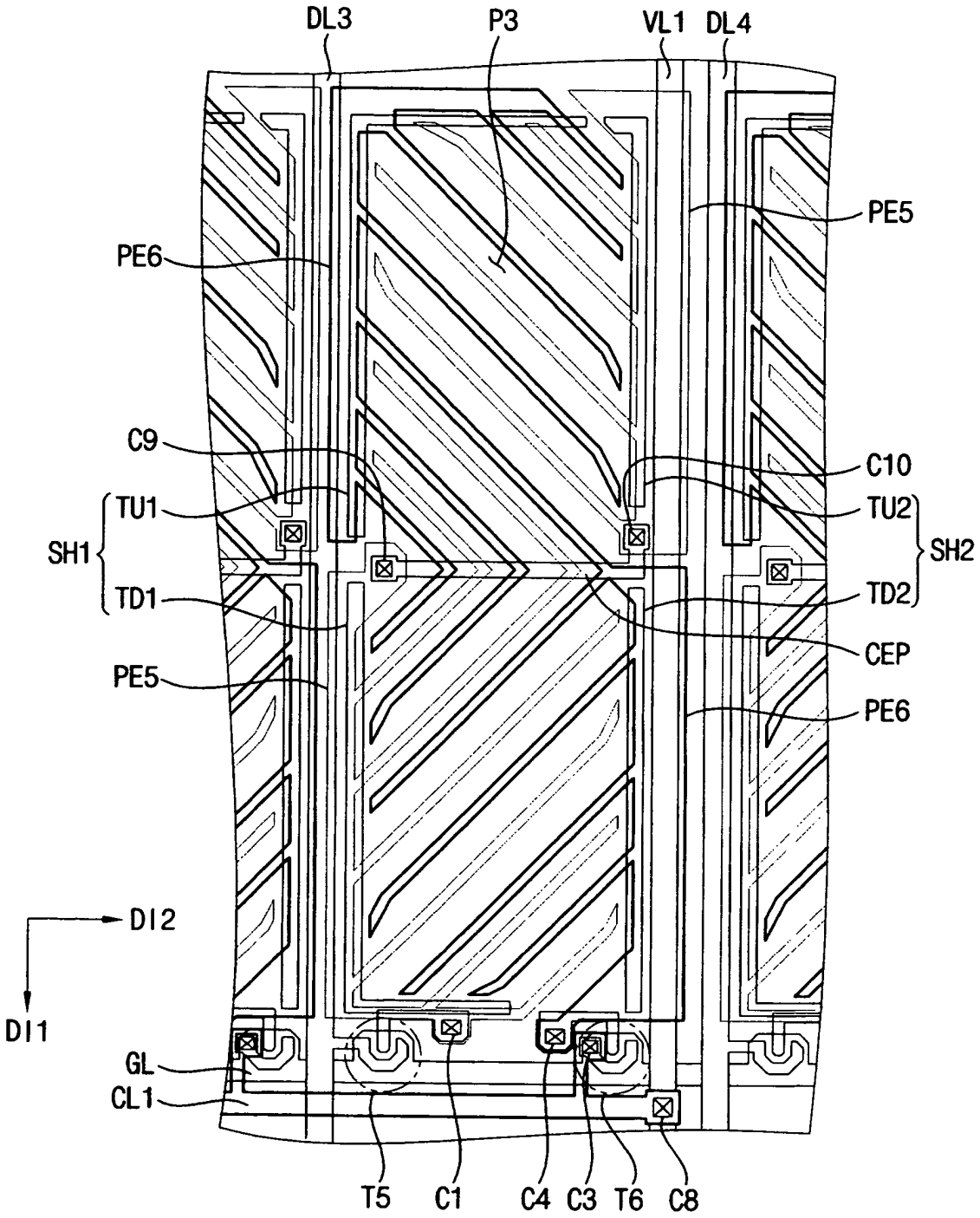

DL3
P3
VL1
DL4
PE5
PE6
C9
C10
TU1
TU2
SH1
SH2
TD1
TD2
CEP
PE5
PE6
DI2
DI1
GL
CL1
T5
C1
C4
C3
T6
C8

FIG. 9

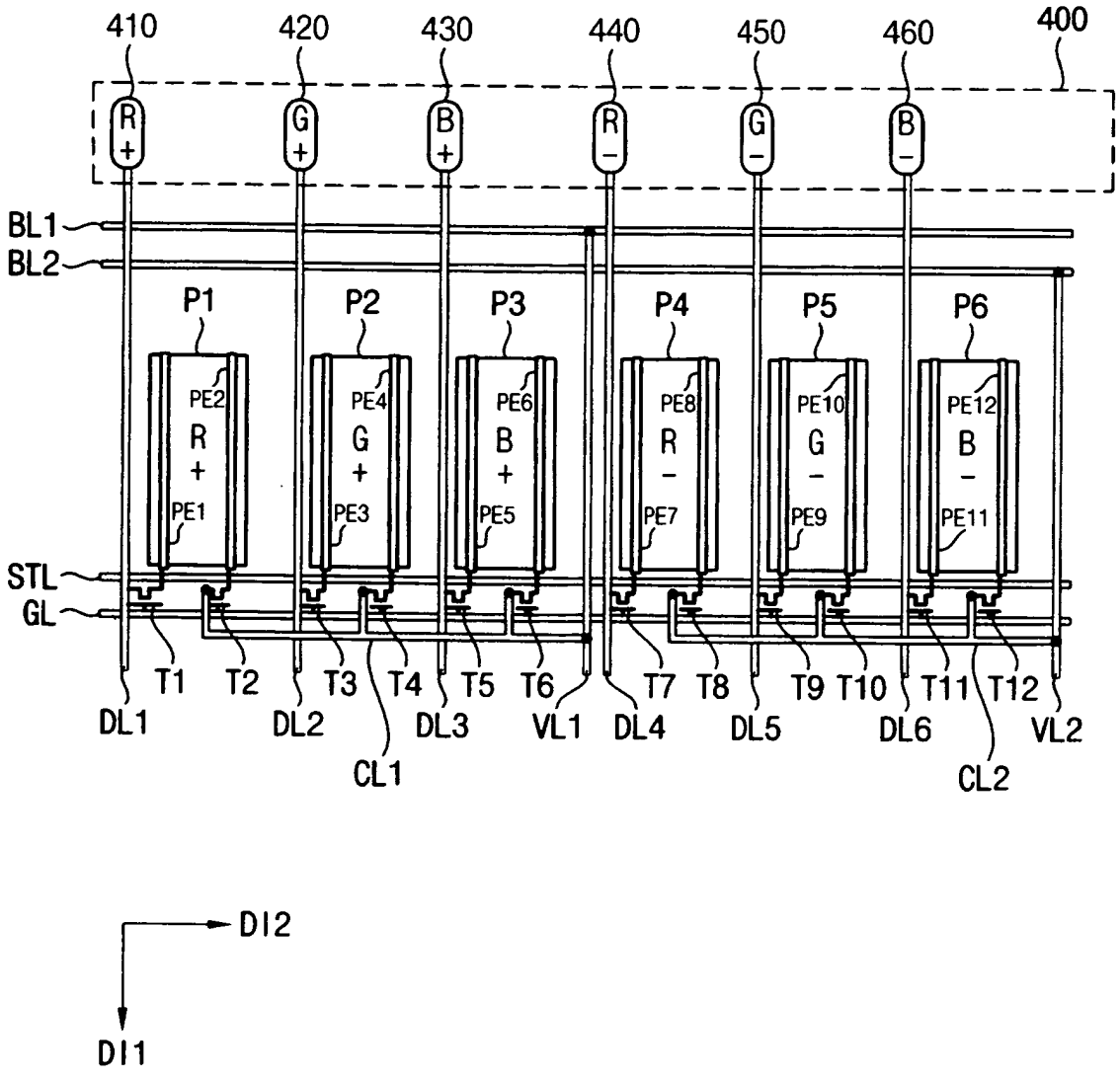

1000B
410
420
430
440
450
460
400
R +
G +
B +
R −
G −
B −
BL1
BL2
P1
P2
P3
P4
P5
P6
PE1
PE2
PE3
PE4
PE5
PE6
PE7
PE8
PE9
PE10
PE11
PE12
R + −
G + −
B + −
STL
GL
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
DL1
DL2
DL3
DL4
DL5
DL6
CL1
CL2
VL1
VL2
DI2
DI1

FIG. 10

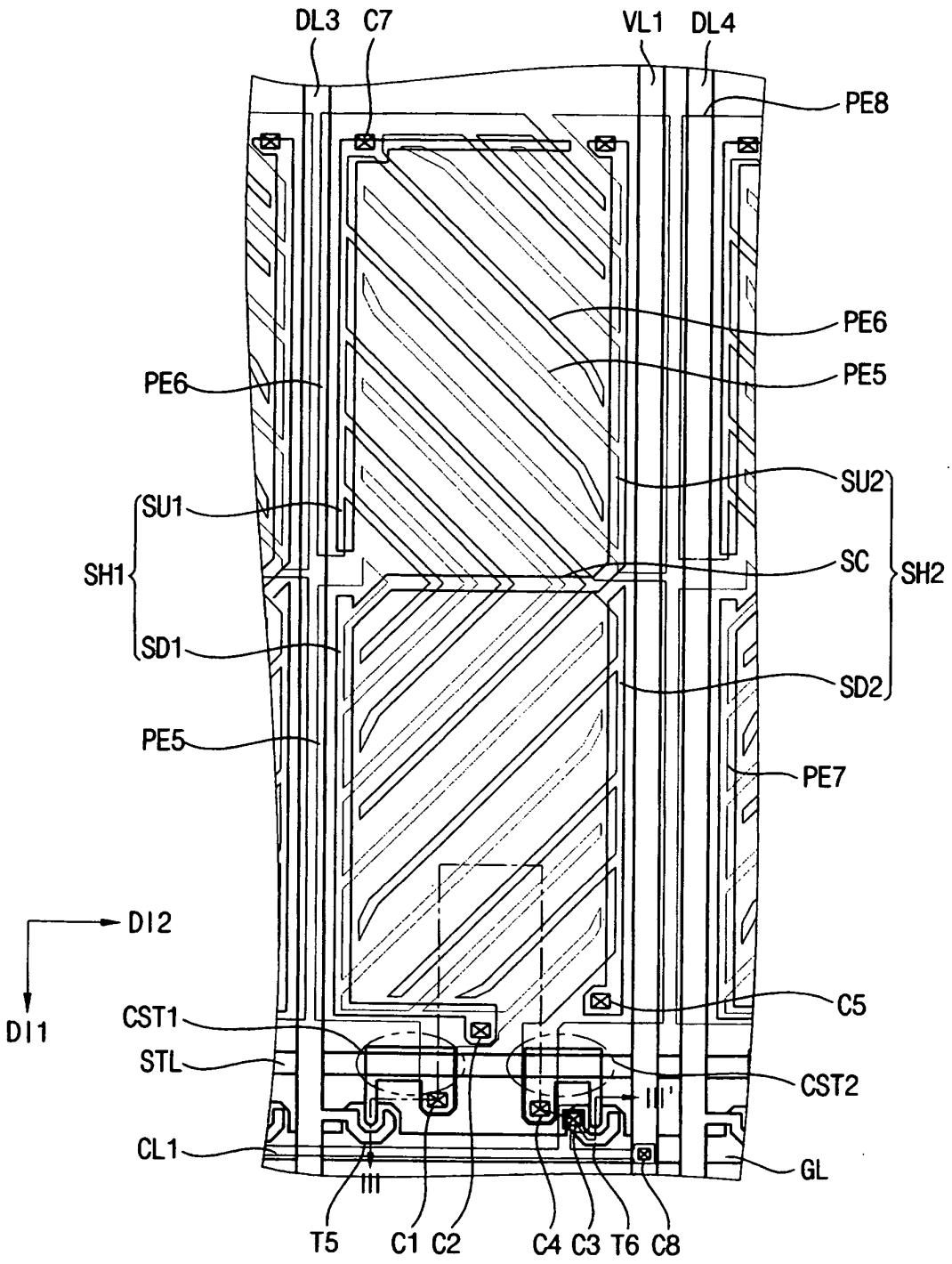

P3
DL3
C7
VL1
DL4
PE8
PE6
PE6
PE5
SU2
SU1
SH1
SC
SH2
SD1
SD2
PE5
PE7
D12
D11
C5
CST1
STL
CST2
II
II'
CL1
III
III'
GL
T5
C1
C2
C4
C3
T6
C8

FIG. 11

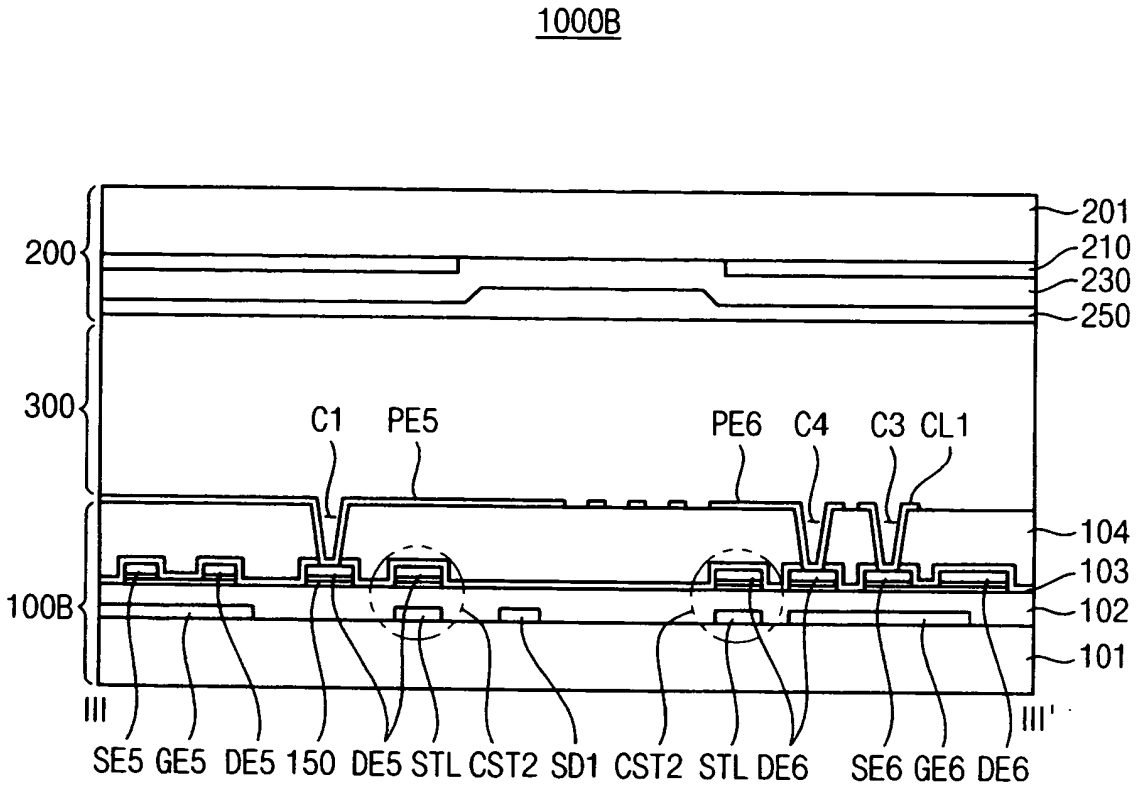

1000B
200
300
100B
201
210
230
250
C1
PE5
PE6
C4
C3
CL1
104
103
102
101
III
III'
SE5
GE5
DE5
150
DE5
STL
CST2
SD1
CST2
STL
DE6
SE6
GE6
DE6

FIG. 12A

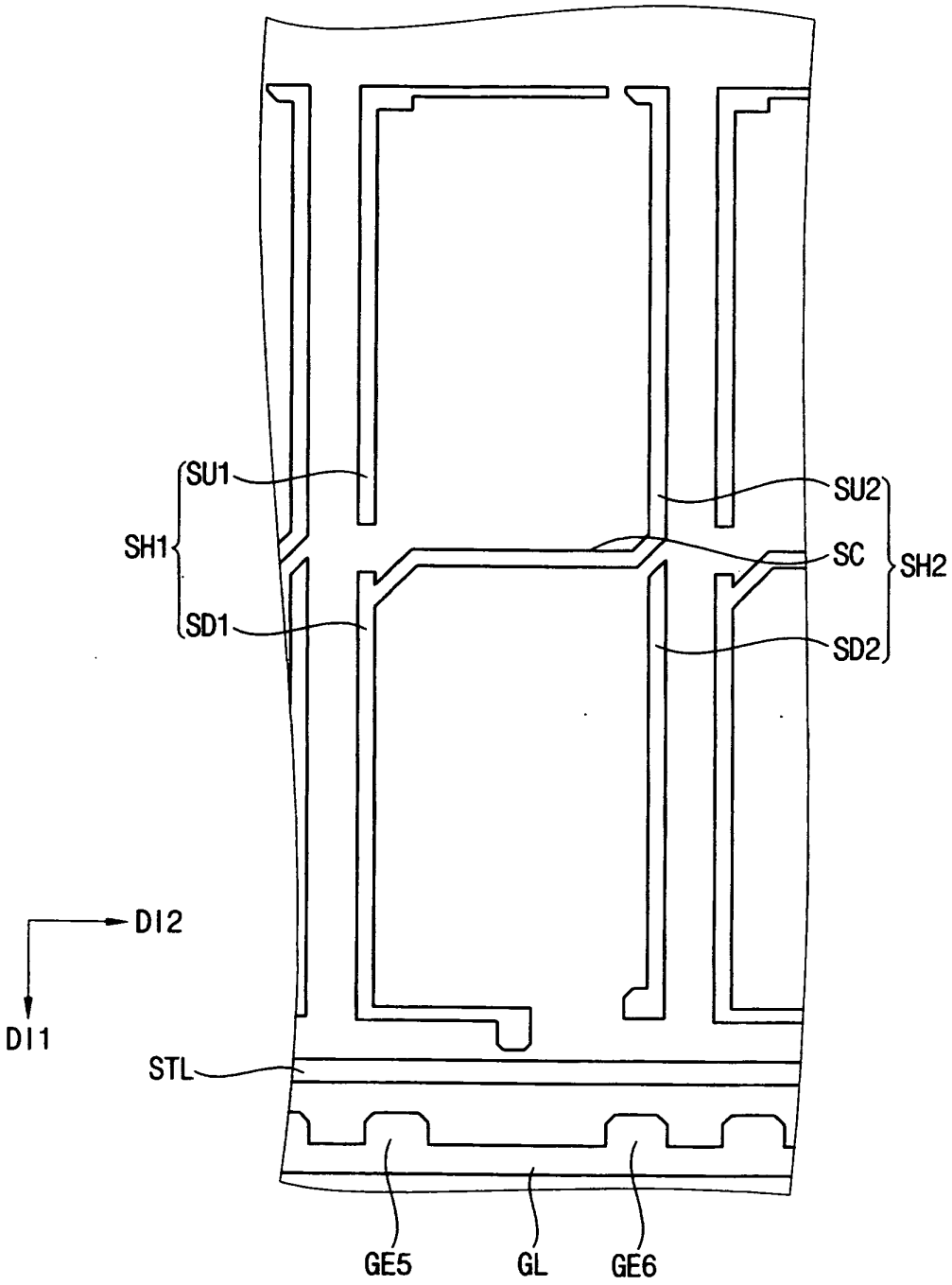


FIG. 12B

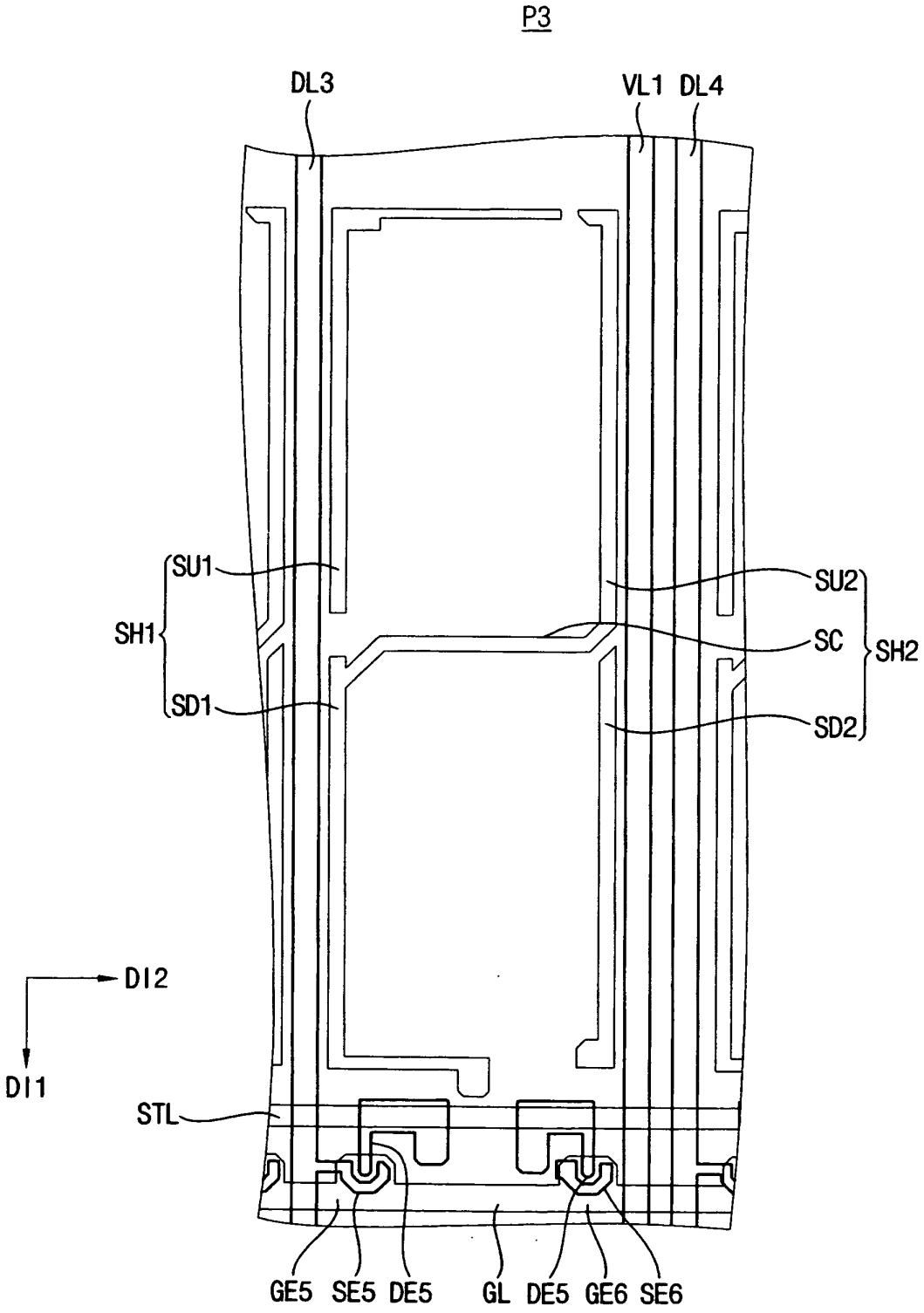

P3
DL3
VL1
DL4
SU1
SH1
SD1
SU2
SC
SH2
SD2
D12
D11
STL
GE5
SE5
DE5
GL
DE5
GE6
SE6

FIG. 12C

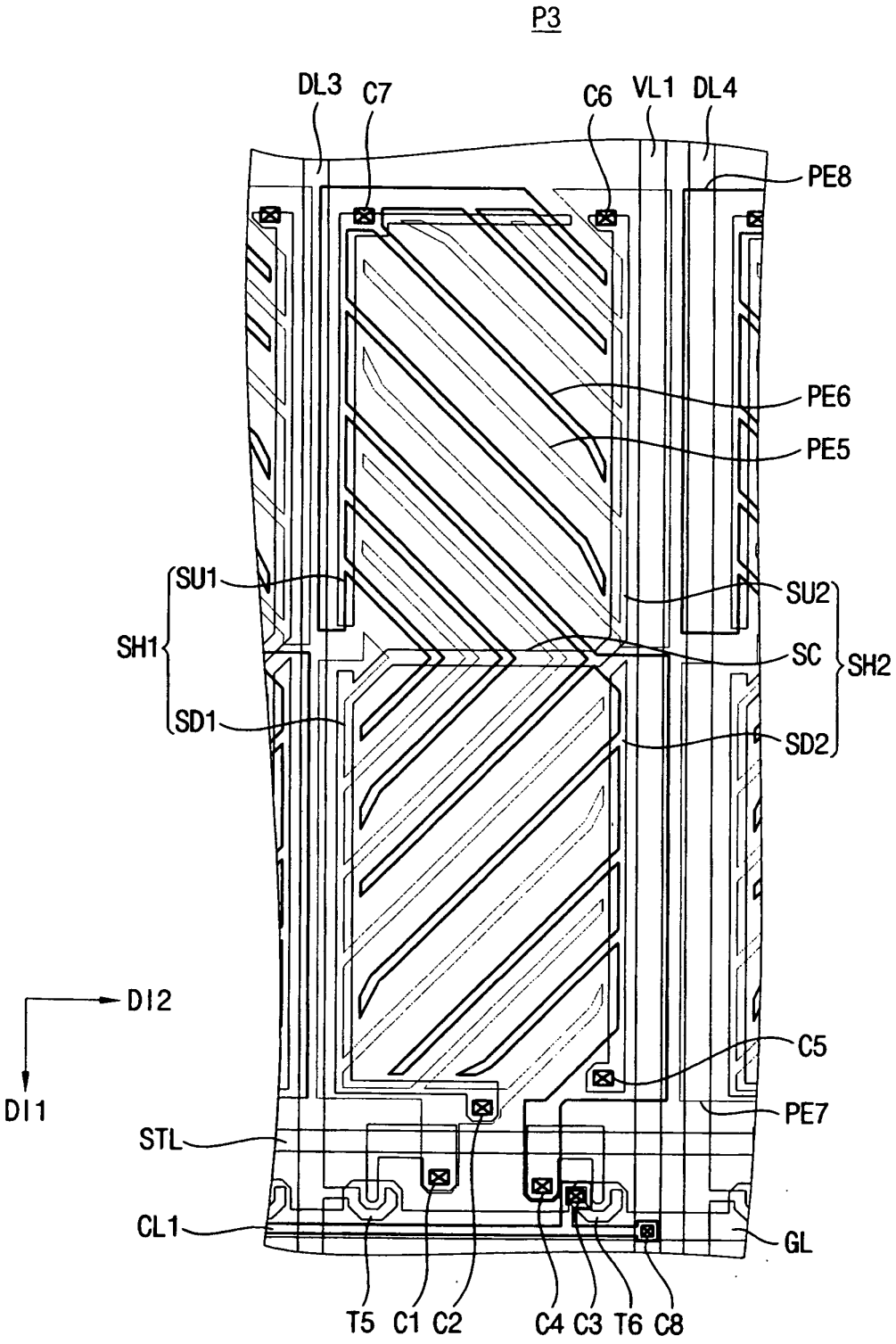

P3
DL3
C7
C6
VL1
DL4
PE8
PE6
PE5
SU1
SH1
SD1
SU2
SC
SH2
SD2
D12
D11
C5
PE7
STL
CL1
GL
T5
C1
C2
C4
C3
T6
C8

FIG. 13

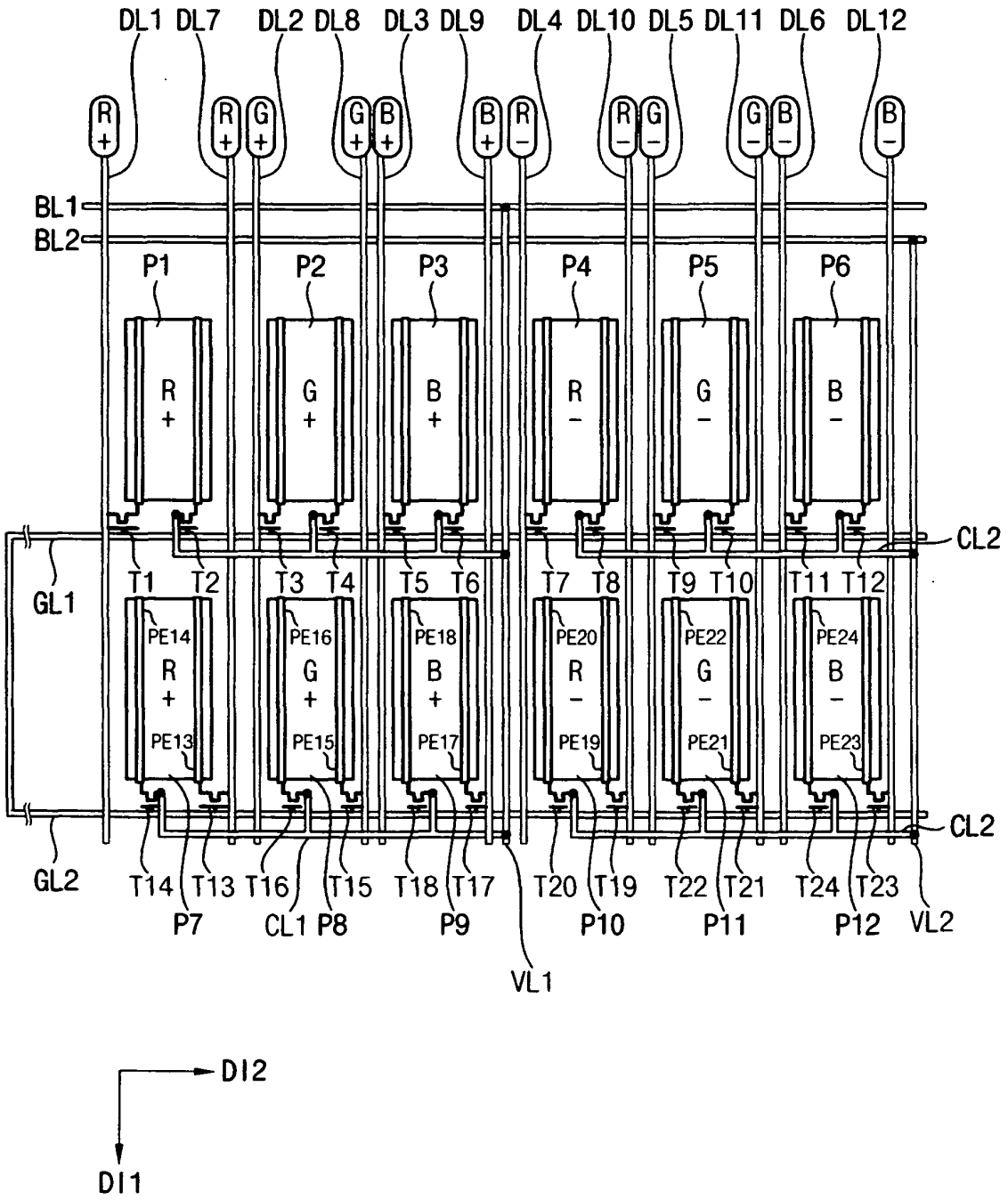

1000C
DL1 DL7 DL2 DL8 DL3 DL9 DL4 DL10 DL5 DL11 DL6 DL12
BL1
BL2
P1 P2 P3 P4 P5 P6
R + G + B + R − G − B −
CL2
GL1
T1 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11 T12
PE14 PE16 PE18 PE20 PE22 PE24
PE13 PE15 PE17 PE19 PE21 PE23
CL2
GL2
T14 T13 T16 T15 T18 T17 T20 T19 T22 T21 T24 T23
P7 CL1 P8 P9 P10 P11 P12 VL2
VL1
DI2
DI1

FIG. 14

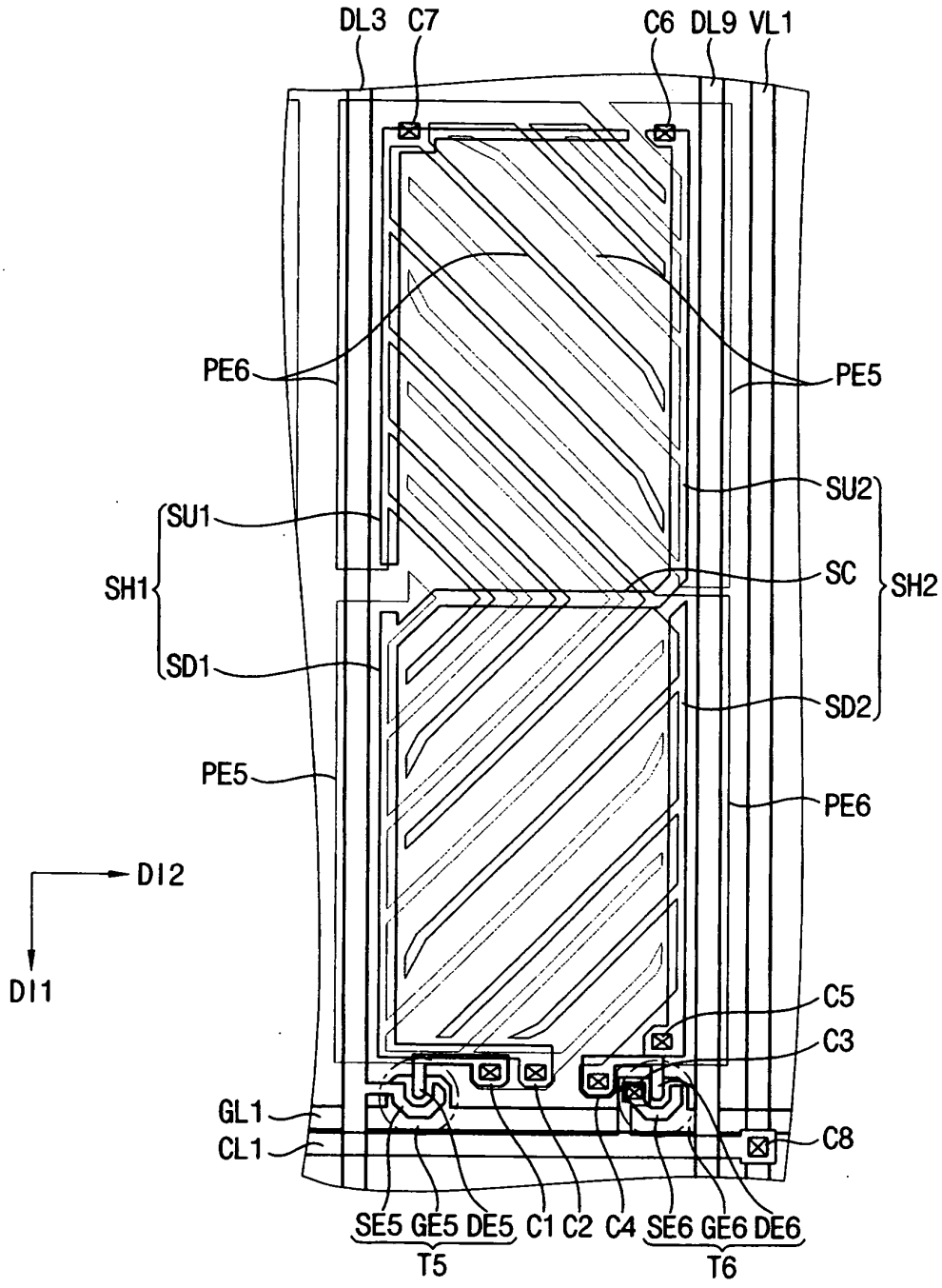

P3
DL3
C7
C6
DL9
VL1
PE6
PE5
SU1
SU2
SH1
SC
SH2
SD1
SD2
PE5
PE6
DI2
DI1
C5
C3
GL1
CL1
C8
SE5
GE5
DE5
C1
C2
C4
SE6
GE6
DE6
T5
T6

FIG. 15

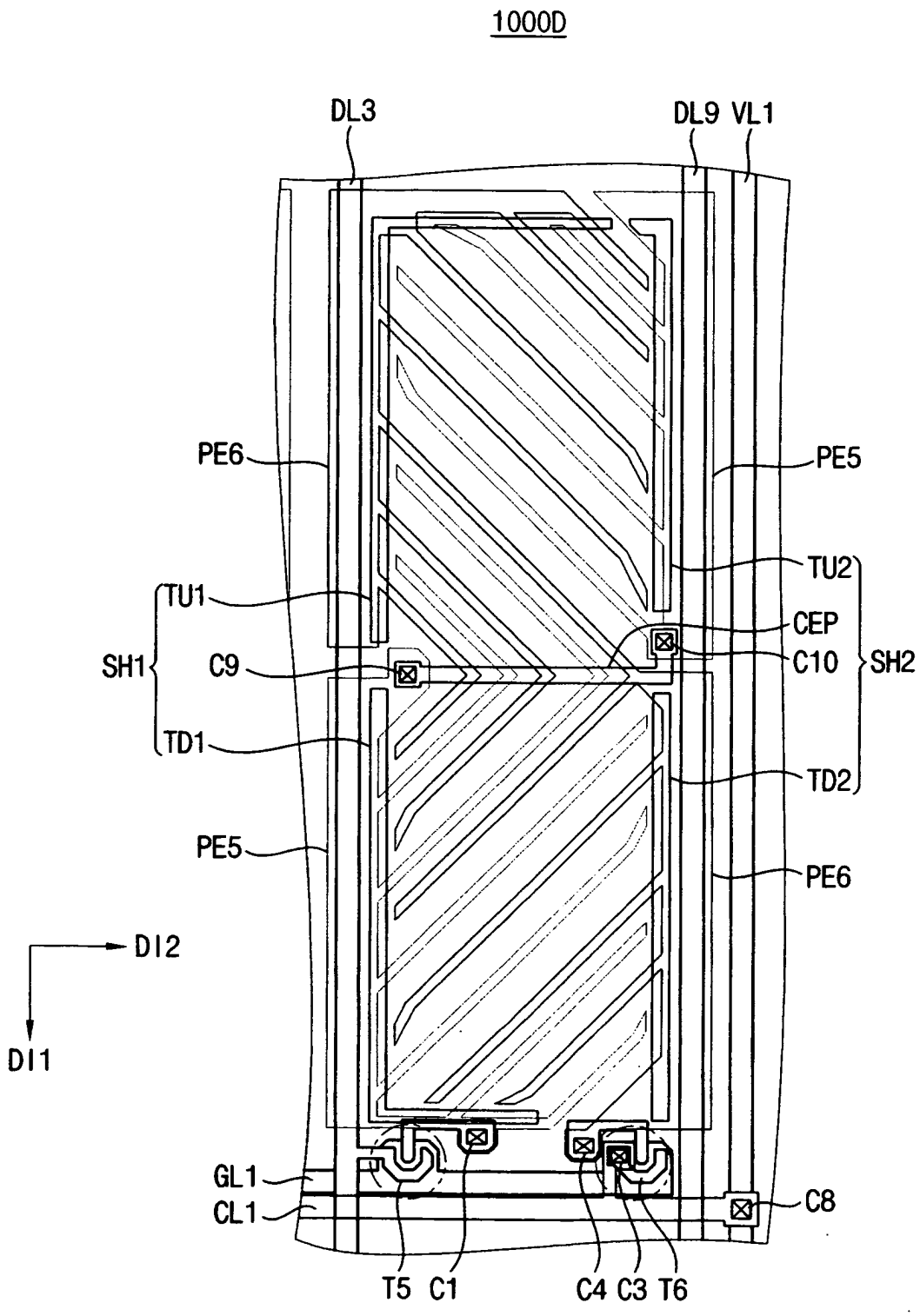

1000D
DL3
DL9
VL1
PE6
PE5
TU2
TU1
CEP
SH1
C9
C10
SH2
TD1
TD2
PE5
PE6
DI2
DI1
GL1
CL1
C8
T5
C1
C4
C3
T6

FIG. 16

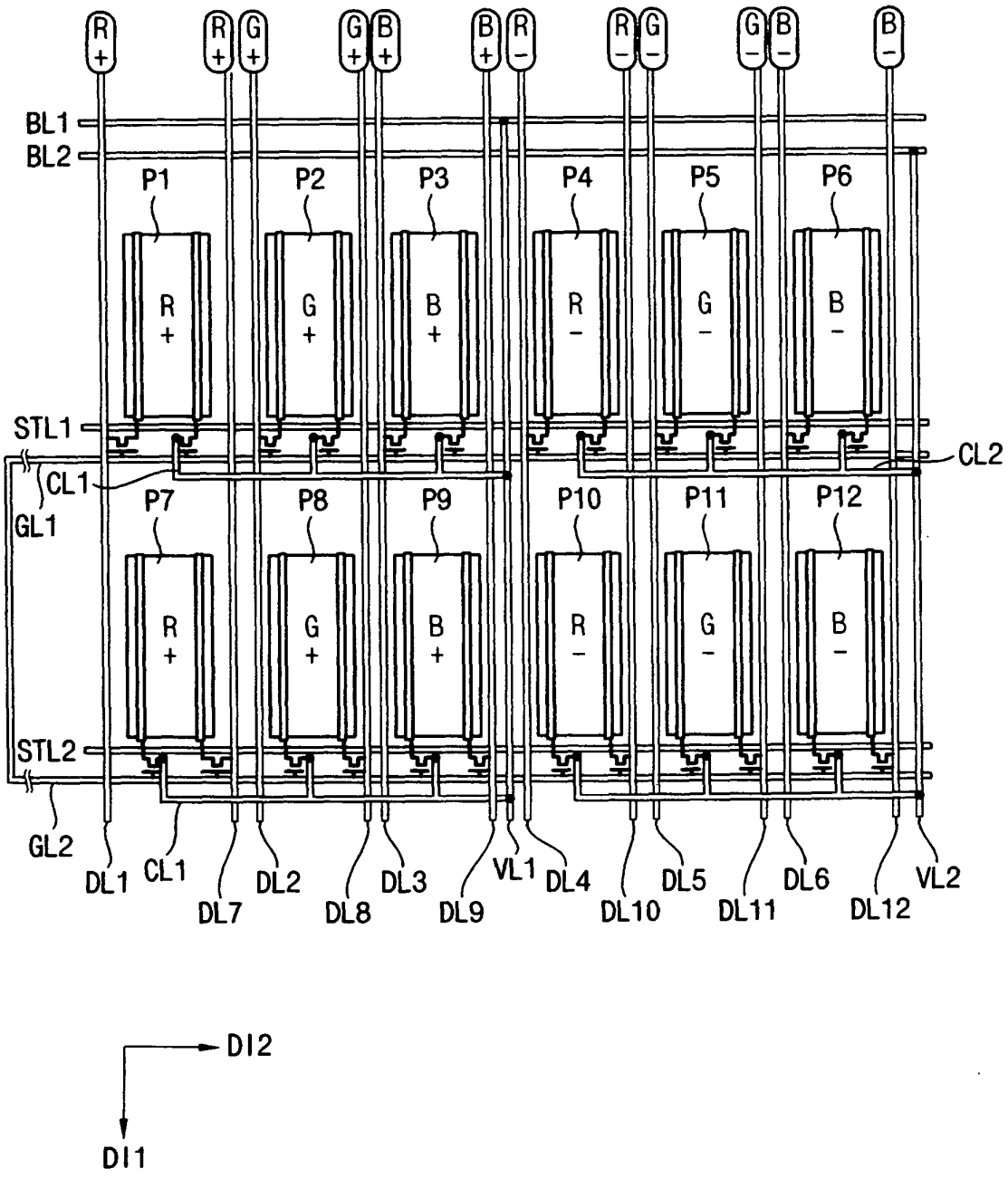

1000E
R+
R+
G+
G+
B+
B+
R−
R−
G−
G−
B−
B−
BL1
BL2
P1
P2
P3
P4
P5
P6
R+
G+
B+
R−
G−
B−
STL1
CL1
CL2
GL1
P7
P8
P9
P10
P11
P12
R+
G+
B+
R−
G−
B−
STL2
GL2
DL1
CL1
DL7
DL2
DL8
DL3
DL9
VL1
DL4
DL10
DL5
DL11
DL6
DL12
VL2
DI2
DI1

FIG. 17

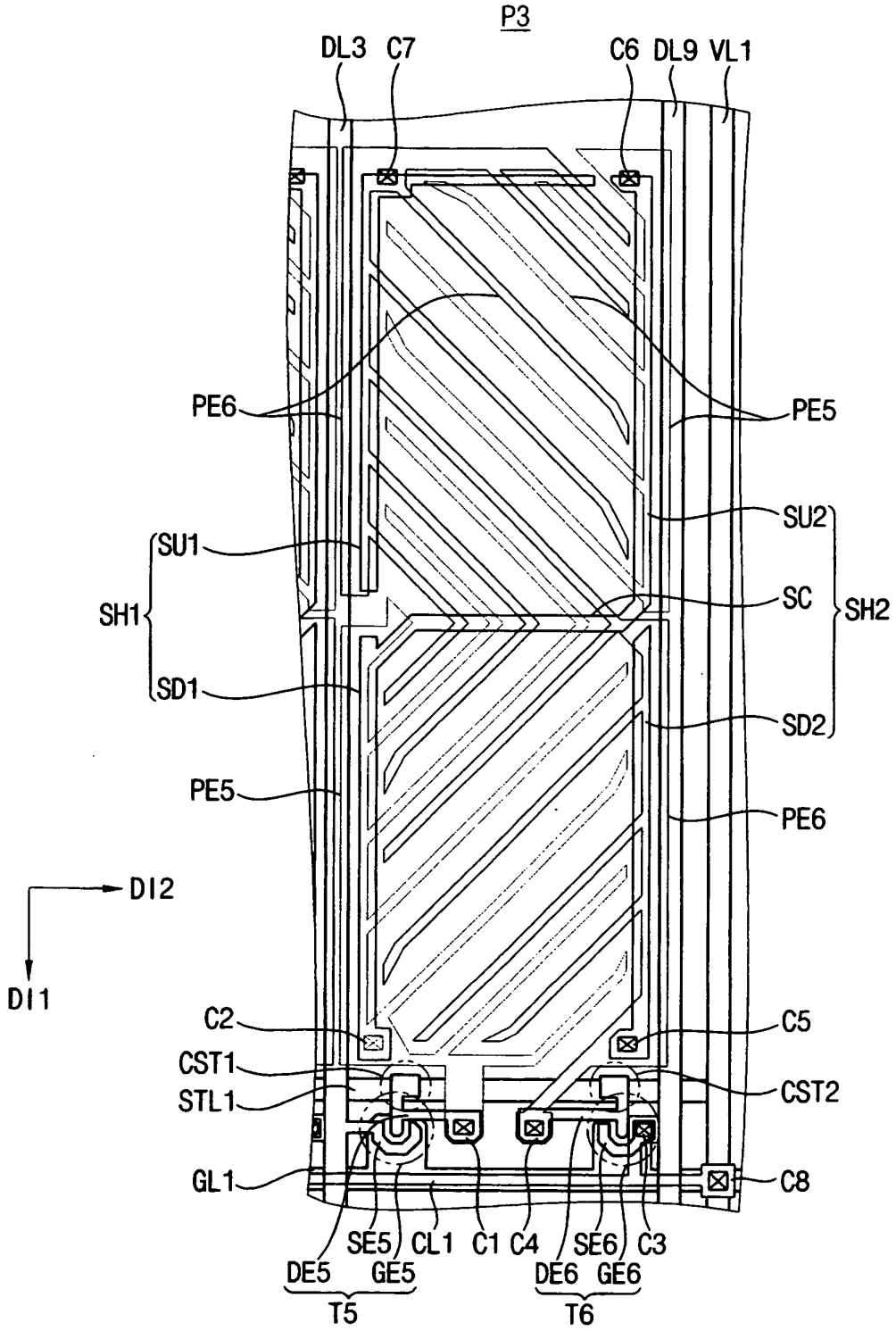

P3
DL3
C7
C6
DL9
VL1
PE6
PE5
SU1
SU2
SH1
SC
SH2
SD1
SD2
PE5
PE6
DI2
DI1
C2
C5
CST1
CST2
STL1
GL1
C8
SE5
CL1
C1
C4
SE6
C3
DE5
GE5
DE6
GE6
T5
T6

FIG. 18

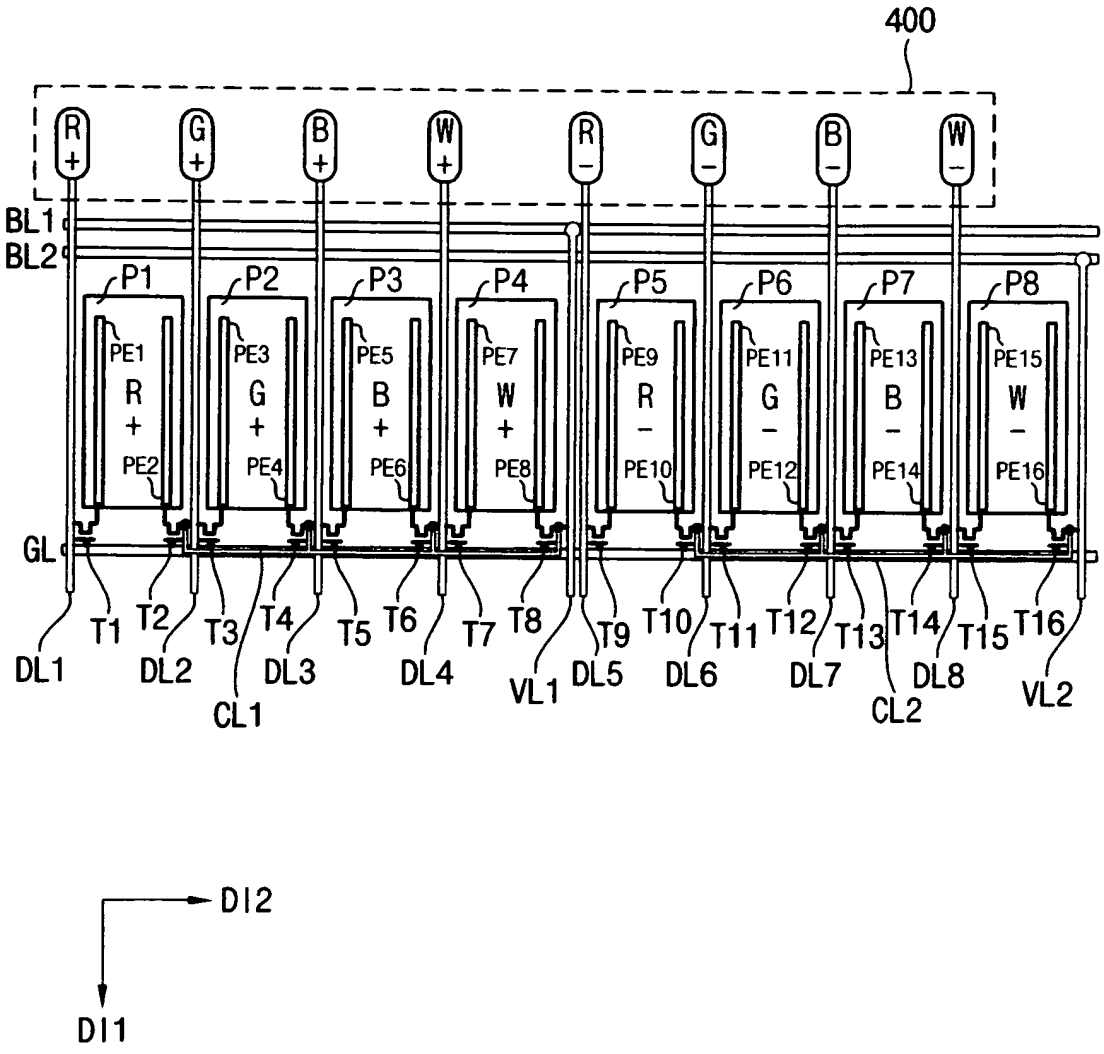

1000F
400
R +
G +
B +
W +
R −
G −
B −
W −
BL1
BL2
P1
P2
P3
P4
P5
P6
P7
P8
PE1
PE2
PE3
PE4
PE5
PE6
PE7
PE8
PE9
PE10
PE11
PE12
PE13
PE14
PE15
PE16
GL
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
T13
T14
T15
T16
DL1
DL2
DL3
DL4
DL5
DL6
DL7
DL8
CL1
CL2
VL1
VL2
DI2
DI1

FIG. 19

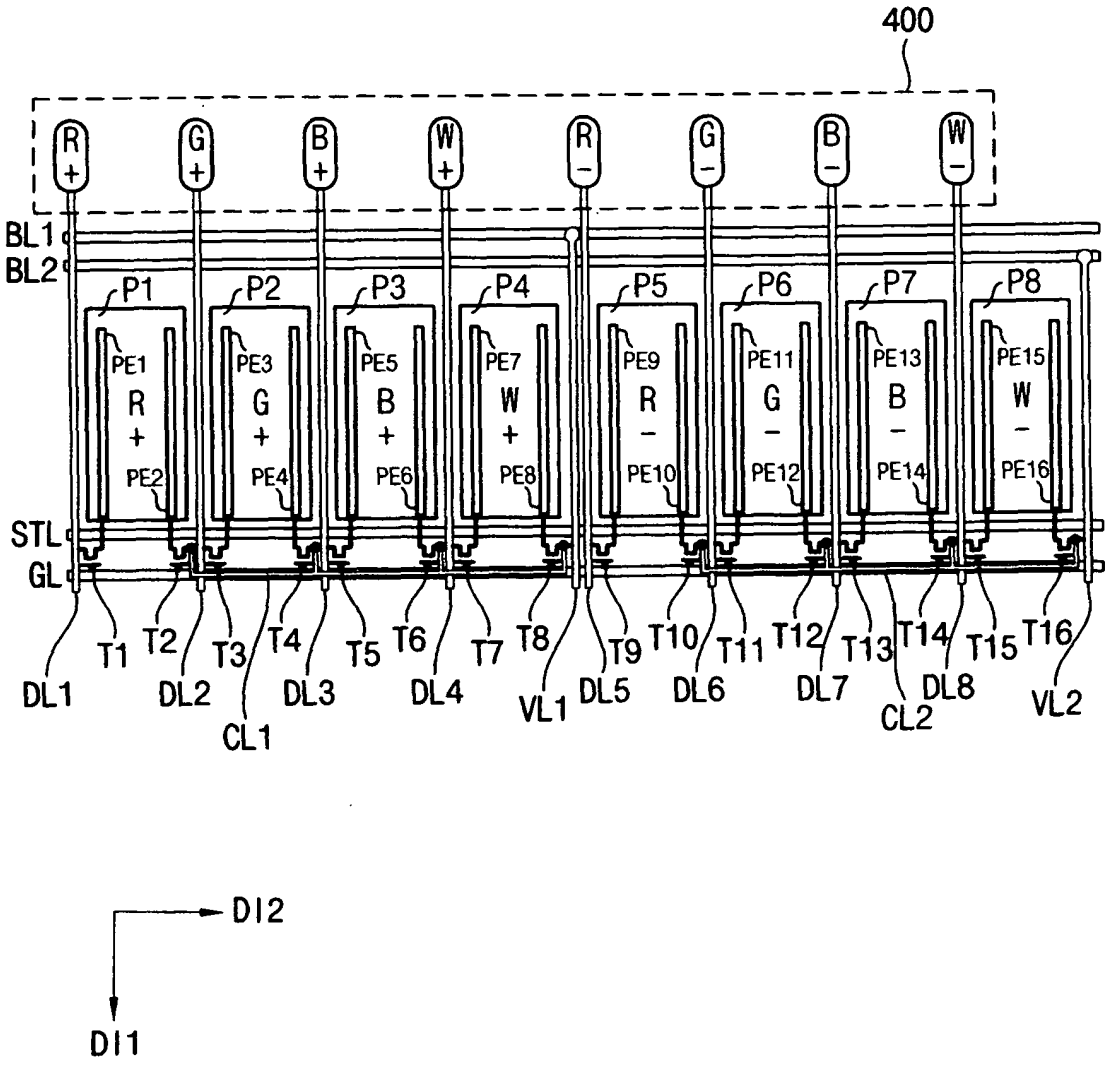

1000G
400
R +
G +
B +
W +
R −
G −
B −
W −
BL1
BL2
P1
P2
P3
P4
P5
P6
P7
P8
PE1
PE2
PE3
PE4
PE5
PE6
PE7
PE8
PE9
PE10
PE11
PE12
PE13
PE14
PE15
PE16
STL
GL
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
T13
T14
T15
T16
DL1
DL2
CL1
DL3
DL4
VL1
DL5
DL6
DL7
CL2
DL8
VL2
DI2
DI1

FIG. 20

1000H

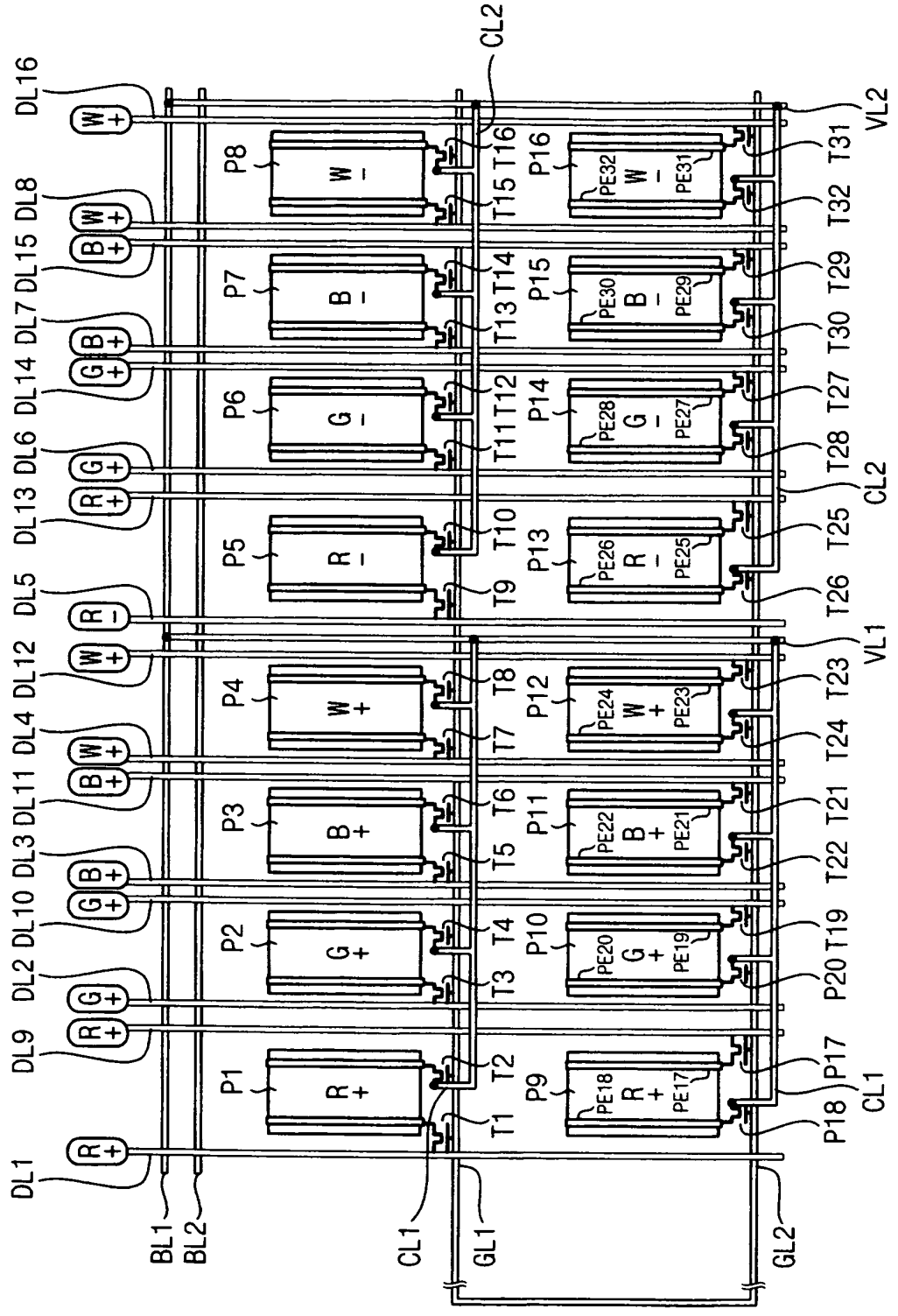

DL1
DL9
DL2
DL10
DL3
DL11
DL4
DL12
DL5
DL13
DL6
DL14
DL7
DL15
DL8
DL16
BL1
BL2
CL1
CL2
GL1
GL2
VL1
VL2
P1
P2
P3
P4
P5
P6
P7
P8
P9
P10
P11
P12
P13
P14
P15
P16
P17
P18
P19
P20
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
T13
T14
T15
T16
T19
T21
T22
T23
T24
T25
T26
T27
T28
T29
T30
T31
T32
PE17
PE18
PE19
PE20
PE21
PE22
PE23
PE24
PE25
PE26
PE27
PE28
PE29
PE30
PE31
PE32

FIG. 21

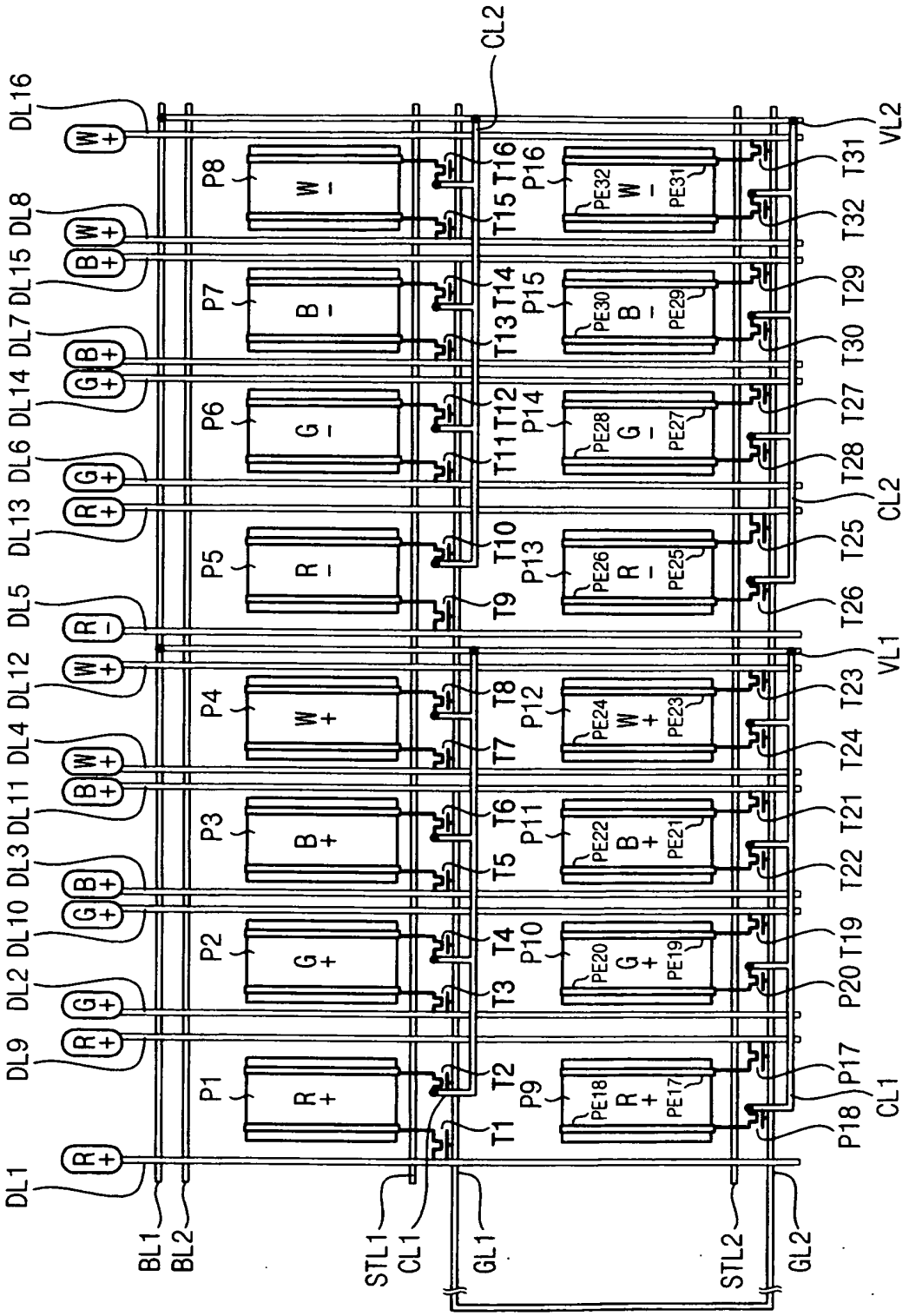

10001
DL1
DL2
DL3
DL4
DL5
DL6
DL7
DL8
DL9
DL10
DL11
DL12
DL13
DL14
DL15
DL16
BL1
BL2
STL1
CL1
GL1
STL2
GL2
CL2
VL1
VL2
P1
P2
P3
P4
P5
P6
P7
P8
P9
P10
P11
P12
P13
P14
P15
P16
P17
P18
P20
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
T13
T14
T15
T16
T19
T21
T22
T23
T24
T25
T26
T27
T28
T29
T30
T31
T32
PE17
PE18
PE19
PE20
PE21
PE22
PE23
PE24
PE25
PE26
PE27
PE28
PE29
PE30
PE31
PE32

FIG. 22

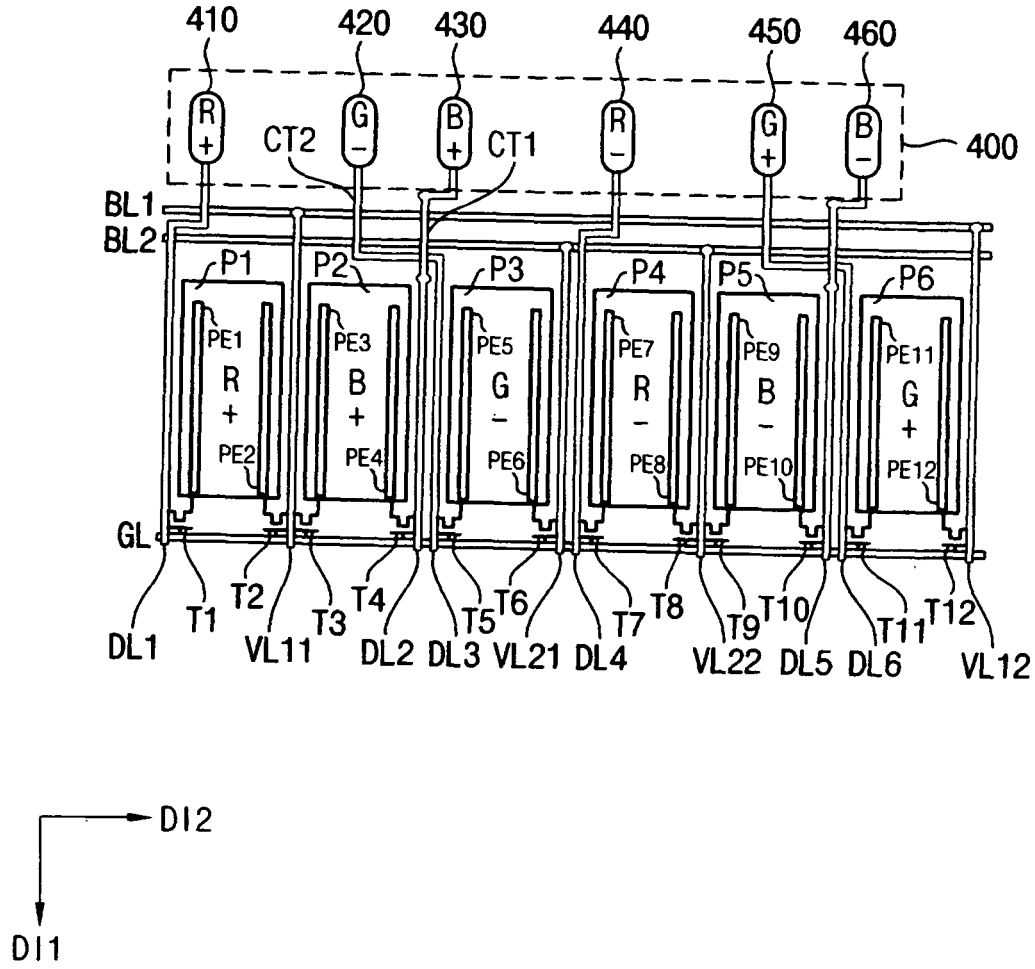

1000J
410
420
430
440
450
460
400
R +
G −
B +
R −
G +
B −
CT2
CT1
BL1
BL2
P1
P2
P3
P4
P5
P6
PE1
PE2
PE3
PE4
PE5
PE6
PE7
PE8
PE9
PE10
PE11
PE12
R + −
B + −
G − +
GL
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
DL1
VL11
DL2
DL3
VL21
DL4
VL22
DL5
DL6
VL12
DI2
DI1

FIG. 23

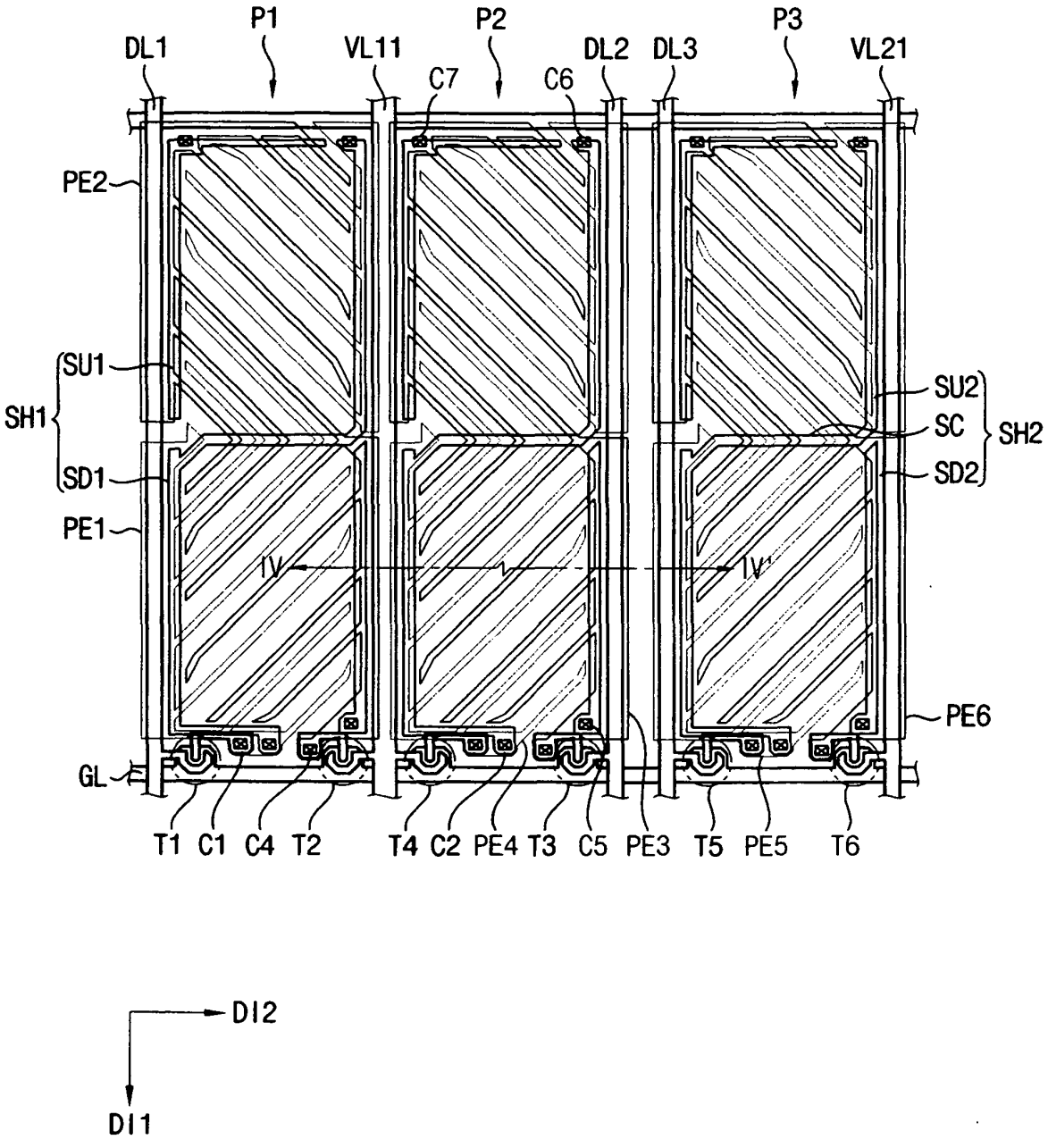

1000J
P1
P2
P3
DL1
VL11
C7
C6
DL2
DL3
VL21
PE2
SU1
SH1
SD1
PE1
IV
IV'
SU2
SC
SD2
SH2
PE6
GL
T1
C1
C4
T2
T4
C2
PE4
T3
C5
PE3
T5
PE5
T6
DI2
DI1

FIG. 24

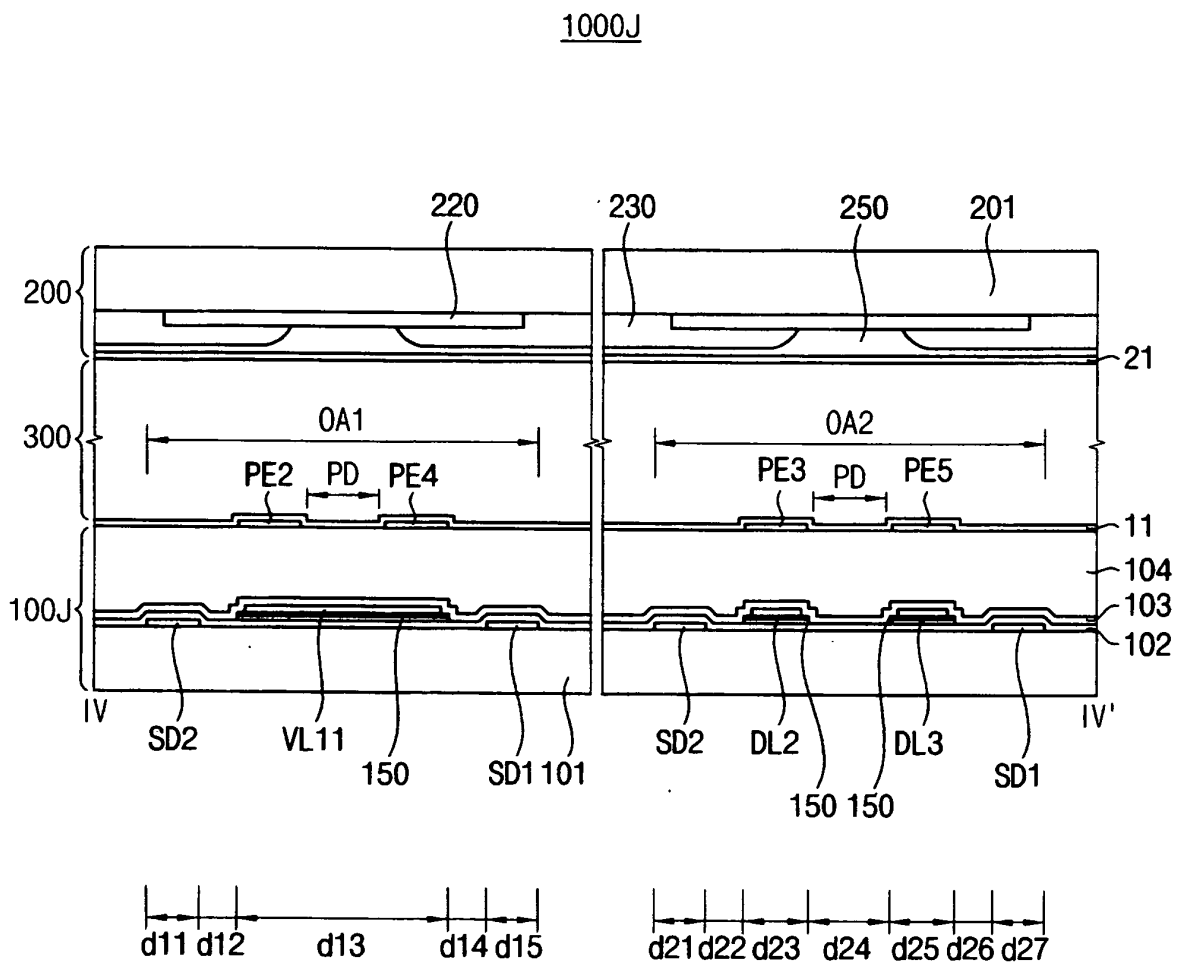

1000J
220
230
250
201
200
21
300
OA1
OA2
PE2
PD
PE4
PE3
PD
PE5
11
104
100J
103
102
IV
IV'
SD2
VL11
150
SD1
101
SD2
DL2
150
150
DL3
SD1
d11
d12
d13
d14
d15
d21
d22
d23
d24
d25
d26
d27

FIG. 25

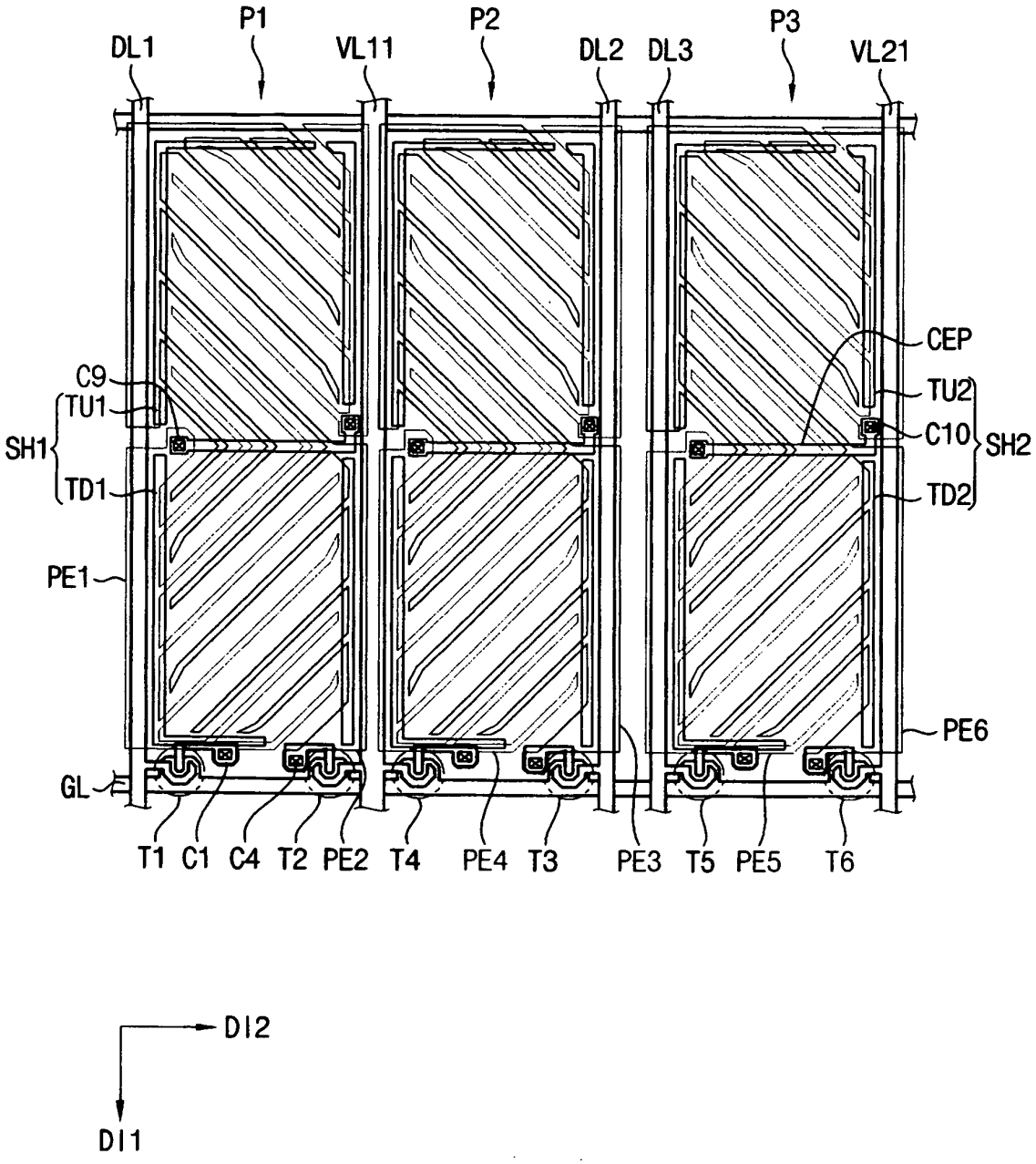

1000K
P1
P2
P3
DL1
VL11
DL2
DL3
VL21
CEP
C9
TU1
SH1
TD1
TU2
C10
SH2
TD2
PE1
PE6
GL
T1
C1
C4
T2
PE2
T4
PE4
T3
PE3
T5
PE5
T6
D12
D11

FIG. 26

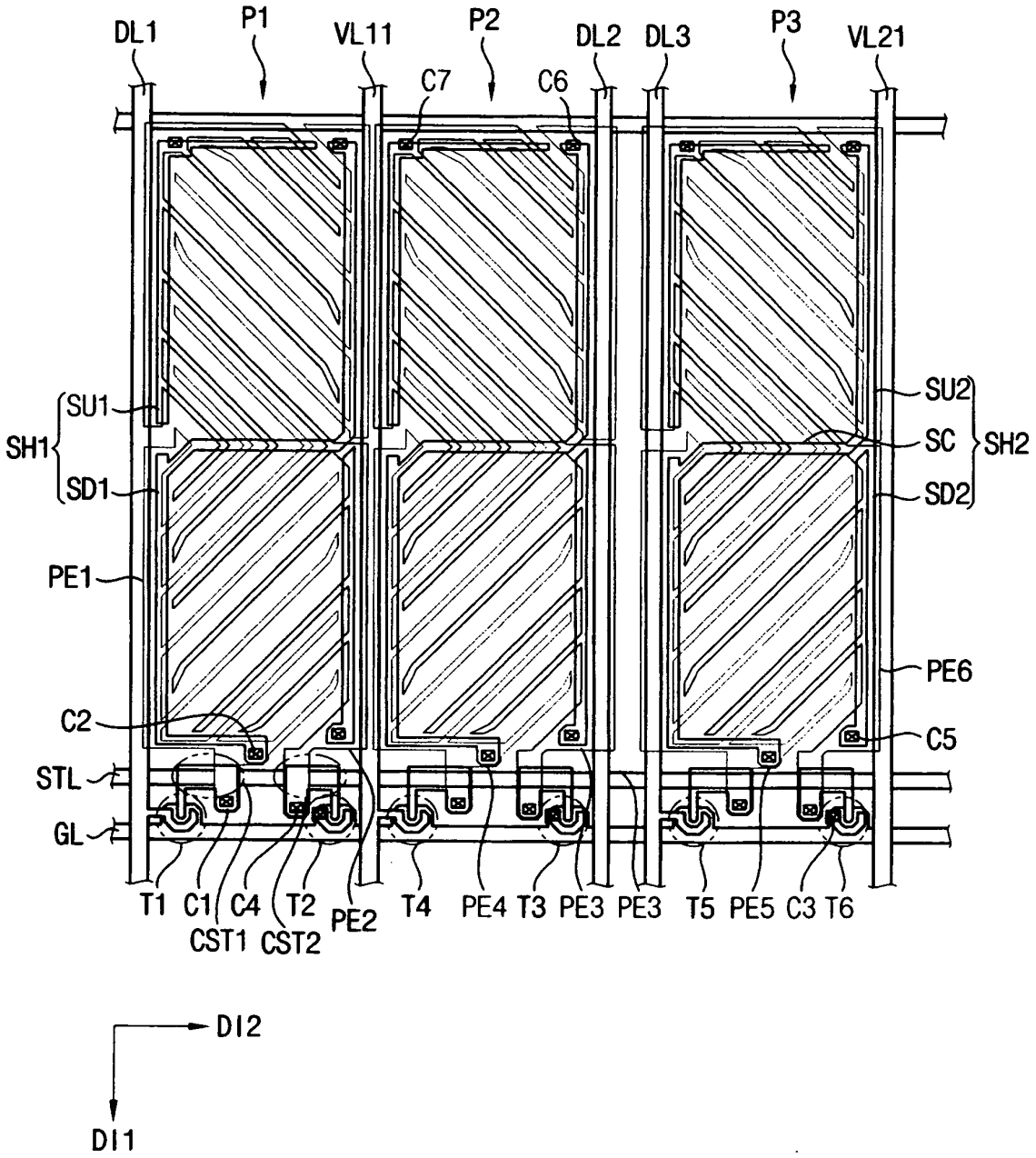

1000L
DL1
P1
VL11
P2
DL2
DL3
P3
VL21
C7
C6
SU1
SH1
SD1
PE1
C2
STL
GL
SU2
SC
SH2
SD2
PE6
C5
T1
C1
C4
T2
CST1
CST2
PE2
T4
PE4
T3
PE3
PE3
T5
PE5
C3
T6
D12
D11

FIG. 27

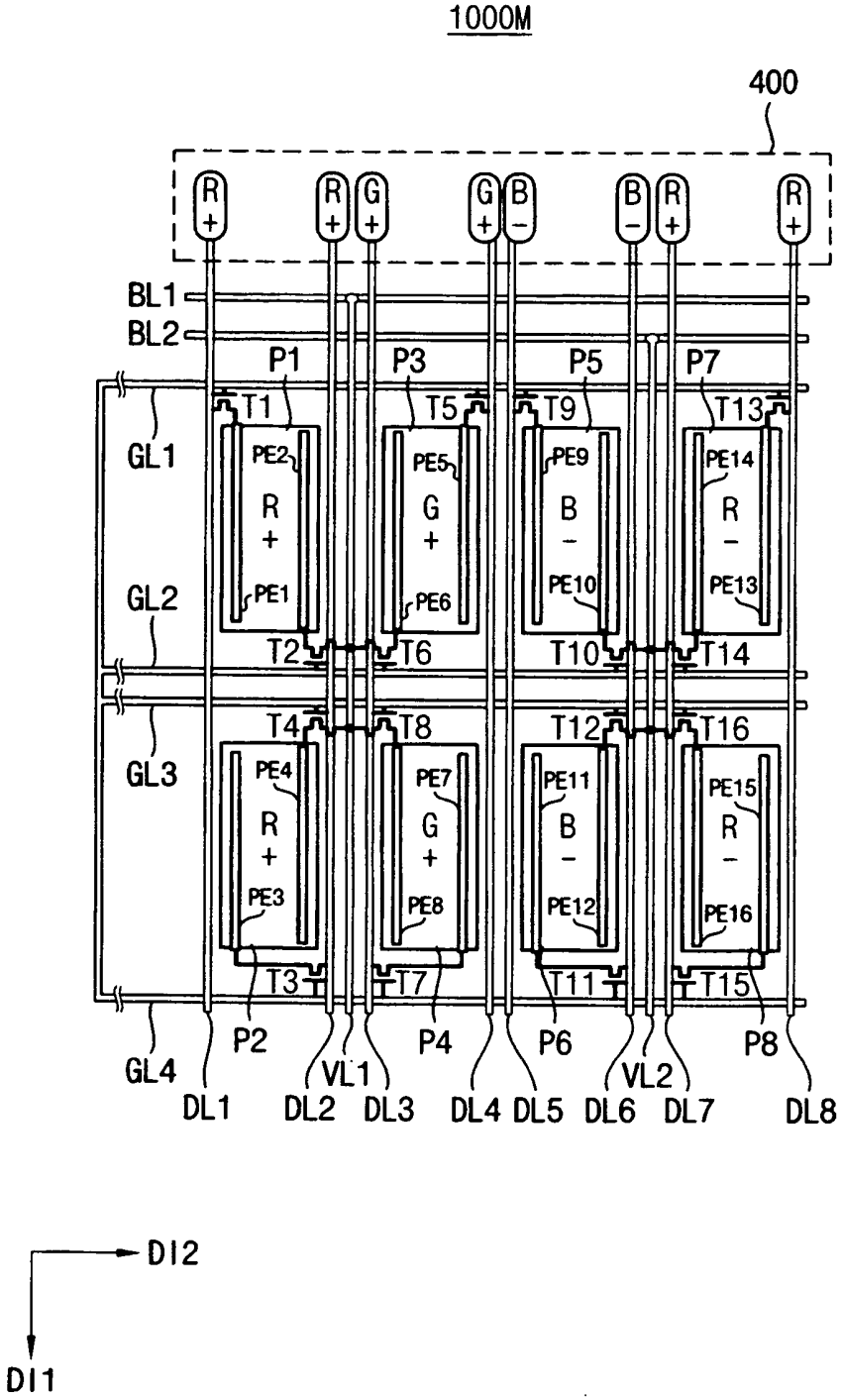
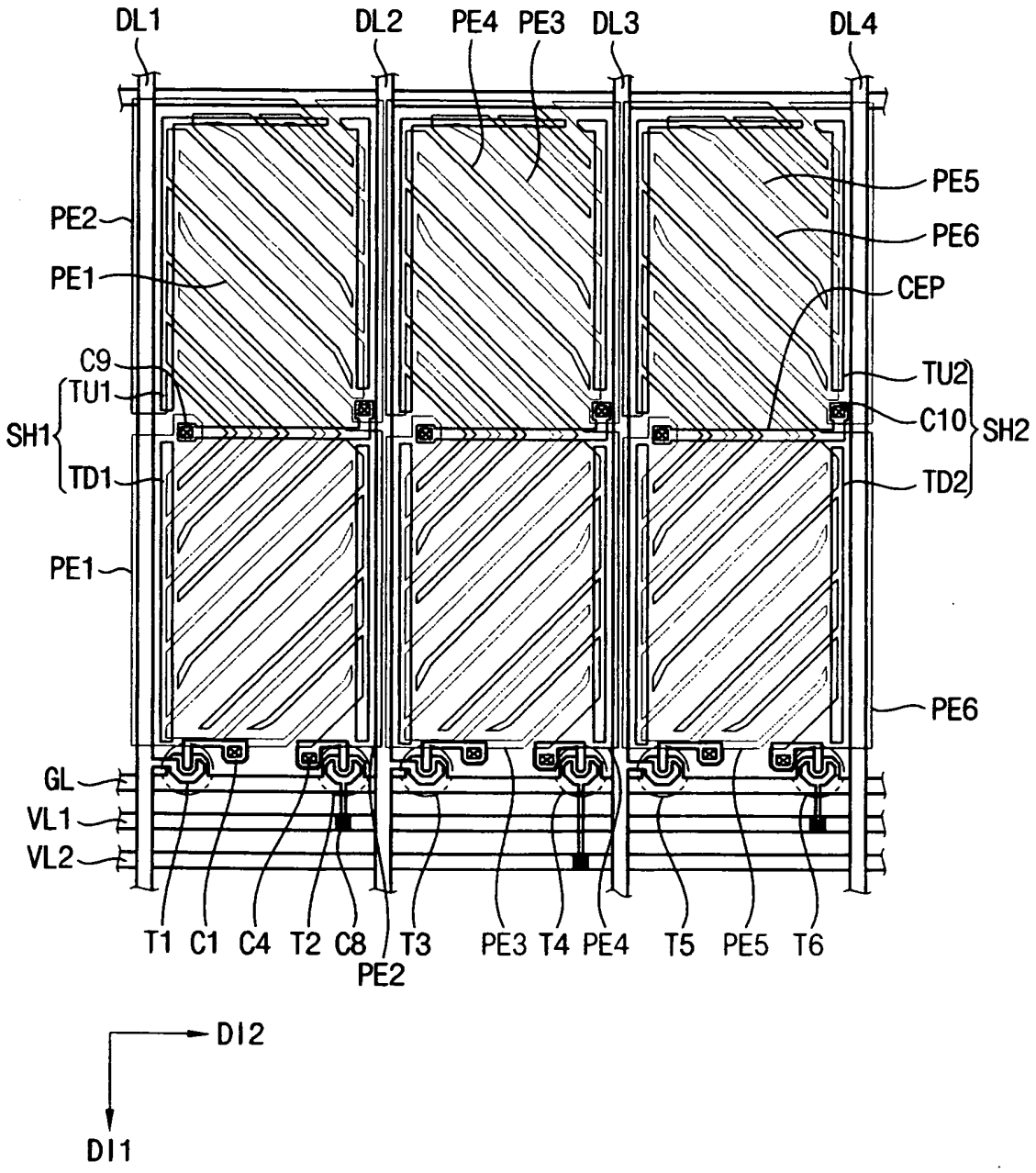

1000M
400
R +
R +
G +
G +
B −
B −
R +
R +
BL1
BL2
P1
P3
P5
P7
T1
T5
T9
T13
GL1
PE2
PE5
PE9
PE14
R +
G +
B −
R −
PE1
PE6
PE10
PE13
GL2
T2
T6
T10
T14
T4
T8
T12
T16
GL3
PE4
PE7
PE11
PE15
R +
G +
B −
R −
PE3
PE8
PE12
PE16
T3
T7
T11
T15
GL4
P2
P4
P6
P8
VL1
VL2
DL1
DL2
DL3
DL4
DL5
DL6
DL7
DL8
DI2
DI1

FIG. 28


1000N
DL1
DL2
PE4
PE3
DL3
DL4
PE5
PE2
PE6
PE1
CEP
C9
TU2
TU1
C10
SH2
SH1
TD1
TD2
PE1
PE6
GL
VL1
VL2
T1
C1
C4
T2
C8
PE2
T3
PE3
T4
PE4
T5
PE5
T6
DI2
DI1

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- US 2010103085 A1 **[0006]**
- US 2006290863 A1 **[0007]**
- US 2009262061 A1 **[0008]**

专利名称(译)	液晶显示装置		
公开(公告)号	EP2407823B1	公开(公告)日	2013-04-03
申请号	EP2011173209	申请日	2011-07-08
[标]申请(专利权)人(译)	三星电子株式会社		
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当前申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
[标]发明人	KIM DONG GYU NA HYE SEOK JUNG MEE HYE KI DONG HYEON CHO SE HYOUNG		
发明人	KIM, DONG-GYU NA, HYE-SEOK JUNG, MEE-HYE KI, DONG-HYEON CHO, SE-HYOUNG		
IPC分类号	G02F1/139 G02F1/1343 G02F1/1362 G09G3/36		
CPC分类号	G02F1/134363 G02F1/136209 G02F1/136213 G02F1/13624 G02F1/136286 G02F1/1393 G09G3/3614 G09G2300/0426 G09G2300/0452 G02F1/134327 G02F1/13458 G02F1/1368		
代理机构(译)	韦策尔，WOLFGANG		
优先权	1020100067661 2010-07-14 KR		
其他公开文献	EP2407823A2 EP2407823A3		
外部链接	Espacenet		

摘要(译)

液晶显示装置包括基板，栅极线（GL），第一和第二数据线（DL1，DL2），第一电源线（VL1），第一，第二，第三和第四开关元件（T1，T2，T3），T4），以及第一，第二，第三和第四像素电极（PE1，PE2，PE3，PE4）。第一开关元件（T1）连接到栅极线（GL）和第一数据线（DL1）。第二开关元件（T2）连接到栅极线（GL）和第一电源线（VL1）。第三开关元件（T3）连接到栅极线（GL）和第二数据线（DL2）。第四开关元件（T4）连接到栅极线（GL）和第一电源线（VL1）。第一至第四像素电极（PE1，PE2，PE3，PE4）分别连接到第一至第四开关元件（T1，T2，T3，T4）。因此，可以防止漏光并且可以增强显示基板的孔径比。

FIG. 1