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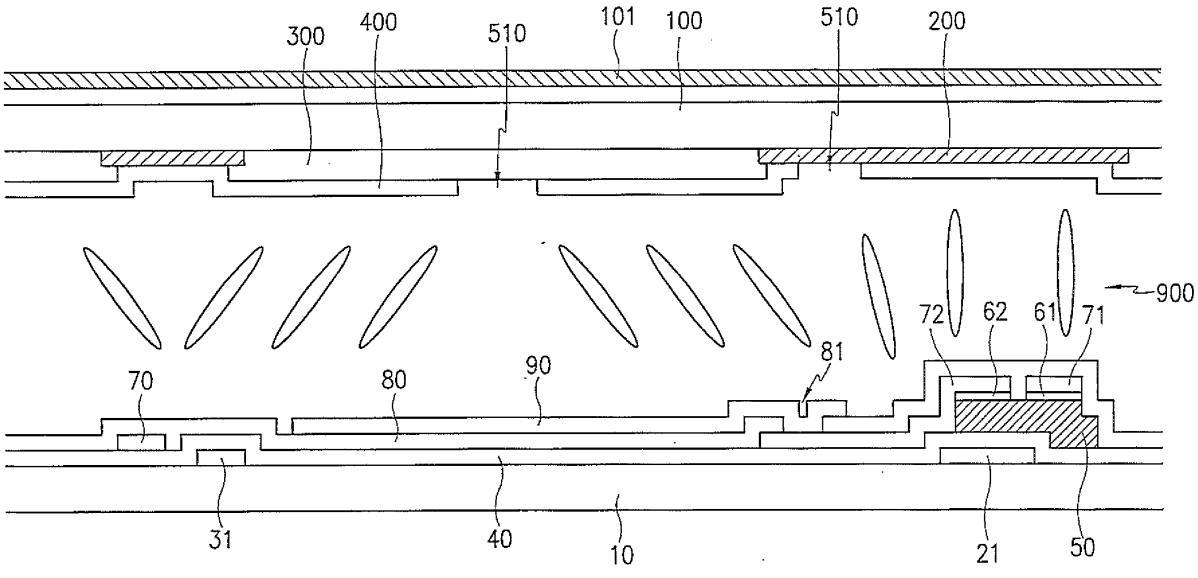
(54) Micro domain partitioning in an active liquid crystal display

(57) A pixel electrode (90) bearing a plurality of slits is formed on a first insulating substrate (10). A common electrode (400) is formed on a second insulating substrate (100) with a plurality of opening portions (510,520,530) and a black matrix (200) and a color filter (300). The horizontal opening portions of the pixel electrode and the opening portions of the common electrode (510,520,530) partition the pixel region into left, right, upper and lower domains. Liquid crystal material (900) is interposed between the first and second insulating substrates. Source and drain electrodes (71,72) are formed on ohmic contact layers (61,62) which are formed on a semiconductor layer (50) which is formed on a gate insulating layer (40) over the gate electrode (20). Certain pixel electrodes (90) may make capacitor-connection with respect to each other.

FIG.2



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Description

BACKGROUND OF THE INVENTION

(a) Field of the Invention

[0001] The present invention relates to a thin film transistor array panel for a liquid crystal display.

(b) Description of the Related Art

[0002] Generally, a liquid crystal display has two panels with electrodes, and a liquid crystal layer interposed between the two panels. Voltages are applied to the electrodes so that the liquid crystal molecules in the liquid crystal layer are re-oriented to thereby control the light transmission.

[0003] The liquid crystal display involves a critical shortcoming of a narrow viewing angle. In order to solve such a problem, various techniques of widening the viewing angle have been developed. For instance, It has been proposed that the liquid crystal molecules may be aligned perpendicular to the top and the bottom panels while forming a predetermined pattern of openings or protrusions at the pixel electrode and the common electrode.

[0004] In the case of formation of the opening pattern, the liquid crystal molecules are controlled in orientation by way of a fringe field due to the openings formed at the pixel electrodes and the common electrode.

[0005] In the case of formation of the protrusion pattern, protrusions are formed at the pixel electrode and the common electrode, and the liquid crystal molecules are controlled in orientation by way of an electric field deformed due to the protrusions.

[0006] Furthermore, it is possible that an opening pattern is formed at the pixel electrode of the bottom panel while forming a protrusion pattern at the common electrode of the top panel. The liquid crystal molecules are controlled in orientation by way of the fringe field due to the openings and the protrusions while forming a plurality of domains.

[0007] In such a multi-domain liquid crystal display, the viewing angle per the contrast ratio of 1:10 or the viewing angle defined as the limit angle of the inter-gray scale brightness inversion excellently reaches 80° or more in all directions. However, the lateral gamma curve is deviated from the front gamma curve so that visibility at the left and right sides is deteriorated, even compared to the twisted nematic (TN) mode liquid crystal display, For instance, in the patterned vertically aligned (PVA) mode where opening portions are formed for the domain partitioning, the screen becomes totally brighter as it comes to the lateral side, and the color becomes to be white. In a serious case, the difference in distance between the bright gray scales is removed while conglomerating the picture images. However, the trend is that visibility becomes important more and more as the monitor has been used for the multi-media purpose.

SUMMARY OF THE INVENTION

[0008] It is an object of the present invention to provide a multi-domain liquid crystal display which involves excellent lateral side visibility.

[0009] This and other objects may be achieved by a liquid crystal display with the following features. The electric field within the left and right domains is established to be weaker than that within the upper and lower domains.

[0010] According to one aspect of the present invention, the liquid crystal display has a plurality of pixel regions. Each pixel region has a plurality of micro domains. The micro domains include a first directional domain and a second directional domain having different average inclination directions of liquid crystal molecules upon application of an electric field. The electric field within the first directional domain is weaker than the electric field within the second directional domain by a predetermined value.

[0011] When viewed from a front side, the liquid crystal molecules in the first directional domain are inclined left and right while the liquid crystal molecules in the second directional domain are inclined up and down. The predetermined value of difference in the electric field between the first directional domain and the second directional domainranges from 0.02/d (V/um) to 0.5/d (V/um) where d is a cell gap.

[0012] According to another aspect of the present invention, the liquid crystal display has a first insulating substrate, and a first signal line formed on the first insulating substrate in a first direction. A second signal line is formed on the first insulating substrate in a second direction while intersecting the first signal line In an insulating manner. A first thin film transistor is connected to the first and the second signal lines. A second thin film transistor is connected to the first and the second signal lines connected to the first thin film transistor. A first pixel electrode is connected to the first thin film transistor. A second pixel electrode is connected to the second thin film transistor. A second insulating substrate faces the first insulating substrate. A common electrode is formed on the second insulating substrate. A liquid crystal layer is interposed between the first and the second substrates. A domain partitioning member is formed on at least one of the first and the second insulating substrates while partitioning the first and the second pixel electrodes into a plurality of

micro domains. The domain partitioning member partitions the first and the second pixel electrodes into first directional domains and second directional domains, and the first and the second pixel electrodes are capacitor-connected to each other.

[0013] The first and the second thin film transistors at the pixel of the nth pixel row on the m-th pixel column are connected to the m-th data line, and the first and the second thin film transistors at the pixel of the (n+1)-th pixel row on the m-th pixel column are connected to the (m+1)-th data line where n and m are integers. The second pixel electrode occupies the pixel region by 30-70%. The liquid crystal molecules in the liquid crystal layer are vertically aligned with respect to the first and the second insulating substrates in absence of an electric field.

[0014] A storage capacitor line is formed on (the first insulating substrate while being placed between the first pixel electrode and the second pixel electrode to thereby form a storage capacitor. When the liquid crystal capacitance formed between the second pixel electrode and the common electrode is indicated by Clcb, the storage capacitance formed between the second pixel electrode and the storage capacitor line is indicated by Cstb, and the connection capacitance formed between the first and the second pixel electrodes is indicated by Cpp, the value of T defined by the equation T = (Clcb+Cstb-Cpp)/(Clcb+Cstb+Cpp) is in the range of 0.65-0.95,

[0015] According to still another aspect of the present invention, the liquid crystal display has a first insulating substrate, and a first signal line formed at the first insulating substrate in a first direction. A second signal line is formed at the first insulating substrate in a second direction while crossing the first signal line in an insulating manner. A thin film transistor is connected to the first and the second signal lines. A pixel electrode is connected to the thin film transistor while bearing a plurality of slits. A second insulating substrate faces the first insulating substrate. A common electrode is formed at the second insulating substrate. A liquid crystal layer is interposed between the first and the second substrates. A domain partitioning member is formed on at least one of the first and the second insulating substrates while partitioning the pixel electrode into a plurality of micro domains. The domain partitioning member partitions the pixel electrode into first directional domains and second directional domains, and the first directional domains are placed at the area of the slits.

[0016] The slit width of the pixel electrode is established to be 2-5 μm, and the distance between the neighboring two slits is established to be 2-10 μm.

[0017] According to still another aspect of the present invention, the liquid crystal display has a first insulating substrate, and a first signal line formed at the first insulating substrate in a first direction. A second signal line is formed at the first insulating substrate in a second direction while crossing the first signal line in an insulating manner. A thin film transistor is connected to the first and the second signal lines. A pixel electrode is connected to the thin film transistor. A second insulating substrate faces the first insulating substrate. A common electrode is formed at the second insulating substrate. A dielectric layer is formed on at least one of the pixel electrode and the common electrode. A liquid crystal layer is interposed between the first and the second substrates. A domain partitioning member is formed on at least one of the first and the second insulating substrates while partitioning the pixel electrode into a plurality of micro domains. The domain partitioning member partitions the pixel electrode into first directional domains and second directional domains, and the dielectric layer is placed at the area of the first directional domains.

[0018] The thickness of the dielectric layer is established to be 500Å -1.5 μm. Opening portions are formed at the pixel electrode and the common electrode as the domain partitioning member.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] A more complete appreciation of the invention, and many of the attendant advantages thereof, will be readily apparent as the same becomes better understood by reference to the following detailed description when considered in conjunction with the accompanying drawings in which like reference symbols indicate the same or the similar components, wherein:

Fig. 1 is a plan view of a liquid crystal display according to a first preferred embodiment of the present invention;
Fig. 2 is a cross sectional view of the liquid crystal display taken along the II-II' line of Fig. 1;
Fig. 3 is a graph illustrating the gamma curves at the front side of the test cell and the 60° side thereof;
Fig. 4 illustrates the VT curves when a single-domain vertically aligned liquid crystal cell is viewed from eight directions;
Fig. 5, illustrates the VT curve at the front side of a single-domain VA cell where the rubbing is vertically made in an anti-parallel manner, the average VT curve at the left and right 60° sides thereof, the average VT curve at the top and bottom 60° sides thereof, and the curve of making the top and bottom average curve move by 0.3V;
Fig. 6 is a plan view of a liquid crystal display according to a second preferred embodiment of the present invention;
Fig. 7 is a cross sectional view of the liquid crystal display taken along the VII-VII' line of Fig. 6;
Fig. 8 is a cross sectional view of a liquid crystal display according to a third preferred embodiment of the present invention;
Fig. 9 is a plan view of a liquid crystal display according to a fourth preferred embodiment of the present invention;
Figs. 10 and 11 are cross sectional views of the liquid crystal display taken along the XI-XI' line and the XII-XII' line

of Fig. 9;
Fig. 12 is an equation circuit diagram of a liquid crystal display with the thin film transistor array panel shown in Fig. 9;
Fig. 13 is a plan view of a liquid crystal display according to a fifth preferred embodiment of the present invention; and
Fig. 14 is an equation circuit diagram of a liquid crystal display with the thin film transistor array panel shown in Fig. 13.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0020] Preferred embodiments of this invention will be explained with reference to the accompanying drawings.

[0021] Fig. 1 is a plan view of a liquid crystal display according to a first preferred embodiment of the present invention, and Fig. 2 is a cross sectional view of the liquid crystal display taken along the II-II' line of Fig. 1.

[0022] As shown in Figs, 1 and 2, gate lines 20 are formed on a transparent insulating substrate 10 such as glass while extending in the horizontal direction. Storage capacitor lines 30 extend parallel to the gate lines 20. Gate electrodes 21 protrude from the gate lines 20. First to fourth storage capacitor electrodes 31 to 34 and storage capacitor electrode connectors 35 and 36 are branched from the storage capacitor lines 30. The first storage capacitor electrode 31 is directly connected to the storage capacitor line 30 while extending in the vertical direction. The second and the third storage capacitor electrodes 32 and 33 are connected to the first storage capacitor electrode 31 while extending in the horizontal direction, The fourth storage capacitor electrode 34 is connected to the second and the third storage capacitor electrodes 32 and 33 while extending in the vertical direction. The storage capacitor electrode connectors 35 and 36 connect the fourth storage capacitor electrode 34 to the first storage capacitor electrode 31 at the pixel adjacent thereto. A gate insulating layer 40 is formed on the gate line assembly 20 and 21 and the storage capacitor line assembly 30 to 36, and a semiconductor layer 50 made of amorphous silicon is formed on the gate insulating layer 40 over the gate electrodes 21. An ohmic contact layer 61 and 62 made of amorphous silicon doped with n-type high concentration impurities such as phosphorous P is formed on the semiconductor layer 50 Source and drain electrodes 71 and 72 are formed on the ohmic contact layer 61 and 62, respectively. Data lines 70 are formed on the gate insulating layer 40 while extending in the vertical direction. The source electrodes 71 are connected to the data lines 70, A protective layer 80 is formed on the data lines assembly 70, 71 and 72 with contact holes 81 exposing the drain electrodes 72. A pixel electrode 90 is formed on the protective layer 80 at each pixel area while being connected to the drain electrode 72 through the contact hole 81. The pixel electrode 90 is formed with a transparent conductive material such as indium tin oxide (ITO) and indium zinc oxide (IZO). Each pixel area is defined by the two gate lines 20 and the two data lines 70 while being partitioned into upper and lower half parts.

[0023] The pixel electrode 90 is separated into first to third electrode portions 91 to 93, which are connected to each other by way of first to third connectors 94 to 96. The first electrode portion 91 is located at the lower half part of the pixel area, and has a rectangular shape where the four edges thereof are cut off. The first electrode portion 91 is directly connected to the drain electrode 72 through the contact hole 81. The second and the third electrode portions 92 and 93 are located at the upper half part of the pixel area, and have a rectangular shape with the four chamfered corners. The second electrode portion 92 is connected to the first electrode portion 91 by way of the first and the second connectors 94 and 96, and the third electrode portion 93 is connected to the second electrode portion 92 by way of the third connector 95.

[0024] A plurality of slits 99 are formed at the first electrode portion 91. The electric field generated between the first electrode portion 91 and the common electrode 400 due to the slits 99 is weaker than that generated between the common electrode 400 and the second electrode portion 92 or the third electrode portion 93.

[0025] Meanwhile, the second storage capacitor electrode 32 is placed between the first electrode portion 91 and the second electrode portion 92, and the third storage capacitor electrode 33 is placed between the second electrode portion 92 and the third electrode portion 93. The first storage capacitor electrode 31 and the fourth storage capacitor electrode 34 are placed between the pixel electrode 90 and the data line 70. The side of the first electrode portion 91 extending parallel to the data line is longer than the side thereof extending parallel to the gate line, The side of the second and the third electrode portions extending parallel to the data line is shorter than the side thereof extending parallel to the gate line. The second and the third electrode portions 92 and 93 overlapp the first and the fourth storage capacitor electrodes 31 and 34, but the first electrode portion 91 does not overlap the first and the fourth storage capacitor electrodes 31 and 34. The storage capacitor line 30 is placed between the gate line 20 and the third electrode portion 93. The electric potential to be applied to the common electrode for the color filter panel is usually applied to the storage capacitor line 30, the storage capacitor electrodes 31 to 34, and the storage capacitor electrode connectors 35 and 36.

[0026] As described above, when the storage capacitor line or the storage capacitor electrode to be applied with the common electric potential is placed between the data line and the pixel electrode, or between the gate line and the pixel electrode, the affection of the data line electric potential and the gate line electric potential to the electric field of the pixel region is intercepted by the storage capacitor line and the storage capacitor electrode, thereby forming stable domains,

[0027] A color filter panel for the liquid crystal display will be now explained in detail.

[0028] A black matrix 200 is formed on a transparent glass substrate 100 with a double-layered structure while defining

the pixel areas. The double-layered structure for the black matrix 200 is formed with chrome/chrome oxide. A color filter 300 is formed at each pixel area, and a common electrode 400 is formed on the entire surface of the substrate 100 having the color filters 400 with a transparent conductive material. The common electrode 400 is provided with an opening pattern at each pixel area. The opening pattern includes first to third opening portions 510, 520 and 530. The first opening portion 510 bisects the lower half part of the pixel region in the vertical direction, and the second and the third opening portions 520 and 530 trisect the upper half part of the pixel region in the horizontal direction. Both ends of the respective opening portions 510, 520 and 530 are gradually enlarged while forming the shape of an isosceles triangle. The opening portions 510, 520 and 530 are separated from each other.

[0029] Alternatively, the black matrix may be formed with an organic material, and the color filters may be formed at the thin film transistor array panel.

[0030] The thin film transistor array panel and the color filter panel are aligned, and assembled with each other, A liquid crystal material 900 is injected between the two panels such that the directors of the liquid crystal molecules are aligned perpendicular to the panels. Two polarizing plates 11 and 101 are attached to the outer surfaces of the substrates 10 and 100 such that the polarizing axes thereof extend perpendicular to each other.

[0031] The electrode portions 91, 92 and 93 of the pixel electrode 90 at the thin film transistor array panel, and the first to third opening portions 510, 520 and 530 of the common electrode 400 at the color filter panel overlap each other to thereby partition the pixel region into a plurality of micro-domains. The micro-domains partitioned by the first electrode portion 91 and the first opening portion 510 are referred to as the upper and lower domains (extending in the horizontal direction), and the micro-domains partitioned by the second and third electrode portions 92 and 93 and the second and third opening portions 520 and 530 are referred to as the left and right domains (extending in the vertical direction). This distinction is made depending upon the inclination directions of the liquid crystal molecules upon the application of the electric field. The respective electrode portions 91 to 93 includes two long sides and two short sides. The long side of the each electrode portion extends parallel to the data line 70 or the gate line 20, and makes an angle of 45° with respect to the polarizing axis of the polarizing plate (as shown in Fig. 3). In case the long side of the respective electrode portions 91 to 93 of the pixel electrode 90 is positioned close to the data line 70 or the gate line 20, the storage capacitor line 30 or the storage capacitor electrodes 31 to 34 are arranged between the data line 70 and the long side of the relevant electrode portion or the gate line 20 and the long side of the relevant electrode portion. Meanwhile, it is preferable that the storage capacitor line assembly 30 to 34 is not positioned close to the short side of the electrode portions 91 to 93 of the pixel electrode 90. In case the storage capacitor line assembly is positioned close to the latter, it is completely covered by the pixel electrode 90, or positioned distant from the pixel electrode 90 by 3 μm or more. The reason is that the electric potential of the data line 70 or the gate line 20 operates in the direction of hindering the domain formation at the area where the data line 70 or the gate line 20 is positioned close to the long side of the pixel electrode portions 91 to 93. On the contrary, the electric potential of the data line 70 or the gate line 20 operates in the direction of exerting the domain formation at the area where the data line 70 or the gate line 20 is positioned close to the short side of the pixel electrode portions 91 to 93.

[0032] Meanwhile, the electric field formed within the left and right domains due to the slit 99 at the first pixel electrode portions 91 is weaker than that formed within the upper and lower domains by a predetermined degree. With this structure, the visibility of the liquid crystal display at the left and the right sides can be improved. When the cell gap of the liquid crystal display is indicated by d (m), the electric field formed within the left and right domains preferably bears a value of from 0.02/d (V/um) to 0.5/d (V/um), which is weaker than the electric field formed within the upper and lower domains, That is, the voltage difference between the common electrode and the pixel electrode is established such that the voltage at the left and right domains is weaker than that at the upper and lower domains by 0.1-1V. For this purpose, the width of the slit 99 is preferably established to be 2-5 microns, and the distance between the neighboring two slits 99 is established to be 2-10 microns.

[0033] Fig. 3 is a graph illustrating the gamma curves at the front side of a test cell and at the 60°-lateral side thereof.

[0034] As shown in Fig. 3, the gamma curve at the front side of the test cell turns out to be higher than the gamma curve at the 60°-lateral side thereof. Particularly, as the width between the front side gamma curve and the lateral side gamma curve is significantly great, the brightness difference of two times to ten times is made depending upon whether the same gay scale is viewed from the front side or from the lateral side. As the gray scales of the red, green and blue pixels are varied separately, the deformation degree in the gamma curve at the lateral side is differentiated at the red, green and blue pixels. Therefore, when viewed from the lateral side, the pixels seem to bear an entirely different color compared to the case where the same pixels are viewed from the front side. For instance, as shown in Fig. 5, assuming that the red, green and blue pixels express 56 gray scales, 48 gray scales and 24 gray scales, when viewed from the front side, the ratios of the red, green and blue colors are established to be as follows: R:G:B = 73:50:10 = 55%:37%:8%. By contrast, when viewed from the 60°-lateral side, the ratios of the red, green and blue colors are established to be as follows: R:G:B = 75:66:41 = 41 %:36%:23%. That is, in the latter case, the content of the blue color becomes heightened by three times or more so that the relevant pixel seems to bear an entirely different color.

[0035] In case the gamma curve is deformed as shown in Fig. 5, the low-proportioned color at the front side becomes

increased in the proportion at the lateral side. By contrast, the high-proportioned color at the front side becomes decreased in the proportion at the lateral side. In this way, the ratios of the red, green and blue colors become to be approximated to each other. Consequently, the colors seemed to be different when viewed from the front side become reduced in the difference in the color sensation when viewed from the lateral side. The colors become totally light while being approximated to the white color, and this is called the "white-shift." As a result, the color representation property becomes deteriorated, and the picture image appears to be cloudy. The most important cause of the white-shift is that the deformation of the gamma curve is serious at the lower gray scales. Even if the gamma deformation is made at the higher gray scales, it is extremely small. However, when the gamma deformation is made at the lower gray scales of 32 or less, the brightness difference is made by two times to ten times, and this makes the white-shift appear to a large scale.

[0036] Fig. 4 illustrates the VT curves when the single-domain vertically aligned liquid crystal cell is viewed from eight directions.

[0037] As shown in Fig. 4, the movement of the VT curve in the left direction with the lower gray scales is significantly made at the top side or at the bottom side. At the left and right sides, the curve at the lower gray scales is elevated with the same outline as that at the front side. At the left bottom side and the right bottom side, the gray scale inversion is made early, and the VT curve again moves in the right direction while being elevated. That is, the phenomenon where the gamma curve is deformed upward with the lower gray scales becomes serious when the direction of viewing the liquid crystal cell and the inclination direction of the liquid crystal molecules under the application of the electric field are the same (when viewed from the head or tail of the liquid crystal molecules), but becomes negligible when those directions are perpendicular to each other. Therefore, the gamma curve deformation at the left and right domains is important in viciously influencing the viewing angle based on the visibility at the left and right sides, and the gamma curve deformation at the upper and lower domains is important in viciously influencing the viewing angle based on the visibility at the top and bottom sides. From the viewpoint of the user, the viewing angle at the left and right sides is more important than the viewing angle at the top and bottom sides. In order to compensate the gamma curve deformation at the left and right domains that viciously influences the left and right side visibility, the strength in the electric field within the left and right domains becomes weaker compared to that within the upper and lower domains. This will be now explained in detail.

[0038] Fig. 5 illustrates the VT curve at the front side of a single-domain VA cell where the rubbing Is vertically made in an anti-parallel manner (the liquid crystal molecules being inclined up and downward), the average VT curve at the left and right 60° sides thereof, the average VT curve at the top and bottom 60° sides thereof, and the curve of making the top and bottom average curve move by 0.3V.

[0039] As shown in Fig. 5, the VT curve at the left and right sides nearly agrees to the VT curve at the front side with the lower gray scales, but the VT curve at the top and bottom sides begins to elevate at lower voltages compared to the VT curve at the front side. That is, the threshold voltage Vth turns out to be lowered at the top and bottom sides, compared to that at the front side. However, when the VT curve at the top and bottom side moves by about 0.3V, it nearly agrees to the VT curve at the front side with the lower gray scales. The fact that the VT curve at the top and bottom sides agrees to the VT curve at the front side means that the visibility at the top and bottom sides is the same as the visibility at the front side. After all, in order that the visibility at the left and right sides be enhanced to the same degree as the visibility at the front side, the left and right side VT curves at the, left and right domains may move by a predetermined voltage. The same effect as with the movement of the left and right side VT curve can be obtained in case the electric field within the left and right domains is established to be weaker than the electric field within the upper and lower domains.

[0040] Fig. 6 is a plan view of a thin film transistor array panel for a liquid crystal display according to a second preferred embodiment of the present invention, and Fig. 7 is a cross sectional view of the thin film transistor array panel taken along the VII-VII' line of Fig. 6.

[0041] As shown in Figs. 6 and 7, in this preferred embodiment, other components and structures of the liquid crystal display are the same as those related to the first preferred embodiment except that a dielectric layer 600 is formed on the first pixel electrode portion 91 without forming any slit there.

[0042] The effect of forming the dielectric layer 600 on the first pixel electrode portion 91 is the same as that of forming slits at the first pixel electrode portion 91. That is, the electric field within the left and right domains is established to be weaker than that within the upper and lower domains. The thickness of the dielectric layer 600 is established to be in the range of 500 Å -1.5 microns.

[0043] Fig. 8 is a sectional view of a liquid crystal display according to a third preferred embodiment of the present invention.

[0044] As shown in Fig. 8, in this preferred embodiment, other components and structures of the liquid crystal display are the same as those related to the first preferred embodiment except that a dielectric layer 600 is formed on the common electrode 400 while corresponding to the first pixel electrode portion 91 without forming any slit at the first pixel electrode portion 91.

[0045] The effect of forming the dielectric layer 600 on the common electrode 400 is the same as that of forming the slits at the first pixel electrode portion 91. That is, the electric field within the left and right domains is established to be weaker than that within the upper and lower domains.

[0046] Fig. 9 is a plan view of a thin film transistor array panel for a liquid crystal display according to a fourth preferred embodiment of the present invention, Figs. 10 and 11 are cross sectional views of the thin film transistor array panel taken along the XI-XI' line and the XII-XII' line of Fig. 9, and Fig. 12 is an equation circuit diagram of a liquid crystal display with the thin film transistor array panel shown in Fig. 9.

[0047] A gate line assembly and storage capacitor lines 30 are formed at a transparent insulating substrate 10 such as glass.

[0048] The gate line assembly Includes gate lines 20 extending in the horizontal direction, and gate electrodes 21 protruded from the gate lines 20 up and downward.

[0049] The storage capacitor line 30 extends parallel to the gate line 20. The storage capacitor line 30 may bear a branch line.

[0050] The gate line assembly and the storage capacitor line 30 are covered by a gate insulating layer 40, and a semiconductor layer 50 made of amorphous silicon is formed on the gate insulating layer 40. The semiconductor layer 50 overlaps the gate electrode 21 to thereby form a channel portion for the thin film transistor. An ohmic contact layer 61, 62 and 63 made of amorphous silicon doped with n-type high concentration impurities such as phosphorous are formed on the semiconductor layer 50.

[0051] A data line assembly and connection electrodes 74 are formed on the ohmic contact layer 61, 62 and 63 and the gate insulating layer 40. The data line assembly includes data lines 70 extending along the semiconductor layer 50, source electrodes 71 connected to the data lines 70, and first and second drain electrodes 72 and 73. The source electrodes 71 protrude from the data lines 70 while being placed over the gate electrodes 21. The first and the second drain electrodes 72 and 73 are placed at both sides of the source electrode 71, respectively. The first and the second drain electrodes 72 and 73 are extended into first and second pixel regions around the gate line 20. The connection electrode 74 partially overlaps the storage capacitor line 30 while electro-magnetically interconnecting the first and the second pixel electrodes 91 and 92 separated around the storage capacitor line 30. The ohmic contact layers 61, 62 and 63 are located only at the area where the semiconductor layer 50 overlapd the data line assembly.

[0052] A protective layer 80 is formed on the data line assembly. The protective layer 80 has first and second contact holes 81 and 82 exposing the one-sided ends of the first and second drain electrodes 72 and 73, and a third contact hole 83 exposing the one-sided end of the connection electrode 74.

[0053] First and second pixel electrodes 91 and 92 are formed on the protective layer 80 such that they are connected to the first and the second drain electrodes 72 and 73 through the first and the second contact holes 81 and 82. The second pixel electrode 92 is connected to the connection electrode 74 through the third contact hole 83. The first pixel electrode 91 is overlapped with the connection electrode 74 while making an electromagnetic combination (capacitor-combination). After all, the first and the second pixel electrodes 91 and 92 are capacitor-combined with each other by way of the connection electrode 74. The pixel electrodes 91 and 92 are made of a transparent conductive material such as indium tin oxide (ITO) and indium zinc oxide (IZO). Meanwhile, the first pixel electrode 91 is provided with a plurality of horizontal opening portions 95 extending in the horizontal direction. Vertical opening portions may be formed at the second pixel electrode 92. The occupation ratio of the first pixel electrode within one pixel region is preferably established to be 30-70%.

[0054] The electric potential of the common electrode counter to the pixel electrode 90 is usually applied to the storage capacitor line 30.

[0055] In the meantime, the color filter panel is provided with a black matrix, color filters and a common electrode. First to third opening portions 510, 520 and 530 are formed at the common electrode. The first opening portion 510 extends in the vertical direction such that it bisects the second pixel electrode 92 into left and right domains. The second and the third opening portions 520 and 530 trisect the first pixel electrode 91 up and downward. Consequently, the first pixel electrode 91 are vertically partitioned into four domains by way of the second and the third opening portions 520 and 530, and the horizontal opening portion 95.

[0056] The connection electrode 74 is formed on the same plane as the data line assembly. Alternatively, the connection electrode 74 may be formed on the same plane as the gate line assembly. In the latter case, the storage capacitor line 30 should not overlap the connection electrode 74,

[0057] The thin film transistor array panel is spaced apart from the color filter panel with a predetermined distance, and a liquid crystal material is injected between the two panels. The directors of the liquid crystal molecules are aligned vertical to the panels. A compensation film such as a biaxial film is attached to the color filter panel. Two polarizing plates are attached to the outer surfaces of the thin film transistor array panel and the color filter panel, respectively.

[0058] As described above, two thin film transistors and two pixel electrodes are formed at one pixel region, and the two pixel electrodes at the pixel neighbors are capacitor-connected to each other by way of a connection electrode. In this structure, excellent visibility can be obtained even when viewed from the left and right sides. This is because the voltage of the second pixel electrode 92 for the left and right domains is kept to be lower than the voltage of the first pixel electrode 91 so that the electric field within the left and right domains is weaker than that within the upper and lower domains.

[0059] The reason that the voltage of the second pixel electrode 92 for the left and right domains is kept to be lower than that of the first pixel electrode 91 for the upper and lower domains will be now explained with reference to Fig. 12.

[0060] In the drawing, Clca indicates the liquid crystal capacitance formed between the a pixel electrode and the common electrode, Csta indicates the storage capacitance formed between the storage capacitor line and the a pixel electrode, Clcb indicates the liquid crystal capacitance formed between the b pixel electrode and the common electrode, Cstb indicates the storage capacitance formed between the storage capacitor line and the b pixel electrode, and Cpp indicates the connection capacitance between the a pixel electrode and the b pixel electrode.

[0061] As shown in Fig. 12, the first and the second thin film transistors are connected to the same gate and data lines, and the first and the second pixel electrodes are connected to the first and the second thin film transistors, respectively, The first and the second pixel electrodes make capacitor-connection (Cpp) with respect to each other while interposing the storage capacitor line 30 between them.

[0062] In relation to one data line 70, when the nth gate line 20 becomes to be on, two thin film transistor (TFT) channels become to be on so that voltage is applied to the first and the second pixel electrodes P(n)-a, and P(n)-b. As the P(n)-b is capacitor-connected to the P(n+1)-a, it is affected by the on-state of the latter. In this connection, the voltages of P(n)-a and P(n)-b may be given by way of mathematical formulas 1 and 2.

$$V[P(n)-a] = Vd(n) \quad (1)$$

$$V[P(n)-b] = Vd(n)+[Vd(n+1)-V'd(n+1)]Cpp/(Clcb+Cstb+Cpp) \quad (2)$$

[0063] In the mathematical formulas 1 and 2, Vd(n) indicates the voltage applied to the data line to drive the P(n) pixel, and Vd(n+1) indicates the voltage applied to the data line to drive the P(n+1) pixel. Furthermore, the V'd(n+1) indicates the voltage applied to the P(n+1) pixel at the previous frame.

[0064] As expressed in the mathematical formulas 1 and 2, the voltage applied to the P(n)-b pixel differs from the voltage applied to the P(n)-a pixel. Particularly, in case dot inversion driving or line inversion driving is made while the next pixel row expressing the same gray scale as with the previous pixel row (practically, most of the pixels being similar to this case), Vd(n) = - Vd(n+1), and Vd(n) = -V'd(n) (assuming that the common electrode voltage is the earth voltage). Therefore, the mathematical formula 2 can be expressed by the following mathematical formula 3:

$$V[P(n)-b] = Vd(n)-2Vd(n)Cpp/(Clcb+Cstb+Cpp) = [(Clcb+Cstb-Cpp)/(Clcb+Cstb+Cpp)]Vd(n) = TVd(n), \quad (3).$$

where T = (ClcbtCstb-Cpp)/(Clcb+Cstb+Cpp).

[0065] It can be known from the mathematical formula 3' that the voltage applied to the P(n)-b pixel is lower than that applied to the P(n)-a pixel. The value of T is preferably established to be 0.65-0.95.

[0066] Fig. 14 is a plan view of a thin film transistor array panel for a liquid crystal display according to a fifth preferred embodiment of the present invention, and Fig. 15 is an equation circuit diagram of a liquid crystal display with the thin film transistor array panel shown in Fig. 14.

[0067] In this preferred embodiment, the thin film transistors and the pixel electrodes at one pixel column are alternately connected to two data lines. That is, the thin film transistor and the two pixel electrodes a and b at the P(n) pixel are connected to the m-th data line, and the thin film transistor and the two pixel electrodes a and b at the P(n+1) pixel are connected to the (m+1)-th data line. The detailed structure of each thin film transistor and pixel electrode is the same as that related to the third preferred embodiment except that the opening portions 95, 510, 520 and 530 are varied in their positions. That is, in the fourth preferred embodiment, the horizontal opening portion 95 is formed at the second pixel electrode 92. The first opening portion 510 is formed at the first pixel electrode 91 while bisecting the latter left and right, and the second and the third opening portions 520 and 530 are formed at the second pixel electrode 92 while trisecting the latter up and down, Consequently, the first pixel electrode 91 forms left and right domains, and the second pixel electrode 92 forms upper and lower domains.

[0068] In the above structure, when the dot inversion driving is made, the electric field within the left and right domains

is kept to be weaker than that within the upper and lower domains. That is, the electric potential of the first pixel electrode 91 is constantly kept to be lower than that of the second pixel electrode 92 so that the visibility at the left and right sides can be improved.

[0069] With the structure shown in Fig. 14, when the dot inversion driving is made, the voltage of the same polarity is applied to the pixel electrodes at the same pixel column so that the same effect as with the column inversion driving is resulted. Therefore, in case the next pixel row indicates the same gray scale as with the previous pixel row (practically, most of the pixels being similar to this case), Vd(n) = Vd(n+1), and Vd(n) = -V'd(n). Therefore, the mathematical formula 2 can be expressed by the following mathematical formula 4:

$$V[P(n)-b] = Vd(n)+2Vd(n)Cpp/(Clcb+Cstb+Cpp) = [(Clcb+Cstb+3Cpp)/(Clcb+Cstb+Cpp)]Vd(n) = TVd(n), \quad (4)$$

where T = (Clcb+Cstb+3Cpp)/(Clcb+Cstb+Cpp).

[0070] In the mathematical formula 4, the voltage of the b pixel is higher than that of the a pixel, Therefore, the electric field within the left and right domains is constantly kept to be weaker than that within the upper and lower domains.

[0071] As described above, the electric field at the left and right domains is constantly kept to be weaker than the upper and lower domains so that the visibility at the left and right sides can be enhanced.

[0072] While the present Invention has been described in detail with reference to the preferred embodiments, those skilled in the art will appreciate that various modifications and substitutions can be made thereto without departing from the spirit and scope of the present invention as set forth in the appended claims.

Claims

1. A liquid crystal display, comprising:

   a first substrate;
   a pixel area divided into a first portion and a second portion on the first substrate;
   a second substrate facing the first substrate; and
   a liquid crystal layer interposed between the first and second substrates,
   wherein the liquid crystal layer on each of the first portion and the second portion is divided into a plurality of domains, each of the plurality of domains being defined by a direction of liquid crystal molecules when an electric field is applied, and a value an electric field of the second portion is weaker than a value of an electric field of the first portion.

2. The liquid crystal display of claim 1, further comprising a plurality of first signal lines, and a pixel electrode on the first substrate.

3. The liquid crystal display of claim 2, wherein the pixel electrode is electrically connected to the first signal line with a first thin film transistor.

4. The liquid crystal display of claim 2, further comprising a plurality of second signal lines, wherein each of the second signal lines are respectively disposed between two adjacent first signal lines.

5. The liquid crystal display of claim 4, wherein a second signal line is capacitively coupled with the pixel electrode.

6. The liquid crystal display of claim 5, wherein the pixel electrode is overlapped by a portion of a second signal line.

7. The liquid crystal display of claim 1, wherein the domains of the liquid crystal layer are divided by a domain partitioning member.

8. The liquid crystal display of claim 1, wherein the liquid crystal molecules of a domain are initially aligned in a vertical direction with respect to the first substrate.

9. The liquid crystal display of claim 8, wherein the domains of the liquid crystal layer are divided by a domain partitioning member.

10. The liquid crystal display of claim 7 or 9, wherein the domain partitioning member is formed on the first substrate.

11. The liquid crystal display of claim 8 or 10, wherein the domain partitioning member includes a plurality of slits formed in a pixel electrode on the first substrate.

12. The liquid crystal display of claim 9 or 11, wherein a width of the slits is about 2 μm to about 5 μm.

13. The liquid crystal display of claim 10 or 12, wherein a width of the slits in the first portion is different from a width of the slits in the second portion.

14. A liquid crystal display according to claim 1, further comprising: a plurality of pixels, at least one of the pixels comprising a first pixel electrode and a second pixel electrode disposed on the first substrate on the same layer respectively;a liquid crystal layer interposed between the first and second substrates, wherein the liquid crystal layer on each of the first pixel electrode and the second pixel electrode is divided into a plurality of domains, each of the plurality of domains being defined by a direction of liquid crystal molecules when an electric field is applied, and a value of an electric field generated by the second pixel electrode is weaker than a value of an electric field generated by the first pixel electrode.

15. The liquid crystal display of claim 1, further comprising a plurality of first signal lines formed on the first substrate.

16. The liquid crystal display of claim 15, wherein the first pixel electrode is electrically connected to the first signal line with a first thin film transistor and the second pixel electrode is electrically connected to the first signal line with a second thin film transistor.

17. The liquid crystal display of claim 16, wherein the electric field of the first pixel electrode is different from the electric field of the second pixel electrode when the first thin film transistor and the second thin film transistor are off.

18. The liquid crystal display of claim 15, wherein the first pixel electrode and the second pixel electrode are paired with each other at opposite sides of the first signal line.

19. The liquid crystal display of claim 18, wherein the first pixel electrode is electrically connected to one of the first signal lines with a first thin film transistor and the second pixel electrode is electrically connected to the one of the first signal lines with a second thin film transistor.

20. The liquid crystal display of claim 14, wherein the domains of the liquid crystal layer are divided by a domain partitioning member.

21. The liquid crystal display of claim 20, wherein the domain partitioning member is formed on the first substrate.

22. The liquid crystal display of claim 20, wherein the domain partitioning member includes a plurality of slits.

23. The liquid crystal display of claim 22, wherein a width of the slits is about 2 μm to about 5 μm.

24. The liquid crystal display of claim 14, wherein the liquid crystal molecules of a domain are initially aligned in a vertical direction with respect to the first substrate.

25. The liquid crystal display of claim 24, wherein the domains of the liquid crystal layer are divided by a domain partitioning member.

26. The liquid crystal display of claim 25, wherein the domain partitioning member is formed on the first substrate.

27. The liquid crystal display of claim 26, wherein the domain partitioning member includes a plurality of slits in the first pixel electrode.

28. The liquid crystal display of claim 27, wherein a width of the slits is about 2 μm to about 5 μm.

29. The liquid crystal display of claim 14, wherein a voltage applied to the first pixel electrode is higher than a voltage applied to the second pixel electrode.

30. The liquid crystal display of claim 14, further comprising a connection electrode connected to the second pixel electrode.

31. The liquid crystal display of claim 30, wherein the connection electrode contacts the second pixel electrode through a contact hole formed in an insulating layer.

32. The liquid crystal display of claim 31, wherein the connection electrode overlaps the first pixel electrode via the insulating layer.

33. The liquid crystal display of claim 32, further comprising a plurality of second signal lines, wherein at least one of the second signal lines is disposed between two adjacent first signal lines.

34. The liquid crystal display of claim 33, wherein the second signal line is capacitively coupled with at least one of the first pixel electrode and the second pixel electrode.

35. The liquid crystal display of claim 32, wherein the second signal line is capacitively coupled with one of the first and second pixel electrodes of an adjacent pixel.

36. The liquid crystal display of claim 35, wherein the first pixel electrode is overlapped by a portion of the second signal line.

37. The liquid crystal display of claim 36, wherein the second pixel electrode is overlapped by a portion of a second signal line different from the second signal line overlapping the first pixel electrode.

38. The liquid crystal display of claim 37, wherein the connection electrode overlaps at least one portion of the second signal line overlapping the first pixel electrode.

39. The liquid crystal display of claim 14, wherein the area of the first pixel electrode is different from the area of the second pixel electrode.

40. The liquid crystal display of claim 39, wherein the area of the first pixel electrode is occupied by about 30% to about 70% of the area of the first pixel electrode and the second pixel electrode.

41. The liquid crystal display of claim 14, wherein the first pixel electrode and the second pixel electrodes are insulated from each other.

FIG.1

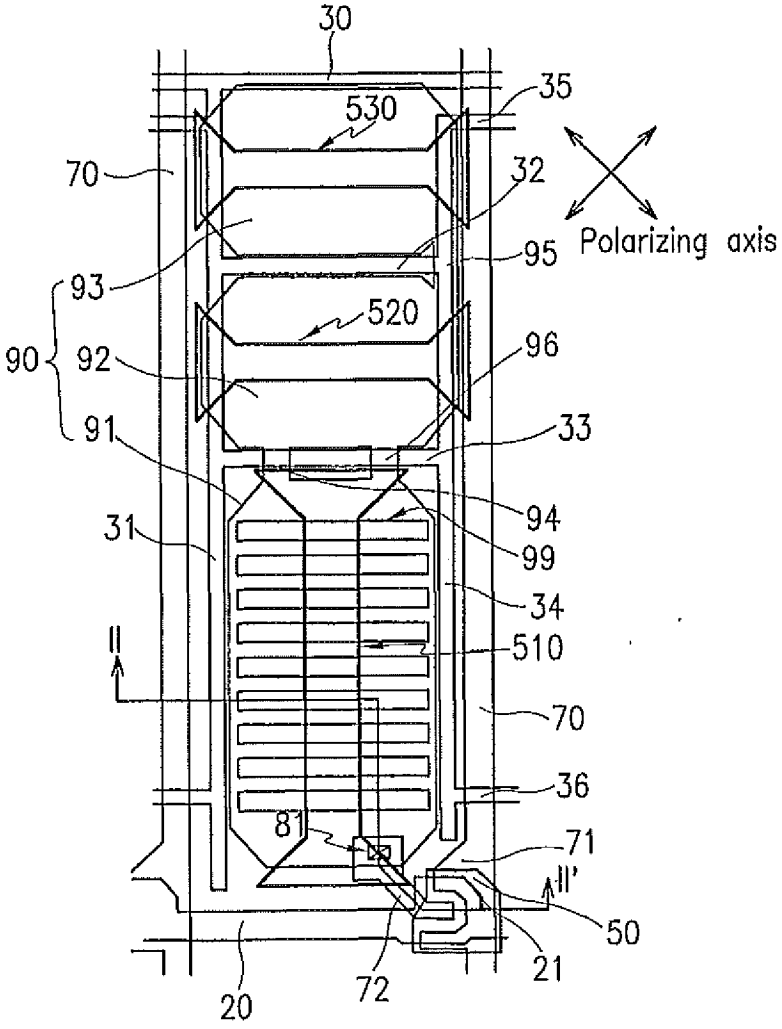

30
35
530
70
32
Polarizing axis
95
93
520
90
92
96
91
33
94
31
99
34
II
510
70
36
81
71
II'
50
21
72
20

FIG.2

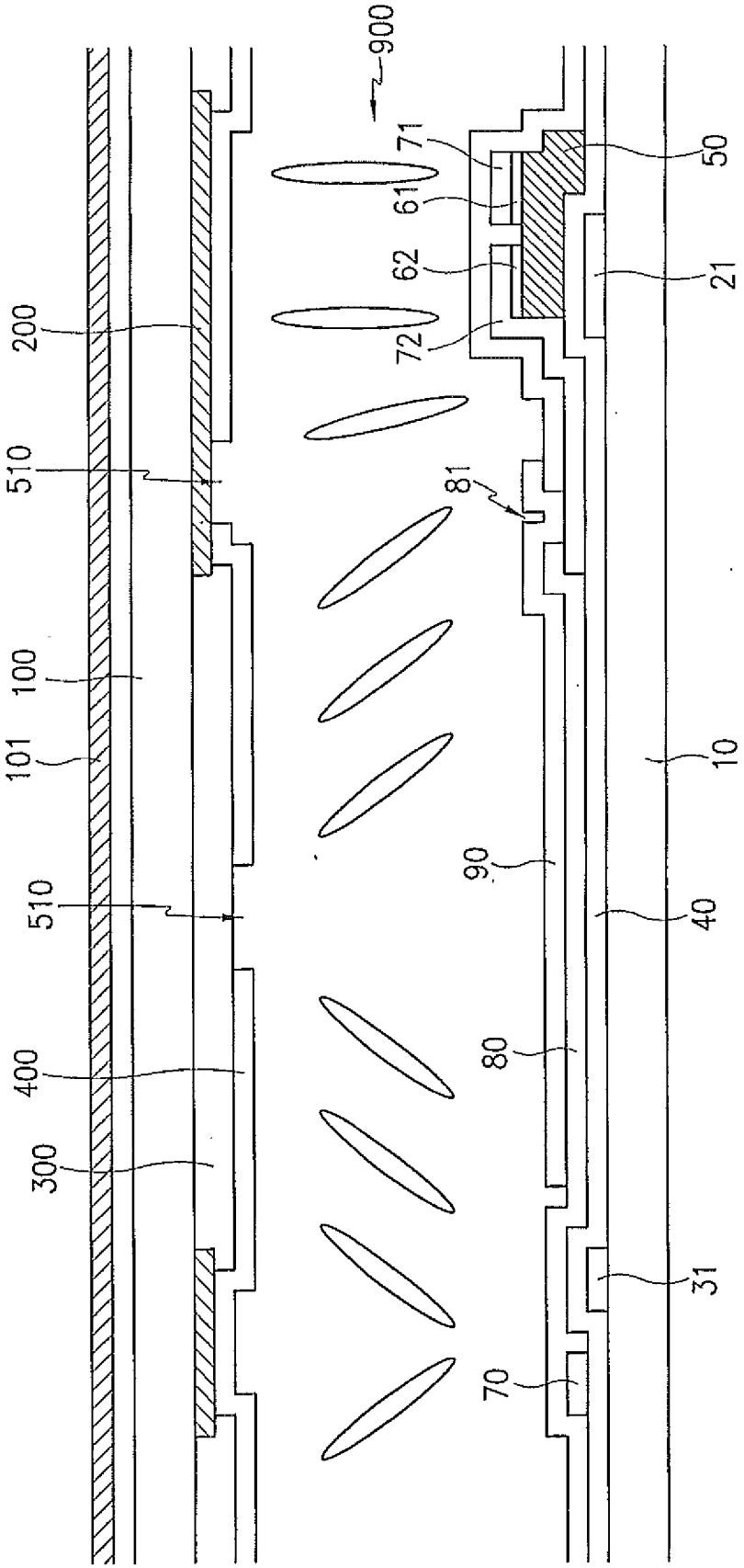

900
71
61
62
72
50
21
200
510
81
100
101
10
510
90
40
400
80
300
31
70

FIG.3

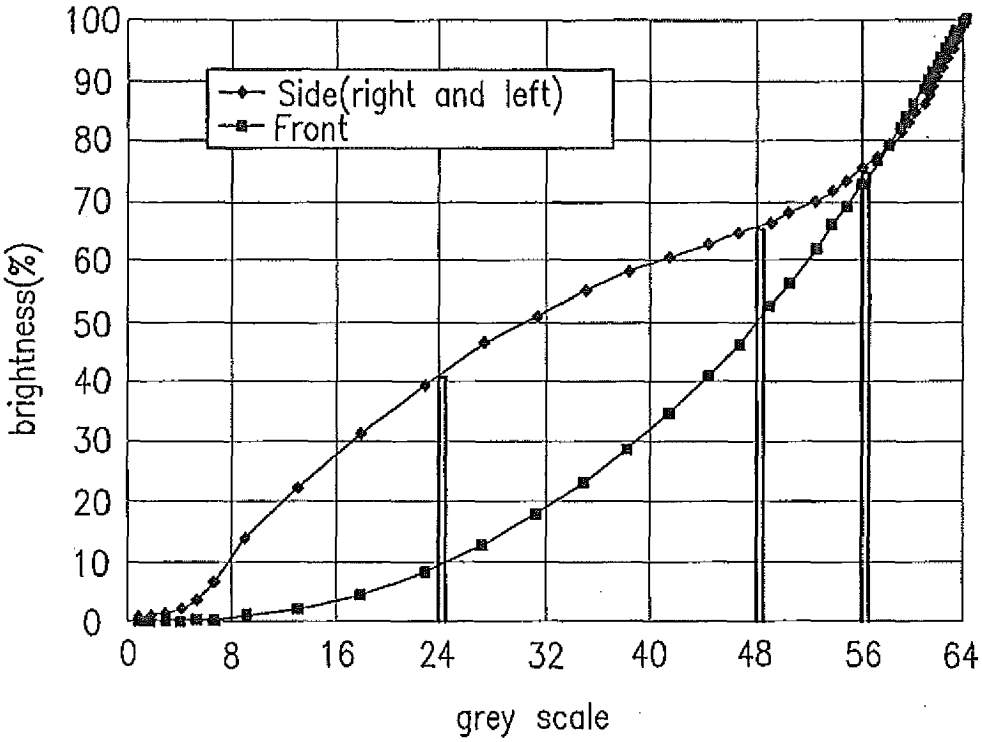

100
90
80
70
60
50
40
30
20
10
0
brightness(%)
Side(right and left)
Front
0
8
16
24
32
40
48
56
64
grey scale

FIG.4

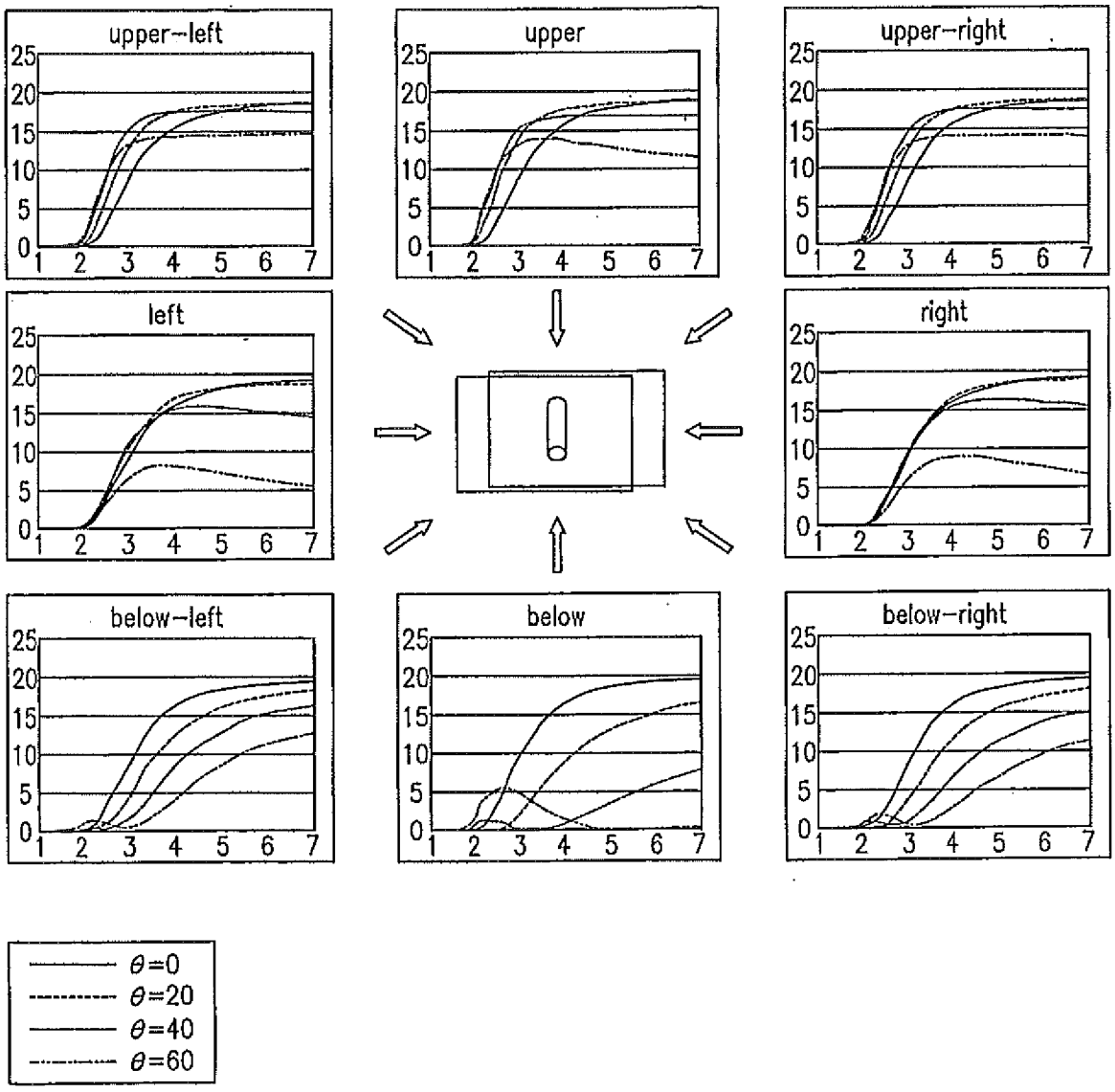

upper–left
upper
upper–right
left
right
below–left
below
below–right
25
20
15
10
5
0
1 2 3 4 5 6 7
θ=0
θ=20
θ=40
θ=60

FIG.5

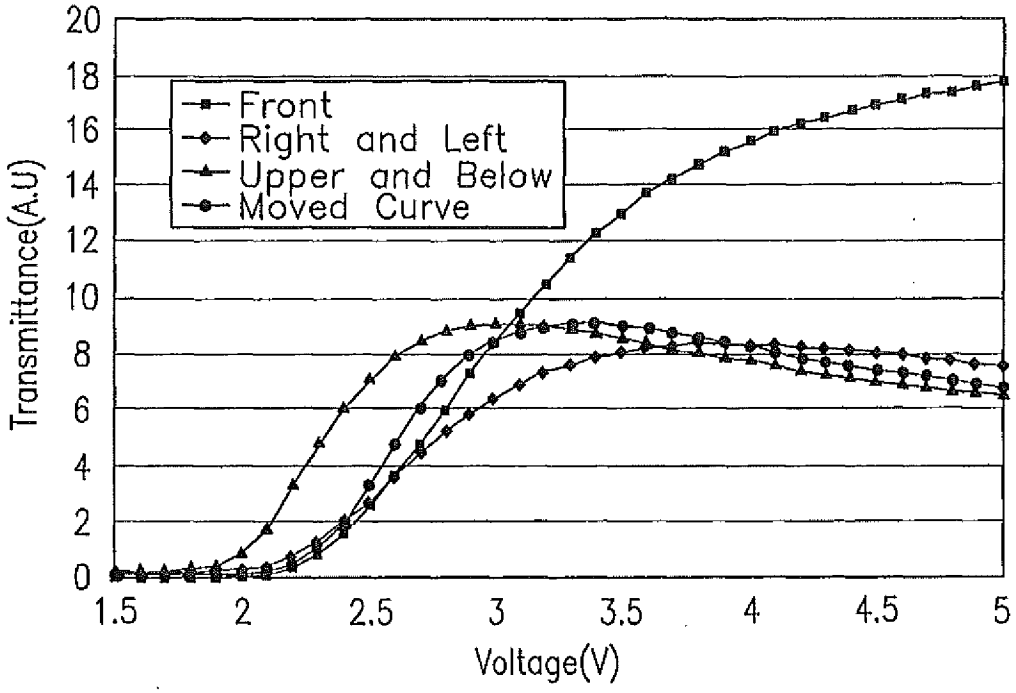

Front
Right and Left
Upper and Below
Moved Curve
Transmittance(A.U)
Voltage(V)
0
2
4
6
8
10
12
14
16
18
20
1.5
2
2.5
3
3.5
4
4.5
5

FIG.6

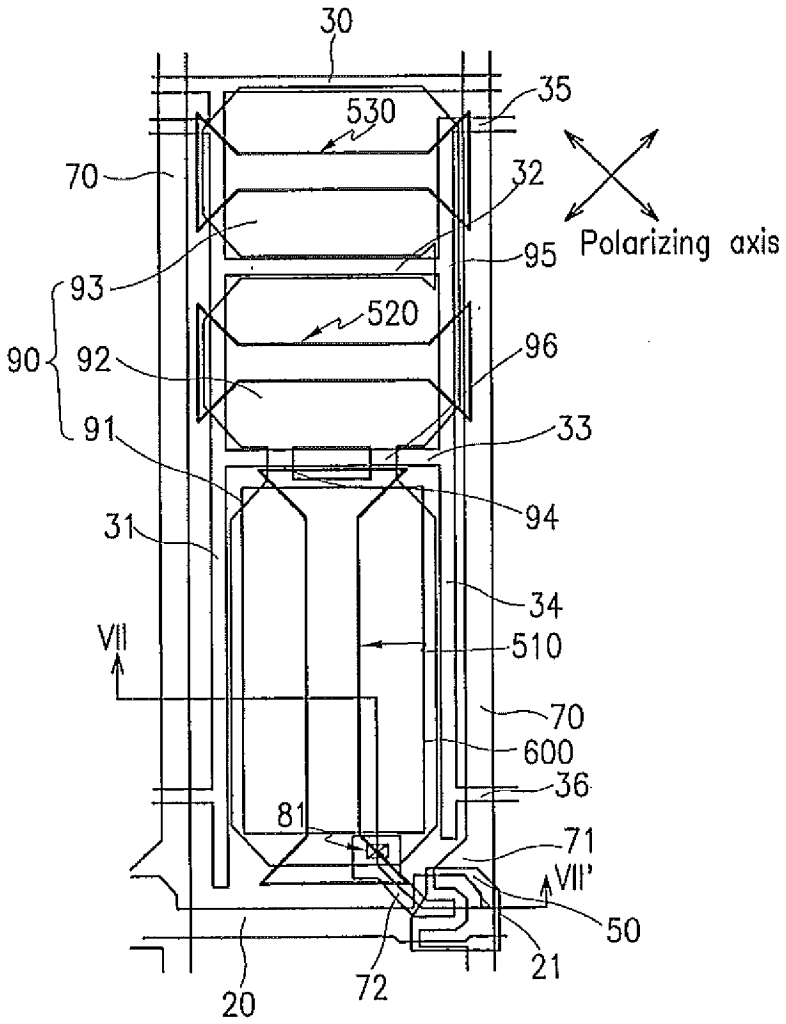

30
35
530
70
32
Polarizing axis
95
93
520
90
92
96
91
33
94
31
34
VII
510
70
600
36
81
71
VII'
50
21
20
72

FIG.7

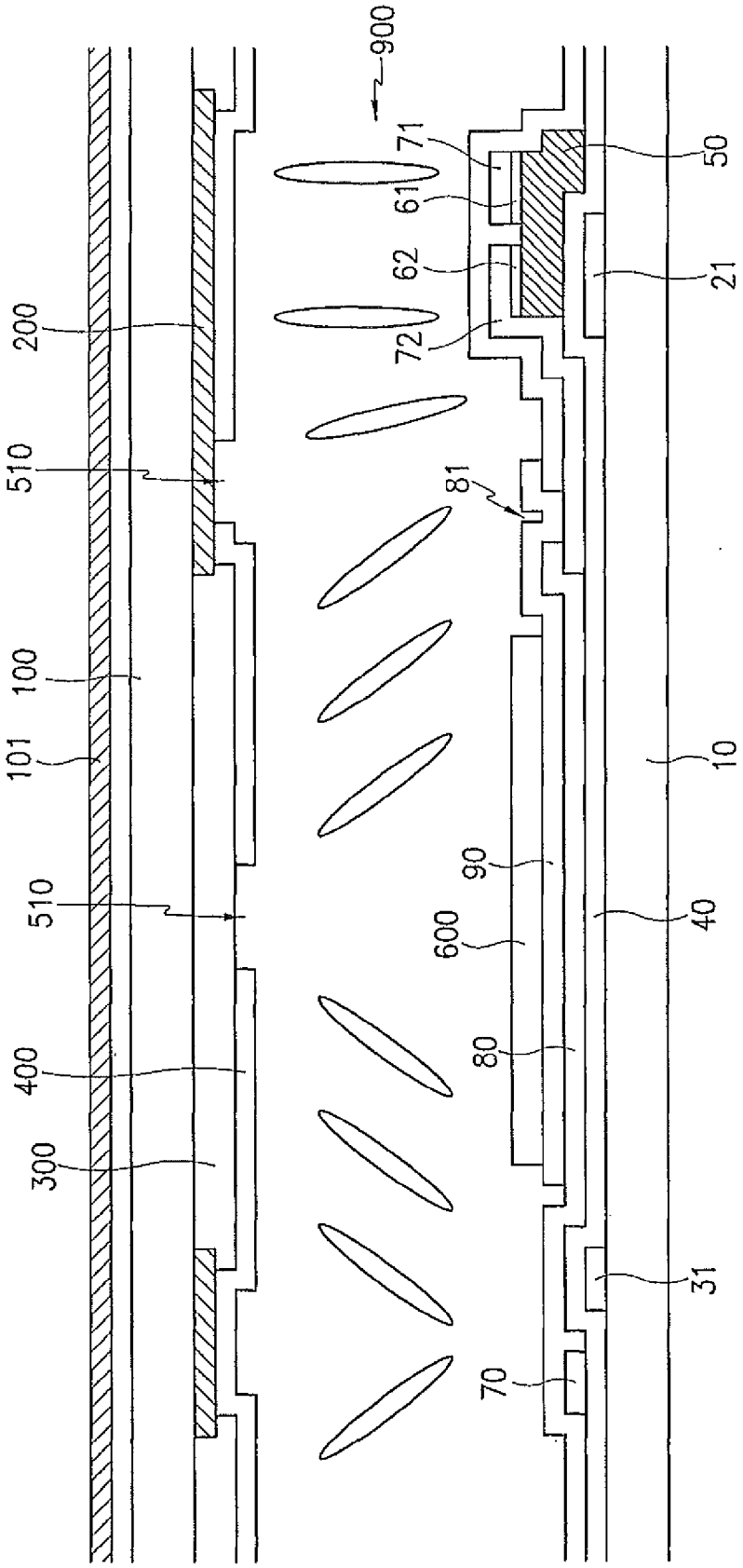

900
71
61
62
72
50
21
200
510
81
100
101
10
510
90
600
40
400
80
300
31
70

FIG.8

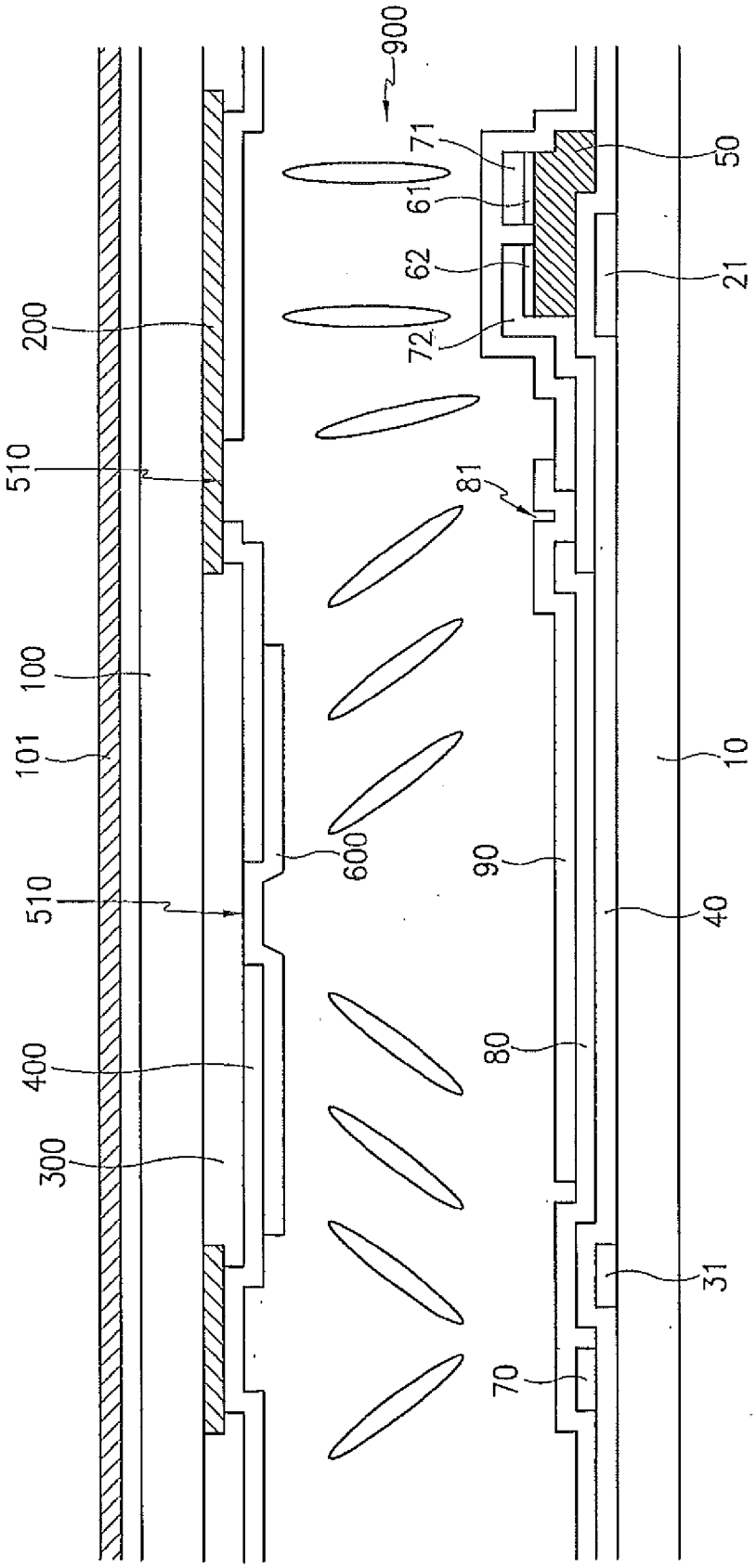

900
71
61
62
72
50
21
200
510
81
100
101
10
600
90
510
40
400
80
300
31
70

FIG.9

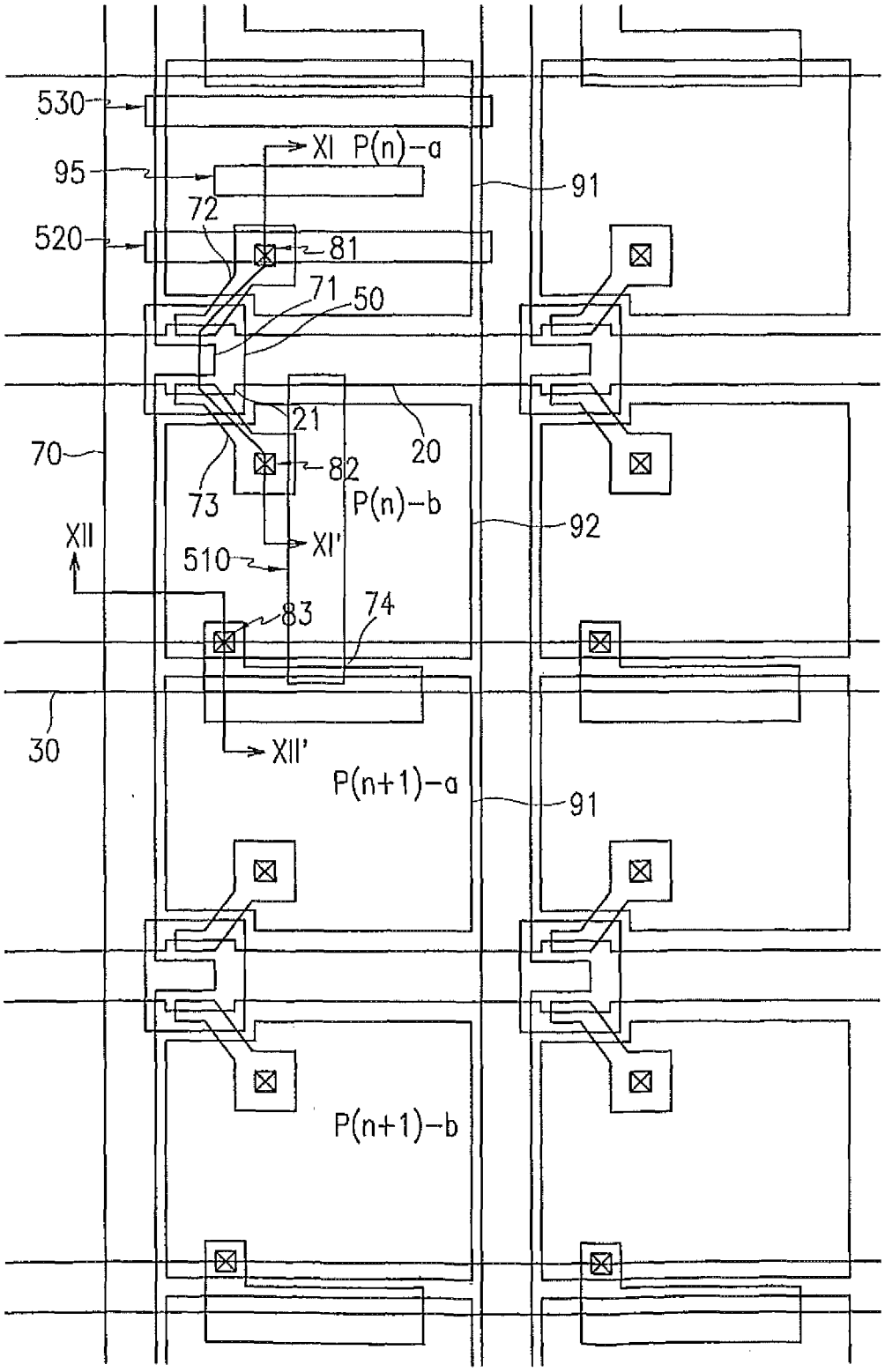

530
95
520
72
81
71
50
21
20
70
82
73
P(n)-b
92
XII
XI'
510
83
74
30
XII'
P(n+1)-a
91
P(n+1)-b
XI
P(n)-a
91

FIG.10

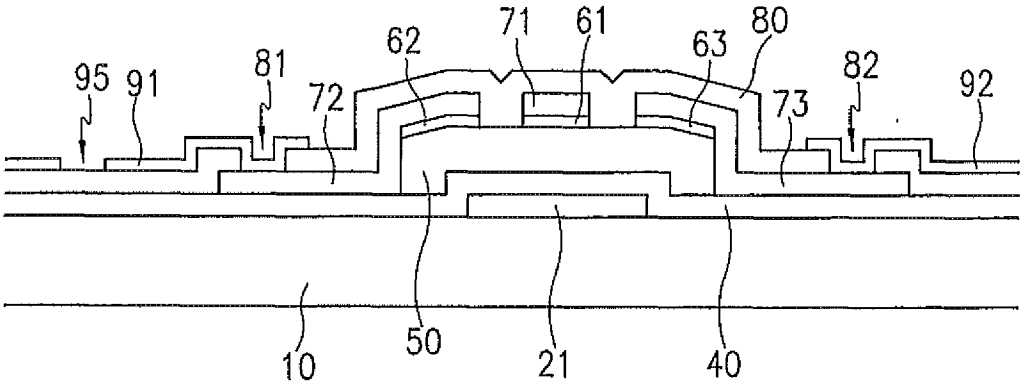

95
91
81
72
62
71
61
63
80
82
73
92
10
50
21
40

FIG.11

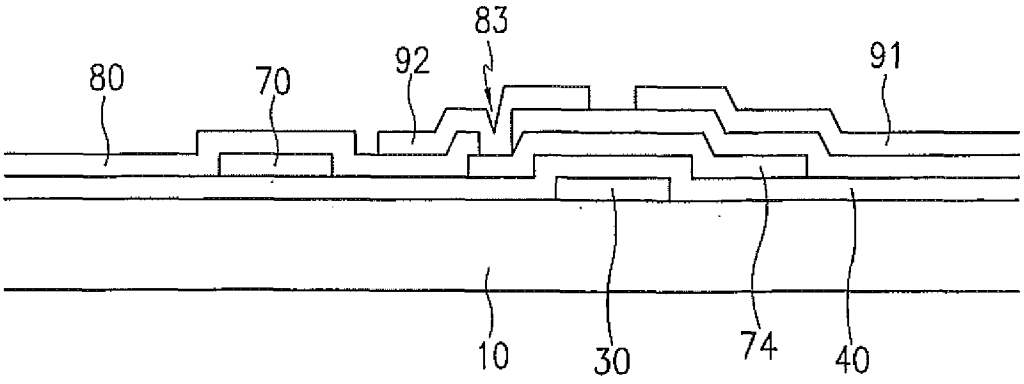

80
70
92
83
91
10
30
74
40

FIG.12

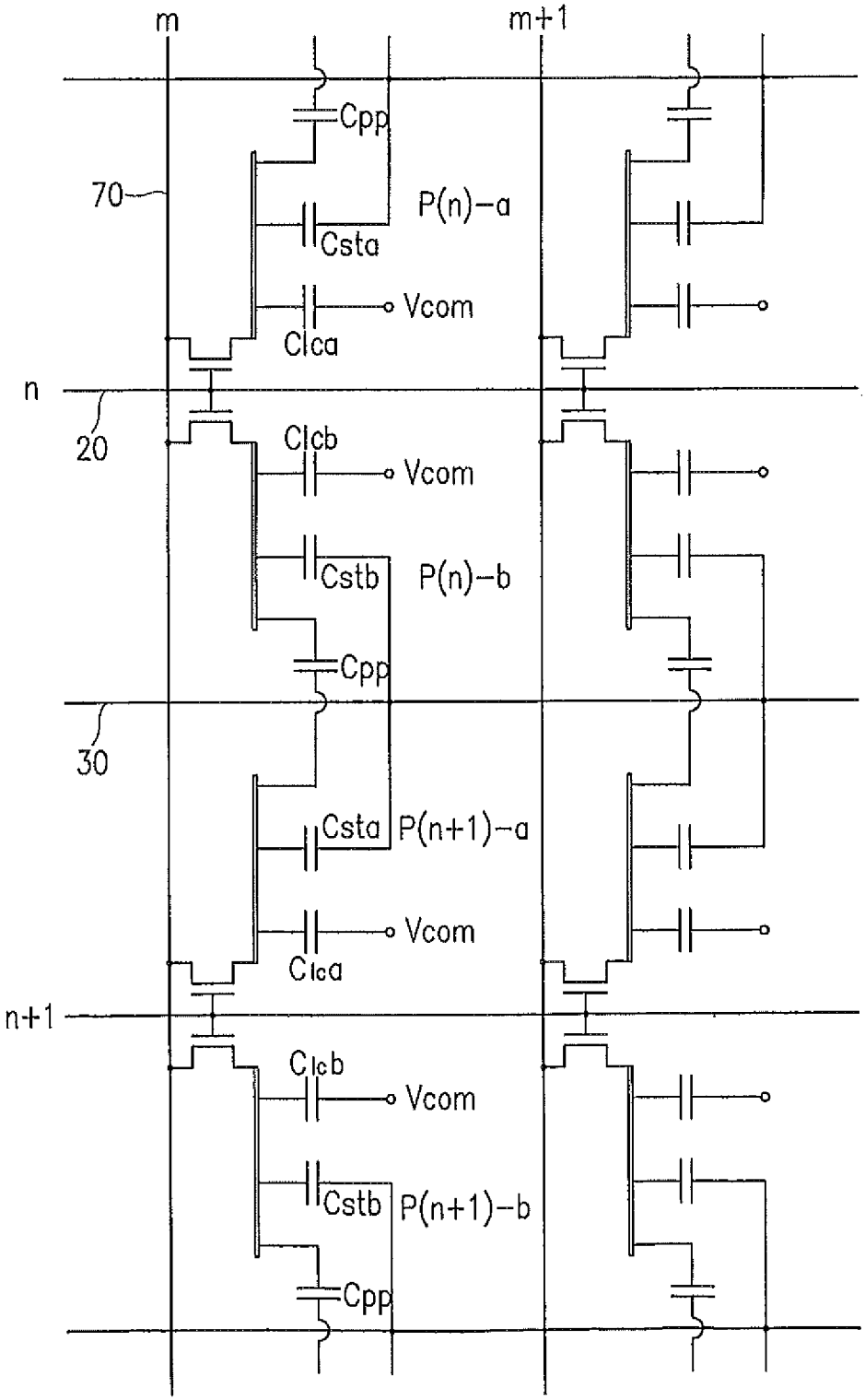

m
m+1
Cpp
70
P(n)-a
Csta
Vcom
Clca
n
20
Clcb
Vcom
Cstb
P(n)-b
Cpp
30
Csta
P(n+1)-a
Vcom
Clca
n+1
Clcb
Vcom
Cstb
P(n+1)-b
Cpp

FIG.13

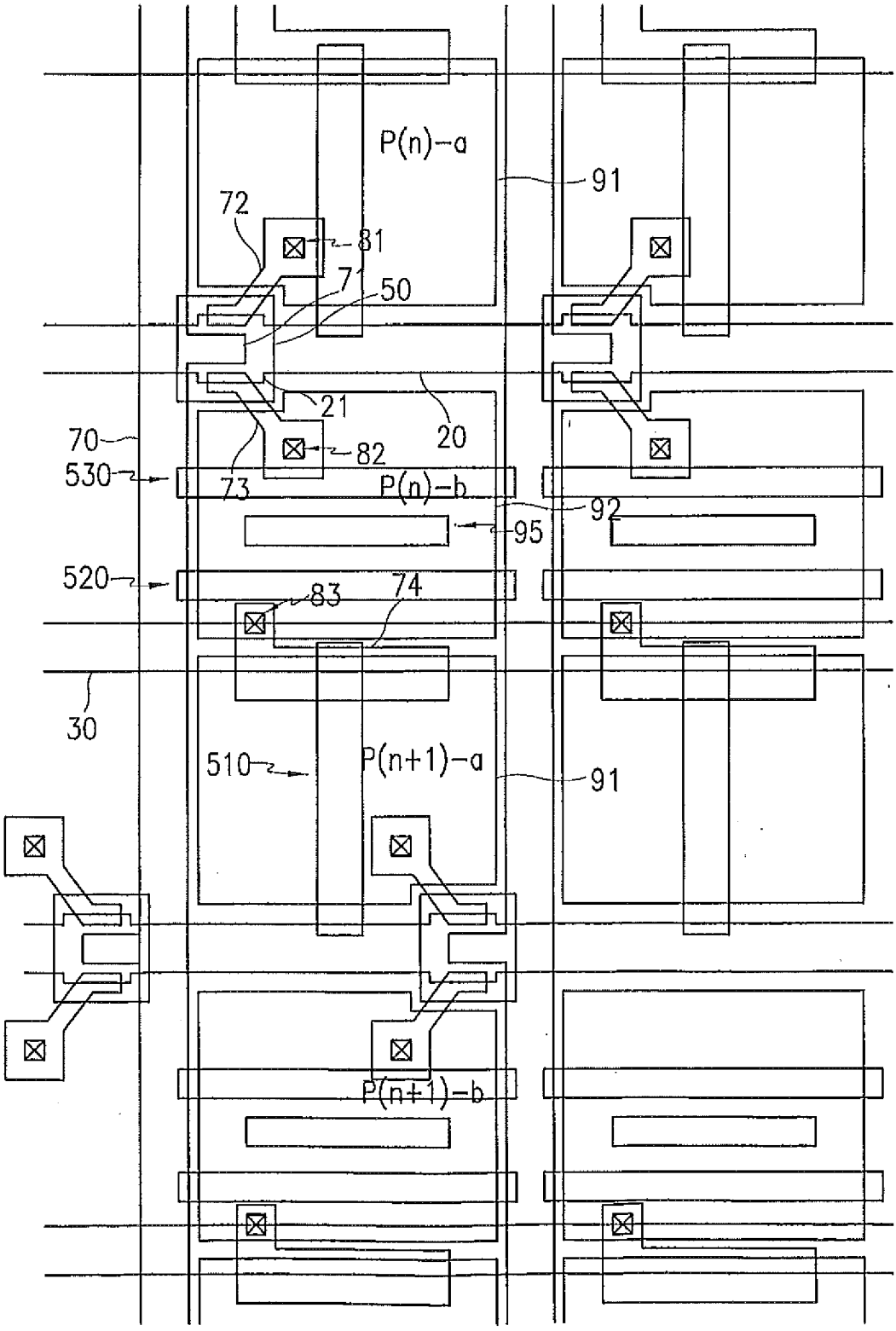
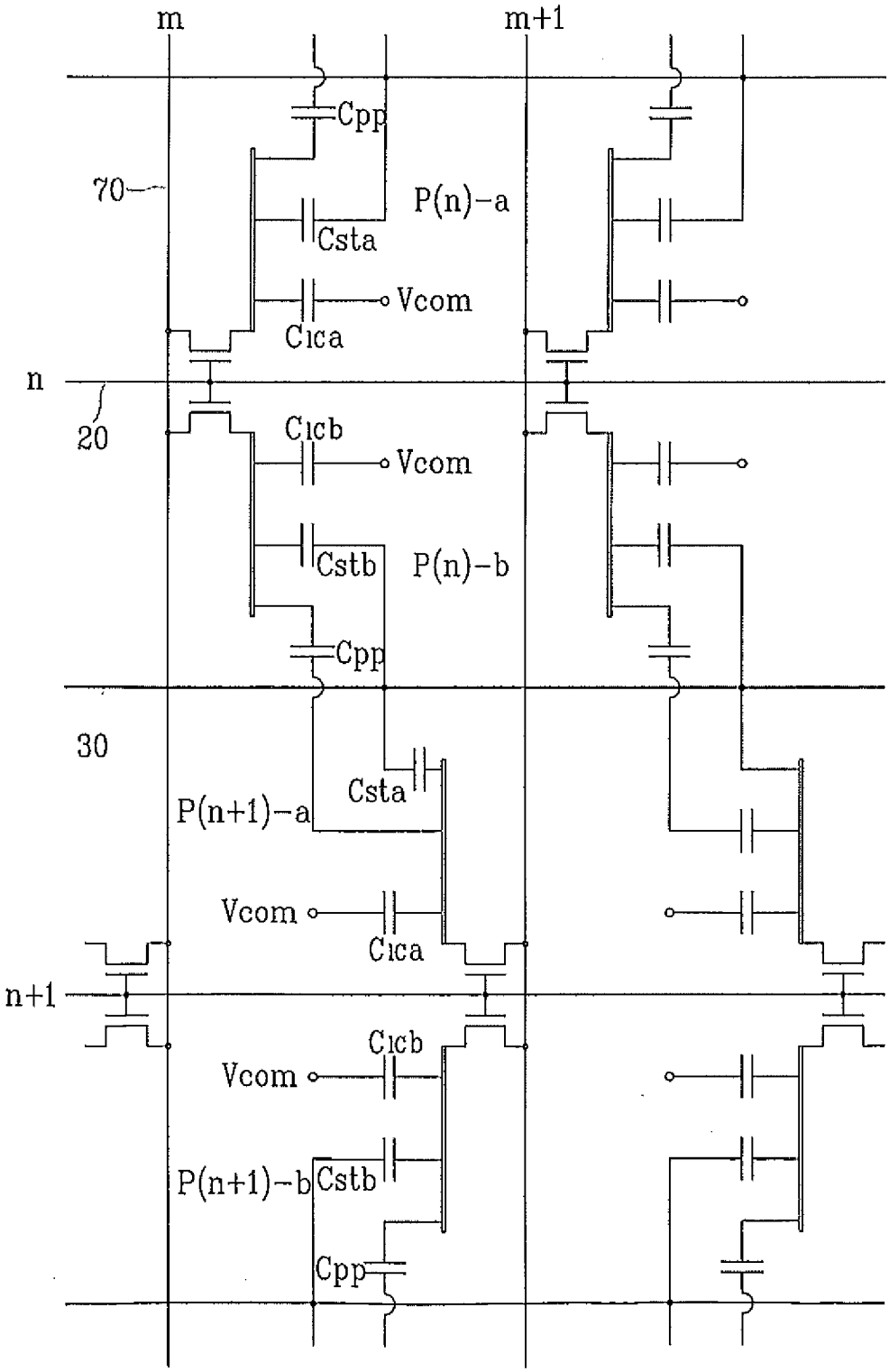

P(n)-a
91
72
81
71
50
21
20
70
82
530
73
P(n)-b
92
95
520
83
74
30
510
P(n+1)-a
91
P(n+1)-b

FIG.14


m
m+1
Cpp
70
P(n)-a
Csta
Vcom
Clca
n
20
Clcb
Vcom
Cstb
P(n)-b
Cpp
30
Csta
P(n+1)-a
Vcom
Clca
n+1
Clcb
Vcom
P(n+1)-b
Cstb
Cpp

专利名称(译)	在有源液晶显示器中的微域分区		
公开(公告)号	EP2241930A2	公开(公告)日	2010-10-20
申请号	EP2010168932	申请日	2002-06-11
[标]申请(专利权)人(译)	三星电子株式会社		
申请(专利权)人(译)	SAMSUNG ELECTRONICS CO.，LTD.		
当前申请(专利权)人(译)	SAMSUNG ELECTRONICS CO.，LTD.		
[标]发明人	SONG JANG KUN		
发明人	SONG, JANG-KUN		
IPC分类号	G02F1/1333 G09G3/36 G02F1/1337 G02F1/133 G02F1/1343 G02F1/1362 G02F1/1368 G02F1/137 G02F1/139		
CPC分类号	G02F1/133707 G02F1/133753 G02F1/136213 G02F1/1393 G02F2001/133746 G02F2001/134345 G02F2001/13712		
优先权	1020010072885 2001-11-22 KR		
其他公开文献	EP2241930A3		
外部链接	Espacenet		

摘要(译)

在第一绝缘基板（10）上形成带有多个狭缝的像素电极（90）。公共电极（400）形成在具有多个开口部分（510,520,530）和黑色矩阵（200）以及滤色器（300）的第二绝缘基板（100）上。像素电极的水平开口部分和公共电极（510,520,530）的开口部分将像素区域划分为左，右，上和下域。液晶材料（900）介于第一和第二绝缘基板之间。源电极和漏电极（71,72）形成在欧姆接触层（61,62）上，欧姆接触层（61,62）形成在半导体层（50）上，半导体层（50）形成在栅电极（20）上方的栅极绝缘层（40）上。某些像素电极（90）可以相对于彼此进行电容器连接。

FIG.2