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(54) **Display device, liquid crystal display device and electronic device including the same**

Anzeigevorrichtung, Flüssigkristallanzeigevorrichtung und elektronisches Gerät, das diese beinhaltet
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Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] One embodiment of this invention relates to a display device or a driving method of the display device. In specific, one embodiment of this invention relates to a liquid crystal display device in which a pixel is divided into a plurality of subpixels and a driving method of the liquid crystal display device. Further, one embodiment of this invention relates to a liquid crystal display device or an electronic device including the liquid crystal display device in a display portion.

2. Description of the Related Art

[0002] Liquid crystal display devices are used for a variety of electronic products such as cell phones and television receiver and many research is conducted for further improvement in the quality.

[0003] While advantages of a liquid crystal display device are small size, light weight, and low power consumption compared to a CRT (cathode-ray tube) and, a problem of the liquid crystal display device is the narrow viewing angle. In recent years, many research about a multi domain method, that is, an alignment division method are made for improving viewing angle characteristics. For example, an MVA (multi-domain vertical alignment) mode which is a combination of a VA (vertical alignment) mode and a multi-domain mode, a PVA (patterned vertical alignment) mode, and the like can be given.

[0004] In addition, researches are made in which one pixel is divided into a plurality of subpixels and the alignment state of liquid crystals in each subpixel is made different so as to improve the viewing angle. However, since the pixel is divided into the plurality of subpixels, a plurality of signals needs to be input to one pixel. Therefore, the number of signals needed for driving a display device is increased. In view of this, research on conversion of a signal for one pixel into signals for respective subpixels is conducted (see Reference 1).

[0005] Reference 1: Japanese Published Patent Application No. 2007-226196

[0006] US 2007/0070008 is concerned with a liquid crystal display panel with improved visibility and transmittance in a multi-domain VA mode. The reference Sang Soo Kim: "66.1: Invited Paper: The World's Largest (82-in.) TFT-LCD", 2005 SID International Symposium, is concerned with a full high definition (1920 x 1080) 82" TFT-LCD panel using Super-PVA technology. US 2003/0011553 is concerned with voltage patterns to drive liquid crystals according to gradation data. The reference Itakura et al.: "A 402-Output TFT-LCD Driver IC With Power Control Based on the Number of Colors Selected", IEEE Journal of Solid-State Circuits, Vol. 38, No. 3, March 2003, is concerned with a TFT-LCD driver integrated cir-

cuit with power control based on the number of colors to be displayed. US 2002/0186230 is concerned with an arrangement for adjusting the gradient and amplitude of the gray scale number-gray scale voltage characteristic of a display device. US 2006/0279498 is concerned with a display signal processing device including a reference gradation voltage circuit and a D/A converting circuit.

SUMMARY OF THE INVENTION

[0007] However, in a display device disclosed in Reference 1, signals corresponding to respective subpixels are generated outside a panel. Therefore, when the pixel is divided into a plurality of subpixels, the number of connection between the panel and an external component is largely increased. As a result, poor connection is generated in a connection portion between the panel and the external component, whereby a problem of decrease in reliability is concerned. Alternatively, an yield in production of the display device is decreased, whereby a problem of an increase in a cost is concerned. Alternatively, the number of connection between the panel and the external component is increased, whereby a problem in that it is difficult to obtain a high-definition display device is concerned.

[0008] Alternatively, in order to generate signals corresponding to respective subpixels, a look-up table is used in some cases. Accordingly, a problem in that it is difficult to form a part for generating the signals corresponding to the respective subpixels and the pixel over the same substrate is concerned.

[0009] Alternatively, in order to read the signals corresponding to the respective subpixels from a memory element in which the look-up table is stored, the memory element needs to be driven at high speed. Therefore, as the look-up table is read from the memory element, heat is generated, whereby power consumption is increased in some cases. Alternatively, since the memory element for storing the look-up table is needed, a cost is increased. Alternatively, a pathway from generating the signals corresponding to the respective subpixels to writing the signals to the respective subpixel is long, and a connection portion of the panel and the external component exists in the course of the pathway. Therefore, the signals are likely to be influenced by noise and display quality is decreased, which is a problem.

[0010] In view of the foregoing problems, one object is to convert one digital signal into a plurality of analog signals without using a look-up table. Alternatively, another object is to reduce the number of connection between a panel and an external component. Alternatively, another object is to increase reliability. Alternatively, another object is to improve an yield. Alternatively, another object is to reduce a cost. Alternatively, another object is to make a high-definition display portion. Alternatively, another object is to try to achieve a low price. Alternatively, another object is to make heat less likely to be generated. Alternatively, another object is to reduce power con-

sumption. Alternatively, another object is to increase display quality by enhancing resistance to noise. Besides, another object is to provide a better display device or semiconductor device by using a variety of other means.

[0011] The invention provides a display device according to claims 1 or 2.

[0012] Note that various types of switches can be used as a switch. An electrical switch, a mechanical switch, and the like are given as examples. That is, any element can be used as long as it can control current flow, without limitations to a certain element. For example, a transistor (e.g., a bipolar transistor or a MOS transistor), a diode (e.g., a PN diode, a PIN diode, a Schottky diode, an MIM (metal insulator metal) diode, an MIS (metal insulator semiconductor) diode, or a diode-connected transistor), or the like can be used as a switch. Alternatively, a logic circuit combining such elements can be used as a switch.

[0013] An example of a mechanical switch is a switch formed using MEMS (micro electro mechanical system) technology, such as a digital micromirror device (DMD). Such a switch includes an electrode which can be moved mechanically, and operates by controlling conduction and non-conduction based on movement of the electrode.

[0014] Note that a CMOS switch may be used as a switch by using both N-channel and P-channel transistors.

[0015] Note that when a transistor is used as a switch, the switch includes an input terminal (one of a source terminal and a drain terminal), an output terminal (the other of the source terminal and the drain terminal), and a terminal for controlling conduction (a gate terminal). On the other hand, when a diode is used as a switch, the switch does not have a terminal for controlling conduction in some cases. Therefore, when a diode is used as a switch, the number of wirings for controlling terminals can be further reduced compared to the case of using a transistor as a switch.

[0016] Note that when it is explicitly described that "A and B are connected," the case where A and B are electrically connected, the case where A and B are functionally connected, and the case where A and B are directly connected are included therein. Here, each of A and B corresponds to an object (e.g., a device, an element, a circuit, a wiring, an electrode, a terminal, a conductive film, or a layer). Accordingly, another connection relation shown in drawings and texts is included without being limited to a predetermined connection relation, for example, the connection relation shown in the drawings and the texts.

[0017] For example, in the case where A and B are electrically connected, one or more elements which enable electric connection between A and B (e.g., a switch, a transistor, a capacitor, an inductor, a resistor, and/or a diode) may be connected between A and B. Alternatively, in the case where A and B are functionally connected, one or more circuits which enable functional connection between A and B (e.g., a logic circuit such as an inverter,

a NAND circuit, or a NOR circuit; a signal converter circuit such as a DA converter circuit, an AD converter circuit, or a gamma correction circuit; a potential level converter circuit such as a power supply circuit (e.g., a step-up dc-dc converter or a step-down dc-dc converter) or a level shifter circuit for changing a potential level of a signal; a voltage source; a current source; a switching circuit; an amplifier circuit such as a circuit which can increase signal amplitude, the amount of current, or the like, an operational amplifier, a differential amplifier circuit, a source follower circuit, or a buffer circuit; a signal generating circuit; a memory circuit; and/or a control circuit) may be connected between A and B. For example, in the case where a signal output from A is transmitted to B even if another circuit is provided between A and B, A and B are connected functionally.

[0018] Note that when it is explicitly described that "A and B are electrically connected", the case where A and B are electrically connected (i.e., the case where A and B are connected by interposing another element or another circuit therebetween), the case where A and B are functionally connected (i.e., the case where A and B are functionally connected by interposing another circuit therebetween), and the case where A and B are directly connected (i.e., the case where A and B are connected without interposing another element or another circuit therebetween) are included therein. That is, when it is explicitly described that "A and B are electrically connected", the description is the same as the case where it is explicitly only described that "A and B are connected".

[0019] Note that a display element, a display device which is a device having a display element, a light-emitting element, and a light-emitting device which is a device having a light-emitting element can use various types and can include various elements. For example, a display medium, whose contrast, luminance, reflectivity, transmittivity, or the like changes by an electromagnetic action, such as an EL (electro-luminescence) element (e.g., an EL element including organic and inorganic materials, an organic EL element, or an inorganic EL element), an LED (a white LED, a red LED, a green LED, a blue LED, or the like), a transistor (a transistor which emits light depending on current), an electron emitter, a liquid crystal element, electronic ink, an electrophoresis element, a grating light valve (GLV), a plasma display panel (PDP), a digital micromirror device (DMD), a piezoelectric ceramic display, or a carbon nanotube can be included as a display element, a display device, a light-emitting element, or a light-emitting device. Note that display devices using an EL element include an EL display; display devices using an electron emitter include a field emission display (FED), an SED-type flat panel display (SED: surface-conduction electron-emitter display), and the like; display devices using a liquid crystal element include a liquid crystal display (e.g., a transmissive liquid crystal display, a transflective liquid crystal display, a reflective liquid crystal display, a direct-view liquid crystal display, or a projection liquid crystal display); and display devices

using electronic ink or an electrophoresis element include electronic paper.

[0020] Note that a liquid crystal element is an element which controls transmission or non-transmission of light by an optical modulation action of liquid crystals and includes a pair of electrodes and liquid crystals. The optical modulation action of liquid crystals is controlled by an electric field applied to the liquid crystal (including a lateral electric field, a vertical electric field and a diagonal electric field). The following liquid crystals can be used for a liquid crystal element: a nematic liquid crystal, a cholesteric liquid crystal, a smectic liquid crystal, a discotic liquid crystal, a thermotropic liquid crystal, a lyotropic liquid crystal, a low molecular liquid crystal, a high molecular liquid crystal, a PDLC (polymer dispersed liquid crystal), a ferroelectric liquid crystal, an anti-ferroelectric liquid crystal, a main chain type liquid crystal, a side chain type polymer liquid crystal, a plasma addressed liquid crystal (PALC), a banana-shaped liquid crystal, a TN (twisted nematic) mode, an STN (super twisted nematic) mode, an IPS (in-plane-switching) mode, an FFS (fringe field switching) mode, an MVA (multi-domain vertical alignment) mode, a PVA (patterned vertical alignment) mode, an ASV (advanced super view) mode, an ASM (axially symmetric aligned microcell) mode, an OCB (optical compensated birefringence) mode, an ECB (electrically controlled birefringence) mode, an FLC (ferroelectric liquid crystal) mode, an AFLC (anti-ferroelectric liquid crystal) mode, a PDLC (polymer dispersed liquid crystal) mode, a guest-host mode, and a blue-phase mode. Note that this invention is not limited thereto, and various kinds of liquid crystal elements can be used.

[0021] Note that various types of transistors can be used as a transistor, without being limited to a certain type. For example, a thin film transistor (TFT) including a non-single-crystal semiconductor film typified by amorphous silicon, polycrystalline silicon, microcrystalline (also referred to as microcrystal, nanocrystal, semi-amorphous) silicon, or the like can be used. In the case of using the TFT, there are various advantages. For example, since the TFT can be formed at temperature lower than that of the case of using single crystal silicon, manufacturing cost can be reduced or a manufacturing apparatus can be made larger. Since the manufacturing apparatus is made larger, the TFT can be formed using a large substrate. Therefore, many display devices can be formed at the same time at low cost. In addition, a substrate having low heat resistance can be used because of low manufacturing temperature. Therefore, the transistor can be formed using a light-transmitting substrate. Accordingly, transmission of light in a display element can be controlled by using the transistor formed using the light-transmitting substrate. Alternatively, part of a film which forms the transistor can transmit light because the film thickness of the transistor is thin. Therefore, the aperture ratio can be improved.

[0022] Note that when a catalyst (e.g., nickel) is used in forming polycrystalline silicon, crystallinity can be fur-

ther improved and a transistor having excellent electric characteristics can be formed.

[0023] Note that when a catalyst (e.g., nickel) is used in the case of forming microcrystalline silicon, crystallinity can be further improved and a transistor having excellent electric characteristics can be formed. At this time, crystallinity can be improved by just performing heat treatment without performing laser light irradiation.

[0024] Note that polycrystalline silicon and microcrystalline silicon can be formed without using a catalyst (e.g., nickel).

[0025] Note that it is preferable that the crystallinity of silicon be improved to polycrystalline, microcrystalline, or the like in the whole panel; however, this invention is not limited to this. The crystallinity of silicon may be improved only in part of the panel. Selective increase in crystallinity can be achieved by selective laser irradiation or the like. For example, only a peripheral driver circuit region excluding pixels may be irradiated with laser light. Alternatively, only a region of a gate driver circuit, a source driver circuit, or the like may be irradiated with laser light. Further alternatively, only part of a source driver circuit (e.g., an analog switch) may be irradiated with laser light.

[0026] Alternatively, a transistor can be formed by using a semiconductor substrate, an SOI substrate, or the like.

[0027] Alternatively, a transistor including a compound semiconductor or an oxide semiconductor such as ZnO, a-InGaZnO, SiGe, GaAs, IZO, ITO, or SnO, a thin film transistor obtained by thinning such a compound semiconductor or an oxide semiconductor, or the like can be used. Note that such a compound semiconductor or an oxide semiconductor can be used for not only a channel portion of the transistor but also other applications. For example, such a compound semiconductor or an oxide semiconductor can be used as a resistor element, a pixel electrode, or a light-transmitting electrode.

[0028] Alternatively, a transistor formed by using an inkjet method or a printing method, or the like can be used.

[0029] Alternatively, a transistor including an organic semiconductor or a carbon nanotube, or the like can be used.

[0030] In addition, various types of transistors can be used. For example, a MOS transistor, a junction transistor, a bipolar transistor, or the like can be employed.

[0031] Further, a MOS transistor, a bipolar transistor and/or the like may be mixed on one substrate.

[0032] Furthermore, various transistors other than the above-described types of transistors can be used.

[0033] Note that a transistor can be formed using various types of substrates without being limited to a certain type. As the substrate, for example, a single crystal substrate, an SOI substrate, a glass substrate, a quartz substrate, a plastic substrate, a stainless steel substrate, a substrate including a stainless steel foil, or the like can be used.

[0034] Note that a structure of a transistor can be various forms without being limited to a certain structure. For example, a multi-gate structure having two or more gate electrodes may be used. When the multi-gate structure is used, a structure where a plurality of transistors are connected in series is provided because channel regions are connected in series.

[0035] As another example, a structure where gate electrodes are formed above and below a channel may be employed.

[0036] A structure where a gate electrode is formed above a channel region, a structure where a gate electrode is formed below a channel region, a staggered structure, an inverted staggered structure, a structure where a channel region is divided into a plurality of regions, or a structure where channel regions are connected in parallel or in series can be used. Further alternatively, a source electrode or a drain electrode may overlap with a channel region (or part of it).

[0037] Note that various types of transistors can be used as a transistor and the transistor can be formed using various types of substrates. Accordingly, all the circuits that are necessary to realize a predetermined function can be formed using the same substrate. For example, all the circuits that are necessary to realize the predetermined function can be formed using a glass substrate, a plastic substrate, a single crystal substrate, an SOI substrate, or any other substrate. When all the circuits that are necessary to realize the predetermined function are formed using the same substrate, cost can be reduced by reduction in the number of component parts or reliability can be improved by reduction in the number of connection to circuit components. Alternatively, part of the circuits which are necessary to realize the predetermined function can be formed using one substrate and another part of the circuits which are necessary to realize the predetermined function can be formed using another substrate. That is, not all the circuits that are necessary to realize the predetermined function are required to be formed using the same substrate. For example, part of the circuits which are necessary to realize the predetermined function may be formed by transistors using a glass substrate and another part of the circuits which are necessary to realize the predetermined function may be formed using a single crystal substrate, so that an IC chip formed by a transistor over the single crystal substrate can be connected to the glass substrate by COG (chip on glass) and the IC chip may be provided over the glass substrate. Alternatively, the IC chip can be connected to the glass substrate by TAB (tape automated bonding) or a printed wiring board. When part of the circuits are formed using the same substrate in this manner, cost can be reduced by reduction in the number of component parts or reliability can be improved by reduction in the number of connection to circuit components. Further alternatively, when circuits with high driving voltage and high driving frequency, which consume large power, are formed, for example, over a single crys-

tal semiconductor substrate instead of forming such circuits using the same substrate and an IC chip formed by the circuit is used, increase in power consumption can be prevented.

[0038] Note that a transistor is an element having at least three terminals of a gate, a drain, and a source. The transistor has a channel region between a drain region and a source region, and current can flow through the drain region, the channel region, and the source region. Here, since the source and the drain of the transistor change depending on the structure, the operating condition, and the like of the transistor, it is difficult to define which is source or drain. Therefore, a region functioning as source and drain is not called the source or the drain in some cases. In such a case, one of the source and the drain may be referred to as a first terminal and the other thereof may be referred to as a second terminal, for example. Alternatively, one of the source and the drain may be referred to as a first electrode and the other thereof may be referred to as a second electrode. Further alternatively, one of the source and the drain may be referred to as a first region and the other thereof may be called a second region.

[0039] Note that a transistor may be an element including at least three terminals of a base, an emitter and a collector. In this case also, the emitter and the collector may be similarly denoted as a first terminal and a second terminal.

[0040] Note that a semiconductor device corresponds to a device having a circuit including a semiconductor element (e.g., a transistor, a diode, or a thyristor). The semiconductor device may also include all devices that can function by utilizing semiconductor characteristics. Alternatively, the semiconductor device corresponds to a device having a semiconductor material.

[0041] Note that a display device corresponds to a device having a display element. The display device may include a plurality of pixels each having a display element. Note that the display device may also include a peripheral driver circuit for driving the plurality of pixels. The peripheral driver circuit for driving the plurality of pixels may be formed over the same substrate as the plurality of pixels. The display device may also include a peripheral driver circuit provided over a substrate by wire bonding or bump bonding, namely, an IC chip connected by chip on glass (COG) or an IC chip connected by TAB or the like. Further, the display device may also include a flexible printed circuit (FPC) to which an IC chip, a resistor, a capacitor, an inductor, a transistor, or the like is attached. Note also that the display device includes a printed wiring board (PWB) which is connected through a flexible printed circuit (FPC) and to which an IC chip, a resistor element, a capacitor element, an inductor, a transistor, or the like is attached. The display device may also include an optical sheet such as a polarizing plate or a retardation plate. Note that the display device may also include a lighting device, a housing, an audio input and output device, a light sensor, or the like.

[0042] Note that a lighting device may include a back-light unit, a light guide plate, a prism sheet, a diffusion sheet, a reflective sheet, a light source (e.g., an LED or a cold cathode fluorescent lamp), a cooling device (e.g., a water cooling device or an air cooling device), or the like.

[0043] In addition, a light-emitting device corresponds to a device having a light-emitting element or the like. When a light-emitting element is used as a display element, a light-emitting device is a typical example of a display device.

[0044] Note that a reflective device corresponds to a device having a light-reflecting element, a light-diffraction element, a light-reflecting electrode, or the like.

[0045] A liquid crystal display device corresponds to a display device including a liquid crystal element. Liquid crystal display devices include a direct-view liquid crystal display, a projection liquid crystal display, a transmissive liquid crystal display, a reflective liquid crystal display, a semi-transmissive liquid crystal display, and the like.

[0046] Note also that a driving device corresponds to a device having a semiconductor element, an electric circuit, an electronic circuit and/or the like. For example, a transistor which controls input of a signal from a source signal line to a pixel (also called a selection transistor, a switching transistor, or the like), a transistor which applies voltage or current to a pixel electrode, a transistor which applies voltage or current to a light-emitting element, and the like are examples of the driving device. A circuit which supplies a signal to a gate signal line (also called a gate driver, a gate line driver circuit, or the like), a circuit which supplies a signal to a source signal line (also called a source driver, a source line driver circuit, or the like) are also examples of the driving device.

[0047] Note that a display device, a semiconductor device, a lighting device, a cooling device, a light-emitting device, a reflective device, a driving device, and the like are provided together in some cases. For example, a display device includes a semiconductor device and a light-emitting device in some cases. Alternatively, a semiconductor device includes a display device and a driving device in some cases.

[0048] According to one embodiment of this invention, since one digital signal can be converted into a plurality of analog signals, a look-up table can be unnecessary. Therefore, heat generation or an increase in power consumption due to reading a look-up table from a memory element can be prevented. Alternatively, since signals corresponding to respective subpixels can be generated on a panel, the number of connection between the panel and an external component can be small. Alternatively, poor connection in the connection portion of the panel and the external component can be suppressed, whereby reliability can be increased. Alternatively, an yield in production of a display device can be increased. Alternatively, a production cost of the display device can be reduced. Alternatively, since the number of connection between the panel and the external component can be reduced, a high-definition display portion can be ob-

tained. Alternatively, since the number of connection between the panel and the external component can be reduced, resistance to noise can be enhanced and display quality can be increased.

BRIEF DESCRIPTION OF THE DRAWINGS

[0049] In the accompanying drawings:

10 FIGS. 1A to 1C are diagrams illustrating a circuit of a converter portion;

FIGS. 2A and 2B are diagrams illustrating a circuit of a converter portion;

15 FIG 3 is a diagram illustrating a circuit of a converter portion;

FIGS. 4A and 4B are diagrams illustrating a circuit of a converter portion;

20 FIGS. 5A and 5B are diagrams illustrating a circuit of a converter portion;

25 FIGS. 6A and 6B are diagrams illustrating a circuit of a converter portion;

FIG 7 is a diagram illustrating a circuit of a converter portion;

30 FIGS. 8A to 8C are diagrams illustrating a circuit of a converter portion;

35 FIGS. 9A to 9C are diagrams illustrating a circuit of a display device;

FIGS. 10A and 10B are diagrams illustrating a circuit of a display device;

40 FIGS. 11A and 11B are diagrams illustrating a circuit and a driving method of a display device;

45 FIGS. 12A and 12B are diagrams illustrating a circuit of a signal line device;

FIG 13 is a cross-sectional view illustrating a transistor;

50 FIGS. 14A to 14E are cross-sectional views illustrating a transistor;

FIGS. 15A to 15H are diagrams each illustrating an electronic device, and

55 FIGS. 16A to 16H are diagrams each illustrating an electronic device.

DETAILED DESCRIPTION OF THE INVENTION

[0050] Hereinafter, embodiments will be described with reference to drawings. However, it is easily understood by those skilled in the art that the invention can be implemented with a variety of different forms, and embodiments and details of this invention can be variously changed without departing from the scope of this invention. Therefore, this invention is not interpreted as being limited to the description of the embodiments below. Note that in a structure of this invention described below, common portions and portions having a similar function are denoted by the same reference numerals in all diagrams, and description thereof is omitted.

[0051] Hereinafter, embodiment modes will be described with reference to a variety of drawings. In that case, in one embodiment, the contents (or may be part of the contents) described in each drawing can be freely applied to, combined with, or replaced with the contents (or may be part of the contents) described in another drawing. Further, even more drawings can be formed when each part in a drawing described in one embodiment is combined with another part in the drawing.

[0052] Similarly, the contents (or may be part of the contents) described in each drawing of embodiment or a plurality of embodiments can be freely applied to, combined with, or replaced with the contents (or may be part of the contents) described in a drawing of another embodiment or a plurality of other embodiments. Further, even more drawings can be formed when each part in the drawing of embodiment or a plurality of embodiments is combined with part of another embodiment or a plurality of other embodiments.

[0053] Note that the contents (or may be part of the contents) described in one embodiment will show an example of an embodied case of other contents (or may be part of the contents) described in the embodiment, an example of slight transformation thereof, an example of partial modification thereof, an example of improvement thereof, an example of detailed description thereof, an application example thereof, an example of related part thereof, or the like. Therefore, the contents (or may be part of the contents) described in one embodiment can be freely applied to, combined with, or replaced with other contents (or may be part of the contents) described in the embodiment.

[0054] Note that the contents (or may be part of the contents) described in one embodiment or a plurality of embodiments will show an example of an embodied case of the contents (or may be part of the contents) described in the embodiment or the plurality of embodiments, an example of slight transformation thereof, an example of partial modification thereof, an example of improvement thereof, an example of detailed description thereof, an application example thereof, an example of related part thereof, or the like. Therefore, the contents (or may be part of the contents) described in another embodiment can be freely applied to, combined with, or replaced with

other contents (or may be part of the contents) described in another embodiment or a plurality of other embodiments.

5 (Embodiment 1)

[0055] In this embodiment, a digital-analog converter portion will be described. The digital-analog converter portion of this embodiment converts one digital signal (e.g., a digital signal with N bits (N is a natural number of 2 or more)) into n (n is a natural number of 2 or more) analog signals. In order to realize this, n groups (e.g., voltage groups or current groups) are input to the digital-analog converter portion.

10 **[0056]** Note that the values (e.g., voltage or current) of the n analog signals are different from each other. However, some of the n analog signals have the same value in some cases. Alternatively, all the values of the n analog signals are the same in some cases. For example, in the case of a digital signal with the maximum or minimum gray levels, the values of analog signals supplied to the respective subpixels are the same in some cases.

15 **[0057]** With reference to FIG 1A, the digital-analog converter portion in the case where one digital signal is converted into two analog signals is described, for example.

[0058] A digital-analog converter portion 100 is connected to a wiring group 111, a wiring group 112_1, a wiring group 112_2, a wiring 113_1 and a wiring 113_2.

20 **[0059]** The wiring group 111, the wiring group 112_1, and the wiring group 112_2 each include a plurality of wirings.

[0060] A digital signal is input to the wiring group 111. Therefore, the number of bits in the digital signal corresponds to the number of wirings in the wiring group 111 in many cases. For example, in the case where the digital signal has N bits, the wiring group 111 includes N wirings of wirings 111_1 to 111_ N (N is a natural number).

25 **[0061]** A first voltage group is input to the wiring group 112_1. Accordingly, the number of voltages in the first voltage group corresponds to the number of wirings of the wiring group 112_1 in many cases. For example, in the case where the number of voltages in the first wiring group is M , the wiring group 112_1 includes M wirings of wirings 112_11 to 112_1 M (M is a natural number of 2 or more). Therefore, the M different voltages are supplied to the M wirings in the wiring group 112_1. In addition, in some cases, the wiring group 112_1 is called a first wiring group depending on the number of wiring groups provided in the digital-analog converter portion 100.

30 **[0062]** Note that terms such as first, second, third to N th (N is a natural number) seen in this specification are used in order to avoid confusion between components and do not set a limitation on number.

35 **[0063]** A second voltage group is input to the wiring group 112_2. Accordingly, the number of voltages in the second voltage group corresponds to the number of wirings of the wiring group 112_2 in many cases. For ex-

ample, in the case where the number of voltages in the second voltage group is M , the wiring group 112_2 includes M wirings of wirings 112_21 to 112_2M. Therefore, the M different voltages are supplied to the M wirings in the wiring group 112_2. In addition, in some cases, the wiring group 112_2 is called a second wiring group depending on the number of wiring groups provided in the digital-analog converter portion 100.

[0064] Note that this embodiment is not limited to this. A variety of signals, voltages, or currents can be input to the wiring group 111, the wiring group 112_1, and the wiring group 112_2. Alternatively, a variety of signals, voltages, or currents can be output from the wiring group 111, the wiring group 112_1, and the wiring group 112_2.

[0065] A digital signal with N bits has a function of determining the value of an output signal from the digital-analog converter portion 100.

[0066] Note that the denotation "a digital signal with N bits" means a digital signal with N bits and also an inverted signal thereof (hereinafter also referred to as an inverted digital signal with N bits) in some cases.

[0067] Note that a digital signal with N bits or a signal with the approximately the same amplitude voltage as the digital signal with N bit is input to gate of a transistor in many cases. Further, the first voltage group and the second voltage group are input to one of source and drain of the transistor in many cases. Therefore, in order to make the transistor easily turned on or off, it is preferable that the amplitude voltage of the digital signal with N bits be equal to or greater than the difference between the minimum value and the maximum value of the first voltage group or the difference between the minimum value and the maximum value of the second voltage group, for example. However, this embodiment is not limited thereto and the amplitude voltage of the digital signal with N bits can be smaller.

[0068] The first voltage group has a plurality of voltages having different values from each other, and the second voltage group has a plurality of voltages having different values from each other in many cases. In addition, the values of the first voltage group and the second voltage group are different from each other in many cases. However, one of the voltages in the first voltage group and one of the voltages in the second voltage group or a plurality of voltages in the first voltage group and a plurality of voltages in the second voltage group have the same value in some cases. In this case, by sharing the wiring and using the wiring in common, the number of wirings in the wiring group 112_1 and the wiring group 112_2 can be reduced.

[0069] Note that a positive first voltage group and a negative first voltage group can be used as the first voltage group, and a positive second voltage group and a negative second voltage group can be used as the second voltage group. In order to achieve this, for example, the number of wirings in the wiring group 112_1 and the number of wirings in the wiring group 112_2 can be increased (for example, approximately twice). In this case,

the positive first voltage group and the negative first voltage group are input to the wiring group 112_1 at the same time and the positive second voltage group and the negative second voltage group are input to the wiring group 112_2 at the same time.

[0070] In another example, one operation period can include a first sub-operation period and a second sub-operation period. Then, positive polarity and negative polarity are switched to each other in each sub-operation period. Such a case is preferable because the number of wirings does not increase. For example, in the first sub-operation period, the positive first voltage group is input to the wiring group 112_1 and the positive second voltage group is input to the wiring group 112_2. In the second sub-operation period, the negative first voltage group is input to the wiring group 112_1 and the negative second voltage group is input to the wiring group 112_2.

[0071] Note that a positive voltage is a voltage which makes the potential of a pixel electrode higher than the potential of a common electrode (hereinafter such potential is referred to as a common potential) when the positive voltage is input to the pixel electrode in the liquid crystal display device. On the other hand, a negative voltage is a voltage which makes the potential of the pixel electrode lower than the common potential.

[0072] Note that in the case where a positive voltage and a negative voltage are input to the digital-analog converter portion 100 as the first voltage group and the second voltage group, inversion drive can be achieved by using the digital-analog converter portion 100 for a liquid crystal display device. In the inversion drive, the polarity of a voltage applied to the pixel electrode is inverted in accordance with the potential (the common potential) of the common electrode in a liquid crystal element in each frame or each pixel with respect to every certain period. By the inversion drive, uneven display such as flickering of an image and deterioration in a liquid crystal material can be suppressed. Note that as an example of the inversion drive, source line inversion drive, gate line inversion drive, dot inversion drive and the like can be given as well as frame inversion drive.

[0073] Note that respective values (or polarities) of the first voltage group and the second group can be changed with time. In such a case, one operation period includes a plurality of sub-operation periods. Then, the respective values (or polarities) of the first voltage group and the second voltage group are changed in every sub-operation period. In this manner, the number of voltages in the first voltage group and the second voltage group, that is, the number of wirings in the wiring group 112_1 and the wiring group 112_2 can be reduced.

[0074] Note that a current group can be input to the wiring group 112_1 and the wiring group 112_2. A pixel circuit, element, and the like which operates by current can be driven. Alternatively, the current group and the voltage group can be input to the wiring group 112_1 and the wiring group 112_2.

[0075] Note that, for example, the wiring group 111,

the wiring group 112_1, the wiring group 112_2, the wiring 113_1, and the wiring 113_2 can function as a first signal line group, a first power supply line group, a second power supply line group, a second signal line, and a third signal line, respectively.

[0076] Note that a variety of signals, voltages, or currents as well as the above-described signals and voltages can be input to the digital-analog converter portion 100.

[0077] For example, an inverted signal of the digital signal with N bits (hereinafter such a signal is referred to as an inverted digital signal) can be input to the digital-analog converter portion 100. In this case, a new wiring group (e.g., N wirings) may be added so that the inverted digital signal with N bits is input to the digital-analog converter portion 100 through the new wiring group. Note that this new wiring group functions as a signal line group, for example.

[0078] Note that the digital-analog converter portion 100 can be referred to as a circuit or a semiconductor device.

[0079] Next, the operation of the digital-analog converter portion 100 shown in FIG. 1A will be described.

[0080] The digital signal with N bits, the first voltage group, and the second voltage group are input to the digital-analog converter portion 100.

[0081] In accordance with the digital signal with N bits, the digital-analog converter portion 100 brings one of the wiring group 112_1 and the wiring 113_1 into conduction and brings the other of the wiring group 112_1 and the wiring 113_1 into out of conduction, so that the potentials of the one of the wiring group 112_1 and the wiring 113_1 are approximately the same. At the same time, in accordance with the digital signal with N bits, the digital-analog converter portion 100 brings one of the wiring group 112_2 and the wiring 113_2 into conduction and brings the other of the wiring group 112_2 and the wiring 113_2 into out of conduction, so that the potentials of the one of the wiring group 112_2 and the wiring 113_2 are approximately the same. In this manner, by the digital-analog converter portion 100, the potential of the wiring 113_1 and the potential of the wiring 113_2 are determined in accordance with the first voltage group and the second voltage group.

[0082] Note that the terms "approximately the same" are used in consideration of an error generated by the effect of noise. Accordingly, the error is preferably equal to or less than 10 %, more preferably equal to or less than 5 %, or further preferably equal to or less than 3 %, for example.

[0083] In this manner, the digital-analog converter portion 100 converts the digital signal with N bits into a first analog signal and a second analog signal and outputs the first analog signal and the second analog signal to the wiring 113_1 and the wiring 113_2, respectively. Alternatively, the digital-analog converter portion 100 selects one of the first voltage group and one of the second voltage group in accordance with the digital signal with

N bits, outputs the one of the first voltage group to the wiring 113_1 as the first analog signal, and outputs the one of the second voltage group to the wiring 113_2 as the second analog signal.

[0084] Note that the values of the first analog signal and the second analog signal are different from each other in many cases. However, this embodiment is not limited to this. Depending on the first voltage group and the second voltage group or the value of the digital signal, the values of the first analog signal and the second analog signal are approximately the same in some cases.

[0085] Note that although the potential of the first analog signal and the potential of the second analog signal are the same as that of one of the first voltage group or one of the second voltage group in many cases, this embodiment is not limited thereto. For example, a new voltage is generated by dividing any voltage in the first voltage group or the second voltage group with a resistor element or a capacitor element. Then, this newly generated voltage can be output as an analog signal.

[0086] Note that each of the wirings included in the wiring group 112_1 and the wiring group 112_2 preferably has a part whose width is larger than that of the wiring included in the wiring group 111. This is because an analog voltage is input to the wiring group 112_1 and the wiring group 112_2 in many cases and wiring resistance per unit length of the wiring group 112_1 and the wiring group 112_2 is preferably lower than that of the wiring group 111.

[0087] However, each of the wirings included in the wiring group 112_1 and the wiring group 112_2 may have a part whose width is smaller than that of the wiring included in the wiring group 111. In this case, for example, since each of the number of the wirings in the wiring group 112_1 and the number of wirings in the wiring group 112_2 is larger than that of the wiring group 111, the layout area of the digital-analog converter portion 100 can be small.

[0088] Note that it is preferable that each of the wiring 113_1 and the wiring 113_2 also has a part whose width is larger than that of the wiring included in the wiring group 111, like the wiring group 112_1 and the wiring group 112_2. However, each of the wiring 113_1 and the wiring 113_2 can have a part whose width is smaller than that of the wiring included in the wiring group 111, like the wiring group 112_1 and the wiring group 112_2.

[0089] Note that the wiring in the wiring group 111 is connected to a gate electrode of a transistor in many cases. Accordingly, part of the wiring included in the wiring group 111, which is connected to the digital-analog converter portion 100, is preferably formed using the same material as the gate electrode of the transistor.

[0090] Note that the wiring included in the wiring group 112_1, the wiring included in the wiring group 112_2, the wiring 113_1, and the wiring 113_2 are connected to a source and drain electrode of the transistor in many cases, for example. Accordingly, each of parts of the wiring included in the wiring group 112_1, the wiring included

in the wiring group 112_2, the wiring 113_1, and the wiring 113_2, which are connected to the digital-analog converter portion 100, is preferably formed using the same material as a conductive layer connected to a semiconductor layer in the transistor.

[0091] Note that although FIG 1A shows a case where the digital signal with N bits is converted into the first analog signal and the second analog signal by the digital-analog converter portion 100, this embodiment is not limited thereto. As shown in FIG 1B, the digital signal with N bits can be converted into n (n is a natural number) analog signals.

[0092] The digital-analog converter portion 100 shown in FIG 1B is connected to the wiring group 111, wiring groups 112_1 to 112_ n , and wirings 113_1 to 113_ n , for example.

[0093] For example, the first to n th voltage groups are input to the wiring groups 112_1 to 112_ n and first to n th analog signals are output from the wirings 113_1 to 113_ n .

[0094] In accordance with the digital signal with N bits, the digital-analog converter portion 100 brings the wirings 113_1 to 113_ n and ones of wirings in the wiring groups 112_1 to 112_ n into conduction so that the potentials of the wirings 113_1 to 113_ n and ones of wirings in the wiring groups 112_1 to 112_ n are made to be the same. For example, in accordance with the digital signal with N bits, the digital-analog converter portion 100 brings a wiring 113_ i (i is one of 1 to n) and one of a wiring group 112_ i into conduction so that the potentials of the wiring 113_ i and the one of the wiring group 112_ i are made to be the same. In this manner, in the digital-analog converter portion 100, the potentials of the wirings 113_1 to 113_ n are determined in accordance with the digital signal with N bits and n voltage groups.

[0095] In this manner, the digital-analog converter portion 100 converts the digital signal with N bits into the n analog signals (the first to n th analog signals) and output the n analog signals to the wirings 113_1 to 113_ n , respectively. In other words, in accordance with the digital signal with N bits, the digital-analog converter portion 100 selects ones of the respective n voltage groups (the first to n th voltage groups) and output the ones of the respective n voltage groups to the wirings 113_1 to 113_ n , respectively.

[0096] Note that the magnitude relation of n , N , and M is preferably $n < N < M$. However, this embodiment is not limited to this.

[0097] Note that when the digital-analog converter portion 100 shown in FIG. 1B is used for a display device, a pixel is divided into n subpixels in many cases. In that case, if n is a large number, the number of subpixels becomes large, whereby the area for one pixel is increased and resolution is decreased in some cases. In order to prevent the decrease in resolution, a magnitude relation of $n \leq 5$ is preferable. A magnitude relation of $n \leq 3$ is more preferable because improvement in a viewing angle is highly effective even when the number of the

subpixels is 3 or less. A magnitude relation of $n = 2$ is further preferable. However, this embodiment is not limited to this.

[0098] Note that when the digital-analog converter portion 100 shown in FIG. 1B is used for a display device, the pixel is preferably divided into n subpixels. Then, n subpixels are connected to the wirings 113_1 to 113_ n . However, the n subpixels can be connected to the wirings 113_1 to 113_ n , through a buffer. The digital-analog converter portion 100 outputs the n analog signals each corresponding to the digital signal with N bits to the n subpixels through the wirings 113_1 to 113_ n .

[0099] However, the wirings 113_1 to 113_ n can be connected to pixels, or circuits other than subpixels; for example, the wirings 113_1 to 113_ n can be connected to a digital-analog converter portion which is different from the digital-analog converter portion 100. Then, the digital-analog converter portion which is different from the digital-analog converter portion 100 can be connected to the pixel or the subpixel. For example, the digital-analog converter portion 100 functions as a DAC for a high-order bit, selects some voltages, and outputs the voltages to the digital-analog converter portion which is different from the digital-analog converter portion 100.

On the other hand, the digital-analog converter portion which is different from the digital-analog converter portion 100 functions as a DAC for a low-order bit, divides some voltages output from the DAC (the digital-analog converter portion 100) for the high-order bit by using a resistor element or a capacitor element, generates a new voltage, and outputs the new voltage to the pixel or the subpixel. In this manner, the number of voltages in the voltage group and the number of wirings in each of the wiring groups 112_1 to 112_ n can be reduced.

[0100] Note that as shown in FIG. 1C, the digital-analog converter portion 100 can include n circuits which function as digital-analog converter circuits (hereinafter referred to as D/A converter circuits or DACs).

[0101] As the n circuits which function as the DACs, circuits 101_1 to 101_ n are used. For example, as the circuits 101_1 to 101_ n , resistor ladder DACs, resistor string DACs, current output DACs, delta-sigma DACs, ROM decoder DACs, tournament DACs, DACs with a demultiplexer, or the like can be used. However, this embodiment is not limited to this.

[0102] The circuits 101_1 to 101_ n are connected to the wiring group 111. The circuits 101_1 to 101_ n are connected to the wiring groups 112_1 to 112_ n , respectively. The circuits 101_1 to 101_ n are connected to the wirings 113_1 to 113_ n , respectively. For example, a circuit 101_ i (i is one of 1 to n) is connected to the wiring group 111, the wiring 112_ i , and the wiring 113_ i .

[0103] For example, with respect to the digital signal with N bits, the circuit 101_ i brings the wiring 113_ i and one of the wiring group 112_ i into conduction so that the potentials thereof are made to be the same. In this manner, in the circuit 101_ i , the potential of the wiring 113_ i is determined with respect to the digital signal with N bits

and the input voltage group.

[0104] In this manner, the circuit 101_{*i*} converts the digital signal with *N* bits into the analog signal and output the analog signal to the wiring 113_{*i*}. In other words, in accordance with the digital signal with *N* bits, the circuit 101_{*i*} selects ones of the input voltage groups and outputs the one from the input voltage groups to the wiring 113_{*i*}.

[0105] In this manner, in the digital-analog converter portion of this embodiment, since one digital signal can be converted into a plurality of analog signals, a look-up table can be unnecessary. Therefore, heat generation or an increase in power consumption due to reading a look-up table from a memory element can be prevented.

[0106] Further, for example, in the case where a video signal is generated in a display device by using the digital-analog converter portion of this embodiment, a portion for generating the video signal and a pixel portion can be formed over the same substrate. Accordingly, since the number of connection between a panel and an external component can be reduced, poor connection in the connection portion of the panel and the external component can be suppressed, whereby improvement in reliability, an increase in yield, reduction in production cost, high-definition, or the like can be achieved.

(Embodiment 2)

[0107] In this embodiment, one example of the digital-analog converter portion 100 in which one digital signal is converted into two analog signals as shown in FIG 1A will be described with reference to FIG 2A.

[0108] The digital-analog converter portion 100 includes a circuit 201, a circuit 202₁, and a circuit 202₂.

[0109] The circuit 201 is connected to the wiring group 111 and a wiring group 114. The circuit 202₁ is connected to the wiring group 112₁, the wiring 113₁, and an output terminal of the circuit 201. The circuit 202₂ is connected to the wiring group 112₂, the wiring 113₂, and the output terminal of the circuit 201.

[0110] The wiring group 114 includes a plurality of wirings. For example, the wiring group 114 includes *N* wirings of wirings 114₁ to 114_{*N*}.

[0111] An inverted digital signal is input to the wiring group 114. Therefore, the number of bits of the inverted digital signal corresponds to the number of wirings in the wiring group 114 in many cases. For example, in the case where the inverted digital signal has *N* bits, the number of the wirings in the wiring group 114 is *N*. However, this embodiment is not limited to this, and a variety of signals, voltages, or currents can be input to the wiring group 114.

[0112] Note that the amplitude voltage of the inverted digital signal with *N* bits is preferably the same as an amplitude voltage with *N* bits. However, this embodiment is no limited to this.

[0113] Note that the wiring group 111 and the wiring group 114 can be connected through a circuit such as an inverter, which has a function of inverting and output-

ting an input signal. For example, a wiring 111_{*j*} (*j* is one of 1 to *N*) is connected to an input terminal of the inverter, and a wiring 114_{*j*} is connected to an output terminal of the inverter. In such a case, the digital signal with *N* bits which is to be input to the wiring group 111 is inverted by the inverter and then input to the wiring group 114. Accordingly, the inverted digital signal with *N* bits can be omitted.

[0114] Note that if the circuit 201 has a function of generating the inverted digital signal with *N* bits, the wiring group 114 can be omitted.

[0115] Note that the inverted digital signal with *N* bits is not necessary depending on the configuration of the circuit 201. In this case, the wiring group 114 can be omitted.

[0116] The circuit 201 function as a decoder circuit, for example. As the circuit 201, a BCD-DEC (binary coded decimal decoder) circuit, a BCD priority decoder circuit, an address decoder circuit, or the like can be used. However, this embodiment is not limited to these. The circuit 201 may include a plurality of logic circuits or a plurality of combinational logic circuits.

[0117] The circuit 202₁ and the circuit 202₂ function as selectors. For example, as the circuits 202₁ and the circuit 202₂, a selector circuit 202_{1a} and a selector circuit 202_{2a} shown in FIG. 2A can be used, respectively.

[0118] The selector circuit 202_{1a} and the selector circuit 202_{2a} each include a plurality of terminals. For example, in the case where the number of voltages in the first voltage group or in the second voltage group is *M*, the number of the terminals is (*M* + 1). In the selector circuit 202_{1a} first to *M*th terminals are connected to the wiring group 112₁ (wirings 112₁₁ to 112_{1*M*}, respectively), and the (*M* + 1)th terminal is connected to the wiring 113₁. On the other hand, in the selector circuit 202_{2a}, first to *M*th terminals are connected to the wiring group 112₂ (wirings 112₂₁ to 112_{2*M*}, respectively), and the (*M* + 1)th terminal is connected to the wiring 113₂.

[0119] The selector circuit 202_{1a} and the selector circuit 202_{2a} are controlled by an output signal of the circuit 201. For example, in accordance with the output signal of the circuit 201, the selector circuit 202_{1a} brings one of the wiring group 112₁ and the wiring 113₁ into conduction, and the selector circuit 202_{2a} brings one of the wiring group 112₂ and the wiring 113₂ into conduction.

[0120] Next, the operation of the digital-analog converter portion 100 shown in FIG 2A will be described.

[0121] The digital signal with *N* bits and the inverted digital signal with *N* bits are input to the circuit 201.

[0122] The circuit 201 generates a digital signal in accordance with the digital signal with *N* bits and the inverted digital signal with *N* bits. In other words, the circuit 201 decodes (decrypts) the digital signal with *N* bits and the inverted digital signal with *N* bits. Specifically, for example, the circuit 201 inputs the digital signal with *N* bits

and the inverted digital signal with N bits to the plurality of logic circuits or the plurality of combinational logic circuits to control whether an output signal from each logic circuit is an H signal or an L signal.

[0123] Since the number of bits of the digital signal generated by the circuit 201 is the same as the number of voltages in the first voltage group or in the second voltage group in many cases, the number of bits of the digital signal is set to be M and the digital signal having M bits is referred to as a digital signal with M bits.

[0124] Note that the amplitude voltage of the digital signal with M bits is the same as that of the digital signal with N bits in many cases. In such a case, a positive power supply voltage and a negative power supply voltage used for the circuit 201 are preferably the same as the value of an H signal of the digital signal with N bits and the value of an L signal of the digital signal with N bits, respectively. However, in the case where the circuit 201 has a level-shift function, the amplitude voltage of the digital signal with M bits can be higher than that of the digital signal with N bits.

[0125] After that, the circuit 201 inputs the digital signal with M bits to the circuit 202_1 and the circuit 202_2 to control the circuit 202_1 and the circuit 202_2.

[0126] In specific, in accordance with the digital signal with M bits, the circuit 202_1 brings one of the wiring group 112_1 and the wiring 113_1 into conduction so that the potentials thereof are made to be the same. At the same time, in accordance with the digital signal with M bits, the circuit 202_2 brings one of the wiring group 112_2 and the wiring 113_2 into conduction so that the potentials thereof are made to be the same.

[0127] In this manner, the circuit 202_1 converts the digital signal with M bits into a first analog signal and outputs the first analog signal to the wiring 113_1. The circuit 202_2 converts the digital signal with M bits into the second analog signal and outputs the second analog signal to the wiring 113_2. Alternatively, in accordance with the digital signal with M bits, the circuit 202_1 selects one of the first voltage group and outputs the one of the first voltage group to the wiring 113_1 as the first analog signal. Based on the digital signal with M bits, the circuit 202_2 selects one of the second voltage group and outputs the one of the second voltage group to the wiring 113_2 as the second analog signal.

[0128] Note that the digital signal with N bits and the inverted digital signal with N bits can be collectively denoted as a first digital signal. Accordingly, the first digital signal may include the digital signal with N bits and the inverted digital signal with N bits in some cases. However, only the digital signal with N bits can be denoted as the first digital signal without including the inverted signal with N bits.

[0129] Note that the digital signal with M bits can be denoted as a second digital signal. However, in the case where the circuit 201 generates the digital signal with M bits and the inverted signal of the digital signal with M bits (hereinafter such an inverted digital signal is referred

to as an inverted digital signal with M bits), the digital signal with M bits and the inverted digital signal with M bits can be collectively denoted as the second digital signal.

[0130] Note that the number of elements (e.g., a switch and a transistor) included in the circuit 201 is preferably larger than the number of elements included in the circuit 202_1 or the number of elements included in the circuit 202_2. Accordingly, the number of the elements included in the circuit 202_1 and the number of the elements included in the circuit 202_2 are reduced, whereby downsizing of a circuit scale can be achieved. However, this invention is not limited to this, and the number of the elements included in the circuit 201 can be smaller than the number of the elements included in the circuit 202_1 or the circuit 202_2.

[0131] Note that as described in FIG. 1B, also in FIG. 2A, the digital-analog converter portion 100 can convert the digital signal with N bits into n analog signals. In this case, for example, the circuit 201 and circuits 202_1 to 202_2 are used as shown in FIG. 3

[0132] The circuits 202_1 to 202_2 are connected to the wiring groups 112_1 to 112_2, respectively, and the wirings 113_1 to 113_2, respectively, and the output terminal of the circuit 201. For example, a circuit 202_1 (i is one of 1 to 2) is connected to the output terminal of the circuit 201, the wiring group 112_1, and the wiring 113_1.

[0133] Each of the circuits 202_1 to 202_2 corresponds to the circuit 202_1 or the circuit 202_2 shown in FIG 2A.

[0134] Next, specific examples of the circuit 201, the circuit 202_1, and the circuit 202_2 shown in FIG 2A will be described with reference to FIG. 4A.

[0135] The circuit 201 includes a plurality of logic circuits. The number of logic circuits corresponds to the number of the voltages in the first voltage group or the number of the voltages in the second voltage group in many cases. Accordingly, for example, in the case where the number of the voltages in the first voltage group or the number of the voltages in the second voltage group is M , the circuit 201 includes M logic circuits of logic circuits 203_1 to 203_2.

[0136] The logic circuits 203_1 to 203_2 each include a plurality of input terminals and one output terminal. The number of input terminals corresponds to the number of the wirings in the wiring group 111 or the number of the wirings in the wiring group 114 in many cases. Accordingly, for example, in the case where the number of the wirings in the wiring group 111 or the number of the wirings in the wiring group 114 is N , the logic circuits 203_1 to 203_2 each include N input terminals. However, in the case where wirings different from those of the wiring group 111 and the wiring group 114 are connected to the logic circuits 203_1 to 203_2, the number of input terminals corresponds to the sum of the different wirings and the number of the wirings in the wiring group 111 or the number of the wirings in the wiring group 114 in many cases.

[0137] The circuit 201_1 and the circuit 201_2 each include a plurality of switches. The number of switches corresponds to the number of the voltages in the first voltage group or the number of the voltages in the second voltage group in many cases. Accordingly, for example, in the case where the number of the voltages in the first voltage group or the number of the voltages in the second voltage group is M , the circuit 202_1 includes M switches of switches 204_11 to 204_1M, and the circuit 202_2 includes M switches of switches 204_21 to 204_2M.

[0138] The N input terminals of the logic circuits 203_1 to 203_M are connected to the wirings 111_1 to 111_N or the wirings 114_1 to 114_N. For example, j th (j is one of 1 to N or a natural number) input terminal of a logic circuit 203_ k (k is one of 1 to M) is connected to the wiring 111_ j or the wiring 114_ j . All the logic circuits 203_1 to 203_M have different combinations of the input terminal and the wiring. For example, $2N$ combinations can be given at a maximum. However, input terminals in some logic circuits can have the same connection relation. Accordingly, $M \leq 2N$ is preferable. In addition, $M = 2N$ is more preferable.

[0139] Output terminals of the logic circuits 203_1 to 203_M are connected to control terminals of the switches 204_11 to 204_1M, respectively, and control terminals of the switches 204_21 to 204_2M, respectively. For example, an output terminal of the logic circuit 203_ k is connected to a control terminal of a switch 204_1 k and the control terminal of a switch 204_2 k .

[0140] First terminals of the switches 204_11 to 204_1M are connected to the wirings 112_11 to 112_1M, respectively. Second terminals of the switches 204_11 to 204_1M are all connected to the wiring 113_1. For example, the first terminal of the switch 204_1 k is connected to a wiring 112_1 k , and the second terminal of the switch 204_1 k is connected to the wiring 113_1. However, the second terminals of the switches 204_11 to 204_1M can be connected to their respective wirings.

[0141] First terminals of the switches 204_21 to 204_2M are connected to the wirings 112_21 to 112_2M, respectively. Second terminals of the switches 204_21 to 204_2M are all connected to the wiring 113_2. For example, the first terminal of the switch 204_2 k is connected to a wiring 112_2 k , and the second terminal of the switch 204_2 k is connected to the wiring 113_2. However, the second terminals of the switches 204_21 to 204_2M can be connected to their respective wirings.

[0142] Next, the operation of the digital-analog converter portion 100 shown in FIG. 4A will be described.

[0143] The digital signal with N bits and the inverted digital signal with N bits are input to the N input terminals of the logic circuits 203_1 to 203_M. For example, the digital signal with j th bit or the inverted digital signal with j th bit is input to the j th input terminal of each of the logic circuits 203_1 to 203_M.

[0144] The logic circuits 203_1 to 203_M each output an H signal or an L signal in accordance with a combination of the digital signal with N bits and the inverted

digital signal with N bits input to each of the logic circuit 203_1 to 203_M. The output signals from these logic circuits 203_1 to 203_M correspond to the digital signals with M bits described in FIG 2A.

[0145] After that, the logic circuits 203_1 to 203_M input the digital signals with M bits to the control terminals of the switches 204_11 to 204_1M and the control terminals of the switches 204_21 to 204_2M so that on and off of the switches 204_11 to 204_1M and the switches 204_21 to 204_2M are controlled. For example, the logic circuit 203_ k (k is one of 1 to M) inputs the digital signal to the control terminal of the switch 204_1 k and the control terminal of the switch 204_2 k so that on and off of the switches 204_1 k and 204_2 k are controlled. Accordingly, the timings of turning on and off the switches 204_1 k and 204_2 k are approximately the same.

[0146] In specific, when one of the switches 204_11 to 204_1M is turned on in accordance with the digital signal with M bits, the switches 204_11 to 204_1M bring one of the wiring group 112_1 and the wiring 113_1 into conduction so that the potentials thereof are made to be the same. At the same time, when one of the switches 204_21 to 204_2M is turned on with respect to the digital signal with M bits, the switches 204_21 to 204_2M bring one of the wiring group 112_2 and the wiring 113_2 into conduction so that the potentials thereof are made to be the same.

[0147] Note that in the case where each of the switches is turned on when an H signal is input to the control terminal, it is preferable that one of the logic circuits 203_1 to 203_M output the H signal in order to turn on one of the switches 204_11 to 204_1M and one of the switches 204_21 to 204_2M on, and that the other logic circuits 203_1 to 203_M output L signals.

[0148] On the other hand, in the case where each of the switches is turned on when an L signal is input to the control terminal, it is preferable that one of the logic circuits 203_1 to 203_M output the L signal in order to turn on one of the switches 204_11 to 204_1M and one of the switches 204_21 to 204_2M on, and that the other logic circuits 203_1 to 203_M output H signals.

[0149] Note that the number of switches included in the circuit 202_1 corresponds to the number of switches included in the circuit 202_2 in many cases. However, the number of switches included in the circuit 202_1 can be different from that of switches included in the circuit 202_2.

[0150] Note that as the logic circuits 203_1 to 203_M, for example, one of AND circuits, OR circuits, NAND circuits, NOR circuits, XOR circuits, XNOR circuits, and the like, or combinational logic circuits of some of them can be used.

[0151] Note that as the switches 204_11 to 204_1M and the switches 204_21 to 204_2M, for example, p-channel transistors, n-channel transistors, or CMOS switches in which p-channel transistors and n-channel transistors are combined can be used. Note that gate, a first terminal (one of source and drain), and a second

terminal (the other of source and drain) of each transistor correspond to the control terminal, the first terminal, and the second terminal of each of the switches, respectively, and have the same connection structure.

[0152] For example, the digital-analog converter portion 100 in the case where n-channel transistors are used as the switches shown in FIG. 4A will be shown in FIG. 4B.

[0153] Transistors 204_11a to 204_1Ma correspond to the switches 204_11 to 204_1M, respectively, and are n-channel transistors. Transistors 204_21a to 204_2Ma correspond to the switches 204_21 to 204_2M and are n-channel transistors.

[0154] NOR circuits 203_1a to 203_Ma correspond to the logic circuits 203_1 to 203_M, respectively. The NOR circuits are used because n-channel transistors are turned on when H signals are input to gate, and also because the NOR circuits output H signals when input signals are all L signals and the logic circuits output L signals when one of input signals is an H signal. However, this embodiment is not limited to this. For example, as the logic circuits 203_1 to 203_M, AND circuits, circuits in which NAND circuits and inverters are connected in series, a variety of combinational logic circuits, or the like can be used.

[0155] In order to make switching noise of the first analog signals approximately the same no matter which transistor is turned on and which voltage is selected, for example, the ratios of W/L (W is channel width and L is channel length) of the transistors 204_11a to 204_1Ma are preferably the same. Accordingly, in the case where the digital-analog converter portion 100 shown in FIG. 4B is used for a display device, a first subpixel expresses gray levels in accordance with the first analog signal with approximately the same switching noise no matter which transistor is turned on. Therefore, the adverse effect due to the switching noise of the first analog signal can be reduced. However, this embodiment is not limited to this. For example, when the ratio of W/L of the transistor 204_1ka is $W/L1a(k)$, the following is possible: $W/L1a(k-1) < W/L1a(k) < W/L1a(k+1)$. At that time, when the potential of the first terminal (the potential of the wiring 112_1k) is $V1a(k)$, the following is preferable: $V1a(k-1) < V1a(k) < V1a(k+1)$.

[0156] Like the transistors 204_11 a to 204_1Ma, for example, the ratios of W/L (W is channel width and L is channel length) of the transistors 204_21 to 204_2Ma are preferably the same. However, this embodiment is not limited to this. For example, when the ratio of W/L of the transistor 204_2ka is $W/L2a(k)$, the following is possible: $W/L2a(k-1) < W/L2a(k) < W/L2a(k+1)$. At that time, when the potential of the first terminal (the potential of the wiring 112_1k) is $V2a(k)$, the following is preferable: $V2a(k-1) < V2a(k) < V2a(k+1)$.

[0157] In order to make switching noise of the first analog signal approximately the same as that of the second analog signal, for example, the ratio of W/L of the transistor 204_1ka and the ratio of W/L of the transistor 204_2ka are preferably the same. Accordingly, in the

case where the digital-analog converter portion 100 shown in FIG. 4B is used for a display device, the first subpixel and a second subpixel express gray levels in accordance with their respective signals with approximately the same switching noise. Therefore, the adverse effect due to the switching noise of the signals can be reduced. However, this embodiment is not limited to this.

[0158] The value of an H signal which is an output signal from the circuit 201 is preferably larger than the maximum value of the first voltage group and the maximum value of the second voltage group, for example, so that a voltage (V_{gs}) between gate and source becomes high when each transistor is turned on. In this manner, the size of each transistor can be small. On the other hand, for example, when each transistor is turned off, the voltage (V_{gs}) between the gate and the source may be equal to or lower than a threshold voltage. Accordingly, the value of an L signal which is an output signal from the circuit 201 is preferably equal to or smaller than the minimum value of the first voltage group or the minimum value of the second voltage group, whichever is smaller, so that the amplitude of the output signal from the circuit 201 is made to be small. In this manner, a reduction in power consumption can be achieved.

[0159] For example, the digital-analog converter portion 100 in the case where p-channel transistors are used as the switches shown in FIG. 4A will be shown in FIG 5A.

[0160] Transistors 204_11b to 204_1Mb correspond to the switches 204_11 to 204_1M and are p-channel transistors. Transistors 204_21b to 204_2Mb correspond to the switches 204_21 to 204_2M and are p-channel transistors.

[0161] NAND circuits 203_1b to 203_Mb correspond to the logic circuits 203_1 to 203_M. The NAND circuits are used because p-channel transistors are turned on when L signals are input to gate, and also because the NAND circuit output L signals when input signals are all H signals and the NAND circuits output H signals when one of input signals is an L signal. However, this embodiment is not limited to this. For example, as the logic circuits 203_1 to 203_M, OR circuits, circuits in which NOR circuits and inverters are connected in series, a variety of combinational logic circuits, or the like can be used.

[0162] Like the transistors 204_11a to 204_1Ma shown in FIG 4B, the ratios of W/L (W is channel width and L is channel length) of the transistors 204_21b to 204_2Mb are preferably the same. However, this embodiment is not limited to this. For example, when the ratio of W/L of the transistor 204_1kb is $W/L1b(k)$, the following is preferable: $W/L1b(k-1) < W/L1b(k) < W/L1b(k+1)$. At that time, when the potential of the first terminal (the potential of the wiring 112_1k) of the transistor 204_1kb is $V1b(k)$, the following is preferable: $V1b(k-1) > V1b(k) > V1b(k+1)$.

[0163] Like the transistors 204_21a to 204_2Ma shown in FIG. 4B, the ratios of W/L (W is channel width and L is channel length) of the transistors 204_21b to 204_2Mb are preferably the same. However, this em-

bodiment is not limited to this. For example, when the ratio of W/L of the transistor 204_2kb is $W/L2b(k)$, the following is preferable: $W/L2b(k-1) < W/L2b(k) < W/L2b(k+1)$. At that time, when the potential of the first terminal (the potential of the wiring 112_1k) of the transistor 204_2kb is $V2b(k)$, the following is preferable: $V2b(k-1) > V2b(k) > V2b(k+1)$.

[0164] As in FIG 4B, the ratio of W/L of the transistor 204_1kb and the ratio of W/L of the transistor 204_2kb are preferably the same. However, this embodiment is not limited to this.

[0165] The value of an L signal which is an output signal from the circuit 201 is preferably smaller than the minimum value of the first voltage group and the minimum value of the second voltage group, for example, so that the absolute value of a voltage (V_{gs}) between gate and source becomes large when each transistor is turned on. In this manner, the size of each transistor can be small. On the other hand, for example, when each transistor is turned off, the absolute value of the voltage (V_{gs}) between the gate and the source may be equal to or smaller than the absolute value of a threshold voltage. Accordingly, the value of an H signal which is an output signal from the circuit 201 is preferably equal to or larger than the maximum value of the first voltage group or the maximum value of the second voltage group, whichever is larger, so that the amplitude of the output signal from the circuit 201 is made to be small. In this manner, a reduction in power consumption can be achieved.

[0166] Note that a CMOS switch can be used as each switch. In the structure of each CMOS switch, a first terminal of an n-channel transistor and a first terminal of a p-channel transistor are connected to each other and a second terminal of the n-channel transistor and a second terminal of the p-channel transistor are connected to each other. Gate of the p-channel transistor and gate of the n-channel transistor are connected to their respective wirings. For example, the gate of the p-channel transistor is connected to the output terminal of the logic circuit 203_k and the gate of the n-channel transistor is connected to the output terminal of the logic circuit 203_k through a circuit such as an inverter, which has a function of inverting an input signal. Alternatively, the gate of the p-channel transistor is connected to the output terminal of the logic circuit 203_k through a circuit such as an inverter, which has a function of inverting an input signal and the gate of the n-channel transistor is connected to the output terminal of the logic circuit 203_k.

[0167] In the case where the CMOS switch is used as each switch, the value of the H signal which is an output signal from the circuit 201 may be approximately equal to or larger than the maximum value of the first voltage group or the maximum value of the second voltage group, whichever is larger. The value of the L signal which is an output signal from the circuit 201 may be approximately equal to or smaller than the minimum value of the first voltage group or the minimum value of the second voltage group, whichever is smaller. Accordingly, a reduction in

power consumption can be achieved because the amplitude voltage of the output signal of the circuit 201 is decreased.

[0168] Note that although the case where the digital-analog converter portion 100 includes the plurality of logic circuits and the plurality of switches is described, this embodiment is not limited thereto. The digital-analog converter portion 100 may include a logic circuit having a plurality of (e.g., N) input terminals and one output terminal, a first switch, and a second switch. In the logic circuit, one input terminal (e.g., a j th input terminal) is connected to a first wiring or a second wiring and an output terminal is connected to a control terminal of the first switch and a control terminal of the second switch. A first terminal of the first switch is connected to a third wiring and a second terminal of the first switch is connected to a fourth wiring. A first terminal of the second switch is connected to a fifth wiring and a second terminal of the second switch is connected to a sixth wiring.

[0169] Note that the first wiring, the second wiring, the third wiring, the fourth wiring, the fifth wiring, and the sixth wiring correspond to one of the wirings included in the wiring group 111, one of the wirings included in the wiring group 114, one of the wirings included in the wiring group 112_1, the wiring 113_1, one of the wiring group 112_2, and the wiring 113_2, respectively. The first switch and the second switch correspond to one of the switches 204_11 to 204_1M and one of the switches 204_21 to 204_2M, respectively.

[0170] Note that as described in FIG 1B and FIG 3, the digital-analog converter portion 100 can convert the digital signal with N bits into n analog signals also in FIG. 4B. In this case, for example, the circuit 201 and the circuits 202_1 to 202_n are used as shown in FIG. 5B.

[0171] The circuits 202_1 to 202_n each include a plurality of switches. For example, the circuit 202_i includes switches 204_i1 to 204_iM. The switches 204_i1 to 204_iM correspond to the switches 204_11 to 204_1M or the switches 204_21 to 204_2M shown in FIG. 4A.

[0172] First terminals of the switches 204_i1 to 204_iM are connected to the wiring group 112_i, second terminals of the switches 204_i1 to 204_iM are all connected to the wiring 113_i, and control terminals of the switches 204_i1 to 204_iM are connected to the output terminals of the circuit 201.

[0173] As described above, since the digital-analog converter portion of this embodiment can convert one digital signal into a plurality of analog signals, a look-up table can be unnecessary. Therefore, heat generation or an increase in power consumption due to reading a look-up table from a memory element can be prevented.

[0174] Further, for example, in the case where a video signal is generated in a display device by using the digital-analog converter portion of this embodiment, a portion for generating the video signal and a pixel portion can be formed over the same substrate. Accordingly, since the number of connection between a panel and an external component can be reduced, poor connection in the con-

nection portion of the panel and the external component can be suppressed, whereby improvement in reliability, an increase in yield, reduction in production cost high-definition, or the like can be achieved.

(Embodiment 3)

[0175] In this embodiment, one example of the digital-analog converter portion 100 which can separately set the polarity of each analog signal will be described with reference to FIG. 6A.

[0176] In order to separately set the polarity of each analog signal, for example, the digital-analog converter portion 100 has a first mode and a second mode. Even when the digital signals with N bits are input, the values (polarities) of the analog signals are different from each other in the first mode and the second mode in many cases.

[0177] For example, each analog signal has a positive potential in the first mode and has a negative potential in the second mode. Accordingly, the polarity of each analog signal can be separately set. However, this embodiment is not limited to this. The values and the polarities of the analog signals are the same in the first mode and the second mode in some cases. Alternatively, the values of the analog signals can be different from each other in the first mode and the second mode.

[0178] In order to switch the first mode and the second mode to each other, a selecting signal is input, for example. Thus, the digital-analog converter portion 100 is connected to a wiring 115, for example. The selecting signal is input to the wiring 115. The selecting signal is a digital signal and has a function of selecting whether the digital-analog converter portion 100 is operated with the first mode or the second mode, for example. However, in the case where the digital signal with N bits has the same function as the selecting signal, the selecting signal can be omitted.

[0179] Note that an inverted signal of the selecting signal (hereinafter such a signal is referred to as an inverted selecting signal) can be input to the digital-analog converter portion 100. In this case, for example, a new wiring is connected to the digital-analog converter portion 100 and the inverted selecting signal is input to the digital-analog converter portion 100 through this wiring. This wiring can function as a signal line, for example. Note that the terms "a selecting signal" mean a selecting signal and also an inverted selecting signal in some cases.

[0180] Note that since the selecting signal and the inverted selecting signal are input to the circuit which is the same as that receives the digital signal with N bits, for example, the amplitude voltage of the selecting signal and the amplitude voltage of the inverted selecting signal are preferably the same as that of the digital signal with N bits. However, this embodiment is not limited to this.

[0181] In order to separately set the polarity of each analog signal, a positive first voltage group, a negative first voltage group, a positive second voltage group, and

a negative second voltage group are input to the digital-analog converter portion 100. In this embodiment, by increasing the number of wirings, these voltage groups are input to the digital-analog converter portion 100 at the same time. For example, the positive first voltage group, the negative first voltage group, the positive second voltage group, and the negative second voltage group are input to a wiring group 112p_1 a wiring group 112n_1, a wiring group 112p_2, and a wiring group 112n_2, respectively.

[0182] Note that the wiring group 112p_1 and the wiring group 112n_1 can be collectively denoted as the wiring group 112_1. Also, the wiring group 112p_2 and the wiring group 112n_2 can be collectively denoted as the wiring group 112_2.

[0183] Note that the positive first voltage group and the negative first voltage group can be collectively denoted as the first voltage group. Also, the positive second voltage group and the negative second voltage group can be collectively denoted as the second voltage group.

[0184] Note that the minimum voltage of the positive first voltage group and the maximum voltage of the negative first voltage group are the same in some cases. Similarly, the minimum voltage of the positive second voltage group and the maximum voltage of the negative second voltage group are the same in some cases.

[0185] Next, the operation of the digital-analog converter portion 100 shown in FIG 6A will be described.

[0186] The digital signal with N bits, the positive first voltage group, the negative first voltage group, the positive second voltage group, the negative second voltage group, and the selecting signal are input to the digital-analog converter portion 100.

[0187] In the first mode, in accordance with the digital signal with N bits, the digital-analog converter portion 100 brings one of the wiring group 112p_1 and the wiring 113_1 into conduction so that the potentials thereof are the same. At the same time, in accordance with the digital signal with N bits, the digital-analog converter portion 100 brings one of the wiring group 112p_2 and the wiring 113_2 into conduction so that the potentials thereof are made to be the same.

[0188] In this manner, in the first mode, the digital-analog converter portion 100 converts the digital signal with N bits into a positive first analog signal and a positive second analog signal. Alternatively, in accordance with the digital signal with N bits, the digital-analog converter portion 100 outputs one of the positive first voltage group to the wiring 113_1 as the positive first analog signal and outputs one of the positive second voltage group to the wiring 113_2 as the positive second analog signal.

[0189] On the other hand, in the second mode, in accordance with the digital signal with N bits, the digital-analog converter portion 100 brings one of the wiring group 112n_1 and the wiring 113_1 into conduction so that the potentials thereof are made to be the same. At the same time, in accordance with the digital signal with N bits, the digital-analog converter portion 100 brings one

of the wiring group 112n_2 and the wiring 113_2 into conduction so that the potentials thereof are made to be the same.

[0190] In this manner, in the second mode, the digital-analog converter portion 100 converts the digital signal with N bits into a negative first analog signal and a negative second analog signal. Alternatively, in accordance with the digital signal with N bits, the digital-analog converter portion 100 outputs one of the positive first voltage group to the wiring 113_1 as the negative first analog signal and outputs one of the negative second voltage group to the wiring 113_2 as the negative second analog signal.

[0191] Note that in the digital-analog converter portion 100, the polarities of the first analog signal and the second analog signal can be set to be different from each other in each mode. In order to realize this, for example, the positive second voltage group is input to the wiring group 112n_2 and the negative second voltage group is input to the wiring group 112p_2.

[0192] Next, one example of the digital-analog converter portion 100 shown in FIG. 6A will be described with reference to FIG. 6B.

[0193] The digital-analog converter portion 100 includes a circuit 201p, a circuit 201n, a circuit 202p_1, a circuit 202n_1, a circuit 202p_2, and a circuit 202n_2.

[0194] The circuit 201p and the circuit 201n correspond to the circuit 201 shown in FIG. 4A. The circuit 202p_1 and the circuit 202n_1 correspond to the circuit 202_1 shown in FIG. 4A. The circuit 202p_2 and the circuit 202n_2 correspond to the circuit 202_2 shown in FIG. 4A.

[0195] Note that the circuit 201p and the circuit 201n can be collectively denoted as a first circuit. The circuit 202p_1 and the circuit 202n_1 can be collectively denoted as a second circuit. The circuit 202p_2 and the circuit 202n_2 can be collectively denoted as a third circuit.

[0196] The circuit 201p is connected to the wiring group 111, the wiring group 114, and the wiring 115. The circuit 201n is connected to the wiring group 111, the wiring group 114, and the wiring 116. The circuit 202p_1 is connected to the wiring group 112p_1, the wiring 113_1, and an output terminal of the circuit 201 p. The circuit 202n_1 is connected to the wiring group 112n_1, the wiring 113_1, and an output terminal of the circuit 201n. The circuit 202p_2 is connected to the wiring group 112p_2, the wiring 113_2, and the output terminal of the circuit 201p. The circuit 202n_2 is connected to the wiring group 112n_2, the wiring 113_2, and the output terminal of the circuit 201n.

[0197] An inverted selecting signal is input to the wiring 116, for example. However, the wiring 115 and the wiring 116 are connected to each other through an inverter, so that a selecting signal input to the wiring 115 is inverted by the inverter and input to the wiring 116. In this manner, the inverted selecting signal can be omitted.

[0198] Next, the operation of the digital-analog converter portion 100 shown in FIG. 6B will be described.

[0199] The digital signal with N bits, the inverted digital

signal with N bits, and the selecting signal are input to the circuit 201p and the digital signal with N bits, the inverted digital signal with N bits, and the inverted selecting signal are input to the circuit 201n.

[0200] Like the circuit 201 shown in FIG. 2A, the circuit 201p converts the digital signal with N bits, the inverted digital signal with N bits, and the selecting signal into digital signals. The circuit 201n converts the digital signal with N bits, the inverted digital signal with N bits, and the inverted selecting signal into digital signals.

[0201] Like the circuit 201 in FIG. 2A, the number of bits of the digital signal generated in this circuit 201p and the number of bits of the digital signal generated in the circuit 202n correspond to the number of the voltages in the positive first voltage group, the number of the voltages in the negative first voltage group, the number of the voltages in the positive second voltage group, or the number of voltages in the negative second voltage group in many cases. Accordingly, for example, in the case where the number of these voltages is M , the number of bits of the digital signal generated in this circuit 201p and the number of bits of the digital signal generated in the circuit 202n are M , like the circuit 201 shown in FIG. 2A. Here, the digital signal generated in the circuit 201p is denoted as a first digital signal with M bits and the digital signal generated in the circuit 201n is denoted as a second digital signal with M bits.

[0202] After that, the circuit 201p inputs the first digital signal with M bits to the circuit 202p_1 and the circuit 202p_2 so that the circuit 202p_1 and the circuit 202p_2 are controlled. The circuit 201n inputs the second digital signal with M bits to the circuit 202n_1 and the circuit 202n_2 so that the circuit 202n_1 and the circuit 202n_2 are controlled.

[0203] In specific, in the first mode, the circuit 202p_1 brings one of the wiring group 112p_1 and the wiring 113_1 into conduction in accordance with the first digital signal with M bits, so that the potentials thereof are the same. At the same time, the circuit 202p_2 brings one of the wiring group 112p_2 and the wiring 113_2 into conduction in accordance with the first digital signal with M bits, so that the potentials thereof are made to be the same. At that time, the circuit 202n_1 brings the wiring group 112n_1 and the wiring 113_1 into non-conduction, and the circuit 202n_2 brings the wiring group 112n_2 and the wiring 113_2 into non-conduction.

[0204] In this manner, in the first mode, the circuit 202p_1 converts the first digital signal with M bits into the positive first analog signal and outputs the positive first analog signal to the wiring 113_1. The circuit 202p_2 converts the first digital signal with M bits into the positive second analog signal and outputs the positive second analog signal to the wiring 113_2. Alternatively, in the first mode, the circuit 202p_1 outputs one of the positive first voltage group to the wiring 113_1 as the positive first analog signal in accordance with the first digital signal with M bits. The circuit 202p_2 outputs one of the positive second voltage group to the wiring 113_2 as the positive

second analog signal in accordance with the first digital signal with M bits.

[0205] On the other hand, in the second mode, the circuit 202n_1 brings one of the wiring group 112n_1 and the wiring 113_1 into conduction in accordance with the second digital signal with M bits, so that the potentials thereof are made to be the same. At the same time, the circuit 202n_2 brings one of the wiring group 112n_2 and the wiring 113_2 into conduction in accordance with the second digital signal with M bits, so that the potentials thereof are made to be the same. At that time, the circuit 202p_1 brings the wiring group 112p_1 and the wiring 113_1 into non-conduction, and the circuit 202p_2 brings the wiring group 112p_2 and the wiring 113_2 into non-conduction.

[0206] In this manner, in the second mode, the circuit 202n_1 converts the second digital signal with M bits into the negative first analog signal and outputs the negative first analog signal to the wiring 113_1. The circuit 202n_2 converts the second digital signal with M bits into the negative second analog signal and outputs the negative second analog signal to the wiring 113_2. Alternatively, in the second mode, the circuit 202n_1 outputs one of the negative first voltage group to the wiring 113_1 as the negative first analog signal in accordance with the second digital signal with M bits. The circuit 202n_2 outputs one of the negative second voltage group to the wiring 113_2 as the negative second analog signal with respect to the second digital signal with M bits.

[0207] Note that the first digital signal with M bits and the second digital signal with M bits each correspond to the digital signal with M bits described in FIG. 2A.

[0208] Note that the first digital signal with M bits and the second digital signal with M bits can be collectively denoted as a second digital signal.

[0209] Note that the selecting signal can be denoted as a third digital signal. However, the selecting signal and the inverted selecting signal can be collectively denoted as the third digital signal.

[0210] Note that the polarities of the first analog signal and the second analog signal can be different from each other. For example, in order to achieve this, the positive second voltage group is input to the wiring group 112n_2 and the negative second voltage group is input to the wiring group 112p_2.

[0211] Next, with reference to FIG. 7, specific examples of the circuits 201p, 201n, 202p_1, 202n_1, 202p_2, and 202n_2 in FIG. 6B will be described.

[0212] Like the circuit 201 shown in FIG. 4A, the circuit 201p includes a plurality of logic circuits, for example, logic circuits 203p_1 to 203p_M. The circuit 201n includes a plurality of logic circuits, for example, logic circuits 203n_1 to 203n_M.

[0213] Like the logic circuits 203_1 to 203_M shown in FIG. 4A, the logic circuits 203p_1 to 203p_M and the logic circuits 203n_1 to 203n_M each include a plurality of input terminals. For example, since the circuit 201p is connected to the wiring 115 as well as the wiring group

111 and the wiring group 114 and the circuit 201n is connected to the wiring 116, the number of the input terminals is $(N + 1)$.

[0214] Like the circuit 202_1 shown in FIG. 4A, the circuit 202p_1 includes a plurality of switches, for example, switches 204p_11 to 204p_1M. The circuit 202n_1 includes a plurality of switches, for example, switches 204n_11 to 204n_M.

[0215] Like the circuit 202_2 shown in FIG. 4A, the circuit 202p_2 includes a plurality of switches, for example, switches 204p_21 to 204p_2M. The circuit 202n_2 includes a plurality of switches, for example, switches 204n_21 to 204n_2M.

[0216] An output terminal of a logic circuit 203p_k is connected to a control terminal of a switch 204p_1k and a control terminal of a switch 204p_2k. An output terminal of a logic circuit 203n_k is connected to a control terminal of a switch 204n_1k and a control terminal of a switch 204n_2k.

[0217] A first terminal of the switch 204p_1k is connected to a wiring 112p_1k. A second terminal of the switch 204p_1k is connected to a wiring 113_1. A first terminal of the switch 204n_1k is connected to a wiring 112n_1k. A second terminal of the switch 204n_1k is connected to the wiring 113_1. A first terminal of the switch 204p_2k is connected to a wiring 112p_2k. A second terminal of the switch 204p_2k is connected to a wiring 113_2. A first terminal of the switch 204n_2k is connected to a wiring 112n_2k. A second terminal of the switch 204n_2k is connected to a wiring 113_2.

[0218] Next, the operation of the digital-analog converter portion 100 shown in FIG 7 will be described.

[0219] The digital signal with N bits, the inverted digital signal with N bits, and the selecting signal are input to the logic circuits 203p_1 to 203p_M, and the digital signal with N bits, the inverted digital signal with N bits, and the inverted selecting signal are input to the input terminals of the logic circuits 203n_1 to 203n_M.

[0220] The logic circuits 203p_1 to 203p_M each output an H signal or an L signal in accordance with a combination of the digital signal with N bits and the inverted digital signal with N bits input. The logic circuits 203n_1 to 203n_M each output an H signal or an L signal in accordance with a combination of the digital signal with N bits and the inverted digital signal with N bits input.

[0221] For example, in the case where each switch is turned on when an H signal is input to the control terminal of the switch, in the first mode, one of the logic circuits 203p_1 to 203p_M outputs an H signal, and the logic circuits 203n_1 to 203n_M and the other of the logic circuits 203p_1 to 203p_M all output L signals. On the other hand, in the second mode, one of the logic circuits 203n_1 to 203n_M outputs an H signal, and the logic circuits 203p_1 to 203p_M and the other of the logic circuits 203n_1 to 203n_M all output L signals.

[0222] In another example, in the case where each switch is turned on when an L signal is input to the control terminal of the switch, in the first mode, one of the logic

circuits 203p_1 to 203p_M outputs an L signal, and the logic circuits 203n_1 to 203n_M and the other of the logic circuits 203p_1 to 203p_M all output H signals. On the other hand, in the second mode, one of the logic circuits 203n_1 to 203n_M outputs an L signal, and the logic circuits 203p_1 to 203p_M and the other of the logic circuits 203n_1 to 203n_M all output H signals.

[0223] Note that output signals of the logic circuits 203p_1 to 203p_M correspond to the first digital signal with M bits in FIG. 6B. Output signals of the logic circuits 203n_1 to 203n_M correspond to the second digital signal with M bits in FIG. 6B.

[0224] After that, the logic circuits 203p_1 to 203p_M input the first digital signals with M bits to control terminals of the switches 204p_11 to 204p_1M and control terminals of switches the 204p_21 to 204p_2M, so that on and off of the switches 204p_11 to 204p_1M and the switches 204p_21 to 204p_2M are controlled. For example, the logic circuit 203p_k (k is one of 1 to M) inputs the digital signal to the control terminal of the switch 204p_1k and the control terminal of the switch 204p_2k, so that on and off of the switches 204p_1k and 204p_2k is controlled. Accordingly, the timings of on and off of the switch 204p_1k and the switch 204p_2k are approximately the same in many cases.

[0225] At the same time, the logic circuits 203n_1 to 203n_M input the second digital signals with M bits to control terminals of the switches 204n_11 to 204n_1M and control terminals of the switches 204n_21 to 204n_2M, so that on and off of the switches 204n_11 to 204n_1M and the switches 204n_21 to 204n_2M are controlled. For example, the logic circuit 203n_k (k is one of 1 to M) inputs the digital signal to the control terminal of the switch 204n_1k and the control terminal of the switch 204n_2k, so that on and off of the switches 204n_1k and 204n_2k is controlled. Accordingly, the timings of on and off the switch 204n_1k and the switch 204n_2k are approximately the same in many cases.

[0226] Specifically, in the first mode, when one of the switches 204p_11 to 204p_1M is turned in response to the first digital signal with M bits, the switches 204p_11 to 204p_1M bring one of the wiring group 112p_1 and the wiring 113_1 into conduction, and the potentials thereof are made to be equal, for example. At the same time, in the first mode, when one of the switches 204p_21 to 204p_2M is turned on in response to the first digital signal with M bits, the switches 204p_21 to 204p_2M bring one of the wiring group 112p_2 and the wiring 113_2 into conduction, and the potentials thereof are made to be the same, for example. At that time, the switches 204n_11 to 204n_1M and the switches 204n_21 to 204n_2M are all turned off with respect to the second digital signal with M bits.

[0227] On the other hand, in the second mode, when one of the switches 204n_11 to 204n_1M is turned on in response to the second digital signal with M bits, the switches 204n_11 to 204n_1M bring one of the wiring group 112n_1 and the wiring 113_1 into conduction, and

the potentials thereof are made to be the same, for example. At the same time, in the second mode, when one of the switches 204n_21 to 204n_2M is turned on in response to the second digital signal with M bits, the switches 204n_21 to 204n_2M bring one of the wiring group 112n_2 and the wiring 113_2 into conduction, and the potentials thereof are made to be the same, for example. At that time, the switches 204p_11 to 204p_1M and the switches 204p_21 to 204p_2M are all turned off with respect to the first digital signal with M bits.

[0228] Note that the polarities of the first analog signal and the second analog signal can be different from each other. For example, in order to differentiate the potentials, the positive second voltage group is input to the wiring group 112n_2 and the negative second voltage group is input to the wiring group 112p_2.

[0229] Note that as the logic circuits 203p_1 to 203p_M and the logic circuits 203n_1 to 203n_M, for example, one of AND circuits, OR circuits, NAND circuits, NOR circuits, XOR circuits, XNOR circuits, and the like, or combinational circuits thereof can be used, like the logic circuits shown in FIG. 4A.

[0230] Note that as the switches 204p_11 to 204p_1M, the switches 204n_11 to 204n_1M, the switches 204p_21 to 204p_2M, and the switches 204n_21 to 204n_2M, for example, p-channel transistors, n-channel transistors, or CMOS switches in which p-channel transistors and n-channel transistors are combined can be used.

[0231] Note that although the case where the digital-analog converter portion 100 includes the plurality of logic circuits and the plurality of switches is described, this embodiment is not limited thereto. The digital-analog converter portion 100 may include a first logic circuit having $(N + 1)$ input terminals and one output terminal, a second logic circuit having $(N + 1)$ input terminals and one output terminal, a first switch, a second switch, a third switch, and a fourth switch. In the first logic circuit, a j th (j is one of 1 to N) input terminal is connected to the first wiring or the second wiring, the $(N + 1)$ th input terminal is connected to the third wiring, and the output terminal is connected to a control terminal of the first switch and a control terminal of the second switch. In the second logic circuit, a j th input terminal is connected to the first wiring or the second wiring, the $(N + 1)$ th input terminal is connected to the fourth wiring, and the output terminal is connected to a control terminal of the third switch and a control terminal of the fourth switch. The first terminal of the first switch is connected to the fifth wiring and a second terminal of the first switch is connected to the sixth wiring. A first terminal of the second switch is connected to a seventh wiring and a second terminal of the second switch is connected to an eighth wiring. A first terminal of the third switch is connected to a ninth wiring, a second terminal of the third switch is connected to a tenth wiring, a first terminal of the fourth switch is connected to the tenth wiring, and the second terminal of the fourth switch is connected to the eighth wiring.

[0232] Note that the first wiring, the second wiring, the third wiring, the fourth wiring, the fifth wiring, the sixth wiring, the seventh wiring, the eighth wiring, the ninth wiring, and the tenth wiring correspond to one of the wiring group 111, one of the wiring group 114, the wiring 115, the wiring 116, one of the wiring group 112p_1, the wiring 113_1, one of the wiring group 112p_2, the wiring 113_2, one of the wiring group 112n_1, and one of the wiring group 112n_2, respectively.

[0233] Note that the first logic circuit, the second logic circuit, the first switch, the second switch, the third switch, and the fourth switch correspond to one of the plurality of logic circuits 203p_1 to 203p_M, one of the logic circuits 203n_1 to 203n_M, one of the switches 204p_11 to 204p_1M, one of the switches 204p_21 to 204p_2M, one of the switches 204n_11 to 204n_1M, and one of the switches 204n_21 to 204n_2M, respectively.

[0234] As described above, since the digital-analog converter portion of this embodiment can convert one digital signal into a plurality of analog signals, a look-up table can be unnecessary. Therefore, heat generation or an increase in power consumption, or the like due to reading a look-up table from a memory element can be prevented.

[0235] Further, for example, in the case where a video signal is generated in a display device by using the digital-analog converter portion of this embodiment, a portion for generating the video signal and a pixel portion can be formed over the same substrate. Accordingly, since the number of connection between a panel and an external component can be reduced, poor connection in the connection portion of the panel and the external component can be suppressed, whereby improvement in reliability, an increase in yield, reduction in production cost high-definition, or the like can be achieved.

(Embodiment 4)

[0236] In this embodiment, one example of the digital-analog converter portion 100 which can separately set the polarities analog signals by a method different from that of Embodiment 3 will be described with reference to FIG. 8A.

[0237] The digital-analog converter portion 100 in this embodiment has a first mode and a second mode, as in Embodiment 3.

[0238] The digital-analog converter portion 100 includes the circuit 201, the circuit 202p_1, the circuit 202n_1, the circuit 202p_2, the circuit 202n_2, a circuit 400_1, and a circuit 400_2.

[0239] The circuit 201 is connected to the wiring group 111 and the wiring group 114. The circuit 202p_1 is connected to the wiring group 112p_1, a wiring 411p_1, and the output terminal of the circuit 201. The circuit 202n_1 is connected to the wiring group 112n_1, a wiring 411n_1, and the output terminal of the circuit 201. The circuit 202p_2 is connected to the wiring group 112p_2, a wiring 411p_2, and the output terminal of the circuit 201. The

circuit 202n_2 is connected to the wiring group 112n_2, a wiring 411n_2, and the output terminal of the circuit 201. The circuit 400_1 is connected to the wiring 411p_1, the wiring 411n_1, the wiring 113_1, the wiring 115, and the wiring 116. The circuit 400_2 is connected to the wiring 411p_2, the wiring 411n_2, the wiring 113_2, the wiring 115, and the wiring 116.

[0240] Next, the operation of the digital-analog converter portion 100 shown in FIG. 8A will be described.

[0241] A digital signal with N bits and an inverted digital signal with N bits are input to the circuit 201.

[0242] As in FIG. 4A, the circuit 201 generates a digital signal with M bits in accordance with the digital signal with N bits and the inverted signal with N bits.

[0243] After that, the circuit 201 input the digital signal with M bits to the circuit 202p_1, the circuit 202n_1, the circuit 202p_2, and the circuit 202n_2 to control the circuit 202p_1, the circuit 202n_1, the circuit 202p_2, and the circuit 202n_2.

[0244] In accordance with the digital signal with M bits, the circuit 202p_1 brings one of the wiring group 112p_1 and the wiring 411p_1 into conduction, and the potentials thereof are made to be approximately equal. With respect to the digital signal with M bits, the circuit 202n_1 brings one of the wiring group 112n_1 and the wiring 411n_1 into conduction, and the potentials thereof are made to be approximately the same. With respect to the digital signal with M bits, the circuit 202p_2 brings one of the wiring group 112p_2 and the wiring 411p_2 into conduction, and the potentials thereof are made to be approximately the same. With respect to the digital signal with M bits, the circuit 202n_2 brings one of the wiring group 112n_2 and the wiring 411n_2 into conduction, and the potentials thereof are made to be approximately the same.

[0245] In this manner, one of the positive first voltage group is input from the circuit 202p_1 to the circuit 400_1 through the wiring 411p_1, and one of the negative first voltage group is input from the circuit 202n_1 to the circuit 400_1 through the wiring 411n_1. At the same time, one of the positive second voltage group is input from the circuit 202p_2 to the circuit 400_2 through the wiring 411p_2, and one of the negative second voltage group is input from the circuit 202n_2 to the circuit 400_2 through the wiring 411n_2.

[0246] Then, in accordance with a selecting signal and an inverted selecting signal, the circuit 400_1 outputs one of the positive first voltage group or one of the negative first voltage group to the wiring 113_1 as a first analog signal. With respect to the selecting signal and the inverted selecting signal, in the first mode, the circuit 400_1 brings the wiring 411p_1 and the wiring 113_1 into conduction, and the potentials thereof are made to be the same, for example. In this manner, one of the positive first voltage group is output to the wiring 113_1 as a positive first analog signal. On the other hand, with respect to the selecting signal and the inverted selecting signal, in the second mode, the circuit 400_1 brings the

wiring 411n_1 and the wiring 113_1 into conduction, and the potentials thereof are made to be the same, for example. In this manner, one of the negative first voltage group is output to the wiring 113_1 as a negative first analog signal.

[0247] Further, with respect to a selecting signal and an inverted selecting signal, the circuit 400_2 outputs one of the positive second voltage group or one of the negative second voltage group to the wiring 113_2 as a second analog signal. With respect to the selecting signal and the inverted selecting signal, in the first mode, the circuit 400_2 brings the wiring 411p_2 and the wiring 113_2 into conduction, and the potentials thereof are made to be the same, for example. In this manner, one of the positive second voltage group is output to the wiring 113_2 as a positive second analog signal. On the other hand, with respect to the selecting signal and the inverted selecting signal, in the second mode, the circuit 400_2 brings the wiring 411n_2 and the wiring 113_2 into conduction, and the potentials thereof are made to be approximately the same, for example. In this manner, one of the negative second voltage group is output to the wiring 113_2 as a negative second analog signal.

[0248] Note that as specific examples of the circuit 400_1 and the circuit 400_2, circuits shown in FIG. 8B can be used. The circuit 400_1 includes a switch 401 and a switch 402, and the circuit 400_2 includes a switch 403 and a switch 404. A first terminal of the switch 401 is connected to the wiring 411p_1, a second terminal of the switch 401 is connected to the wiring 113_1, and a control terminal of the switch 401 is connected to the wiring 115. A first terminal of the switch 402 is connected to the wiring 411n_1, a second terminal of the switch 402 is connected to the wiring 113_1, and a control terminal of the switch 402 is connected to the wiring 116. A first terminal of the switch 403 is connected to the wiring 411p_2, a second terminal of the switch 403 is connected to the wiring 113_2, and a control terminal of the switch 403 is connected to the wiring 115. A first terminal of the switch 404 is connected to the wiring 411n_2, a second terminal of the switch 404 is connected to the wiring 113_2, and a control terminal of the switch 404 is connected to the wiring 116.

[0249] The operation of the circuit 400_1 and the circuit 400_2 will be described.

[0250] In the first mode, the switch 401 is turned on in response to the selecting signal and brings the wiring 411p_1 and the wiring 113_1 into conduction, and the potentials thereof are made to be the same. At the same time, the switch 403 is turned on with respect to the selecting signal and brings the wiring 411p_2 and the wiring 113_2 into conduction, and the potentials thereof are made to be the same. At that time, the switch 402 and the switch 404 are turned off with respect to the inverted selecting signal.

[0251] On the other hand, in the second mode, the switch 402 is turned on with respect to the inverted selecting signal and brings the wiring 411n_1 and the wiring

113_1 into conduction, so that the potentials thereof are made to be the same. At the same time, the switch 404 is turned on with respect to the inverted selecting signal and brings the wiring 411n_2 and the wiring 113_2 into conduction, so that the potentials thereof are made to be the same. At that time, the switch 401 and the switch 403 are turned off with respect to the selecting signal.

[0252] Note that in order to make the polarities of the first analog signal and the second analog signal different from each other, the control terminal of the switch 403 can be connected to the wiring 116 and the control terminal of the switch 404 can be connected to the wiring 115.

[0253] Note that as the switches 401, 402, 403, and 404, p-channel transistors, n-channel transistors, or CMOS switches in which n-channel transistors and p-channel transistors are combined can be used. Note that gate, a first terminal (one of source and drain), and a second terminal (the other of source and drain) of each transistor correspond to the control terminal, the first terminal, and the second terminal of each of the switches, respectively, and have the same connection structure.

[0254] In specific, as shown in FIG 8C, as the switches 401, 402, 403, and 404, a transistor 401a, a transistor 402a, a transistor 403a, and a transistor 404a are preferably used, respectively. The transistor 401 a and the transistor 403a are p-channel transistors and the transistor 402a and the transistor 404a are n-channel transistors. Further, control terminals of the transistor 401a, 402a, 403a, and 404a are all connected to the same wiring (the wiring 116 in FIG 8C). Accordingly, one of the wiring 115 and the wiring 116 can be omitted.

[0255] Here, since a positive voltage is input to a first terminal of the transistor 401 a and a first terminal of the transistor 403a, the potentials thereof are high. Since the transistor 401a and the transistor 403a are p-channel transistors, the absolute value of a potential difference (V_{gs}) between gate and source of each of the transistor 401a and the transistor 403a is large. Accordingly, the size (e.g., channel width W) of each of the transistor 401a and the transistor 403a can be small. On the other hand, since a negative voltage is input to a first terminal of the transistor 402a and a first terminal of the transistor 404a, the potentials thereof become low. Since the transistor 402a and the transistor 404a are n-channel transistors, a potential difference (V_{gs}) between gate and source of each of the transistor 402a and the transistor 404a becomes large. Accordingly, the size (e.g., channel width W) of each of the transistor 402a and the transistor 404a can be small.

[0256] Note that in order to make switching noise of the first analog signal approximately the same as that of the second analog signal, for example, the ratio of W/L of the transistor 401a and the ratio of W/L of the transistor 403a are preferably the same. Accordingly, in the case where the digital-analog converter portion 100 shown in FIG 8C is used for a display device, the first subpixel and a second subpixel express gray levels in accordance with

respective signals with approximately the same switching noise. Therefore, the effect due to the switching noise of the analog signals can be suppressed. However, this embodiment is not limited to this.

[0257] Note that for example, the ratio of W/L of the transistor 402a and the ratio of W/L of the transistor 404a are preferably the same, like the transistor 401a and the transistor 403a. However, this embodiment is not limited to this.

[0258] Note that in the case where the circuits 202p_1, 202n_1, 202p_2, and 202n_2 each includes a transistor, the ratio of W/L of the transistor is preferably lower than the ratios of W/L of the transistors 401a to 404a. However, this embodiment is not limited to this.

[0259] As described above, since the digital-analog converter portion of this embodiment can convert one digital signal into a plurality of analog signals, a look-up table can be unnecessary. Therefore, heat generation or an increase in power consumption, or the like due to reading a look-up table from a memory element can be prevented.

[0260] Further, for example, in the case where a video signal is generated in a display device by using the digital-analog converter portion of this embodiment, a portion for generating the video signal and a pixel portion can be formed over the same substrate. Accordingly, since the number of connection between a panel and an external component can be reduced, poor connection in the connection portion of the panel and the external component can be suppressed, whereby improvement in reliability, an increase in yield, reduction in production cost, high-definition, or the like can be achieved.

(Embodiment 5)

[0261] In this embodiment, the case where the digital-analog converter portion 100 described in Embodiments 1 to 4 is used for a display device will be described. Note that for example, the case where a digital-analog converter portion which converts one digital signal into two analog signals will be described with reference to FIG. 9A.

[0262] The display device includes a pixel 502 which includes the digital-analog converter portion 100, a circuit 501_1, a circuit 501_2, a first subpixel 502_1, and a second subpixel 502_2.

[0263] The digital-analog converter portion 100 is connected to the wiring group 111, the wiring group 112_1, the wiring group 112_2, the wiring group 113_1, and the wiring group 113_2. The circuit 501_1 is connected to the wiring group 112_1. The circuit 501_2 is connected to the wiring group 112_2. The first subpixel 502_1 is connected to the wiring group 113_1. The second subpixel 502_2 is connected to the wiring group 113_2.

[0264] The circuit 501_1 generates a plurality of voltages and inputs the plurality of voltages to the digital-analog converter portion 100 through the wiring group 112_1. The circuit 501_2 generates a plurality of voltages

and input the plurality of voltages to the digital-analog converter portion 100 through the wiring group 112_2.

[0265] Note that the plurality of voltages generated by the circuit 501_1 corresponds to the first voltage group and the plurality of voltages generated by the circuit 501_2 corresponds to the second voltage group.

[0266] Note that the circuit 501_1 and the circuit 501_2 can function as a first reference driver and a second reference driver, respectively.

[0267] As described in Embodiments 1 to 4, the digital-analog converter portion 100 generates a first analog signal and a second analog signal in accordance with a digital signal with N bits, an output voltage (e.g., the first voltage group) of the circuit 501_1, and an output voltage (e.g., the second voltage group) of the circuit 501_2. Then, the first analog signal is input to the first subpixel 502_1 through the wiring 113_1, so that the gray level of the first subpixel 502_1 is controlled. The second analog signal is input to the second subpixel 502_2 through the wiring 113_2, so that the gray level of the second subpixel 502_2 is controlled.

[0268] The first subpixel 502_1 expresses a gray level with respect to the first analog signal and the second subpixel 502_2 expresses a gray level with respect to the second analog signal. For example, in the case where the first subpixel 502_1 and the second subpixel 502_2 each include a liquid crystal element, the orientation of the liquid crystal element included in the first subpixel 502_1 is changed in accordance with the first analog signal, whereby the transmittance of the liquid crystal element is changed. Similarly, the orientation of the liquid crystal element included in the second subpixel 502_2 is changed in accordance with the second analog signal, whereby the transmittance of the liquid crystal element is changed. For example, in the case where the values of the first analog signal and the second analog signal are different from each other, the orientation state of the liquid crystal element included in the first subpixel 502_1 and the orientation state of the liquid crystal element included in the second subpixel 502_2 are different from each other. Accordingly, improvement in viewing angle characteristics can be achieved.

[0269] Note that a variety of circuits can be used for the circuit 501_1 and the circuit 501_2 as long as the circuit has a structure which is capable of generating a plurality of voltages. For example, a structure in which a plurality of resistor elements is connected in series can be employed. In examples shown in FIGS. 9B and 9C, the circuit 501_1 includes a plurality of resistor elements of resistor elements 501_11 to 501_1M, and the circuit 501_2 includes a plurality of resistor elements of resistor elements 501_21 to 501_2M. The resistor elements 501_11 to 501_1M are connected in series between a power supply V1 and a power supply V2. The resistor elements 501_21 to 501_2M are connected in series between a power supply V3 and a power supply V4. The resistor elements 501_11 to 501_1M generate a plurality of voltages (the first voltage group) by dividing a voltage

supplied from the power supply V1 and a voltage supplied from the power supply V2. The resistor elements 501_21 to 501_2M generate a plurality of voltages (the second voltage group) by dividing a voltage supplied from the power supply V3 and a voltage supplied from the power supply V4. The first voltage group and the second voltage group depend on the resistance value of a resistor element and a power supply voltage.

[0270] Note that in order to reduce the number of power supply and wirings, the circuit 501_1 and the circuit 501_2 can share a power supplies, for example. In a specific example, in the case where the power supply V1 and the power supply V3 are shared, the resistor elements 501_11 to 501_1M are connected in series between the power supply V1 and the power supply V2. Then, the resistor element 501_21 to 501_2M are connected in series between the power supply V1 and the power supply V4.

[0271] Note that in order to freely set the characteristics of the first voltage group, one of the resistor elements 501_11 to 501_1M or some of them can be variable resistor elements, for example. Similarly, in order to freely set the characteristics of the second voltage group, one of the resistor elements 501_21 to 501_2M or some of them can be variable resistor elements, for example.

[0272] Note that in order to freely set the characteristics of the first voltage group and the second voltage group, a voltage of the power supply V1, a voltage of the power supply V2, a voltage of the power supply V3, or a voltage of the power supply V4 can be a variable power supply. As an example, a variable power supply which selects any one of a plurality of power supplies can be given. Each of the plurality of power supplies is connected to a resistor element (e.g., the resistor element 501_11) through a switch. Then, by controlling on and off of each switch, a voltage to be supplied is controlled.

[0273] Note that in the case where the polarity of the first analog signal and the polarity of the second analog signal are separately set, a circuit 501p_1 which generates a positive first voltage group, a circuit 501n_1 which generates a negative second voltage group, a circuit 501p_2 which generates a positive first voltage group, and a circuit 501n_2 which generates a negative second voltage group are used, as shown in one example in FIG. 10A. For example, like the circuit 501_1 or the circuit 501_2 shown in FIGS. 9B and 9C, each of such circuits has a structure in which a plurality of resistor elements is connected in series between two power supplies. Note that in order to output a positive voltage group, for example, at least one of power supply voltages used for the circuit 501p_1 and the circuit 501p_2 is preferably made to be higher than a common voltage. On the other hand, in order to output a negative voltage group, for example, at least one of power supply voltages used for the circuit 501n_1 and the circuit 501n_2 is preferably made to be lower than the common voltage.

[0274] Note that the circuit 501p_1 and the circuit 501n_1 can be collectively denoted as the circuit 501_1

and the circuit 501p_2 and the circuit 501n_2 can be collectively denoted as the circuit 501_2. In this case, for example, the circuit 501_1 and the circuit 501_2 each generate both of the positive voltage group and the negative voltage group.

[0275] Note that in the case where a digital signal with N bits is converted into n analog signals, the circuits 501_1 to 501_n are used as shown in one example in FIG. 10B. The circuits 501_1 to 501_n each generate a plurality of voltages and output the plurality of voltages to the digital-analog converter portion 100. For example, like the circuit 501_1 or the circuit 501_2 shown in FIGS. 9B and 9C, each of the circuits 501_1 to 501_n has a structure in which a plurality of resistor elements is connected in series between two power supplies. The digital-analog converter portion 100 generates the n analog signals in accordance with n voltage groups and the digital signal with N bits. Then, the digital-analog converter portion 100 input the n analog signals to n subpixels 502_1 to 502_n. For example, an i th (i is one of 1 to n) analog signal is output to a subpixel 502_i.

[0276] Next, one example of a display device in more detail than that shown in FIG. 9A will be described with reference to FIG. 11A.

[0277] The display device includes a signal line driver circuit 601, a scanning line driver circuit 602, a pixel portion 603, the circuit 501_1, and the circuit 501_2. The signal line driver circuit 601 includes a shift register 621, a first latch portion 622, a second latch portion 623, a plurality of digital-analog converter portions 100, and a buffer portion 625. The pixel portion 603 includes a plurality of pixels 605. The plurality of pixels 605 each includes a first subpixel 606a and a second subpixel 606b. The first subpixel 606a and the second subpixel 606b each has means for storing a signal written.

[0278] First signal lines S1_1 to S1_m and second signal lines S2_1 to S2_m are provided by being extended from the signal line driver circuit 601 in column direction. Scanning lines G1 to G n are provided by being extended from the scanning driver circuit 602 in row direction.

[0279] Note that the first signal lines S1_1 to S1_m, the second signal lines S2_1 to S2_m, and the scanning lines G1 to G n can function as first signal lines, second signal lines, and third signal lines.

[0280] Note that a new wiring such as a capacitor line, a power supply line, a new scanning line, or a new signal line can be additionally provided, depending on the structure of the pixel. For example, the capacitor line is provided in parallel with the scanning lines G1 to G n and a certain level of voltage is applied to the capacitor line in many cases. However, a signal is input to the capacitor line in some cases.

[0281] The pixels 605 are provided in matrix corresponding to the first signal lines S1_1 to S1_m, the second signal lines S2_1 to S2_m, and the scanning lines G1 to G n , respectively. The first subpixel 606a is connected to a first signal line S1_j (one of the first signal lines S1_1 to S1_m) and a scanning line Gi (one of the

scanning lines G_1 to G_n). The second subpixel 606b is connected to a second signal line S_{2_j} (any one of the second signal lines S_{2_1} to S_{2_m}) and a scanning line G_i (any one of the scanning lines G_1 to G_n).

[0282] A start pulse (SSP), a clock signal (SCK), and an inverted clock signal (SCKB) are input to the shift register 621. The shift register 621 outputs a sampling pulse to the first latch portion 622 in accordance with such a signal.

[0283] Note that as the shift register 621, for example, a counter, a decoder, or the like can be used as long as it can output a sampling pulse.

[0284] The sampling pulse and a video signal (Vdata) are input to the first latch portion 622. The first latch portion 622 sequentially stores a video signal in each column in accordance with the sampling pulse. When storing of a video signal in the last column is finished, the first latch portion 622 outputs the stored video signals in respective columns to the second latch portion 623 all at one time. Note that the video signal (Vdata) corresponds to the digital signal with N bits described in Embodiments 1 to 4.

[0285] The video signals and a latch pulse (LAT_Pulse) are input to the second latch portion 623 from the first latch portion 622. The second latch portion 623 stores the video signals input from the first latch portion 622 all at one time in accordance with the latch pulse. After that, the second latch portion 623 outputs the video signals to the plurality of digital-analog converter portion 100 all at one time.

[0286] Note that for example, by using an output signal, a start pulse, or the like of the shift register as a latch pulse, the latch pulse can be omitted.

[0287] Note that a video signal output from each column of the second latch portion 623 in each column corresponds to, for example, the digital signal with N bits described in Embodiments 1 to 4.

[0288] The plurality of analog converter portion 100 each convert a video signal into a first analog signal and a second analog signal as described in Embodiments 1 to 4. Then, the plurality of digital-analog converter portion 100 each write the first analog signal to the first subpixel 502_1 through the buffer portion 625 and the second analog signal to the second subpixel 502_2 through the buffer portion 625.

[0289] Here, in order to make the amplitude voltage of the video signal low, for example, the first latch portion 622 and/or the second latch portion 623 can have a level-shift function or a level shifter. In this case, the amplitude voltage of the video signal input to the first latch portion 622 is, for example, lower than that of the video signal output from each column of the first latch portion 622 in each column or that of the video signal output from the second latch portion 623 in each column. Accordingly, for example, the driving voltage of the shift register 621, the first latch portion 622, or the second latch portion 623 can be low, whereby reduction in power consumption can be achieved.

[0290] Next, one example of the operation of the dis-

play device will be described with reference to FIG. 11B. One example of a timing chart in FIG 11B shows one frame period corresponding to a period when an image of one screen is displayed. In this one frame period, rows of pixels are sequentially selected from first to n th rows. The cycle of one frame period is desirably equal to or less than 1/60 sec. (equal to or more than 60 Hz) so that flickering is not sensed by a viewer of an image. The cycle of one frame period is more desirably equal to or less than 1/120 sec. (frequency is equal to or more than 120 Hz). The cycle of one frame period is still more desirably equal to or less than 1/180 sec. (frequency is equal to or more than 180 Hz). However, in the case where a frame frequency is high, a frame frequency in the display device and the frame frequency of original image data do not correspond to each other in some cases. Therefore, image data needs to be compensated. For example, the image data is compensated by detecting a motion vector. Thus, display with a high frame frequency can be performed. In this manner, the motion of the image is smoothly displayed and display with a few afterimages can be performed.

[0291] The scanning line driver circuit 602 outputs scanning signals to the scanning lines G_1 to G_n in response to a start pulse (GSP), a clock signal (GCK), and an inverted clock signal (GCKB). The first to n th rows of the pixels are sequentially selected in accordance with the scanning signals. A video signal can be written to the pixels in the selected row. Every time the row of these pixels is selected, the signal line driver circuit 601 writes the first analog signal to the first subpixel 606a and the second analog signal to the second subpixel 606a. Note that a period when the pixels in one row are selected is referred to as one gate selecting period.

[0292] As described above, since each of the digital-analog converter portions 100 in the display device shown in FIG 11A can convert one digital signal into a plurality of analog signals, the amount of data of a video signal does not increase even though the pixel is divided into a plurality of subpixels. Accordingly, the scale of the circuits for processing a video signal (e.g., the shift register, the first latch portion, and the second latch portion) can be small.

[0293] Further, in the display device shown in FIG. 11A, since a look-up table, that is, a memory portion is not necessary for converting one digital signal into the plurality of analog signals, the pixel portion and peripheral circuits thereof (e.g., the signal line driver circuit, the scanning line driver circuit, and the reference driver) can be easily formed over the same substrate.

[0294] Note that the structure of the signal line driver circuit 601 is not limited to the structure in FIG. 11A. For example, in the case where the current capability of the digital-analog converter portion 100 is high, the buffer portion 625 can be omitted. In another example, in the case where the voltage groups generated in the circuit 501_1 and the circuit 501_2 are input to the digital-analog converter portion 100 through a buffer, the buffer portion

625 can be omitted. For example, in the case where the number of voltages in the voltage group is smaller than the number of the signal lines, the number of buffers is reduced. Therefore, the voltage groups generated in the circuit 501_1 and the circuit 501_2 are preferably input to the digital-analog converter portion 100 through the buffer.

[0295] Note that in order to realize dot inversion drive in each pixel, one example of the signal line driver circuit shown in FIG 12A is used for the display device. For example, the positive first voltage group, the positive second voltage group, the negative first voltage group, and the negative second voltage group output from the circuit 501p_1, the circuit 501p_2, the circuit 501n_1, and the circuit 501n_2, respectively, which are described in FIG 10A are input to the plurality of digital-analog converter portion 100. Further, a selecting signal and an inverted selecting signal are input alternately to each column. Then, in the selecting signal and the inverted selecting signal, an H signal and an L signal alternate with each other in every single gate selecting period. Accordingly, for example, by using a clock signal (GCK) and an inverted clock signal (GCKB) as the selecting signal and the inverted selecting signal, the selecting signal and the inverted selecting signal can be omitted. In this manner, the dot inversion drive can be realized.

[0296] Note that although one example of the signal line driver circuit in the case where dot inversion drive in each pixel is realized is described in FIG. 12A, this embodiment is not limited to this. For example, dot inversion drive in each subpixel may be realized. In this case, as described in Embodiments 3 and 4, the polarities of the first video signal and the second video signal can be made different from each other by switching the positive first voltage group and the negative second voltage group to each other and inputting each of them to the digital-analog converter portions 100.

[0297] In another example, the selecting signal and the inverted selecting signal can be alternately input to every n columns. By switching an H signal and an L signal to each other in the selecting signal and the inverted selecting signal in every n gate selecting periods, dot inversion drive in every n pixels can be realized.

[0298] In another example, by switching an H signal and an L signal to each other in the selecting signal and the inverted selecting signal in every single frame period, source line inversion drive can be realized.

[0299] Next, one example in which the pixel 605 includes a liquid crystal element will be described with reference to FIG 12B. The pixel 605 includes the first subpixel 606a including a transistor 701a, a liquid crystal element 702a, and a capacitor element 703a and the second subpixel 606b having a transistor 701b, a liquid crystal element 702b, and a capacitor element 703b. A first terminal of the transistor 701a is connected to the signal line $S1_j$, a second terminal of the transistor 701a is connected to one electrode of the liquid crystal element 702a, and gate of the transistor 701a is connected to the

scanning line G_i . The capacitor element 703a is connected between the second terminal of the transistor 701a and a capacitor line 705. The other electrode of the liquid crystal element 702a corresponds to a common electrode 704. On the other hand, a first terminal of the transistor 701b is connected to the signal line $S2_j$, a second terminal of the transistor 701b is connected to one electrode of the liquid crystal element 702b, and gate of the transistor 701b is connected to the scanning line G_i . The capacitor element 703b is connected between the second terminal of the transistor 701b and a capacitor line 705. The other electrode of the liquid crystal element 702b corresponds to the common electrode 704.

[0300] For example, when an i th row is selected, an H signal is input to the scanning line G_i from the scanning line driver circuit 602, whereby the transistor 701a and the transistor 701b are turned on. Then, a first video signal is written to the first subpixel 606a from the signal line driver circuit 601 through the signal line $S1_j$ and a potential difference between the first video signal and the capacitor line 705 is stored in the capacitor element 703a. Then, the liquid crystal element 704a has a transmittance which is based on the first video signal and expresses a gray level which is based on the first video signal. At the same time, a second video signal is written to the second subpixel 606b from the signal line driver circuit 601 through the signal line $S2_j$ and a potential difference between the second video signal and the capacitor line 705 is stored in the capacitor element 703b. Then, the liquid crystal element 704b has a transmittance which is based on the second video signal and expresses a gray level which is based on the second video signal.

[0301] As described above, since the digital-analog converter portion of this embodiment can convert one digital signal into a plurality of analog signals by using the digital-analog converter portion described in Embodiments 1 to 4, a look-up table can be unnecessary. Therefore, heat generation, an increase in power consumption, or the like due to reading a look-up table from a memory element can be prevented.

[0302] Further, since a look-up table is not used, a portion for generating a video signal and a pixel portion can be formed over the same substrate. Accordingly, since the number of connection between a panel and an external component can be reduced, poor connection in the connection portion of the panel and the external component can be suppressed, whereby improvement in reliability, an increase in yield, reduction in production cost, high-definition, or the like can be achieved.

[0303] Further, the portion for generating the video signal and the pixel portion can be provided close together. Accordingly, a pathway through which the video signal is input to the pixel after the video signal is generated can be shortened. Therefore, noise generated in the video signal can be suppressed, so that display quality can be improved.

(Example 6)

[0304] Example 6 will describe a structure of a transistor.

[0305] FIG 13 is one example of cross-sectional view of transistors. However, the structure of the transistor is not limited to that shown in FIG 13 and a variety of structures can be employed.

[0306] Note that although FIG 13 shows one example of the cross-sectional view of the plurality of transistors juxtaposed, this is representation for describing the structure of the transistor. Therefore, the transistors are not needed to be actually juxtaposed as shown in FIG 13 and can be separately formed as needed.

[0307] A transistor 5051 is one example of a single-drain transistor. A transistor 5052 is one example of a transistor having an angle which is tapered at a certain degrees or more in a gate electrode 5063. A transistor 5053 is one example of a transistor in which the gate electrode 5063 includes at least two layers and a lower gate electrode is longer than an upper gate electrode. A transistor 5054 is one example of a transistor including side walls 5066 which are in contact with the side surfaces of the gate electrode 5063. A transistor 5055 is one example of a transistor in which an LDD (Loff) region is formed in a semiconductor layer by doping with the use of a mask.

[0308] Then, layers constituting a transistor are each described.

[0309] As one example of a substrate 5057, a glass substrate made of barium borosilicate glass, aluminoborosilicate glass, or the like, a quartz substrate, a ceramic substrate, a metal substrate such as a stainless steel substrate, and the like can be given. Alternatively, a flexible synthetic resin such as plastic typified by polyethylene terephthalate (PET), polyethylene naphthalate (PEN), polyether sulfone (PES), and acrylic, or the like can be used.

[0310] An insulating film 5058 serves as a base film. As one example of the insulating film 5058, a single-layer structure or a layered structure of an insulating film containing oxygen or nitrogen, such as silicon oxide (SiOx), silicon nitride (SiNx), silicon oxynitride (SiOxNy) ($x > y$), or silicon nitride oxide (SiNxOy) ($x > y$) can be given. In one example in the case where the insulating film 5058 is formed to have a two-layer structure, a silicon nitride oxide film and a silicon oxynitride film can be formed as a first insulating film and a second insulating film, respectively. In another example, in the case where the insulating film 5058 has a three-layer structure, a silicon oxynitride film, a silicon nitride oxide film, and a silicon oxynitride film can be formed as a first insulating film, a second insulating film, and a third insulating film, respectively.

[0311] As an example of each of a semiconductor layer 5059, a semiconductor layer 5060, and a semiconductor layer 5061, an amorphous semiconductor, a microcrystalline semiconductor, a semi-amorphous semiconductor (SAS), a polycrystalline semiconductor, a single-crys-

tal semiconductor, or the like can be given.

[0312] Note that the semiconductor layer 5059, the semiconductor layer 5060, and the semiconductor layer 5061 preferably have impurity concentrations which are different from each other. For example, the semiconductor layer 5059, the semiconductor layer 5060, and the semiconductor layer 5061 function as a channel region, a lightly doped drain (LDD) region, and source and drain regions, respectively.

[0313] Like the insulating film 5058, the insulating film 5062 has, for example, a single-layer structure or a layered structure of an insulating film containing oxygen or nitrogen, such as silicon oxide (SiOx), silicon nitride (SiNx), silicon oxynitride (SiOxNy) ($x > y$), or silicon nitride oxide (SiNxOy) ($x > y$).

[0314] As one example of the gate electrode 5063, a single-layer conductive film or an accumulated structure of a multi-layer (e.g., two-layer or three-layer) conductive film can be given. As one example of a conductive film used for the gate electrode 5063, a single film of an element such as tantalum (Ta), titanium (Ti), molybdenum (Mo), tungsten (W), chromium (Cr), silicon (Si), or the like; a nitride film containing the aforementioned element (typically, a tantalum nitride film, a tungsten nitride film, or a titanium nitride film); an alloy film in which the aforementioned elements are combined (typically, a Mo-W alloy or a Mo-Ta alloy); a silicide film containing the aforementioned element (typically, a tungsten silicide film or a titanium silicide film); and the like can be used.

[0315] Note that the aforementioned single element film, nitride film, alloy film, silicide film, or the like can have a single-layer structure or a layered structure.

[0316] As one example of an insulating film 5064, a single-layer structure or a layered structure of an insulating film containing oxygen or nitrogen, such as silicon oxide (SiOx), silicon nitride (SiNx), silicon oxynitride (SiOxNy) ($x > y$), or silicon nitride oxide (SiNxOy) ($x > y$); or a film containing carbon, such as DLC (diamond like carbon) can be given.

[0317] As one example of an insulating film 5065, a siloxane resin is given. Alternatively, an insulating film containing oxygen or nitrogen such as silicon oxide (SiOx), silicon nitride (SiNx), silicon oxynitride (SiOxNy), ($x > y$), or silicon nitride oxide (SiNxOy) ($x > y$) is given. Alternatively, a film containing carbon, such as DLC (Diamond Like Carbon) is given. Alternatively, an organic material such as epoxy, polyimide, polyamide, polyvinylphenol, benzocyclobutene, or acrylic is given. Alternatively, a single-layer structure or a layered structure thereof is given.

[0318] As one example of a siloxane resin, a resin including a Si-O-Si bond is given. For example, siloxane includes a skeleton structure of a bond between silicon (Si) and oxygen (O). An organic group containing at least hydrogen (for example, an alkyl group and aromatic hydrocarbon) is used as a substituent. A fluoro group may be included in the organic group.

[0319] Note that the insulating film 5065 can be pro-

vided to cover the gate electrode 5063 directly without providing the insulating film 5064.

[0320] As one example of a conductive film 5067, a single-layer conductive film or an accumulated structure of a multi-layer (e.g., two-layer or three-layer) conductive film can be given. Examples of a material for the conductive film 5067 include a single element film of an element such as Al, Ni, C, W, Mo, Ti, Pt, Cu, Ta, Au, or Mn, a nitride film of any of the elements, an alloy film in which any of the elements are combined, a silicide film of any of the elements, and the like. As one example of an alloy film in which any of the elements are combined, an Al alloy containing C and Ti, an Al alloy containing Ni, an Al alloy containing C and Ni, an Al alloy containing C and Mn, or the like is given.

[0321] Note that in the case where the above-described conductive film is formed to have a layered structure, for example, a structure in which Al is sandwiched between Mo, Ti, or the like is preferable. Accordingly, the resistance of Al to heat or a chemical reaction can be enhanced.

[0322] As one example of the sidewalls 5066, silicon oxide (SiO_x) or silicon nitride (SiN_x) can be used.

[0323] In this manner, the structure of the transistor described in this example can be employed for the transistor included in the digital-analog converter portion described in Embodiments 1 to 4. The digital-analog converter portion described in Embodiments 1 to 4 can generate signals corresponding to respective subpixels without using a look-up table. Therefore, heat generation, an increase in power consumption, or the like due to reading a look-up table from a memory element can be prevented.

[0324] Further, since a look-up table is not used, a portion for generating a video signal and a pixel portion can be formed over the same substrate. Accordingly, since the number of connection between a panel and an external component can be reduced, improvement in reliability, an increase in yield, reduction in cost, high-definition, or the like can be achieved.

(Example 7)

[0325] In this example, one example of a formation method of a semiconductor layer will be described. The formation method of the semiconductor layer in this example can be employed for the structure and the manufacturing method of the transistor described in Embodiment 4.

[0326] FIG 14A shows an SOI substrate. In FIG. 14A, a base substrate 9200 is a substrate having an insulating surface or an insulating substrate, and a variety of glass substrates that are used in the electronics industry, such as aluminosilicate glass, aluminoborosilicate glass, or barium borosilicate glass, can be used. Alternatively, a quartz glass substrate or a semiconductor substrate such as a silicon wafer can be used. An SOI layer 9202 is a single-crystal semiconductor, and single-crystal silicon is typically applied thereto. Alternatively, a crystalline

semiconductor layer which is formed using silicon, germanium, or a compound semiconductor such as indium phosphide or gallium arsenide, which can be separated from a single-crystal semiconductor substrate or a polycrystalline semiconductor substrate using a hydrogen ion implantation separation method, may be applied.

[0327] Between the base substrate 9200 and the SOI layer 9202 described above, a bonding layer 9204 which has a smooth surface and forms a hydrophilic surface is provided. A silicon oxide film is suitable for the bonding layer 9204. In particular, a silicon oxide film formed by a chemical vapor deposition method using an organosilane gas is preferable. As an organosilane gas, a silicon-containing compound such as tetraethoxysilane (TEOS) (chemical formula: Si(OC₂H₅)₄), tetramethylsilane (TMS) (chemical formula: Si(CH₃)₄), tetramethylcyclotetrasiloxane (TMCTS), octamethylcyclotetrasiloxane (OMCTS), hexamethyldisilazane (HMDS), triethoxysilane (chemical formula: SiH(OC₂H₅)₃), or trisdimethylaminosilane (chemical formula: SiH(N(CH₃)₂)₃) can be used.

[0328] The bonding layer 9204 which has a smooth surface and forms a hydrophilic surface is provided with a thickness of 5 to 500 nm. With such a thickness, roughness of a surface on which the bonding layer 9204 is formed can be smoothed and smoothness of a growth surface of the film can be ensured. In addition, distortion between the bonding substrate 9204 and a substrate to be bonded to the bonding substrate 9204 can be reduced. The base substrate 9200 may be provided with a similar silicon oxide film. That is, when the SOI layer 9202 is bonded to a substrate having an insulating surface or the insulating base substrate 9200, the base substrate 9200 and the SOI layer 9202 can be firmly bonded to each other when the bonding layer 9204 formed of a silicon oxide film which is preferably formed using organosilane as a material is provided on either one or both surfaces of the base substrate 9200 and the SOI layer 9202 which are to be bonded.

[0329] A method for manufacturing such an SOI substrate is described with reference to FIGS. 14B to 14E.

[0330] A semiconductor substrate 9201 shown in FIG 14B is cleaned, and ions which are accelerated by an electric field are introduced to reach a predetermined depth from the surface of the semiconductor substrate 9201 to form an ion doping layer 9203. Introduction of ions is conducted in consideration of the thickness of an SOI layer which is to be transferred to a base substrate. The thickness of the SOI layer is 5 to 500 nm, preferably 10 to 200 nm. Accelerating voltage for introducing ions into the semiconductor substrate 9201 is set in consideration of such a thickness. The ion doping layer 9203 is formed by introducing ions of hydrogen, helium, or halogen typified by fluorine. In this case, it is preferable to use one ion or plural ions formed of the same atoms which have different mass. In the case of introducing hydrogen ions, the hydrogen ions preferably include H⁺, H₂⁺, and H₃⁺ ions with a high percentage of H₃⁺ ions. In the case of introducing hydrogen ions, introducing efficiency can

be increased and introducing time can be shortened by making H^+ , H_2^+ , and H_3^+ ions contained and increasing the percentage of H_3^+ ions. With such a structure, separation can be easily performed.

[0331] In the case of introducing ions at a high dose, the surface of the semiconductor substrate 9201 is roughened in some cases. Therefore, a protective film against introduction of ions, such as a silicon nitride film, a silicon nitride oxide film, or the like with a thickness of 50 to 200 nm may be provided on a surface to which ions are introduced.

[0332] Next, as shown in FIG. 14C, a silicon oxide film is formed over a surface to which the base substrate is bonded as a bonding layer 9204. As the silicon oxide film, a silicon oxide film formed by a chemical vapor deposition method using an organosilane gas as described above is preferably used. Alternatively, a silicon oxide film formed by a chemical vapor deposition method using a silane gas can be used. In film formation by a chemical vapor deposition method, film formation temperature at, for example, 350 °C or lower, at which degassing of the ion doping layer 9203 formed in a single-crystal semiconductor substrate does not occur, is used. Heat treatment for separating an SOI layer from a single-crystal or polycrystalline semiconductor substrate is performed at a higher temperature than the film formation temperature.

[0333] FIG 14D shows a mode in which a surface of the base substrate 9200 and a surface of the semiconductor substrate 9201, on which the bonding layer 9204 is formed are disposed in contact to be bonded to each other. The surfaces which are to be bonded are cleaned sufficiently. Then, when the base substrate 9200 and the bonding layer 9204 are disposed in contact, a bond is formed. This bond is formed by Van der Waals forces. When the base substrate 9200 and the semiconductor substrate 9201 are pressed against each other, a stronger bond can be formed by hydrogen bonding.

[0334] In order to form a favorable bond, the surfaces may be activated. For example, the surfaces which are to form a bond are irradiated with an atomic beam or an ion beam. When an atomic beam or an ion beam is used, an inert gas neutral atom beam or inert gas ion beam of argon or the like can be used. Alternatively, plasma irradiation or radical treatment is performed. With such a surface treatment, a bond between different kinds of materials can be easily formed even at a temperature of 200 to 400 °C.

[0335] After the base substrate 9200 and the semiconductor substrate 9201 are bonded to each other with the bonding layer 9204 interposed therebetween, heat treatment or pressure treatment is preferably performed. When heat treatment or pressure treatment is performed, bonding strength can be increased. Temperature of heat treatment is preferably lower than or equal to the upper temperature limit of the base substrate 9200. Pressure treatment is performed so that pressure is applied in a perpendicular direction to the bonded surface, in consideration of pressure resistance of the base substrate 9200

and the semiconductor substrate 9201.

[0336] In FIG. 14E, after the base substrate 9200 and the semiconductor substrate 9201 are bonded to each other, heat treatment is performed to separate the semiconductor substrate 9201 from the base substrate 9200 with the ion doping layer 9203 used as a cleavage surface. The heat treatment is preferably performed at a temperature higher than or equal to the film formation temperature of the bonding layer 9204 and lower than or equal to the upper temperature limit of the base substrate 9200. When the heat treatment is performed at, for example, 400 to 600 °C, the volume of fine voids formed in the ion doping layer 9203 is changed, so that separation can be performed along the ion doping layer 9203. Since the bonding layer 9204 is bonded to the base substrate 9200, the SOI layer 9202 having the same crystallinity as the semiconductor substrate 9201 remains over the base substrate 9200.

[0337] In this manner, in accordance with this mode, even if a substrate with an upper temperature limit of 700 °C or lower, such as a glass substrate, is used as the base substrate 9200, the SOI layer 9202 having strong adhesiveness of a bonded portion can be obtained. As the base substrate 9200, various glass substrates which are used in the electronics industry and are referred to as non-alkali glass substrates, such as aluminosilicate glass substrates, aluminoborosilicate glass substrates, and barium borosilicate glass substrates can be used. That is, a single-crystal semiconductor layer can be formed over a substrate which is longer than one meter on a side. When such a large-area substrate is used, not only a display device such as a liquid crystal display but also a semiconductor integrated circuit can be manufactured.

[0338] The transistor formed using the above-described semiconductor layer can be formed over a substrate which transmits light, such as a glass substrate. Accordingly, the pixel portion of the display device and the digital-analog converter portion described in Embodiment 1 can be formed over the same substrate.

[0339] The transistor formed using the above-described semiconductor layer has high mobility and small variations in characteristics. Therefore, by manufacturing the digital-analog converter portion described in Embodiment 1 with the use of the transistor, the layout area of the digital-analog converter portion can be made to be small.

[0340] In this manner, the structure of the transistor described in this example can be employed for the transistor included in the digital-analog converter portion described in Embodiments 1 to 4. The digital-analog converter portion described in Embodiments 1 to 4 can generate signals corresponding to respective subpixels without using a look-up table. Therefore, heat generation, an increase in power consumption, or the like due to reading a look-up table from a memory element can be prevented.

[0341] Further, since a look-up table is not used, a portion for generating a video signal and a pixel portion can

be formed over the same substrate. Accordingly, since the number of connection between a panel and an external component can be reduced, improvement in reliability, an increase in yield, reduction in cost, high-definition, or the like can be achieved.

(Embodiment 8)

[0342] In this embodiment, examples of electronic devices will be described.

[0343] FIGS. 15A to 15H and FIGS. 16A to 16D are diagrams illustrating electronic devices. These electronic devices can each include a housing 5000, a display portion 5001, a speaker 5003, an LED lamp 5004, an operation key 5005, a connecting terminal 5006, a sensor 5007 (a sensor having a function of measuring force, displacement, position, speed, acceleration, angular velocity, rotational frequency, distance, light, liquid, magnetism, temperature, chemical substance, sound, time, hardness, electric field, current, voltage, electric power, radiation, flow rate, humidity, gradient, oscillation, odor, or infrared rays), a microphone 5008, and the like.

[0344] FIG. 15A is a mobile computer which can include a switch 5009, an infrared rays port 5010, and the like in addition to the above-described objects. FIG. 15B is a portable image reproducing device (e.g., a DVD reproducing device) provided with a memory medium which can include a second display portion 5002, a memory medium reading portion 5011, and the like in addition to the above-described objects. FIG. 15C is a goggle-type display which can include a second display portion 5002, a supporting portion 5012, an earphone 5013, and the like in addition to the above-described objects. FIG. 15D is a portable game machine which can include a memory medium reading portion 5011 and the like in addition to the above-described objects. FIG. 15E is a projector which can include a light source 5033, a projecting lens 5034, and the like in addition to the above-described objects. FIG. 15F is a portable game machine which can include a second display portion 5002, a memory medium reading portion 5011, and the like in addition to the above-described objects. FIG. 15G is a television receiver which can include a tuner, an image processing portion, and the like in addition to the above-described objects. FIG. 15H is a portable television receiver which can include a charger 5017 which can transmit and receive signals and the like in addition to the above-described objects. FIG. 16A is a display which can include a supporting board 5018 and the like in addition to the above-described objects. FIG. 16B is a camera which can include an external connecting port 5019, a shutter button 5015, an image receiver portion 5016, and the like in addition to the above-described objects. FIG. 16C is a computer which can include a pointing device 5020, an external connecting port 5019, a reader/writer 5021, and the like in addition to the above-described objects. FIG. 16D is a mobile phone which can include an antenna 5014, a tuner of one-segment partial reception service for mobile

phones and mobile stations, and the like in addition to the above-described objects.

[0345] The electronic devices shown in FIGS. 15A to 15H and FIGS. 16A to 16D can have a variety of functions. For example, a function of displaying a variety of information (a still image, a moving image, a text image, and the like) on a display portion, a touch panel function, a function of displaying a calendar, date, time, and the like, a function for controlling a process with a variety of software (programs), a wireless communication function, a function of being connected to a variety of computer networks with a wireless communication function, a function of transmitting and receiving a variety of data with a wireless communication function, a function of reading program or data stored in a memory medium and displaying the program or data on a display portion, and the like can be given. Further, the electronic device including a plurality of display portions can have a function of displaying image information mainly on one display portion while displaying text information on another display portion, a function of displaying a three-dimensional image by displaying images where parallax is considered on a plurality of display portions, or the like. Furthermore, the electronic device including an image receiver portion can have a function of shooting a still image, a function of shooting a moving image, a function of automatically or manually correcting a shot image, a function of storing a shot image in a memory medium (an external memory medium or a memory medium incorporated in the camera), a function of displaying a shot image on the display portion, or the like. Note that functions which can be provided for the electronic devices shown in FIGS. 15A to 15H and FIGS. 16A to 16D are not limited thereto, and the electronic devices can have a variety of functions.

[0346] The electronic devices described in this embodiment each include the display portion for displaying some sort of information. By using the display device described in Embodiment 5 for a display portion of an electronic device, improvement in viewing angle characteristics can be achieved. Since the display device described in Embodiment 5 can be driven with the small number of signals, the number of components of an electronic device can be reduced. Further, since the display device described in Embodiment 5 does not need a lookup table, an electronic device can be manufactured at low cost.

[0347] Next, applications of a semiconductor device will be described.

[0348] FIG. 16E shows an example in which a semiconductor device is provided so as to be integrated with a building. In FIG. 16E, a housing 5022, a display portion 5023, a remote controller device 5024 which is an operation portion, a speaker 5025, and the like are included. The semiconductor device is integrated with the building as a hung-on-wall type and can be provided without a large space for provision.

[0349] FIG. 16F shows another example in which a semiconductor device is provided so as to be integrated

within a building. The display panel 5026 is integrated with a prefabricated bath 5027, so that a person who takes a bath can watch the display panel 5026.

[0350] Note that although this embodiment gives the wall and the prefabricated bath as examples of the building, this embodiment is not limited to them and the semiconductor device can be provided in a variety of buildings.

[0351] Next, an example in which the semiconductor device is provided so as to be integrated with a moving body will be shown.

[0352] FIG 16G shows an example in which the semiconductor device is provided in a vehicle. A display panel 5028 is provided in a body 5029 of the vehicle and can display information input from the operation of the body or the outside of the body on demand. Note that the display panel 5028 may have a navigation function.

[0353] FIG 16H shows an example in which the semiconductor device is provided so as to be integrated with a passenger airplane. FIG 16H shows a usage pattern when a display panel 5031 is provided on a ceiling 5030 above a seat in the passenger airplane. The display panel 5031 is integrated with the ceiling 5030 through a hinge portion 5032, and a passenger can watch the display panel 5031 by extending and contracting the hinge portion 5032. The display panel 5031 has a function of displaying information when operated by the passenger.

[0354] Note that although this embodiment gives the body of the vehicle and the body of the plane as examples of the moving body, this embodiment is not limited thereto. The semiconductor device can be provided to a variety of moving bodies such as a two-wheel motor vehicle, a four-wheel vehicle (including a car, bus, and the like), a train (including a monorail, a railway, and the like), and a ship.

[0355] In this manner, the structure of the display device in the electronic device and the semiconductor device which are described in this embodiment can be employed for the display device provided with the digital-analog converter portion described in Embodiment 5. The digital-analog converter portion described in Embodiments 1 to 4 can generate signals corresponding to respective subpixels without using a look-up table. Therefore, heat generation or an increase in power consumption, or the like due to reading a look-up table from a memory element can be prevented.

[0356] Further, since a look-up table is not used, a portion for generating a video signal and a pixel portion can be formed over the same substrate. Accordingly, since the number of connection between a panel and an external component can be reduced, improvement in reliability, an increase in yield, reduction in cost, or high-definition can be achieved.

Claims

1. A display device comprising:

a plurality of pixels, wherein each pixel (502; 605) is divided into first to n th, n is a natural number of 2 or more, subpixels (502_1 to 502_n; 606a; 606b), wherein each of the first to n th subpixels (502_1 to 502_n; 606a; 606b) is provided with an electrode for driving a liquid crystal element;

n wiring groups (112_1 to 112_n) each supplying M , where M is a natural number of 2 or more, different voltages;

a plurality of first wiring groups (111), wherein a digital signal with N , where N is a natural number of 2 or more, bits is input into each said first wiring group (111);

a plurality of scanning lines (G_i);

a plurality of converter portions (100);

each converter portion (100) having a function to convert the respective digital signal into a first to n th analog signal, the converter portion (100) including first to n th circuits (101_1 to 101_n) each being connected to a respective wiring group (112_1 to 112_n) and having a function of:

converting the digital signal into an analog signal by using the M different voltages supplied from a respective wiring group (112_1 to 112_n), and

inputting the analog signal to the respective one of the first to n th subpixels (502_1 to 502_n; 606a; 606b) through the respective one of a first to n th wiring (113_1 to 113_n);

wherein each of the first to n th circuits (101_1 to 101_n) are connected to the respective first to n th wirings (113_1 to 113_n), the respective first to n th wirings being connected to respective first to n th subpixels (502_1 to 502_n; 606a; 606b);

wherein the first to n th subpixels (502_1 to 502_n; 606a; 606b) of each pixel are connected to a same scanning line (G_i);

the display device further comprising a signal line driver circuit (601) adapted to write each of the first to n th analog signals into a respective one of the first to n th subpixels (502_1 to 502_n; 606a; 606b) during one gate selecting period, wherein the signal line driver circuit comprises the plurality of converter portions;

wherein the first to n th wiring (113_1, ..., 113_n) are part of the display device.

2. A display device comprising:

a plurality of pixels, wherein each pixel (502; 605) is divided into first to n th, n is a natural number of 2 or more, subpixels (502_1 to 502_n; 606a; 606b), wherein each of the first to n th subpixels (502_1 to 502_n; 606a; 606b) is provided

with an electrode for driving a liquid crystal element;

n wiring groups (112_1 to 112_n) each supplying M , where M is a natural number of 2 or more, different voltages;

a plurality of first wiring groups (111), wherein a digital signal with N , where N is a natural number of 2 or more, bits is input into each said first wiring group (111);

a plurality of scanning lines (G_i);

a plurality of converter portions (100);

each converter portion (100) having a function to convert a respective digital signal into a first to n th analog signal and including a decoder circuit (201), wherein the decoder circuit has the function to decode the digital signal with N bits into a further digital signal with M bits,

each converter portion (100) including first to n th circuits (101_1 to 101_n) each being connected to a respective wiring group (112_1 to 112_n) and having a function of:

converting the further digital signal into an analog signal by using the M different voltages supplied from a respective wiring group (112_1 to 112_n), and

inputting the analog signal to the respective one of the first to n th subpixels (502_1 to 502_n; 606a; 606b) through the respective one of a first to n th wiring (113_1 to 113_n);

wherein each of the first to n th circuits (101_1 to 101_n) are connected to the respective first to n th wirings (113_1 to 113_n), the respective first to n th wirings being connected to respective first to n th subpixels (502_1 to 502_n; 606a; 606b);

wherein the first to n th subpixels (502_1 to 502_n; 606a; 606b) of each pixel are connected to a same scanning line (G_i);

the display device further comprising a signal line driver circuit (601) adapted to write each of the first to n th analog signals into a respective one of the first to n th subpixels (502_1 to 502_n; 606a; 606b) during one gate selecting period, wherein the signal line driver circuit comprises the plurality of converter portions;

wherein the first to n th wiring (113_1, ..., 113_n) are part of the display device.

3. The display device according to any claims 1 or 2, wherein the display device is a liquid crystal display device.

4. An electronic device provided with the display device according to any one of claims 1 to 3 and a switch or an operation key.

Patentansprüche

1. Anzeigevorrichtung, die umfasst:

5 eine Vielzahl von Pixeln, wobei jedes Pixel (502; 605) in erste bis n -te, n ist eine natürliche Zahl von 2 oder mehr, Subpixel (502_1 bis 502_n; 606a; 606b) unterteilt ist, wobei jedes der ersten bis n -ten Subpixel (502_1 bis 502_n; 606a; 606b) mit einer Elektrode zum Ansteuern eines Flüssigkristallelements bereitgestellt ist;

10 n Leitungsgruppen (112_1 bis 112_n), die jeweils M unterschiedliche Spannungen zuführen, wobei M eine natürliche Zahl von 2 oder mehr ist;

15 eine Vielzahl von ersten Leitungsgruppen (111), wobei ein digitales Signal mit N Bits in jede der ersten Leitungsgruppen (111) eingegeben wird, wobei N eine natürliche Zahl von 2 oder mehr ist;

20 eine Vielzahl von Abtastleitungen (G_i);
eine Vielzahl von Umwandlungsabschnitten (100);

wobei jeder Umwandlungsabschnitt (100) eine Funktion zum Umwandeln des entsprechenden digitalen Signals in ein erstes bis n -tes analoges Signal aufweist, und wobei der Umwandlungsabschnitt (100) erste bis n -te Schaltungen (101_1 bis 101_n) umfasst, die jeweils mit einer entsprechenden Leitungsgruppe (112_1 bis 112_n) verbunden sind und eine der folgenden Funktionen aufweisen:

Umwandeln des digitalen Signals in ein analoges Signal, indem die M unterschiedlichen Spannungen verwendet werden, die von einer entsprechenden Leitungsgruppe (112_1 bis 112_n) zugeführt werden, und Eingeben des analogen Signals in das entsprechende der ersten bis n -ten Subpixel (502_1 bis 502_n; 606a; 606b) über die entsprechende von einer ersten bis n -ten Leitung (113_1 bis 113_n);

wobei jede der ersten bis n -ten Schaltungen (101_1 bis 101_n) mit der entsprechenden ersten bis n -ten Leitung (113_1 bis 113_n) verbunden ist, und wobei die entsprechenden ersten bis n -ten Leitungen mit entsprechenden ersten bis n -ten Subpixeln (502_1 bis 502_n; 606a; 606b) verbunden sind;

wobei die ersten bis n -ten Subpixel (502_1 bis 502_n; 606a; 606b) jedes Pixels mit derselben Abtastleitung (G_i) verbunden sind;

wobei die Anzeigevorrichtung ferner eine Signalleitungstreiberschaltung (601) umfasst, die konfiguriert ist, jedes der ersten bis n -ten analogen Signale während einer Gate-Auswahlperiode in ein entsprechendes der ersten bis n -ten

Subpixel (502_1 bis 502_n; 606a; 606b) zu schreiben, wobei die Signalleitungstreiberschaltung die Vielzahl von Umwandlungsabschnitten umfasst;
wobei die ersten bis n -ten Leitungen (113_1, ..., 113_n) ein Teil der Anzeigevorrichtung sind.

2. Anzeigevorrichtung, die umfasst:

eine Vielzahl von Pixeln, wobei jedes Pixel (502; 605) in erste bis n -te, n ist eine natürliche Zahl von 2 oder mehr, Subpixel (502_1 bis 502_n; 606a; 606b) unterteilt ist, und wobei jedes der ersten bis n -ten Subpixel (502_1 bis 502_n; 606a; 606b) mit einer Elektrode zum Ansteuern eines Flüssigkristallelements bereitgestellt ist; n Leitungsgruppen (112_1 bis 112_n), die jeweils M unterschiedliche Spannungen zuführen, wobei M eine natürliche Zahl von 2 oder mehr ist;
eine Vielzahl von ersten Leitungsgruppen (111), wobei ein digitales Signal mit N Bits in jede der ersten Leitungsgruppen (111) eingegeben wird, wobei N eine natürliche Zahl von 2 oder mehr ist;
eine Vielzahl von Abtastleitungen (Gi);
eine Vielzahl von Umwandlungsabschnitten (100);

wobei jeder Umwandlungsabschnitt (100) eine Funktion zum Umwandeln eines entsprechenden digitalen Signals in ein erstes bis n -tes analoges Signal aufweist und eine Decoderschaltung (201) umfasst, wobei die Decoderschaltung die Funktion zum Decodieren des digitalen Signals mit N Bits in ein weiteres digitales Signal mit M Bits aufweist,
wobei jeder Umwandlungsabschnitt (100) erste bis n -te Schaltungen (101_1 bis 101_n) umfasst, die jeweils mit einer entsprechenden Leitungsgruppe (112_1 bis 112_n) verbunden sind und eine der folgenden Funktionen aufweisen:

Umwandeln des weiteren digitalen Signals in ein analoges Signal, indem die M unterschiedlichen Spannungen verwendet werden, die von einer entsprechenden Leitungsgruppe (112_1 bis 112_n) zugeführt werden, und

Eingeben des analogen Signals in das entsprechende der ersten bis n -ten Subpixel (502_1 bis 502_n; 606a; 606b) über die entsprechende von einer ersten bis n -ten Leitung (113_1 bis 113_n);

wobei jede der ersten bis n -ten Schaltungen (101_1 bis 101_n) mit der entsprechenden ersten bis n -ten Leitung (113_1 bis 113_n) verbunden ist, wobei die entsprechenden ersten bis n -ten Leitungen mit entsprechenden ersten bis

n -ten Subpixeln (502_1 bis 502_n; 606a; 606b) verbunden sind;

wobei die ersten bis n -ten Subpixel (502_1 bis 502_n; 606a; 606b) jedes Pixels mit derselben Abtastleitung (Gi) verbunden sind;

wobei die Anzeigevorrichtung ferner eine Signalleitungstreiberschaltung (601) umfasst, die konfiguriert ist, jedes der ersten bis n -ten analogen Signale in ein entsprechendes erstes bis n -tes Subpixel (502_1 bis 502_n; 606a; 606b) während einer Gate-Auswahlperiode zu schreiben, wobei die Signalleitungstreiberschaltung die Vielzahl von Umwandlungsabschnitten umfasst;

wobei die ersten bis n -ten Leitungen (113_1, ..., 113_n) ein Teil der Anzeigevorrichtung sind.

3. Anzeigevorrichtung nach einem der Ansprüche 1 oder 2, wobei die Anzeigevorrichtung eine Flüssigkristallanzeigevorrichtung ist.

4. Elektronisches Gerät, das mit der Anzeigevorrichtung nach einem der Ansprüche 1 bis 3 und einem Schalter oder einer Bedienungstaste bereitgestellt ist.

Revendications

1. Dispositif d'affichage comprenant:

une pluralité de pixels, dans laquelle chaque pixel (502; 605) est divisé en premier à $n^{\text{ème}}$ sous-pixels (502_1 à 502_n; 606a; 606b), n étant un nombre naturel de 2 ou plus, dans laquelle chacun du premier au $n^{\text{ème}}$ sous-pixels (502_1 à 502_n; 606a; 606b) est fourni avec une électrode destinée à commander un élément à cristaux liquides;

n groupes de câblages (112_1 à 112_n), chacun fournissant M tensions différentes, dans lequel M est un nombre naturel de 2 ou plus;

une pluralité de premiers groupes de câblages (111), dans laquelle un signal numérique de N bits, N étant un nombre naturel de 2 ou plus, est entré dans chacun desdits premiers groupes de câblages (111);

une pluralité de lignes de balayage (Gi);

une pluralité de parties convertisseur (100);

chaque partie convertisseur (100) ayant une fonction pour convertir le signal numérique respectif en un premier à $n^{\text{ème}}$ signal analogique, la partie convertisseur (100) comportant un premier à $n^{\text{ème}}$ circuits (101_1 à 101_n), chacun étant connecté à un groupe de câblages respectif (112_1 à 112_n) et ayant une fonction de:

convertir le signal numérique en un signal

analogique par utilisation des M tensions différentes fournies par un groupe de câblages respectif (112_1 à 112_n), et entrer le signal analogique à l'un respectif du premier au $n^{\text{ème}}$ sous-pixels (502_1 à 502_n; 606a; 606b) par l'un respectif d'un premier à $n^{\text{ème}}$ câblage (113_1 à 113_n);

dans lequel chacun du premier au $n^{\text{ème}}$ circuits (101_1 à 101_n) est connecté au premier au $n^{\text{ème}}$ câblages respectifs (113_1 à 113_n), le premier au $n^{\text{ème}}$ câblages respectifs étant connectés au premier au $n^{\text{ème}}$ sous-pixels respectifs (502_1 à 502_n; 606a; 606b); dans lequel le premier au $n^{\text{ème}}$ sous-pixels (502_1 à 502_n; 606a; 606b) de chaque pixel sont connectés à une même ligne de balayage (Gi); le dispositif d'affichage comprenant en plus un circuit de commande de ligne de signal (601) adapté pour écrire chacun du premier au $n^{\text{ème}}$ signaux analogiques dans l'un respectif du premier au $n^{\text{ème}}$ sous-pixels (502_1 à 502_n; 606a; 606b) au cours d'une période de sélection de grille, dans lequel le circuit de commande de ligne de signal comprend la pluralité de parties convertisseur; dans lequel le premier au $n^{\text{ème}}$ câblage (113_1, ..., 113_n) sont une partie du dispositif d'affichage.

2. Dispositif d'affichage comprenant:

une pluralité de pixels, dans laquelle chaque pixel (502; 605) est divisé en premier à $n^{\text{ème}}$ sous-pixels (502_1 à 502_n; 606a; 606b), n étant un nombre naturel de 2 ou plus, dans laquelle chacun du premier au $n^{\text{ème}}$ sous-pixels (502_1 à 502_n; 606a; 606b) est fourni avec une électrode destinée à commander un élément à cristaux liquides; n groupes de câblages (112_1 à 112_n), chacun fournissant M tensions différentes, dans lequel M est un nombre naturel de 2 ou plus; une pluralité de premiers groupes de câblages (111), dans laquelle un signal numérique de N bits, N étant un nombre naturel de 2 ou plus, est entré dans chacun desdits premiers groupes de câblages (111); une pluralité de lignes de balayage (Gi); une pluralité de parties convertisseur (100); chaque partie convertisseur (100) ayant une fonction pour convertir un signal numérique respectif en un premier à $n^{\text{ème}}$ signal analogique et comportant un circuit décodeur (201), dans laquelle le circuit décodeur a la fonction pour décodifier le signal numérique de N bits en un autre signal numérique de M bits,

chaque partie convertisseur (100) comportant un premier à $n^{\text{ème}}$ circuits (101_1 à 101_n), chacun étant connecté à un groupe de câblages respectif (112_1 à 112_n) et ayant une fonction de:

convertir l'autre signal numérique en un signal analogique par utilisation des M tensions différentes fournies par un groupe de câblages respectif (112_1 à 112_n), et entrer le signal analogique à l'un respectif du premier au $n^{\text{ème}}$ sous-pixels (502_1 à 502_n; 606a; 606b) par l'un respectif d'un premier à $n^{\text{ème}}$ câblage (113_1 à 113_n);

dans lequel chacun du premier au $n^{\text{ème}}$ circuits (101_1 à 101_n) est connecté au premier au $n^{\text{ème}}$ câblages respectifs (113_1 à 113_n), le premier au $n^{\text{ème}}$ câblages respectifs étant connectés au premier au $n^{\text{ème}}$ sous-pixels respectifs (502_1 à 502_n; 606a; 606b); dans lequel le premier au $n^{\text{ème}}$ sous-pixels (502_1 à 502_n; 606a; 606b) de chaque pixel sont connectés à une même ligne de balayage (Gi); le dispositif d'affichage comprenant en plus un circuit de commande de ligne de signal (601) adapté pour écrire chacun du premier au $n^{\text{ème}}$ signaux analogiques dans l'un respectif du premier au $n^{\text{ème}}$ sous-pixels (502_1 à 502_n; 606a; 606b) au cours d'une période de sélection de grille, dans lequel le circuit de commande de ligne de signal comprend la pluralité de parties convertisseur; dans lequel le premier au $n^{\text{ème}}$ câblage (113_1, ..., 113_n) sont une partie du dispositif d'affichage.

3. Dispositif d'affichage selon l'une quelconque des revendications 1 ou 2, dans lequel le dispositif d'affichage est un dispositif d'affichage à cristaux liquides.

4. Dispositif électronique fourni avec le dispositif d'affichage selon l'une quelconque des revendications 1 à 3 et un interrupteur ou une touche d'opération.

FIG. 1A

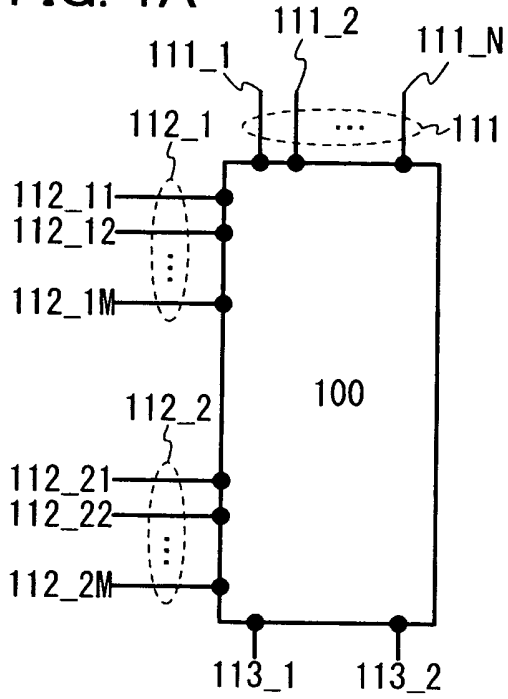


FIG. 1B

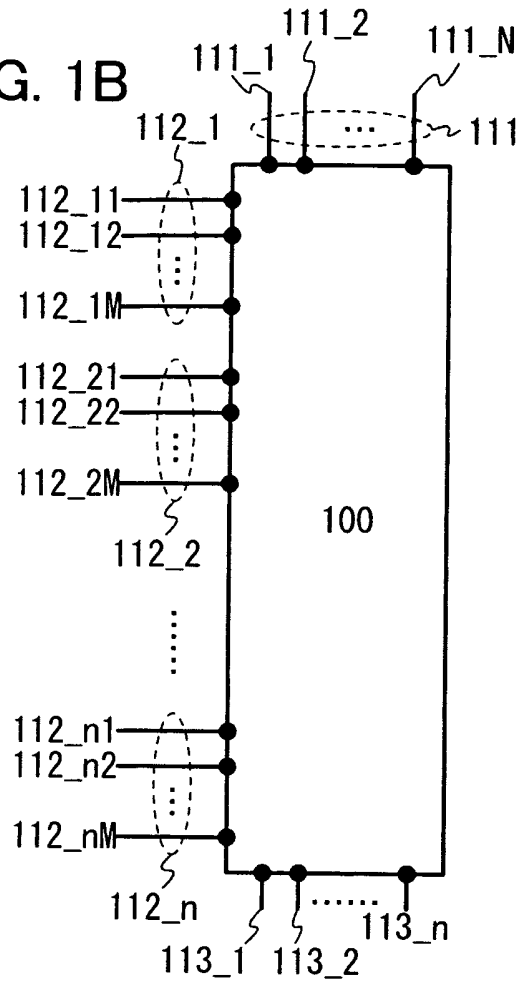


FIG. 1C

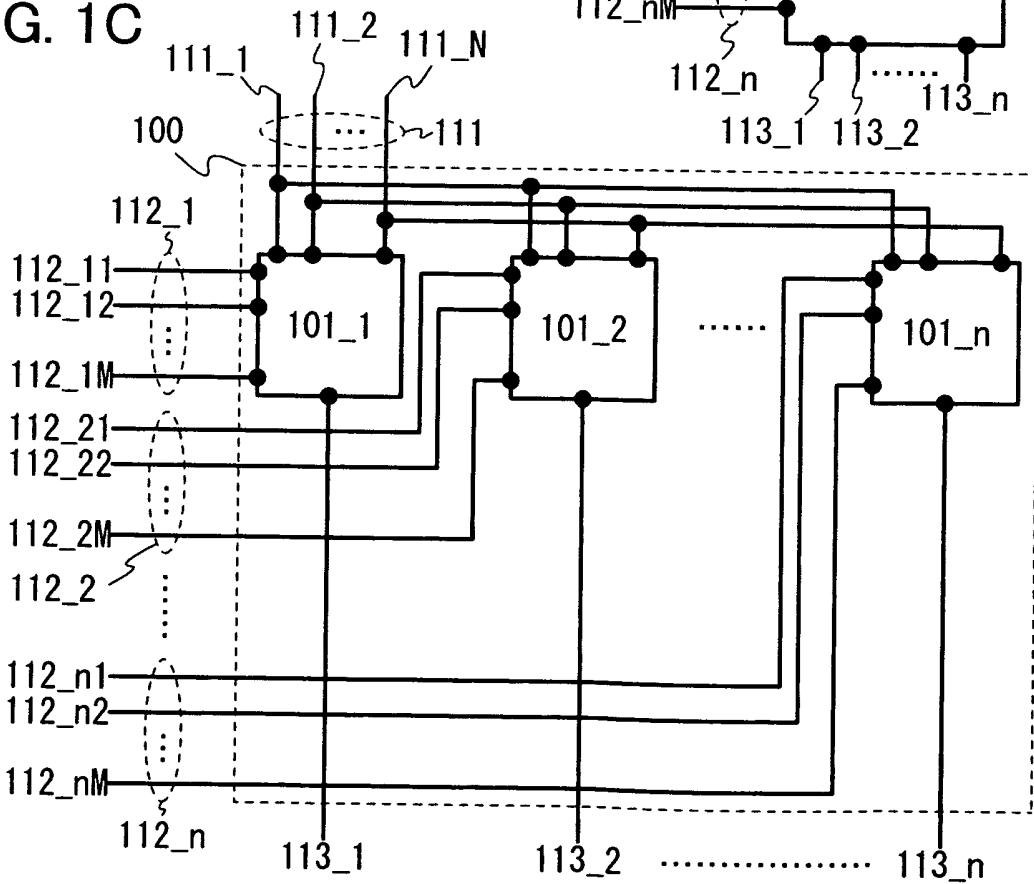


FIG. 2A

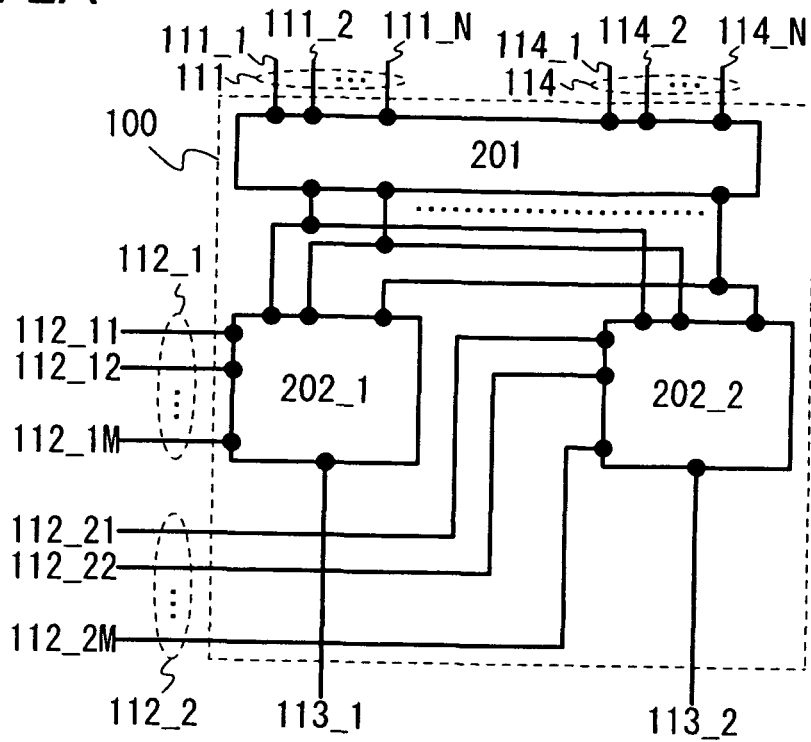


FIG. 2B

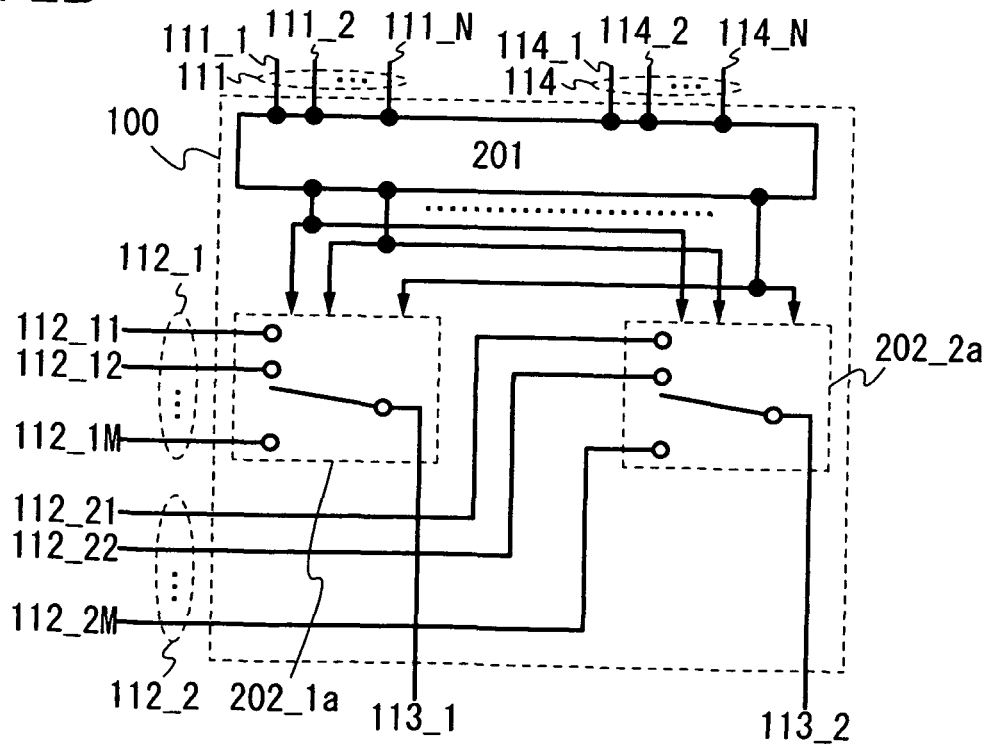
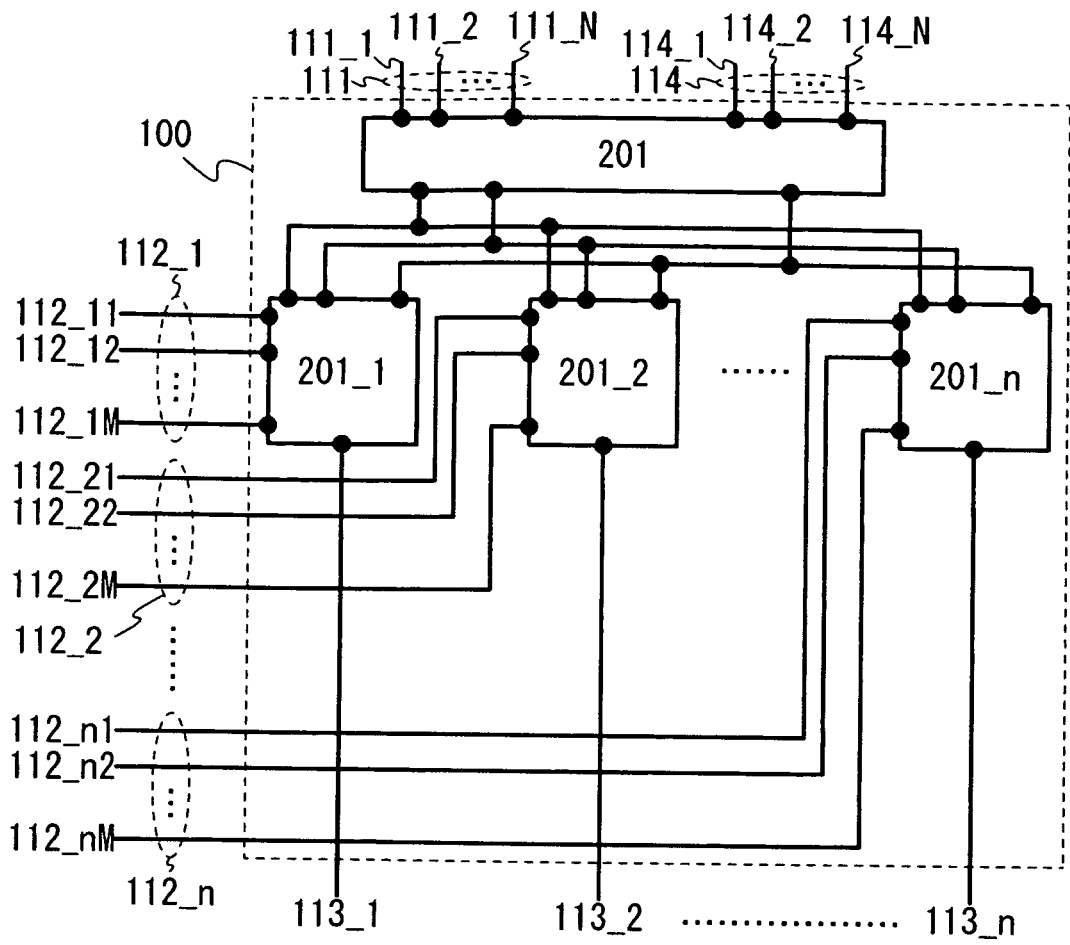
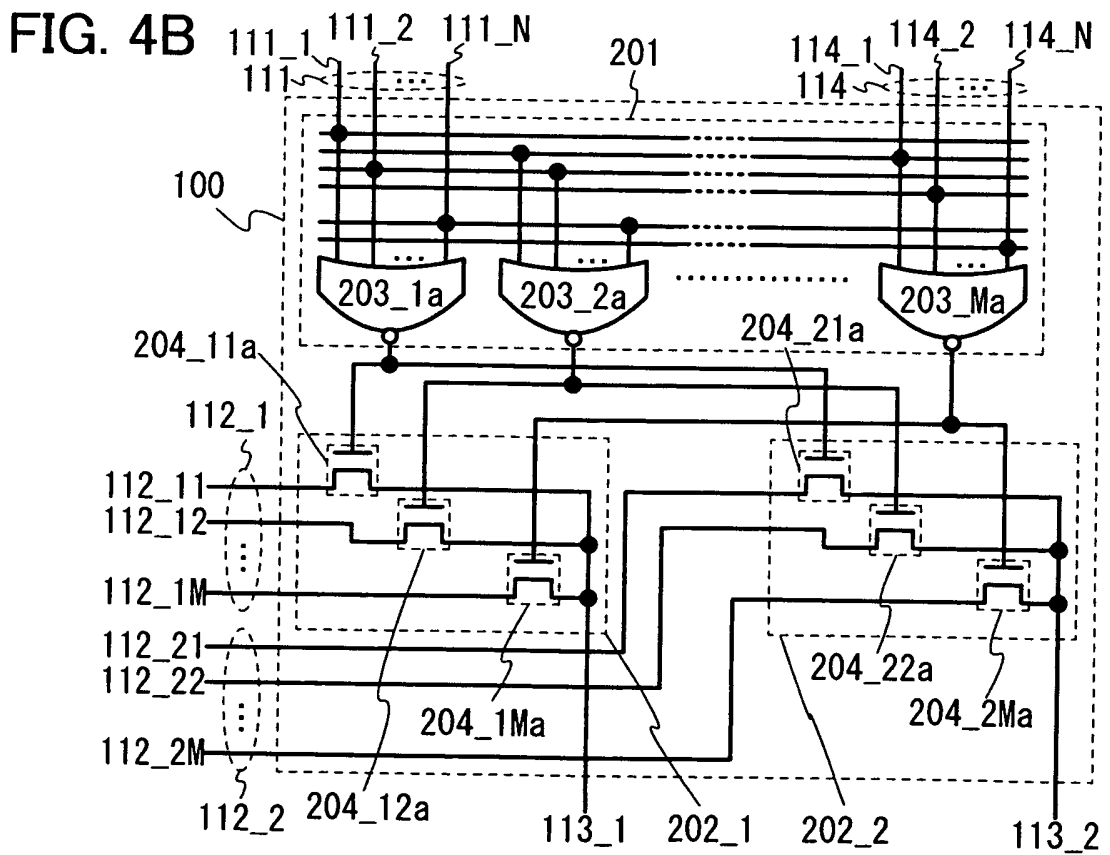
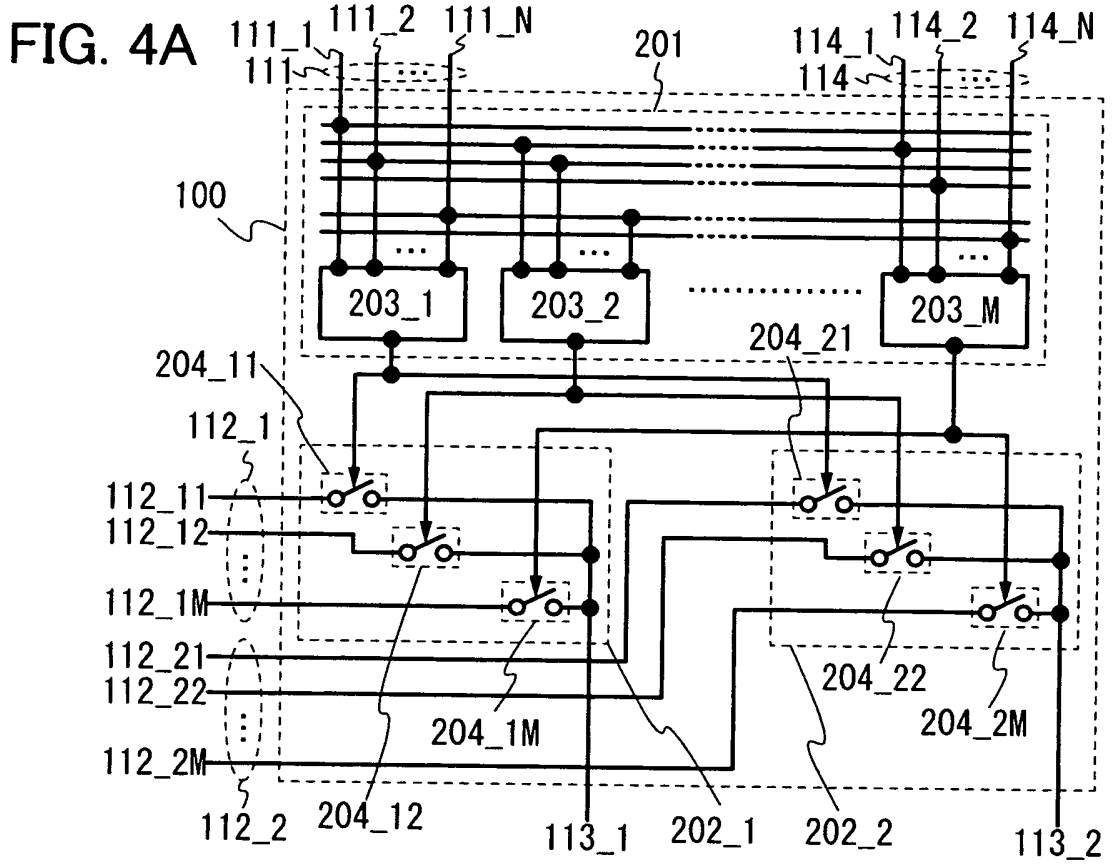
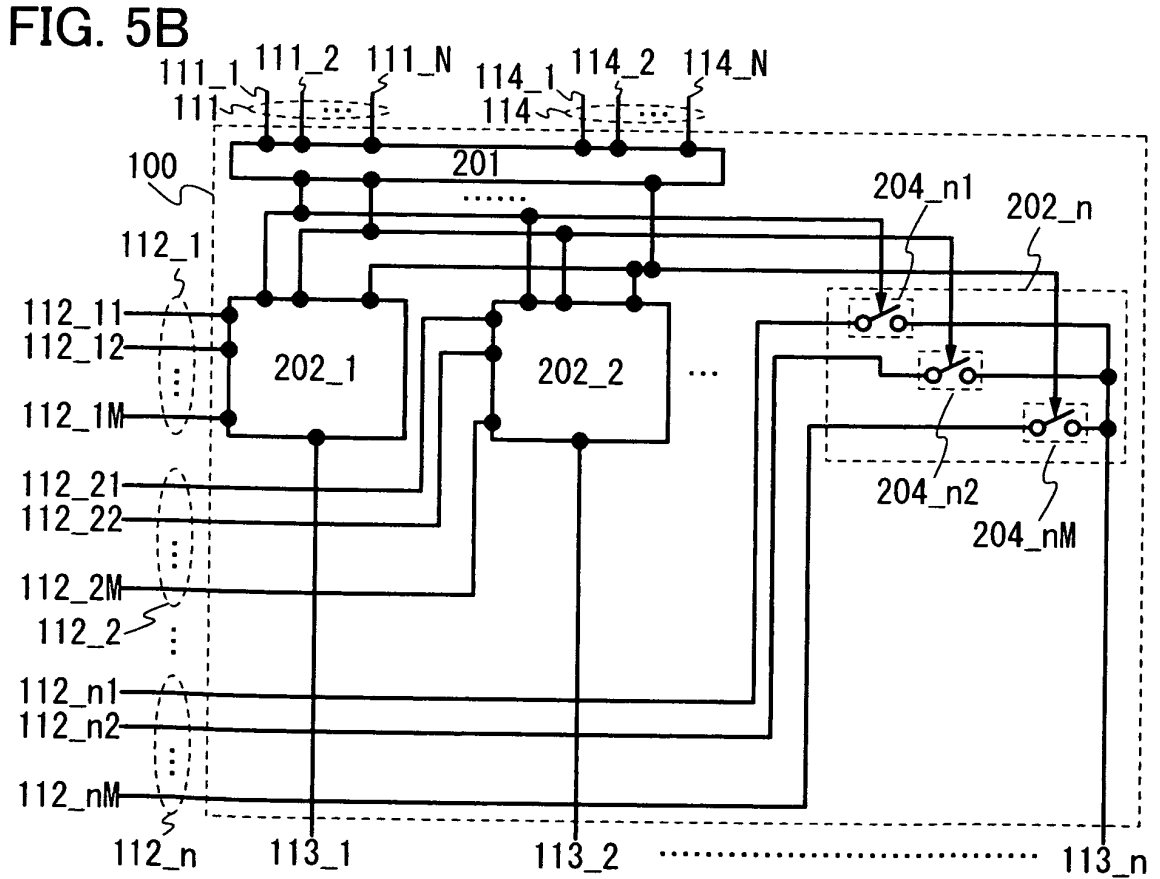
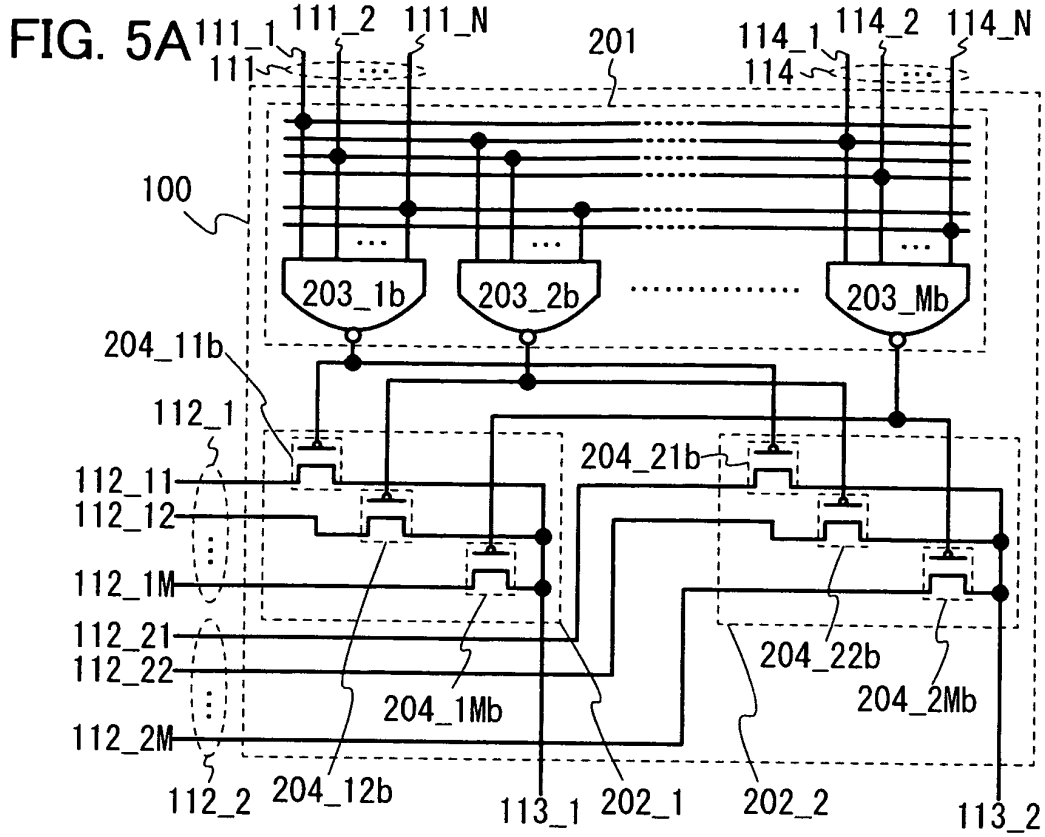


FIG. 3







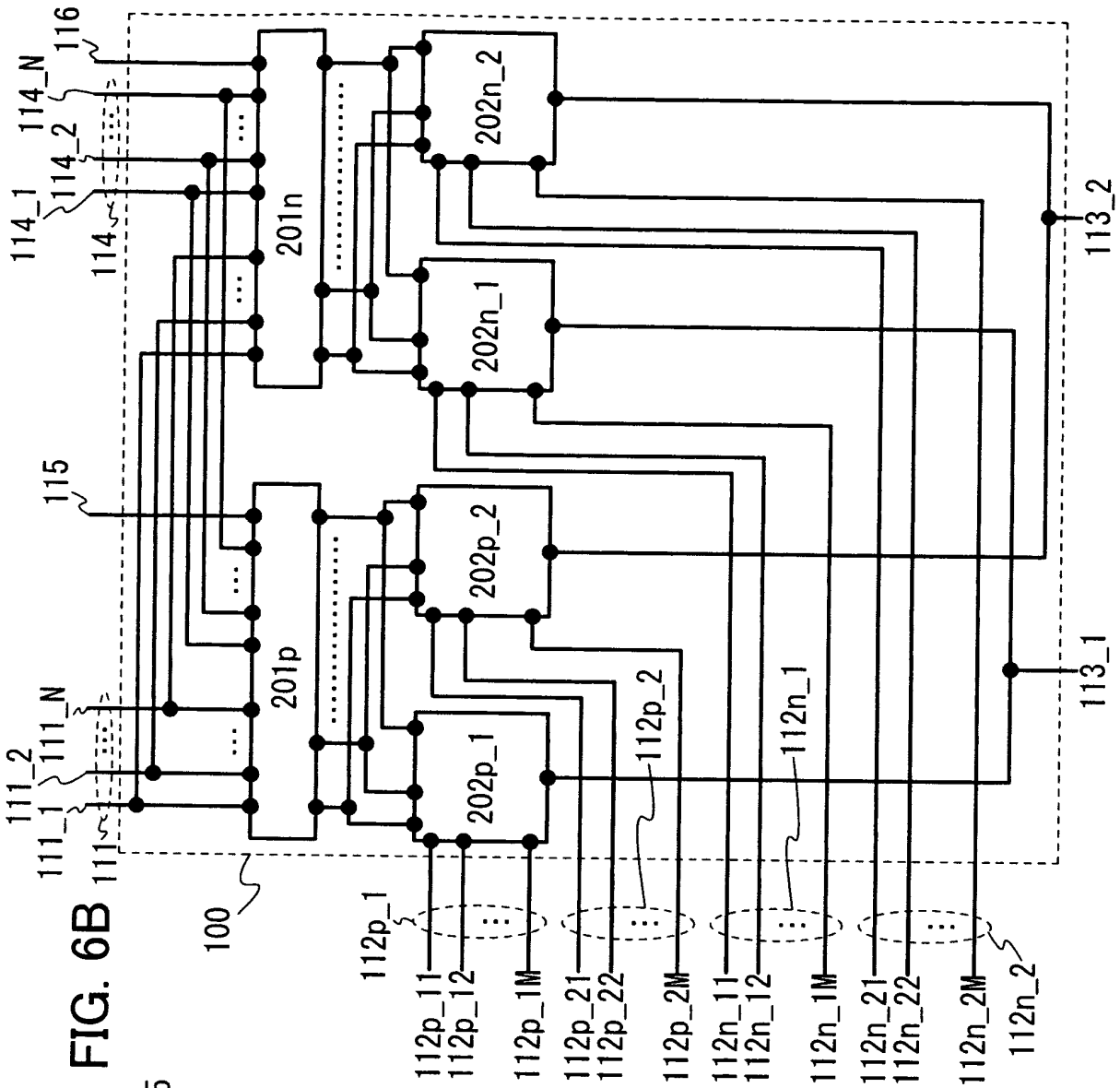


FIG. 6A

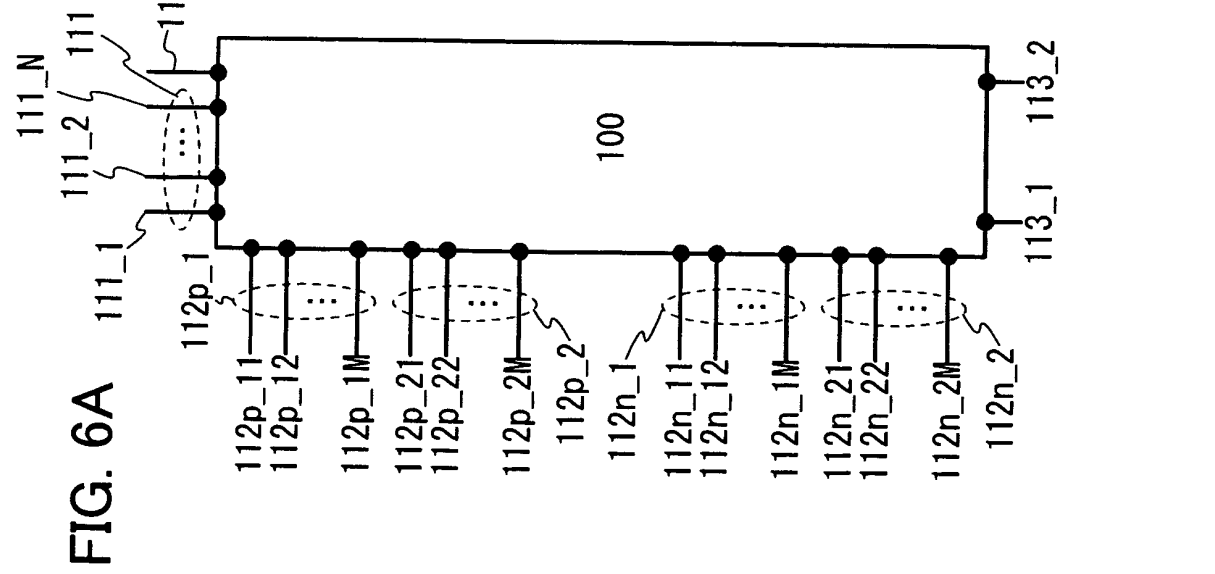


FIG. 6B

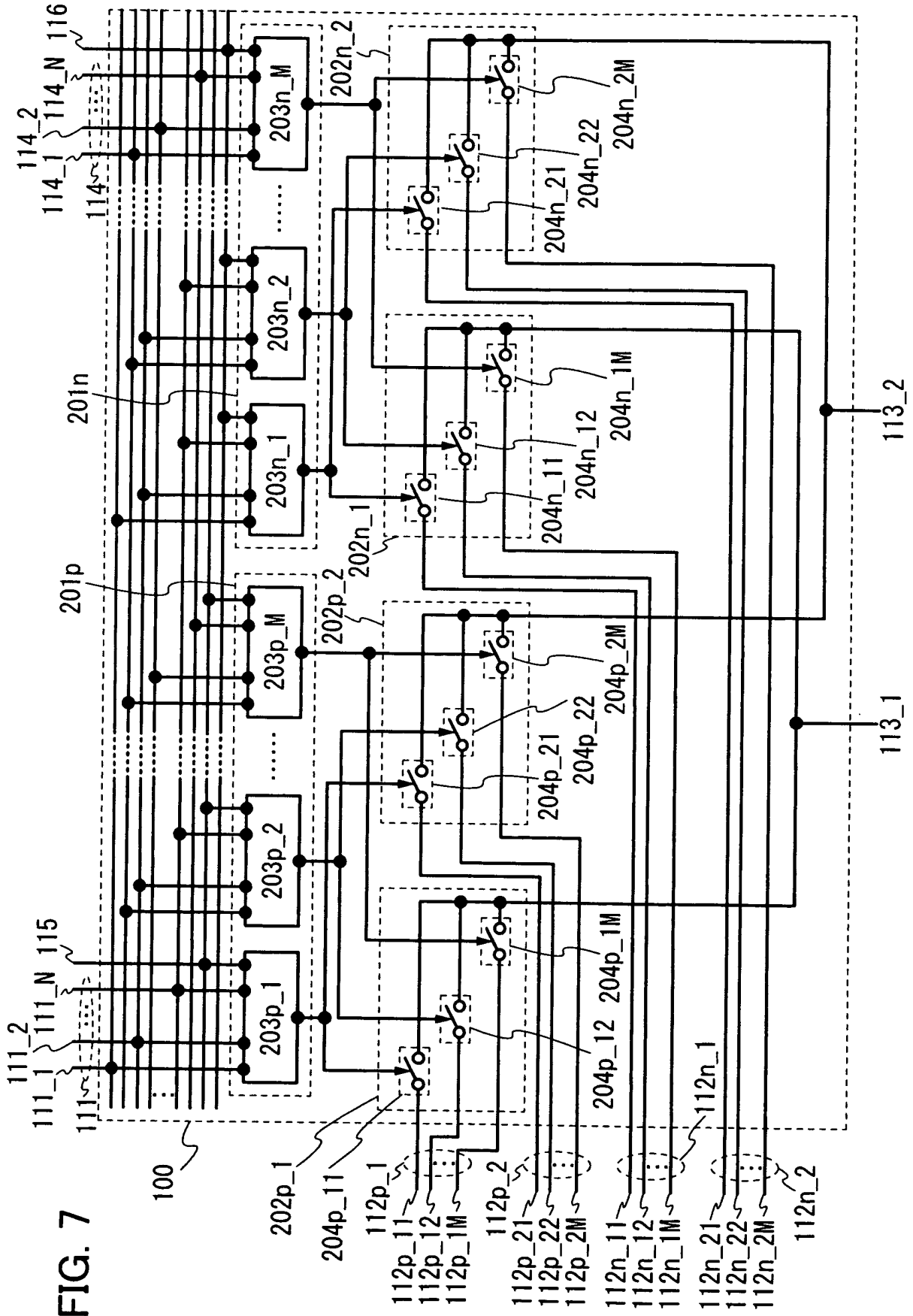


FIG. 7

FIG. 8A

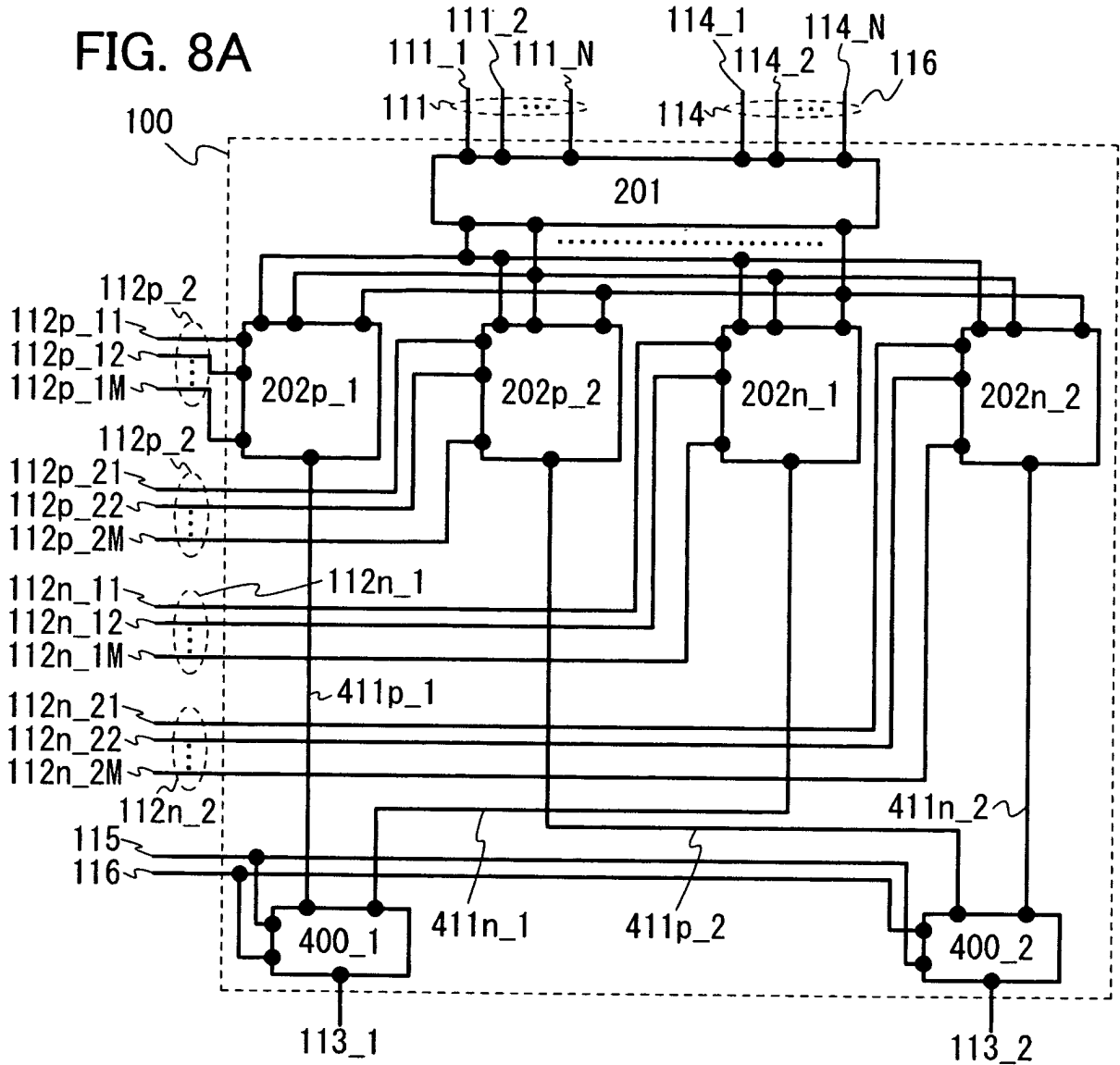


FIG. 8B

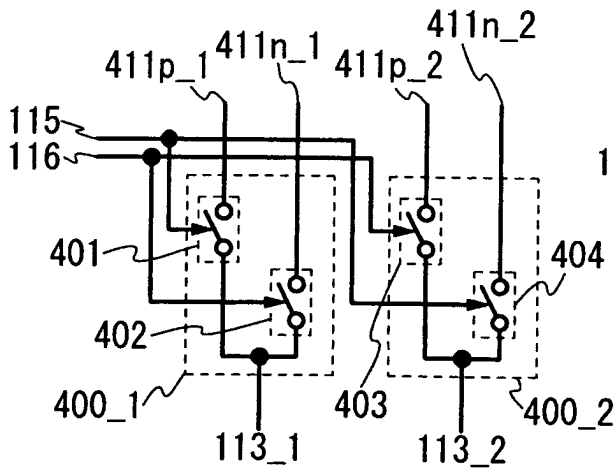


FIG. 8C

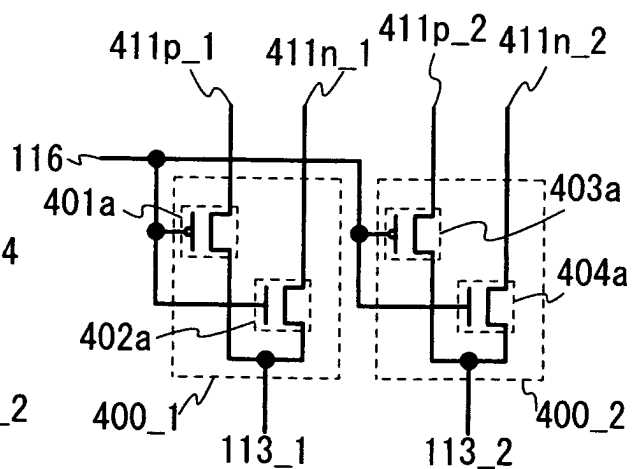


FIG. 9A

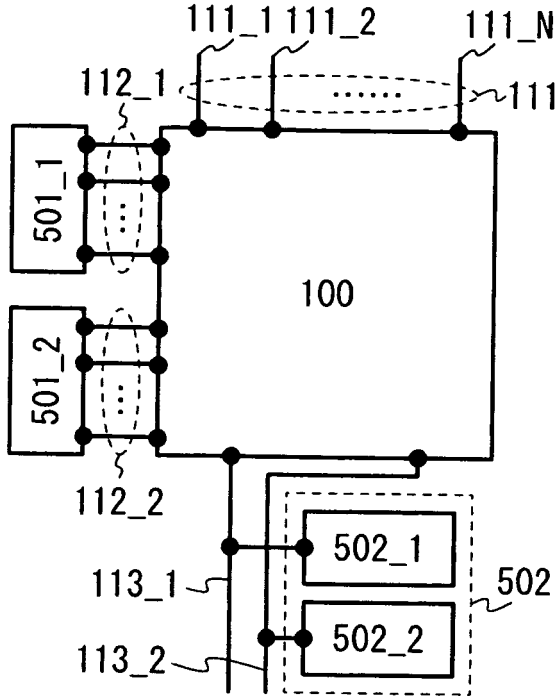


FIG. 9B

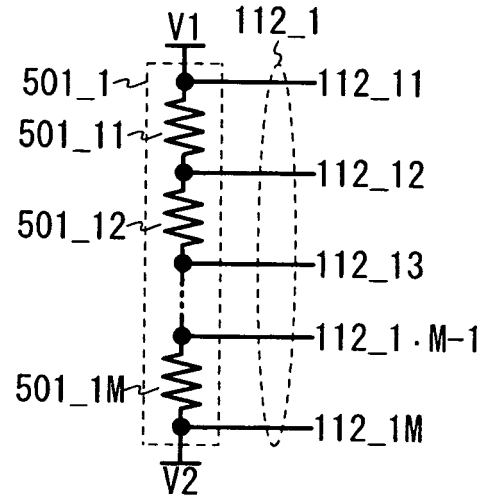


FIG. 9C

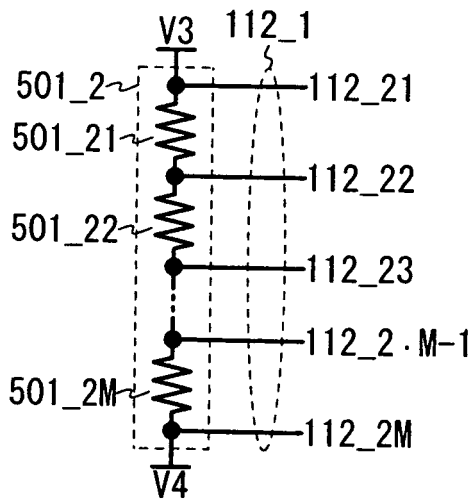


FIG. 10A

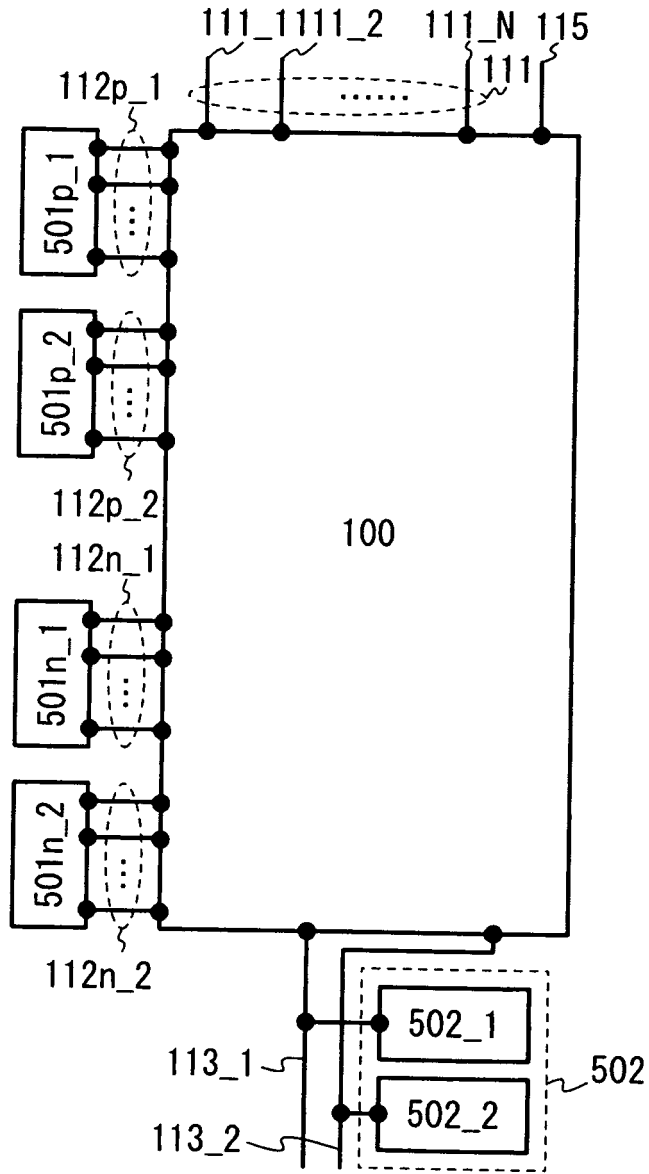


FIG. 10B

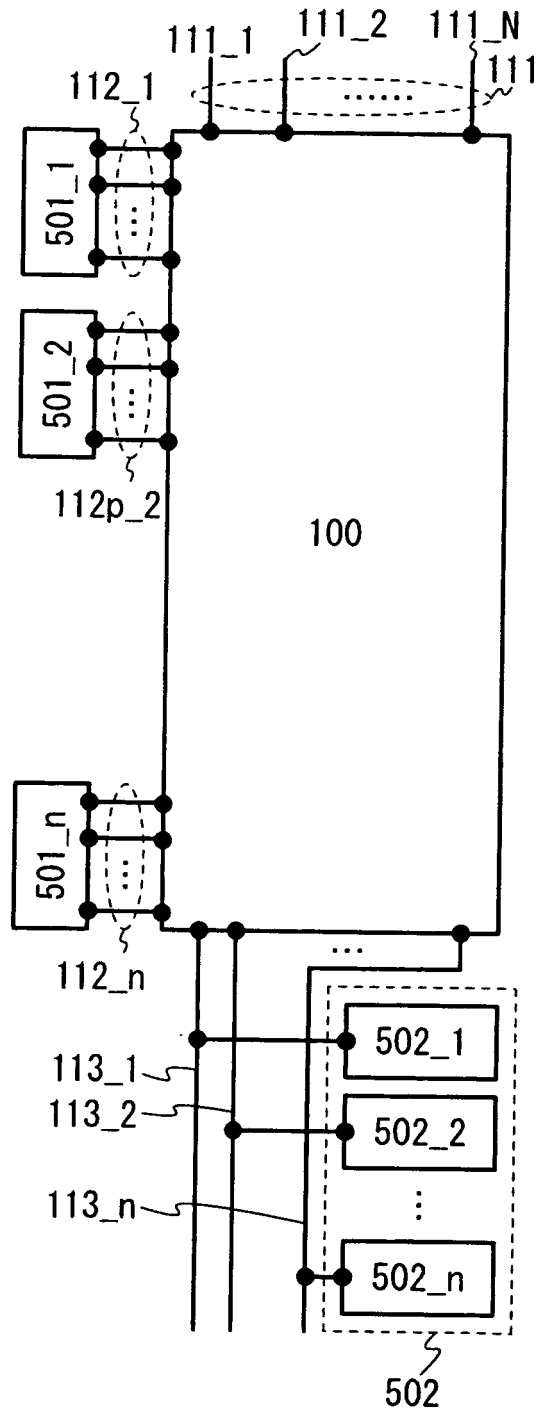


FIG. 11A

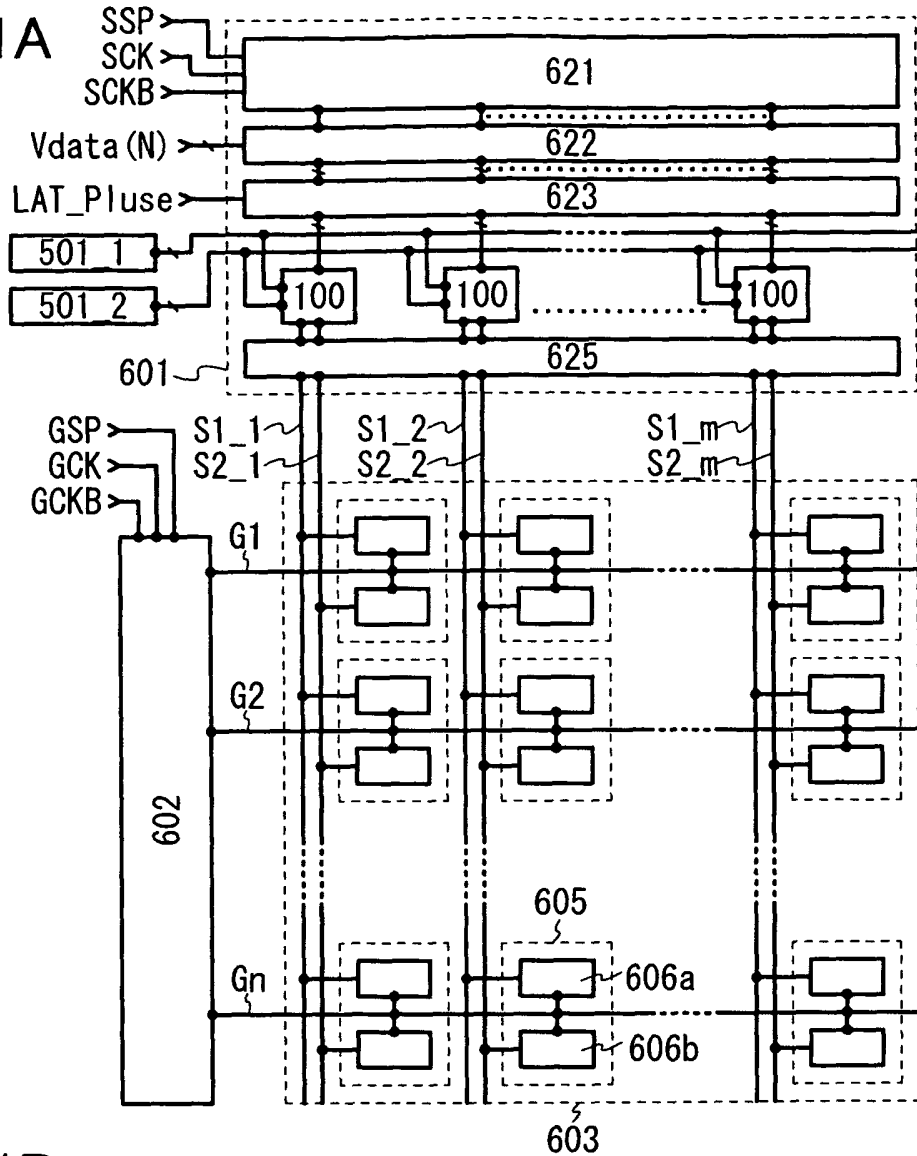


FIG. 11B

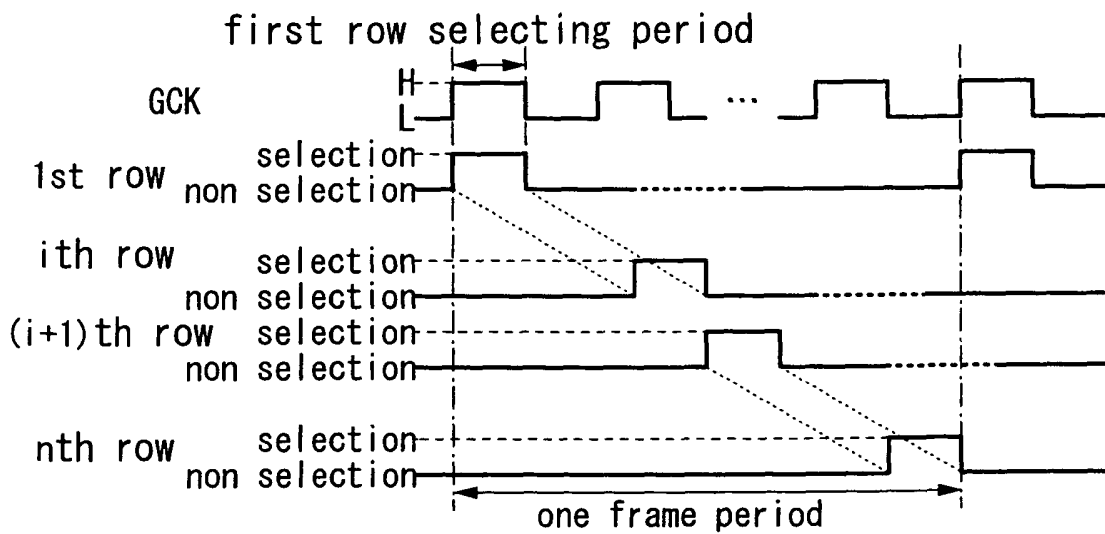


FIG. 12A

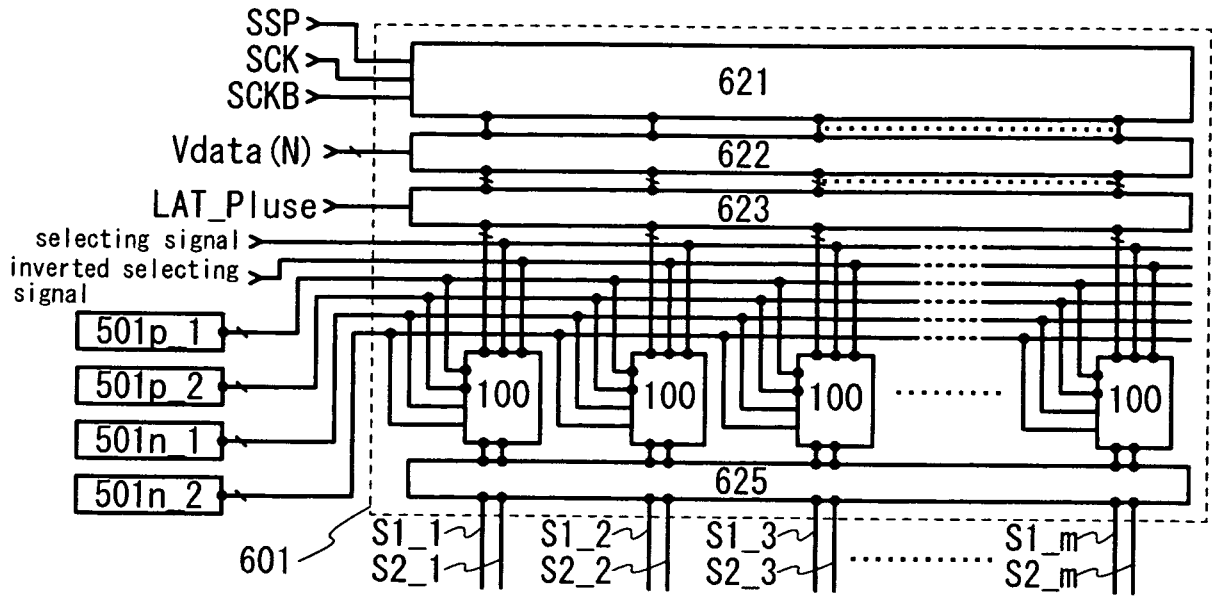


FIG. 12B

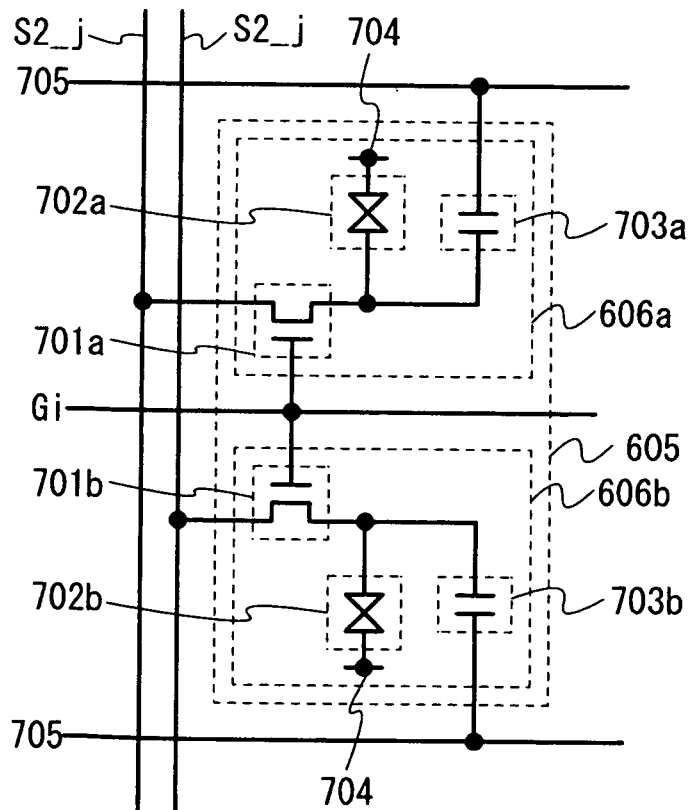
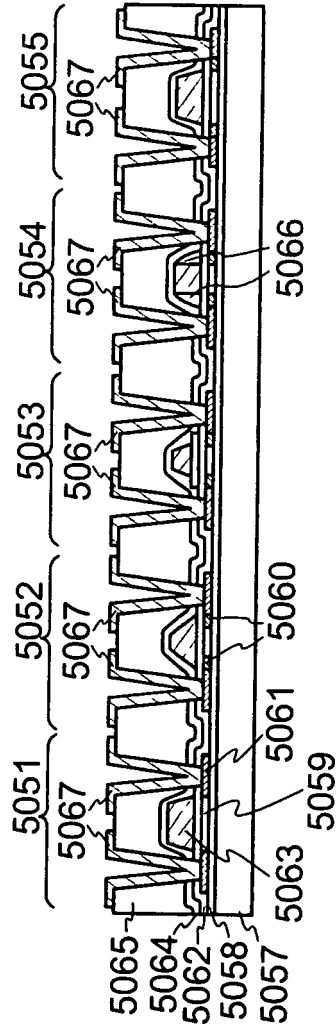


FIG. 13



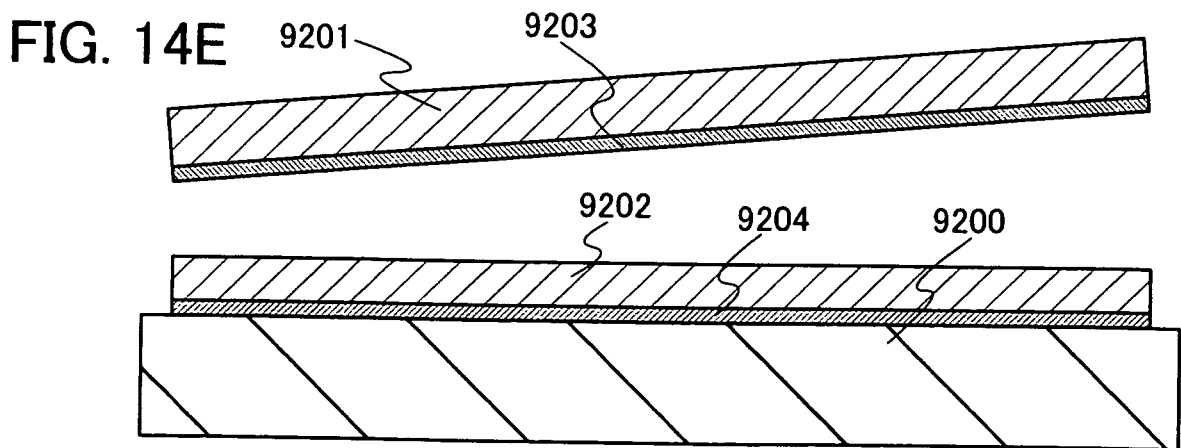
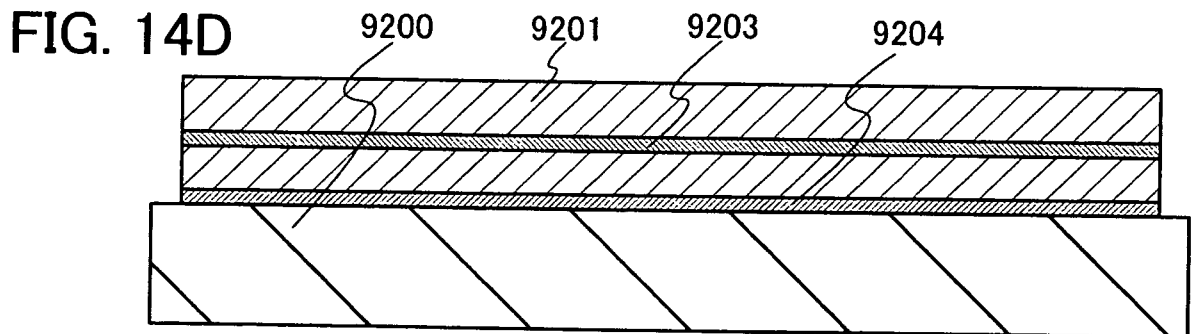
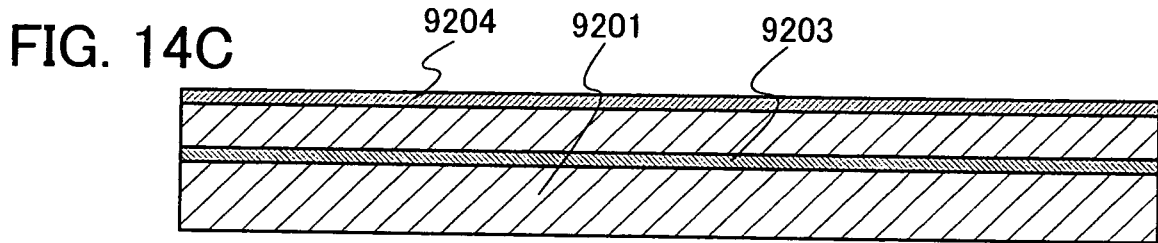
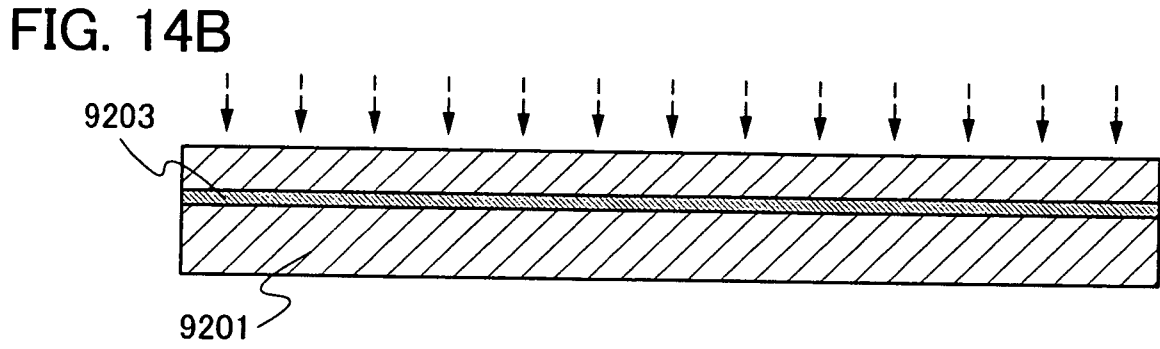
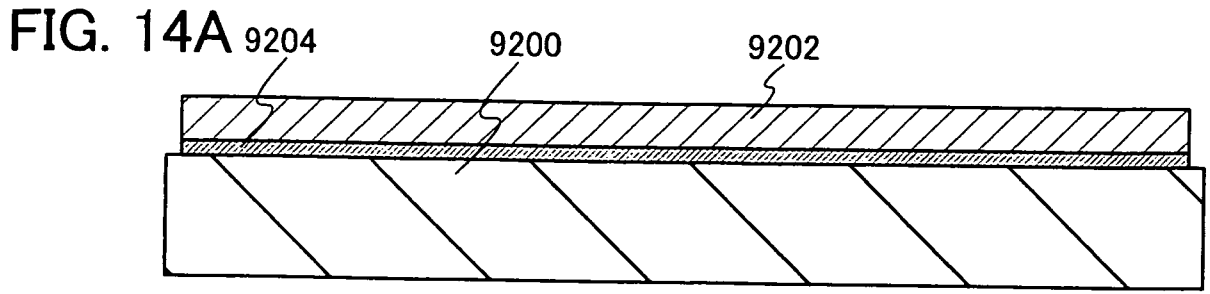


FIG. 15A

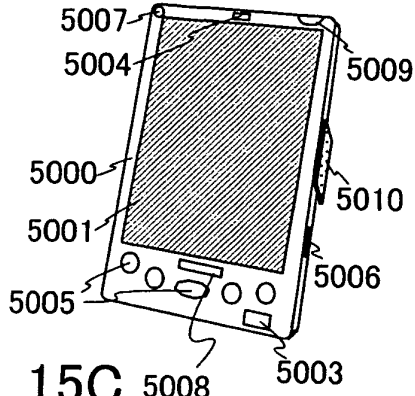


FIG. 15B

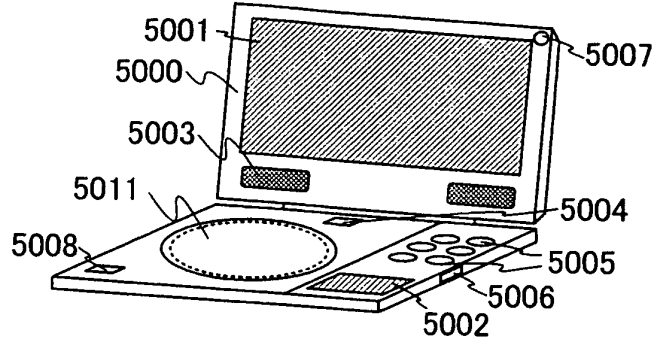


FIG. 15C

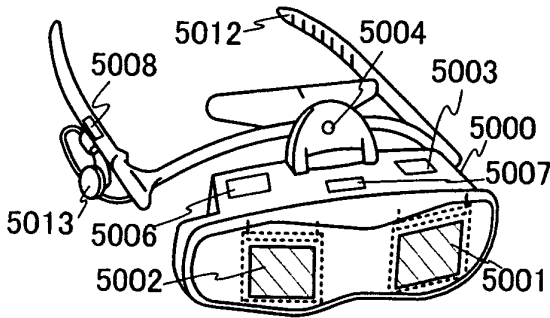


FIG. 15D

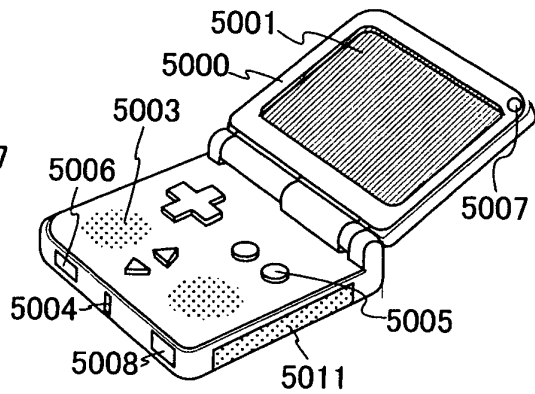


FIG. 15E

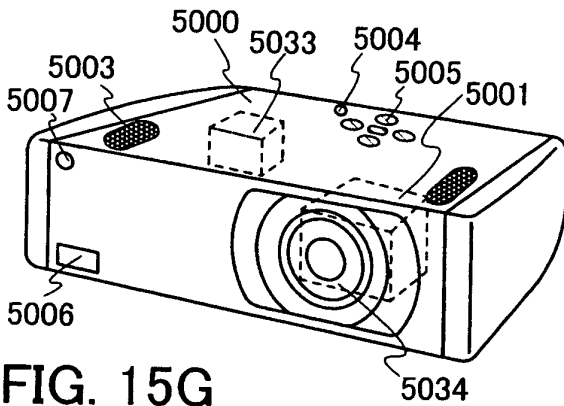


FIG. 15F

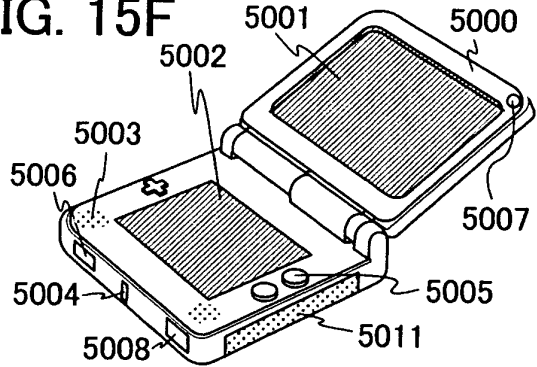


FIG. 15G

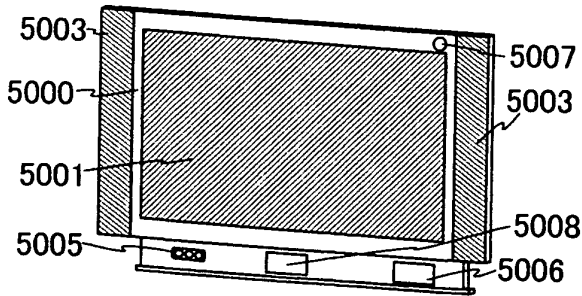


FIG. 15H

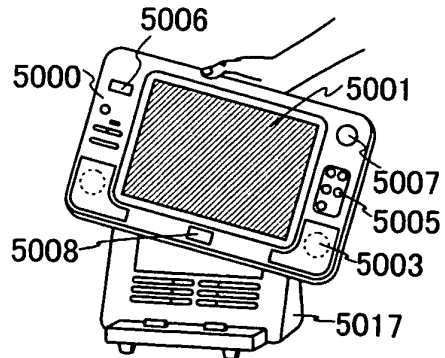


FIG. 16A

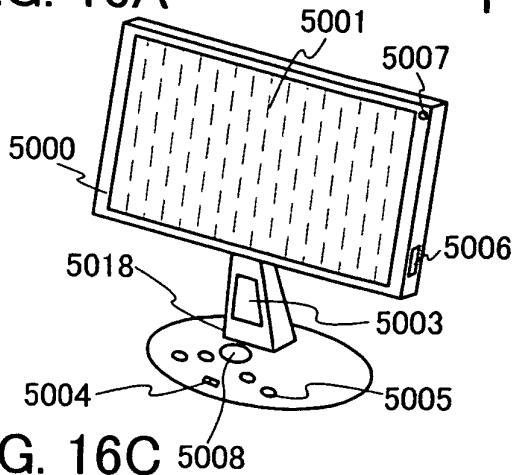


FIG. 16B

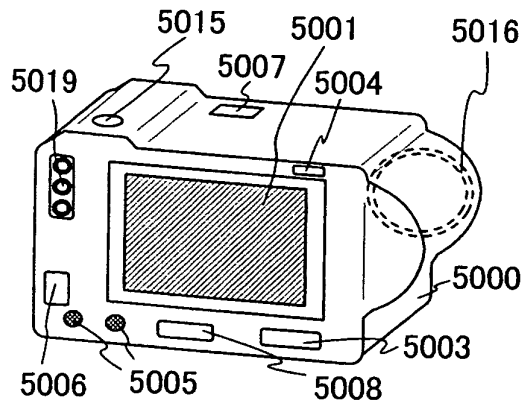


FIG. 16C

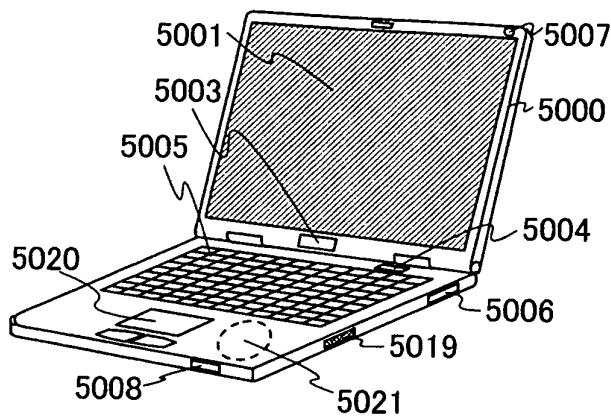


FIG. 16D

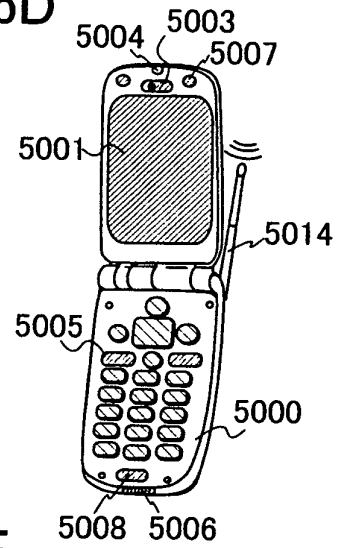


FIG. 16E

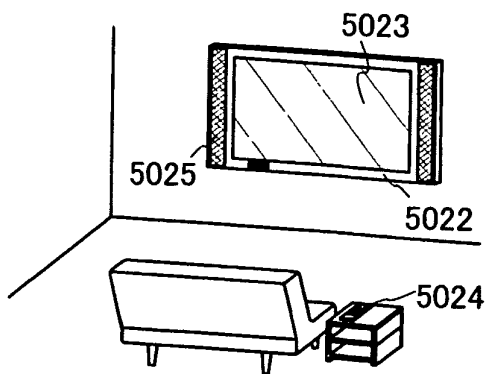


FIG. 16F

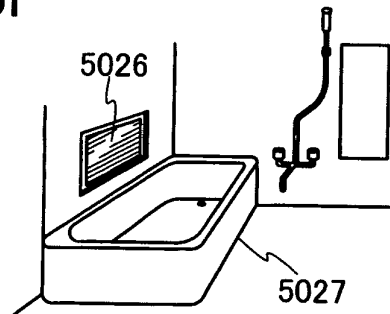


FIG. 16G

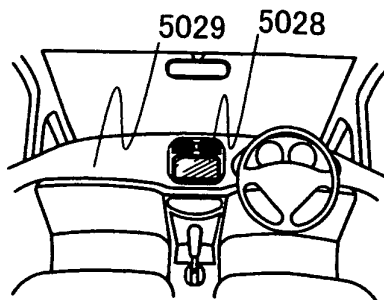
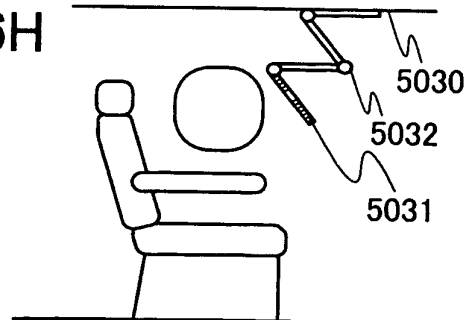


FIG. 16H



REFERENCES CITED IN THE DESCRIPTION

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专利名称(译)	显示装置，液晶显示装置和包括其的电子设备		
公开(公告)号	EP2136354B1	公开(公告)日	2017-03-22
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[标]申请(专利权)人(译)	株式会社半导体能源研究所		
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优先权	2008150608 2008-06-09 JP		
其他公开文献	EP2136354A3 EP2136354A2		
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摘要(译)

液晶显示装置包括具有第一至第n (n是2或更大的自然数) 个子像素的像素和电路 (100)。对于电路, N (N是2或更多的自然数) 布线 (111_1, 111_N) 用于提供具有N位的数字信号, 并且第一至第n布线组具有M (M是2或更大的自然数) 用于提供M个不同电压的布线 (112_11, ..., 112_2M) 电连接。液晶显示装置具有通过使用提供给第一至第n布线组的M个电压将数字信号转换为n个模拟信号并将n个模拟信号输入第一至第n子像素的功能。第一至第n子像素均包括用于驱动液晶元件的电极 (113_1, 113_2)。

