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(54) **Liquid crystal display device and display control device**

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Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to a liquid crystal display device, a liquid crystal display method, a display control device, and a display control method. The present invention relates more specifically to a liquid crystal display device, a liquid crystal display method, a display control device, and a display control method that are capable of suppressing the occurrence of inconsistencies in the form of streaks without the size of a thin-film transistor (TFT) being increased.

2. Description of the Related Art

[0002] Fig. 1 shows a schematic diagram of an active matrix of a liquid crystal display panel used in, for example, liquid crystal televisions or the like. Here, four rows denoted by n through n+3 and four columns denoted by m through m+3 are shown. Although the pixel positioned at (n+1, m+3) is used as an example to describe constituent elements that constitute one of pixels, the constituent elements of each of the pixels of the liquid crystal panel are the same as those of the pixel positioned at (n+1, m+3), as a matter of course.

[0003] A pixel electrode is provided to each of the pixels that perform display, and a liquid crystal capacitor 11 is formed between the pixel electrode and a common electrode opposite the pixel electrode with liquid crystal therebetween. For each pixel electrode, a TFT 12 that functions as a switch is formed, a gate electrode of the TFT 12 is connected to a gate bus line 14, a source electrode of the TFT 12 is connected to a source bus line 13, and a drain electrode of the TFT 12 is connected to the pixel electrode.

[0004] Patent application publication US 2005/0174310 A1 discloses a drive method for a liquid crystal display device that comprises providing an array of pixels formed in rows and columns. The method and a respectively designed drive circuit control the selection of odd-numbered rows of pixels during the first half and selection of even-numbered rows of pixels during the second half of a frame period.

[0005] Patent application publication US 2008/0036933 A1 presents a liquid crystal display device (LCD) with a pairs of signal lines Da, Db, scanning liens G, subpixels Pa and Pb arranged in matrix format. Subpixels Pa and Pb are connected in checkerboard manner along a column of pixels with respect to the corresponding pair of signal lines. Adjacent pixels connected to the same scanning line have first subpixels Pa or second subpixels Pb connected to adjacent signal lines of the pairs.

[0006] Representative examples of a pattern of the polarity arrangement of pixels in a case where liquid crystal is driven will be described using Figs. 2 and 3.

The pattern of the polarity arrangement shown in Fig. 2 is the most common, and is called dot inversion driving. In the pattern of the polarity arrangement, pixels of positive polarity and pixels of negative polarity are arranged in a checkerboard manner. In dot inversion driving, for example, pixels positioned at the top, the bottom, the right, and the left of a pixel of positive polarity at an arbitrary position have negative polarity. Similarly, pixels positioned at the top, the bottom, the right, and the left of a pixel of negative polarity at an arbitrary position have positive polarity. This pattern has an advantage in that even when the absolute value of the voltage of pixels of positive polarity and the absolute value of the voltage of pixels of negative polarity are not balanced because of inconsistencies in the common voltage, inconsistencies or flicker tends not to occur. However, in dot inversion driving, since the polarity of the output of a source bus line is inverted between positive and negative polarities in units of one line, there is a disadvantage in that the power consumption of a driver integrated circuit (IC) becomes large. In particular, when high-speed writing at 120 Hz or higher is performed in order to realize high-speed responsivity, this disadvantage becomes a severe problem.

[0007] Thus, at the time of high-speed driving, as shown in Fig. 3, vertical line inversion driving in which the polarity of pixels arranged in the vertical direction is not inverted within one frame is often performed (for example, see Japanese Unexamined Patent Application Publication No. 63-55590).

[0008] When liquid crystal driving is performed, it is ideal that the electric potential whose value is the center point between the positive and negative voltages applied to pixels is applied to the common electrode formed on the counter substrate, liquid crystal being provided between the pixel and common electrodes. When the value of a voltage applied to the common electrode has the central electric potential, the effective voltage applied to the liquid crystal is balanced in terms of positive and negative polarities and brightness does not vary between frames even when display is continuously performed at the same tone. However, it is significantly difficult to make the common voltage be optimal over the entire display unit because of various factors such as use of a transparent electrode ITO whose resistance is relatively high as the common electrode, the resistance of bus lines near TFTs, the parasitic capacitance of TFTs, TFT leakage, variations in liquid crystal capacitance. In this case, the effective voltage applied to a pixel of positive polarity is different from the effective voltage applied to a pixel of negative polarity pixel, and thus there is a problem in that the variations in brightness occur in units of one frame, that is, flicker occurs.

[0009] In dot inversion driving described using Fig. 2, positive and negative polarities are finely and evenly arranged in a mixed manner and the variations in brightness cancel each other out, whereby the degree of per-

ception of flicker is greatly reduced. However, when vertical line inversion is employed, flicker occurs in the form of vertical streaks since positive polarities or negative polarities are continuously arranged in each vertical column.

[0010] The frequency at which flicker occurs is half the frequency of the driving frequency, and thus in the case of a normal driving frequency of 60 Hz, flicker occurs at a frequency of 30 Hz. Thus, the degree of perception of flicker is very high. In contrast, when the driving frequency becomes high such as 120 Hz or 240 Hz, flicker occurs at a frequency of 60 Hz or 120 Hz, whereby it is not perceived as flicker by the human eye. That is, even when vertical line inversion is employed, if display is performed at high frequencies, general flicker becomes unrecognizable.

[0011] In a VA mode, there is a disadvantage regarding the viewing-angle characteristics in halftones. In order to improve the viewing-angle characteristics in halftones, multi-pixel technology is widely used. Fig. 4 is a drawing illustrating a principle of a multi-pixel structure used for achieving a wide viewing angle in liquid crystal televisions and the like. A pixel is divided into two, for example, a sub-pixel A and a sub-pixel B. Regarding an input tone, the pixel is configured in such a manner that the brightness of the sub-pixel A first increases and then the brightness of the sub-pixel B increases, and thus the entire brightness is adjusted so as to satisfy a gamma characteristic.

[0012] There are a plurality of ways to differentiate the electric potential of the sub-pixel A from the electric potential of the sub-pixel B. For example, a dedicated TFT is provided for each sub-pixel as shown in Fig. 5A and, as shown in an equivalent circuit of Fig. 5C, two source bus lines are provided for the same gate bus line using the pattern of the counter electrode ITO as shown in Fig. 5B. By driving TFTs for the sub-pixels A and B, the electric potential of the sub-pixel A can be differentiated from the electric potential of the sub-pixel B.

[0013] More specifically, in Fig. 5A, a pixel electrode for the sub-pixel A is denoted by Px1, and a pixel electrode for the sub-pixel B is denoted by Px2. A TFT for driving the pixel electrode Px1 is denoted by TFT1, and a TFT for driving the pixel electrode Px2 is denoted by TFT2. In the pixel electrodes Px1 and Px2, there are slits for inclining liquid crystal at an angle of 45 degrees, which is unique to the VA mode, and part of the slits are also used as slits for separating the pixel electrode Px1 from the pixel electrode Px2. Similarly, liquid-crystal orientation regulation means is necessary for the common electrode provided on the counter substrate. In Fig. 5A, the slits are indicated by broken lines, and the slits only for the counter electrode are shown in Fig. 5B. Here, an insulator protrusion may be formed on the common electrode as orientation regulation means. As shown in the equivalent circuit of Fig. 5C, the pixel electrodes Px1 and Px2 are electrically independent, and what voltages are to be applied to the pixel electrodes Px1 and Px2 are determined by a control circuit.

SUMMARY OF THE INVENTION

[0014] As described above, vertical line inversion has an advantage over dot inversion in terms of power consumption. However, a problem may occur in a moving image regardless of frame frequency. For example, as shown in Fig. 6, when an area having a uniform tone (in this case, a box-shaped area indicated by α in Fig. 6) moves by one dot per frame, inconsistencies in the form of vertical streaks of one-dot pitch clearly appear, as shown in Fig. 7, in this area α. This phenomenon is related to the moving speed of the area α. If the area α is still, the inconsistencies do not appear. If the moving speed is two dots per frame, the inconsistencies do not appear; however, if the moving speed is three dots per frame, the inconsistencies appear again.

[0015] A cause of this phenomenon will be described using Figs. 8 and 9. First, when the common voltage of the common electrode is shifted to Vcom' from the central electric potential Vcom which is the center point between the positive and negative voltages, a difference occurs in brightness between the positive and negative polarities, as shown in Fig. 8. As described above, if the driving frequency is high to a certain level (for example, in the case of driving at 120 Hz, flicker occurs at a frequency of 60 Hz), when the area α is still, this difference in brightness is not perceived by the human eye.

[0016] However, it has been proved that when this area α moves by one dot per frame as shown in Fig. 9A, the line of sight of a person moves by one dot per frame in synchronization with the movement of the area α. As a result, the positions of bright and dark columns are fixed with respect to the outline of the area α whose shape is a box and on which a person focuses, whereby inconsistencies in the form of vertical streaks appear because of a difference in brightness between the positive and negative polarities. In contrast, as shown in Fig. 9B, when the area α moves by two dots per frame, the positions of bright and dark columns change with respect to the outline of the area α, inconsistencies in the form of vertical streaks do not appear.

[0017] In this way, vertical line inversion has an advantage over dot inversion in terms of power consumption; however, it is necessary to solve the problem of the occurrence of inconsistencies in the form of vertical streaks described using Figs. 6 through 9B.

[0018] Regarding the above-described multi-pixel structure, similarly to the case described using Fig. 1, there is an arrangement in which only pixel electrodes Px1 are connected to a source bus line and only pixel electrodes Px2 are connected to the next source line; however, it is necessary to employ the arrangement of pixels shown in Fig. 10 in order to solve the problem of the occurrence of inconsistencies in the form of vertical streaks described using Figs. 6 through 9B.

[0019] In Fig. 10, the pixel electrodes Px1 and Px2

each have a dedicated TFT. The pixel electrodes Px1 and Px2 are connected to right and left source bus lines in a checkerboard manner. Thus, for each source bus line, the pixel electrodes Px1 and Px2 are alternately connected such as Px1, Px2, Px1, Px2, and so on.

[0020] Figs. 11A through 12C show patterns of writing polarity in Fig. 10. Fig. 11A shows a pattern of the polarity arrangement of all the polarities detected through each of the bus lines in the k-th frame. Fig. 11B shows a pattern of the polarity arrangement regarding only the pixel electrodes Px1 in the k-th frame. Fig. 11C shows a pattern of the polarity arrangement regarding only the pixel electrodes Px2 in the k-th frame. Fig. 12A shows a pattern of the polarity arrangement of all the polarities detected through each of the bus lines in the k+1-th frame. Fig. 12B shows a pattern of the polarity arrangement regarding only the pixel electrodes Px1 in the k+1-th frame. Fig. 12C shows a pattern of the polarity arrangement regarding only the pixel electrodes Px2 in the k+1-th frame. Here, bold pluses (+) and bold minuses (-) indicate the pixel electrodes Px1 and regular pluses (+) and regular minuses (-) indicate the pixel electrodes Px2.

[0021] As shown in Figs. 11A and 12A, the output of source bus lines indicates vertical line inversion, and it is advantageous in terms of power consumption. As shown in Figs. 11B and 11C and Figs. 12B and 12C, the polarities of the pixels for the pixel electrodes Px1 are arranged in a checkerboard manner and the polarities of the pixels for the pixel electrodes Px2 are arranged in a checkerboard manner. Thus, even when the electric potential of the common electrode becomes shifted from the central electric potential Vcom, which is optimal, and a difference in brightness occurs, the difference in brightness is canceled out between pixels positioned within a short distance, whereby perceptible inconsistencies do not occur.

[0022] However, there is a new problem regarding the structure described using Figs. 10 through 12C. More specifically, in the operation of writing described using Figs. 11A through 12C, the polarity of the outputs of specific source bus lines is not inverted and consumption power is suppressed. For example, when the entire screen is white, that is, in the case of a tone of 255/255, the maximum voltage is applied to all pixels including the pixel electrodes Px1 and Px2; however, since there is no change in voltage and the maximum voltage is supplied to the bus lines on every occasion, it is almost not necessary for a driver IC to feed a current and power consumption is significantly small. However, when a halftone is displayed, it is necessary to differentiate the sub-pixel A from the sub-pixel B in terms of brightness in each pixel having a multi-pixel structure. Thus, for example, in the case of a tone of about 64/255, a tone difference is caused such as a tone of 240/255 for the pixel electrodes Px1 and a tone of 0/255 for the pixel electrodes Px2. An actual source driver operates with a large difference in electric potential such as 240/255, 0/255, 240/255, 0/255, and so on, whereby a power-consumption suppression effect decreases and the power consumption becomes almost the same as that in dot inversion driving.

[0023] In an image that is actually displayed (for example, an image received and displayed by a television tuner), a video whose images are all white is quite rare, and a video usually contains many halftones. Thus, the structure described using Figs. 10 through 12C greatly decreases an advantage obtained as a result of employment of vertical line inversion in terms of the entire power consumption.

[0024] Moreover, with the structure described using Figs. 10 through 12C, uniform display is performed as shown in Fig. 13A at room temperature; however, when the temperature is low, the inconsistencies in the form of streaks occur which correspond to the pitch with which drivers are implemented, as shown in Fig. 13B.

[0025] Using Figs. 14A though 16B, a cause of the streaks in the forms of streaks will be described. Figs. 14A and 14B show a voltage Vg of a gate bus line, a voltage Vs of a source bus line, and a voltage Vpx of a pixel electrode in a halftone (for example, a tone of 127/255) when an ideal waveform is input. Fig. 14A shows the operation of writing to a pixel electrode Px1, and Fig. 14B shows the operation of writing to a pixel electrode Px2. The voltage Vs of a source bus line changes by a large difference in electric potential in such a manner that the level of halftone changes such as 240/255, 0/255, 240/255, 0/255, and so on. In a state in which the write gate pulse is high, electric current flows between a pixel electrode and a corresponding source bus line via a TFT, and the voltage Vpx of the pixel electrode changes.

[0026] Figs. 15A and 15B show the voltage Vg of a gate bus line, the voltage Vs of a source bus line, and the voltage Vpx of a pixel electrode in a halftone (for example, a tone of 127/255) when a delay time in a bus line is assumed. Fig. 15A shows the operation of writing to a pixel electrode Px1, and Fig. 15B shows the operation of writing to a pixel electrode Px2. When driving is performed at room temperature, the operation of writing is performed in a state that is almost similar to the state as shown in Figs. 15A and 15B. In such a case, the gate pulse and the source voltage are attenuated at a portion where the gate pulse rises, and thus more time is necessary to charge a pixel electrode than in a state described using Figs. 14A and 14B. However, normally, TFTs are designed to be able to perform the operation of writing even in such a state, and thus no problem occurs.

[0027] However, if the temperature further lowers, the mobility of TFTs decreases, whereby more time is necessary for charging. Figs. 16A and 16B show the voltage Vg of a gate bus line, the voltage Vs of a source bus line, and the voltage Vpx of a pixel electrode in a halftone (for example, a tone of 127/255) when a delay time in a bus line is assumed and the performance of TFTs becomes low at low temperatures. Fig. 16A shows the operation of writing performed to a pixel electrode Px1, and Fig.

16B shows the operation of writing performed to a pixel electrode Px2. In the case shown in Figs. 16A and 16B, the delayed voltage of a source bus line affects the operation of writing, whereby inconsistencies in the form of streaks as described using Fig. 13B occur.

[0028] As a matter of course, it is possible to decrease the inconsistencies in the form of streaks as shown in Fig. 13B by designing a TFT in such a manner that it mainly supports low temperatures. However, if the size of the TFT becomes large for the design, the risk of occurrence of different problems may arise. For example, the aperture ratio lowers, or the inconsistencies become worse because of an increased delay time which is caused by the increase in gate load. The higher the writing speed, for example, 120 Hz or 240 Hz, the greater the effect of such problems. Thus, conditions become worse.

[0029] The present invention has been made in light of such circumstances, and it is desirable to suppress the occurrence of inconsistencies in the form of streaks and to decrease a necessary capacity of a memory without the size of a TFT being increased.

[0030] A liquid crystal display device according to embodiments of the present invention is defined by claims 1-3.

BRIEF DESCRIPTION OF THE DRAWINGS

[0031]

Fig. 1 is a diagram for describing an active matrix of a liquid crystal display panel;
Fig. 2 is a diagram for describing patterns of the polarity arrangement of pixels in a case where liquid crystal is driven;
Fig. 3 is a diagram for describing patterns of the polarity arrangement of pixels in a case where liquid crystal is driven;
Fig. 4 is a diagram for describing a multi-pixel structure used for achieving a wide viewing angle;
Figs. 5A through 5C are diagrams for describing a multi-pixel structure used for achieving a wide viewing angle;
Fig. 6 is a diagram for describing the occurrence of inconsistencies in the form of vertical streaks when vertical line inversion is performed;
Fig. 7 is a diagram for describing the occurrence of inconsistencies in the form of vertical streaks when vertical line inversion is performed;
Fig. 8 is a diagram for describing the occurrence of inconsistencies in the form of vertical streaks when vertical line inversion is performed;
Figs. 9A and 9B are diagrams for describing the occurrence of inconsistencies in the form of vertical streaks when vertical line inversion is performed;
Fig. 10 is a diagram for describing the arrangement of pixels for solving a problem of the occurrence of inconsistencies in the form of vertical streaks;
Figs. 11A through 11C are diagrams for describing patterns of writing polarity in Fig. 10;
Figs. 12A through 12C are diagrams for describing patterns of writing polarity in Fig. 10;
Figs. 13A and 13B are diagrams for describing the occurrence of inconsistencies in the form of streaks at low temperatures;
Figs. 14A and 14B are diagrams for describing the occurrence of inconsistencies in the form of streaks at low temperatures;
Figs. 15A and 15B are diagrams for describing the occurrence of inconsistencies in the form of streaks at low temperatures;
Figs. 16A and 16B are diagrams for describing the occurrence of inconsistencies in the form of streaks at low temperatures;
Fig. 17 is a block diagram showing the structure of a display device;
Fig. 18 is a diagram for describing a first driving example executed in the display device;
Figs. 19A through 19D are diagrams for describing a second driving example executed in the display device;
Figs. 20A through 20D are diagrams for describing the second driving example executed in the display device;
Figs. 21A and 21B are diagrams for describing voltages applied to a TFT in the second driving example;
Fig. 22 is a diagram for describing sub-frames;
Figs. 23A and 23B are diagrams for describing selected lines and inversion of a polarity signal in the case of Fig. 22;
Fig. 24 is a diagram for describing driving signals in the case of Fig. 22;
Fig. 25 is a diagram for describing sub-frames when a frame is divided;
Figs. 26A through 26C are diagrams for describing selected lines and inversion of a polarity signal in the case of Fig. 25;
Fig. 27 is a diagram for describing driving signals in the case of Fig. 25;
Fig. 28 is a diagram for describing driving waveforms in the case of Fig. 25;
Fig. 29 is a diagram for describing sub-frames in a case where frame division for odd lines is different from frame division for even lines; and
Figs. 30A through 30C are diagrams for describing selected lines and inversion of a polarity signal in the case of Fig. 29.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0032] In the following, embodiments of the present invention will be described with reference to the drawings.

[0033] Fig. 17 is a block diagram showing the structure of a display device 51. The display device 51 includes a control unit 71, a read-only memory (ROM) 72, a frame

buffer 73, a gate driver 74, a source driver 75, and a liquid crystal display (LCD) panel 76.

[0034] The control unit 71 is a unit for controlling the display device 51, and includes a receiver 91, a data sorting unit 92, a signal processing unit 93, a timing generator 94, and a memory controller 95. The control unit 71 performs signal processing (for example, color control and the like) unique to the display device 51 and also controls the gate driver 74 and the source driver 75 for driving scanning (gate) lines and data (source) lines of the LCD panel 76 in order to write image data to pixels for display.

[0035] The receiver 91 receives a video signal input from the outside, and supplies the video signal to the data sorting unit 92.

[0036] The data sorting unit 92 executes sorting of the data of an input image, and supplies the sorted input image to the signal processing unit 93.

[0037] The signal processing unit 93 refers to a parameter stored in the ROM 72, and executes gamma correction or signal processing for compensating the response of the liquid crystal and the voltage with which the operation of writing is performed to a pixel. The signal processing unit 93 supplies the processed signal to the timing generator 94 or the memory controller 95.

[0038] The timing generator 94 includes a timing generator 111 for controlling drivers, a data formatter 112, and a transmitter 113, and is a unit for performing the most basic control regarding display of the display device 51.

[0039] The timing generator 111 for controlling drivers generates a control signal for controlling the gate driver 74 for driving display elements and the source driver 75 for writing image data to pixels in accordance with the signal supplied from the signal processing unit 93, the gate driver 74 being for scanning.

[0040] The data formatter 112 converts the signal supplied from the signal processing unit 93 into a video signal whose signal format can be supplied to the source driver 75. The transmitter 113 sends the video signal converted by the data formatter 112 to the source driver 75.

[0041] The memory controller 95 controls input/output of a processed image signal to/from the frame buffer 73.

[0042] The ROM 72 stores a parameter which is necessary for the internal operation of the control unit 71 such as processing to be performed by the signal processing unit 93.

[0043] The frame buffer 73 stores image data in accordance with control performed by the memory controller 95.

[0044] A plurality of gate drivers 74 (here, three gate drivers 74-1 through 74-3) may be provided. The gate drivers 74 drive scanning (gate) lines that correspond to pixels arranged in matrix on the LCD panel 76, in accordance with control performed by the timing generator 111 for controlling drivers, and perform on/off control of active elements connected to gate bus lines.

[0045] A plurality of source drivers 75 (here, ten drivers 75-1 through 75-10) may be provided. The source drivers 75 convert, from digital to analog, the video signal supplied from the transmitter 113 into data to be written to pixels and drive corresponding source bus lines, in accordance with control performed by the timing generator 111 for controlling drivers, in such a manner that the video signal is displayed on display elements arranged in matrix on the LCD panel 76.

[0046] The LCD panel 76 includes liquid crystal display elements corresponding to the pixels arranged in matrix, and displays an image in accordance with the holding potential of the liquid crystal display elements.

[0047] The operation of the display device 51 will be described.

[0048] First, the receiver 91 of the control unit 71 receives a video signal, and supplies the video signal to the data sorting unit 92. The data sorting unit 92 sorts the data of the video signal and supplies the sorted video signal to the signal processing unit 93 in accordance with the setting recorded in the ROM 72, in such a manner that display can be performed, for example, as described in the following description using Figs. 18 through 30.

[0049] Then, the signal processing unit 93 performs one-to-one correction regarding RGB γ using a parameter recorded in the ROM 72, and supplies the resulting signal to the frame buffer 73 via the memory controller 95. The signal processing unit 93 reads an image signal which is delayed by one frame from the frame buffer 73 via the memory controller 95 and executes signal processing for compensating the response of the liquid crystal of the LCD panel 76 and the voltage with which the operation of writing is performed to a pixel, by performing comparison operation between the read image signal and an image signal of the next frame. The signal processing unit 93 supplies the processed signal to the timing generator 94.

[0050] The timing generator 111 for controlling drivers and data formatter 112 of the timing generator 94 receive the processed signal from the signal processing unit 93. The timing generator 111 for controlling drivers generates a control signal for controlling the gate drivers 74 and the source drivers 75 for driving display elements of the LCD panel 76, and outputs the control signal to the gate drivers 74 and the source drivers 75.

[0051] Then, the data formatter 112 converts the signal supplied from the signal processing unit 93 into a video signal whose signal format can be supplied to the source drivers, and supplies the video signal to the transmitter 113. The transmitter 113 sends the video signal converted by the data formatter 112 to the source drivers.

[0052] The source drivers 75 convert, from digital to analog, the video signal supplied from the transmitter 113 into data to be written to pixels and drive corresponding source bus lines to display the video signal on display elements arranged in matrix on the LCD panel 76 in accordance with control performed by the timing generator 111 for controlling drivers, whereby the LCD panel 76 displays an image. Here, the timing generator 111 for

controlling drivers controls the timing at which a polarity signal POL is inverted, the polarity signal POL being used to determine the output characteristics of the source drivers 75. The inversion of the polarity signal POL and the writing polarities for pixels will be specifically described below.

[0053] A first driving example executed in the display device 51 will be described with reference to Fig. 18.

[0054] One frame is divided into two sub-frames 1/2 and 2/2. The polarity of the source bus lines is not inverted in each of the sub-frames. The polarity of the source bus lines is inverted between the sub-frames. Furthermore, the gates of every other line are selected in units of one sub-frame. That is, one frame is divided into an odd sub-frame in which only odd lines are selected and an even sub-frame in which only even lines are selected.

[0055] In this case, the number of times the polarity inversion is performed increases to two times/frame, compared with existing vertical line inversion driving whose number of times the polarity inversion is performed is one time/frame. However, the number of times the polarity inversion is performed in this case is much less than that of dot-inversion driving (that is, the number of times the polarity inversion is performed is determined by the number of lines, and thus, for example, the number of times the polarity inversion is performed is 1080 in the case of full high-definition TV). Thus, the power consumption merely slightly increases.

[0056] The right side of Fig. 18 shows the polarity arrangement in units of one frame. In contrast to existing vertical line inversion driving in which positive polarities or negative polarities are continuously arranged in each vertical column on every occasion, if this proposed scheme is used, the polarity arrangement is equivalent to that of dot inversion driving at least during half a period of one frame, whereby a problem of flicker or inconsistencies in the form of vertical streaks in a moving image can be greatly reduced.

[0057] Next, as a second driving example executed in the display device 51, a case in which the LCD panel 76 having a multi-pixel structure is driven will be described.

[0058] In the display device 51, for example, the LCD panel 76 having a multi-pixel structure described using Figs. 4, 5, and 10 can also be driven. That is, each of the pixels can be divided into a plurality of pixels (here, two pixels of a sub-pixel A and a sub-pixel B). Regarding an input tone, the pixel is configured in such a manner that the brightness of the sub-pixel A first increases and then the brightness of the sub-pixel B increases, and thus the entire brightness is adjusted so as to satisfy a gamma characteristic. There are a plurality of ways to differentiate the electric potential of the sub-pixel A from the electric potential of the sub-pixel B. For example, as described using Fig. 5A, a dedicated TFT is provided for each sub-pixel and, as shown in the equivalent circuit as described using Fig. 5C, two source bus lines are provided for the same gate bus line using the pattern of a counter electrode ITO as described using Fig. 5B and the TFTs for the sub-pixels A and B can individually be driven.

[0059] Then, the pixel arrangement of the LCD panel 76 is the same as that described using Fig. 10. That is, the pixel electrode for the sub-pixel A is denoted by Px1, and the pixel electrode for the sub-pixel B is denoted by Px2. The TFT for driving the pixel electrode Px1 is denoted by TFT1, and the TFT for driving the pixel electrode Px2 is denoted by TFT2. The pixel electrodes Px1 and Px2 each have a dedicated TFT. The pixel electrodes Px1 and Px2 are connected to right and left source bus lines in a checkerboard manner. Thus, for each source bus line, the pixel electrodes Px1 and Px2 are alternately connected such as Px1, Px2, Px1, Px2, and so on.

[0060] Even in a case of driving such pixels having a multi-pixel structure, in the display device 51, one frame is divided into sub-frames 1/2 and 2/2. The polarity of the source bus lines is not inverted in each of the sub-frames and the polarity of the source bus lines is inverted between the sub-frames. Moreover, the gates of every other line are selected in units of one sub-frame. That is, even in this case, one frame is divided into an odd sub-frame in which only odd lines are selected and an even sub-frame in which only even lines are selected. In this case, the polarity arrangement in the k-th frame is shown in Fig. 19 and the polarity arrangement in the k+1-th frame is shown in Fig. 20.

[0061] Here, bold pluses (+) and bold minuses (-) indicate the pixel electrodes Px1 and regular pluses (+) and regular minuses (-) indicate the pixel electrodes Px2. More specifically, in the k(1/2)-th frame shown in Fig. 19A, vertical lines of m1, m2+1, m1+2, and m2+3 correspond to the pixel electrodes Px1 and others correspond to the pixel electrodes Px2. In the k(2/2)-th frame shown in Fig. 19B, inversion occurs from the k(1/2)-th frame, and vertical lines of m2, m1+1, m2+2, and m1+3 correspond to the pixel electrodes Px1 and others correspond to the pixel electrodes Px2.

[0062] That is, in the polarity arrangement shown in Figs. 19A through 20D, the polarity is different between m1 and m2 and between m1+β and m2+β (β is an integer greater than or equal to 1). The polarity is the same between m1 and m1+1, between m2 and m2+1, between m1+β and m1+(β+1), and between m2+β and m2+(β+1) (β is an integer greater than or equal to 1).

[0063] In such a case, even when only odd lines are driven or only even lines are driven, each source bus line only drives either the pixel electrode Px1 or the pixel electrode Px2. Then, as shown in Figs. 19C and 19D and Figs. 20C and 20D, the pixel electrodes Px1 have a polarity arrangement equivalent to that of dot inversion driving and the pixel electrodes Px2 also have a polarity arrangement equivalent to that of dot inversion driving. That is, in the display device 51, when such driving is performed, a problem of flicker and inconsistencies in the form of vertical streaks in a moving image can be greatly reduced by the polarity arrangement obtained in a state in which driving of two sub-frames is finished.

[0064] When a halftone is displayed using pixels having a multi-pixel structure, in the related art, the voltage of source bus lines greatly changes, whereby the power consumption becomes large; however, as described using Figs. 19A through 20D, in the display device 51, the operation of writing is performed using a group of pixel electrodes Px1 or a group of pixel electrodes Px2 in units of a sub-frame. Thus, the change in voltage can be suppressed, whereby the power consumption can be prevented from becoming large. For example, in the case of uniform tone display over the entire display, no matter which tone is displayed, electric current flows the source bus lines for a moment when switching is performed between sub-frames and this happens only two times in one frame in such a case. In this way, in the display device 51, even when a halftone is displayed using pixels having a multi-pixel structure, the effects of vertical frame inversion can be utilized to the utmost.

[0065] Next, Fig. 21 shows voltages applied to a TFT in the display device 51. In Fig. 21, the central electric potential Vcom of the common voltage, the voltage Vg of a gate bus line, the voltage Vs of a source bus line, and the voltage Vpx of a pixel electrode.

[0066] As shown in Fig. 21, the change in the voltage Vs of a source bus line is small, even when the performance of the TFT lowers, the operation of writing data within a period is easily performed. Thus, as its effect, a safety margin of TFT performance can be obtained. As a result, the inconsistencies occurring at low temperatures can be decreased without increasing the burden due to the increase in the size of the TFT.

[0067] As described above, two sub-frames 1/2 and 2/2 are designed to drive only odd lines and only even lines, respectively. That is, in the display device 51, even in the case of pixels having a multi-pixel structure or even in the case of pixels having a general structure, for example, as shown in Fig. 22, driving is performed in such a manner that only the odd lines are first selected from the top of the screen and driven, and then only the even lines are selected from the top of the screen and driven.

[0068] Here, as shown in Fig. 23A, after the first line is driven, the third line is driven and then the fifth line is driven. After all the odd lines are driven, the second line, the fourth line, and so on are driven (the numbers in Fig. 23A indicate the driving order of the lines). Thus, as shown in Fig. 23B, the polarity signal POL changes once every time switching is performed between sub-frames (the numbers in Fig. 23B indicate the line number counted from the top of the screen).

[0069] Fig. 24 shows driving signals for operating the LCD panel 76 in the case described using Figs. 22 through 23B. In Fig. 24, GSTR_Left denotes a signal indicating the start of scanning odd lines, GSTR_Right denotes a signal indicating the start of scanning even lines, CGLK denotes a reference clock signal for horizontal synchronization, G1, G2, and so on each denote a gate-driving waveform of a corresponding line, and POL denotes a signal for controlling the driving polarity for source drivers.

[0070] In this way, in the case described using Figs. 22 through 23B, driving is performed in such a manner that after only the odd lines are selected from the top of the screen, only the even lines are selected from the top of the screen.

[0071] In contrast, one screen may be divided into a plurality of frames, and each of the frames may further be divided into two sub-frames 1/2 and 2/2 as described above.

[0072] That is, as described using Figs. 22 through 24, in order to divide one frame into two sub-frames 1/2 and 2/2 for driving only the odd lines and only the even lines, a frame memory of at least the capacity of storing one screen is necessary for storing an input signal. Thus, in the display device 51, as shown in Fig. 25, even in the case of pixels having a multi-pixel structure or even in the case of pixels having a general structure, one screen is divided into some areas, and odd and even sub-frames are switched therebetween several times within one frame. As the number of areas into which one screen is divided increases, a necessary capacity of a memory becomes smaller; however, the number of times the polarity inversion is performed increases and thus the power consumption increases. If the inversion is performed every line, it is the same as dot inversion driving and the power consumption is high; however, for example, if the inversion is performed every two lines, a power-consumption reducing effect can be obtained, compared with dot inversion driving.

[0073] For example, as shown in Fig. 26A, when one screen is divided into twelve areas along the horizontal direction, as shown in Fig. 26B, after the first line is driven, the third line is driven and then the fifth line is driven. After 32 odd lines to the 63rd line are driven, the second line, the fourth line, and so on are driven (the numbers in Fig. 26B indicate the driving order of the lines). Thus, as shown in Fig. 26C, the polarity signal POL changes 24 times within one frame, that is, the polarity signal POL changes once every time switching is performed between sub-frames in the frame that is divided into twelve areas (the numbers in Fig. 26C indicate the line number counted from the top of the screen).

[0074] Fig. 27 shows driving signals for operating the LCD panel 76 in the case described using Figs. 26A through 26C. In Fig. 27, GSTR_Left denotes a signal indicating the start of scanning odd lines, GSTR_Right denotes a signal indicating the start of scanning even lines, CGLK_Left denotes a reference clock signal for horizontal synchronization for odd lines, and CGLK_Right denotes a reference clock signal for horizontal synchronization for even lines. Here, as a matter of course, a reference clock signal may be a single signal as in the case described using Fig. 24. Moreover, G1, G2, and so on each denote a gate-driving waveform of a corresponding line, and POL denotes a signal for controlling the driving polarity for source drivers.

[0075] In this way, in the case described using Figs.

26A through 27, switching is performed between the sub-frames in the frame that is divided into twelve areas, and odd lines or even lines are driven in each sub-frame, whereby the power consumption can be suppressed and a necessary capacity of a memory can be smaller, compared with dot inversion driving.

[0076] Fig. 28 shows driving waveforms that operate each pixel of the LCD panel 76 in the driving method described using Figs. 26A through 27.

[0077] In Fig. 28, VCOM denotes the electric potential of the counter electrode regarding the electric potential of each of the pixels of the LCD panel 76. The display potential is determined by the capacitance determined by the counter electrode and the pixel. Then, S1 denotes a driving waveform of a source bus line, and G33 denotes a driving waveform of the 33rd scanning (gate) line, and POL denotes a signal for controlling the driving polarity for the source drivers 75.

[0078] While the first through 31st odd lines are being driven, that is, while the polarity signal POL is fixed, the source drivers 75 do not cause any change that crosses the electric potential VCOM and thus a rising time can be short. However, next, when the 33rd gate line is driven, that is, when odd-line driving is switched to even-line driving and when the polarity signal POL is inverted and the driving waveform G33 becomes high, a time period necessary for the electric potential of the source driver to become a desired level is longer than a fixed time period necessary for the electric potential of the source drivers to become a desired level in a state in which the polarity signal POL is fixed (Tr_B > Tr_A). Thus, for example, if Tr_B = Tr_A is set, a sufficient time period for performing an operation of writing is not obtained. Thus, as shown in Fig. 28, by setting the time period for performing an operation of writing at the 33rd gate line to be longer than other time periods for performing the operation of writing at other lines, conditions of the operation of writing are balanced. That is, it is preferable that the timings in Fig. 28 are set in such a manner that T3 > T1 and T1 = T2 = T4.

[0079] By performing setting in this way, a sufficient time period for performing the operation of writing can be obtained when the signal POL is inverted, and thus the occurrence of inconsistencies at this portion can be prevented.

[0080] Moreover, similarly, at other timings when odd-line driving is switched to even-line driving and when even-line driving is switched to odd-line driving, as a matter of course, the time period for performing the operation of writing at the first line after switching is performed should be set longer than other time periods for performing the operation of writing at other lines.

[0081] Then, furthermore, when one screen is divided into a plurality of frames, each frame may be divided into two sub-frames 1/2 and 2/2 in such a manner that an area in which odd lines are scanned and an area in which even lines are scanned do not match.

[0082] That is, as shown in Fig. 29, in the display device 51, even in the case of pixels having a multi-pixel structure or even in the case of pixels having a general structure, the position of each of the selected lines is made to be different between subsequent odd and even sub-frames and switching is performed between these sub-frames a plurality of times within one frame. In other words, in the display device 51, even in the case of pixels having a multi-pixel structure or even in the case of pixels having a general structure, the position at which the polarity signal POL changes can be set for each sub-frame in such a manner that the position for the sub-frame does not overlap the position for another sub-frame. The number of the selected lines in an odd sub-frame and the number of selected lines in an even sub-frame may be randomly set; however, for ease of control, they may be set in a predetermined regulated manner. Here, also, as the number of areas obtained as a result of division increase, a necessary capacity of a memory becomes smaller; however, the number of times the polarity inversion is performed increases and thus the power consumption increases. However, for example, if inversion is performed every two or more lines, a power-consumption reducing effect can be obtained, compared with dot inversion driving.

[0083] For example, as shown in Fig. 30A, when one screen is divided into twelve areas along the horizontal direction and the number of lines selected in the first odd sub-frame is half the number of the lines of one of the areas, as shown in Fig. 30B, after the first line is driven, the third line is driven and then the fifth line is driven. After 16 odd lines to the 31st line are driven, the second line, the fourth line, and so on are driven (the numbers in Fig. 30B indicate the driving order of the lines). Thus, as shown in Fig. 30C, the polarity signal POL changes 25 times, which is one time more than the case described using Figs. 26A and 26B, within one frame (the numbers in Fig. 30B indicate the line number counted from the top of the screen).

[0084] Here, even in this case, as described using Fig. 28, when odd-line driving is switched to even-line driving and when even-line driving is switched to odd-line driving, as a matter of course, it is preferable that the time period for performing the operation of writing at the first line after switching is performed is set to be longer than other time periods for performing the operation of writing at other lines.

[0085] In this way, in the case described using Fig. 30, in a frame that is divided into twelve areas, switching is performed between sub-frames in such a manner that the position of each of the selected lines is made to be different between the sub-frames, and odd lines or even lines are driven in each of the sub-frames, whereby the power consumption can be suppressed and a necessary capacity of a memory can be smaller, compared with dot inversion driving. Furthermore, positions at which the polarity signal POL changes can be dispersedly set for even lines and odd lines, and thus the inconsistencies that tend to occur at these positions can be suppressed and the LCD panel 76 can be easily controlled.

[0086] As described above, even when a half tone is displayed using pixels having a multi-pixel structure, in the display device 51, since the operation of writing is performed using a group of pixel electrodes Px1 or a group of pixel electrodes Px2 in units of a sub-frame, the changes in voltage can be suppressed, whereby the power consumption can be prevented from becoming large. For example, when a uniform tone is displayed over the entire screen, no matter which tone is displayed, electric current flows the source bus lines for a moment when switching is performed between sub-frames and this happens only two times in one frame in such a case. In this way, in the display device 51, even when a halftone is displayed using pixels having a multi-pixel structure, the effects of vertical frame inversion can be utilized to the utmost and a problem of flicker and inconsistencies in the form of vertical streaks in a moving image can be greatly reduced by the polarity arrangement obtained in a state in which driving of two sub-frames is finished.

[0087] Moreover, in the display device 51, even in the case of pixels having a multi-pixel structure or in the case of pixels having a general structure, one screen is divided into a plurality of frames along the horizontal direction, switching is performed between sub-frames in the frames, and odd lines or even lines can be driven in each of the sub-frames, whereby the power consumption can be suppressed and a necessary capacity of a memory can be smaller, compared with dot inversion driving.

[0088] Moreover, in the display device 51, even in the case of pixels having a multi-pixel structure or in the case of pixels having a general structure, the position of each of the selected lines is made to be different between subsequent odd and even sub-frames, in other words, the position at which the polarity signal POL changes can be set for each sub-frame in such a manner that the position for the sub-frame does not overlap the position for another sub-frame. Thus, compared with dot inversion driving, the power consumption can be suppressed and a necessary capacity of a memory can be smaller. Furthermore, the inconsistencies that tend to occur at positions at which the polarity signal POL changes can be suppressed and the LCD panel 76 can be easily controlled.

[0089] Here, description has been made by treating the display device 51 as a single device; however, the LCD panel 76 may be a separate device and the remaining portion may be configured as a display control device, as a matter of course.

[0090] The present application contains subject matter related to that disclosed in Japanese Priority Patent Applications JP 2008-075696 and JP 2008-075697 filed in the Japan Patent Office on March 24, 2008.

[0091] It should be understood by those skilled in the art that various modifications, combinations, sub-combinations and alterations may occur depending on design requirements and other factors insofar as they are within the scope of the appended claims or the equivalents thereof.

Claims

1. A liquid crystal display device, comprising:

a plurality of pairs of signal lines (m1, m2; m1+1, m2+1; m1+2, m2+2)extending in a column direction;
a plurality of scanning lines (n, n+1, n+2) extending in a row direction;
a plurality of pixels (Px(m,n)) arranged in a matrix, each pixel corresponding to one of said pair of signal lines (m1, m2) and to one of said plurality of scanning lines (n) and having a multi-pixel structure consisting of a first subpixel (Px1) connected to one of the signal lines (m1) of the pair and by a second subpixel (Px2) connected to the other of the signal lines (m2) of the pair ; wherein adjacent pixels (Px(m,n), Px(m,n+1)) connected to a same pair of signal lines (m1, m2) have respective first subpixels connected to a different one of the signal lines of the pair of signal lines (m1, m2), so that the first and second subpixels of each column of the matrix of pixels are connected in a checkerboard manner with respect to first and second lines of the corresponding pair of signal lines, and
wherein adjacent pixels (Px(m,n), Px(m+1,n)) connected to a same scanning line (n) have either respective first subpixels or respective second subpixels connected to the two adjacent lines (m2, m1+1) of their corresponding pair of signal lines (m1,m2; m1+1,m2+1), wherein a first line (m2) of the two adjacent lines belongs to the pair of signal lines (m1,m2) connected to the first pixel (Px(m,n)) and the second line (m1+1) of the two adjacent lines belongs to the pair of signal lines (m1+1, m2+1) connected to the second pixel (Px(m+1,n));
first driving means (74) for driving the scanning lines;
second driving means (75) for driving the signal lines;
image acquisition means for acquiring an image signal to be displayed on the display; and
control means (71) for controlling the first driving means (74) and the second driving means (75) in accordance with the image signal acquired by the image acquisition means, and
characterized in that
in order to improve the viewing angle characteristics in halftones, the control circuit (71) is configured to drive a pixel in such a manner that, as an input tone for the pixel increases, the brightness of its first subpixel first increases, and then the brightness of its second subpixel increases,
wherein, the control means (71) is arranged to control the first driving means (74) in such a manner that all horizontal scanning lines of a

frame are scanned by scanning a first sub-frame in which only odd lines of horizontal scanning lines are scanned followed by a second sub-frame in which only even lines of horizontal scanning lines are scanned,
wherein the control means (71) is arranged to control the second driving means (75) in such a manner that each signal line is provided with data having a constant polarity during the whole frame, and adjacent signal lines are provided with data having different polarities, so that
the polarity of the first subpixel of each of the pixels differs from the polarity of the second subpixel of the pixel,
the polarities of the first subpixels of adjacent pixels connected either to a same pair of signal lines (m1, m2) or to a same scanning line (n) differ from each other,
and the polarities of the second subpixels of adjacent pixels connected either to a same pair of signal lines (m1, m2) or to a same scanning line (n) differ from each other.

2. The liquid crystal display device according to Claim 1,
wherein the control means (71) divides all horizontal scanning lines (n, n+1, n+2) of the display into a plurality of areas constituted by four lines or more, and controls the first driving means (74) in such a manner that all horizontal scanning lines (n, n+1, n+2) of one frame are scanned by executing scanning of the first sub-frame and the second sub-frame in the plurality of areas.

3. The liquid crystal display device according to Claim 1 or 2,
wherein the control means (71) sets a time period for performing an operation of writing at the first horizontal scanning line (n) after switching is performed between the first sub-frame and the second sub-frame, to be longer than a time period for performing the operation of writing at another horizontal scanning line (n+1, n+2).

Patentansprüche

1. Flüssigkristallanzeigevorrichtung aufweisend:

eine Mehrzahl von Paaren von Signalleitungen (m1, m2; m1+1, m2+1, m1+2, m2+2), die sich in Spaltenrichtung erstrecken;
eine Mehrzahl von Abtastleitungen (n, n+1, n+2), die sich in Zeilenrichtung erstrecken;
eine Mehrzahl von Bildpunkten (Px, (m, n)), die in einer Matrix angeordnet sind, wobei jeder Bildpunkt einem der Paare der Signalleitungen (m1, m2) und einer der Mehrzahl der Abtastleitungen (n) entspricht und einen Mehrfachbildpunktaufbau hat, der aus einem ersten Subbildpunkt (Px1) und einem zweiten Subbildpunkt (Px2) besteht, wobei der erste Subbildpunkt (Px1) mit einer der Signalleitungen (m1) des Paares verbunden ist und wobei der zweite Subbildpunkt (px2) mit der anderen der Signalleitungen des Paares verbunden ist;
wobei benachbarte Bildpunkte (Px (m,n), Px (m, n+1), die mit dem gleichen Paar von Signalleitungen (m1, m2) verbunden sind, entsprechende erste Subbildpunkte haben, die mit unterschiedlichen Signalleitungen des Paares von Signalleitungen (m1, m2) verbunden sind, so dass die ersten und zweiten Subbildpunkte jeder Spalte der Matrix von Bildpunkten in einer Schachbrettart in Bezug auf die ersten und zweiten Leitungen des entsprechenden Paares der Signalleitungen verbunden sind, und
wobei benachbarte Bildpunkte (Px (m,n), Px (m+1,n)), die mit derselben Abtastleitung (n) verbunden sind, entweder entsprechende erste Subbildpunkte oder entsprechende zweite Subbildpunkte haben, die mit zwei benachbarten Leitung (m2, m1+1) ihres entsprechenden Paares von Signalleitungen (m1, m2; m1+1, m2+1) verbunden sind, wobei eine erste Leitungen (m2) der zwei benachbarten Leitungen zu dem Paar von Signalleitungen (m1, m2) gehört, das mit dem ersten Subpixel (Px (m,n) verbunden ist, und die zweite Leitung (m1+1) der beiden benachbarten Leitungen zu dem Paar von Signalleitungen (m1+1, m2+1) gehört, die mit dem zweiten Subpixel (Px (m+1, n)) verbunden ist;
erste Ansteuermittel (74) zum Ansteuern der Abtastleitungen;
zweite Ansteuermittel (75) zum Ansteuern der Signalleitungen;
Bilderlangungsmittel zum Erlangen eines Bildsignals, welches auf der Anzeige anzuzeigen ist; und
Steuerungsmittel (71) zum Steuern der ersten Ansteuermittel (74) und der zweiten Ansteuermittel (75) entsprechend dem Bildsignal, das von dem Bilderlangungsmittel erlangt wurde, und
dadurch gekennzeichnet, dass um die Betrachtungswinkeleigenschaft in Rasterbildern zu verbessern, der Steuerschaltkreis (71) eingerichtet ist, einen Bildpunkt in einer solchen Weise anzusteuern, wenn sich ein eingegebener Farbwert für den Bildpunkt erhöht,
sich die Helligkeit seines ersten Subbildpunkts erst erhöht und sich dann die Helligkeit seinen zweiten Subbildpunkts erhöht,
wobei das Steuerungsmittel (71) eingerichtet ist, das erste Ansteuermittel (74) in einer solchen Weise zu steuern, dass alle horizontalen Abtast-

leitungen eines Bilds (frame) durch Abtasten eines ersten Teilbilds (sub-frame) abgetastet werden, in dem nur ungerade Leitungen der horizontalen Abtastleitungen abgetastet werden, gefolgt von einem zweiten Teilbild, in dem nur gerade Leitungen der horizontalen Abtastleitungen abgetastet werden,
wobei die Steuerungsmittel (71) eingerichtet sind, die zweiten Ansteuermittel (75) in einer solchen Weise zu steuern, dass jede Signalleitung mit Daten versorgt wird, die eine konstante Polarität während des gesamten Bildes haben und benachbarte Signalleitungen mit Daten versorgt werden, die unterschiedliche Polaritäten haben, so dass
die Polarität der ersten Subbildpunkte eines jeden Pixels von der Polarität der zweiten Subbildpunkte des Pixels verschieden sind,
die Polaritäten der ersten Subbildpunkte benachbarter Bildpunkte, die entweder zu dem gleichen Paar von Signalleitungen (m1, m2) oder zu derselben Abtastleitung (n) verbunden sind, verschieden voneinander sind,
und die Polaritäten der zweiten Subbildpunkte benachbarter Bildpunkte entweder mit dem gleichen Paar von Signalleitungen (m1, m2) oder derselben Abtastleitung (n) verbunden sind, voneinander verschieden sind.

2. Flüssigkristallanzeigevorrichtung nach Anspruch 1, wobei die Steuermittel (71) alle horizontalen Abtastleitungen (n, n+1, n+2) der Anzeige in einer Mehrzahl von Bereichen teilen, die durch vier Leitungen oder mehr gebildet werden und das die ersten Ansteuerungsmittel (74) in einer solchen Weise steuert, dass alle horizontalen Abtastleitungen (n, n+1, n+2) eines Bilds durch Ausführen des Abtastens des ersten Teilbilds und des zweiten Teilbilds in der Mehrzahl von Bereichen durchgeführt wird.

3. Flüssigkristallanzeigevorrichtung nach Anspruch 1 oder 2,
wobei die Steuerungsmittel (71) eine Zeitdauer zum Durchführen einer Operation des Schreibens auf der ersten horizontalen Abtastleitung (n) setzen, nachdem das Schalten zwischen dem ersten Teilbild und dem zweiten Teilbild durchgeführt wurde, länger zu sein als eine Zeitdauer zum Durchführen der Operation des Schreibens bei einer anderen horizontalen Abtastleitung (n+1, n+2).

Revendications

1. Dispositif d'affichage à cristaux liquides, comprenant :

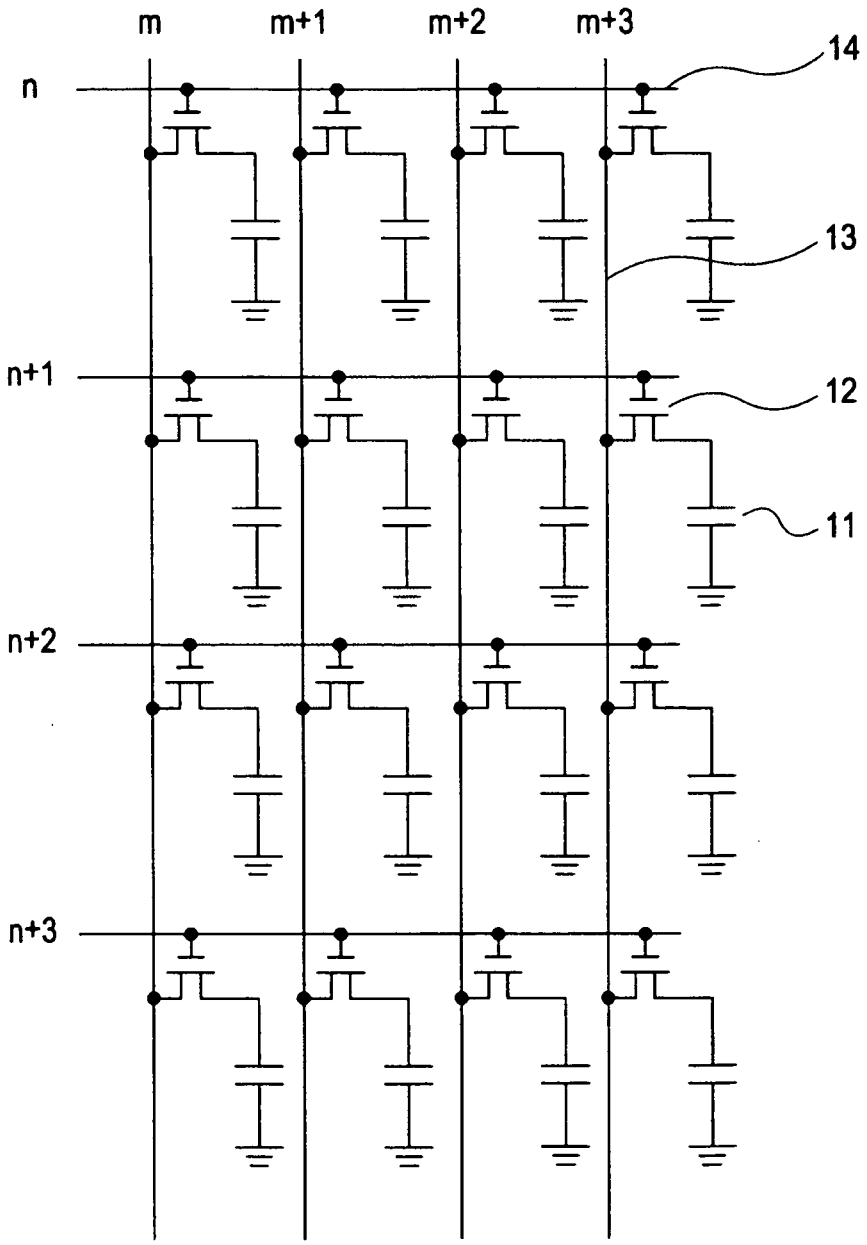
une pluralité de paires de lignes de signaux (m1, m2 ; m1+1, m2+1 ; m1+2, m2+2) s'étendant dans une direction de colonne ;
une pluralité de lignes de balayage (n, n+1, n+2) s'étendant dans une direction de rangée ;
une pluralité de pixels (Px(m,n)) agencés en une matrice, chaque pixel correspondant à l'une de ladite paire de lignes de signaux (m1, m2) et à l'une de ladite pluralité de lignes de balayage (n) et comportant une structure de multiples pixels comprenant un premier sous-pixel (Px1) connecté à l'une des lignes de signaux (m1) de la paire et un deuxième sous-pixel (Px2) connecté à l'autre des lignes de signaux (m2) de la paire ;
dans lequel des pixels adjacents (Px(m,n), Px (m,n+1)) connectés à une même paire de lignes de signaux (m1, m2) ont des premiers sous-pixels respectifs connectés à une ligne différente parmi les lignes de signaux de la paire de lignes de signaux (m1, m2), de sorte que les premier et deuxième sous-pixels de chaque colonne de la matrice de pixels sont connectés à la manière d'un damier par rapport à des première et deuxième lignes de la paire correspondante de lignes de signaux, et
dans lequel des pixels adjacents (Px(m,n), Px (m+l,n)) connectés à une même ligne de balayage (n) ont soit les premiers sous-pixels respectifs, soit les deuxièmes sous-pixels respectifs connectés aux deux lignes adjacentes (m2, m1+1) de leur paire correspondante de lignes de signaux (m1, m2 ; m1+1, m2+1), dans lequel une première ligne (m2) des deux lignes adjacentes appartient à la paire de lignes de signaux (m1, m2) connectées au premier pixel (Px(m,n)) et la deuxième ligne (m1+1) des deux lignes adjacentes appartient à la paire de lignes de signaux (m1+1, m2+1) connectées au deuxième pixel (Px(m+1,n)) ;
des premiers moyens de commande (74) pour commander les lignes de balayage ;
des deuxièmes moyens de commande (75) pour commander les lignes de signaux ;
des moyens d'acquisition d'image pour acquérir un signal d'image à afficher sur l'afficheur ; et
des moyens de contrôle (71) pour contrôler les premiers moyens de commande (74) et les deuxièmes moyens de commande (75) conformément au signal d'image acquis par les moyens d'acquisition d'image, et
caractérisé en ce que
afin d'améliorer les caractéristiques d'angle d'observation dans les demi-teintes, le circuit de contrôle (71) est configuré pour commander un pixel d'une manière telle que, alors qu'une teinte d'entrée pour le pixel augmente, la luminosité de son premier sous-pixel augmente en premier, et ensuite la luminosité de son deuxième

sous-pixel augmente,
dans lequel, les moyens de contrôle (71) sont agencés pour contrôler les premiers moyens de commande (74) d'une manière telle que toutes les lignes de balayage horizontal d'une trame soient balayées en balayant une première sous-trame dans laquelle seules les lignes impaires des lignes de balayage horizontal sont balayées, suivie d'une deuxième sous-trame dans laquelle seules les lignes paires des lignes de balayage horizontal sont balayées,
dans lequel les moyens de contrôle (71) sont agencés pour contrôler les deuxièmes moyens de commande (75) d'une manière telle que chaque ligne de signal soit pourvue de données ayant une polarité constante pendant la trame entière et que les lignes de signaux adjacentes soient pourvues de données ayant différentes polarités, de sorte que
la polarité du premier sous-pixel de chacun des pixels diffère de la polarité du deuxième sous-pixel du pixel,
les polarités des premiers sous-pixels de pixels adjacents connectés soit à une même paire de lignes de signaux (m1, m2), soit à une même ligne de balayage (n) diffèrent l'une de l'autre,
et les polarités des deuxièmes sous-pixels parmi les pixels adjacents connectés soit à une même paire de lignes de signaux (m1, m2), soit à une même ligne de balayage (n) diffèrent l'une de l'autre.

2. Dispositif d'affichage à cristaux liquides selon la revendication 1,
dans lequel les moyens de contrôle (71) divisent toutes les lignes de balayage horizontal (n, n+1, n+2) de l'afficheur en une pluralité de zones constituées de quatre lignes ou plus, et contrôlent les premiers moyens de commande (74) d'une manière telle que toutes les lignes de balayage horizontal (n, n+1, n+2) d'une trame soient balayées en exécutant un balayage de la première sous-trame et de la deuxième sous-trame dans la pluralité de zones.

3. Dispositif d'affichage à cristaux liquides selon la revendication 1 ou 2,
dans lequel les moyens de contrôle (71) déterminent une période de temps pour effectuer une opération d'écriture sur la première ligne de balayage horizontal (n) après qu'une commutation a été effectuée entre la première sous-trame et la deuxième sous-trame, pour qu'elle soit plus longue qu'une période de temps pour effectuer l'opération d'écriture sur une autre ligne de balayage horizontal (n+1, n+2).

FIG. 1



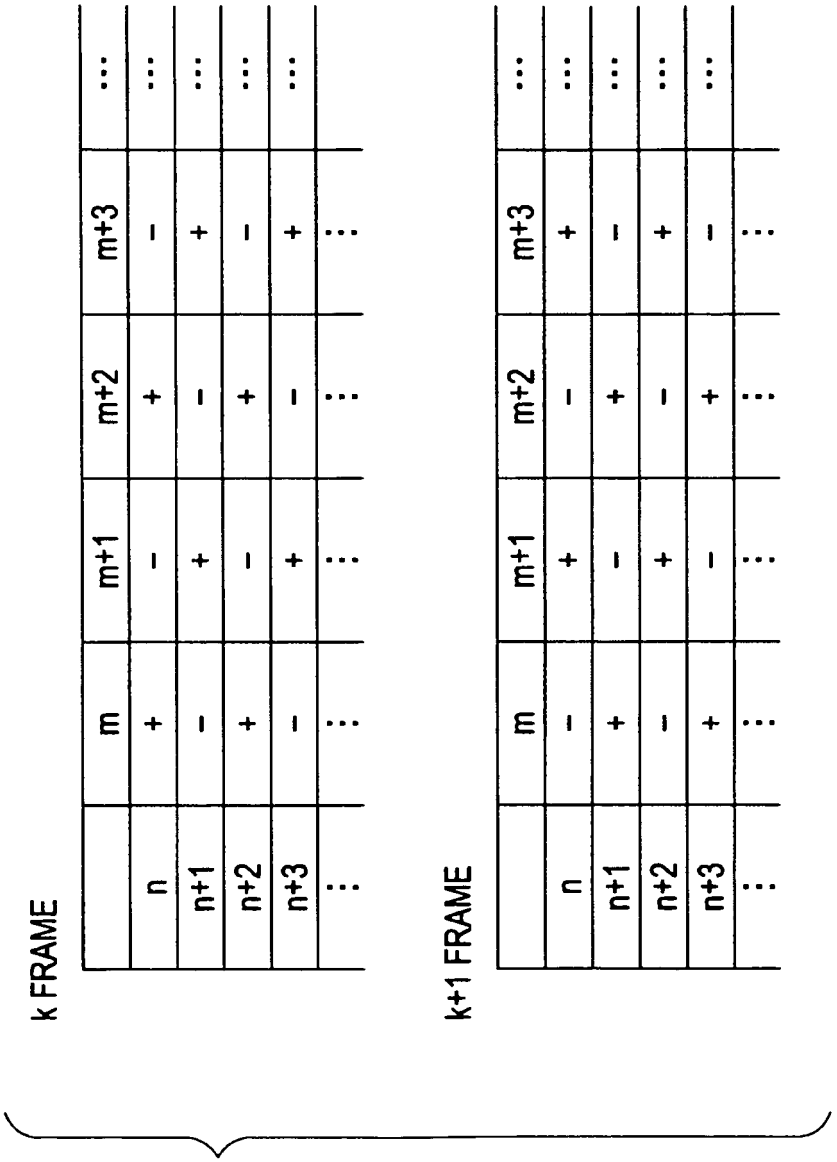


FIG. 2

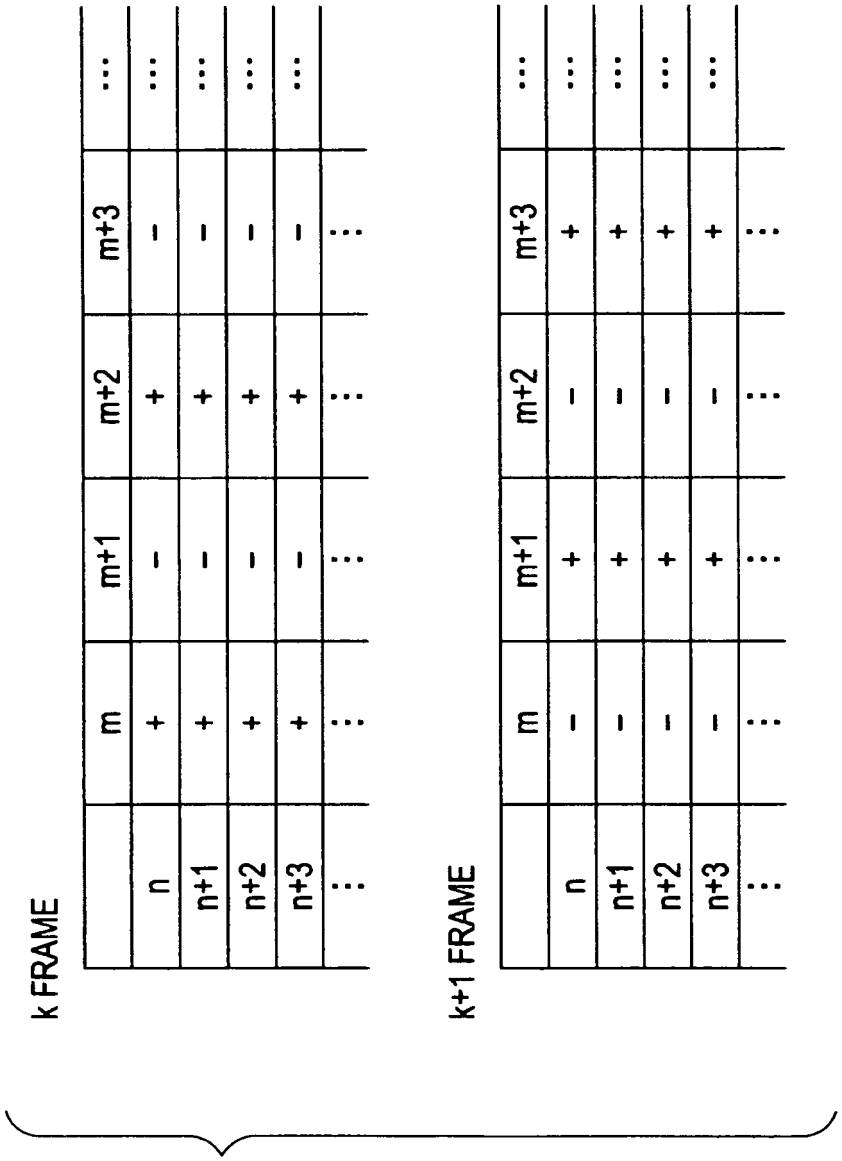


FIG. 3

FIG. 4

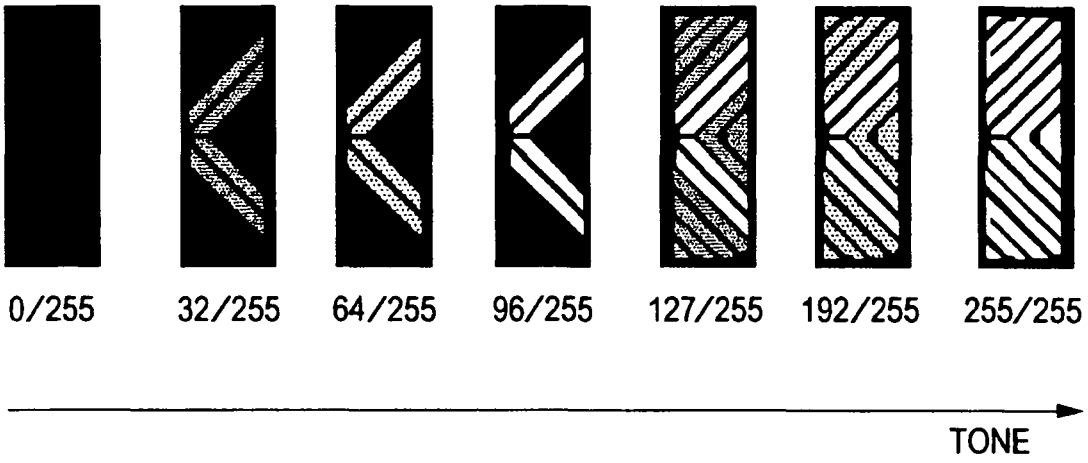


FIG. 5A

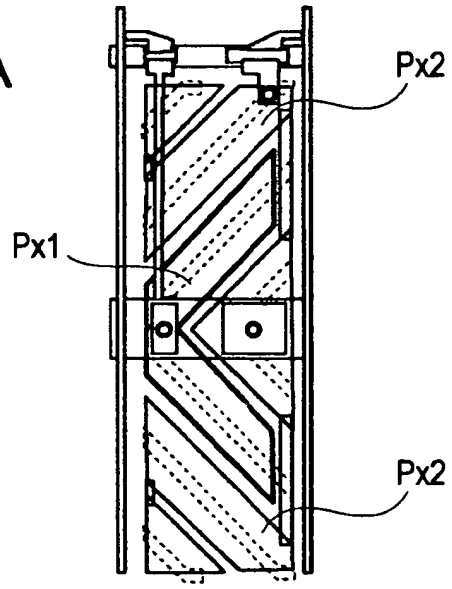


FIG. 5B

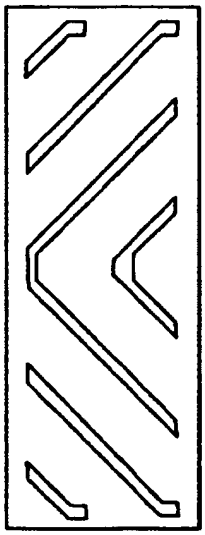


FIG. 5C

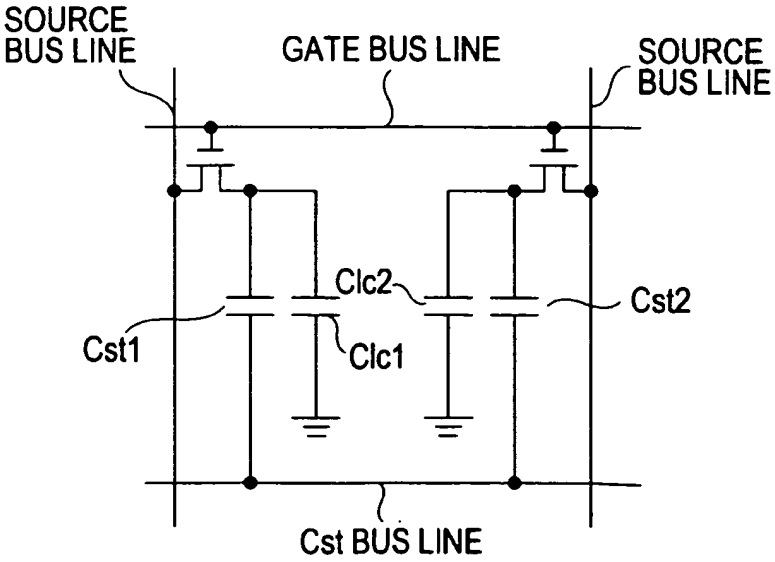


FIG. 6

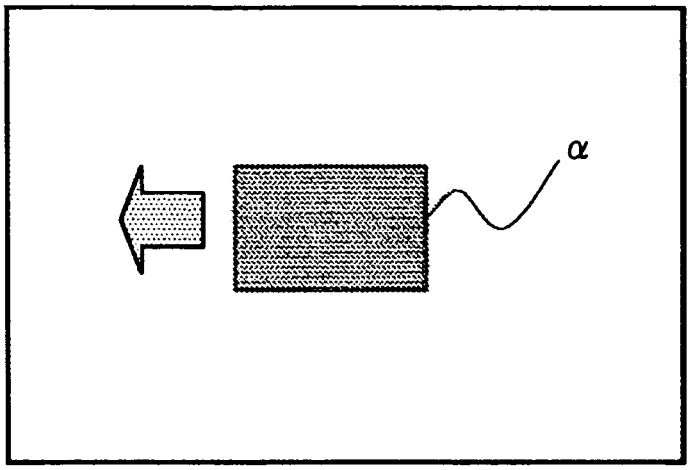


FIG. 7

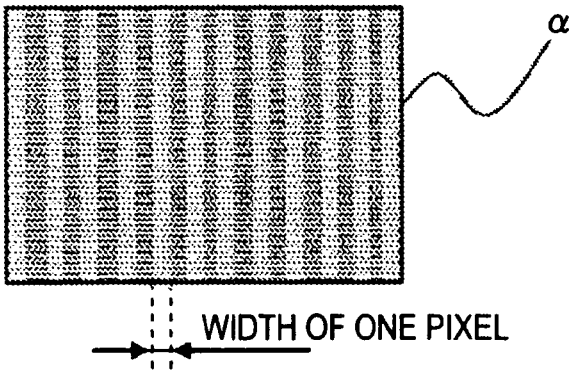


FIG. 8

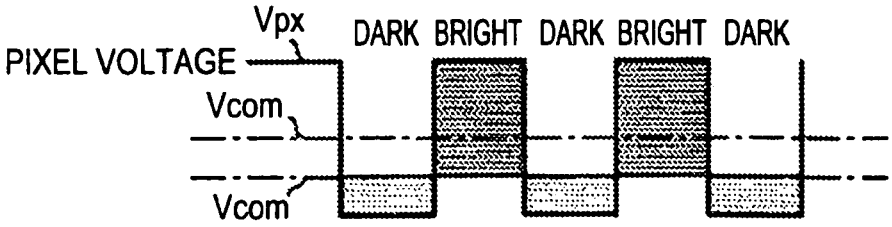


FIG. 9A

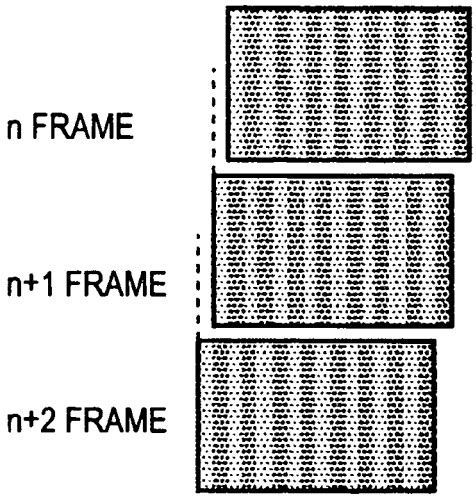


FIG. 9B

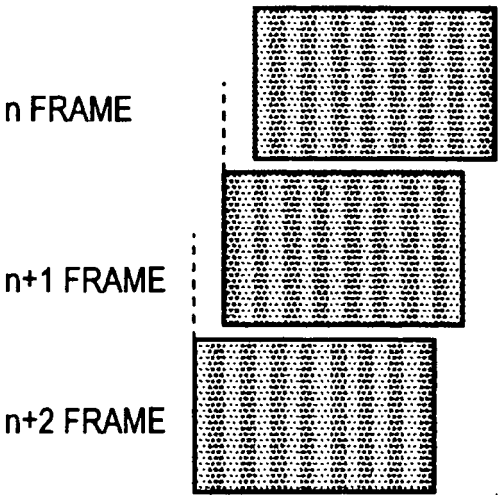


FIG. 10

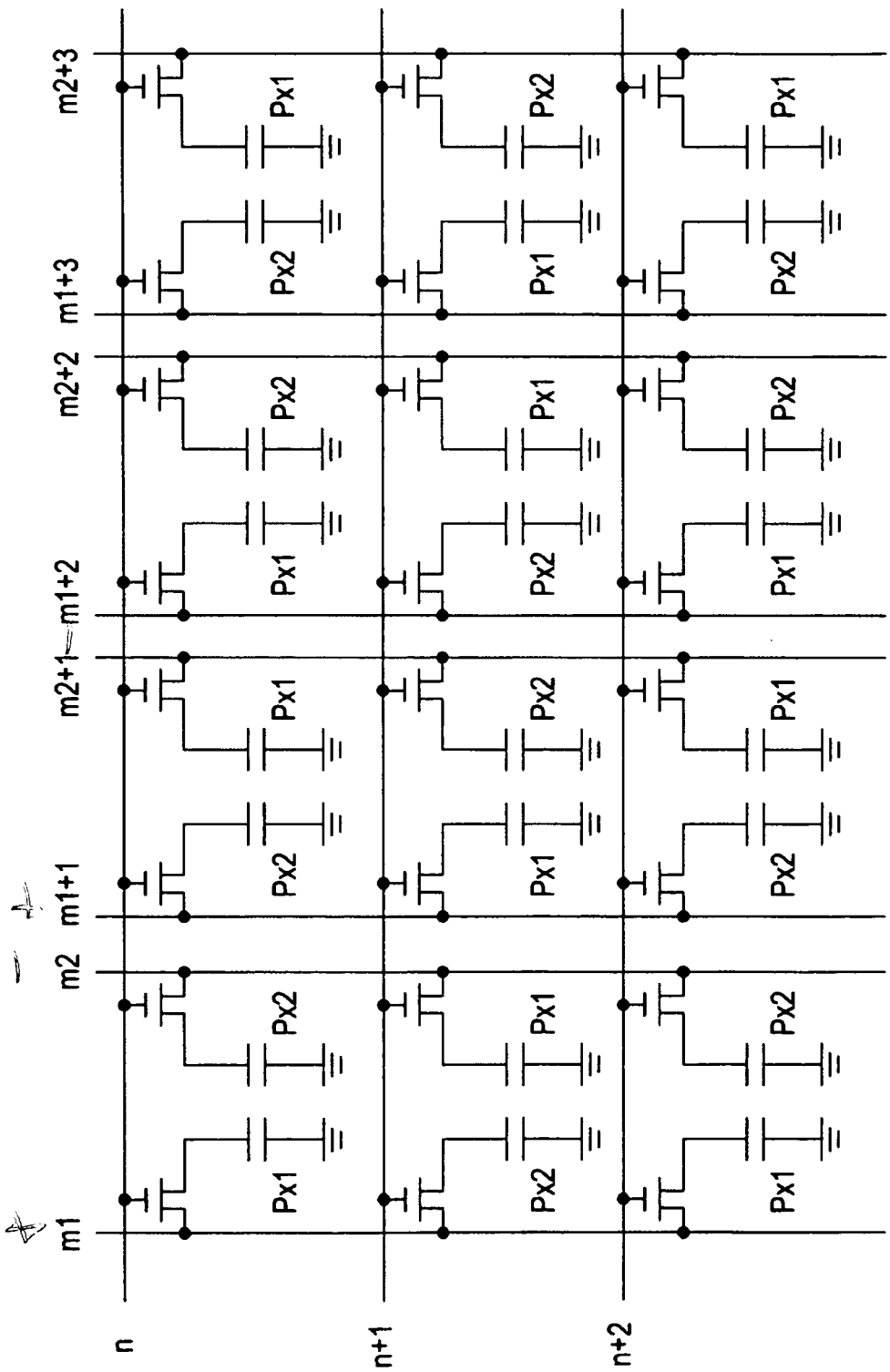


FIG. 11A

	m1	m2	m1+1	m2+1	m1+2	m2+2	m1+3	m2+3	
n	+	−	+	−	+	−	+	−	···
n+1	+	−	+	−	+	−	+	−	···
n+2	+	−	+	−	+	−	+	−	···
n+3	+	−	+	−	+	−	+	−	···
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	

FIG. 11B

	i=0	i=1	i=2	i=3	
n	+	−	+	−	···
n+1	−	+	−	+	···
n+2	+	−	+	−	···
n+3	−	+	−	+	···
⋮	⋮	⋮	⋮	⋮	

FIG. 11C

	i=0	i=1	i=2	i=3	
n	−	+	−	+	···
n+1	+	−	+	−	···
n+2	−	+	−	+	···
n+3	+	−	+	−	···
⋮	⋮	⋮	⋮	⋮	

FIG. 12A

	m1	m2	m1+1	m2+1	m1+2	m2+2	m1+3	m2+3	
n	−	+	−	+	−	+	−	+	···
n+1	−	+	−	+	−	+	−	+	···
n+2	−	+	−	+	−	+	−	+	···
n+3	−	+	−	+	−	+	−	+	···
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	

FIG. 12B

	i=0	i=1	i=2	i=3	
n	−	+	−	+	···
n+1	+	−	+	−	···
n+2	−	+	−	+	···
n+3	+	−	+	−	···
⋮	⋮	⋮	⋮	⋮	

FIG. 12C

	i=0	i=1	i=2	i=3	
n	+	−	+	−	···
n+1	−	+	−	+	···
n+2	+	−	+	−	···
n+3	−	+	−	+	···
⋮	⋮	⋮	⋮	⋮	

FIG. 13A

ROOM TEMPERATURE
NORMAL STATE

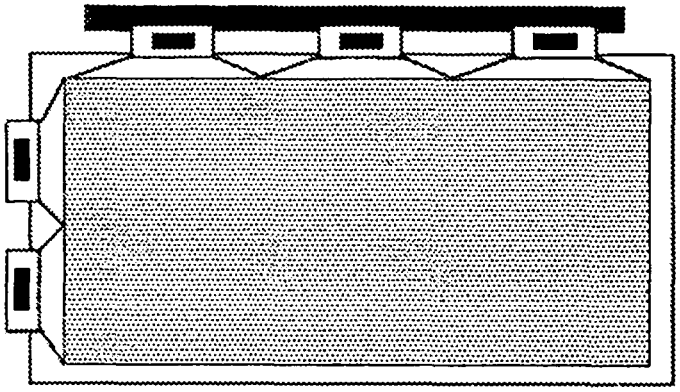


FIG. 13B

LOW TEMPERATURE
STATE IN WHICH
INCONSISTENCIES OCCUR

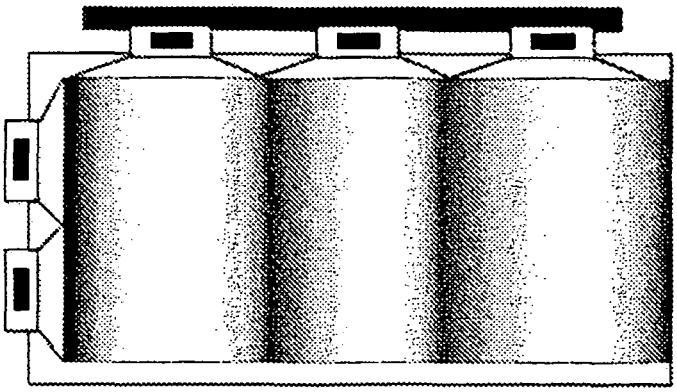


FIG. 14A

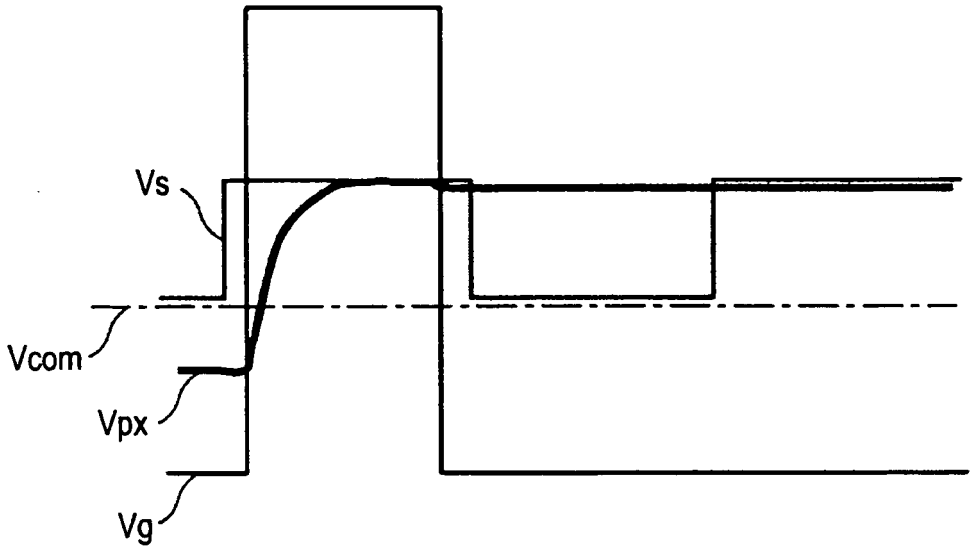


FIG. 14B

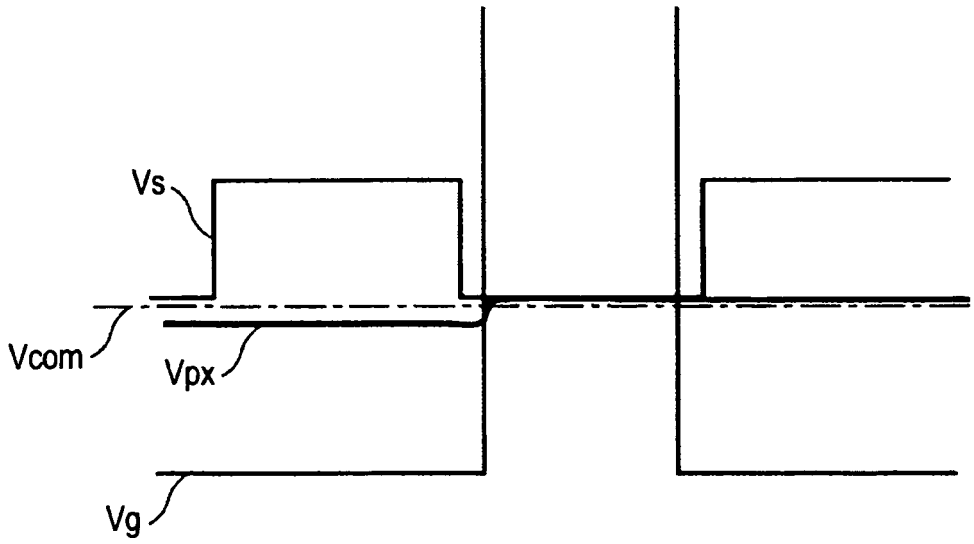


FIG. 15A

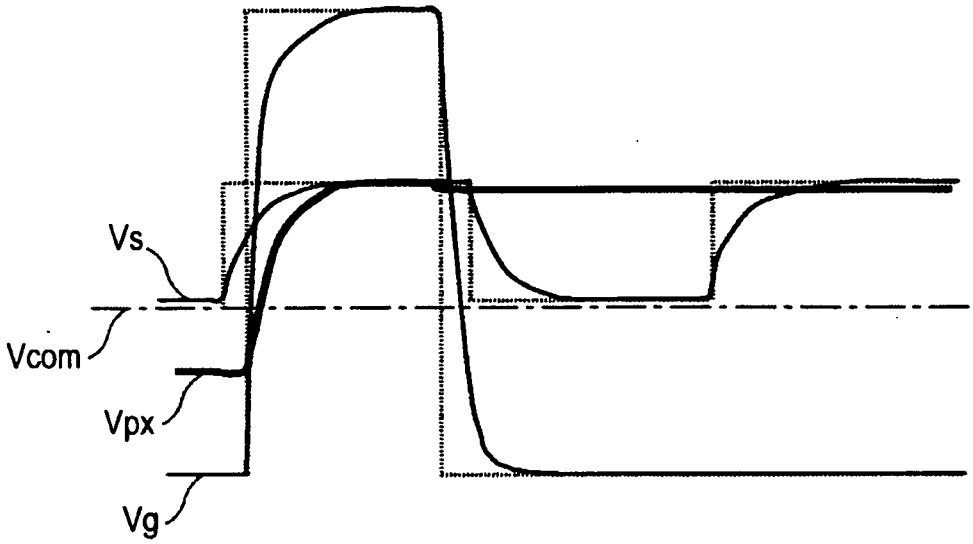


FIG. 15B

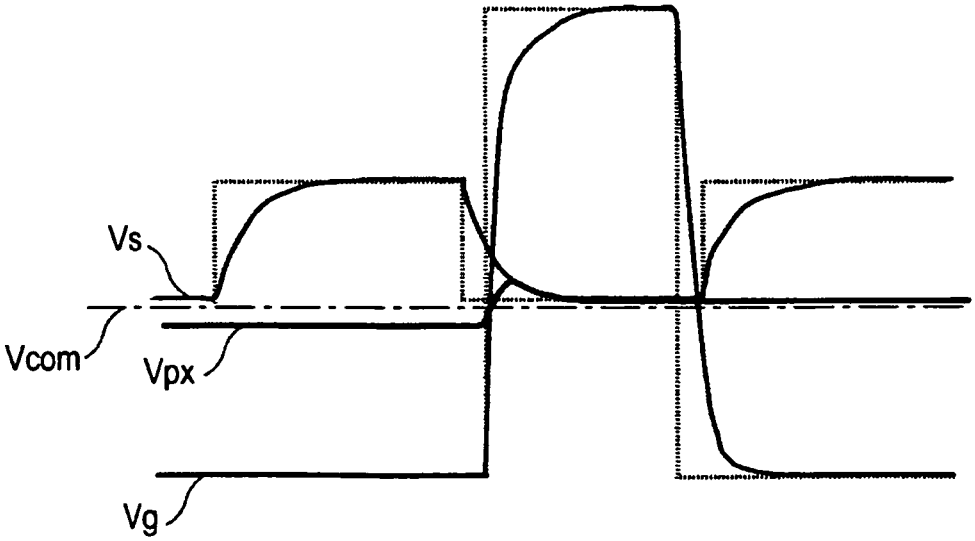


FIG. 16A

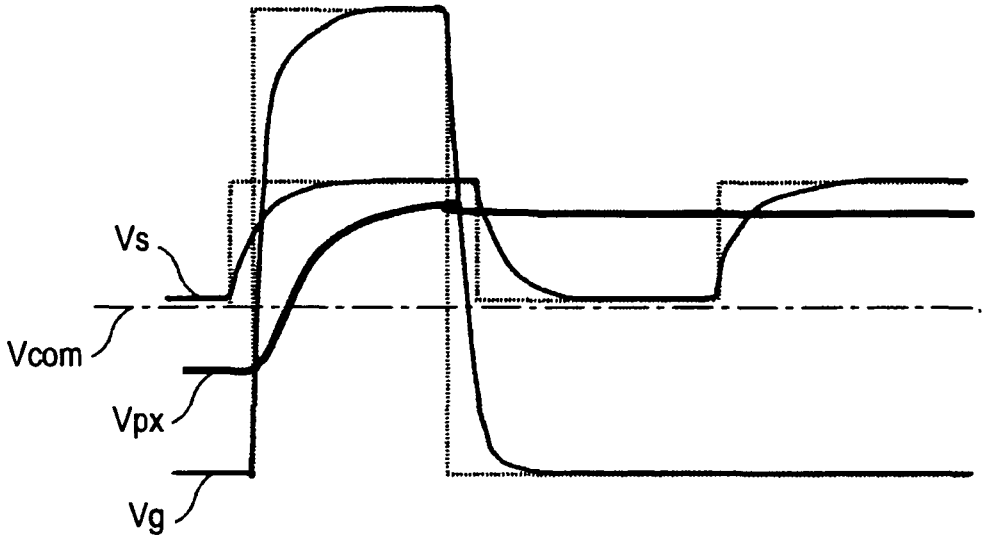


FIG. 16B

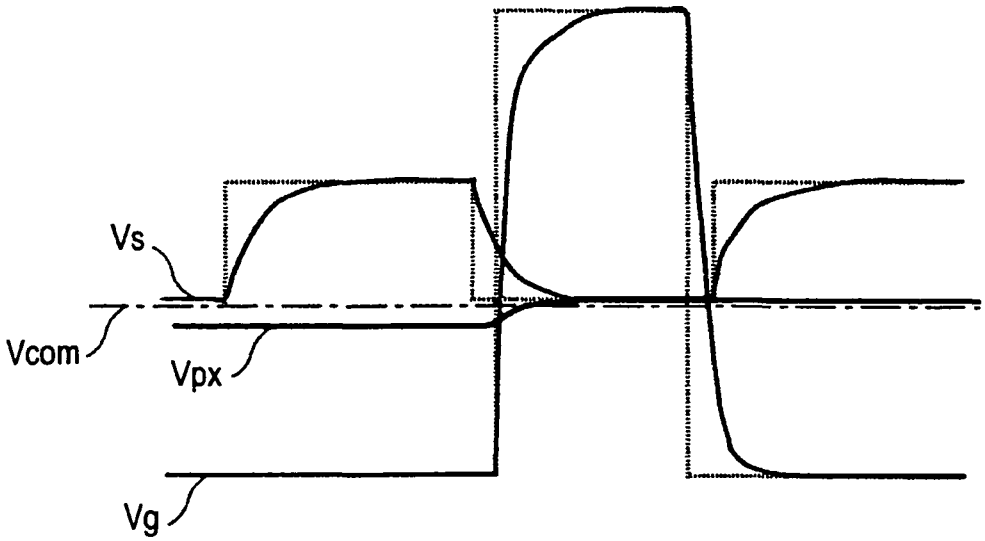


FIG. 17

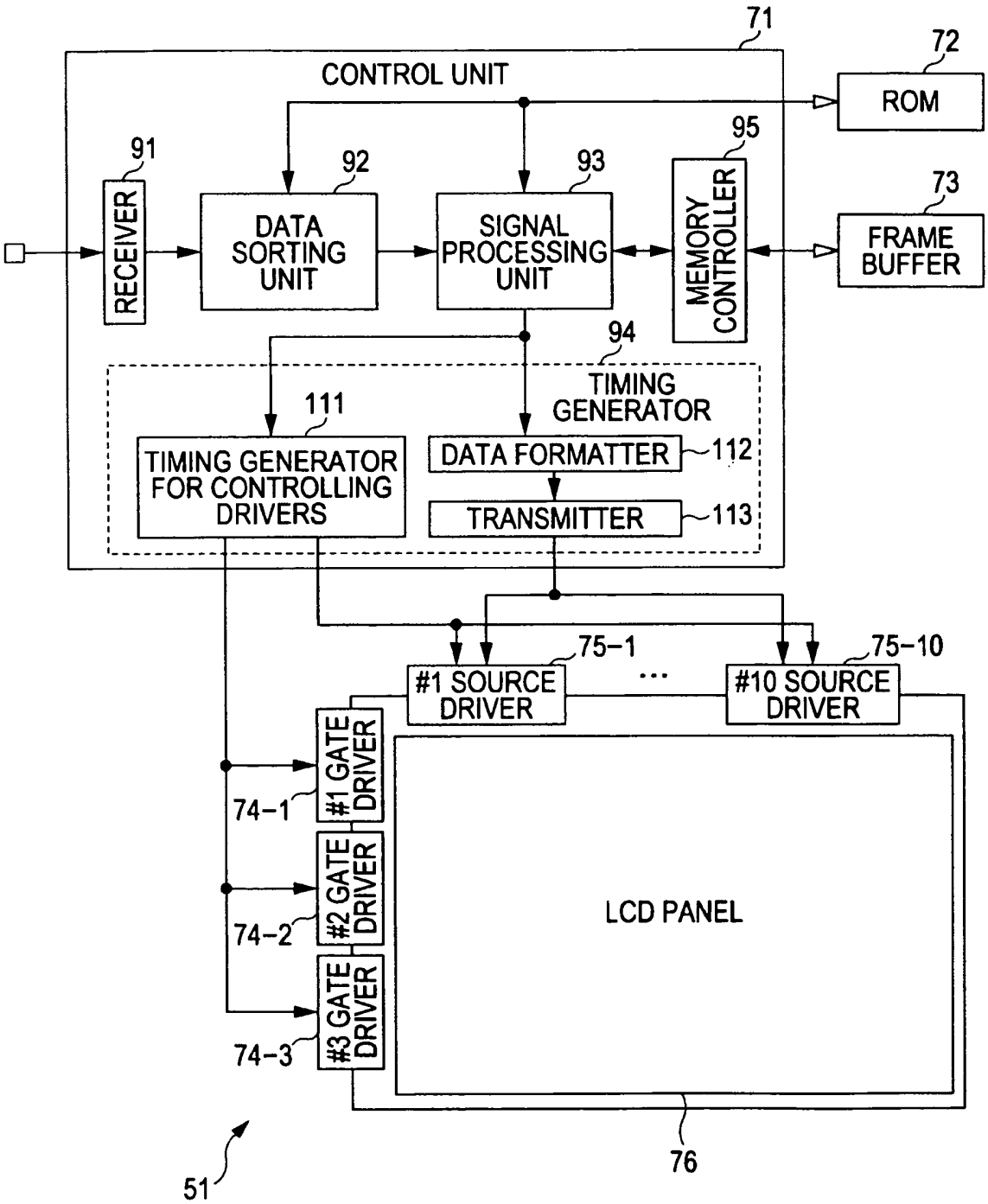

71
CONTROL UNIT
72
ROM
91
RECEIVER
92
DATA SORTING UNIT
93
SIGNAL PROCESSING UNIT
95
MEMORY CONTROLLER
73
FRAME BUFFER
94
TIMING GENERATOR
111
TIMING GENERATOR FOR CONTROLLING DRIVERS
DATA FORMATTER
112
TRANSMITTER
113
75-1
#1 SOURCE DRIVER
75-10
#10 SOURCE DRIVER
#1 GATE DRIVER
#2 GATE DRIVER
#3 GATE DRIVER
74-1
74-2
74-3
LCD PANEL
76
51

FIG. 18

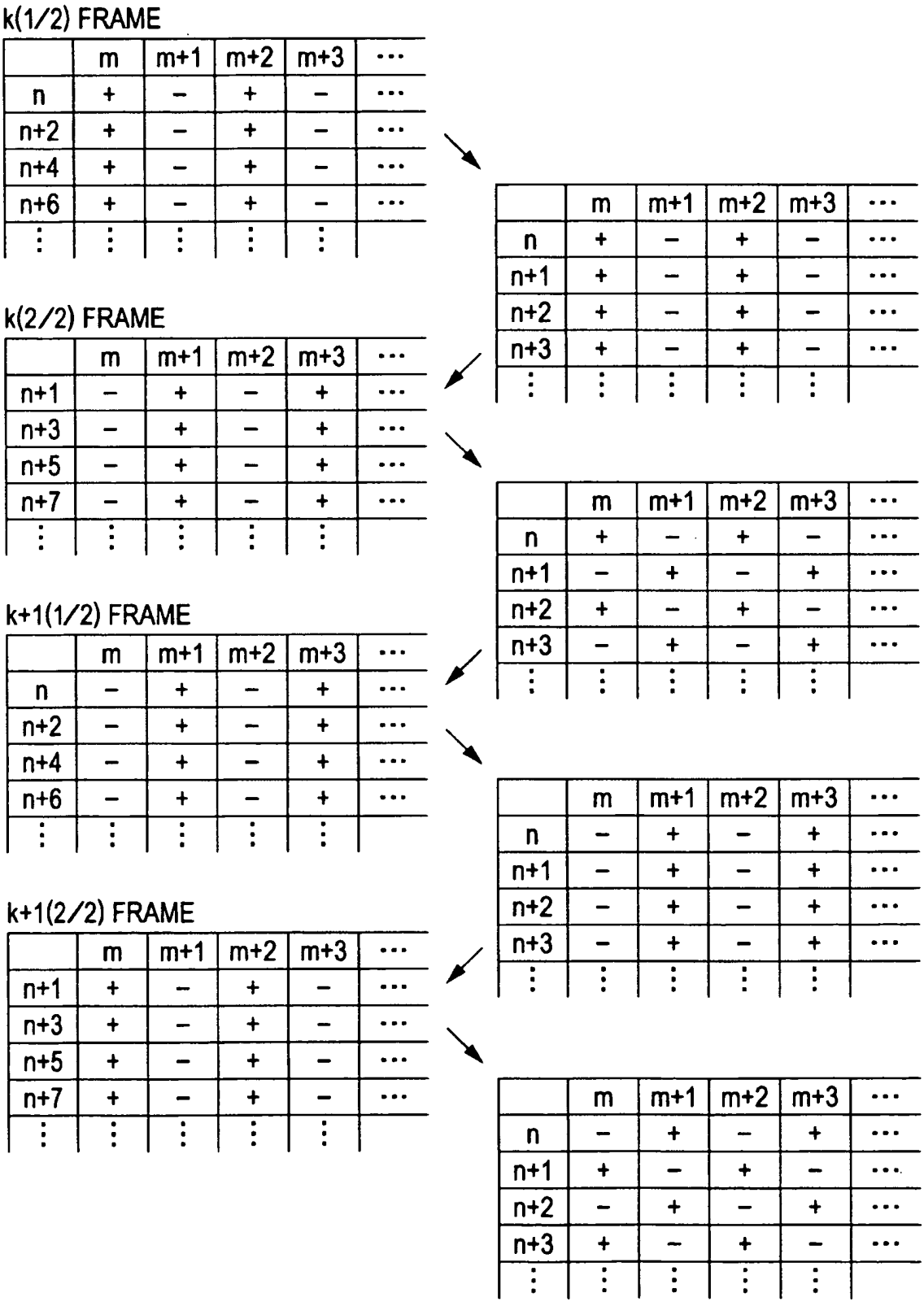


FIG. 19A

k(1/2) FRAME

	m1	m2	m1+1	m2+1	m1+2	m2+2	m1+3	m2+3	
n	+	−	+	−	+	−	+	−	···
n+2	+	−	+	−	+	−	+	−	···
n+4	+	−	+	−	+	−	+	−	···
n+6	+	−	+	−	+	−	+	−	···
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	

FIG. 19B

k(2/2) FRAME

	m1	m2	m1+1	m2+1	m1+2	m2+2	m1+3	m2+3	
n+1	+	−	+	−	+	−	+	−	···
n+3	+	−	+	−	+	−	+	−	···
n+5	+	−	+	−	+	−	+	−	···
n+7	+	−	+	−	+	−	+	−	···
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	

FIG. 19C

ONLY Px1

	i=0	i=1	i=2	i=3	
n	+	−	+	−	···
n+1	−	+	−	+	···
n+2	+	−	+	−	···
n+3	−	+	−	+	···
⋮	⋮	⋮	⋮	⋮	

FIG. 19D

ONLY Px2

	i=0	i=1	i=2	i=3	
n	−	+	−	+	···
n+1	+	−	+	−	···
n+2	−	+	−	+	···
n+3	+	−	+	−	···
⋮	⋮	⋮	⋮	⋮	

FIG. 20A

k+1(1/2) FRAME

	m1	m2	m1+1	m2+1	m1+2	m2+2	m1+3	m2+3	
n	−	+	−	+	−	+	−	+	···
n+2	−	+	−	+	−	+	−	+	···
n+4	−	+	−	+	−	+	−	+	···
n+6	−	+	−	+	−	+	−	+	···
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	

FIG. 20B

k+1(2/2) FRAME

	m1	m2	m1+1	m2+1	m1+2	m2+2	m1+3	m2+3	
n+1	−	+	−	+	−	+	−	+	···
n+3	−	+	−	+	−	+	−	+	···
n+5	−	+	−	+	−	+	−	+	···
n+7	−	+	−	+	−	+	−	+	···
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	

FIG. 20C

ONLY Px1

	i=0	i=1	i=2	i=3	
n	−	+	−	+	···
n+1	+	−	+	−	···
n+2	−	+	−	+	···
n+3	+	−	+	−	···
⋮	⋮	⋮	⋮	⋮	

FIG. 20D

ONLY Px2

	i=0	i=1	i=2	i=3	
n	+	−	+	−	···
n+1	−	+	−	+	···
n+2	+	−	+	−	···
n+3	−	+	−	+	···
⋮	⋮	⋮	⋮	⋮	

FIG. 21A

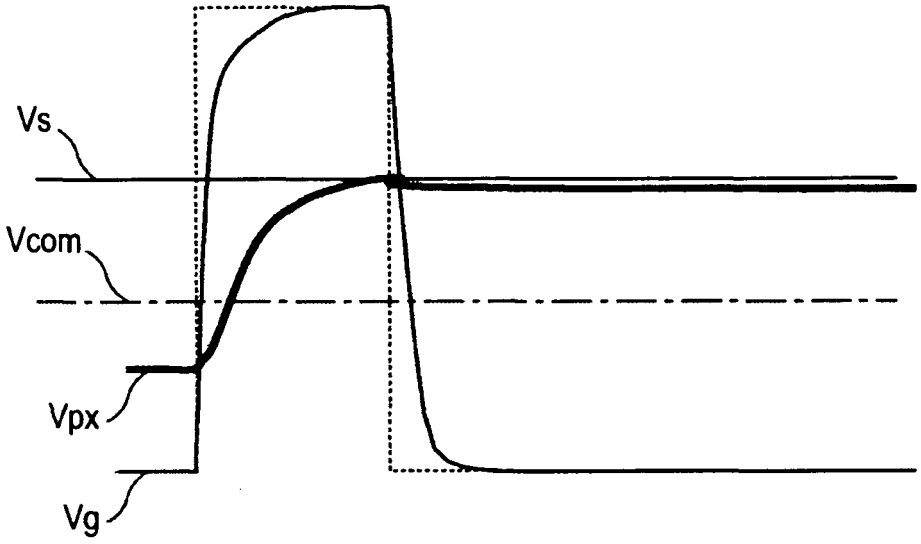


FIG. 21B

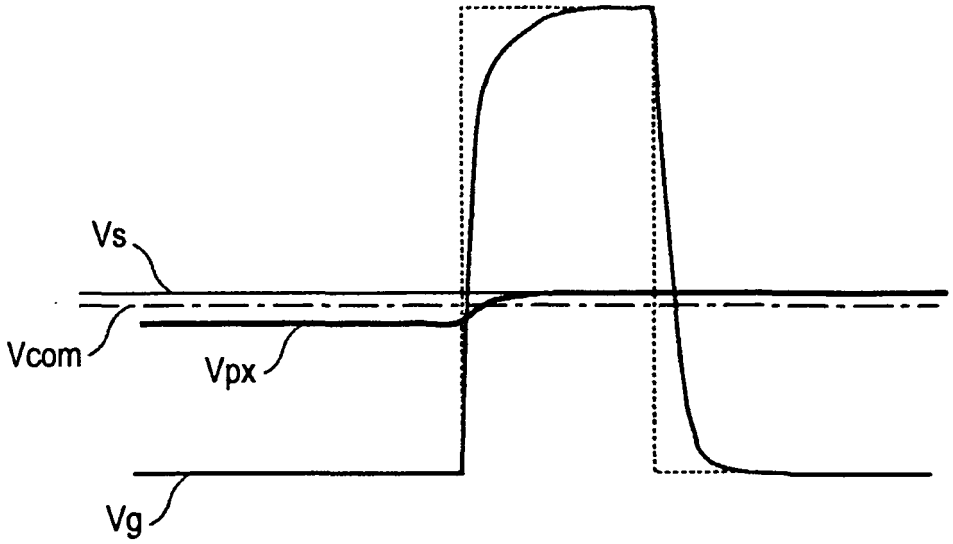


FIG. 22

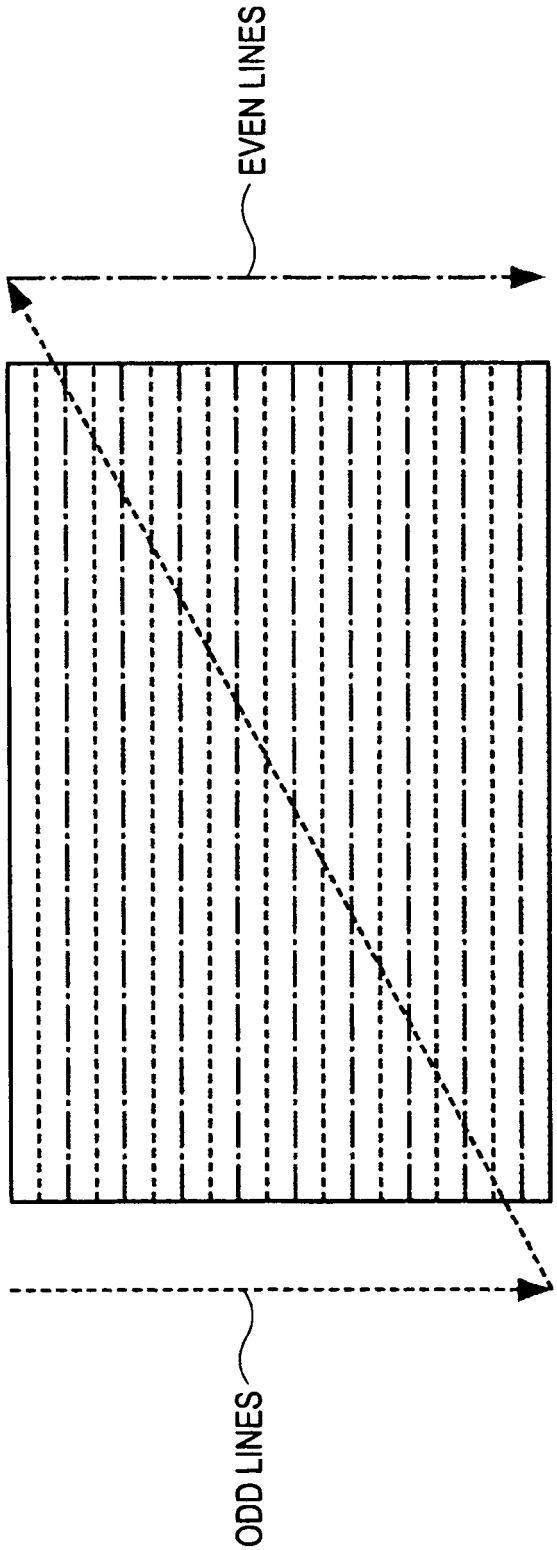


FIG. 23A

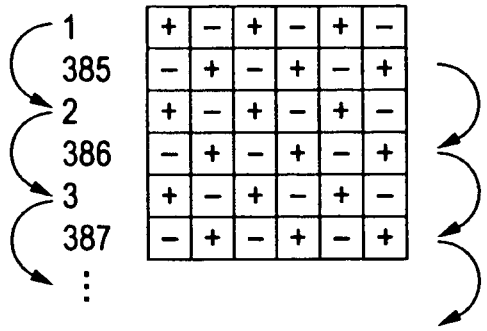


FIG. 23B

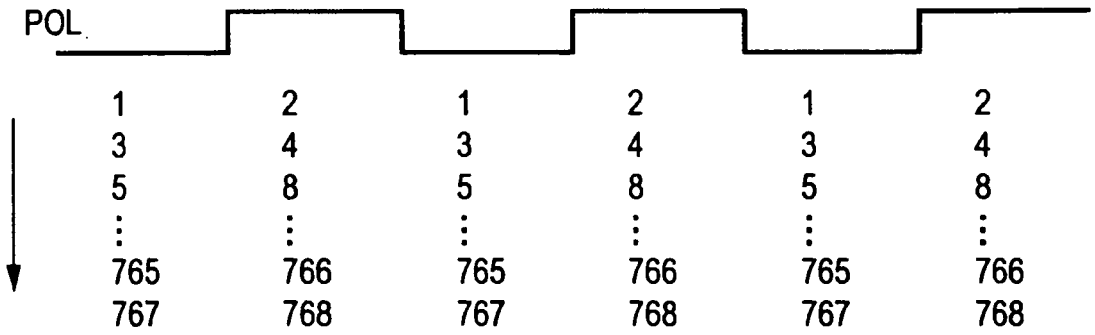


FIG. 24

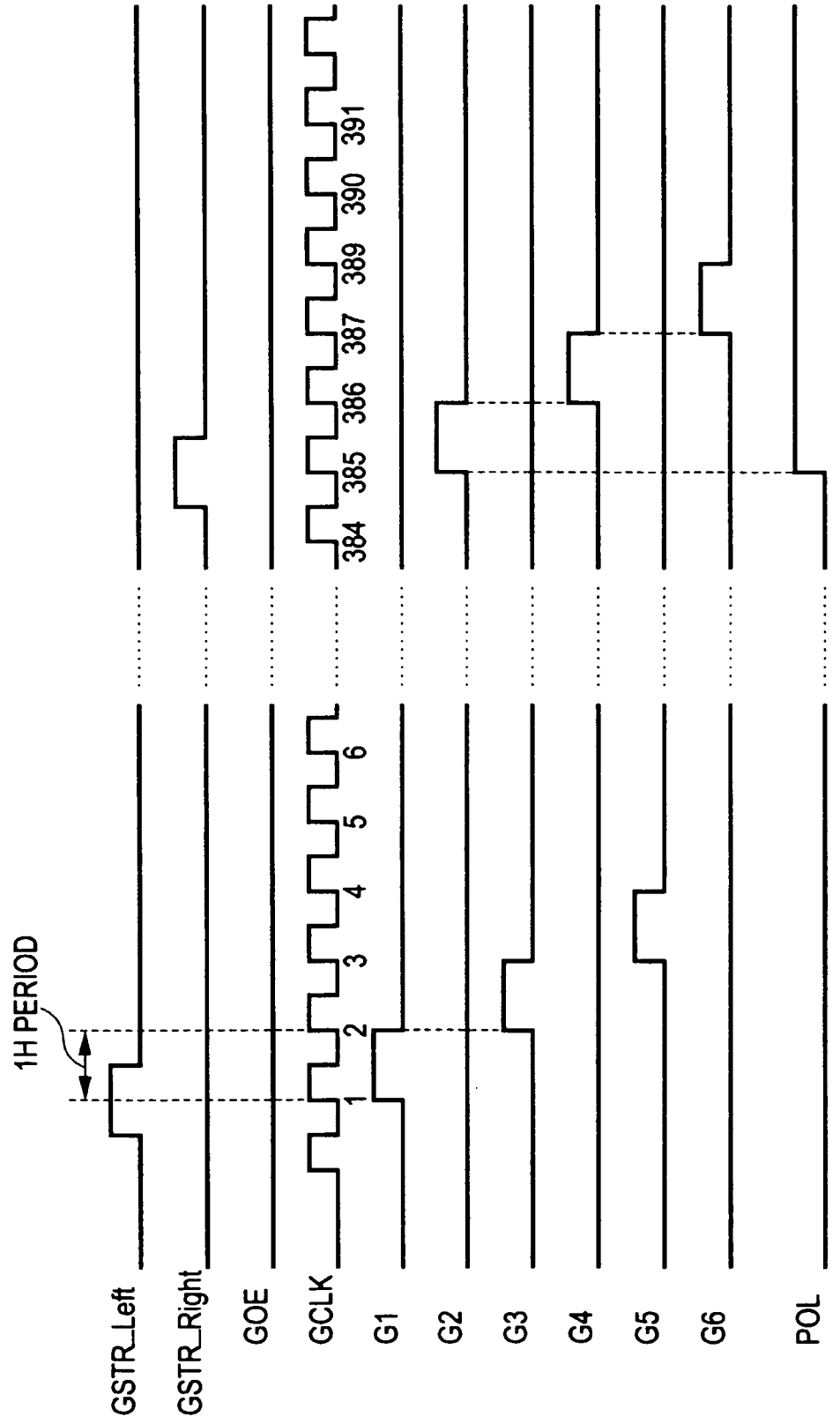

1H PERIOD
GSTR_Left
GSTR_Right
GOE
GCLK
G1
G2
G3
G4
G5
G6
POL
1
2
3
4
5
6
384
385
386
387
389
390
391

FIG. 25

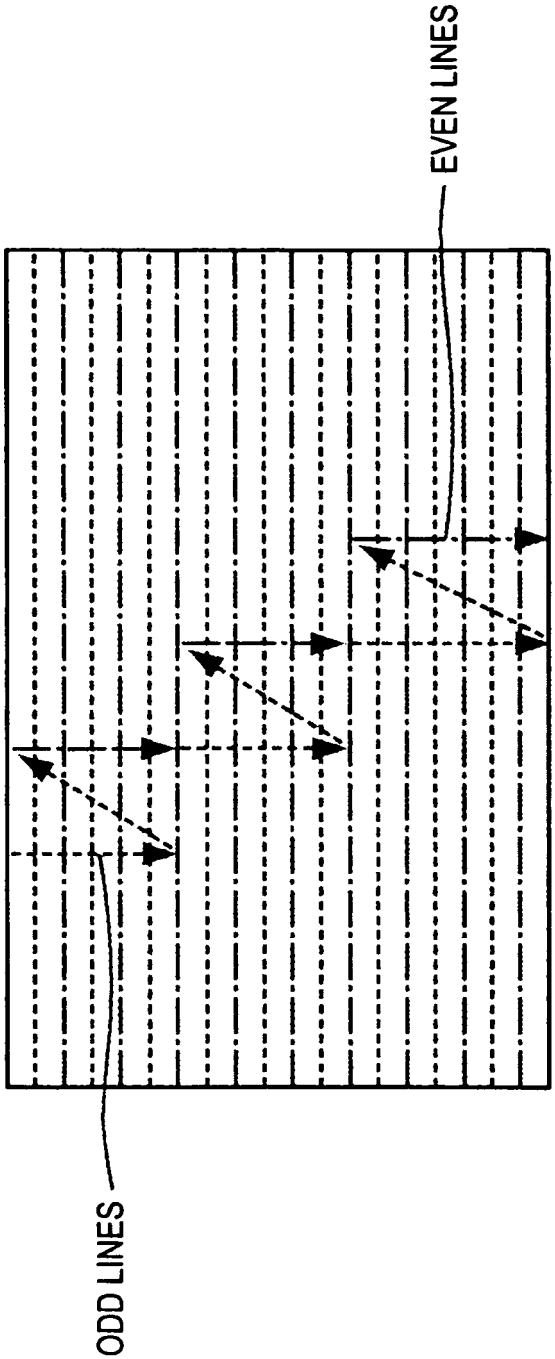


FIG. 26A

1ST BLOCK
2ND BLOCK
3RD BLOCK
4TH BLOCK
5TH BLOCK
6TH BLOCK
7TH BLOCK
8TH BLOCK
9TH BLOCK
10TH BLOCK
11TH BLOCK
12TH BLOCK

FIG. 26B

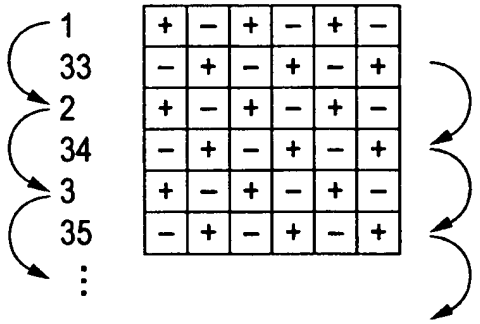


FIG. 26C

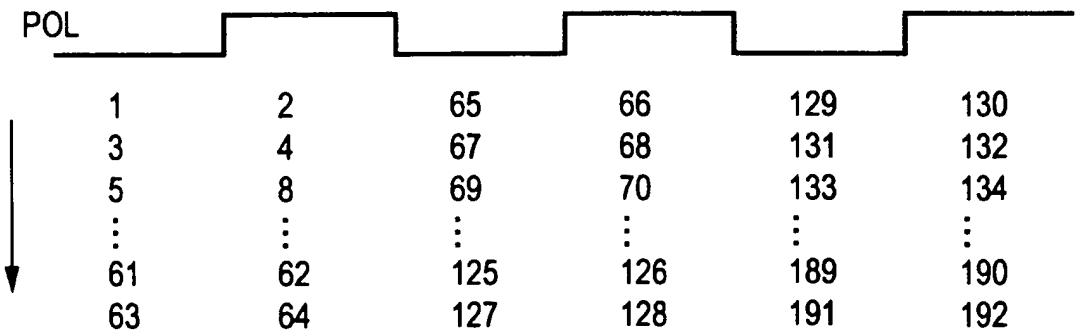
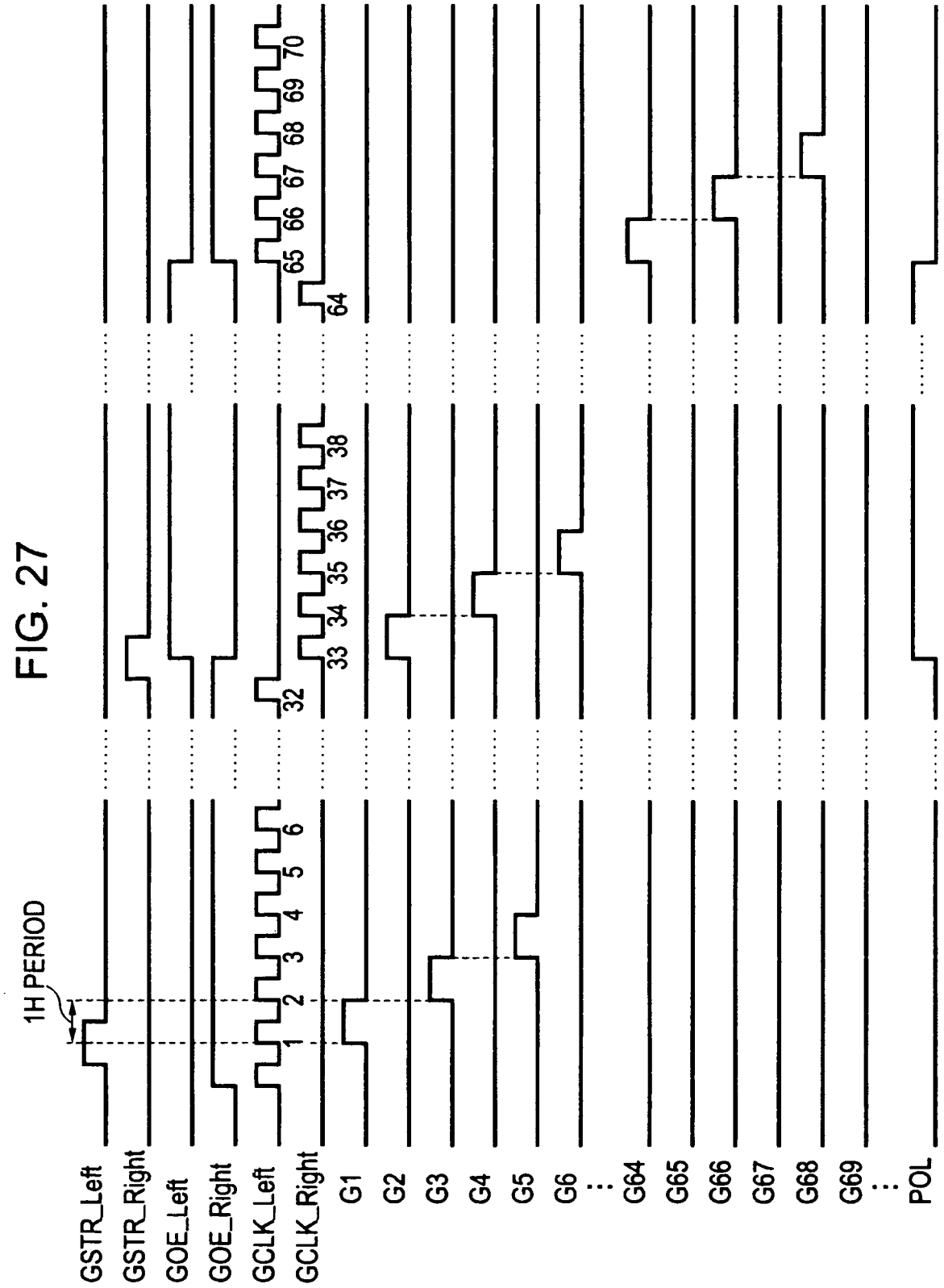


FIG. 27


1H PERIOD
GSTR_Left
GSTR_Right
GOE_Left
GOE_Right
GCLK_Left
GCLK_Right
G1
G2
G3
G4
G5
G6
...
G64
G65
G66
G67
G68
G69
...
POL
1
2
3
4
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33
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69
70

FIG. 28

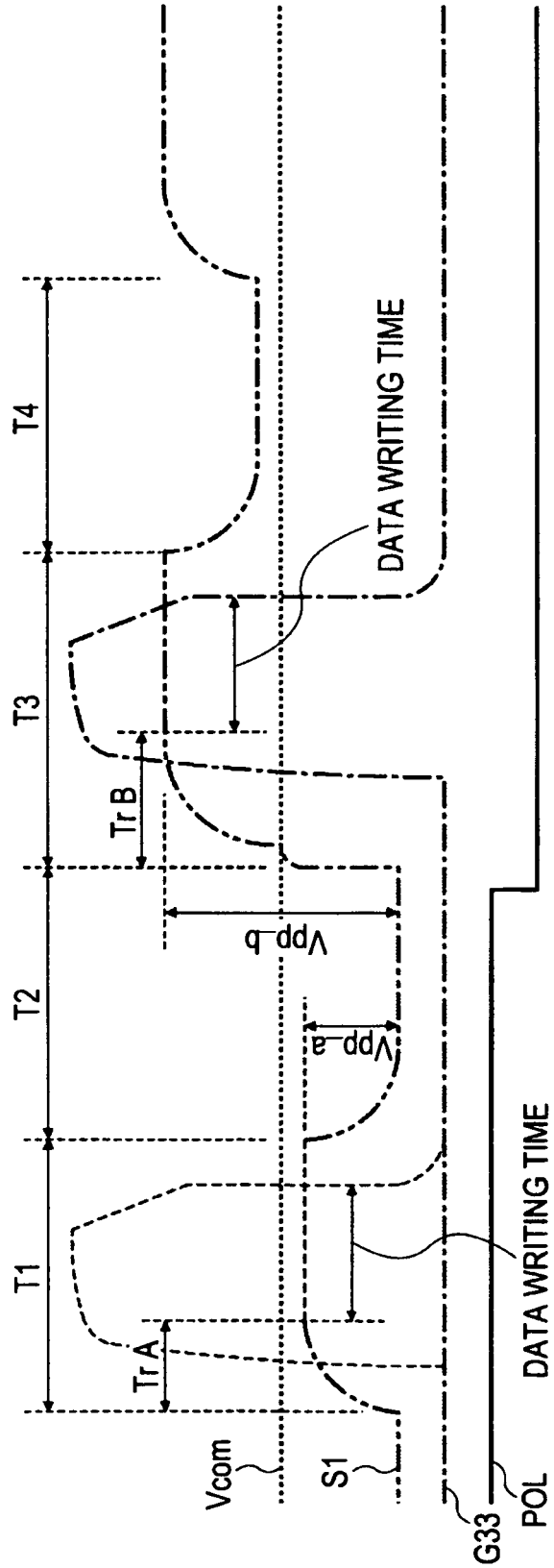

T4
T3
T2
T1
DATA WRITING TIME
TrB
Vpp_b
Vpp_a
TrA
Vcom
S1
G33
POL
DATA WRITING TIME

FIG. 29

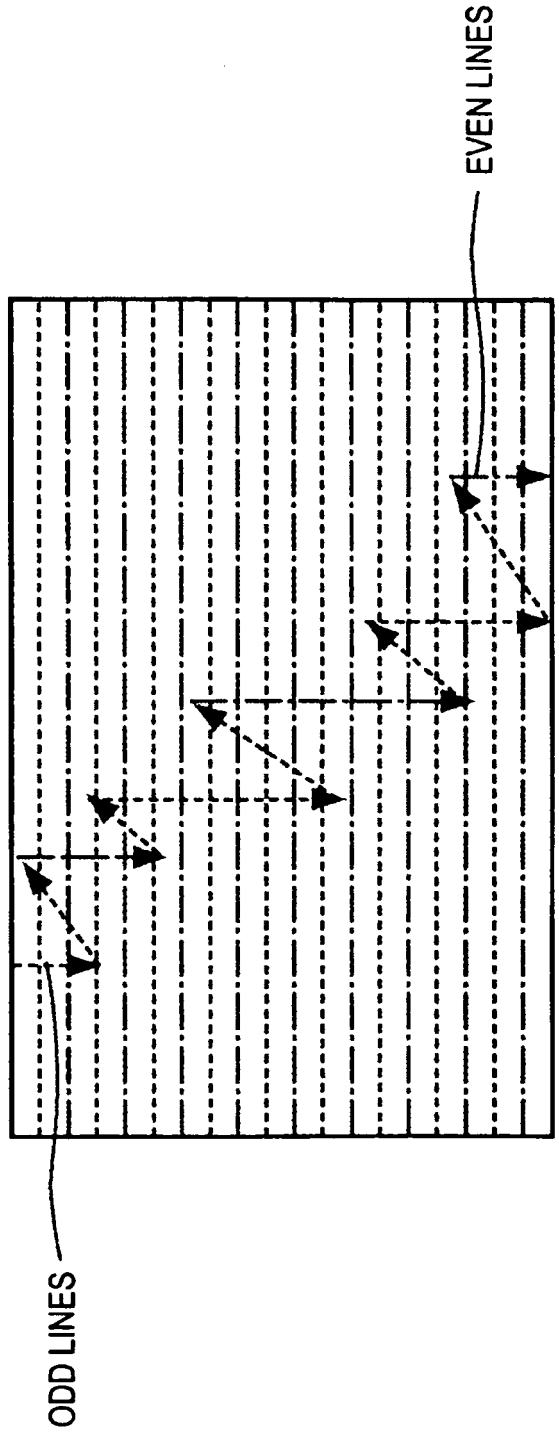


FIG. 30A

DIVISION REGARDING ODD LINES	DIVISION REGARDING EVEN LINES
1ST BLOCK ODD	1ST BLOCK EVEN
2ND BLOCK ODD	2ND BLOCK EVEN
3RD BLOCK ODD	3RD BLOCK EVEN
4TH BLOCK ODD	4TH BLOCK EVEN
5TH BLOCK ODD	5TH BLOCK EVEN
6TH BLOCK ODD	6TH BLOCK EVEN
7TH BLOCK ODD	7TH BLOCK EVEN
8TH BLOCK ODD	8TH BLOCK EVEN
9TH BLOCK ODD	9TH BLOCK EVEN
10TH BLOCK ODD	10TH BLOCK EVEN
11TH BLOCK ODD	11TH BLOCK EVEN
12TH BLOCK ODD	12TH BLOCK EVEN
13TH BLOCK ODD	

FIG. 30B

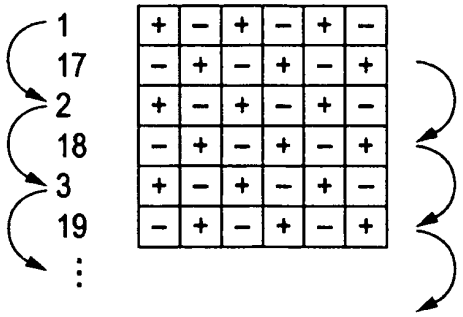
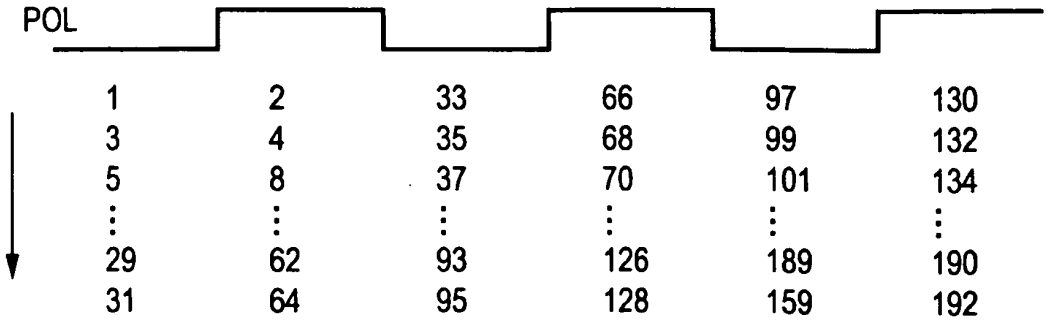


FIG. 30C



REFERENCES CITED IN THE DESCRIPTION

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专利名称(译)	液晶显示装置和显示控制装置		
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摘要(译)

一种LCD装置，包括显示单元，该显示单元包括具有多像素结构的像素;分别驱动扫描线和信号线的第一和第二驱动单元;图像获取单元和控制单元。每个像素包括第一和第二像素，并且像素的第一和第二像素以棋盘方式连接到两个对应的信号线。控制第一驱动单元以重复扫描奇数行的第一子帧和偶数行的第二子帧，并且控制第二驱动单元使得像素的第一像素的极性不同于在像素的第二像素的极性中，相邻的第一像素的极性彼此不同，并且相邻的第二像素的极性彼此不同，并且当在第一和第二子帧之间执行切换时，极性信号被反转。

FIG. 1