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(54) Liquid crystal display

Flüssigkristallanzeige

Dispositif d'affichage à cristaux liquides

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Description

CROSS-REFERENCE TO RELATED APPLICATION

BACKGROUND OF THE INVENTION

(a) Technical Field

[0001] The present disclosure relates to a liquid crystal display.

b) Discussion of the Related Art

[0002] A liquid crystal display (LCD), which is one of the flat panel display apparatuses that is being most widely used, includes two panels having electric field generating electrodes, such as pixel electrodes, and a common electrode and a liquid crystal layer interposed between the two panels.

[0003] The LCD displays an image by applying a voltage to the electric field generating electrodes to generate an electric field in the liquid crystal layer and by determining alignment of the liquid crystal molecules in the liquid crystal layer to control the polarization of incident light.

[0004] The LCD includes switching devices and a plurality of signal lines, such as gate and data lines, for controlling the switching devices connected to pixel electrodes to apply voltages to the pixels.

[0005] The gate lines transmit gate signals generated by a gate driver circuit, and the data lines transmit data voltages generated by a data driver circuit. The switching devices transmit the data voltages to the pixel electrodes according to the gate signals.

[0006] The gate and data driver circuits are directly mounted on the panels in the form of integrated chips. Otherwise, the gate and data driver circuits can be mounted on flexible printed circuit films that are attached to the panels. The integrated circuit chips are responsible for a large portion of production costs of the liquid crystal display.

[0007] More specifically, since the data driver integrated chips are much more expensive than the gate driver integrated chips, there is a need to reduce the number of data driver integrated chips for a high-resolution, large-sized liquid crystal display.

[0008] When the gate driver circuits together with gate lines, data lines, and switching devices are integrated into the panels, the production costs can be reduced. Since the structure of the data driver circuits is relatively complicated, however, the data circuits are not easy to integrate into the panels, so that there is a need to greatly reduce the number of data driver circuits.

[0009] FR-A1-2 719 936 discloses a liquid crystal display as per the preamble of claim 1. This document does not disclose the features of the characterizing portion.

SUMMARY OF THE INVENTION

[0010] An exemplary embodiment of the present invention has been made in an effort to provide a liquid crystal display having advantages of reducing the number of data driver circuit chips, in order to reduce the production cost.

[0011] The said objective is achieved by the features of claim 1.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] Exemplary embodiments of the present invention will be understood in more detail from the following descriptions taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a block diagram showing a liquid crystal display according to an exemplary embodiment of the present invention;

Fig. 2 is an equivalent circuit diagram of a pixel in a liquid crystal display according to an exemplary embodiment of the present invention;

Figs. 3A and 3B are views for explaining a pixel electrode in a liquid crystal display according to an exemplary embodiment of the present invention;

Fig. 4 is a view showing a spatial arrangement of pixels and signal lines of a liquid crystal display according to an exemplary embodiment of the present invention;

Fig. 5A shows waveforms of a common voltage, a data voltage, and a gate voltage when a liquid crystal display according to an exemplary embodiment of the present invention is driven;

Fig. 5B shows waveforms of a common voltage, a data voltage, and a gate voltage when a liquid crystal display according to an exemplary embodiment of the present invention is driven;

Fig. 6 is a view showing a layout of a liquid crystal display panel assembly according to an exemplary embodiment of the present invention;

Fig. 7 is a view showing a layout of a liquid crystal display panel assembly according to an exemplary embodiment of the present invention;

Fig. 8 is a view showing a layout of a liquid crystal display panel assembly according to an exemplary embodiment of the present invention;

Fig. 9 is a cross-sectional view of the liquid crystal display panel assembly taken along line XIV-XIV of Fig. 8;

Fig. 10 is a view showing a layout of a liquid crystal display panel assembly according to an exemplary embodiment of the present invention;

Fig. 11 is a cross-sectional view of the liquid crystal display panel assembly taken along line XVI-XVI of Fig. 10;

Fig. 12 is a view showing a layout of a liquid crystal display panel assembly according to an exemplary

embodiment of the present invention; and
Fig. 13 is a view showing a layout of a liquid crystal display panel assembly according to an exemplary embodiment of the present invention.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

[0013] Hereinafter, exemplary embodiments of the present invention will be described in detail with reference to the attached drawings such that the present invention can be easily put into practice by those skilled in the art.

[0014] A liquid crystal display LCD according to an exemplary embodiment of the present invention is described with reference to Figs. 1,2, 3A, and 3B.

[0015] Fig. 1 is a block diagram showing a liquid crystal display according to an exemplary embodiment of the present invention, Fig. 2 is an equivalent circuit diagram of a pixel in a liquid crystal display according to an exemplary embodiment of the present invention, and Figs. 3A and 3B are views for explaining a pixel electrode in a liquid crystal display according to an exemplary embodiment of the present invention.

[0016] Referring to Figs. 1 and 2, the LCD includes a liquid crystal display panel assembly 300, a gate driver 400 and a data driver 500 that are connected to the liquid crystal display panel 300, a gray voltage generator 800 that is connected to the data driver 500, and a signal controller 600 that controls the above units.

[0017] The liquid crystal display panel assembly 300 includes a plurality of pixels PX that are connected to a plurality of signal lines (not shown) and arrayed substantially in a matrix.

[0018] In the structure shown in Fig. 2, the liquid crystal display panel assembly 300 includes lower and upper panels 100 and 200 facing each other and a liquid crystal layer 3 interposed therebetween.

[0019] The signal lines include a plurality of gate lines (not shown) for transmitting gate signals (sometimes referred to as "scan signals") and a plurality of data lines (not shown) for transmitting data signals.

[0020] The gate lines extend in parallel to each other substantially in a row direction, and the data lines extend in parallel to each other substantially in a column direction.

[0021] Each pixel PX includes a switching device Q and a liquid crystal capacitor Clc connected to the switching device Q and a storage capacitor Cst.

[0022] The storage capacitor Cst may be omitted as desired.

[0023] The switching devices Q are constructed with thin film transistors and the like in the lower panel 100. Each of the switching devices is a three-port device having a control port connected to the gate line GL, an input port connected to the data line DL, and an output port connected to the liquid crystal capacitor C1 c and the storage capacitor Cst.

[0024] The pixel electrode PE is connected to the switching device Q, and the common electrode CE is disposed on the entire surface of the upper panel 200 to receive a common voltage Vcom.

[0025] Unlike what is shown in FIG. 2, the common electrode CE may be disposed on the lower panel 100. In this case, at least one of the two electrodes PE and CE may be formed in the shape of a line or bar.

[0026] The pixel electrode PE includes at least one parallelogrammic electrode piece 196 shown in Fig. 3A and one parallelogrammic electrode piece 197 shown in Fig. 3B.

[0027] As shown in Figs. 3A and 3B, each of the electrode pieces 196 and 197 has a shape of a parallelogram with a pair of oblique edges 196o (197o) and a pair of transverse edges 196t (197t).

[0028] The oblique edges 196o and 197o have oblique angles with respect to the transverse edges 196t and 197t, and sizes of the oblique angles are preferably in a range of from 45° to 135°.

[0029] The electrode piece slanted in the rightward direction is referred to as a "right slant" electrode piece as shown in Fig. 3A, and the electrode piece slanted in the leftward direction is referred to as a "left slant" electrode piece as shown in Fig. 3B.

[0030] The shape of the pixel electrode PE is not limited thereto, however, and a substantially rectangular shape may also be used.

[0031] The storage capacitor Cst having an auxiliary function for the liquid crystal capacitor C1c is constructed by overlapping a separate signal line (not shown) and the pixel electrode PE provided to the lower panel 100 with an insulating member interposed therebetween, and a predetermined voltage such as a common voltage Vcom is applied to the separate signal line.

[0032] Alternatively, the storage capacitor Cst may be constructed by overlapping the pixel electrode PE and a last stage gate line disposed just above it with an insulating member interposed therebetween.

[0033] In order to implement a color display, each of the pixels PX uniquely displays one of the primary colors (spatial division), or each of the pixels PX alternately displays the primary colors according to time (time division). A desired color can be obtained by a spatial or time combination of the primary colors.

[0034] An example of the primary colors is the three primary colors, such as red, green, and blue.

[0035] FIG. 2 shows an example of the spatial division implementation. As shown in FIG. 2, each of the pixels PX includes a color filter CF for representing one of the primary colors, which is provided to a region of the upper panel 200 corresponding to the pixel electrode PE.

[0036] Unlike what is shown in FIG. 2, the color filter CF may be provided above or under the sub pixel electrode PE of the lower panel 100.

[0037] Hereinafter, each of color filters CF is assumed to represent one of red, green, and blue. A pixel including a red color filter CF is referred to as a red pixel, a pixel

including a green color filter CF is referred to as a green pixel, and a pixel including a blue color filter CF is referred to as a blue pixel.

[0038] In addition, a pixel electrode included in the red pixel is referred to as a red pixel electrode, a pixel electrode included in the green pixel is referred to as a green pixel electrode, and a pixel electrode included in the blue pixel is referred to as a blue pixel electrode.

[0039] The red, blue, and green pixels are sequentially arrayed in a row direction.

[0040] At least one polarizer (not shown) for polarizing light is attached on an outer surface of the liquid crystal display panel assembly 300.

[0041] Referring to Fig. 4, the liquid crystal display according to an exemplary embodiment of the present invention includes pixels that are arrayed in a matrix.

[0042] The pixel PX includes red pixels RP1 and RP2, green pixels GP1 and GP2 and blue pixels BP1 and BP2, which represent three different colors (for example, red, green, and blue) according to types of the color filters (not shown).

[0043] Pixels of the three types are sequentially arrayed in the order of red, green, and blue in the row direction, and pixels of the same type are adjacent to each other in the column direction.

[0044] In Fig. 4, a pair of the gate lines GLa and GLb is disposed along upper and lower edges of each pixel row, and one data line is provided to each pixel column.

[0045] Unlike what is shown in Fig. 4, however, in one pixel row, adjacent groups of two pixels PX are connected to different gate lines.

[0046] For example, the first red pixel RP1 and the first green pixel GP1 are connected to the first gate line GLa, and the first blue pixel BP1 and the second red pixel RP2 are connected to the second gate line GLb.

[0047] The connection repeats in every pixel row.

[0048] Two even-numbered data lines connected to the pixels are connected to each other, and two odd-numbered data lines connected to the pixels are connected to each other.

[0049] In other words, every other data line is connected together.

[0050] For example, the data line DR1 connected to the first red pixel RP1 is connected to the data line DB1 that is connected to the first blue pixel BP 1. The data line DG1 connected to the first green pixel GP1 is connected to the data line DR2 that is connected to the second red pixel RP2. The data line DG2 connected to the second green pixel GP2 is connected to the data line DR3 that is connected to the third red pixel RP3. The data line DB2 connected to the second blue pixel BP2 is connected to the data line DG3 that is connected to the third green pixel GP3.

[0051] Returning to FIG. 1, the gray voltage generator 800 generates two gray voltage sets (reference gray sets) corresponding to the light transmittance of the pixels PX.

[0052] The one gray set has a positive value with respect to the common voltage V_{com}, and the other gray voltage set has a negative value with respect to the common voltage V_{com}.

[0053] The gate driver 400 is connected to the gate lines G_1 to G_n (not shown) of the liquid crystal panel assembly 300 to apply gate signals constructed with a combination of gate-on and gate-off voltages V_{on} and V_{off} to the gate lines G_1 to G_n.

[0054] The data driver 500 is connected to the data lines D_1 to D_m (not shown) of the liquid crystal panel assembly 300 to select the gray voltage from the gray voltage generator 800 and apply the gray voltages as data signals to the data lines D_1 to D_m.

[0055] Alternatively, in a case where the gray voltage generator 800 generates only a predetermined number of the reference gray voltages instead of all the gray voltages, the data driver 500 may generate the gray voltages for all the grays by dividing the reference gray voltages and select the data signals among the generated gray voltages.

[0056] The signal controller 600 controls the gate driver 400 and the data driver 500.

[0057] The gate driver 400 together with signal lines and thin film transistor switching devices Q is integrated into the liquid crystal display panel assembly 300.

[0058] The gate driver 400 may be divided into two drivers (not shown) that may be directly mounted in the form of IC chips on the liquid crystal display panel assembly 300. Alternatively, the gate driver 500 may be mounted on a flexible printed circuit (FPC) film (not shown) that may be attached in the form of a tape carrier package (TCP) on the liquid crystal display panel assembly 300. Otherwise, the gate driver 400 may be mounted on a separate printed circuit board (PCB) (not shown).

[0059] In addition, the driver, the controller, and the generator 500, 600, and 800 may be directly mounted in the form of IC chips on the liquid crystal display panel assembly 300. Alternatively, the driver, the controller, and the generator 500, 600, and 800 mounted on a flexible printed circuit (FPC) film (not shown) may be attached in the form of a tape carrier package (TCP) on the liquid crystal display panel assembly 300. Otherwise, the driver, the controller, and the generator 500, 600, and 800 may be mounted on a separate printed circuit board (PCB) (not shown).

[0060] Alternatively, the driver, the controller, and the generator 500, 600, and 800 together with signal lines and thin film transistor switching devices Q may be integrated into the liquid crystal display panel assembly 300.

[0061] In addition, the driver, the controller, and the generator 500, 600, and 800 may be integrated in the form of a single chip. In this case, at least one of the drivers or at least one circuit device constituting the drivers may be disposed outside the single chip.

[0062] Now, operations of the liquid crystal display apparatus will be described in detail.

[0063] The signal controller 600 receives input image signals R, G, and B and input control signals for control-

ling display thereof from an external graphic controller (not shown).

[0064] Input image signals R, G, and B contain luminance information of the pixels PX, and the luminance can be represented by a predetermined number of gray values, for example, $1024 = 2^{10}$, $256 = 2^8$, or $64 = 2^6$.

[0065] As an example of the input control signals, there are a vertical synchronization signal Vsync, a horizontal synchronization signal Hsync, a main clock signal MCLK, and a data enable signal DE.

[0066] The signal controller 600 processes the input image signals R, G, and B according to an operating condition of the liquid display panel assembly 300 based on the input control signals and the input image signals R, G, and B to generate a gate control signal CONT1, a data control signal CONT2, and the like, and after that, transmits the generated gate control signal CONT1 to the gate driver 400 and the generated data control signal CONT2 and the processed image signal DAT2 to the data driver 500.

[0067] The image signal process of the signal controller 600 includes an operation of rearranging the input image signals R, G, and B according to the pixel arrangement shown in Fig. 1.

[0068] The gate control signal CONT1 includes a scan start signal for indicating scan start and at least one clock signal for controlling an output period of the gate-on voltage V_{on}.

[0069] The gate control signal CONT1 may further include an output enable signal for defining a duration time of the gate-on voltage V_{on}.

[0070] The data control signal CONT2 includes a horizontal synchronization start signal for indicating data transmission for one pixel row, a load signal for commanding to apply the associated data voltages to the data lines D_1 to D_m (not shown), and a data clock signal.

[0071] The data control signal CONT2 may further include an inversion signal for inverting a voltage polarity of the data signal with respect to the common voltage V_{com}, hereinafter, the phrase "the voltage polarity of the data signal with respect to the common voltage V_{com}" is shortened to a "data signal polarity".

[0072] In response to the data control signal CONT2 from the signal controller 600, the data driver 500 receives the digital image data DAT2 for one pixel row and selects the gray voltages corresponding to the digital image data DAT2, so that the digital image data DAT2 are converted into the associated analog data signals. After that, the analog data signals are applied to the associated data lines D1 to Dm.

[0073] The gate driver 400 applies the gate-on voltage V_{on} to the gate lines G_1 to G_n (not shown) according to the gate control signals CONT1 from the signal controller 600 to turn on the switching devices Q connected to the gate lines G_1 to G_n.

[0074] As a result, the data signals applied to the data lines D_1 to D_m are applied to the associated pixels PX through the turned-on switching devices Q.

[0075] A difference between the voltage of the data signal applied to the pixel PX and the common voltage V_{com} becomes a charge voltage of the liquid crystal capacitors C_{LC}, that is, a pixel voltage.

[0076] Alignment of the liquid crystal molecules varies according to the intensity of the pixel voltage.

[0077] Therefore, polarization of light passing through the liquid crystal layer 3 changes. The change in the polarization results in a change in transmittance of the light due to the polarizer attached to the liquid crystal panel assembly 300.

[0078] In units of one horizontal period (or 1H), that is, one period of the horizontal synchronization signal Hsync and the data enable signal DE, the aforementioned operations are repeatedly performed to sequentially apply the gate-on voltages V_{on} to all the gate lines G_1 to G_n, so that the data signals are applied to all the pixels. As a result, one frame of an image is displayed.

[0079] When one frame ends the next frame starts, and a state of the inversion control signal applied to the data driver 500 is controlled so that the polarity of the data signal applied to each of the pixels is opposite to the polarity in the previous frame (frame inversion).

[0080] At this time, even in one frame, according to the characteristics of the inversion control signals, the polarity of the data signal flowing through the one data line may be inverted (row inversion and dot inversion). In addition, the polarities of the data signals applied to the one pixel row may be different from each other (column inversion and dot inversion).

[0081] Now, an inversion operation of a liquid crystal display according to the embodiment of the present invention is described in detail with reference to Figs. 5A and 5B.

[0082] Figs. 5A and 5B are waveforms of a common voltage, a data voltage, and a gate voltage at the time of driving the liquid crystal display according to an exemplary embodiment of the present invention.

[0083] Firstly, an operation scheme relative to what is shown in Fig. 5A is described.

[0084] In the liquid crystal display according to the exemplary embodiment of the present invention shown in Fig. 4, since the number of the gate lines GLa and GLb is two per one pixel row, the time taken to scan one pixel row is 1/2H.

[0085] Therefore, the gate-on voltages Von are applied to the adjacent gate lines in a period of 1/2H.

[0086] In addition, in the liquid crystal display shown in Fig. 4, the number of data lines is equal to the number of pixel columns, but the gate lines are connected in groups of two data lines. Therefore, the same data voltage is applied to the pixels of the two pixel columns.

[0087] As shown in Fig. 5B, the gate-on voltages Von applied to the two adjacent gate lines in a period of 1/2H overlap each other, so that a time of applying the gate-on voltages to the gate lines becomes 1H. Therefore, it is possible to obtain a sufficient charging time.

[0088] At this time, the data voltages are applied to the

data lines of each data line pair in a period of 1H in the column inversion scheme.

[0089] The gate-on voltages Von are sequentially applied to all the gate lines during one frame, so that all the pixels have the data voltage applied to them.

[0090] When one frame ends the next frame starts, and a state of the reverse signal applied to the data driver 500 is controlled so that the polarity of the data signal applied to each of the pixels is opposite to the polarity in the previous frame.

[0091] Fig. 4 shows the polarities of the pixels in the driving scheme shown in Fig. 5B.

[0092] Referring to Fig. 4, a positive polarity data voltage (+) is applied to a first pair of data lines DR1 and DG1, and a negative polarity data voltage (-) is applied to a next pair of data lines DR2 and DG2. The positive polarity voltage (+) is applied to the next pair of data lines DB1 and DB2.

[0093] The first red pixel RP1, the first blue pixel BP1, and the second red pixel RP2 connected to the first gate line GLa are charged with the gate-on voltage for a first half-period 1/2H.

[0094] The first red pixel RP1 is applied with the positive polarity voltage (+) from the data line DR1 connected thereto. The first blue pixel BP1 is applied with the positive polarity voltage (+) from the data line DB1 connected thereto. The second red pixel RP2 is applied with the negative polarity voltage (-) from the data line DR2 connected thereto.

[0095] The first green pixel GP1, the second green pixel GP2, and the second blue pixel BP2 connected to the second gate line GLb are charged with the gate-on voltage for a second half-period 1/2H.

[0096] The first green pixel GP1 is applied with the positive polarity voltage (+) from the data line DG1 connected thereto. The second green pixel GP2 is applied with the negative polarity voltage (-) from the data line DG2 connected thereto. The second blue pixel BP2 is applied with the positive polarity voltage (+) from the data line DB2 connected thereto.

[0097] Therefore, in the first pixel row, the polarities of the first red pixel RP1, the first green pixel GP1, the first blue pixel BP1, the second red pixel RP2, the second green pixel GP2, and the second blue pixel BP2 are represented by (+ + + - - +) as shown in Fig. 4.

[0098] Polarities of the pixels of one pixel row are opposite to those of the pixels of the adjacent pixel row, and polarities of the pixels of one pixel column are also opposite to those of the pixels of the adjacent pixel column. The polarity arrangement repeats in the row and column directions.

[0099] Now, a liquid crystal display panel assembly according to an exemplary embodiment of the present invention is described in detail with reference to Figs. 1 to 3.

[0100] Now, a liquid crystal display panel assembly according to an exemplary embodiment of the present invention is described in detail with reference to Figs. 6, 1, 2, and 4.

[0101] Fig. 6 is a view showing a layout of the liquid crystal display panel assembly according to an exemplary embodiment of the present invention.

[0102] As shown in Fig. 6, the liquid crystal display panel assembly includes lower and upper panels (not shown) facing each other, and a liquid crystal layer (not shown) interposed therebetween.

[0103] In the lower panel, a plurality of gate conductors including a plurality of pairs of first and second gate lines 121a and 121b and a plurality of storage electrode lines 131 are formed on the insulating substrate (not shown).

[0104] The gate lines 121a and 12 1b include gate electrodes 124a and 124b and end portions 129a and 129b, respectively, and each of the storage electrode lines 131 includes storage electrodes 137a and 137b.

[0105] A gate insulating film (not shown) is formed on the gate conductors 121a, 121b, and 131.

[0106] A plurality of semiconductors 154a and 154b are formed on the gate insulating film, and a plurality of ohmic contacts (not shown) are formed on the semiconductors.

[0107] Data conductors including a plurality of data lines 171 and a plurality of first and second drain electrodes 175a and 175b are disposed on the ohmic contacts and the gate insulating film.

[0108] Each of the data lines 171 includes a plurality of source electrodes 173a and 173b and end portions 179a, 179b, and 179c, and the drain electrodes 175 and 175b include enlarged end portions 177a and 177b.

[0109] A protective film 180 is formed on the data conductors 171, 175a, and 175b and the exposed portions of the semiconductors 154a and 154b, and a plurality of contact holes 181a, 181b, 182a, 182b, 182c, 185a, and 185b are formed on the protective film 180 and the gate insulating film 140.

[0110] A plurality of pixel electrodes 191 and a plurality of contact assistants 81, 82a, 82b, and 82c are disposed on the protective film 180.

[0111] An alignment film (not shown) is disposed on the pixel electrodes 191, the contact assistants 81, 82a, 82b, and 82c, and the protective film 180.

[0112] In the upper panel (not shown), a light blocking member, a plurality of color filters, an overcoat film, a common electrode having cutout portions 71, and an alignment film are formed on an insulating substrate.

[0113] In comparison with the liquid crystal display assemblies shown in Figs. 9 and 5, however, in the liquid crystal display panel assembly according to the exemplary embodiment of the present invention, each of the pixel electrodes 191 is constructed with two pairs of electrode pieces having different slant directions.

[0114] More specifically, the right slant parallelogrammic electrode pieces 196 shown in Fig. 3A and the left slant parallelogrammic electrode pieces 197 shown in Fig. 3B are alternately connected to each other in the up-down direction and oblique edges of the electrode pieces of the two pairs of electrode pieces 196 and 196 are continuous with each other to form a pair of curved edges

that are curved three times.

[0115] Cutout portions 91, 92, and 93 are formed on the pixel electrode 191.

[0116] Each of the cutout portions 91, 92, and 93 is formed to extend from one of three concave vertexes formed by the two pairs of electrode pieces 196 and 197 to the corresponding convex vertex.

[0117] The storage electrode line 131 is arranged to extend in the transverse direction through the second turning point among three turning points of the curved edge formed by two pairs of electrode pieces 196 and 197.

[0118] In general, alignment of liquid crystal molecule may be easily disturbed in the regions where the electrode pieces 196 and 197 are connected, so that a resultant texture may easily occur. According to the construction, the texture can be shielded, and the aspect ratio can be improved.

[0119] The first and second gate lines 121a and 121b are arranged to extend in the transverse direction through other turning points.

[0120] The pixel electrodes 191 may be classified into, for example, red, green, and blue pixel electrodes 191R, 191G, and 191B corresponding to the color filters 270R, 270G, and 270B for respectively displaying three colors.

[0121] The red pixel electrodes 191R are connected to first drain electrodes 173a, and the green pixel electrodes 191G are connected to second drain electrodes 173b. The blue pixel electrodes 191B are alternately connected to the first and second drain electrodes 173a and 173b.

[0122] The pixel electrodes 191 connected to the drain electrodes 175a and 175b are applied with data voltages from the associated data lines 171.

[0123] The data line 171 connected to the first/second red pixel electrode 191Ra/191Rb and the data line 171 connected to the first/second green pixel electrode 191Ga/191Gb are connected to each other and share an end portion 179a/179b.

[0124] Each of the data lines 171 connected to the first blue pixel electrodes 191Ba includes an enlarged portion 178a having a wide area, and each of the data lines 171 connected to the second blue pixel electrodes 191Bb includes an enlarged portion 178b having a wide area.

[0125] The two enlarged portions 178a and 178b are connected to a connection member 86 made of ITO or the like through contact holes 186a and 186b, respectively.

[0126] In addition, the two enlarged portions 178a and 178b are connected to another enlarged portion 178c and the connection member 86 through a contact hole 186c.

[0127] Therefore, the two data lines 171 connected to the first and second blue pixel electrodes 191Ba and 191Bb share the end portion 179c that has a wide area for connection to other layers or external driver circuits.

[0128] As a result, it is possible to reduce the number of data drivers by half.

[0129] In portions of the gate lines 121 a and 121b overlapping the blue pixel electrodes 191Ba and 191Bb, gate protrusions 125a and 125b are formed in the same shape as that of the gate electrodes 124a and 124b on regions of the source electrodes 173a and 173b and the drain electrodes 175a and 175b.

[0130] As a result, it is possible to equalize overlap areas of all the blue pixel electrodes 191B overlapping the gate lines.

[0131] The operations of the aforementioned liquid crystal display, the polarities of pixel electrodes, and the inversion driving therefor can be employed by the liquid crystal display panel assembly shown in Fig. 6 and the liquid crystal display including the liquid crystal display panel assembly.

[0132] In addition, other features of the liquid crystal display panel assembly shown in Figs. 9 and 10 can be employed by the liquid crystal display panel assembly shown in Fig. 6.

[0133] Now, a liquid crystal display panel assembly according to an exemplary embodiment of the present invention is described in detail with reference to Fig. 7.

[0134] Fig. 7 is a view showing a layout of the liquid crystal display panel assembly according to an exemplary embodiment of the present invention.

[0135] As shown in Fig. 7, the liquid crystal display panel assembly includes lower and upper panels (not shown) facing each other and a liquid crystal layer (not shown) interposed therebetween.

[0136] In the lower panel, a plurality of gate conductors including a plurality of pairs of first and second gate lines 121a and 121 b and a plurality of storage electrode lines 131 are formed on the insulating substrate (not shown).

[0137] The gate lines 121a and 121b include gate electrodes 124a and 124b and end portions 129a and 129b, respectively, and each of the storage electrode lines 131 includes storage electrodes 137a and 137b.

[0138] A gate insulating film (not shown) is formed on the gate conductors 121 a, 121 b, and 131.

[0139] A plurality of semiconductors 154a and 154b are disposed on the gate insulating film, and a plurality of ohmic contacts (not shown) is disposed on the semiconductors.

[0140] Data conductors including a plurality of data lines 171 and a plurality of first and second drain electrodes 175a and 175b are disposed on the ohmic contacts and the gate insulating film.

[0141] Each of the data lines 171 includes a plurality of source electrodes 173a and 173b and end portions 179a, 179b, and 179c, and the drain electrodes 175 and 175b include enlarged end portions 177a and 177b.

[0142] A protective film 180 is formed on the data conductors 171, 175a, and 175b and the exposed portions of the semiconductors 154a and 154b, and a plurality of contact holes 181, 185a, and 185b are formed on the protective film 180 and the gate insulating film 140.

[0143] A plurality of pixel electrodes 191 and a plurality of contact assistants 81 are disposed on the protective

film 180.

[0144] An alignment film (not shown) is disposed on the pixel electrode 191, the contact assistants 81, and the protective film 180.

[0145] In the upper panel (not shown), a light blocking member, a plurality of color filters, an overcoat film, a common electrode having cutout portions 71, and an alignment film are formed on an insulating substrate.

[0146] Unlike the liquid crystal display panel assembly shown in Fig. 6, however, in the liquid crystal display panel assembly according to the exemplary embodiment of the present invention, the pixel electrodes 191 have two parallelogrammic electrode pieces having different slant directions.

[0147] Namely, the right slant parallelogrammic electrode pieces shown in Fig. 3A and the left slant parallelogrammic electrode pieces shown in Fig. 3B are connected to each other in the up-down direction.

[0148] In addition, other features of the liquid crystal display panel assembly shown in Fig. 6 can be employed by the liquid crystal display panel assembly shown in Fig. 7.

[0149] Now, a liquid crystal display panel assembly according to an exemplary embodiment of the present invention is described in detail with reference to Figs. 8, 9, and 7.

[0150] Fig. 8 is a view showing a layout of the liquid crystal display panel assembly according to an exemplary embodiment of the present invention, and Fig. 9 is a cross-sectional view of the liquid crystal display panel assembly taken along line XIV-XIV of Fig. 8.

[0151] As shown in Figs. 8 and 9, the liquid crystal display panel assembly includes lower and upper panels 100 and 200 facing each other, and a liquid crystal layer 3 interposed therebetween.

[0152] In the lower panel 100, a plurality of gate conductors including a plurality of pairs of first and second gate lines 121a and 121b and a plurality of storage electrode lines 131 are formed on the insulating substrate 110.

[0153] The gate lines 121a and 121b includes gate electrodes 124a and 124b and end portions 129a and 129b, respectively, and each of the storage electrode lines 131 includes storage electrodes 137a and 137b.

[0154] A gate insulating film 140 is formed on the gate conductors 121a, 121b, and 131.

[0155] A plurality of semiconductors 154a and 154b are disposed on the gate insulating film, and a plurality of ohmic contacts 163a and 163b are disposed on the semiconductors.

[0156] Data conductors including a plurality of data lines 171 and a plurality of first and second drain electrodes 175a and 175b are disposed on the ohmic contacts 163a and 163b and the gate insulating film 140.

[0157] Each of the data lines 171 includes a plurality of source electrodes 173a and 173b and end portions (not shown), and the drain electrodes 175 and 175b includes enlarged end portions 177a and 177b.

[0158] A protective film 180 is formed on the data conductors 171, 175a, and 175b and the exposed portions of the semiconductors 154a and 154b, and a plurality of contact holes 181, 185a, and 185b are formed on the protective film 180 and the gate insulating film 140.

[0159] A plurality of pixel electrodes 191 and a plurality of contact assistants 81 are disposed on the protective film 180.

[0160] An alignment film 11 is disposed on the pixel electrode 191, the contact assistants 81, and the protective film 180.

[0161] In the upper panel 200, a light blocking member 220, a plurality of color filters 230, an overcoat film 250, a common electrode 270 having cutout portions 71, and an alignment film 21 are formed on the insulating substrate 210.

[0162] Unlike the liquid crystal display panel assembly shown in Fig. 7, however, in the liquid crystal display panel assembly shown in Figs. 8 and 9, the storage electrodes 137a and 137b are arranged to extend along gaps between the pixel electrodes 191.

[0163] In addition, the enlarged portions 177a and 177b of the drain electrodes 175a and 175b are arranged to extend along the gaps between the pixel electrodes 191 and overlap the storage electrodes 137a and 137b.

[0164] By constructing the drain electrodes 175a and 175b in such a form, it is possible to more effectively block light and prevent light leakage between the pixel electrodes 191.

[0165] In addition, other features of the liquid crystal display panel assembly shown in Fig. 7 can be employed by the liquid crystal display panel assembly shown in Figs. 8 and 9.

[0166] Now, a liquid crystal display panel assembly according to an exemplary embodiment of the present invention is described in detail with reference to Figs. 10, 11, 8, and 9.

[0167] Fig. 10 is a view showing a layout of the liquid crystal display panel assembly according to an exemplary embodiment of the present invention, and Fig. 11 is a cross-sectional view of the liquid crystal display panel assembly taken along line XVI-XVI of Fig. 10.

[0168] As shown in Figs. 10 and 11, the liquid crystal display panel assembly includes lower and upper panels 100 and 200 facing each other, and a liquid crystal layer 3 interposed therebetween.

[0169] In the lower panel 100, a plurality of gate conductors including a plurality of pairs of first and second gate lines 121a and 121b and a plurality of storage electrode lines 131 are formed on the insulating substrate 110.

[0170] The gate lines 121a and 121b include gate electrodes 124a and 124b and end portions 129a and 129b, respectively, and each of the storage electrode lines 131 includes storage electrodes 137a and 137b.

[0171] A gate insulating film 140 is formed on the gate conductors 121a, 121 b, and 131.

[0172] A plurality of semiconductors 154a and 154b

are disposed on the gate insulating film, and a plurality of ohmic contacts 163a and 163b are disposed on the semiconductors.

[0173] Data conductors including a plurality of data lines 171 and a plurality of first and second drain electrodes 175a and 175b are disposed on the ohmic contacts 163a and 163b and the gate insulating film 140.

[0174] Each of the data lines 171 includes a plurality of source electrodes 173a and 173b and end portions (not shown), and the drain electrodes 175 and 175b include enlarged end portions 177a and 177b.

[0175] A protective film 180 is formed on the data conductors 171, 175a, and 175b and the exposed portions of the semiconductors 154a and 154b, and a plurality of contact holes 181, 185a, and 185b are formed on the protective film 180 and the gate insulating film 140.

[0176] A plurality of pixel electrodes 191 and a plurality of contact assistants 81 are disposed on the protective film 180.

[0177] An alignment film 11 is disposed on the pixel electrodes 191, the contact assistants 81, and the protective film 180.

[0178] In the upper panel 200, a light blocking member 220, a plurality of color filters 230, an overcoat film 250, a common electrode 270 having cutout portions 71, and an alignment film 21 are formed on the insulating substrate 210.

[0179] Unlike the liquid crystal display panel assembly shown in Figs. 8 and 9, however, in the liquid crystal display panel assembly shown in Figs. 15 and 16, each of the data lines 171 includes first and second portions 171n and 1711 having different widths.

[0180] The width of the second portion 1711 is larger than that of the first portion 171, and the width of the second portion 1711 is about twice that of the first portion 171n.

[0181] The first portion 171n includes third and fourth portions 171 a and 171 b that are disposed above and below the second portion 1711, respectively.

[0182] The third and fourth portions 171a and 171 b are aligned in a straight line, and the second portion 1711 is disposed to deviate from the straight line.

[0183] Therefore, an overlap area of one pixel electrode 191 and an overlap area of the adjacent pixel electrode 191 in one data line 171 can be equalized, so that it is possible to prevent a variation in the pixel electrode voltage caused from parasitic capacitance generated between the data line 171 and the pixel electrodes 191.

[0184] Unlike the liquid crystal display panel assembly shown in Figs. 13 and 14, in this liquid crystal display panel assembly, the color filters 230 are provided not to the common electrode panel 200 but under the protective film 180 of the thin film transistor panel 100.

[0185] The color filters 230 are arranged to extend in a stripe pattern along the pixel electrode column, and two adjacent color filters 230 are arranged to overlap each other in regions above the data lines 171.

[0186] The overlapped color filters 230 are constructed with an organic film, so as to insulate the pixel electrodes 191 from the data lines 171.

[0187] Therefore, even in a case where the insulating film 180 is not constructed with an organic film, it is possible to prevent a parasitic capacitance from being generated in the overlapped regions of the pixel electrodes 191 and the data lines 171.

[0188] In addition, the color filters 230 may have a function as a light blocking member for preventing light leakage between the pixel electrodes 191.

[0189] In this case, the light blocking member 220 on the common electrode panel 200 can be omitted, so that the production process can be simplified.

[0190] The color filters 230 are provided with through-holes 235 for access to the contact holes 185, and the through-holes 235 are wider than the contact holes 185.

[0191] Peripheral regions where the end portions 129 of the gate lines 121 and the end portions 179 of the data lines 171 are disposed are not provided with the color filters 230.

[0192] A protective film (not shown) may also be disposed under the color filters 230.

[0193] In addition, other features of the liquid crystal display panel assembly shown in Figs. 8 and 9 can be employed by the liquid crystal display panel assembly shown in Figs. 10 and 11.

[0194] Now, a liquid crystal display panel assembly according to an exemplary embodiment of the present invention is described in detail with reference to Figs. 12 and 6.

[0195] Fig. 12 is a view showing a layout of the liquid crystal display panel assembly according to an exemplary embodiment of the present invention.

[0196] As shown in Fig. 12, the liquid crystal display panel assembly includes lower and upper panels (not shown) facing each other, and a liquid crystal layer (not shown) interposed therebetween.

[0197] The layered structure of the liquid crystal display panel assembly according to the embodiment is substantially the same as that of the liquid crystal display panel assembly shown in Fig. 6.

[0198] In the lower panel, a plurality of gate conductors including a plurality of pairs of first and second gate lines 121a and 121b and a plurality of storage electrode lines 131 are formed on the insulating substrate (not shown).

[0199] The gate lines 121a and 121b include gate electrodes 124a and 124b and end portions 129a and 129b, respectively, and each of the storage electrode lines 131 includes storage electrodes 137a and 137b.

[0200] A gate insulating film 140 is formed on the gate conductors 121a, 121b, and 131.

[0201] A plurality of semiconductors 154a and 154b are disposed on the gate insulating film 140, and a plurality of ohmic contacts (not shown) is disposed on the semiconductors.

[0202] Data conductors including a plurality of data lines 171 and a plurality of first and second drain electrodes 175a and 175b are disposed on the ohmic con-

tacts and the gate insulating film 140.

[0203] Each of the data lines 171 includes a plurality of source electrodes 173a and 173b and end portions 179a, 179b, and 179c, and the drain electrodes 175 and 175b include enlarged end portions 177a and 177b.

[0204] A protective film 180 is formed on the data conductors 171, 175a, and 175b and the exposed portions of the semiconductors 154a and 154b, and a plurality of contact holes 181, 185a, and 185b are formed on the protective film 180 and the gate insulating film 140.

[0205] A plurality of pixel electrodes' 191 and a plurality of contact assistants 81 are disposed on the protective film 180.

[0206] An alignment film (not shown) is disposed on the pixel electrode 191, the contact assistants 81, and the protective film 180.

[0207] In the upper panel (not shown), a light blocking member, a plurality of color filters, an overcoat film, a common electrode having cutout portions 71, and an alignment film are formed on an insulating substrate.

[0208] Unlike the liquid crystal display panel assembly shown in Fig. 6, however, in this liquid crystal display panel assembly, the pixel electrodes 191 have different shapes.

[0209] Each of the red and green pixel electrodes 191R and 191G includes three parallelogrammic electrode pieces having different slant directions.

[0210] As shown in Fig. 3A, the red pixel electrode 191R includes first to third base electrodes 191R1, 191 R2, and 191 R3 having right and left slant parallelogrammic electrode pieces 196 and 197. Similarly, the green pixel electrode 191G includes first to third base electrodes 191G1, 191G2, and 191G3 having right and left slant parallelogrammic electrode pieces 196 and 197.

[0211] The adjacent first and second base electrodes 191R1 and 191R2/191G1 and 191G2 are connected to each other in the row direction, and the adjacent third base electrodes 191R3/191G3 are connected to each other in the column direction of the first base electrode 191R1/191G1.

[0212] The red pixel electrode 191R and the green pixel electrode 191G have inversion symmetry.

[0213] Unlike the red and green pixel electrodes 19R and 19G, the blue pixel electrode 191B includes two pairs of electrode pieces having different slant directions.

[0214] Namely, the right slant parallelogrammic electrode pieces 196 shown in Fig. 3A and the left slant parallelogrammic electrode pieces 197 shown in Fig. 3B are alternately disposed in the row direction.

[0215] The electrode pieces constituting the blue pixel electrode 191B are wider than the electrode pieces constituting the red and green pixel electrodes 191R and 191G, and, the electrode pieces constituting the blue pixel electrode 191B have widths that are about 1.4 times to 1.6 times those of the electrode pieces constituting the red and green pixel electrodes 191R and 191G.

[0216] As a result, it is possible to equalize the areas of the pixel electrodes 191 irrespective of shapes of the pixel electrodes.

[0217] In addition, other features of the liquid crystal display panel assembly shown in Fig. 11 can be employed by the liquid crystal display panel assembly shown in Fig. 12.

[0218] Now, a liquid crystal display panel assembly according to an exemplary embodiment of the present invention is described in detail with reference to Fig. 13.

[0219] Fig. 13 is a view showing a layout of the liquid crystal display panel assembly according to an exemplary embodiment of the present invention.

[0220] As shown in Fig. 13, the liquid crystal display panel assembly includes lower and upper panels (not shown) facing each other, and a liquid crystal layer (not shown) interposed therebetween.

[0221] In the lower panel, a plurality of gate conductors including a plurality of pairs of first and second gate lines 121a and 121 b and a plurality of storage electrode lines 131 are formed on the insulating substrate (not shown).

[0222] The gate lines 121a and 121b include gate electrodes 124a and 124b and end portions 129a and 129b, respectively, and each of the storage electrode lines 131 includes storage electrodes 137a and 137b.

[0223] A gate insulating film (not shown) is formed on the gate conductors 121a, 121b, and 131.

[0224] A plurality of semiconductors 154a and 154b are disposed on the gate insulating film, and a plurality of ohmic contacts (not shown) is disposed on the semiconductors.

[0225] Data conductors including a plurality of data lines 171 and a plurality of first and second drain electrodes 175a and 175b are disposed on the ohmic contacts and the gate insulating film.

[0226] Each of the data lines 171 includes a plurality of source electrodes 173a and 173b and end portions (not shown), and the drain electrodes 175 and 175b include enlarged end portions 177a and 177b.

[0227] A protective film 180 is formed on the data conductors 171, 175a, and 175b and the exposed portions of the semiconductors 154a and 154b, and a plurality of contact holes 181, 185a, and 185b are formed on the protective film 180 and the gate insulating film 140.

[0228] A plurality of pixel electrodes 191 and a plurality of contact assistants 81 are disposed on the protective film 180.

[0229] An alignment film (not shown) is disposed on the pixel electrodes 191, the contact assistants 81, and the protective film 180.

[0230] In the upper panel (not shown), a light blocking member, a plurality of color filters, an overcoat film, a common electrode, and an alignment film are disposed on the insulating substrate.

[0231] Unlike the above-described exemplary embodiment of the present invention, in the liquid crystal display panel assembly, all the pairs of first and second gate lines 12 1 a and 121b are disposed under the storage electrode lines 131.

[0232] In addition, each pixel electrode 191 includes

two edges parallel to the gate lines 121a and 121 b and two edges parallel to the data lines 171, and a portion thereof overlaps the data lines 171, so that it is possible to maximize the aspect ratio.

[0233] Each pixel electrode 191 overlaps the last stage gate line disposed just above to constitute a storage capacitor, so that the storage capacitance is increased.

[0234] Features of the liquid crystal display shown in Figs. 6 to 12 can be employed by the liquid crystal display shown in Fig. 13.

[0235] According to exemplary embodiments of the present invention, it is possible to prevent a variation in luminance and aspect ratio among pixels and to reduce the number of data drivers and production costs.

Claims

1. A liquid crystal display comprising:

a plurality of pixels (PX) including pixel electrodes (PE) and switching devices (Q) connected to the pixel electrodes (PE) and arrayed in a matrix;
a plurality of pairs of first and second gate lines (GLa, GLb; 121a, 121b), each pair consisting of a first gate line (GLa; 121a) extending in a distance to an interrelated second gate line (GLb, 121b), the pairs of first and second gate lines (GLa, GLb; 121a, 121b) being connected to the switching devices (Q) and separated from each other; and
a plurality of data lines (DL; 171) connected to the switching devices (Q) and intersecting the first and second gate lines (GLa, GLb; 121a, 121b), wherein the plurality of data lines (DL; 171) are connected so that end portions of two data lines (DR1, DG1, DB1; DR2, DG2, Db2) in each pair of data lines are connected to each other, wherein each of the pixels (PX) includes a first pixel (RP1; RP2), a second pixel (GP1; GP2) and a third pixel (BP1; BP2) representing three different colors, respectively,
characterized in that
a data line (DR1; DR2) connected to the first pixel (RP1; RP2) and a data line (DG1; DG2) connected to the second pixel (GP1; GP2) are connected to each other, and
wherein two adjacent data lines (DB1, DB2) connected to the third pixels (BP1, BP2) are connected to each other.

2. The liquid crystal display of claim 1, wherein each of the pixel electrodes (PE) includes at least two parallelogrammic electrode pieces (196, 197) having different respective slant directions.

3. The liquid crystal display of claim 2, wherein each of the pixel electrodes (PE) includes one right slant parallelogrammic electrode piece (196) and one left slant parallelogrammic electrode piece (197).

4. The liquid crystal display of claim 3, wherein each of the pixel electrodes (PE) includes two right slant parallelogrammic electrode pieces and two left slant parallelogrammic electrode pieces.

5. The liquid crystal display of claim 4, wherein the right slant parallelogrammic electrode pieces and the left slant parallelogrammic electrode pieces are alternately arrayed upward and downward.

6. The liquid crystal display of claim 5, wherein each of the first and second gate lines (GLa, GLb; 121a, 121b) extends along a boundary where the right slant parallelogrammic electrode pieces and the left slant parallelogrammic electrode pieces are connected to each other in an up-down direction.

7. The liquid crystal display of claim 1,
wherein each of the pixel electrodes (PE) of the first and second pixels (PX) includes three right slant parallelogrammic electrode pieces and three left slant parallelogrammic electrode pieces, and
wherein the pixel electrode (PE) of the third pixel includes two right slant parallelogrammic electrode pieces and two left slant parallelogrammic electrode pieces.

8. The liquid crystal display of claim 7,
wherein the three right slant parallelogrammic electrode pieces and the three left slant parallelogrammic electrode pieces of the pixel electrode (PE) of each of the first and second pixels (PX) are connected to each other in an up-down direction to constitute a first base electrode, a second base electrode and a third base electrode,
wherein the first and second base electrodes are connected to each other in a row direction,
wherein the first and third base electrodes are connected to each other in a column direction, and
wherein the right slant parallelogrammic electrode pieces and the left slant parallelogrammic electrode pieces of the pixel electrode (PE) of the third pixel are alternately connected upwardly and downwardly.

9. The liquid crystal display of claim 7, wherein areas of the pixel electrodes (PE) of the first, second, and third pixels (PX) are substantially equal to each other.

10. The liquid crystal display of claim 9, wherein a width of the pixel electrode (PE) of the third pixel is greater than widths of the pixel electrodes (PE) of the first and second pixels (PX).

11. The liquid crystal display of claim 10, wherein the width of the pixel electrode (PE) of the third pixel is 1.4 to 1.6 times the widths of the first and second pixels (PX).

12. The liquid crystal display of claim 1, wherein the first pixel is connected to the first gate line.

13. The liquid crystal display of claim 1, wherein the second pixel is connected to the second gate line.

14. The liquid crystal display of claim 1, wherein the third pixels (PX) at different columns are alternately connected to the first or second gate line.

15. The liquid crystal display of claim 14, wherein the third pixels (PX) at the different columns are alternately charged.

16. The liquid crystal display of claim 1, further comprising gate protrusions, wherein at least one gate protrusion is disposed at portions where the data lines (DL; 171) intersect the first and second gate lines (GLa, GLb; 121a, 121b).

17. The liquid crystal display of claim 1, wherein each of the pixel electrodes (PE) has four edges that are parallel to the gate and data lines (DL; 171).

18. The liquid crystal display of claim 17, wherein a portion of the data line overlaps the pixel electrode (PE).

19. The liquid crystal display of claim 17, wherein the pixel electrode (PE) covers first and second gate lines (GLa, GLb; 121a, 121b) of a last stage.

20. The liquid crystal display of claim 1, further comprising storage electrode lines that transmit storage electrode signals.

21. The liquid crystal display of claim 20, wherein the storage electrode lines include extensions that extend upward and downward.

22. The liquid crystal display of claim 21, wherein the extensions of the storage electrode lines extend into spaces between adjacent pixel electrodes (PE).

23. The liquid crystal display of claim 1, wherein each of the data lines (DL; 171) includes first and second portions that overlap two adjacent pixel electrodes (PE), respectively.

24. The liquid crystal display of claim 23, wherein areas of the first and second portions of each data line are equal to each other.

25. The liquid crystal display of claim 23, wherein the first portion includes third and fourth portions that are separated from one of the two pixel electrodes (PE) and overlap one of the two adjacent pixel electrodes (PE).

26. The liquid crystal display of claim 25, wherein the third and fourth portions of the data line are disposed along a straight line, and the second portion is curved at the third and fourth portions.

27. The liquid crystal display of claim 1, wherein each data line extends in a straight line.

28. The liquid crystal display of claim 1, further comprising organic films that are formed between the pixel electrodes (PE) and the data lines (DL; 171) and between the pixel electrodes (PE) and the first and second gate lines (GLa, GLb; 121a, 121b).

29. The liquid crystal display of claim 1, further comprising a plurality of color filters that are disposed under the pixel electrodes (PE).

Patentansprüche

1. Flüssigkristallanzeige, umfassend:

eine Vielzahl von Pixeln (PX), enthaltend Pixelelektroden (PE) und Schaltvorrichtungen (Q), die mit den Pixelelektroden (PE) verbunden und in einer Matrix angeordnet sind;
eine Vielzahl von Paaren erster und zweiter Gateleitungen (GLa, GLb; 121a, 121b), wobei jedes Paar aus einer ersten Gateleitung (GLa; 121a) und einer mit dieser zusammenhängenden zweiten Gateleitung (GLb, 121 b), von der erstere beabstandet ist, besteht, wobei die Paare erster und zweiter Gateleitungen (GLa, GLb; 121a, 121b) mit den Schaltvorrichtungen (Q) verbunden und voneinander getrennt sind, und eine Vielzahl von Datenleitungen (DL; 171), die mit den Schaltvorrichtungen (Q) verbunden sind und die ersten und zweiten Gateleitungen (GLa, GLb; 121a, 121b) schneiden, wobei
die Vielzahl von Datenleitungen (DL; 171) so verbunden sind, dass Endabschnitte zweier Datenleitungen (DR1, DG1, DB1; DR2, DG2, Db2) jedes Paars von Datenleitungen miteinander verbunden sind, wobei jedes der Pixel (PX) ein erstes Pixel (RP1; RP2), ein zweites Pixel (GP1; GP2) und ein drittes Pixel (BP1; BP2) umfasst, die drei unterschiedliche Farben darstellen,
dadurch gekennzeichnet, dass
eine Datenleitung (DR1; DR2), die mit dem ersten Pixel (RP1; RP2) verbunden ist, und eine Datenleitung (DG1; DG2), die mit dem zweiten Pixel (GP1; GP2) verbunden ist, miteinander

verbunden sind, und
wobei zwei benachbarte Datenleitungen (DB1; DB2), die mit den dritten Pixeln (BP1, BP2) verbunden sind, miteinander verbunden sind.

2. Flüssigkristallanzeige nach Anspruch 1, wobei jede der Pixelelektroden (PE) mindestens zwei parallelogrammförmige Elektrodenstücke (196, 197) mit jeweils unterschiedlichen Neigungsrichtungen aufweist.

3. Flüssigkristallanzeige nach Anspruch 2, wobei jede der Pixelelektroden (PE) mindestens ein nach rechts geneigtes parallelogrammförmiges Elektrodenstück (196) und ein nach links geneigtes parallelogrammförmiges Elektrodenstück (197) aufweist.

4. Flüssigkristallanzeige nach Anspruch 3, wobei jede der Pixelelektroden (PE) zwei nach rechts geneigte parallelogrammförmige Elektrodenstücke und zwei nach links geneigte parallelogrammförmige Elektrodenstücke aufweist.

5. Flüssigkristallanzeige nach Anspruch 4, wobei die nach rechts geneigten parallelogrammförmigen Elektrodenstücke und die nach links geneigten parallelogrammförmigen Elektrodenstücke abwechselnd aufwärts und abwärts angeordnet sind.

6. Flüssigkristallanzeige nach Anspruch 5, wobei jede der ersten und zweiten Gateleitungen (GLa, GLb; 121a, 121b) entlang einer Grenze verläuft, an der die nach rechts geneigten parallelogrammförmigen Elektrodenstücke und die nach links geneigten parallelogrammförmigen Elektrodenstücke in Richtung von oben nach unten miteinander verbunden sind.

7. Flüssigkristallanzeige nach Anspruch 1, wobei jede der Pixelelektroden (PE) der ersten und zweiten Pixel (PX) drei nach rechts geneigte parallelogrammförmige Elektrodenstücke und drei nach links geneigte parallelogrammförmige Elektrodenstücke aufweist, und
wobei die Pixelelektrode (PE) des dritten Pixels zwei nach rechts geneigte parallelogrammförmige Elektrodenstücke und zwei nach links geneigte parallelogrammförmige Elektrodenstücke aufweist.

8. Flüssigkristallanzeige nach Anspruch 7, wobei die drei nach rechts geneigten parallelogrammförmigen Elektrodenstücke und die drei nach links geneigten parallelogrammförmigen Elektrodenstücke der Pixelelektrode (PE) jedes der ersten und zweiten Pixel (PX) in Richtung von oben nach unten miteinander verbunden sind, um eine erste Basiselektrode, eine zweite Basiselektrode und eine dritte Basiselektrode zu bilden,
wobei die erste und zweite Basiselektrode in einer Reihenrichtung miteinander verbunden sind,
wobei die erste und dritte Basiselektrode in einer Spaltenrichtung miteinander verbunden sind, und
wobei die nach rechts geneigten parallelogrammförmigen Elektrodenstücke und die nach links geneigten parallelogrammförmigen Elektrodenstücke der Pixelelektrode (PE) des dritten Pixels abwechselnd aufwärts und abwärts verbunden sind.

9. Flüssigkristallanzeige nach Anspruch 7, wobei Bereiche der Pixelelektroden (PE) der ersten, zweiten und dritten Pixel (PX) im Wesentlichen einander entsprechen.

10. Flüssigkristallanzeige nach Anspruch 9, wobei eine Breite der Pixelelektrode (PE) des dritten Pixels größer als Breiten der Pixelelektroden (PE) der ersten und zweiten Pixel (PX) ist.

11. Flüssigkristallanzeige nach Anspruch 10, wobei die Breite der Pixelelektrode (PE) des dritten Pixels dem 1,4- bis 1,6-fachen der Breiten der ersten und zweiten Pixel (PX) entspricht.

12. Flüssigkristallanzeige nach Anspruch 1, wobei das erste Pixel mit der ersten Gateleitung verbunden ist.

13. Flüssigkristallanzeige nach Anspruch 1, wobei das zweite Pixel mit der zweiten Gateleitung verbunden ist.

14. Flüssigkristallanzeige nach Anspruch 1, wobei die dritten Pixel (PX) an unterschiedlichen Spalten abwechselnd mit der ersten oder zweiten Gateleitung verbunden sind.

15. Flüssigkristallanzeige nach Anspruch 14, wobei die dritten Pixel (PX) an den unterschiedlichen Spalten alternierend geladen sind.

16. Flüssigkristallanzeige nach Anspruch 1, ferner umfassend Gate-Vorsprünge, wobei wenigstens ein Gate-Vorsprung an Abschnitten angeordnet ist, an denen die Datenleitungen (DL; 171) die ersten und zweiten Gateleitungen (GLa, GLb; 121a, 121b) schneiden.

17. Flüssigkristallanzeige nach Anspruch 1, wobei jede der Pixelelektroden (PE) vier Ränder aufweist, die parallel zu den Gate- und Datenleitungen (DL; 171) verlaufen.

18. Flüssigkristallanzeige nach Anspruch 17, wobei ein Abschnitt der Datenleitung die Pixelelektrode (PE) überlappt.

19. Flüssigkristallanzeige nach Anspruch 17, wobei die Pixelelektrode (PE) die ersten und zweiten Gatelei-

tungen (GLa, GLb; 121a, 121b) einer letzten Stufe überdeckt.

20. Flüssigkristallanzeige nach Anspruch 1, ferner umfassend Speicherelektrodenleitungen, die Speicherelektrodensignale übertragen.

21. Flüssigkristallanzeige nach Anspruch 20, wobei die Speicherelektrodenleitungen nach oben und unten verlaufende Erweiterungen umfassen.

22. Flüssigkristallanzeige nach Anspruch 21, wobei die Erweiterungen der Speicherelektrodenleitungen sich in Räume zwischen benachbarten Pixelelektroden (PE) erstrecken.

23. Flüssigkristallanzeige nach Anspruch 1, wobei jede der Datenleitungen (DL; 171) erste und zweite Abschnitte umfasst, die jeweils zwei benachbarte Pixelelektroden (PE) überlappen.

24. Flüssigkristallanzeige nach Anspruch 23, wobei Bereiche der ersten und zweiten Abschnitte jeder Datenleitung einander entsprechen.

25. Flüssigkristallanzeige nach Anspruch 23, wobei der erste Abschnitt dritte und vierte Abschnitte umfasst, die von einer der beiden Pixelelektroden (PE) getrennt sind und eine der beiden benachbarten Pixelelektroden (PE) überlappen.

26. Flüssigkristallanzeige nach Anspruch 25, wobei die dritten und vierten Abschnitte der Datenleitung entlang einer geraden Linie angeordnet sind und der zweite Abschnitt an den dritten und vierten Abschnitten gekrümmt ist.

27. Flüssigkristallanzeige nach Anspruch 1, wobei jede Datenleitung geradlinig verläuft.

28. Flüssigkristallanzeige nach Anspruch 1, ferner umfassend organische Filme, die zwischen den Pixelelektroden (PE) und den Datenleitungen (DL; 171) und zwischen den Pixelelektroden (PE) und den ersten und zweiten Gateleitungen (GLa, GLb; 121a, 121b) gebildet sind.

29. Flüssigkristallanzeige nach Anspruch 1, ferner umfassend eine Vielzahl von Farbfiltern, die unter den Pixelelektroden (PE) angeordnet sind.

Revendications

1. Afficheur à cristaux liquides comprenant :

une pluralité de pixels (PX) incluant des électrodes de pixel (PE) et des dispositifs de commutation (Q) connectés aux électrodes de pixel (PE) et agencés en une matrice ;
une pluralité de paires de première et deuxième lignes de grille (GLa, GLb ; 121a, 121b), chaque paire étant constituée d'une première ligne de grille (GLa ; 121a) s'étendant à une certaine distance d'une deuxième ligne de grille interreliée (GLb ; 121b), les paires de première et deuxième lignes de grille (GLa, GLb ; 121a, 121b) étant connectées aux dispositifs de commutation (Q) et séparées l'une de l'autre ; et
une pluralité de lignes de données (DL ; 171) connectées aux dispositifs de commutation (Q) et croisant les première et deuxième lignes de grille (GLa, GLb ; 121a, 121b), la pluralité de lignes de données (DL; 171) étant connectées de sorte que des parties d'extrémité de deux lignes de données (DR1, DG1, DB1 ; DR2, DG2, Db2) dans chaque paire de lignes de données sont connectées l'une à l'autre, chacun des pixels (PX) incluant un premier pixel (RP1 ; RP2), un deuxième pixel (GP1 ; GP2) et un troisième pixel (BP1 ; BP2) représentant trois couleurs différentes, respectivement.
caractérisé en ce que
une ligne de données (DR1 ; DR2) connectée au premier pixel (RP1 ; RP2) et une ligne de données (DG1 ; DG2) connectée au deuxième pixel (GP1 ; GP2) sont connectées l'une à l'autre et
dans lequel deux lignes de données adjacentes (DB1, DB2) connectées aux troisièmes pixels (BP1 ; BP2) sont connectées l'une à l'autre.

2. Afficheur à cristaux liquides selon la revendication 1, dans lequel chacune des électrodes de pixel (PE) inclut au moins deux pièces d'électrode en forme de parallélogramme (196, 197) ayant des directions d'inclinaison respectives différentes.

3. Afficheur à cristaux liquides selon la revendication 2, dans lequel chacune des électrodes de pixel (PE) inclut une pièce d'électrode en forme de parallélogramme incliné vers la droite (196) et une pièce d'électrode en forme de parallélogramme incliné vers la gauche (197).

4. Afficheur à cristaux liquides selon la revendication 3, dans lequel chacune des électrodes de pixel (PE) inclut deux pièces d'électrode en forme de parallélogramme incliné vers la droite et deux pièces d'électrode en forme de parallélogramme incliné vers la gauche.

5. Afficheur à cristaux liquides selon la revendication 4, dans lequel les pièces d'électrode en forme de parallélogramme incliné vers la droite et les pièces d'électrode en forme de parallélogramme incliné

vers la gauche sont disposées alternativement vers le haut et vers le bas.

6. Afficheur à cristaux liquides selon la revendication 5, dans lequel chacune des première et deuxième lignes de grille (GLa, GLb ; 121a, 121b) s'étend le long d'une limite où les pièces d'électrode en forme de parallélogramme incliné vers la droite et les pièces d'électrode en forme de parallélogramme incliné vers la gauche sont connectées l'une à l'autre dans une direction descendante.

7. Afficheur à cristaux liquides selon la revendication 1, dans lequel chacune des électrodes de pixel (PE) des premier et deuxième pixels (PX) inclut trois pièces d'électrode en forme de parallélogramme incliné vers la droite et trois pièces d'électrode en forme de parallélogramme incliné vers la gauche, et
dans lequel l'électrode de pixel (PE) du troisième pixel inclut deux pièces d'électrode en forme de parallélogramme incliné vers la droite et deux pièces d'électrode en forme de parallélogramme incliné vers la gauche.

8. Afficheur à cristaux liquides selon la revendication 7, dans lequel les trois pièces d'électrode en forme de parallélogramme incliné vers la droite et les trois pièces d'électrode en forme de parallélogramme incliné vers la gauche de l'électrode de pixel (PE) de chacun des premier et deuxième pixels (PX) sont connectées l'une à l'autre dans une direction descendante pour constituer une première électrode de base, une deuxième électrode de base et une troisième électrode de base,
dans lequel les première et deuxième électrodes de base sont connectées l'une à l'autre dans une direction de rangée,
dans lequel les première et troisième électrodes de base sont connectées l'une à l'autre dans une direction de colonne, et
dans lequel les pièces d'électrode en forme de parallélogramme incliné vers la droite et les pièces d'électrode en forme de parallélogramme incliné vers la gauche de l'électrode de pixel (PE) du troisième pixel sont alternativement connectées vers le haut et vers le bas.

9. Afficheur à cristaux liquides selon la revendication 7, dans lequel les zones des électrodes de pixel (PE) des premier, deuxième et troisième pixels (PX) sont sensiblement égales entre elles.

10. Afficheur à cristaux liquides selon la revendication 9, dans lequel une largeur de l'électrode de pixel (PE) du troisième pixel est supérieure aux largeurs des électrodes de pixel (PE) des premier et deuxième pixels (PX).

11. Afficheur à cristaux liquides selon la revendication 10, dans lequel la largeur de l'électrode de pixel (PE) du troisième pixel est de 1,4 à 1,6 fois les largeurs des premier et deuxième pixels (PX).

12. Afficheur à cristaux liquides selon la revendication 1, dans lequel le premier pixel est connecté à la première ligne de grille.

13. Afficheur à cristaux liquides selon la revendication 1, dans lequel le deuxième pixel est connecté à la deuxième ligne de grille.

14. Afficheur à cristaux liquides selon la revendication 1, dans lequel les troisièmes pixels (PX) à différentes colonnes sont connectés alternativement à la première ou à la deuxième ligne de grille.

15. Afficheur à cristaux liquides selon la revendication 14, dans lequel les troisièmes pixels (PX) aux différentes colonnes sont chargés alternativement.

16. Afficheur à cristaux liquides selon la revendication 1, comprenant en outre des saillies de grille, dans lequel au moins une saillie de grille est disposée sur des parties où les lignes de données (DL ; 171) croisent les première et deuxième lignes de grille (GLa, GLb ; 121a, 121b).

17. Afficheur à cristaux liquides selon la revendication 1, dans lequel chacune des électrodes de pixel (PE) comporte quatre arêtes qui sont parallèles aux lignes de grille et de données (DL ; 171).

18. Afficheur à cristaux liquides selon la revendication 17, dans lequel une partie de la ligne de données chevauche l'électrode de pixel (PE).

19. Afficheur à cristaux liquides selon la revendication 17, dans lequel l'électrode de pixel (PE) recouvre les première et deuxième lignes de grille (GLa, GLb ; 121a, 121b) d'un dernier étage.

20. Afficheur à cristaux liquides selon la revendication 1, comprenant en outre des lignes d'électrode de stockage qui transmettent des signaux d'électrode de stockage.

21. Afficheur à cristaux liquides selon la revendication 20, dans lequel les lignes d'électrode de stockage incluent des extensions qui s'étendent vers le haut et vers le bas.

22. Afficheur à cristaux liquides selon la revendication 21, dans lequel les extensions des lignes d'électrode de stockage s'étendent dans les espaces entre des électrodes de pixel (PE) adjacentes.

23. Afficheur à cristaux liquides selon la revendication 1, dans lequel chacune des lignes de données (DL; 171) inclut des première et deuxième parties qui chevauchent respectivement deux électrodes de pixel (PE) adjacentes.

24. Afficheur à cristaux liquides selon la revendication 23, dans lequel les zones des première et deuxième parties de chaque ligne de données sont égales entre elles.

25. Afficheur à cristaux liquides selon la revendication 23, dans lequel la première partie inclut des troisième et quatrième parties qui sont séparées de l'une des deux électrodes de pixel (PE) et chevauchent l'une des deux électrodes de pixel (PE) adjacentes.

26. Afficheur à cristaux liquides selon la revendication 25, dans lequel les troisième et quatrième parties de la ligne de données sont disposées le long d'une ligne droite et la deuxième partie est incurvée au niveau des troisième et quatrième parties.

27. Afficheur à cristaux liquides selon la revendication 1, dans lequel chaque ligne de données s'étend en ligne droite.

28. Afficheur à cristaux liquides selon la revendication 1, comprenant en outre des films organiques qui sont formés entre les électrodes de pixel (PE) et les lignes de données (DL ; 171) et entre les électrodes de pixel (PE) et les première et deuxième lignes de grille (GLa, GLb ; 121a, 121b).

29. Afficheur à cristaux liquides selon la revendication 1, comprenant en outre une pluralité de filtres de couleur qui sont disposés sous les électrodes de pixel (PE).

FIG.1

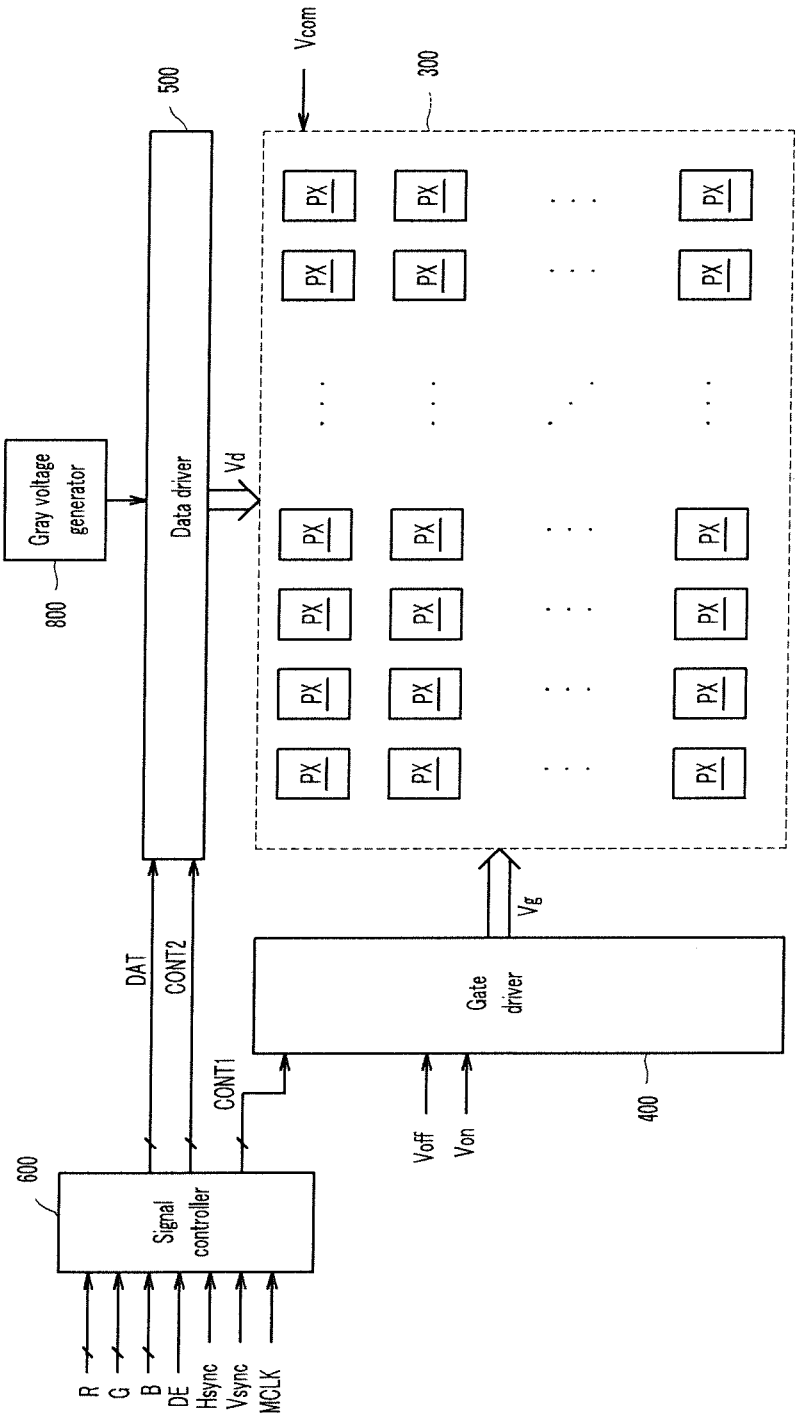

Vcom
500
300
PX
Gray voltage generator
800
Data driver
Vd
DAT
CONT2
CONT1
Gate driver
Vg
Voff
Von
400
600
Signal controller
R
G
B
DE
Hsync
Vsync
MCLK

FIG.2

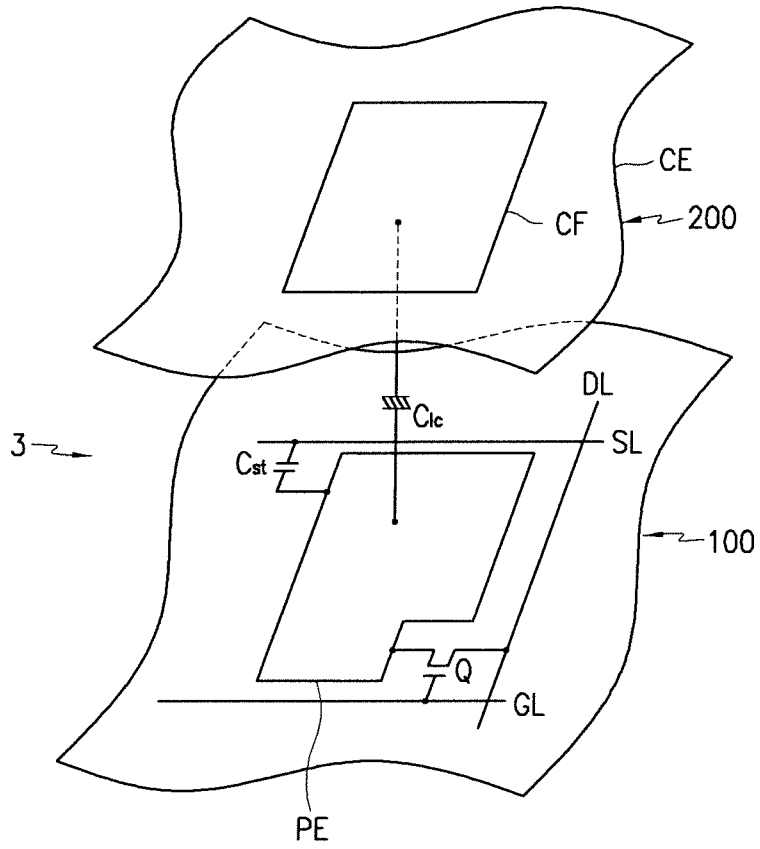


FIG.3A

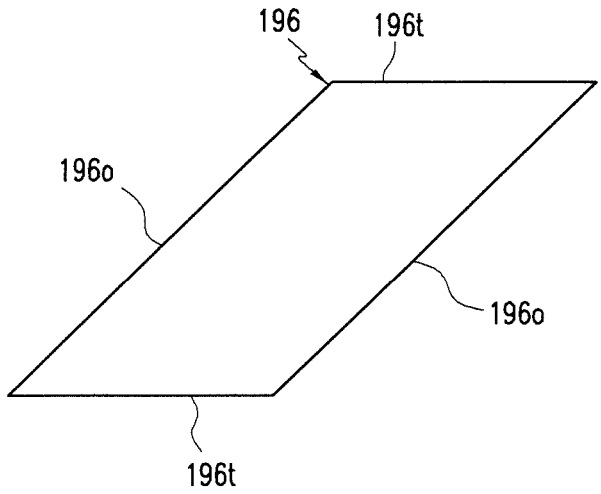


FIG.3B

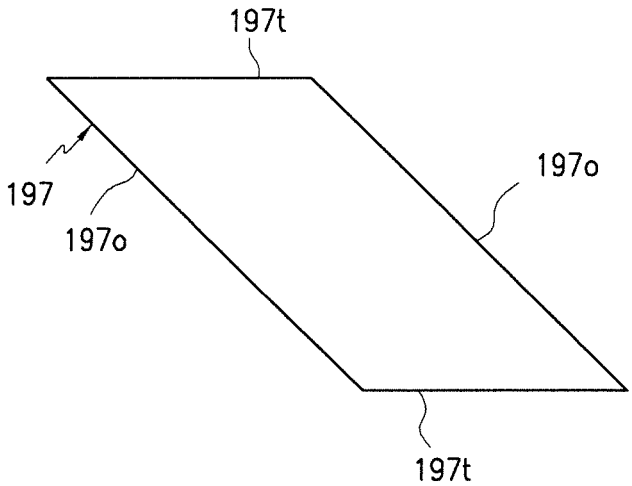


FIG.4

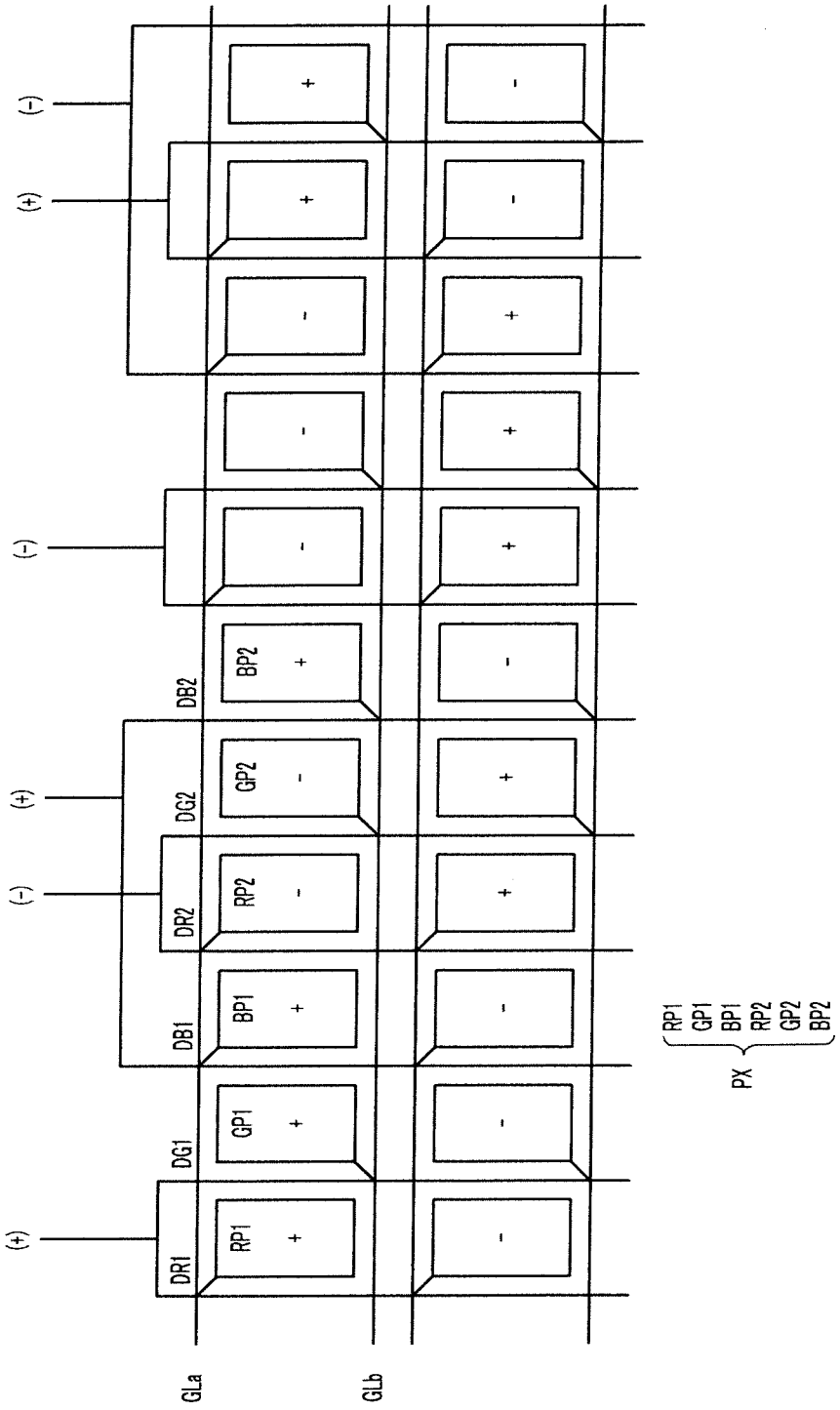


FIG.5A

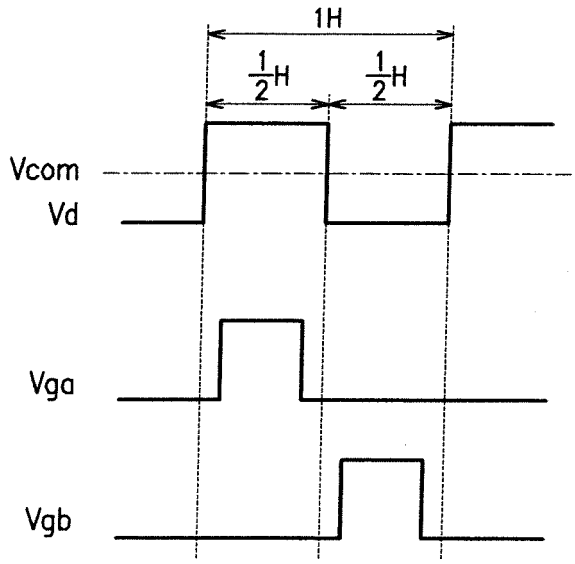


FIG.5B

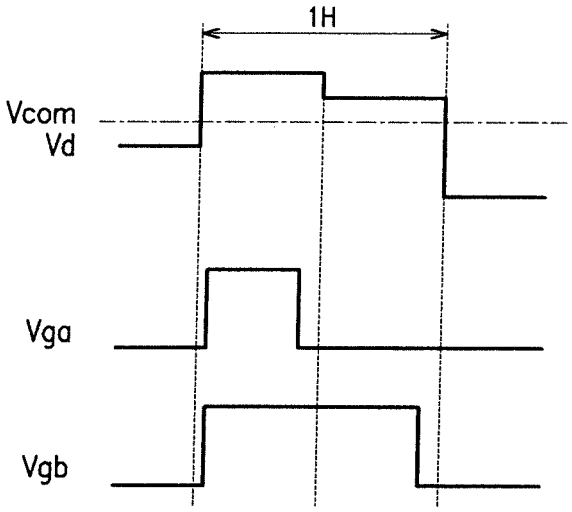
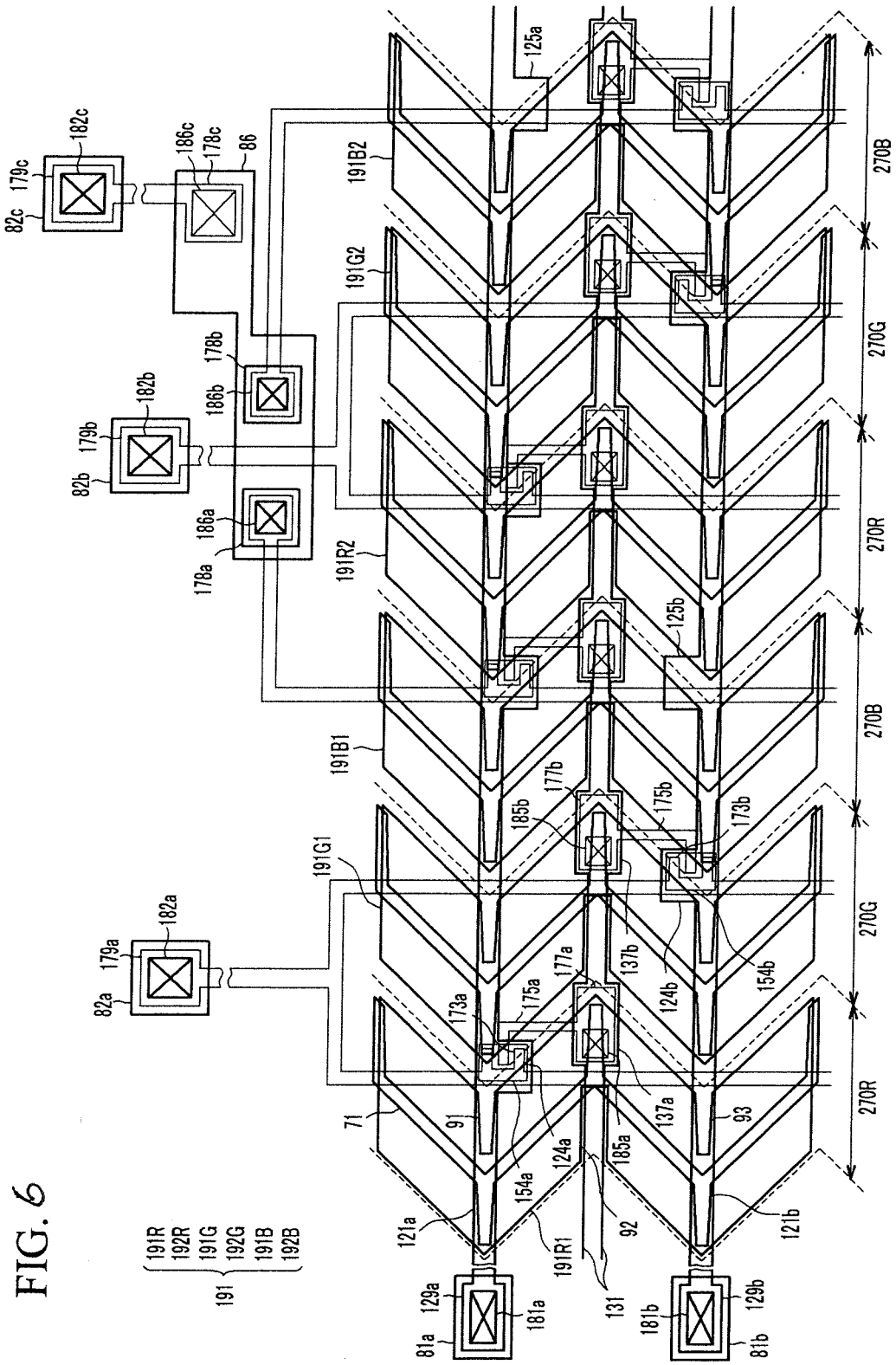


FIG. 6


191R
192R
191G
192G
191B
192B
191
270B
270G
270R
270B
270G
270R
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191G2
191R2
125b
191B1
191G1
71
91
93
92
121a
121b
191R1
131
82a
179a
182a
82b
179b
182b
82c
179c
182c
178a
186a
178b
186b
178c
186c
86
81a
129a
181a
81b
129b
181b
154a
124a
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137a
173a
175a
177a
137b
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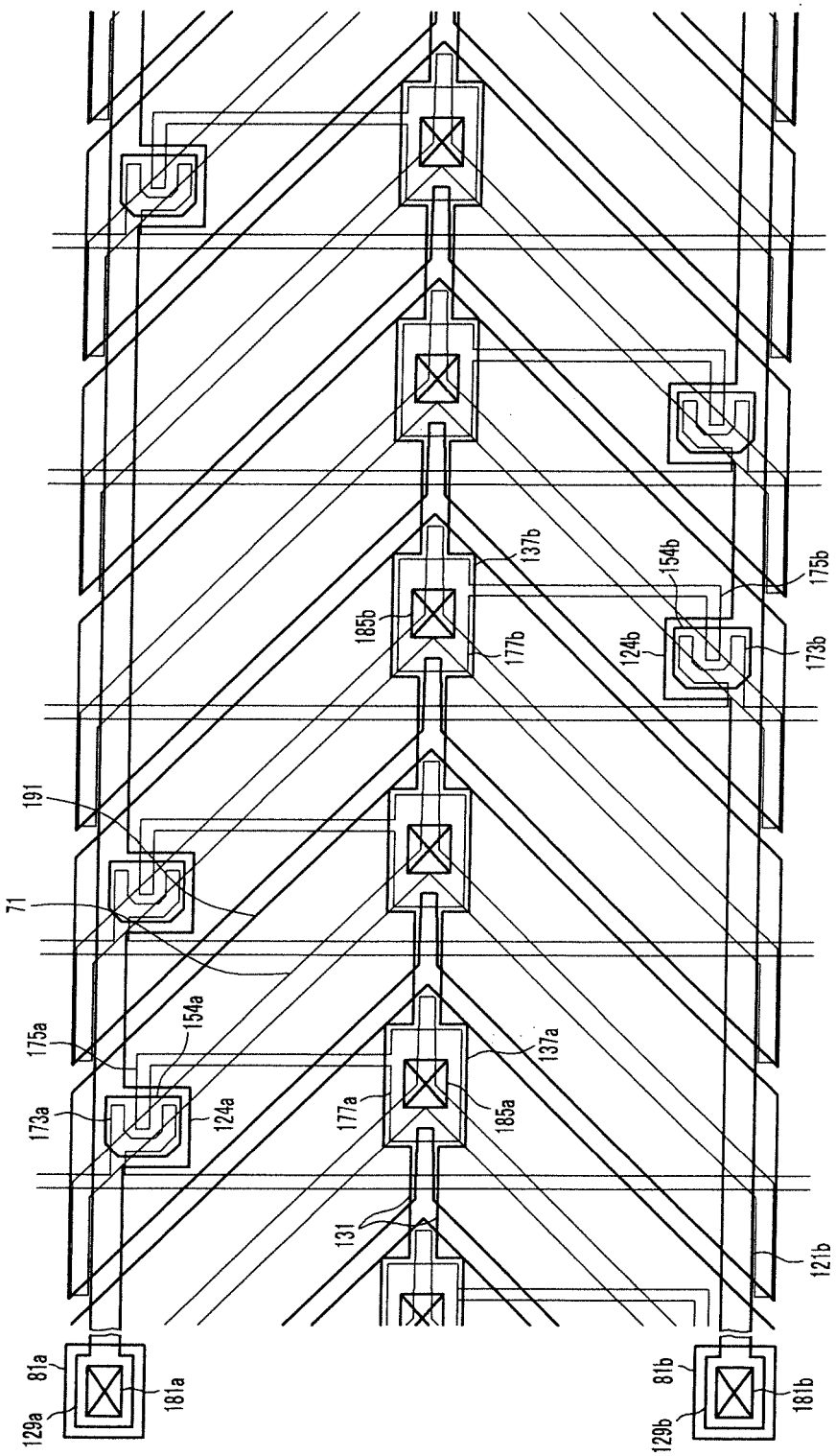
154b
173b
175b
177b
185b

FIG. 7


191
71
175a
154a
137a
173a
124a
177a
185a
131
121b
81a
129a
181a
81b
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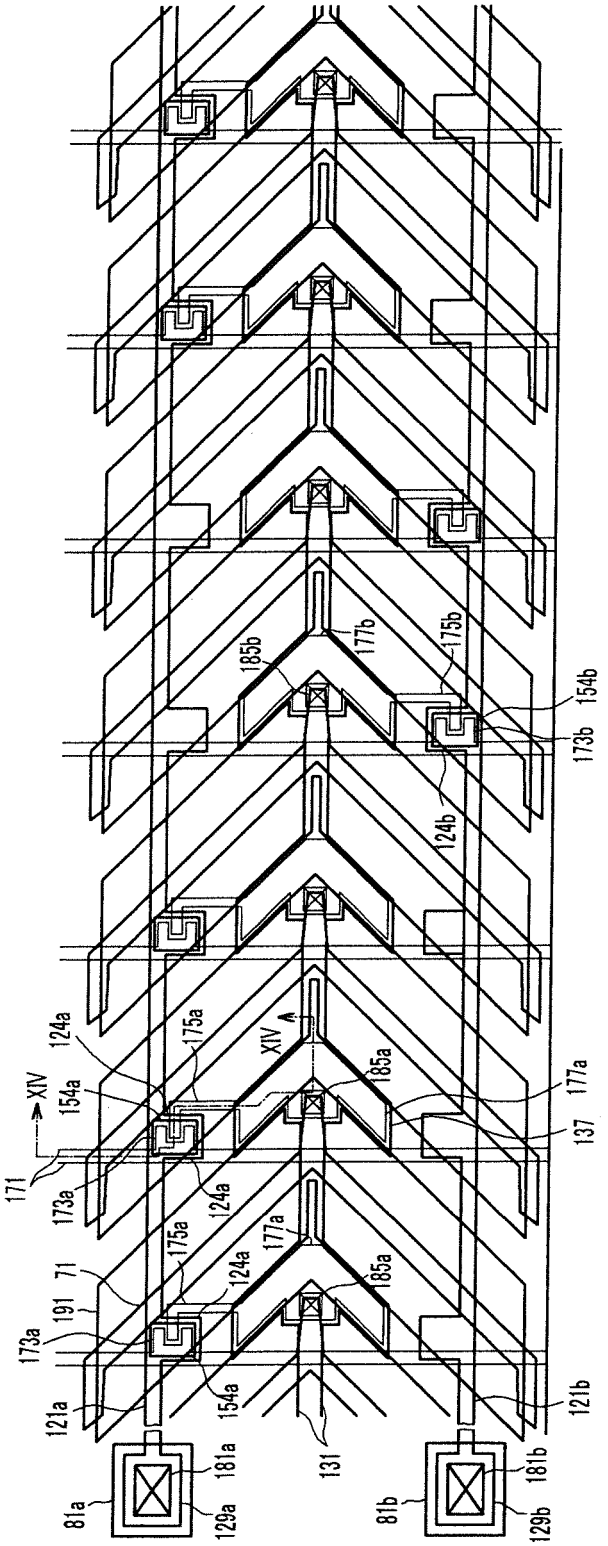
181b
137b
154b
175b
185b
177b
124b
173b

FIG.8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175b
154b
173b
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175a
XIV
185a
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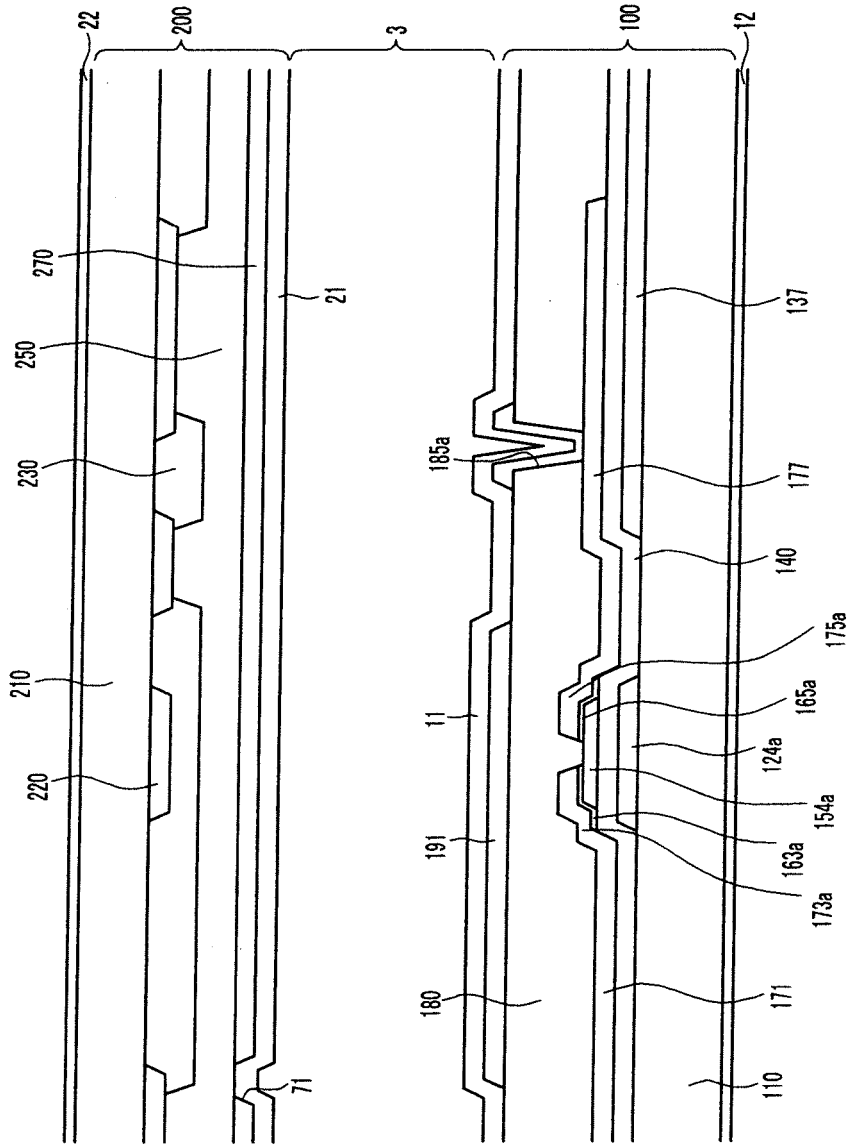
171
173a
71
191
121a
131
121b
181a
181b
81a
81b
129a
129b

FIG. 9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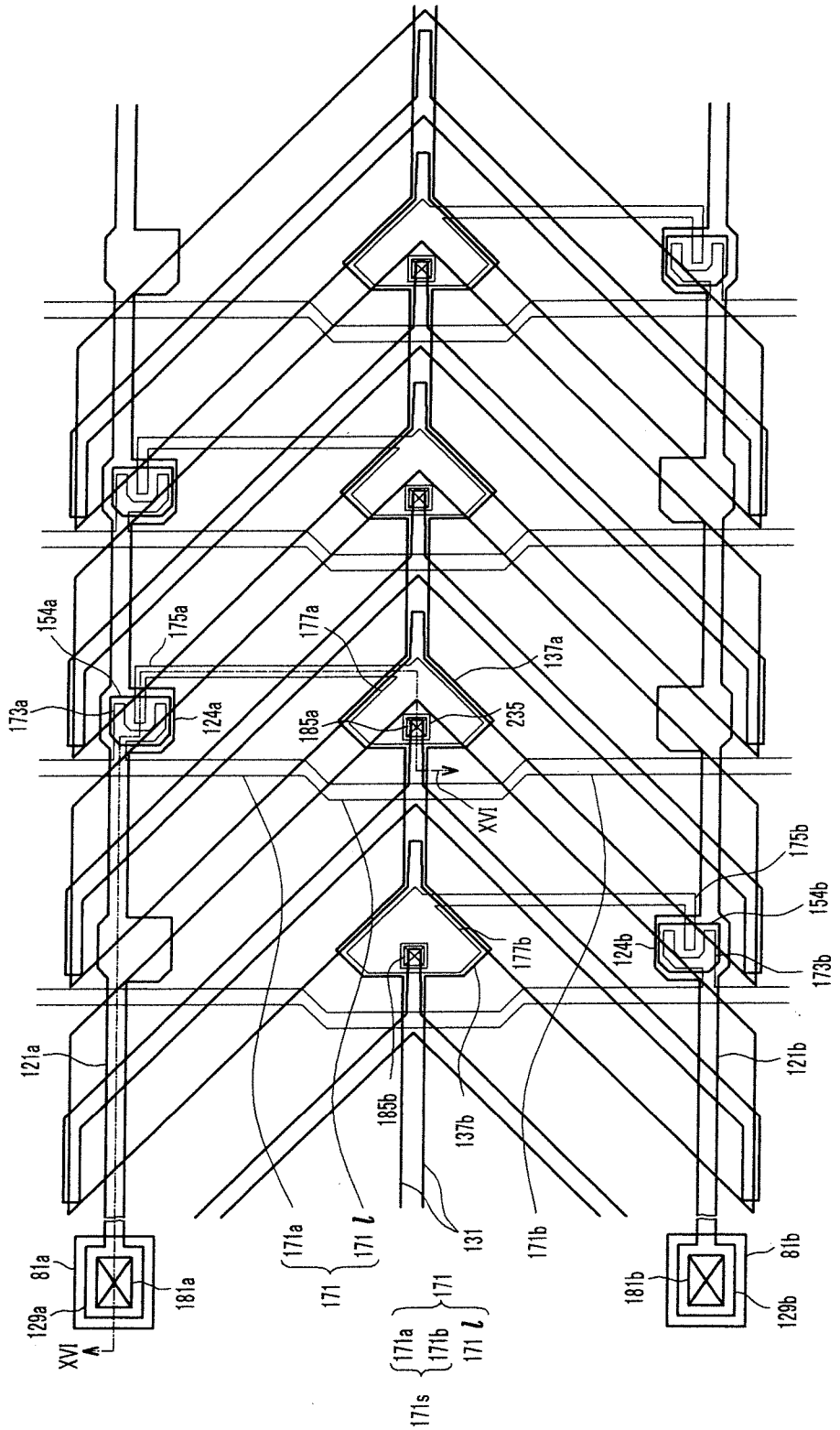
250
230
210
220
21
71
185a
11
191
180
137
177
140
175a
165a
124a
154a
163a
173a
171
110

FIG. 10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177a
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173a
124a
185a
235
XVI
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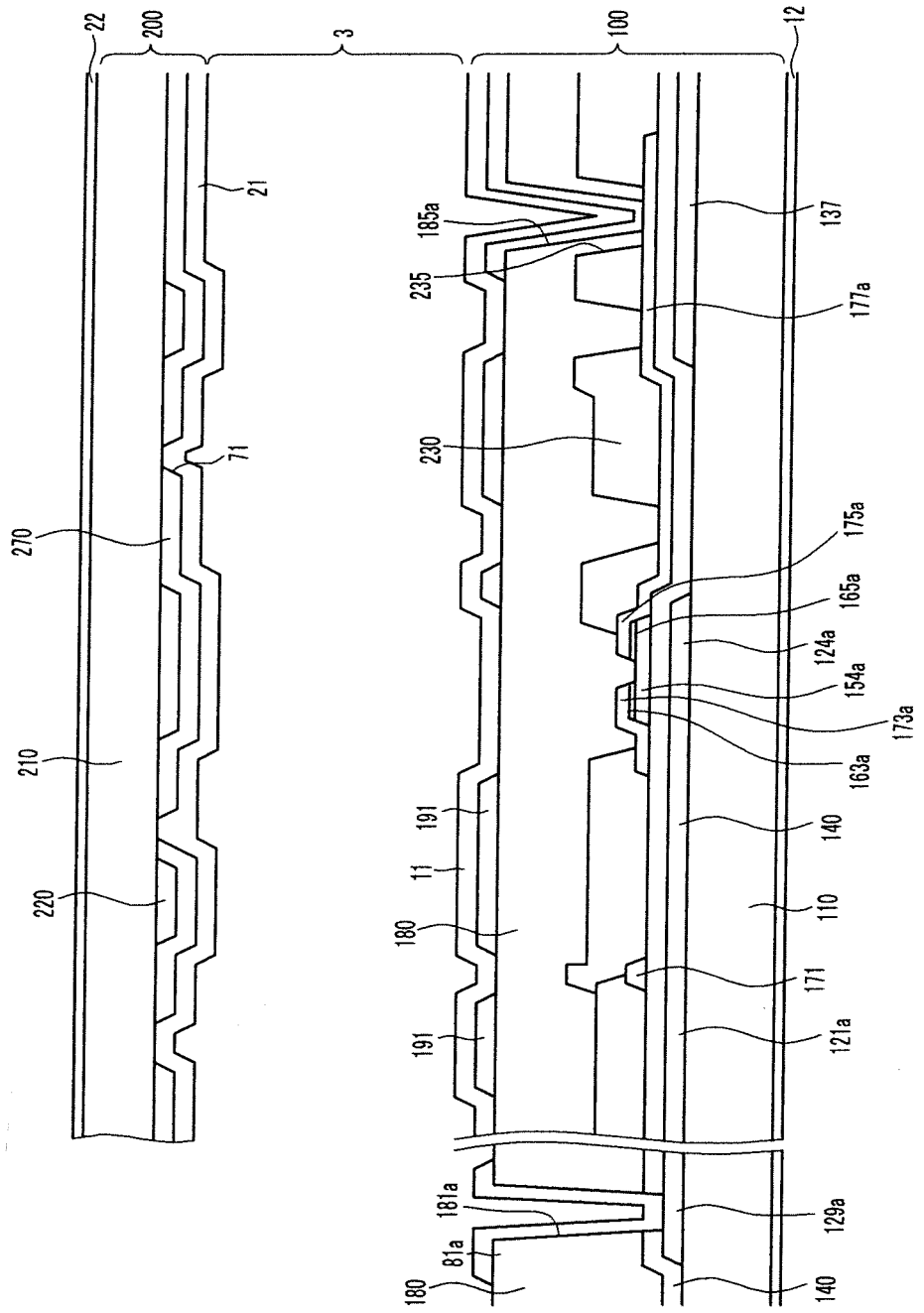
154b
177b
124b
173b
121a
121b
185b
137b
171a
171
131
171b
81a
181a
129a
XVI
171a
171b
171s
181b
81b
129b

FIG. 11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137
177a
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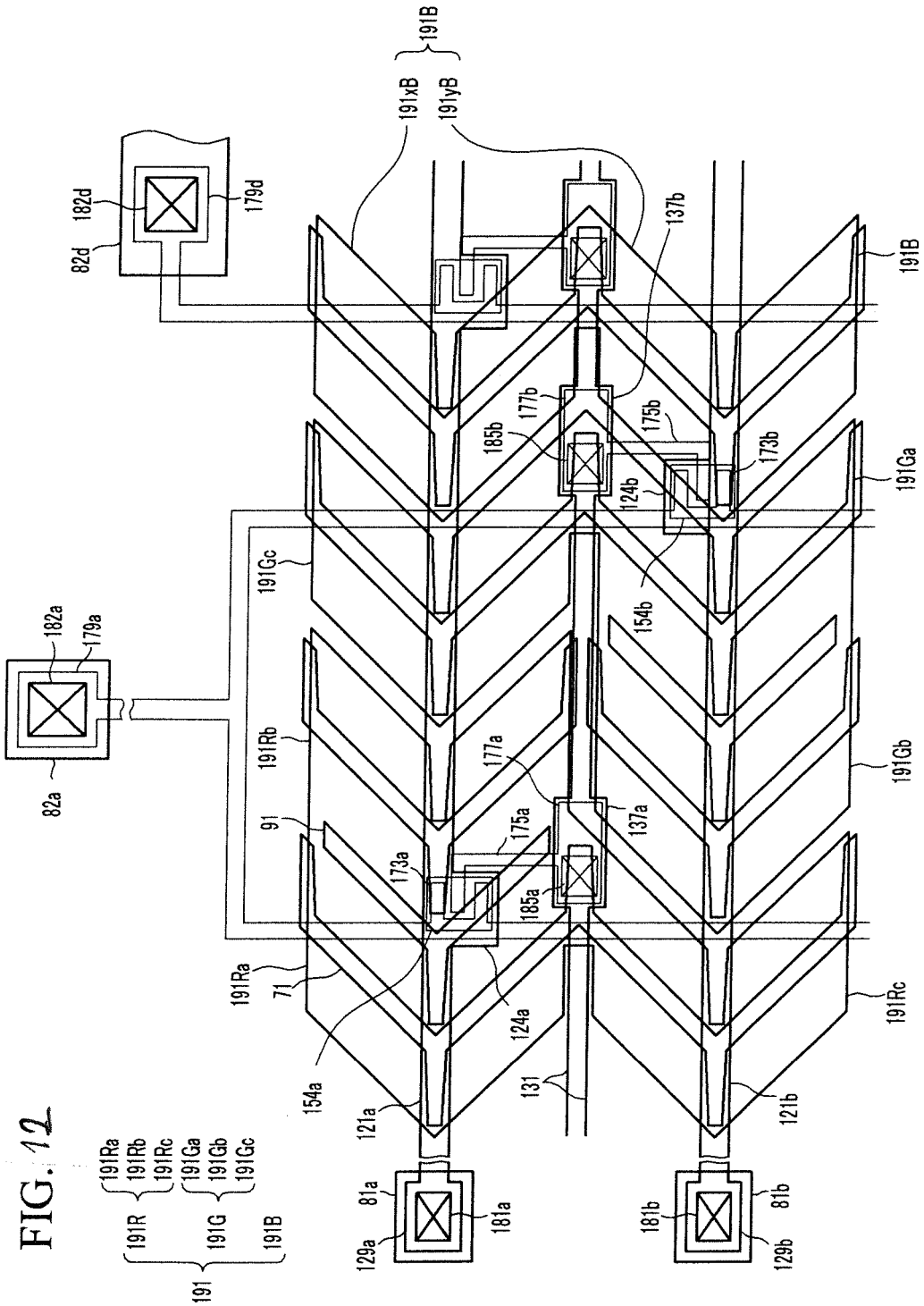
173a
163a
191
11
180
140
110
171
121a
181a
81a
129a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182d
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173b
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124b
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182a
179a
82a
191Rb
177a
91
175a
137a
191Gb
173a
185a
191Ra
71
124a
191Rc
154a
131
121a
121b
81a
81b
181a
181b
129a
129b
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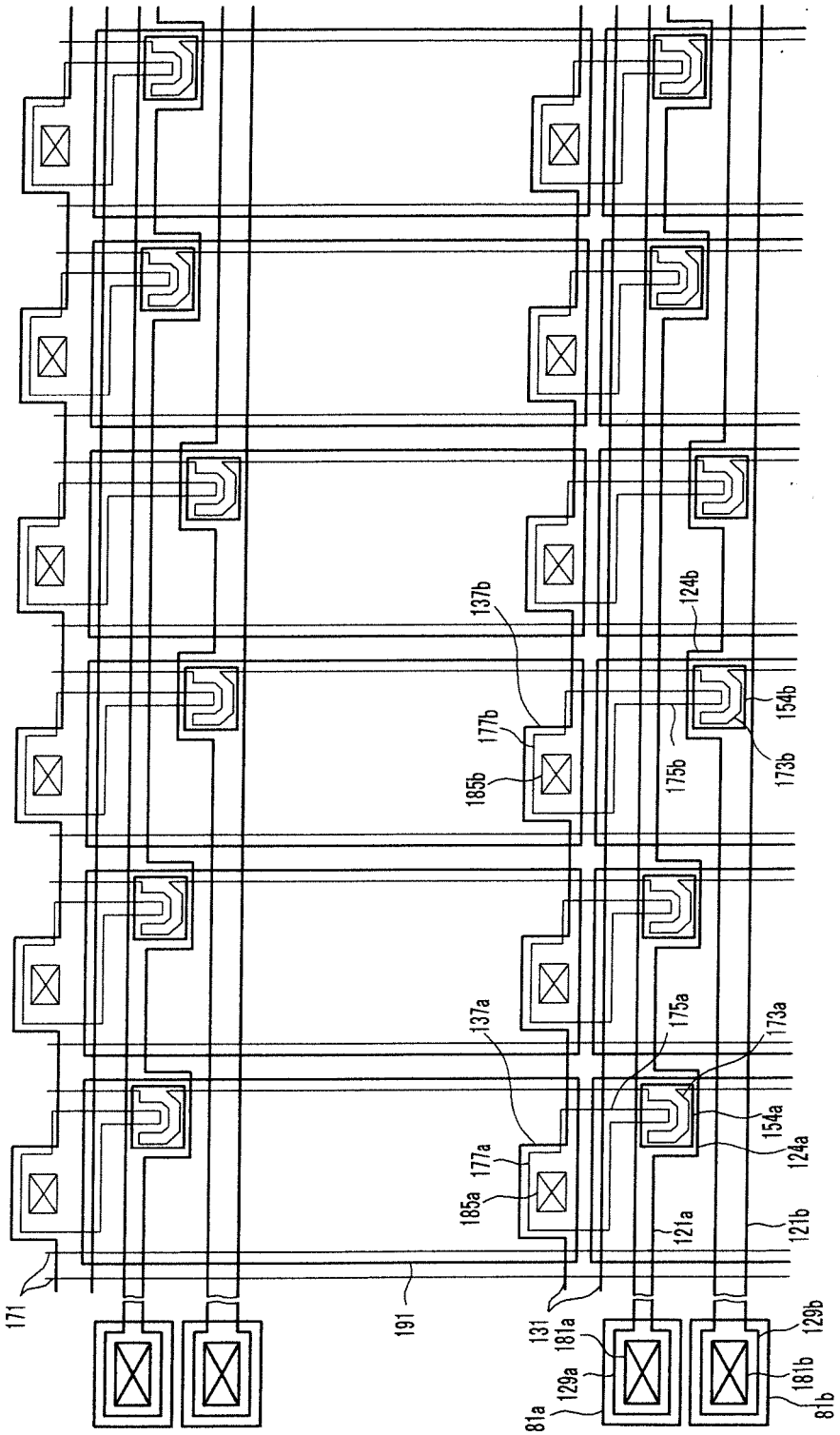
191Rb
191Rc
191Ga
191Gb
191Gc
191R
191G
191B
191

FIG. 12

FIG. 13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121b
171
191
131
181a
129b
129a
181b
81a
81b

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- FR 2719936 A1 **[0009]**

专利名称(译)	液晶显示器		
公开(公告)号	EP1775624B1	公开(公告)日	2017-12-13
申请号	EP2006020802	申请日	2006-10-04
[标]申请(专利权)人(译)	三星电子株式会社		
申请(专利权)人(译)	SAMSUNG ELECTRONICS CO.，LTD.		
当前申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
[标]发明人	KIM DONG GYU		
发明人	KIM, DONG-GYU		
IPC分类号	G02F1/1345 G02F1/1362 G02F1/1343 G09G3/36		
CPC分类号	G09G3/3677 G02F1/134336 G02F1/1345 G02F1/136286 G09G2310/02		
代理机构(译)	DR.威猛和合作伙伴		
优先权	1020050096540 2005-10-13 KR		
其他公开文献	EP1775624A1		
外部链接	Espacenet		

摘要(译)

液晶显示器包括多个像素，包括像素电极和连接到像素电极并以矩阵排列的开关器件，连接到开关器件并彼此分离的多对第一和第二栅极线，以及多个像素电极和多个像素数据线连接到开关器件并与第一和第二栅极线交叉，其中多条数据线连接成使得每对数据线中的两条数据线的端部彼此连接。

FIG.1