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(54) **Liquid crystal display device and driving method therefor**

Flüssigkristallanzeigevorrichtung und deren Ansteuerungsverfahren

Dispositif d'affichage à cristaux liquides et son procédé de commande

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## Description

[0001] The present invention relates to a liquid crystal display and a driving method thereof.

[0002] An LCD includes a pair of panels provided with field generating electrodes and a liquid crystal (LC) layer having dielectric anisotropy, which is disposed between the two panels. The field generating electrodes generally include a plurality of pixel electrodes connected to switching elements such as thin film transistors (TFTs) to be supplied with data voltages and a common electrode covering an entire surface of a panel and supplied with a common voltage. A pair of field generating electrodes that generate the electric field in cooperation with each other and a liquid crystal disposed therebetween form so called a liquid crystal capacitor.

[0003] The LCD applies the voltages to the field generating electrodes to generate electric field to the liquid crystal layer, and the strength of the electric field can be controlled by adjusting the voltage across the liquid crystal capacitor. Since the electric field determines the orientation of liquid crystal molecules and the molecular orientation determines the transmittance of light passing through the liquid crystal layer, the light transmittance is adjusted by controlling the applied voltages, thereby obtaining desired images.

[0004] In order to prevent image deterioration due to long-time application of the unidirectional electric field, etc., polarity of the data voltages with respect to the common voltage is reversed every frame, every row, or every dot.

[0005] Among various inversion types, a dot inversion reversing the polarity every given number of pixels reduces vertical crosstalk or vertical flickering due to kickback voltage, thereby improving image quality. However, the polarity inversion of the data voltages flowing in each data line may require complicated driving scheme and may cause signal delay. Although the signal delay may be reduced by employing low resistivity metal, etc., it may complicate the manufacturing process and increase the production cost.

[0006] On the contrary, a column inversion reverses the voltage polarity every given number of pixel columns. Since the column inversion does not reverse the polarity of the data voltages applied to each data line during one frame, the issue of the signal delay is remarkably reduced.

[0007] However, the column inversion is inferior to the dot inversion in the vertical crosstalk and the vertical flickering, etc.

[0008] US 2002/0080295 describes a TPT liquid crystal display with three gates for each pixel and complex arrangement of pixels of different colours. In embodiments, the pixels of alternative rows are on different sides of data lines.

[0009] US 6,327,008 describes driving a liquid crystal display with different patterns of inversion.

[0010] A liquid crystal display according to claim 1 is provided.

[0011] The switching elements in each pixel row group may be connected to the data lines at the same side of the pixels.

[0012] The data voltages supplied to adjacent pixel row groups through each data line may have opposite polarities.

[0013] The data voltages supplied to each pixel row group through each data line may have the same polarity.

[0014] Each pixel row group may include first and second pixel rows and the gate-on voltage for the first pixel row of each pixel row group may have a duration different from the gate-on voltage for the second pixel row of each pixel row group.

[0015] The transmission of the gate-on voltage for at least a pixel row of each pixel row group may start after a predetermined time from termination of a previous transmission of the gate-on voltage for any other pixel rows of each pixel row group.

[0016] The liquid crystal display may further include: a signal controller providing image data; and a data driver converting the image data from the signal controller to the data voltages and applying the data voltages to the data lines, wherein the signal controller outputs at least twice a packet of the image data for at least one pixel row of each pixel row group to the data driver.

[0017] The liquid crystal display may further include: a gate driver outputting the gate-on voltage via a plurality of output terminals under the control of the signal controller, wherein the output terminals include first terminals connected to the gate lines and a second terminal disconnected from the gate lines and the output of the gate-on voltage is performed in sequence via the first terminals and the second terminal.

[0018] In another aspect there is provided a method of driving a liquid crystal display according to claim 9.

[0019] The present invention will become more apparent by describing embodiments thereof in detail with reference to the accompanying drawing in which:

Fig. 1 is a block diagram of an LCD according to an embodiment of the present invention;

Fig. 2 is an equivalent circuit diagram of a pixel of an LCD according to an embodiment of the present invention;

Figs. 3 to 5B illustrate arrangements of the switching elements of the pixels according to a comparative example (Figure 3) and embodiments of the present invention (Figures 4 and 5);

Figs. 6A to 6C show waveforms of a black data voltage applied to a data line of a normally white mode LCD;

Figs. 7A and 7B illustrate gate signals in an LCD according to embodiments of the present invention; and

Fig. 8 is an equivalent circuit diagram of a pixel, gate lines and data lines.

**[0020]** The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Like numerals refer to like elements throughout.

**[0021]** In the drawings, the thickness of layers and regions are exaggerated for clarity. Like numerals refer to like elements throughout. It will be understood that when an element such as a layer, region or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements present.

**[0022]** Then, liquid crystal displays according to embodiments of the present invention will be described with reference to the accompanying drawings.

**[0023]** Fig. 1 is a block diagram of an LCD according to an embodiment of the present invention, and Fig. 2 is an equivalent circuit diagram of a pixel of an LCD according to an embodiment of the present invention.

**[0024]** Referring to Fig. 1, an LCD according to an embodiment includes a LC panel assembly 300, a gate driver 400 and a data driver 500 that are connected to the panel assembly 300, a gray voltage generator 800 connected to the data driver 500, and a signal controller 600 controlling the above elements.

**[0025]** Referring to Fig. 1, the panel assembly 300 includes a plurality of display signal lines  $G_1-G_n$  and  $D_1-D_m$  and a plurality of pixels connected thereto and arranged substantially in a matrix. In a structural view shown in Fig. 2, the panel assembly 300 includes lower and upper panels 100 and 200 and a LC layer 3 interposed therebetween.

**[0026]** The display signal lines  $G_1-G_n$  and  $D_1-D_m$  are disposed on the lower panel 100 and include a plurality of gate lines  $G_1-G_n$  transmitting gate signals (also referred to as "scanning signals"), and a plurality of data lines  $D_1-D_m$  transmitting data signals. The gate lines  $G_1-G_n$  extend substantially in a row direction and substantially parallel to each other, while the data lines  $D_1-D_m$  extend substantially in a column direction and substantially parallel to each other.

**[0027]** Each pixel includes a switching element Q connected to the signal lines  $G_1-G_n$  and  $D_1-D_m$ , and a LC capacitor  $C_{LC}$  and a storage capacitor  $C_{ST}$  that are connected to the switching element Q. If unnecessary, the storage capacitor  $C_{ST}$  may be omitted.

**[0028]** The switching element Q including a TFT is provided on the lower panel 100 and has three terminals: a control terminal connected to one of the gate lines  $G_1-G_n$ ; an input terminal connected to one of the data lines  $D_1-D_m$ ; and an output terminal connected to both the LC capacitor  $C_{LC}$  and the storage capacitor  $C_{ST}$ .

**[0029]** The LC capacitor  $C_{LC}$  includes a pixel electrode 190 provided on the lower panel 100 and a common electrode 270 provided on an upper panel 200 as two terminals. The LC layer 3 disposed between the two electrodes 190 and 270 functions as dielectric of the LC capacitor  $C_{LC}$ . The pixel electrode 190 is connected to the switching element Q, and the common electrode 270 is supplied with a common voltage  $V_{com}$  and covers an entire surface of the upper panel 200. Unlike Fig. 2, the common electrode 270 may be provided on the lower panel 100, and both electrodes 190 and 270 may have shapes of bars or stripes.

**[0030]** The storage capacitor  $C_{ST}$  is an auxiliary capacitor for the LC capacitor  $C_{LC}$ . The storage capacitor  $C_{ST}$  includes the pixel electrode 190 and a separate signal line, which is provided on the lower panel 100, overlaps the pixel electrode 190 via an insulator, and is supplied with a predetermined voltage such as the common voltage  $V_{com}$ . Alternatively, the storage capacitor  $C_{ST}$  includes the pixel electrode 190 and an adjacent gate line called a previous gate line, which overlaps the pixel electrode 190 via an insulator.

**[0031]** In a planar view, a pixel is assigned to an area enclosed by a pair of adjacent gate lines  $G_1-G_n$  and a pair of adjacent data lines  $D_1-D_m$ , and the switching elements Q of each pixel is connected to one of upper and lower gate lines  $G_1-G_n$  and to one of left and right data lines  $D_1-D_m$ .

**[0032]** Figs. 3 to 5B illustrate arrangements of the switching elements of the pixels according to a comparative example (Figure 3) and embodiments of the present invention (Figures 4 and 5), i.e., the connections between the switching elements denoted by x and the gate lines  $G_1-G_n$  and the data lines  $D_1-D_m$ .

**[0033]** Figs. 3 to 5B show arrangements wherein the switching elements of all the pixels are connected to lower gate lines  $G_1-G_n$ . On the contrary, all the switching elements may be connected to upper gate lines  $G_1-G_n$ . All the switching elements in each pixel row are connected to the data lines  $D_1-D_m$  disposed at the same side. For example, all the switching elements in the uppermost pixel row shown in Fig. 3 are connected to the left data lines  $D_1-D_m$ , while all the switching elements in the lowermost pixel row shown in Fig. 4A are connected to the right data lines  $D_1-D_m$ .

**[0034]** The arrangement shown in Fig. 3 alternates the positions of the switching elements every row. In other words, the switching elements in adjacent pixel rows are connected to opposite-sided data lines  $D_1-D_m$ . Among four pixel rows shown in Fig. 3, the switching elements in the uppermost and the third pixel rows are connected to the left data lines  $D_1-D_m$ , while the switching elements in the second and the lowermost pixel rows are connected to the right data lines  $D_1-D_m$ .

**[0035]** In the arrangements shown in Figs. 4A and 4B, the positions of the switching elements alternate every two pixel rows. In other words, the switching elements in a group of pixel rows (referred to as "pixel row group" hereinafter) including successive two pixel rows occupy the same position, and the switching elements in successive two pixel row

groups occupy opposite positions. It is noted that the uppermost or the lowermost pixel row in a LC panel assembly 300 may solely form a pixel row group. Among four pixel rows shown in Fig. 4A, the switching elements in the first pixel row group including upper two pixel rows are connected to the left data lines  $D_1$ - $D_m$ , while the switching elements in the second pixel row group including lower two pixel rows are connected to the right data lines  $D_1$ - $D_m$ . Among four pixel rows shown in Fig. 4B, the switching elements in the first pixel row group including the uppermost pixel row and those in the third pixel row group including the lowermost pixel row are connected to the left data lines  $D_1$ - $D_m$ , while the switching elements in the second pixel row group including the second and the third pixel row groups are connected to the right data lines  $D_1$ - $D_m$ .

**[0036]** The positions of the switching elements may alternate every three pixel rows. To summarize, the arrangements of the switching elements shown in Figs. 3 to 4B make the switching elements in each pixel row group, which includes at least a pixel row, occupy the same position and make the switching elements in adjacent pixel row groups occupy the opposite positions.

**[0037]** In the arrangement shown in Fig. 5A, the switching elements in a predetermined number of successive pixel rows (referred to as "pixel row set" hereinafter) 101 and 102 form the same configuration as that shown in Fig. 3, and the arrangements in two adjacent pixel row sets 101 and 102 are symmetrical with respect to a boundary of the pixel row sets 101 and 102. In the arrangement shown in Fig. 5B, the switching elements in each pixel row set 103 and 104 form the same configuration as that shown in Fig. 4A, and the arrangements in two adjacent pixel row sets 101 and 102 are also symmetrical with respect to a boundary of the pixel row sets 101 and 102. The number of the pixel row sets is at least one, and the arrangement having only one pixel row set is equal to the arrangement shown in Fig. 3 or 4A.

**[0038]** For color display, each pixel uniquely represents one of primary colors (i.e., spatial division) or each pixel sequentially represents the primary colors in turn (i.e., temporal division) such that spatial or temporal sum of the primary colors are recognized as a desired color. An example of a set of the primary colors includes red, green, and blue colors. Fig. 2 shows an example of the spatial division that each pixel includes a color filter 230 representing one of the primary colors in an area of the upper panel 200 facing the pixel electrode 190. Alternatively, the color filter 230 is provided on or under the pixel electrode 190 on the lower panel 100.

**[0039]** The red, green and blue color filters 230 shown in Figs. 3 to 5B in a pixel row are arranged in sequence and a pixel column includes the pixels representing only one color, thereby forming a striped arrangement.

**[0040]** One or more polarizers (not shown) are attached to at least one of the panels 100 and 200.

**[0041]** Referring to Fig. 1 again, the gray voltage generator 800 generates two sets of a plurality of gray voltages related to the transmittance of the pixels. The gray voltages in one set have a positive polarity with respect to the common voltage  $V_{com}$ , while those in the other set have a negative polarity with respect to the common voltage  $V_{com}$ .

**[0042]** The gate driver 400 is connected to the gate lines  $G_1$ - $G_n$  of the panel assembly 300 and synthesizes the gate-on voltage  $V_{on}$  and the gate-off voltage  $V_{off}$  from an external device to generate gate signals for application to the gate lines  $G_1$ - $G_n$ .

**[0043]** The data driver 500 is connected to the data lines  $D_1$ - $D_m$  of the panel assembly 300 and applies data voltages, which are selected from the gray voltages supplied from the gray voltage generator 800, to the data lines  $D_1$ - $D_m$ .

**[0044]** The drivers 400 and 500 may include at least one integrated circuit (IC) chip mounted on the panel assembly 300 or on a flexible printed circuit (FPC) film in a tape carrier package (TCP) type, which are attached to the LC panel assembly 300. Alternately, the drivers 400 and 500 may be integrated into the panel assembly 300 along with the display signal lines  $G_1$ - $G_n$  and  $D_1$ - $D_m$  and the TFT switching elements Q.

**[0045]** The signal controller 600 controls the gate driver 400 and the gate driver 500.

**[0046]** Now, the operation of the above-described LCD will be described in detail.

**[0047]** The signal controller 600 is supplied with input image signals R, G and B and input control signals controlling the display thereof such as a vertical synchronization signal  $V_{sync}$ , a horizontal synchronization signal  $H_{sync}$ , a main clock MCLK, and a data enable signal DE, from an external graphics controller (not shown). After generating gate control signals CONT1 and data control signals CONT2 and processing the image signals R, G and B suitable for the operation of the panel assembly 300 on the basis of the input control signals and the input image signals R, G and B, the signal controller 600 transmits the gate control signals CONT1 to the gate driver 400, and the processed image signals DAT and the data control signals CONT2 to the data driver 500.

**[0048]** The gate control signals CONT1 include a scanning start signal STV for instructing to start scanning and at least a clock signal for controlling the output time of the gate-on voltage  $V_{on}$ . The gate control signals CONT1 may further include an output enable signal OE for defining the duration of the gate-on voltage  $V_{on}$ .

**[0049]** The data control signals CONT2 include a horizontal synchronization start signal STH for informing of start of data transmission for a group of pixels, a load signal LOAD for instructing to apply the data voltages to the data lines  $D_1$ - $D_m$ , and a data clock signal HCLK. The data control signal CONT2 may further include an inversion signal RVS for reversing the polarity of the data voltages (with respect to the common voltage  $V_{com}$ ).

**[0050]** Responsive to the data control signals CONT2 from the signal controller 600, the data driver 500 receives a packet of the image data DAT for the group of pixels from the signal controller 600, converts the image data DAT into

analog data voltages selected from the gray voltages supplied from the gray voltage generator 800, and applies the data voltages to the data lines  $D_1$ - $D_m$ .

**[0051]** The gate driver 400 applies the gate-on voltage  $V_{on}$  to the gate line  $G_1$ - $G_n$  in response to the gate control signals CONT1 from the signal controller 600, thereby turning on the switching elements Q connected thereto. The data

voltages applied to the data lines  $D_1$ - $D_m$  are supplied to the pixels through the activated switching elements Q.

**[0052]** The difference between the data voltage and the common voltage  $V_{com}$  is represented as a voltage across the LC capacitor  $C_{LC}$ , which is referred to as a pixel voltage. The LC molecules in the LC capacitor  $C_{LC}$  have orientations depending on the magnitude of the pixel voltage, and the molecular orientations determine the polarization of light passing through the LC layer 3. The polarizer(s) converts the light polarization into the light transmittance.

**[0053]** By repeating this procedure by a unit of the horizontal period (which is denoted by "1H" and equal to one period of the horizontal synchronization signal Hsync and the data enable signal DE), all gate lines  $G_1$ - $G_n$  are sequentially supplied with the gate-on voltage  $V_{on}$  during a frame, thereby applying the data voltages to all pixels. When the next frame starts after finishing one frame, the inversion control signal RVS applied to the data driver 500 is controlled such that the polarity of the data voltages is reversed (which is referred to as "frame inversion").

**[0054]** Other than the frame inversion, the data driver 500 varies the polarity of the data voltages flowing in each data line during one frame, thereby varying the polarity of the pixel voltages. Since the connections between the pixels and the data lines  $D_1$ - $D_m$  are various as shown in Figs. 3 and 5B, the polarity inversion pattern generated by the data driver 500 is different from that of the pixel voltages appearing on the panel assembly 300. Hereinafter, the polarity inversion of the data driver 500 is referred to as "driver inversion" and the polarity inversion appearing on the panel assembly 300 is referred to as "apparent inversion."

**[0055]** Now, several inversion types according to embodiments of the present invention will be described in detail with reference to Fig. 3 to 5B.

**[0056]** Figs. 3 to 4B show cases that the driver inversion is a column inversion that the polarity of the data voltages in each data line is fixed and the polarities of the data voltages in adjacent data lines are opposite.

**[0057]** Referring to Fig. 3, the apparent inversion is  $1 \times 1$  dot inversion since the positions of the switching elements are interchanged every pixel row. Similarly, the apparent inversion shown in Fig. 4A and 4B are  $2 \times 1$  dot inversion since the positions of the switching elements are interchanged every two pixel rows.

**[0058]** The driver inversion employed in the arrangements shown in Figs. 5A and 5B is a kind of dot inversion, where the data voltages in adjacent data lines have opposite polarities and the data voltages in each data line are reversed every pixel row set. (Since a pixel row set form a section on a screen of the panel assembly 300, the above-described inversion is referred to as "sectional inversion" hereinafter and the term "section" will be used in the same meaning as the term "pixel row set.") That is, two data voltages applied to each data line have the same polarity if they will be applied to the pixels belonging to a pixel row set. However, the data voltages have opposite polarities if they will be applied to the pixels belonging to adjacent pixel rows. Therefore, when the number of the pixel rows in a pixel row set is equal to M, the above-described inversion is said to be  $M \times 1$  dot inversion.

**[0059]** Under such a driver inversion, the apparent inversion shown in Fig. 5A becomes  $1 \times 1$  dot inversion like Fig. 3, while the apparent inversion shown in Fig. 5B becomes  $2 \times 1$  dot inversion like Fig. 4A.

**[0060]** The dot-type apparent inversion disperses the difference in the luminance due to the kickback voltages between the positive-polarity pixel voltages and the negative-polarity pixel voltages to thereby reduce vertical line defect.

**[0061]** Figs. 6A to 6C show waveforms of a black data voltage applied to a data line of a normally white mode LCD. Figs. 6A and 6B are related to a sectional driver inversion with four sections and one section, respectively, and Fig. 6C is related to a  $1 \times 1$  dot-type driver inversion.

**[0062]** The polarity of the data voltage shown in Fig. 6A is reversed four times in a frame, while the polarity for a  $1 \times 1$  dot-type driver inversion shown in Fig. 6C is reversed once in a frame. The inversion shown in Fig. 6B is equivalent to a column inversion since the number of the section is only one and the polarity of the data voltages is not reversed during a frame.

**[0063]** When the data voltages flowing in a data line in a frame have opposite polarities as describe above, a vertical crosstalk is reduced. In particular, the inversion approaches to a normal dot inversion as the number of the sections increases, thereby increasingly reducing the vertical crosstalk. However, the increase of the number of the sections may cause the increase of signal delay and power consumption and thus the number of the sections is preferably in a range of 1-32. The reason for the reduction of the crosstalk will be described later in detail.

**[0064]** In the meantime, the section inversion may cause the delay of data voltages for the first pixel row in each section since the polarity of the data voltages for the first pixel row is opposite to the polarity of the data voltages for a previous pixel row. Such a signal delay may be reduced by increasing the charging time of the data voltages for the first pixel row of each section or by starting the charging of the data voltages for the first pixel row of each section after delaying the charging for a time until the voltages of the data lines are greater than a predetermined level. Since the application of the data voltages in an LCD is performed in a unit of one horizontal period and the increased charging time or the delay time may be multiples of one horizontal period.

[0065] Figs. 7A and 7B illustrate gate signals in an LCD according to embodiments of the present invention. In Figs. 7A and 7B, the gate signal for the first pixel row of a section is denoted as  $g_j$ .

[0066] Referring to Fig. 7A, the gate signal  $g_j$  applied to a gate line connected to the first pixel row has an increased duration of the gate-on voltage  $V_{on}$ , for example, for a time twice a conventional one. For this purpose, the signal controller 600 may double the duration of a pulse of a clock signal, which is supplied to the gate driver 400 for controlling the output time of the gate-on voltage  $V_{on}$ , for the gate signal  $g_j$ .

[0067] Referring to Fig 7B, the gate-on voltage of the gate signal  $g_j$  for the first pixel row is delayed for a time, for example, for 1H, such that the charging into the pixels starts when the voltages of the data lines reach a predetermined level.

[0068] In order to delay the gate signal  $g_j$  for 1H, the  $l$ -th gate signal outputted from the gate driver 400 is abandoned and the  $(l+1)$ -th gate signal is applied to the  $l$ -th gate line  $G_l$ . This is obtained by connecting the  $(l+1)$ -th output terminal of the gate driver 400 to the gate line  $G_l$  and connecting the  $l$ -th output terminal of the gate driver 400 to none.

[0069] In the examples shown in Figs. 7A and 7B, the signal controller 600 provides the data driver 500 with the image data for the first pixel rows of the sections twice in a successive manner such that the data lines hold the data voltages for the first pixel row of each section for 2H. However, since such a successive provision is not required for the first pixel row of the first section, total number of the pixel rows to be twice provided with the image data is equal to  $(k-1)$  when the number of the sections is equal to  $k$ . The signal controller 600 may include  $(k-1)$  line memories for storing the image data for such pixel rows.

[0070] Alternatively, an external device such as a scaler for transmitting the image data from an external signal source to the signal controller 600 may include  $(k-1)$  line memories.

[0071] The additional time or the delay time of the gate-on voltage  $V_{on}$  may be varied to 2H, etc., depending on the delay level of the data voltages.

[0072] As described above, the section inversion applied to the LCD reduces the vertical crosstalk, which will be described in detail.

[0073] Generally, the vertical crosstalk is generated by the voltage variation of pixel electrodes due to the parasitic capacitance between the pixel electrodes and data lines adjacent thereto or due to the leakage current of turned-off switching transistors.

[0074] Referring to Fig. 8, a voltage variation of a pixel electrode due to the parasitic capacitance between the pixel electrode and data line is described in detail.

[0075] Fig. 8 is an equivalent circuit diagram of a pixel, gate lines and data lines.

[0076] Referring to Fig. 8, a pixel electrode  $P_x$  is connected to a gate line  $G_j$  and a data line  $D_j$  through a transistor  $Q$ . Parasitic capacitors  $C_{DP1}$  and  $C_{DP2}$  are formed between the pixel electrode  $P_x$  and two data lines  $D_j$  and  $D_{j+1}$  adjacent thereto. The capacitors and their capacitances are denoted as the same reference characters.

[0077] A voltage variation  $\Delta V$  of the pixel electrode  $P_x$  due to the parasitic capacitances  $C_{DP1}$  and  $C_{DP2}$  between the pixel electrode  $P_x$  and the data line  $D_j$  and  $D_{j+1}$  is given by:

$$\Delta V = \frac{C_{DP1}(V1 - V1') + C_{DP2}(V2 - V2')}{C_{LC} + C_{ST} + C_{GS} + C_{DP1} + C_{DP2}}, \quad (1)$$

where  $V1$  and  $V2$  denote voltages of the data lines  $D_j$  and  $D_{j+1}$  when the pixel electrode  $P_x$  are charged, respectively,  $V1'$  and  $V2'$  denote voltages of the data lines  $D_j$  and  $D_{j+1}$  after the pixel electrode  $P_x$  are charged, respectively,  $C_{GS}$  denotes parasitic capacitance between gate and source of the transistor  $Q$ ,  $C_{LC}$  denotes liquid crystal capacitance, and  $C_{ST}$  denotes storage capacitance.

[0078] It is assumed that the LCD is subjected to a column inversion and that the data voltages in the data lines  $D_j$  and  $D_{j+1}$  represent the same gray.

[0079] Since  $(V2 - V_{com}) = - (V1 - V_{com})$  and  $(V2' - V_{com}) = - (V1' - V_{com})$ , it is satisfied that  $(V2 - V2') = - (V1 - V1')$ . Accordingly, Equation 1 is expressed as:

$$\Delta V = \frac{\Delta C_{DP}(V1 - V1')}{C_{LC} + C_{ST} + C_{GS} + C_{DP1} + C_{DP2}}, \quad (2)$$

where  $\Delta C_{DP} = C_{DP1} - C_{DP2}$ .

[0080] In the meantime, the voltage variation  $\Delta V$  due to the leakage current is given by:

$$\Delta V = \frac{I_{\text{off}} \times t}{C_{\text{LC}} + C_{\text{ST}} + C_{\text{GS}} + C_{\text{DP1}} + C_{\text{DP2}}},$$

5 where  $t$  is a time for applying data voltages to the data line  $D_j$ , which is different from the voltage charged in the pixel electrode  $P_x$ , and  $I_{\text{off}}$  is a leakage current between the pixel electrode  $P_x$  and the data line  $D_j$ . The leakage current  $I_{\text{off}}$  is positive or negative depending on the sign of the voltage difference between the pixel electrode  $P_x$  and the data line  $D_j$ .

10 **[0081]** According to the embodiments of the present invention, the polarity of the data voltages is reversed every section. Therefore, the voltage difference between the data line  $D_j$  and the pixel electrode  $P_x$  alternates between positive and negative, and thus the voltage variation due to the parasitic capacitance between the pixel electrode and the data line alternates between negative and positive to be cancelled. In addition, the alternating voltage difference alternates the leakage current  $I_{\text{off}}$  between positive and negative to be also cancelled. Accordingly, the polarity inversion of the data voltages exceedingly reduces the voltage variation  $\Delta V$  of the pixel electrode  $P_x$ , thereby greatly reducing the vertical crosstalk.

15 **[0082]** The above-described arrangements of the switching elements of the pixels realize an  $N \times 1$  dot-type apparent inversion for a given column-type driver inversion. The column-type driver inversion diversifies materials available for the data lines and thus it is easy to find a material suitable for simplifying the manufacturing process. In addition, the charging time for the data voltages into the pixels is increased to improve the response time of the LCD, and the width of the data lines can be reduced to increase the aperture ratio since the signal delay is insignificant. Furthermore, the increase of the variation of the contact resistance between the data lines and other devices may not cause significant signal delay that may generate vertical line defect, and the increase of the resistance of the data lines due to repair of the data lines may not cause a significant problem. Moreover, the loss of the data voltage due to the signal delay is decreased to reduce the power consumption, thereby reducing the heat dissipation of driving devices.

20 **[0083]** In addition, the section inversion with appropriately defined sections significantly reduces the vertical crosstalk to improve the image quality of the LCD.

25 **[0084]** Although preferred embodiments of the present invention have been described in detail hereinabove, it should be clearly understood that many variations and/or modifications of the basic inventive concepts herein taught which may appear to those skilled in the present art will still fall within the scope of the present invention, as defined in the appended claims.

## Claims

35 1. A liquid crystal display (300) comprising:

a plurality of pixels arranged in a matrix having rows extending in a row direction and columns extending in a column direction, each pixel including a switching element, the pixels being arranged as a plurality of pixel row groups, each pixel row group including a plurality of pixel rows ;

40 a plurality of gate lines extending in the row direction, the gate lines being connected to the switching elements for transmitting a gate-on voltage for turning on the switching elements; and

a plurality of data lines extending in the column direction and being connected to the switching elements for transmitting data voltages, wherein the pixels are enclosed by adjacent gate lines and data lines, the switching element of each pixel being connected to one of the upper and lower gate lines around the pixel and to one of the left and right data lines, **characterized in that** the switching elements of the pixels in pixel row groups are connected to the data lines at opposite sides of the pixels compared with the switching elements of the pixels in adjacent pixel row groups; and

45 further comprising a data driver for supplying the data voltages to the data lines and a gate driver (400) arranged to delay or increase the duration of the transmission of the gate-on voltage for the first pixel row of each pixel row group compared with other pixel rows of the same pixel row group.

50 2. The liquid crystal display of claim 1, wherein the switching elements in each pixel row group are connected to the data lines at the same side of the pixels.

55 3. The liquid crystal display of claim 2, wherein the data driver is (500) arranged to supply the data voltages to adjacent pixel row groups through each  $\Delta V$  line with opposite polarities.

4. The liquid crystal display of claim 2, wherein the data driver is (500) arranged to supply the data voltages to each

pixel row group through each data line with the same polarity.

5 5. The liquid crystal display of claim 2, 3 or 4, wherein the gate driver (400) is arranged to generate the gate-on voltage for the first pixel row of each pixel row group with a duration different from the gate-on voltage for the second pixel row of each pixel row group.

10 6. The liquid crystal display of any of claims 2 to 5 wherein the gate driver is arranged to start the transmission of the gate-on voltage for at least a first pixel row of each pixel row group after a predetermined time delay from termination of a previous transmission of the gate-on voltage for any other pixel rows of each pixel row group.

7. The liquid crystal display of any preceding claim, further comprising:

15 a signal controller (600) providing image data; wherein the data driver (500) converts the image data from the signal controller to the data voltages and applies the data voltages to the data lines, and wherein the signal controller outputs at least twice a packet of the image data for at least one pixel row of each pixel row group to the data driver.

20 8. The liquid crystal display of claim 7:

25 wherein the gate driver is arranged to output the gate-on voltage via a plurality of output terminals under the control of the signal controller, wherein the output terminals include first terminals connected to the gate lines and a second terminal disconnected from the gate lines and the output of the gate-on voltage is performed in sequence via the first terminals and the second terminal.

30 9. A method of driving a liquid crystal display including a plurality of pixels arranged in a matrix having rows extending in a row direction and columns extending in a column direction, each pixel including a switching element, the pixels being arranged as a plurality of pixel row groups, each pixel row group including a plurality of pixel rows; a plurality of gate lines extending in the row direction, the gate lines being connected to the switching elements for transmitting a gate-on voltage for turning on the switching elements; and a plurality of data lines extending in the column direction connected to the switching elements for transmitting data voltages, wherein the pixels are enclosed by adjacent gate lines and data lines, the switching element of each pixel being connected to one of the upper and lower gate lines around the pixel and to one of the left and right data lines, the method comprising:

35 applying first data voltages to the data lines; applying a gate-on voltages to the gate lines connected a first one of to the pixel row groups to turn on the switching elements of the first pixel row group such that the first pixel row group is charged with the first data voltages; 40 applying second data voltages having polarity opposite the first voltages to the data lines; and applying a gate-on voltage to the gate lines connected to a second one of the pixel row groups to turn on the switching elements of the second pixel row group such that the second pixel row group is charged with the second data voltages, **characterized in that** the switching elements of the pixels in pixel row groups are connected to the data lines at opposite sides of the pixels compared with the switching elements of the pixels in adjacent pixel row groups; and 45 the gate-on voltage is delayed or increased in duration for the first pixel row of each pixel row group compared with the other pixel rows of the same pixel row group.

50 **Patentansprüche**

1. Flüssigkristallanzeige (300), umfassend:

55 eine Mehrzahl von Pixeln, die in einer Matrix mit Zeilen angeordnet sind, die sich in einer Zeilenrichtung erstrecken, und mit Spalten, die sich in einer Spaltenrichtung erstrecken, wobei jedes Pixel ein Schaltelement aufweist, wobei die Pixel als eine Mehrzahl von Pixelzeilengruppen angeordnet sind, wobei jede Pixelzeilengruppe eine Mehrzahl von Pixelzeilen aufweist; eine Mehrzahl von Gateleitungen, die sich in die Zeilenrichtung erstrecken, wobei die Gateleitungen mit den

Schaltelementen verbunden sind, um eine Gate-Einschaltspannung zum Einschalten der Schaltelemente zu übermitteln; und

eine Mehrzahl von Datenleitungen, die sich in die Spaltenrichtung erstrecken und mit den Schaltelementen verbunden sind, um Datenspannungen zu übermitteln, wobei die Pixel eingeschlossen sind durch benachbarte Gateleitungen und Datenleitungen, wobei das Schaltelement jedes Pixels mit einer der oberen und unteren Gateleitungen um das Pixel und mit einer der linken und rechten Datenleitungen verbunden ist, **dadurch gekennzeichnet, dass** die Schaltelemente der Pixel in Pixelzeilengruppen mit Datenleitungen auf entgegengesetzten Seiten der Pixel verbunden sind im Vergleich zu den Schaltelementen der Pixel in benachbarten Pixelzeilengruppen; und

ferner umfassend einen Datentreiber für die Zufuhr von Datenspannungen an die Datenleitungen und einen Gate-Treiber (400), der so angeordnet ist, dass er die Dauer der Übermittlung der Gate-Einschaltspannung für die erste Pixelzeile jeder Pixelzeilengruppe im Vergleich zu den anderen Pixelzeilen der gleichen Pixelzeilengruppe verzögert oder erhöht.

2. Flüssigkristallanzeige nach Anspruch 1, wobei die Schaltelemente in jeder Pixelzeilengruppe mit Datenleitungen auf der gleichen Seite der Pixel verbunden sind.

3. Flüssigkristallanzeige nach Anspruch 2, wobei der Datentreiber (500) so angeordnet ist, dass er die Datenspannungen durch jede Datenleitung mit entgegengesetzten Polaritäten benachbarten Pixelzeilengruppen zuführt.

4. Flüssigkristallanzeige nach Anspruch 2, wobei der Datentreiber (500) so angeordnet ist, dass er die Datenspannungen durch jede Datenleitung mit der gleichen Polarität jeder Pixelzeilengruppe zuführt.

5. Flüssigkristallanzeige nach Anspruch 2, 3 oder 4, wobei der Gate-Treiber (400) so angeordnet ist, dass er die Gate-Einschaltspannung für die erste Pixelzeile jeder Pixelzeilengruppe mit einer anderen Dauer erzeugt als die Gate-Einschaltspannung für die zweite Pixelzeile jeder Pixelzeilengruppe.

6. Flüssigkristallanzeige nach einem der Ansprüche 2 bis 5, wobei der Gate-Treiber so angeordnet ist, dass er die Übermittlung der Gate-Einschaltspannung für mindestens eine erste Pixelzeile jeder Pixelzeilengruppe nach einer vorbestimmten zeitlichen Verzögerung ab dem Ende einer vorherigen Übermittlung der Gate-Einschaltspannung für alle anderen Pixelzeilen jeder Pixelzeilengruppe startet.

7. Flüssigkristallanzeige nach einem der vorstehenden Ansprüche, ferner umfassend:

einen Signal-Controller (600), der Bilddaten bereitstellt; wobei der Datentreiber (500) die Bilddaten von dem Signal-Controller in die Datenspannungen umwandelt und die Datenspannungen den Datenleitungen zuführt; und wobei der Signal-Controller mindestens zweimal ein Paket der Bilddaten für die mindestens eine Pixelzeile jeder Pixelzeilengruppe an den Datentreiber ausgibt.

8. Flüssigkristallanzeige nach Anspruch 7:

wobei der Gate-Treiber so angeordnet ist, dass er die Gate-Einschaltspannung über eine Mehrzahl von Ausgangsanschlüssen unter der Steuerung des Signal-Controllers ausgibt;

wobei die Ausgangsanschlüsse erste Anschlüsse aufweisen, die mit den Gateleitungen verbunden sind, und einen zweiten Anschluss, der von den Gateleitungen getrennt ist, und wobei die Ausgabe der Gate-Einschaltspannung sequentiell über die ersten Anschlüsse und den zweiten Anschluss ausgeführt wird.

9. Verfahren zum Ansteuern einer Flüssigkristallanzeige, die folgendes aufweist:

eine Mehrzahl von Pixeln, die in einer Matrix mit Zeilen angeordnet sind, die sich in einer Zeilenrichtung erstrecken, und mit Spalten, die sich in einer Spaltenrichtung erstrecken, wobei jedes Pixel ein Schaltelement aufweist, wobei die Pixel als eine Mehrzahl von Pixelzeilengruppen angeordnet sind, wobei jede Pixelzeilengruppe eine Mehrzahl von Pixelzeilen aufweist; eine Mehrzahl von Gateleitungen, die sich in die Zeilenrichtung erstrecken, wobei die Gateleitungen mit den Schaltelementen verbunden sind, um eine Gate-Einschaltspannung zum Einschalten der Schaltelemente zu übermitteln; und eine Mehrzahl von Datenleitungen, die sich in die Spaltenrichtung erstrecken und mit den Schaltelementen verbunden sind, um Datenspannungen zu übermitteln, wobei die Pixel eingeschlossen sind durch benachbarte Gateleitungen und Datenleitungen, wobei das Schaltelement

jedes Pixels mit einer der oberen und unteren Gateleitungen um das Pixel und mit einer der linken und rechten Datenleitungen verbunden ist, wobei das Verfahren folgendes umfasst:

- 5 Zuführen erster Datenspannungen an die Datenleitungen;  
 Zuführen einer Gate-Einschaltspannung an die Gateleitungen, die mit einer ersten Gruppe der Pixelzeilen-  
 gruppen verbunden sind, um die Schaltelemente der ersten Pixelzeilengruppe einzuschalten, so dass die  
 erste Pixelzeilengruppe mit den ersten Datenspannungen geladen wird;  
 Zuführen zweiter Datenspannungen mit einer zu den ersten Spannungen entgegengesetzten Polarität an  
 10 die Datenleitungen; und  
 Zuführen einer Gate-Einschaltspannung an die Gateleitungen, die mit einer zweiten Gruppe der Pixelzei-  
 lengruppen verbunden sind, um die Schaltelemente der zweiten Pixelzeilengruppe einzuschalten, so dass  
 die erste Pixelzeilengruppe mit den zweiten Datenspannungen geladen wird;  
**dadurch gekennzeichnet, dass** die Schaltelemente der Pixel in den Pixelzeilengruppen mit den Daten-  
 15 leitungen auf entgegengesetzten Seiten der Pixel verbunden sind im Vergleich zu den Schaltelementen  
 der Pixel in benachbarten Pixelzeilengruppen; und  
 wobei die Dauer der Gate-Einschaltspannung für die erste Pixelzeile jeder Pixelzeilengruppe im Vergleich  
 zu den anderen Pixelzeilen der gleichen Pixelzeilengruppe verzögert oder erhöht wird.

## 20 Revendications

### 1. Dispositif à cristaux liquides (300), comprenant :

- 25 une pluralité de pixels disposés dans une matrice ayant des lignes s'étendant dans une direction de ligne et  
 de colonnes s'étendant dans une direction de colonne, chaque pixel comprenant un élément de commutation,  
 les pixels étant agencés comme une pluralité de groupes de lignes de pixels, chaque groupe de lignes de pixels  
 comprenant une pluralité de lignes de pixels ;  
 une pluralité de lignes de grilles s'étendant dans la direction de ligne, les lignes de grilles étant connectées aux  
 30 éléments de commutation pour transmettre une tension d'excitation de grille pour mettre en service les éléments  
 de commutation ; et  
 une pluralité de lignes de données s'étendant dans la direction de colonne et étant connectées aux éléments  
 de commutation pour transmettre des tensions de données, dans lequel les pixels sont entourés par des lignes  
 de grilles et des lignes de données adjacentes, l'élément de commutation de chaque pixel étant connecté à  
 35 l'une des lignes de grilles supérieure et inférieure autour du pixel et à l'une des lignes de données gauche et  
 droite, **caractérisé en ce que** les éléments de commutation des pixels dans des groupes de lignes de pixels  
 sont connectés aux lignes de données sur des côtés opposés des pixels par rapport aux éléments de commu-  
 tation des pixels dans des groupes de lignes de pixels adjacents ; et  
 comprenant en outre un pilote de données pour fournir des tensions de données aux lignes de données et un  
 40 pilote de grille (400) conçu pour retarder ou augmenter la durée de la transmission de la tension d'excitation  
 de grille pour la première ligne de pixels de chaque groupe de lignes de pixels par rapport à d'autres lignes de  
 pixels du même groupe de lignes de pixels.

### 2. Affichage à cristaux liquides selon la revendication 1, dans lequel les éléments de commutation dans chaque groupe 45 de lignes de pixels sont connectés aux lignes de données sur le même côté des pixels.

### 3. Affichage à cristaux liquides selon la revendication 2, dans lequel le pilote de données (500) est conçu pour fournir les tensions de données à des groupes de lignes de pixels adjacents à travers chaque ligne de données ayant des 50 polarités opposées.

### 4. Affichage à cristaux liquides selon la revendication 2, dans lequel le pilote de données (500) est conçu pour fournir les tensions de données à chaque groupe de lignes de pixels à travers chaque ligne de données ayant la même 55 polarité.

### 5. Affichage à cristaux liquides selon la revendication 2, 3 ou 4, dans lequel le pilote de grille (400) est conçu pour générer la tension d'excitation de grille pour la première ligne de pixels de chaque groupe de lignes de pixels avec une durée différente à partir de la tension d'excitation de grille pour la seconde ligne de pixels de chaque groupe de lignes de pixels.

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5 6. Affichage à cristaux liquides selon l'une quelconque des revendications 2 à 5, dans lequel le pilote de grille est agencé pour commencer la transmission de la tension d'excitation de grille pendant au moins une première ligne de pixels de chaque groupe de lignes de pixels après un temps de retard prédéterminé à partir de la fin d'une transmission précédente de la tension d'excitation de grille pour toutes les autres lignes de pixels de chaque groupe de lignes de pixels.

7. Affichage à cristaux liquides selon l'une quelconque des revendications précédentes, comprenant en outre :

10 un dispositif de commande de signal (600) fournissant des données d'image ; dans lequel le pilote de données (500) convertit les données d'image provenant du dispositif de commande de signal en tensions de données et applique les tensions de données aux lignes de données, et dans lequel le dispositif de commande de signal transmet au moins deux fois un paquet des données d'image pour au moins une ligne de pixels de chaque groupe de lignes de pixels pour le pilote de données.

15 8. Affichage à cristaux liquides selon la revendication 7 :

20 dans lequel le pilote de grille est conçu pour transmettre la tension d'excitation de grille par l'intermédiaire d'une pluralité de bornes de sortie sous la commande du dispositif de commande de signal, dans lequel les bornes de sortie comprennent des premières bornes connectées aux lignes de grilles et une seconde borne déconnectée des lignes de grilles et la sortie de la tension d'excitation de grille est effectuée en séquence par l'intermédiaire des premières bornes et de la seconde borne.

25 9. Procédé d'entraînement d'un affichage à cristaux liquides comprenant une pluralité de pixels disposés dans une matrice ayant des lignes s'étendant dans une direction de ligne et de colonnes s'étendant dans une direction de colonne, chaque pixel comprenant un élément de commutation, les pixels étant agencés comme une pluralité de groupes de lignes de pixels, chaque groupe de lignes de pixels comprenant une pluralité de lignes de pixels ; une pluralité de lignes de grilles s'étendant dans la direction de ligne, les lignes de grilles étant connectées aux éléments de commutation pour transmettre une tension d'excitation de grille pour mettre sous tension les éléments de commutation ; et une pluralité de lignes de données s'étendant dans la direction de colonne connectées aux éléments de commutation pour transmettre des tensions de données, dans lequel les pixels sont entourés par des lignes de grilles et des lignes de données adjacentes, l'élément de commutation de chaque pixel étant connecté à l'une des lignes de grilles supérieure et inférieure autour du pixel et à l'une des lignes de données gauche et droite, le procédé comprenant les étapes consistant à :

35 appliquer des premières tensions de données aux lignes de données ;  
appliquer des tensions d'excitation de grille aux lignes de grilles connectées à un premier des groupes de lignes de pixels pour mettre sous tension les éléments de commutation du premier groupe de lignes de pixels de sorte que le premier groupe de lignes de pixels soit chargé avec les premières tensions de données ;  
40 appliquer des secondes tensions de données ayant une polarité opposée aux premières tensions aux lignes de données ; et  
appliquer une tension d'excitation de grille aux lignes de grilles connectées à un second des groupes de lignes de pixels pour mettre sous tension les éléments de commutation du second groupe de lignes de pixels de sorte que le second groupe de lignes de pixels soit chargé avec les secondes tensions de données,  
45 **caractérisé en ce que** les éléments de commutation des pixels dans des groupes de lignes de pixels sont connectés aux lignes de données sur les côtés opposés des pixels par rapport aux éléments de commutation des pixels dans des groupes de lignes de pixels adjacents ; et  
la tension d'excitation de grille est retardée ou augmentée en durée pour la première ligne de pixels de chaque groupe de lignes de pixels par rapport aux autres lignes de pixels du même groupe de lignes de pixels.

FIG. 1

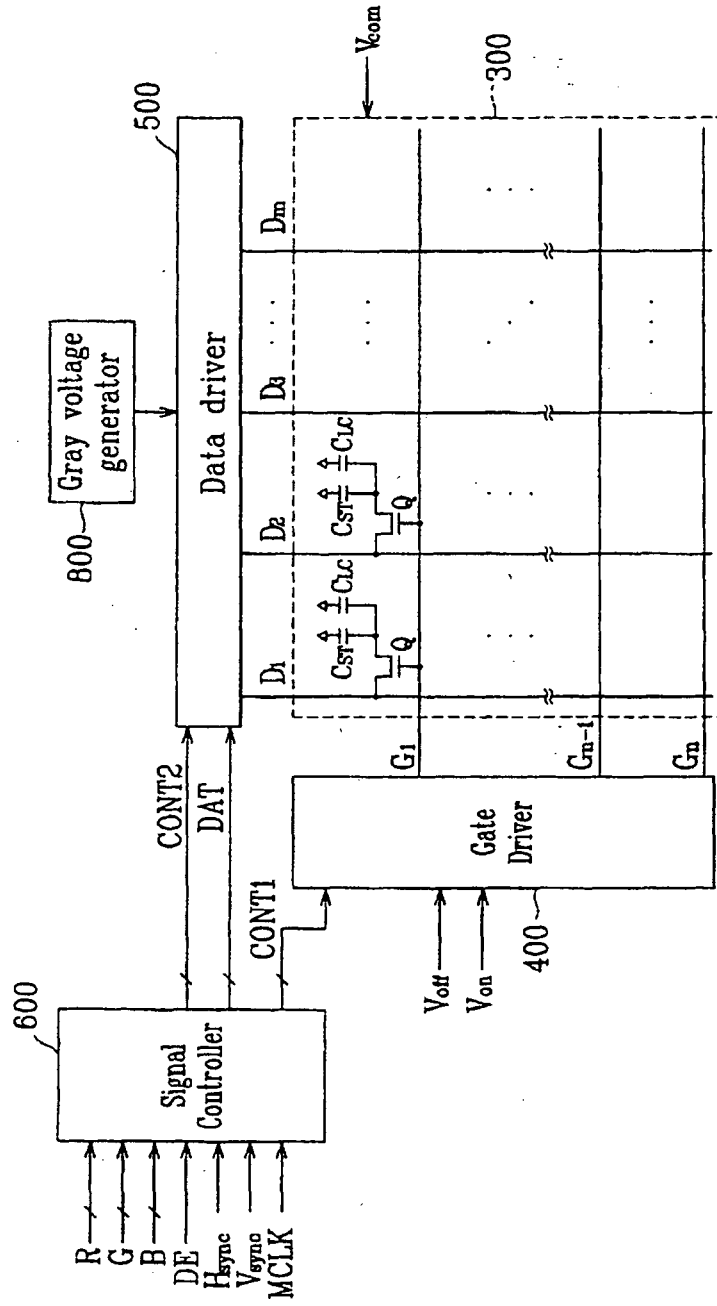


FIG. 2

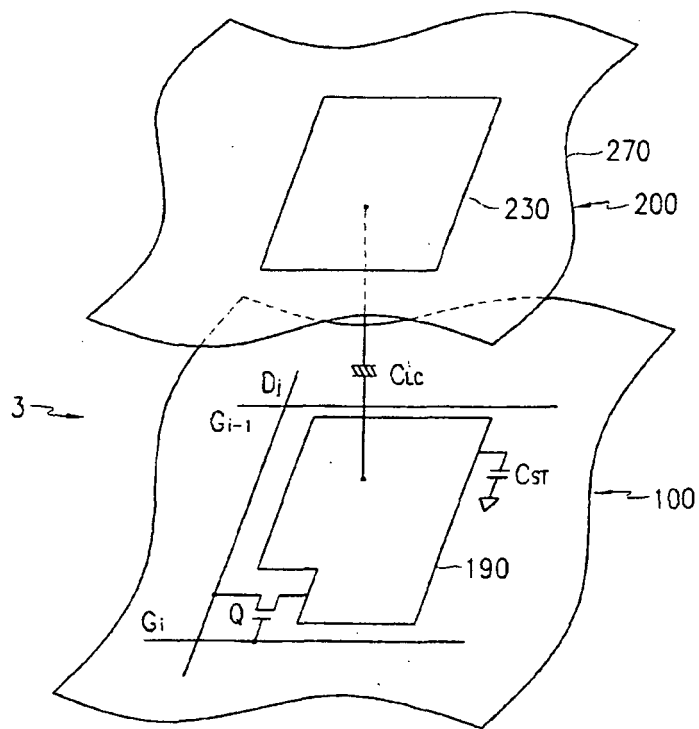


FIG. 3

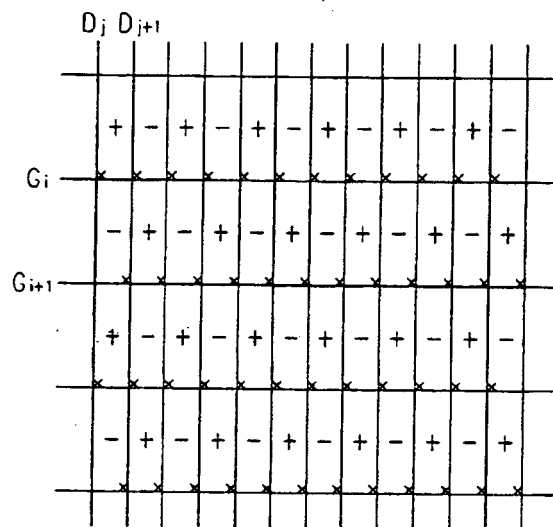


FIG. 4A

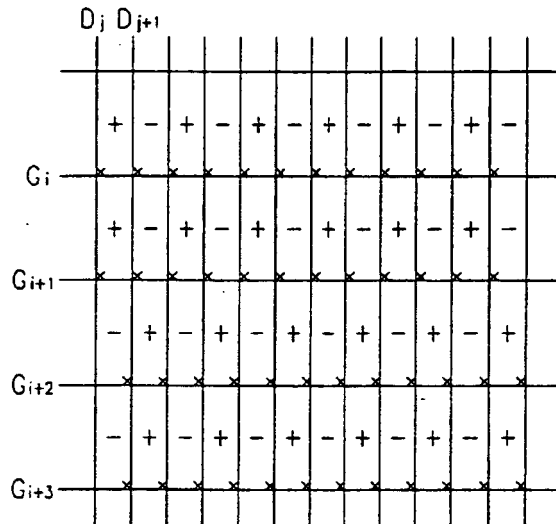


FIG. 4B

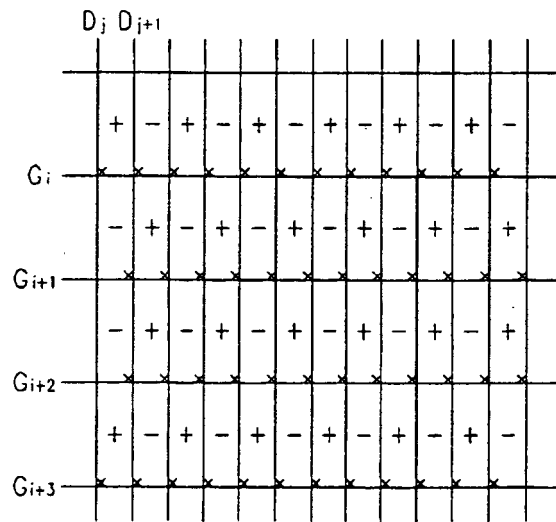


FIG. 5A

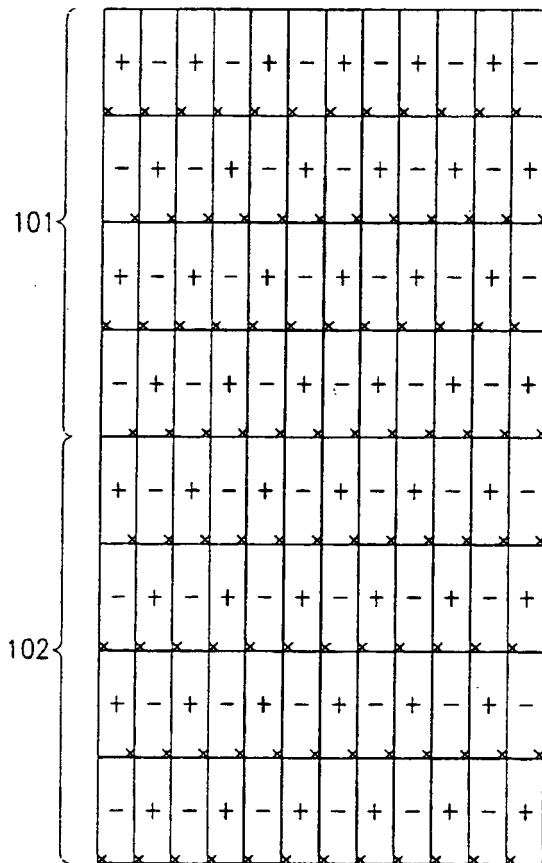


FIG. 5B

	+	-	+	-	+	-	+	-	+	-	+	-
	x	x	x	x	x	x	x	x	x	x	x	x
103<	+	-	+	-	+	-	+	-	+	-	+	-
	x	x	x	x	x	x	x	x	x	x	x	x
	-	+	-	+	-	+	-	+	-	+	-	+
	x	x	x	x	x	x	x	x	x	x	x	x
>	-	+	-	+	-	+	-	+	-	+	-	+
	x	x	x	x	x	x	x	x	x	x	x	x
	+	-	+	-	+	-	+	-	+	-	+	-
	x	x	x	x	x	x	x	x	x	x	x	x
104<	+	-	+	-	+	-	+	-	+	-	+	-
	x	x	x	x	x	x	x	x	x	x	x	x
	-	+	-	+	-	+	-	+	-	+	-	+
	x	x	x	x	x	x	x	x	x	x	x	x
	-	+	-	+	-	+	-	+	-	+	-	+
	x	x	x	x	x	x	x	x	x	x	x	x

FIG. 6A

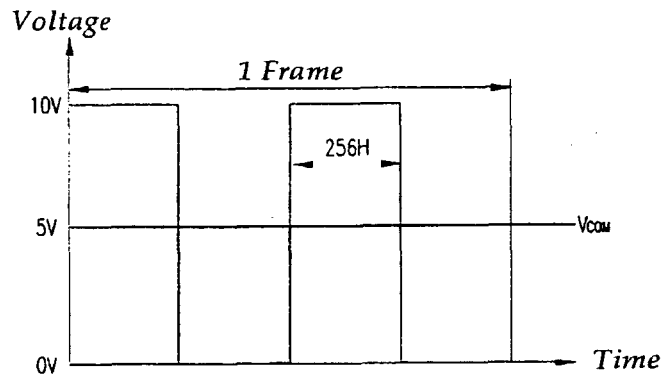


FIG. 6B

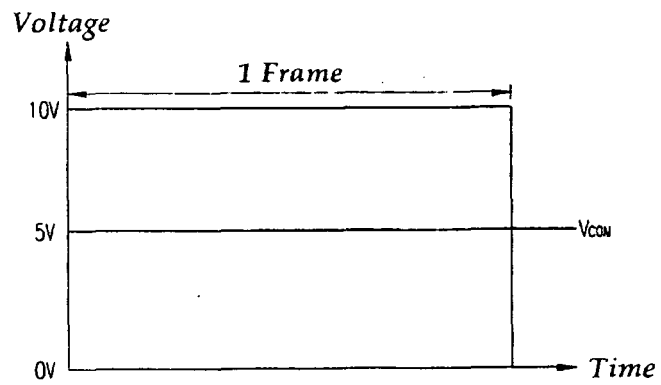


FIG. 6C

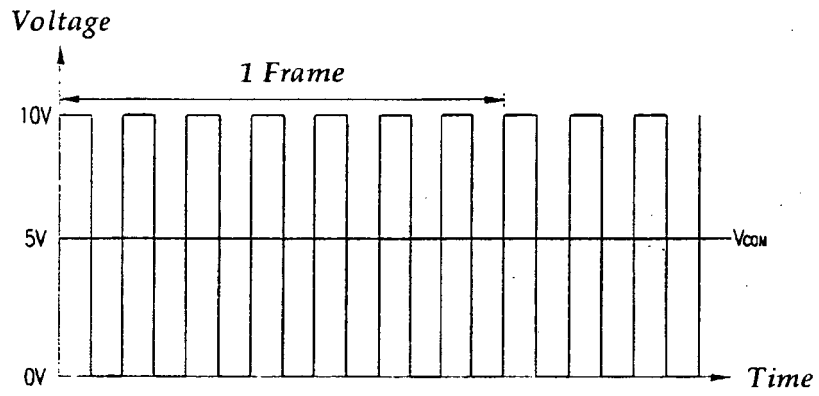


FIG. 8

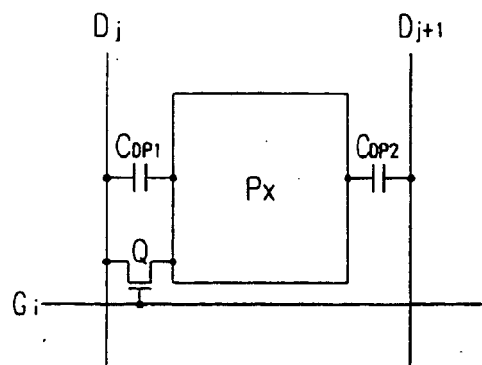


FIG. 7A

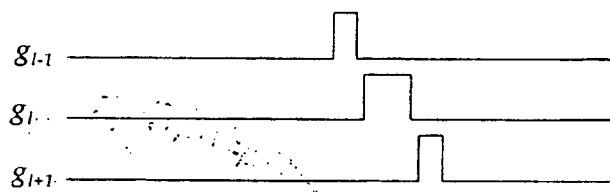
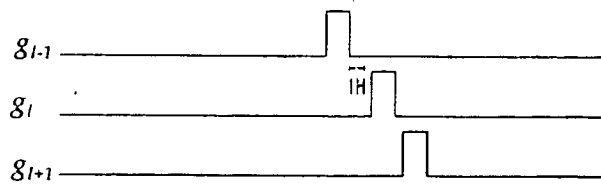


FIG. 7B



**REFERENCES CITED IN THE DESCRIPTION**

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[标]申请(专利权)人(译)	三星电子株式会社		
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摘要(译)

提供一种液晶显示器，包括：多个像素行组，每个像素行组包括至少一个像素行，所述像素行包括以矩阵排列并包括开关元件的多个像素；多条栅极线，连接到开关元件，并传输栅极导通电压，用于导通开关元件；多个数据线连接到开关元件并传输数据电压，其中相邻像素行组中的开关元件连接到相对侧的数据线。

$$\Delta V = \frac{C_{OP1}(V1 - V2) + C_{OP2}(V2 - V2)}{C_{IC} + C_{ST} + C_{GS} + C_{OP1} + C_{OP2}}$$