



(11) **EP 1 293 957 B1**

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:  
**27.02.2013 Bulletin 2013/09**

(51) Int Cl.:  
**G09G 3/36<sup>(2006.01)</sup>**

(21) Application number: **02019833.9**

(22) Date of filing: **06.09.2002**

(54) **Liquid crystal display, apparatus for driving a liquid crystal display, and method of generating gray voltages**

Flüssigkristallanzeige, Treiber für eine Flüssigkristallanzeige und Methode zur Erzeugung von Grauskala-Spannungen

Dispositif d'affichage à cristaux liquides, circuit d'excitation d'un dispositif d'affichage à cristaux liquides et méthode de génération de tensions de niveaux de gris

(84) Designated Contracting States:  
**DE FR GB NL**

(30) Priority: **07.09.2001 KR 2001055036**

(43) Date of publication of application:  
**19.03.2003 Bulletin 2003/12**

(73) Proprietor: **Samsung Display Co., Ltd.**  
**Yongin-City, Gyeonggi-Do (KR)**

(72) Inventors:  
• **Moon, Seung-Hwan**  
**Seocho-ku,**  
**Seoul (KR)**

• **Kang, Nam-Soo**  
**Ansan-city,**  
**Kyungki-do (KR)**

(74) Representative: **Modiano, Micaela Nadia**  
**Modiano Josif Pisanty & Staub Ltd**  
**Thierschstrasse 11**  
**80538 München (DE)**

(56) References cited:  
**WO-A-01/24154 JP-A- 10 301 538**  
**JP-A- 11 271 716 US-A- 6 075 507**

**EP 1 293 957 B1**

Note: Within nine months of the publication of the mention of the grant of the European patent in the European Patent Bulletin, any person may give notice to the European Patent Office of opposition to that patent, in accordance with the Implementing Regulations. Notice of opposition shall not be deemed to have been filed until the opposition fee has been paid. (Art. 99(1) European Patent Convention).

**Description****BACKGROUND OF THE INVENTION****(a) Field of the Invention**

[0001] The present invention relates to a liquid crystal display, an apparatus for driving a liquid crystal display, and a method of generating gray voltages for a liquid crystal display.

**(b) Description of the Related Art**

[0002] A typical liquid crystal display ("LCD") includes a pair of transparent glass substrates facing each other to define a narrow gap therebetween and a liquid crystal layer with dielectric anisotropy filled in the gap. A plurality of field-generating electrodes opposite each other are provided on the inner surfaces of the respective glass substrates. The field-generating electrodes are applied with voltages to generate an electric field in the liquid crystal layer. The LCD displays a desired image by controlling the voltages applied to the field-generating electrodes to adjust the transmittance of light passing through the liquid crystal layer.

[0003] Among the LCDs, a thin-film transistor ("TFT") LCD using TFTs as switching elements is widely used. A typical TFT LCD has a plurality of pixels arranged in a matrix, a plurality of gate lines extending in a row direction, and a plurality of data lines extending in a column direction. Each pixel includes a TFT connected to one of the gate lines and one of the data lines and a liquid crystal capacitor having a pixel electrode, a common electrode opposite thereto and a liquid crystal layer therebetween.

[0004] An electric field is generated by the voltage difference between the pixel electrodes and the common electrode, and the field direction is periodically inverted in order to prevent the deterioration of the characteristics of the LCD. If not, continuous application of unidirectional electric field causes precipitation of ionic impurities in the liquid crystal layer onto the pixel electrodes and the common electrode, thereby causing electro-chemical reactions in the electrodes. The field-direction is inverted by reversing the polarity of the voltages applied to the pixel electrodes (referred to as "data voltages" hereinafter) with respect to the voltage applied to the common electrodes (referred to as "common voltage" hereinafter).

[0005] The inversion in an LCD reverses the polarity of the data voltages by frame ("frame inversion"), by row ("line inversion"), and by pixel ("dot inversion").

[0006] The dot inversion includes one dot inversion and two-to-one dot inversion. The dot inversion reverses the polarities of the pixels adjacent to each other in the row direction. In the one dot inversion, the adjacent pixels in the column direction have the opposite polarities. On the other hand, the polarity of the pixels in the column direction is reversed every two rows in the two-to-one inversion.

[0007] In the dot inversion, voltages across liquid crystal capacitors (referred to as "pixel voltages") in a row are dropped when liquid crystal capacitors in the next row are charged, since parasitic capacitors between the liquid crystal capacitors in the adjacent rows generate AC currents. In particular, the voltage difference of the pixels in adjacent two rows with the same polarity in the two-to-one dot inversion induces brightness difference therebetween. For example, the upper one of two adjacent pixels with the same polarity in the column direction, when applied with the same data voltage, has larger pixel voltage than the lower one.

[0008] On the contrary, voltage delay caused by a slew rate decreases the pixel voltage of the upper pixel larger than the lower pixel. For example, it is assumed that the same data voltage is applied to the upper and the lower pixels. The data voltage flowing through the data line experiences RC delay when charging the upper pixel since the voltage difference from the previous data voltage with different polarity is large. That is, the large voltage difference makes it to take time to reach the expected value. However, the data voltage hardly experiences the RC delay when charging the lower pixel since the data voltages for the upper and the lower pixels are the same. Therefore, the pixel voltage of the upper pixel has a smaller value than the lower pixel.

[0009] WO O1124154 A discloses a liquid crystal display device in which correction voltages are supplied to power supply voltages to compensate alterations (e.g. the appearance of stripes in image portions) of the voltages applied for reducing parasitic capacitances between neighboring subpixels.

[0010] US-A-6075507 discloses a liquid crystal display device having less number of signal line drive circuits, where there is applied a dot inversion drive, and where a former stage pixel is subjected to modulation due to interpixel parasitic capacitance. More in detail, US-A-6075507 discloses to equalize an electric voltage of the former stage pixel being modulated as a latter stage pixel.

**SUMMARY OF THE INVENTION**

[0011] A liquid crystal display is provided, which includes: a plurality of gate lines transmitting gate signals; a plurality of data lines intersecting the plurality of gate lines and transmitting data voltages; and a plurality of pixel rows, each pixel row including a plurality of pixels, each of the plurality of pixels including a switching element connected to one of the plurality of gate lines and one of the plurality of data lines, wherein polarity of the data voltages supplied to the plurality of pixels are inverted by a pixel group including two or more pixel rows, and absolute values of the data voltages applied to one row of the pixel group with respect to a first predetermined voltage are greater than the absolute values of the data voltages applied to another row of the pixel group for the same grays.

[0012] It is preferable that the one pixel row is firstly or

lastly applied with the data voltages in the pixel group.

**[0013]** According to an embodiment of the present invention, the liquid crystal display further includes a gate driver for sequentially supplying a gate-on voltage to the plurality of gate lines to turning on the switching elements; a gray voltage generator generating a plurality of gray voltages, each gray voltage having at least two different values; and a data driver for selecting the plurality of gray voltages and supplying the selected gray voltages as the data voltages to the plurality of pixels via the turned on switching elements.

**[0014]** According to an embodiment of the present invention, the gray voltage generator includes a gray voltage producer generating the plurality of gray voltages based on a plurality of reference voltages including a first reference voltage; and a reference voltage producer, connected to the gray voltage producer, generating the first reference voltage with a value which varies depending on the number of the pixel rows in the pixel group to provide for the gray voltage producer.

**[0015]** According to an embodiment of the present invention, the reference voltage producer includes a pulse signal producer generating at least one pulse signal having a period depending on the number of the pixel rows in the pixel group; and a level adjuster adjusting a voltage level of the at least one pulse signal from the pulse signal producer to generate the first reference voltage.

**[0016]** According to an embodiment of the present invention, the at least one pulse signal includes a first pulse signal and a second pulse signal, the first and the second pulse signals are inverted signals of each other. The level adjuster includes an input voltage generator alternately switching the first and the second pulse signals and changing levels of the first and the second pulse signals to generate a first voltage, and a level changer changing the first voltage to generate the first reference voltage.

**[0017]** According to an embodiment of the present invention, the input voltage generator comprises a switch alternately switching the first and the second pulse signals and a plurality of resistors comprising a pair of first resistors connected in series between a second predetermined voltage and a third predetermined voltage and a pair of second resistors respectively connected to the first and the second pulse signals, the switch is connected to a first node between the first resistors and alternately connected to the second resistors, and the input voltage generator outputs a voltage of the first node.

**[0018]** It is preferable that the level changer includes an amplifier amplifying the first voltage, and a third resistor connected between the amplifier and the gray voltage producer. Furthermore, when the plurality of reference voltages further comprises a second reference voltage, the level changer preferably includes an inverter inverting an output of the amplifier with respect to a second predetermined voltage, a fourth resistor, connected between the inverter and the gray voltage producer, for providing the second reference voltage.

**[0019]** According to an embodiment of the present in-

vention, the gray voltage producer includes a plurality of fifth resistors for positive grays connected in series a plurality of sixth resistors for negative grays connected in series, one of the first and the second reference voltages are provided for a node between the fifth resistors, and the other of the first and the second reference voltages are provided for a node between the sixth resistors

**[0020]** According to an embodiment of the present invention, the pulse signal producer includes a D flip flop generating the first and the second pulse signals based on a clock signal for the gate driver. The pulse signal producer further comprises an OR gate ORing the first pulse signal and a start signal for the gate driver to provide a signal for the D flip flop as an input.

**[0021]** According to another embodiment of the present invention, the at least one pulse signal includes a first pulse signal and a second pulse signal, the first and the second pulse signals are inverted signals of each other, and the level adjuster includes a resistor connected to one of the first and the second pulse signals.

**[0022]** An apparatus for driving a liquid crystal display is provided, which includes: a gray voltage producer generating a plurality of positive gray voltages and a plurality of negative gray voltages based on a plurality of reference voltages including a first reference voltage for positive grays and a second reference voltages for negative grays; a pulse signal producer generating first and second pulse signals with inverted phases; and a level adjuster adjusting a voltage level of the first and the second pulse signals from the pulse signal producer to generate the first and the second reference voltages.

**[0023]** The level adjuster preferably includes a switch alternately switching the first and the second pulse signals; a pair of first resistors connected in series between a first predetermined voltage and a second predetermined voltage; a pair of second resistors respectively connected to the first and the second pulse signals, the switch connected to a node between the first resistors and alternately connected to the second resistors; a first amplifier, connected to the node, for amplifying a voltage of the node to produce the first reference voltage; and a second amplifier inverting an output of the amplifier with respect to a predetermined voltage to produce the second reference voltage.

**[0024]** A method for generating gray voltages with changing amplitudes for a liquid crystal display is provided, which includes: generating first and second pulse signals with inverted phases; periodically switching the first and the second pulse signals; changing levels of the first and the second pulse signals to generate a first voltage; amplifying the first voltage to produce a first reference voltage; inverting the first reference voltage with respect to a predetermined voltage to produce a second reference voltage; and generating a plurality of positive and negative gray voltages based on the first and the second reference voltages.

## BRIEF DESCRIPTION OF THE DRAWINGS

[0025] The above and other objects and advantages of the present invention will become more apparent by describing preferred embodiments thereof in detail with reference to the accompanying drawings in which:

FIG. 1 is a block diagram of an LCD according to an embodiment of the present invention;

FIG. 2 is a schematic diagram of an LCD according to an embodiment of the present invention;

FIG. 3 shows the polarities of pixel of an LCD according to an embodiment of the present invention;

FIG. 4 illustrates waveforms of signals suitable for an LCD according to an embodiment of the present invention;

FIG. 5 is a circuit diagram of a gray voltage generator according to an embodiment of the present invention;

FIG. 6 shows signals required for operations of a gray voltage generator according to an embodiment of the present invention; and

FIG. 7 is a circuit diagram of a gray voltage generator according to another embodiment of the present invention.

## DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0026] The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Like numerals refer to like elements throughout. Then, liquid crystal displays and methods of driving the same according to embodiments of the present invention will be described with reference to the drawings.

[0027] FIG. 1 is a block diagram of an LCD according to an embodiment of the present invention.

[0028] As shown in FIG. 1, an LCD includes an LCD panel assembly 300, a gate driver 400, a data driver 500, a signal controller 600, a driving voltage generator 700, and a gray voltage generator 800.

[0029] In view of circuit diagram, the panel assembly 300 includes a plurality of display signal lines  $G_1$ - $G_n$  and  $D_1$ - $D_m$  and a plurality of pixels connected thereto.

[0030] The display signal lines include a plurality of gate lines (or scanning signal lines)  $G_1$ - $G_n$  extending in a row direction, a plurality of data lines (or image signal lines)  $D_1$ - $D_m$  extending in a column direction to intersecting the gate lines  $G_1$ - $G_n$ . The gate lines  $G_1$ - $G_n$  transmit gate signals (or scanning signals), while the data lines  $D_1$ - $D_m$  transmit data signals (or image signals).

[0031] Each pixel is defined by one of the gate lines  $G_1$ - $G_n$  and one of the data lines  $D_1$ - $D_m$ , and includes a switching element Q connected to the display signal lines

$G_1$ - $G_n$  and  $D_1$ - $D_m$ , a liquid crystal capacitor  $C_{lc}$  and a storage capacitor  $C_{st}$  connected thereto. Each switching element Q has three terminals, a control terminal connected to one of the gate lines  $G_1$ - $G_n$ , an input terminal connected to one of the data lines  $D_1$ - $D_m$ , and an output terminal connected to the liquid crystal capacitor  $C_{lc}$  and the storage capacitor  $C_{st}$ . The liquid crystal capacitor  $C_{lc}$  is connected between the switching element Q and a common voltage (or a reference voltage)  $V_{com}$ , while the storage capacitor  $C_{st}$  is connected between the switching element Q and a predetermined voltage such as the common voltage  $V_{com}$ . Alternatively, the storage capacitor  $C_{st}$  is connected between the switching element Q and a gate line located just above the associated pixel (referred to as a "previous gate line" hereinafter). The former connection type of the storage capacitor  $C_{st}$  is called a "separate wire type", while the latter is called a "previous gate type".

[0032] FIG. 2 shows a schematic structural view of an LCD according to an embodiment of the present invention. For convenience, only one pixel is depicted in FIG. 2.

[0033] As shown in FIG. 2, a liquid crystal panel assembly 300 includes a lower panel 100, an upper panel 200 and a liquid crystal layer 3 interposed therebetween.

A plurality of gate lines  $G_{i-1}$  and  $G_i$ , a data line  $D_j$ , a switching element Q and a storage capacitor  $C_{st}$  is provided on the lower panel 100. A liquid crystal capacitor  $C_{lc}$  has two terminals respectively formed of a pixel electrode 190 on the lower panel 100 and a reference electrode 270 on the upper panel 200, and a dielectric formed of the liquid crystal layer 3 between the electrodes 190 and 270.

[0034] The pixel electrode 190 is connected to the switching element Q. The reference electrode 270 covers the entire surface of the upper panel 200 and is connected to the reference voltage  $V_{com}$ .

[0035] The liquid crystal molecules in the liquid crystal layer 3 changes their arrangement depending on the variation of electric field generated by the electrodes 190 and 270, thereby inducing the change of the polarization of light incident into the liquid crystal layer 3. The change of the polarization turns out to be the change of the light transmittance by polarizers (not shown).

[0036] In the meantime, a wire applied with the reference voltage  $V_{com}$  is preferably provided on the lower panel 100 and overlaps the pixel electrode 190 to form a storage capacitor  $C_{st}$  along with the pixel electrode 190. In case of the previous gate type, the pixel electrode 190 overlaps a previous gate line  $G_{i-1}$  via an insulator to form two terminals of a storage capacitor  $C_{st}$  along with the previous gate line  $G_{i-1}$ .

[0037] FIG. 2 shows a MOS transistor as an example of a switching element, and the MOS transistor is practically realized as a TFT with a channel layer made of amorphous silicon or polysilicon.

[0038] According to another embodiment, the reference electrode 270 is provided on the lower panel 100, and, in this case, the two electrodes 190 and 270 have stripe shapes parallel to each other.

**[0039]** In order to obtain color display, each pixel displays a color by providing red, green or blue color filter 230 in an area corresponding to the pixel electrode 190. In FIG. 2, the color filter 230 is provided in an appropriate area on the upper panel 100. Alternatively, the color filter 230 is provided on or under the pixel electrode 190 of the lower panel 100.

**[0040]** Referring again to FIG. 1, the driving voltage generator 700 generates a gate-on voltage  $V_{on}$  for turning on the switching elements Q, a gate-off voltage  $V_{off}$  for turning off the switching elements, and the common voltage  $V_{com}$ .

**[0041]** The gray voltage generator 800 generates a plurality of gray voltages associated with grays.

**[0042]** The gate driver 400, also referred to as the "scan driver", is connected to the gate lines  $G_1$ - $G_n$ , and applies gate signals to the appropriate gate lines  $G_1$ - $G_n$ . Each gate signal is formed of a combination of the gate-on voltage and the gate-off voltage,.

**[0043]** The data driver 500, also referred to as the "source driver", is connected to the data lines  $D_1$ - $D_m$ , and selects the gray signals from the gray voltage generator 800 to apply as the data signals to the appropriate data lines  $D_1$ - $D_m$ .

**[0044]** The signal controller 600 generates control signals for controlling the operations of the gate driver 400, the data driver 500, the driving voltage generator 700 and the gray voltage generator 800, to provide for appropriate devices.

**[0045]** Now, the operation of the LCD will be described in detail.

**[0046]** The signal controller 600 receives gray signals R, G and B and input control signals controlling the display of the gray signals R, G and B from an external source (not shown). The input control signals include a vertical synchronization signal  $V_{sync}$ , a horizontal synchronization signal  $H_{sync}$ , a main clock  $CLK$  and a data enable signal  $DE$ . After generating gate control signals  $GCS$  and data control signals  $DCS$  based on the input control signals and processing the gray signals suitable for the liquid crystal panel assembly 300, the signal controller 600 supplies the gate control signals to the gate driver 400 and the data control signals and the processed gray signals R', G' and B' to the data driver 500. The signal controller 600 also provides some control signals for the driving voltage generator 700 and the gray voltage generator.

**[0047]** The gate control signals  $GCS$  include a vertical synchronization start signal  $STV$  instructing to begin outputting gate-on pulses with the gate-on voltage  $V_{on}$ , a gate clock  $CPV$  controlling the timing of the gate on pulses, and a gate on enable signal  $OE$  determining the width of the gate on pulse. The data control signals  $DCS$  include a horizontal synchronization start signal  $STH$  instructing to begin inputting the gray signals, a load signal  $LOAD$  or  $TP$  instructing to apply the data voltages to appropriate data lines  $D_1$ - $D_m$ , a reverse control signal  $RVS$  for reversing the polarities of the data voltages, and a data

clock  $HCLK$ . Among the gate control signals  $GCS$ , the a vertical synchronization start signal  $STV$  and a gate clock  $CPV$  are provided for the gray voltage generator 800.

**[0048]** The gate driver 400 sequentially applies the gate on pulses to the gate lines  $G_1$ - $G_n$  based on the gate control signals  $GCS$ , thereby turning on the switching elements Q connected thereto. At the same time, the data driver 500 provides the gray voltages from the gray voltage generator 800, which correspond to the gray signals R', G' and B' for the pixels including the turned-on switching elements Q, to the appropriate data lines  $D_1$ - $D_m$  as the data voltages. The data voltages are applied to the corresponding pixels via the turned-on switching elements Q. In this way, all the pixels are applied with the data voltages by sequentially applying the gate on pulses to all the gate lines  $G_1$ - $G_n$  during one frame.

**[0049]** At this time, as shown in FIG. 3, the polarities of the data voltages with respect to the common voltage  $V_{com}$ , which are referred to as simply "the polarities of the data voltages" hereinafter, are subject to two-to-one inversion and frame inversion. That is, the polarities of the data voltages are inverted by every two rows and every column and by every frame.

**[0050]** In addition, between the two adjacent pixel rows with the same polarity, the absolute values of "the data voltages subtracted by the common voltage  $V_{com}$ " for the pixels in an upper row are larger than those in a lower

row for the same grays. That is,  $\left| d_{upper} - V_{com} \right| >$   
 $\left| d_{lower} - V_{com} \right|$ , where  $d_{upper}$  and  $d_{lower}$  are the data

voltages indicating the same gray for the upper and the lower pixel rows, respectively. The "absolute value of a voltage" in this specification means the absolute value of the voltage subtracted by the common voltage  $V_{com}$ .

**[0051]** According to an embodiment shown in FIG. 3, the data voltages for the  $i$ -th pixel row and the  $(i+1)$ -th pixel row have the same polarity, but have the different polarity from those for the  $(i-2)$ -th and the  $(i-1)$ -th pixel rows. For example, the data voltages for the  $j$ -th pixels in both the  $i$ -th and the  $(i+1)$ -th pixel rows have the positive polarity, while those in both the  $(i-2)$ -th and the  $(i-1)$ -th pixel rows have the negative polarity.

**[0052]** Let us assume that  $d_i$  and  $d_{i+1}$  are the data voltages for the  $j$ -th pixels in the  $i$ -th and the  $(i+1)$ -th pixel rows, respectively, and  $V_i$  and  $V_{i+1}$  are the pixel voltages, which are defined by the voltages across the liquid crystal capacitors  $C_{lc}$ , of the  $j$ -th pixels in the  $i$ -th and the  $(i+1)$ -th pixel rows, respectively. Furthermore, it is assumed that  $d_i$  and  $d_{i+1}$  represent the same gray, and thus

$$\left| d_i - V_{com} \right| > \left| d_{i+1} - V_{com} \right|.$$

**[0053]** As shown in FIG. 4, the data voltages  $d_i$  and  $d_{i+1}$  experience RC delay to become  $d'_i$  and  $d'_{i+1}$  during flowing through the data line  $D_j$ . The data voltage  $d_i$  ex-

periences much larger RC delay since it takes time to reach the expected value from the previous data voltage  $d_{i-1}$  with the negative polarity. On the contrary, the data voltage  $d_{i+1}$  hardly experiences the RC delay since the difference between the data voltages  $d_i$  and  $d_{i+1}$  is relatively small. Since the data voltage  $d_i$  has a larger absolute value than the data voltage  $d_{i+1}$ , the voltage drop of the pixel voltages  $V_i$  in the upper row due to the RC delay is compensated. In particular, if the difference between the values of the data voltages  $d_i$  and  $d_{i+1}$  is determined such that the pixel voltages  $V_i$  and  $V_{i+1}$  reach the same value, the voltage drop is fully compensated.

**[0054]** In the meantime, when the voltage drop due to the parasitic capacitance between the upper and the lower pixels is larger than the voltage drop due to the RC delay, the data voltage for the upper pixel has a smaller absolute value than that for the lower pixel for the same gray. However, in general, since the voltage drop due to the parasitic capacitance is smaller than the voltage drop due to the RC delay, the data voltage for the upper pixel is determined to have a larger absolute value than that for the lower pixel.

**[0055]** For this purpose, gray voltage generators according to embodiments of the present invention are designed to generate a plurality of gray voltages having different values for the same grays.

**[0056]** FIG. 5 is a circuit diagram of an exemplary gray voltage generator according to an embodiment of the present invention.

**[0057]** As shown in FIG. 5, a gray voltage generator according to an embodiment of the present invention includes a gray voltage producer 810, a pulse signal generator 820, and a reference voltage generator 830.

**[0058]** The gray voltage producer 810 includes a first array of resistors R1-R5 generating positive gray voltages VREF1-VREF5, and a second array of resistors R6-R10 generating negative gray voltages VREF6-VREF10. The first array of resistors R1-R5 and the second array of resistors R6-R10 are connected in series. The gray voltage producer 810 further includes a pair of resistors R12 and R11 connected in series between the first and the second arrays of the resistors R1-R10, a pair of diodes  $D_1$  and  $D_2$  connected in series between the pair of resistors R12 and R11, and a capacitor C1 connected between a node *RFC* between the diodes  $D_1$  and  $D_2$  and a predetermined voltage such as the ground voltage. The forward directions of the diodes  $D_1$  and  $D_2$  are a direction from the first array of resistors R1-R5 to the second array of resistors R6-R10.

**[0059]** The resistors R1-R5 in the first array are connected in series between a predetermined voltage  $V_{dd}$  from an external source and the resistor R12. The gray voltages VREF1-VREF4 are obtained from respective nodes between the resistors R1-R5, and the gray voltage VREF5 is obtained from a node between the resistors R5 and R12.

**[0060]** The resistors R6-R10 in the second array are connected in series between the resistor R11 and a pre-

determined voltage such as the ground voltage. The gray voltage VREF6 is obtained from a node between the resistors R11 and R6, and the gray voltages VREF7-VREF10 are obtained from respective nodes between the resistors R6-R10.

**[0061]** The pulse generator 820 includes a D flip-flop 822, an OR gate 824, a switch *SW*, a pair of resistors R15 and R16, and another pair of resistors R13 and R14.

**[0062]** The resistors R13 and R14 are connected in series between the predetermined voltage  $V_{dd}$  and another predetermined voltage such as a ground voltage.

**[0063]** The D flip-flop 822 has a clock terminal *CLK* connected to a gate clock *CPV* from the signal processor (600 in FIG. 1), a preset terminal *PRE* connected to a high level *HI*, a clear terminal *CLR* connected to the high level *HI*, an input terminal *D*, an output terminal *Q* and an inverted output terminal  $\bar{Q}$ .

**[0064]** The OR gate 824 has a first input terminal coupled to the inverted output terminal  $\bar{Q}$  of the D flip-flop 822, a second input terminal coupled to a horizontal synchronization start signal *STV*, and an output terminal connected to the input terminal *D* of the D flip-flop 822. The OR gate 824 may be substituted with dual diodes and resistors.

**[0065]** The resistor R15 is coupled between the output terminal *Q* of the D flip-flop 822 and the switch *SW*, while the resistor R16 is coupled between the inverted output terminal  $\bar{Q}$  of the D flip-flop 822 and the switch *SW*. The resistances of the resistors R15 and R16 are preferably different. The switch *SW* in turn is connected to a node N3 between the resistors R13 and R14 to alternately connect the output terminal *Q* and the inverted output terminal  $\bar{Q}$  to the node N3.

**[0066]** The reference voltage generator 830 includes a pair of amplifiers 832 and 834, two pairs of voltage gain resistors R17 and R18; R19 and R20, and another pair of resistors *RF* and *RG*.

**[0067]** Two supply terminals of each amplifier 832 or 834 are connected to the voltage  $V_{dd}$  and a predetermined voltage such as the ground voltage, respectively. The non-inverted input terminal of the amplifier 832 is connected to the node N3 between the resistors R13 and R14, while the non-inverted input terminal of the amplifier 834 is connected to a node *RFC* between the diodes  $D_1$  and  $D_2$ . The output terminal of the amplifier 832 is connected to a node N2 between the resistors R7 and R8 via the resistor *RG*, while the output terminal of the amplifier 834 is connected to a node N1 between the resistors R3 and R4 via the resistor *RF*.

**[0068]** One pair of voltage gain resistors R17 and R18 are connected in series between the output terminal of the amplifier 832 and a predetermined voltage such as the ground voltage, while the other pair of voltage gain resistors R19 and R20 are connected in series between the output terminals of the amplifiers 832 and 834. Respective inverted input terminals of the amplifiers 832 and 834 are connected to a node N4 between the resistors R17 and R18 and a node N5 between the resistors

R19 and R20, respectively.

**[0069]** Now, the operation of the gray voltage generator shown in FIG. 5 is described in detail with reference to FIG. 6, which is a timing chart of signals for operation of the gray voltage generator.

**[0070]** Upon receipt of the horizontal synchronization start signal *STV*, the OR gate 824 ORs the horizontal synchronization start signal *STV* and the output from the inverted output terminal  $\bar{Q}$  of the D flip-flop 822 to provide for the input terminal *D* of the D flip-flop 822.

**[0071]** Since the clear terminal *CLR* and the preset terminal *PRE* of the D flip-flop 822 are fixed to the high level *HI*, the D flip-flop 822 outputs a pair of pulse signals having a period twice the period of the gate clock *CPV* and inverted phases through the non-inverted output terminal *Q* and the inverted output terminal  $\bar{Q}$  in synchronization with the gate clock *CPV* entering into the clock terminal *CLK*. The output of the inverted output terminal  $\bar{Q}$  is ORed again with the horizontal synchronization start signal *STV* by the OR gate 824 to be returned to the input terminal *D*. The OR gate 824 makes the initial phase of the pulse signals to be the same for every frame.

**[0072]** The pair of pulse signals from the output terminal *Q* and the inverted output terminal  $\bar{Q}$  of the D flip-flop 822 are alternately coupled to the node N3 between the resistors R13 and R14 via the resistors R15 and R16 according to switching operations of the switch *SW*. The switching of the switch *SW* is preferably performed in the same period of the gate clock *CLK*. Since the resistances of the resistors R15 and R16 are different, the voltage value of the node N3 is changed periodically, particularly in the same period as that of the gate clock *CLK*. Accordingly, the input voltage  $V_{in}$  into the non-inverted terminal of the amplifier 832 periodically varies.

**[0073]** The amplifier 832 amplifies the input voltage  $V_{in}$  of the non-inverted input terminal by a voltage gain determined by the resistances of the voltage gain resistors R17 and R18 to generate an output voltage with the same phase as the input voltage  $V_{in}$ , and provides the output voltage for the node N2 between the resistors R7 and R8 via the resistor *RG* as a reference voltage of the negative gray voltages.

**[0074]** The output voltage of the amplifier 832 is also provided for the inverted input terminal of the amplifier 834 via the resistor R20. The amplifier 834 inverts the input voltage of its inverted input terminal with respect to the voltage of the node *RFC* or the half of the voltage  $V_{dd}$  to output an output voltage with reversed phase compared with the input voltage, and provides the output voltage for the node N1 between the resistors R3 and R4 via the resistor *RF* as a reference voltage of the positive gray voltages.

**[0075]** The resistances of the resistors R13, R14 and R17-R20 are determined in a manner that, when the switch *SW* is opened, the voltage *VREF8* of the node N2 between the resistors R7 and R8 has the center value among the negative gray voltages, while the voltage *VREF3* of the node N1 between the resistors R3 and R4

has the center value among the positive gray voltages.

**[0076]** As a result, the varying input voltage  $V_{in}$  changes the values of the reference voltages *VREF3* and *VREF8*, thereby causing the different values of the gray voltages *VREF1-VREF10*. The variation of the values of the reference voltages *VREF3* and *VREF8* can be adjusted by adjusting the resistances of the resistors *RF* and *RG*, and the resistors *RF* and *RG* are preferably variable resistors for this purpose.

**[0077]** FIG. 7 is a circuit diagram of an exemplary gray voltage generator according to another embodiment of the present invention.

**[0078]** As shown in FIG. 7, a gray voltage generator according to another embodiment of the present invention includes a gray voltage producer 810, a pulse generator 820, and a pair of variable resistors *RF* and *RG*.

**[0079]** The gray voltage producer 810 including a series of resistors R1-R10, a pair of resistors R12 and R11, a pair of diodes D1 and D2, and a capacitor C1 has substantially the same configuration as that shown in FIG. 5.

**[0080]** The pulse generator 820 includes a D flip flop 822 and an OR gate 824. Four terminals *PRE*, *CLR*, *CLK* and *I* of the D flip flop 822 are configured in substantially the same way as shown in FIG. 5, while two output terminals *Q* and  $\bar{Q}$  are directly connected to the resistors *RF* and *RG*, respectively, which in turn are connected to respective nodes N1 and N2 between the resistors R3 and R4 and between the resistors R7 and R8.

**[0081]** The values of reference voltages *VREF3* and *VREF8* are alternately changed by the output pulse signals from the output terminals of the D flip-flop 822, and the variation of the values are adjusted by adjusting the resistances of the variable resistors *RF* and *RG*.

**[0082]** The above embodiments described the gray voltages varying in the same period as the gate clock *CLK*, that is, varying every pixel row for two-to-one inversion. However, the present invention can be also applied to any types of two or more line inversions including two line inversion without column inversion, three line inversion without column inversion, three-to-one inversion, four-to-one inversion or the like. This can be obtained by changing the periods of the pulse signals from the pulse signal generator.

**[0083]** While the present invention has been described in detail with reference to the preferred embodiments, it is to be understood that the invention is not limited to the disclosed embodiments, but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the scope of the appended claims.

**[0084]** Where technical features mentioned in any claim are followed by reference signs, those reference signs have been included for the sole purpose of increasing the intelligibility of the claims and accordingly, such reference signs do not have any limiting effect on the scope of each element identified by way of example by such reference signs.

## Claims

1. An apparatus for driving a liquid crystal display and adapted to generate compensated data voltages for two-to-one dot inversion, three-to-one dot inversion or four-to-one dot inversion, comprising:

a gray voltage producer (810) arranged to generate a plurality of positive gray voltages (VREF1, VREF2, VREF4, VREF5) and a plurality of negative gray voltages (VREF6, VREF7, VREF9, VREF10) based on a plurality of reference voltages including a first reference voltage (VREF8) for positive grays (VREF1, VREF2, VREF4, VREF5) and a second reference voltage (VREF3) for negative grays (VREF6, VREF7, VREF9, VREF10);  
 a pulse signal producer (822, 824) arranged to generate first and second pulse signals (Q,  $\bar{Q}$ ) with inverted phases; and  
 a level adjuster arranged to adjust a voltage level of the first and the second pulse signals (Q,  $\bar{Q}$ ) from the pulse signal producer (822, 824) to generate the first and the second reference voltages (VREF8, VREF3), **characterized in that** the level adjuster comprises:

a pair of first resistors (R13, R14) connected in series between a first predetermined voltage (Vdd) and a second predetermined voltage and having a node (N3) connected there between, which node (N3) having a voltage (Vin);

a pair of second resistors (R15, R16) arranged to respectively connect to the first and the second pulse signals (Q,  $\bar{Q}$ );

a switch arranged to connect said node (N3) between the first pair of resistors (R13, R14) alternately to one resistor (R15, R16) or to the other of the second pair of resistors (R15, R16) so that the connected one resistor of the second pair of resistors (R15, R16) is coupled between the respective output for one of the first and second pulse signals (Q,  $\bar{Q}$ ) and said node (N3);

a first amplifier (832), receiving an input from the node (N3), for amplifying the voltage (Vin) of the node (N3) to produce the first reference voltage (VREF8); and

a second amplifier (834) arranged to invert an output of the first amplifier (832) with respect to a predetermined voltage (RFC, Vdd/2) to produce the second reference voltage (VREF3).

2. A method of driving a liquid crystal display and generating compensated data voltages for two-to-one dot inversion, three-to-one dot inversion or four-to-

one dot inversion, the method comprising:

generating first and second pulse signals (Q,  $\bar{Q}$ ) with inverted phases;

generating a first voltage (Vin) of a node (N3) between a first pair of resistors (R13, R14) connected in series between a first predetermined voltage (Vdd) and a second predetermined voltage by alternatively switching between either a connection of the node (N3) to the output of the first pulse signal via the first resistor of a second pair of resistors (R15) or a connection of the node (N3) to the output of the second pulse signal via the second resistor of the second pair of resistors (R16);

amplifying the first voltage (Vin) to produce a first reference voltage (VREF8);

inverting the first reference voltage (VREF8) with respect to a predetermined voltage (RFC, Vdd/2) to produce a second reference voltage (VREF3); and

generating a plurality of positive and negative gray voltages (VREF1, VREF2, VREF4, VREF5, VREF6, VREF7, VREF9, VREF10) based on the first and the second reference voltages (VREF8, VREF3).

3. A liquid crystal display comprising:

a plurality of gate lines (G1-Gn) transmitting gate signals;

a plurality of data lines (D1-Dm) intersecting the plurality of gate lines (G1-Gn) and transmitting data voltages; and

a plurality of pixel rows, each pixel row including a plurality of pixels, each of the plurality of pixels including a switching element (Q) connected to one of the plurality of gate lines (G1-Gn) and one of the plurality of data lines (D1-Dm), and means arranged to apply absolute values of the data voltages to one row of the pixel group with respect to a first predetermined voltage being greater than the absolute values of the data voltages applied to another row of the pixel group for the same grays, and further comprising the drive apparatus of claim 1

4. The liquid crystal display of claim 3, further comprising means arranged to invert polarity of the data voltages supplied to the plurality of pixels by a pixel group including two or more pixel rows.

5. The liquid crystal display of claims 3 and 4, wherein the one pixel row is the first to be applied with the data voltages in the pixel group.

6. The liquid crystal display of claims 3 and 4, wherein the one pixel row is the last to be applied with the

- data voltages in the pixel group.
7. The liquid crystal display of claims 3 and 4, further comprising:
- a gate driver (400) arranged to sequentially supply a gate-on voltage to the plurality of gate lines (G1-Gn) to turn on the switching elements;
- a gray voltage generator (800) arranged to generate a plurality of gray voltages, each gray voltage having at least two different values; and
- a data driver (500) arranged to select the plurality of gray voltages and to supply the selected gray voltages as the data voltages to the plurality of pixels via the turned on switching elements.
8. The liquid crystal display of claim 7, wherein the gray voltage generator (800) comprises:
- a reference voltage producer, connected to the gray voltage producer (810), adapted to generate the first reference voltage (VREF8) with a value which varies depending on the number of the pixel rows in the pixel group to provide for the gray voltage producer (810).
9. The liquid crystal display of claim 8, wherein the reference voltage producer comprises:
- a level adjuster arranged to adjust a voltage level of the at least one pulse signal from the pulse signal producer (822, 824) to generate the first reference voltage (VREF8).
10. The liquid crystal display of claim 8, wherein the level adjuster comprises an input voltage generator arranged to alternately switch between output of the first and the second pulse signal (Q,  $\bar{Q}$ ) and to change levels of the first and the second pulse signals (Q,  $\bar{Q}$ ) to generate a first voltage (Vin), and a level changer arranged to change the first voltage (Vin) to generate the first reference voltage (VREF8).
11. The liquid crystal display of claim 10, wherein the input voltage generator comprises
- a switch (SW) arranged to alternately switch between the outputs of the first and the second pulse signals (Q,  $\bar{Q}$ ) and
- a plurality of resistors comprising a pair of first resistors (R13, R14) connected in series between a second predetermined voltage and a third predetermined voltage and a pair of second resistors (R15, R16) respectively connected to the outputs of the first and the second pulse signals (Q,  $\bar{Q}$ ),
- the switch (SW) is connected to a first node (N3) between the first resistors (R13, R14) and alternately connected to one or other of the second resistors (R15, R16), and
- the input voltage generator is arranged to output a voltage (Vin) of the first node (N3).
12. The liquid crystal display of claim 11, wherein the level changer comprises:
- an amplifier (832) arranged to amplify the first voltage (Vin);
- a third resistor (RG) connected between the amplifier (832) and the gray voltage producer (810) to produce the first reference voltage (VREF8).
13. The liquid crystal display of claim 12, wherein the plurality of reference voltages further comprises a second reference voltage (VREF3), and the level changer comprises:
- an inverter (834, R19, R20, N51) arranged to invert an output of the amplifier (832) with respect to a second predetermined voltage (RFC);
- a fourth resistor (RF), connected between the inverter and the gray voltage producer (810), arranged to provide the second reference voltage (VREF3).
14. The liquid crystal display of claim 13, wherein the gray voltage producer (810) comprises a plurality of fifth resistors (R1-R5) for positive grays (VREF1, VREF2, VREF4, VREF5) connected in series a plurality of sixth resistors (R6-R10) for negative grays (VREF6, VREF7, VREF9, VREF10) connected in series, one of the first and the second reference voltages (VREF8, VREF3) are provided for a node (N1) between the fifth resistors (R1-R5), and the other of the first and the second reference voltages (VREF8, VREF3) are provided for a node (N2) between the sixth resistors (R6-R10)
15. The liquid crystal display of claim 13, wherein the third and the fourth resistors (RF, RG) comprise variable resistors.
16. The liquid crystal display of claim 10, wherein the pulse signal producer (822, 824) comprises a D flip flop (822) arranged to generate the first and the second pulse signals (Q,  $\bar{Q}$ ) based on a clock signal for the gate driver (400).
17. The liquid crystal display of claim 16, wherein the pulse signal producer (822, 824) further comprises an OR gate (824) arranged for ORing the first pulse signal (Q) and a start signal (STV) for the gate driver (400) to provide a signal for the D flip flop (822) as an input.
18. An apparatus for driving a liquid crystal display and adapted to generate compensated data voltages for

two-to-one dot inversion, three-to-one dot inversion or four-to-one dot inversion, comprising:

a gray voltage producer (810) arranged to generate a plurality of positive gray voltages (VREF1, REF2, REF4, VEERS) and a plurality of negative gray voltages (VREF6, VREF7, VREF9, VREF10) based on a plurality of reference voltages including a first reference voltages (VREF8) for positive grays (VREF1, VREF2, VREF4, VREF5) and a second reference voltage (VREF3) for negative grays (VREF6, VREF7, VREF9, VREF10); the gray voltage producer (810) including a first array of resistors (R1-R5) connected in series generating positive gray voltages (VREF1-VREF5), and a second array of resistors (R6-R10) connected in series generating negative gray voltages (VREF6-VREF10), and

a pulse signal producer (822, 824) arranged to generate first and second pulse signals (Q,  $\bar{Q}$ ) with inverted phases;

**characterized in that**

the gray voltage producer (810) further includes a pair of resistors (R12, R11) connected in series between the first and the second arrays of resistors (R1-R5, R6-R10), a pair of diodes (D1, D2) connected in series between said pair of resistors (R12, R11), and a capacitor (C1) connected between a node between the diodes (D1, D2) and a predetermined voltage such as the ground voltage, the forward directions of the diodes (D1, D2) being in the direction from the first array of resistors (R1-R5) to the second array of resistors (R6-R10),

the resistors in the first array (R1-R5) being connected in series between a predetermined voltage (Vdd) from an external source and one of the pair of resistors (R12), the plurality of positive gray voltages (VREF1-VREF5) being obtained from respective nodes between the resistors of the first array of resistors (R1-R5) and from a node between the first array of resistors and the one of the pair of resistors (R5 and R12),

the resistors in the second array (R6-R10) being connected in series between the other of the pair of resistors (R11) and a predetermined voltage such as the ground voltage, the plurality of negative gray voltages (VREF6 - VREF10) being obtained from a node between the other of the pair of resistors (R11) and the second array of resistors and from respective nodes between the resistors of the second array of resistors (R6-R10),

further **characterized by**

a level adjuster arranged to adjust a voltage level of the first and the second pulse signals (Q,  $\bar{Q}$ ) from the pulse signal producer (822, 824) to gen-

erate the first and the second reference voltages (VREF8, VREF3), which level adjuster comprises:

a pair of resistors (RF, RG) arranged so that each of the two output terminals for the first and second pulse signals (Q,  $\bar{Q}$ ) is directly connected to a respective one of the pair of resistors (RF, RG), one of the pair of resistors being in turn connected to a node (N1) within the first array of resistors (R1-R5), the other of the pair of resistors being in turn connected to a node (N2) within the second array of resistors (R6-R10).

19. The apparatus according to claim 18, wherein a resistor directly connected to one of the two output terminals for the first and second pulse signals (Q,  $\bar{Q}$ ) comprises a variable resistor.

**Patentansprüche**

1. Eine Vorrichtung zum Ansteuern einer Flüssigkristallanzeige und ausgebildet, um kompensierte Datenspannungen für Zwei-zu-Eins-Punkt-Inversion, Drei-zu-Eins-Punkt-Inversion oder Vier-zu-Eins-Punkt-Inversion zu erzeugen, die Folgendes umfasst:

einen Grauspannungserzeuger (810), der angeordnet ist, um eine Vielzahl positiver Grauspannungen (VREF1, VREF2, VREF4, VREF5) und eine Vielzahl negativer Grauspannungen (VREF6, VREF7, VREF9, VREF10) zu erzeugen, basierend auf einer Vielzahl von Referenzspannungen, die eine erste Referenzspannung (VREF8) für positive Graustufen (VREF1, VREF2, VREF4, VREF5) und eine zweite Referenzspannung (VREF3) für negative Graustufen (VREF6, VREF7, VREF9, VREF10) einschließen,

einen Impulssignalerzeuger (822, 824), der angeordnet ist, um erste und zweite Impulssignale (Q,  $\bar{Q}$ ) mit invertierten Phasen zu erzeugen, und einen Pegelregler, der angeordnet ist, um einen Spannungspegel der ersten und der zweiten Impulssignale (Q,  $\bar{Q}$ ) vom Impulssignalerzeuger (822, 824) anzupassen, um die erste und die zweite Referenzspannung (VREF8, VREF3) zu erzeugen, **dadurch gekennzeichnet, dass** der Pegelregler Folgendes umfasst:

ein Paar erster Widerstände (R13, R14), die seriell zwischen einer ersten vordefinierten Spannung (Vdd) und einer zweiten vordefinierten Spannung angeschlossen sind und einen dazwischen angeschlossenen Kno-

ten (N3) haben, wobei der Knoten (N3) eine Spannung ( $V_{in}$ ) hat,  
 ein Paar zweiter Widerstände (R15, R16), die angeordnet sind, um eine Verbindung zu dem ersten beziehungsweise dem zweiten Impulssignal ( $Q$ ,  $\bar{Q}$ ) herzustellen, einen Schalter, der angeordnet ist, um den Knoten (N3) zwischen dem ersten Paar von Widerständen (R13, R14) abwechselnd mit einem Widerstand (R15, R16) oder mit dem anderen des zweiten Paares von Widerständen (R15, R16) zu verbinden, so dass der angeschlossene eine Widerstand des zweiten Paares von Widerständen (R15, R16) zwischen dem jeweiligen Ausgang für eines der ersten und zweiten Impulssignale ( $Q$ ,  $\bar{Q}$ ) und dem Knoten (N3) gekoppelt wird, einen ersten Verstärker (832), der vom Knoten (N3) eine Eingabe empfängt, um die Spannung ( $V_{in}$ ) des Knotens (N3) zu verstärken, um die erste Referenzspannung (VREF8) zu erzeugen, und einen zweiten Verstärker (834), der angeordnet ist, um eine Ausgabe des ersten Verstärkers (832) mit Bezug auf eine vordefinierte Spannung (RFC,  $V_{dd}/2$ ) zu invertieren, um die zweite Referenzspannung (VREF3) zu erzeugen.

2. Ein Verfahren zum Ansteuern einer Flüssigkristallanzeige und zur Erzeugung kompensierter Daten- spannungen für Zwei-zu-Eins-Punkt-Inversion, Drei-zu-Eins-Punkt-Inversion oder Vier-zu-Eins-Punkt-Inversion, wobei das Verfahren Folgendes umfasst:

Erzeugung erster und zweiter Impulssignale ( $Q$ ,  $\bar{Q}$ ) mit invertierten Phasen,  
 Erzeugung einer ersten Spannung ( $V_{in}$ ) eines Knotens (N3) zwischen einem ersten Paar von Widerständen (R13, R14), die seriell zwischen einer ersten vordefinierten Spannung ( $V_{dd}$ ) und einer zweiten vordefinierten Spannung angeschlossen sind, durch alternatives Schalten zwischen entweder einer Verbindung des Knotens (N3) mit dem Ausgang des ersten Impulssignals über den ersten Widerstand eines zweiten Paares von Widerständen (R15) oder einer Verbindung des Knotens (N3) mit dem Ausgang des zweiten Impulssignals über den zweiten Widerstand des zweiten Paares von Widerständen (R16),  
 Verstärkung der ersten Spannung ( $V_{in}$ ), um eine erste Referenzspannung (VREF8) zu erzeugen,  
 Invertieren der ersten Referenzspannung (VREF8) mit Bezug auf eine vordefinierte Spannung (RFC,  $V_{dd}/2$ ), um eine zweite Referenz-

spannung (VREF3) zu erzeugen, und Erzeugen einer Vielzahl positiver und negativer Grauspannungen (VREF1, VREF2, VREF4, VREF5, VREF6, VREF7, VREF9, VREF10) auf der Grundlage der ersten und der zweiten Referenzspannung (VREF8, VREF3).

3. Eine Flüssigkristallanzeige, die Folgendes umfasst:

eine Vielzahl von Gate-Leitungen (G1-Gn), die Gate-Signale senden,  
 eine Vielzahl von Datenleitungen (D1-Dm), die die Vielzahl von Gate-Leitungen (G1-Gn) kreuzen und Datenspannungen senden, und eine Vielzahl von Pixelzeilen, wobei jede Pixelzeile eine Vielzahl von Pixeln einschließt, wobei jeder der Vielzahl von Pixeln ein Schaltelement ( $Q$ ) einschließt, das mit einer der Vielzahl von Gate-Leitungen (G1-Gn) und einer der Vielzahl von Datenleitungen (D1-Dm) verbunden ist, und Mittel, die angeordnet sind, um absolute Werte der Datenspannungen auf eine Zeile der Pixelgruppe anzuwenden, mit Bezug auf eine erste vordefinierte Spannung, die höher ist als die absoluten Werte der Datenspannungen, die auf eine andere Zeile der Pixelgruppe für dieselben Graustufen angewandt werden, und weiter die Ansteuervorrichtung gemäß Anspruch 1 umfassend.

4. Die Flüssigkristallanzeige gemäß Anspruch 3, die weiter Mittel umfasst, die angeordnet sind, um die Polarität der Datenspannungen zu invertieren, die der Vielzahl von Pixeln durch eine Pixelgruppe zugeführt werden, welche zwei oder mehr Pixelzeilen einschließt.

5. Die Flüssigkristallanzeige gemäß Anspruch 3 und 4, wobei die eine Pixelzeile die erste ist, auf die die Datenspannungen in der Pixelgruppe anzuwenden sind.

6. Die Flüssigkristallanzeige gemäß Anspruch 3 und 4, wobei die eine Pixelzeile die letzte ist, auf die die Datenspannungen in der Pixelgruppe anzuwenden sind.

7. Die Flüssigkristallanzeige gemäß Anspruch 3 und 4, die weiter Folgendes umfasst:

einen Gate-Treiber (400), der angeordnet ist, um der Vielzahl von Gate-Leitungen (G1-Gn) sequentiell eine Gate-ein-Spannung zuzuführen, um die Schaltelemente einzuschalten,  
 einen Grauspannungsgenerator (800), der angeordnet ist, um eine Vielzahl von Grauspannungen zu erzeugen, wobei jede Grauspannung mindestens zwei verschiedene Werte hat, und

- einen Datentreiber (500), der angeordnet ist, um die Vielzahl von Grauspannungen auszuwählen und um die ausgewählten Grauspannungen als Datenspannungen über die eingeschalteten Schaltelemente der Vielzahl von Pixeln zuzuführen. 5
- 8.** Die Flüssigkristallanzeige gemäß Anspruch 7, wobei der Grauspannungsgenerator (800) Folgendes umfasst: 10
- einen Referenzspannungserzeuger, der mit dem Grauspannungserzeuger (810) verbunden ist, ausgebildet, um die erste Referenzspannung (VREF8) mit einem Wert zu erzeugen, der in Abhängigkeit von der Anzahl der Pixelzeilen in der Pixelgruppe variiert, um den Grauspannungserzeuger (810) zur Verfügung zu stellen. 15
- 9.** Die Flüssigkristallanzeige gemäß Anspruch 8, worin der Referenzspannungserzeuger Folgendes umfasst: 20
- einen Pegelregler, der angeordnet ist, um einen Spannungspegel des mindestens einen Impulssignals vom Impulssignalerzeuger (822, 824) einzustellen, um die erste Referenzspannung (VREF8) zu erzeugen. 25
- 10.** Die Flüssigkristallanzeige gemäß Anspruch 8, worin der Pegelregler eine Eingangsspannungsquelle umfasst, die angeordnet ist, um abwechselnd zwischen der Ausgabe des ersten und des zweiten Impulssignals (Q,  $\bar{Q}$ ) zu schalten und um Pegel des ersten und des zweiten Impulssignals (Q,  $\bar{Q}$ ) zu ändern, um eine erste Spannung (Vin) zu erzeugen, und eine Pegeländerungsvorrichtung, die angeordnet ist, um die erste Spannung (Vin) zu ändern, um die erste Referenzspannung (VREF8) zu erzeugen. 30
- 11.** Die Flüssigkristallanzeige gemäß Anspruch 10, worin die Eingangsspannungsquelle Folgendes umfasst: 35
- einen Schalter (SW), der angeordnet ist, um abwechselnd zwischen den Ausgaben des ersten und des zweiten Impulssignals (Q,  $\bar{Q}$ ) zu schalten, und 40
- eine Vielzahl von Widerständen, die ein Paar erster Widerstände (R13, R14) umfassen, die seriell zwischen einer zweiten vordefinierten Spannung und einer dritten vordefinierten Spannung angeschlossen sind, und ein Paar zweiter Widerstände (R15, R16), jeweils mit den Ausgaben des ersten und des zweiten Impulssignals (Q,  $\bar{Q}$ ) verbunden, 45
- wobei der Schalter (SW) mit einem ersten Knoten (N3) zwischen den ersten Widerständen 50
- (R13, R14) verbunden ist und abwechselnd mit dem einen oder anderen der zweiten Widerstände (R15, R16) verbunden wird, und wobei die Eingangsspannungsquelle angeordnet ist, um eine Spannung (Vin) des ersten Knotens (N3) auszugeben. 55
- 12.** Die Flüssigkristallanzeige gemäß Anspruch 11, worin die Pegeländerungsvorrichtung Folgendes umfasst: 60
- einen Verstärker (832), der angeordnet ist, um die erste Spannung (Vin) zu verstärken, einen dritten Widerstand (RG), der zwischen dem Verstärker (832) und dem Grauspannungserzeuger (810) angeschlossen ist, um die erste Referenzspannung (VREF8) zu erzeugen. 65
- 13.** Die Flüssigkristallanzeige gemäß Anspruch 12, worin die Vielzahl von Referenzspannungen weiter eine zweite Referenzspannung (VREF3) umfasst und die Pegeländerungsvorrichtung Folgendes umfasst: 70
- einen Inverter (834, R19, R20, N5), der angeordnet ist, um eine Ausgabe des Verstärkers (832) mit Bezug auf eine zweite vordefinierte Spannung (RFC) zu invertieren, einen vierten Widerstand (RF), der zwischen dem Inverter und dem Grauspannungserzeuger (810) angeschlossen ist, angeordnet, um die zweite Referenzspannung (VREF3) bereitzustellen. 75
- 14.** Die Flüssigkristallanzeige gemäß Anspruch 13, worin der Grauspannungserzeuger (810) folgendes umfasst: eine Vielzahl fünfter Widerstände (R1-R5) für positive Graustufen (VREF1, VREF2, VREF4, VREF5), die seriell angeschlossen sind, und eine Vielzahl sechster Widerstände (R6-R10) für negative Graustufen (VREF6, VREF7, VREF9, VREF10), die seriell angeschlossen sind, wobei eine der ersten und der zweiten Referenzspannungen (VREF8, VREF3) für einen Knoten (N1) zwischen den fünften Widerständen (R1-R5) bereitgestellt wird, und die andere der ersten und der zweiten Referenzspannungen (VREF8, VREF3) für einen Knoten (N2) zwischen den sechsten Widerständen (R6-R10) bereitgestellt wird. 80
- 15.** Die Flüssigkristallanzeige gemäß Anspruch 13, worin die dritten und vierten Widerstände (RF, RG) veränderliche Widerstände umfassen. 85
- 16.** Die Flüssigkristallanzeige gemäß Anspruch 10, worin der Impulssignalerzeuger (822, 824) einen D-Flipflop (822) umfasst, der angeordnet ist, um die ersten und zweiten Impulssignale (Q,  $\bar{Q}$ ) anhand eines Taktsignals für den Gate-Treiber (400) zu erzeugen. 90

gen.

17. Die Flüssigkristallanzeige gemäß Anspruch 16, worin der Impulssignalerzeuger (822, 824) weiter ein ODER-Gatter (824) umfasst, das angeordnet ist, um das erste Impulssignal (Q) und ein Startsignal (STV) für den Gate-Treiber (400) mit ODER zu verknüpfen, um ein Signal für den D-Flipflop (822) als Eingabe zu liefern.

18. Eine Vorrichtung zum Ansteuern einer Flüssigkristallanzeige und ausgebildet, um kompensierte Datenspannungen für zwei-zu-Eins-Punkt-Inversion, Drei-zu-Eins-Punkt-Inversion oder Vier-zu-Eins-Punkt-Inversion zu erzeugen, die Folgendes umfasst:

einen Grauspannungserzeuger (810), der angeordnet ist, um eine Vielzahl positiver Grauspannungen (VREF1, VREF2, VREF4, VREF5) und eine Vielzahl negativer Grauspannungen (VREF6, VREF7, VREF9, VREF10) zu erzeugen, basierend auf einer Vielzahl von Referenzspannungen, die eine erste Referenzspannung (VREF8) für positive Graustufen (VREF1, VREF2, VREF4, VREF5) und eine zweite Referenzspannung (VREF3) für negative Graustufen (VREF6, VREF7, VREF9, VREF10) einschließen. wobei der Grauspannungserzeuger (810) eine erste Reihe seriell angeschlossener Widerstände (R1-R5) einschließt, die positive Grauspannungen (VREF1-VREF5) erzeugen, und eine zweite Reihe seriell angeschlossener Widerstände (R6-R10), die negative Grauspannungen (VREF6-VREF10) erzeugen, und einen Impulssignalerzeuger (822, 824), der angeordnet ist, um erste und zweite Impulssignale (Q,  $\bar{Q}$ ) mit invertierten Phasen zu erzeugen, **dadurch gekennzeichnet, dass**

der Grauspannungserzeuger (810) weiter ein Paar von Widerständen (R12, R11) einschließt, die seriell zwischen der ersten und der zweiten Reihe von Widerständen (R1-R5, R6-R10) angeschlossen sind, ein Paar von Dioden (D1, D2), die seriell zwischen dem Paar von Widerständen (R12, R11) angeschlossen sind, und einen Kondensator (C1), der zwischen einem Knoten zwischen den Dioden (D1, D2) und einer vordefinierten Spannung angeschlossen ist, wie zum Beispiel der Erdspannung, wobei die Vorwärtsrichtungen der Dioden (D1, D2) in der Richtung von der ersten Reihe von Widerständen (R1-R5) zur zweiten Reihe von Widerständen (R6-R10) liegen,

wobei die Widerstände in der ersten Reihe (R1-R5) seriell zwischen einer vordefinierten Spannung (V<sub>dd</sub>) von einer externen Quelle und einem des Paares von Widerständen (R12) ange-

schlossen sind, wobei die Vielzahl positiver Grauspannungen (VREF1-VREF5) von jeweiligen Knoten zwischen den Widerständen der ersten Reihe von Widerständen (R1-R5) und von einem Knoten zwischen der ersten Reihe von Widerständen und dem anderen des Paares von Widerständen (R5 und R12) gewonnen wird,

wobei die Widerstände in der zweiten Reihe (R6-R10) seriell zwischen dem anderen des Paares von Widerständen (R11) und einer vordefinierten Spannung, wie zum Beispiel der Erdspannung, angeschlossen sind, wobei die Vielzahl negativer Grauspannungen (VREF6-VREF10) von einem Knoten zwischen dem anderen des Paares von Widerständen (R11) und der zweiten Reihe von Widerständen und von jeweiligen Knoten zwischen den Widerständen der zweiten Reihe von Widerständen (R6-R10) gewonnen wird,

weiter **gekennzeichnet durch**

einen Pegelregler, der angeordnet ist, um einen Spannungspegel der ersten und zweiten Impulssignale (Q,  $\bar{Q}$ ) vom Impulssignalerzeuger (822, 824) anzupassen, um die ersten und zweiten Referenzspannungen (VREF8, VREF3) zu erzeugen, wobei der Pegelregler Folgendes umfasst:

ein Paar von Widerständen (RF, RG), die angeordnet sind, so dass jede der beiden Ausgangsklemmen für die ersten und zweiten Impulssignale (Q,  $\bar{Q}$ ) direkt mit einem entsprechenden des Paares von Widerständen (RF, RG) verbunden ist, wobei einer des Paares von Widerständen wiederum mit einem Knoten (N1) innerhalb der ersten Reihe von Widerständen (R1-R5) verbunden ist, wobei der andere des Paares von Widerständen wiederum mit einem Knoten (N2) innerhalb der zweiten Reihe von Widerständen (R6-R10) verbunden ist.

19. Die Vorrichtung gemäß Anspruch 18, worin ein Widerstand, der direkt mit einer der beiden Ausgangsklemmen für die ersten und zweiten Impulssignale (Q,  $\bar{Q}$ ) verbunden ist, einen veränderlichen Widerstand umfasst.

## Revendications

1. Circuit d'excitation d'un dispositif d'affichage à cristaux liquides et apte à générer des tensions de données compensées pour une inversion de points deux-à-un, une inversion de points trois-à-un ou une inversion de points quatre-à-un, comprenant :

un producteur (810) de tensions de niveaux de gris configuré pour générer une pluralité de tensions de niveaux de gris positives (VREF1, VREF2, VREF4, VREF5) et une pluralité de tensions de niveaux de gris négatives (VREF6, VREF7, VREF9, VREF10) sur la base d'une pluralité de tensions de référence incluant une première tension de référence (VREF8) pour les niveaux de gris positifs (VREF1, VREF2, VREF4, VREF5) et une seconde tension de référence (VREF3) pour les niveaux de gris négatifs (VREF6, VREF7, VREF9, VREF10);  
 un producteur (822, 824) de signaux d'impulsion disposé pour générer un premier et un second signaux d'impulsion (Q,  $\bar{Q}$ ) à phases inversées ;  
 et  
 un régleur de niveau disposé pour régler un niveau de tension du premier et du second signaux d'impulsion (Q,  $\bar{Q}$ ) à partir du producteur de signaux d'impulsion (822, 824) pour générer la première et la seconde tensions de référence (VREF8, VREF3), **caractérisé en ce que** le régleur de niveau comprend :

une paire de premiers résisteurs (R13, R14) connectés en série entre une première tension prédéterminée (Vdd) et une seconde tension prédéterminée et ayant un noeud (N3) connecté entre les deux, lequel noeud (N3) ayant une tension (Vin);  
 une paire de second résisteurs (R15, R16) disposés pour se connecter respectivement au premier et au second signaux d'impulsion (Q,  $\bar{Q}$ );  
 un interrupteur disposé pour connecter ledit noeud (N3) entre la paire de résisteurs (R13, R14) alternativement à un résisteur (R15, R16) ou à l'autre de la seconde paire de résisteurs (R15, R16) de sorte que le résisteur connecté de la seconde paire de résisteur (R15, R16) est accouplé entre la sortie respective pour l'un des premier et second signaux d'impulsion (Q,  $\bar{Q}$ ) et ledit noeud (N3);  
 un premier amplificateur (832), recevant une entrée du noeud (N3), pour amplifier la tension (Vin) du noeud (N3) pour produire la première tension de référence (VREF8) ;  
 et  
 un second amplificateur (834) disposé pour inverser une sortie du premier amplificateur (832) par rapport à une tension prédéterminée (RFC, Vdd/2) pour produire la seconde tension de référence (VREF3).

2. Méthode d'excitation d'un dispositif d'affichage à cristaux liquides et de génération de tensions de données compensées pour une inversion de points

deux-à-un, une inversion de points trois-à-un ou une inversion de points quatre-à-un, la méthode comprenant :

la génération de premier et second signaux d'impulsion (Q,  $\bar{Q}$ ) à phases inversées;  
 la génération d'une première tension (Vin) d'un noeud (N3) entre une première paire de résisteurs (R13, R14) connectés en série entre une première tension prédéterminée (Vdd) et une seconde tension prédéterminée en commutant alternativement entre soit une connexion du noeud (N3) à la sortie du premier signal d'impulsion à travers le premier résisteur d'une seconde paire de résisteurs (R15), soit une connexion du noeud (N3) à la sortie du second signal d'impulsion à travers le second résisteur de la seconde paire de résisteurs (R16) ;  
 l'amplification de la première tension (Vin) pour produire une première tension de référence (VREF8) ;  
 l'inversion de la première tension de référence (VREF8) par rapport à une tension prédéterminée (RFC, Vdd/2) pour produire une seconde tension de référence (VREF3) ; et  
 la génération d'une pluralité de tensions de niveaux de gris positive et négative (VREF1, VREF2, VREF4, VREF5, VREF6, VREF7, VREF9, VREF10) sur la base des première et seconde tension de référence (VREF8, VREF3).

3. Dispositif d'affichage à cristaux liquides comprenant :

une pluralité de lignes de grille (G1-Gn) transmettant des signaux de grille ;  
 une pluralité de lignes de données (D1-Dm) croisant la pluralité de lignes de grille (G1-Gn) et transmettant les tensions de données ; et  
 une pluralité de rangées de pixels, chaque rangée de pixels incluant une pluralité de pixels, chacune de la pluralité de pixels incluant un élément de commutation (Q) connecté à l'une de la pluralité de lignes de grille (G1-Gn) et l'une de la pluralité de lignes de données (D1-Dm), et des moyens disposés pour appliquer des valeurs absolues des tensions de données à une rangée de l'ensemble de pixels par rapport à une première tension prédéterminée supérieure aux valeurs absolues des tensions de données appliquées à une autre rangée de l'ensemble de pixels pour les mêmes niveaux de gris, et comprenant en outre le circuit d'excitation de la revendication 1.

4. Dispositif d'affichage à cristaux liquides selon la revendication 3, comprenant en outre des moyens dis-

posés afin d'inverser la polarité des tensions de données fournies à la pluralité de pixels par un ensemble de pixels incluant deux ou plusieurs rangées de pixels.

5. Dispositif d'affichage à cristaux liquides selon les revendications 3 et 4, dans lequel l'une rangée de pixels est la première à laquelle sont appliquées les tensions de données dans l'ensemble de pixels.

6. Dispositif d'affichage à cristaux liquides selon les revendications 3 et 4, dans lequel l'une rangée de pixels est la dernière à laquelle sont appliquées les tensions de données dans l'ensemble de pixels.

7. Dispositif d'affichage à cristaux liquides selon les revendications 3 et 4, comprenant en outre :

un circuit de commande de grille (400) disposé afin d'alimenter séquentiellement une tension d'activation de grille à la pluralité de lignes de grille (G1-Gn) pour activer les éléments de commutation ;

un générateur (800) de tensions de niveaux de gris disposé afin de générer une pluralité de tensions de niveaux de gris, chaque tension de niveaux de gris ayant au moins deux valeurs différentes; et

un circuit de commande de données (500) disposé afin de sélectionner une pluralité de tensions de niveaux de gris et pour alimenter les tensions de niveaux de gris sélectionnées comme les tensions de données à la pluralité de pixels à travers les éléments de commutation activées.

8. Dispositif d'affichage à cristaux liquides selon la revendication 7, dans lequel le générateur (800) de tension de niveaux de gris comprend :

un producteur de tension de référence, connecté au producteur (810) de tension de niveaux de gris, apte à générer la première tension de référence (VREF8) avec une valeur qui change selon le nombre de rangées de pixels dans l'ensemble de pixels à fournir pour le producteur de tension de niveaux de gris (810).

9. Dispositif d'affichage à cristaux liquides selon la revendication 8, dans lequel le producteur de tension de référence comprend :

un régulateur de niveau disposé afin de régler un niveau de tension d'au moins un signal d'impulsion du producteur de signaux d'impulsion (822, 824) pour générer la première tension de référence (VREF8).

10. Dispositif d'affichage à cristaux liquides selon la revendication 8, dans lequel le régulateur de niveau comprend un générateur de tension de terminal d'entrée disposé afin de commuter alternativement entre la sortie du premier et du second signaux d'impulsion (Q,  $\bar{Q}$ ) et pour changer les niveaux du premier et du second signaux d'impulsion (Q,  $\bar{Q}$ ) pour générer une première tension (Vin), et un changeur de niveau disposé afin de changer la première tension (Vin) pour générer la première tension de référence (VREF8).

11. Dispositif d'affichage à cristaux liquides selon la revendication 10, dans lequel le générateur de tension de terminal d'entrée comprend :

un commutateur (5W) disposé afin de commuter alternativement entre les sorties du premier et du second signaux d'impulsion (Q,  $\bar{Q}$ ) et une pluralité de résisteurs comprenant une paire de premiers résisteurs (R13, R14) connectés en série entre une deuxième tension prédéterminée et une troisième tension prédéterminée et une paire de seconds résisteurs (R15, R16) respectivement connectés aux sorties des premier et second signaux d'impulsion (Q,  $\bar{Q}$ ), le commutateur (SW) est connecté à un premier noeud (N3) entre les premiers résisteurs (R13, R14) et alternativement connecté à l'un ou à l'autre des seconds résisteurs (R15, R16), et le générateur de tension d'entrée est configuré pour émettre une tension (Vin) du premier noeud (N3).

12. Dispositif d'affichage à cristaux liquides selon la revendication 11, dans lequel le changeur de niveau comprend :

un amplificateur (832) configuré pour amplifier la première tension (Vin) ;  
un troisième résistor (RG) connecté entre l'amplificateur (832) et le producteur de tension de niveaux de gris (810) pour produire la première tension de référence (VREF8).

13. Dispositif d'affichage à cristaux liquides selon la revendication 12, dans lequel la pluralité de tension de référence comprend en outre une seconde tension de référence (VREF3), et le changeur de niveau comprend :

un inverseur (834, R19, R20, N5) disposé afin d'inverser une sortie de l'amplificateur (832) par rapport à une seconde tension de référence (RFC) ;  
un quatrième résistor (RF), connecté entre l'inverseur et le producteur de tension de niveaux de gris (810), disposé afin de fournir la seconde

tension de référence (VREF3).

14. Dispositif d'affichage à cristaux liquides selon la revendication 13, dans lequel le producteur de tension de niveaux de gris (810) comprend une pluralité de cinquièmes résisteurs (R1-R5) pour les niveaux de gris positifs (VREF1, VREF2, VREF4, VREF5) connectés en série, une pluralité de sixièmes résisteurs (R6-R10) pour les niveaux de gris négatifs (VREF6, VREF7, VREF9, VREF10) connectés en série, l'une de la première et de la seconde tension de référence (VREF8, VREF3) sont fournies pour un noeud (N1) entre les cinquièmes résisteurs (R1-R5), et l'autre de la première et de la seconde tensions de référence (VREF8, VREF3) sont fournies pour un noeud (N2) entre les sixièmes résisteurs (R6-R10).
15. Dispositif d'affichage à cristaux liquides selon la revendication 13, dans lequel le troisième et le quatrième résisteurs (RF, RG) comprennent des résisteurs variables.
16. Dispositif d'affichage à cristaux liquides selon la revendication 10, dans lequel le producteur de signal d'impulsion (822, 824) comprend une bascule bistable D (822) disposée afin de générer les premier et second signaux d'impulsion (Q,  $\bar{Q}$ ) sur la base d'un signal d'horloge pour le circuit de commande de grille (400).
17. Dispositif d'affichage à cristaux liquides selon la revendication 16, dans lequel le producteur de signal d'impulsion (822, 824) comprend en outre une porte OU (824) disposée pour opération OU du premier signal d'impulsion (Q) et un signal de démarrage (STV) pour le circuit de commande de grille (400) pour fournir un signal pour la bascule bistable D (822) en tant qu'entrée.
18. Circuit d'excitation d'un dispositif d'affichage à cristaux liquides et apte à générer des tensions de données compensées pour une inversion de points deux-à-un, une inversion de points trois-à-un ou une inversion de points quatre-à-un, comprenant :
- un producteur (810) de tensions de niveaux de gris configuré pour générer une pluralité de tensions de niveaux de gris positives (VREF1, VREF2, VREF4, VREF5) et une pluralité de tensions de niveaux de gris négatives (VREF6, VREF7, VREF9, VREF10) sur la base d'une pluralité de tensions de référence incluant une première tension de référence (VREF8) pour les niveaux de gris positifs (VREF1, VREF2, VREF4, VREF5) et une seconde tension de référence (VREF3) pour les niveaux de gris négatifs (VREF6, VREF7, VREF9, VREF10); le producteur de tension de niveaux de gris (810) in-

cluant une première disposition de résisteurs (R1-R5) connectés en série générant des tensions de niveaux de gris positives (VREF1-VREF5), et une seconde disposition de résisteurs (R6-R10) connectés en série générant des tensions de niveaux de gris négatives (VREF6-VREF10), et

un producteur de signal d'impulsion (822, 824) disposé afin de générer un premier et un second signaux d'impulsion (Q,  $\bar{Q}$ ) à phases inversées ; **caractérisé en ce que**

le producteur de tension de niveaux de gris (810) inclut en outre une paire de résisteurs (R12, R11) connectés en série entre la première et la seconde disposition de résisteurs (R1-R5, R6-R10), une paire de diode (D1, D2) connectés en série entre ladite paire de résisteurs (R12, R11), et un condensateur (C1) connecté entre un noeud entre les diodes (D1, D2) et une tension prédéterminée comme la tension de terre, les directions directes des diodes (D1, D2) étant en direction de la première disposition de résisteurs (R1-R5) à la seconde disposition de résisteurs (R6-R10),

les résisteurs dans la première disposition (R1-R5) étant connectés en série entre une tension prédéterminée (Vdd) d'une source extérieure et l'un de la paire de résisteurs (R12), la pluralité de tension de niveaux de gris (VREF1-VREF5) étant obtenue des noeuds respectifs entre les résisteurs de la première disposition de résisteurs (R1-R5) et d'un noeud entre la première disposition de résisteurs et l'un de la paire de résisteurs (R5 et R12),

les résisteurs de la seconde disposition (R6-R10) étant connectés en série entre l'autre de la paire de résisteurs (R11) et une tension prédéterminée comme la tension de terre, la pluralité de tension de niveaux de gris négatives (VREF6-VREF10) étant obtenue d'un noeud entre l'autre de la paire de résisteurs (R11) et la seconde disposition de résisteurs et des noeuds respectifs entre le résistor de la seconde disposition de résisteurs (R6-R10),

**caractérisée en outre par**

un régleur de niveau disposé afin de régler un niveau de tension des premier et second signaux d'impulsion (Q,  $\bar{Q}$ ) du producteur de signal d'impulsion (822, 824) pour générer les première et seconde tensions de référence (VREF8, VREF3), lequel régleur de niveau comprend :

une paire de résisteurs (RF, RG) disposés de sorte que chacun des deux terminaux de sortie pour les premier et second signaux d'impulsion (Q,  $\bar{Q}$ ) est directement connecté à l'un respectif de la paire de résisteurs

(RF, RG), l'un de la paire de résisteurs étant à son tour connecté à un noeud (N1) dans la première disposition de résisteurs (R1-R5), l'autre de la paire de résisteurs étant à son tour connecté à un noeud (N2) dans la seconde disposition de résisteurs (R6-R10).

5

19. Circuit d'excitation selon la revendication 18, dans lequel un résistor directement connecté à l'un des deux terminaux de sortie pour le premier et le second signaux d'impulsion (Q,  $\bar{Q}$ ) comprend un résistor variable.

10

15

20

25

30

35

40

45

50

55

FIG. 1

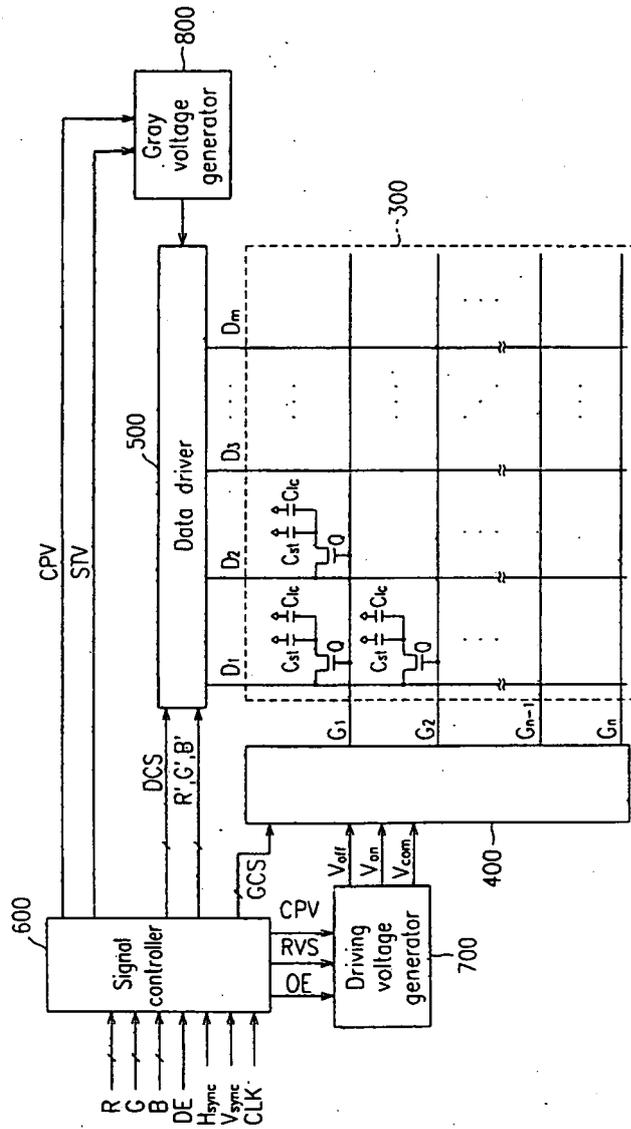


FIG. 2

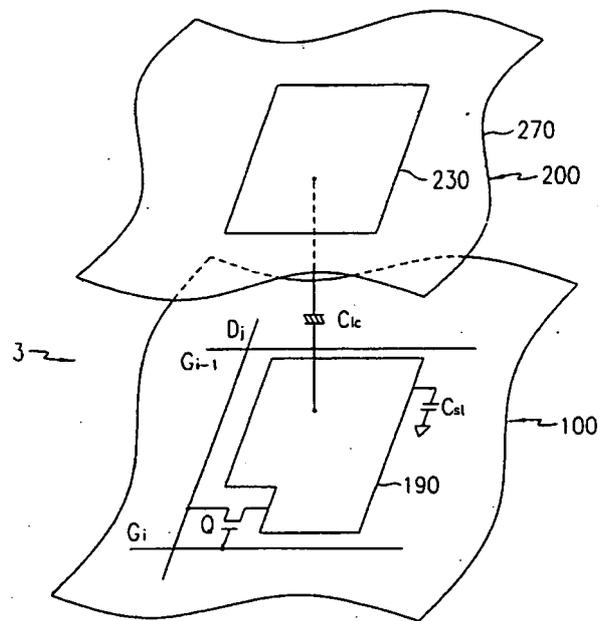


FIG. 3

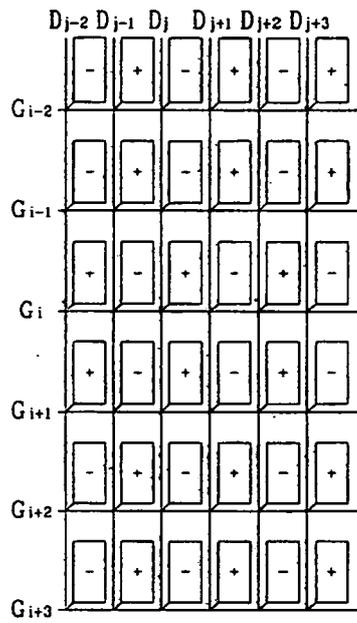
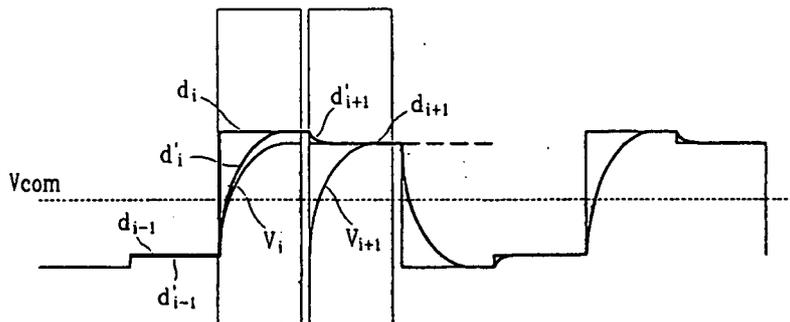


FIG. 4



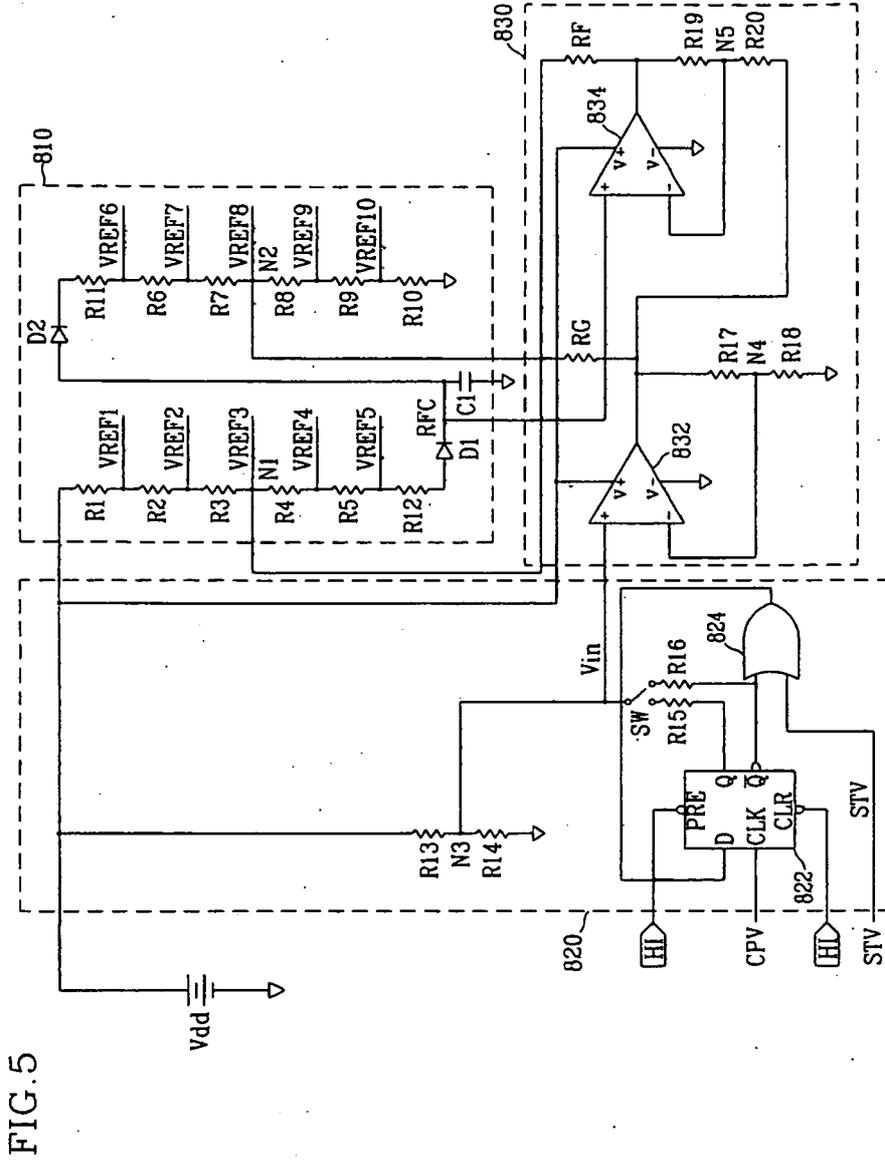
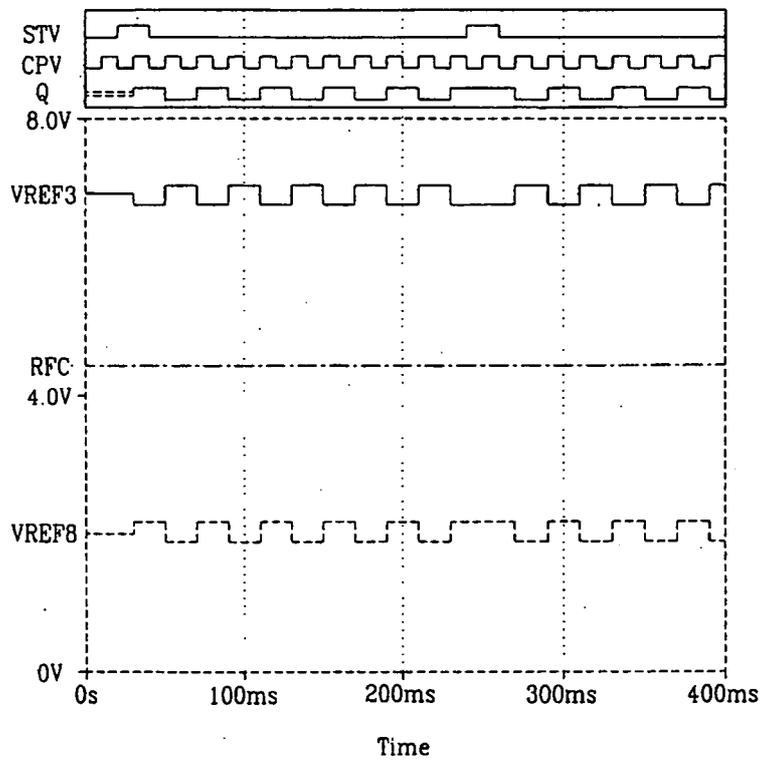


FIG.6



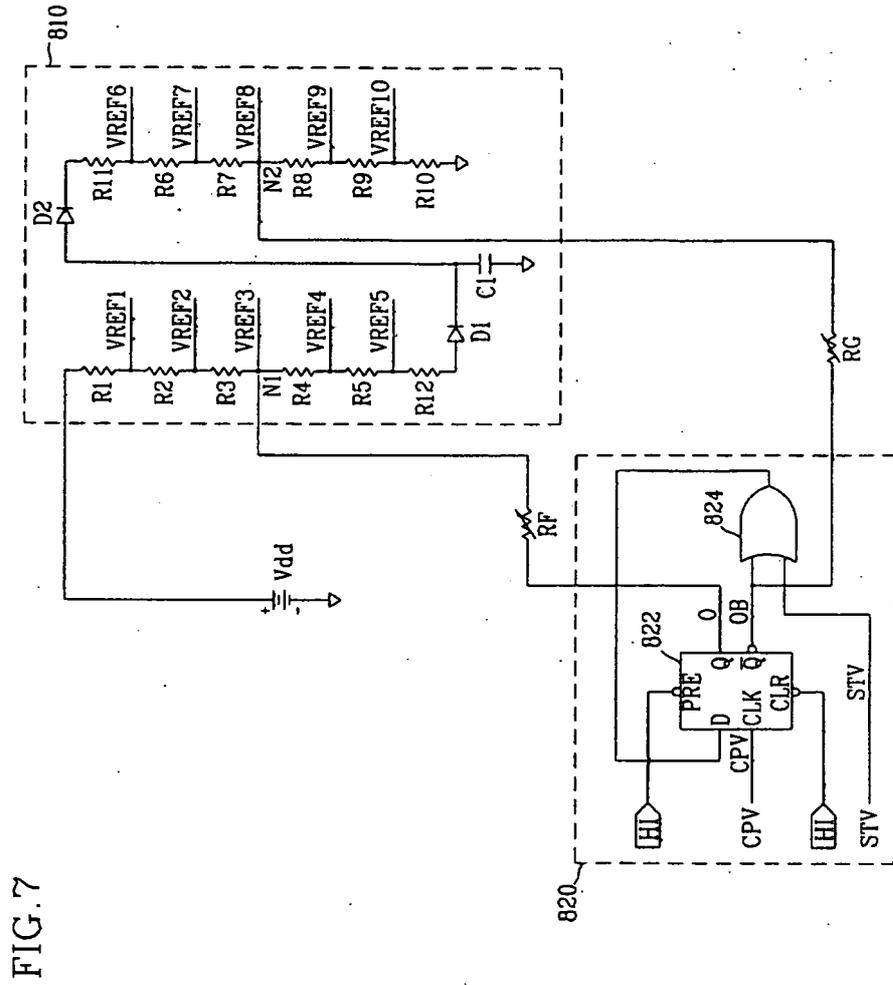


FIG. 7

**REFERENCES CITED IN THE DESCRIPTION**

*This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.*

**Patent documents cited in the description**

- WO 01124154 A [0009]
- US 6075507 A [0010]

专利名称(译)	液晶显示器，用于驱动液晶显示器的装置和产生灰度电压的方法		
公开(公告)号	<a href="#">EP1293957B1</a>	公开(公告)日	2013-02-27
申请号	EP2002019833	申请日	2002-09-06
[标]申请(专利权)人(译)	三星电子株式会社		
申请(专利权)人(译)	SAMSUNG ELECTRONICS CO. , LTD.		
当前申请(专利权)人(译)	三星DISPLAY CO. , LTD.		
[标]发明人	MOON SEUNG HWAN KANG NAM SOO		
发明人	MOON, SEUNG-HWAN KANG, NAM-SOO		
IPC分类号	G09G3/36 G02F1/133 G02F1/136 G09G3/20		
CPC分类号	G09G3/3688 G09G3/3614 G09G3/3696 G09G2310/027 G09G2320/0223		
优先权	1020010055036 2001-09-07 KR		
其他公开文献	EP1293957A2 EP1293957A3		
外部链接	<a href="#">Espacenet</a>		

摘要(译)

液晶显示器，用于驱动液晶显示器的装置和用于驱动液晶显示器的灰度电压的方法。液晶显示器包括传输栅极信号的多条栅极线，与多条栅极线交叉并传输数据电压的多条数据线，以及多个像素行。每个像素行包括多个像素，并且每个像素包括连接到多条栅极线之一和多条数据线之一的开关元件。提供给多个像素的数据电压的极性被包括两个或更多个像素行的像素组反转。相对于第一预定电压施加到像素组的一行的数据电压的绝对值大于施加到相同灰度的像素组的另一行的数据电压的绝对值。

$$\left| d_{upper} - V_{com} \right|$$