(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 174 758 A1

(12) EUROPEAN PATENT APPLICATION
published in accordance with Art. 158(3) EPC

(43) Date of publication:
23.01.2002 Bulletin 2002/04

(21) Application number: **00979031.2**

(22) Date of filing: **30.11.2000**

(51) Int Cl.[7]: **G02F 1/1368**, G02F 1/133, G09G 3/36

(86) International application number:
PCT/JP00/08477

(87) International publication number:
WO 01/40857 (07.06.2001 Gazette 2001/23)

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **03.12.1999 JP 34483299**

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(54) LIQUID CRYSTAL DISPLAY

(57) An object is to provide a liquid crystal display device, which can be driven with low power consumption while keeping display quality. A liquid crystal display device includes a plurality of first vertical scanning lines and a plurality of horizontal scanning lines formed on a substrate in a matrix form; first switching means connected to the horizontal scanning lines and being controllable by the first vertical scanning lines; control capacitor elements for holding control signals on the horizontal scanning lines connected to the first switching means; and second switching means for connecting pixel signal lines and pixel electrodes together to write the potentials on the pixel signal lines to the pixel electrodes, the second switching means being connected to the control capacitor elements.

FIG. 2(a)

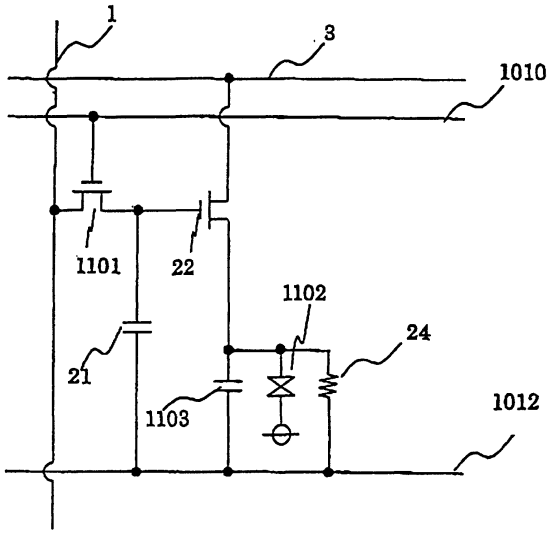

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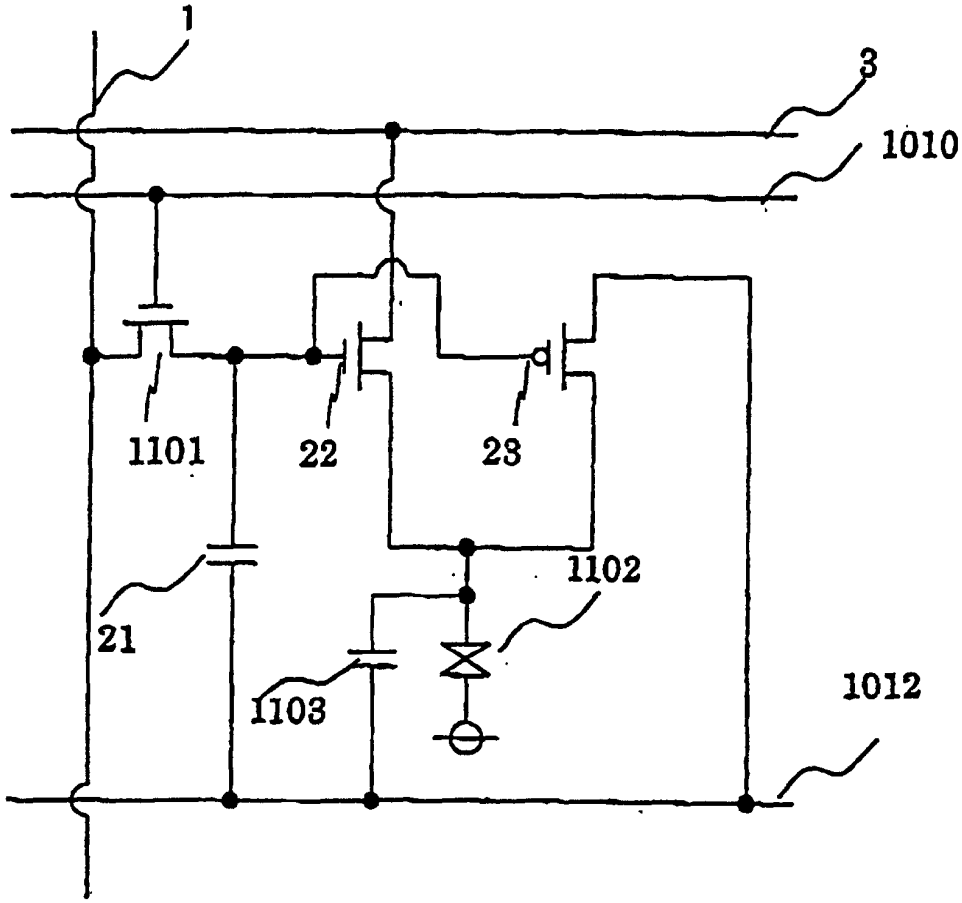
FIG. 2(b)



Description

Technical Field

[0001] The present invention relates to a liquid crystal display device for displaying images with liquid crystal, and particularly a liquid crystal display device for use in a portable information terminal or a mobile telephone, in which low power consumption is required.

Background Art

[0002] Some kinds of personal computers and television sets use liquid crystal display devices for displaying still images and moving images. Fig. 14 shows a structure of a conventional color liquid crystal display device. In Fig. 14, 1001 indicates one pixel formed of three, i. e., R, B and G pixels. 1002 indicates a liquid crystal display portion formed of a large number of pixels arranged in rows and columns. 1003 indicates a vertical scanning circuit, which is formed of a shift register circuit 1004 and a buffer circuit 1005, and can select one row in the liquid crystal display portion. 1006 indicates a horizontal scanning circuit, which is formed of a shift register circuit 1007, a buffer circuit 1008 and a switch 1009 for applying a signal to one column in the liquid crystal display portion. 1010 and 1011 indicate a vertical scanning line and a signal line, which connect vertical scanning circuit 1003 and horizontal scanning circuit 1006 to each pixel, respectively. Fig. 15 is a circuit diagram showing one pixel in Fig. 11. In Fig. 15, 1101 indicates a TFT, 1102 indicates a liquid crystal display element and 1103 indicates a capacitor.

[0003] An operation will now be described. When a positive voltage is applied to vertical scanning line 1010, TFT 1101 is turned on to connect signal line 1011 to liquid crystal display element 1102 and capacitor 1103. Thereby, liquid crystal display element 1102 and capacitor 1103 are charged to a potential equal to that on signal line 1011. In a case of a so-called dot sequential drive, horizontal scanning circuit 1006 successively charges the respective column pixels in one row. After all the column pixels are scanned, vertical scanning circuit 1003 sets the voltage on vertical scanning line 1010 to zero or negative value so that TFT 1101 is turned off, and the voltages on liquid crystal display element 1102 and capacitor 1103 are maintained. In a similar manner, the subsequent rows are successively scanned. After vertical scanning circuit 1003 scanned all the rows (which will be referred to as "one frame"), the positive voltage is applied to vertical scanning line 1010 again, and the voltage is written from the signal line to liquid crystal display element 1102 and capacitor 1103. In this manner, all the pixels are successively written a frame at a time, and the display is performed.

[0004] Since the liquid crystal display device has the structure described above, it is necessary to maintain a voltage by the electrostatic capacitances of the liquid crystal display element and capacitor for a period (i.e., one frame period) from writing of the signal in one pixel to rewriting thereof. However, the voltage lowers due to a finite resistivity of the liquid crystal, leakage in TFT and others, resulting in lowering of display quality such as flicker. Fig. 16 shows this state. At (a) is represented an operation with a usual frame frequency of 60 Hz. In this operation, one pixel is rewritten one time for a frame period of 1/60 seconds. Therefore, the voltage lowering is small, and the reflectance (brightness) of the pixel does not change so that lowering of the display quality such as flicker and lowering of contrast does not occur.

[0005] A major portion of the power consumed in the liquid crystal display device is occupied by the powers consumed by the shift register circuits, which perform fast operations in vertical scanning circuit 1003 operating at a frequency of ((frame frequency) x (number of vertical scanning lines)) as well as horizontal scanning circuit 1006 operating at a frequency of ((frame frequency) x (number of vertical scanning lines) x (number of horizontal scanning lines)). For reducing the power consumption, it is effective to reduce the operation frequencies of these circuits or to operate them intermittently. At (b) is represented a case where the operation frequencies of the horizontal and vertical scanning circuits are lowered for reducing the power consumption. In this case, the rewriting time period (i.e., frame period) of the liquid crystal display element increase, and the voltage lowers to an extremely large extent during such a long period. When the display is performed under such conditions, the voltage changes with time so that the reflectance (brightness) changes to a large extent to cause flicker. Also, the average voltage lowers so that sufficient contrast and others cannot be achieved, resulting in low display quality.

[0006] An object of the invention is to provide a liquid crystal display device overcoming the above disadvantages, and particularly a liquid crystal display device operating with low power consumption without lowering display quality.

Disclosure of the Invention

[0007] A liquid crystal display device of a first structure of the invention includes a plurality of first vertical scanning lines and a plurality of horizontal scanning lines formed on a substrate in a matrix form; first switching means connected to the horizontal scanning lines and being controllable by the first vertical scanning lines; a control capacitor element for holding a control signal on the horizontal scanning line connected to the first switching means; and second switching means for connecting a pixel signal line and a pixel electrode together to write the potential on the pixel signal lines to the pixel electrodes, the second switching means being connected to the control capacitor elements. Since this structure includes the switch, which is connected to the control element and the control capacitor element for holding

the pixel select signal, and can write the reference potential to the pixel, the liquid crystal display device operating with low power consumption can be achieved.

[0008] In a liquid crystal display device of a second structure of the invention, the pixel electrode is connected to the two reference lines via independent switching means, respectively, and at least one of the switching means is a second switching means being controlled by the control capacitor element. According to this structure, the switching means for writing the potential on the common line to the pixel is employed in addition to the switch for writing the reference potential. Therefore, the liquid crystal display device capable of display with good contrast can be achieved.

[0009] A liquid crystal display device of a third structure of the invention has the second structure, and further has such a structure that the second switching means is formed of n-type and p-type TFTs, and one and the other of the TFTs are connected to the different reference line potentials, respectively. According to this structure, since the switching means for writing the potential on the common line to the pixel is employed in addition to the switch for writing the reference potential, the liquid crystal display device capable of display with good contrast can be achieved.

[0010] A liquid crystal display device of a fourth structure of the invention has any one of the first to third structures, and further has such a structure that third switching means being controllable by a second vertical scanning line is connected in series between the second switching means and the pixel electrode. According to this structure, the switch formed of a p-type TFT for writing the potential on the common line to the pixel is employed in addition to the switch for writing the reference potential. Therefore, the liquid crystal display device capable of display with good contrast can be achieved.

[0011] A liquid crystal display device of a fifth structure of the invention has any one of the first to third structures, and further has such a structure that third switching means is connected in series between the n-type TFT forming the second switching means and the pixel electrode, and fourth switching means being controllable by a third vertical scanning line is connected in series between the p-type TFT forming the second switching means and the pixel electrode. According to this structure, the switch, which is controlled by the vertical scanning circuit, is arranged in series with the switch for writing the reference potential or the potential on the common line. Therefore, a defect can be suppressed in the liquid crystal display device. According to this structure, the switch controlled by the third control line is arranged in series with the switch for writing the reference potential, and the switch controlled by the fourth control line is arranged in series with the switch for writing the potential on the common line. Therefore, it is possible to provide the liquid crystal display device, which can perform a multi-level display operation in addition to the operation with low power consumption.

[0012] In a liquid crystal display device of a sixth structure of the invention, fifth switch means being controllable by the first vertical scanning line is connected in series between the n-type TFT forming the second switching means and the pixel electrode, and sixth switching means being controllable by the third vertical scanning line is connected in series between the n- and p-type TFTs forming the second switching means and the pixel electrode. According to this structure, it is possible to achieve the liquid crystal display device of a simple structure, which can perform the multi-level display in addition to the operation with low power consumption.

[0013] A seventh structure of the invention has any one of the first to fifth structures, and further has such a structure that a drive circuit connected to the second vertical scanning line divides a row of externally supplied time-series binary control signals into signals corresponding to the pixel electrodes so that the control signal corresponding to the pixel electrode can be held until the end of writing to the control capacitor element. According to this structure, the switch controlled by the vertical scanning line is arranged in series with the switch for writing the reference potential, and the switch controlled by the third control line is arranged in series with the switch for writing the reference potential and the switch for writing the potential on the common line. Therefore, it is possible to achieve the liquid crystal display device of a simple structure, which can perform the multi-level display in addition to the operation with low power consumption.

[0014] An eighth structure of the invention has any one of the first to seventh structures, and further has such a structure that the reference potential on the pixel signal line is set such that the potential written into the pixel electrode by the second switching means is equal to a value obtained by adding or subtracting a liquid crystal drive voltage to or from the potential on the opposed substrate, and the potential on the common line is set such that the potential written into the pixel electrode by the second switching means is equal to the potential on the opposed substrate. According to this structure, the reference potential and the potential on the common line are set to attain the maximum and minimum reflectances of the liquid crystal, respectively, so that the liquid crystal display can exhibit high contrast.

[0015] A ninth structure of the invention has any one of the first to eighth structures, and further has such a structure that the pixel signal line is connected by switching means to a reference potential bus line for externally supplying the reference potential into the device, and the switching means is configured to operate together with at least one of the first, second and third vertical scanning lines. According to this structure, the liquid crystal display device can have a power supply of a compact structure for generating the reference potential.

[0016] A tenth structure of the invention has any one of the third to eighth structures, and further has such a

structure that a time interval between the writing operations for the pixel electrode is shorter than the time interval between the writing operations for the control capacitor element. According to this structure, the liquid crystal display device can perform high-contrast display with low power consumption while eliminating flicker.

[0017] An eleventh structure of the invention has any one of the fourth to tenth structures, and further has such a structure that a time interval between changes of the potential on the pixel signal line between the opposite sides of the potential on the opposite substrate is longer than a time interval between the writing operations for the pixel electrode. This structure can achieve the liquid crystal display device requiring further reduced power consumption.

[0018] A twelfth structure of the invention has any one of the first to eleventh structures, and further has such a structure that the pixel electrode for one pixel is divided into a plurality of pixel electrodes, and first switching means connected to the first vertical scanning line and the horizontal scanning line, the control capacitor element for holding the control signal on the horizontal scanning line connected to the switching means, and the second switching means for writing the potential of the pixel signal to the pixel electrode are provided for each of the pixel electrodes. This structure can achieve the liquid crystal display device capable of multi-level display.

[0019] A thirteenth structure of the invention has the twelfth structure, and further has such a structure that at least one of the plurality of divided pixel electrodes has an area different from those of the other pixel electrodes. According to this structure, the liquid crystal display device can perform display in further increased levels.

[0020] A fourteenth structure has any one of the first to thirteenth structures, and further has such a structure that the pixel electrode is formed of a metal film, and is of a reflection type. It is possible to achieve the liquid crystal display device of the reflection type operating with extremely low power consumption.

Brief Description of the Drawings

[0021]

Fig. 1 shows a structure of a drive circuit of a liquid crystal display device according to a first embodiment of the invention;

Fig. 2 is a circuit diagram showing a drive circuit of the liquid crystal display device according to first and second embodiments of the invention;

Fig. 3 shows a third embodiment of the invention;

Fig. 4 shows a structure of a drive circuit of a liquid crystal display device according to the third embodiment of the invention;

Fig. 5 shows a structure of a drive circuit of a liquid crystal display device according to a fourth embodiment of the invention;

Fig. 6 is a circuit diagram showing the drive circuit of the liquid crystal display device according to the fourth embodiment of the invention;

Fig. 7 is a circuit diagram showing a drive circuit of a liquid crystal display device of a fifth embodiment of the invention;

Fig. 8 is a waveform diagram showing a circuit operation of the fifth embodiment of the invention;

Fig. 9 is a circuit diagram showing a drive circuit of a liquid crystal display device of a sixth embodiment of the invention;

Fig. 10 shows a structure of a drive circuit of a liquid crystal display device of a seventh embodiment of the invention;

Fig. 11 shows a structure of a drive circuit of a liquid crystal display device of an eighth embodiment of the invention;

Fig. 12 is a waveform diagram showing a drive waveform of a liquid crystal display device according to a ninth embodiment of the invention;

Fig. 13 is a waveform diagram showing a drive waveform of the liquid crystal display device according to the ninth embodiment of the invention;

Fig. 14 shows a structure of a drive circuit of a liquid crystal display device in the prior art;

Fig. 15 is a circuit diagram showing the drive circuit of the liquid crystal display device in the prior art; and

Fig. 16 is a waveform diagram showing an operation of the drive circuit of the liquid crystal display device in the prior art.

Best Mode for Carrying Out the Invention

[0022] Embodiments of the invention will now be described with reference to the drawings. In the drawings, the same parts and portions bear the same reference numbers, and description thereof is not repeated.

First Embodiment

[0023] Fig. 1 shows a structure of a first embodiment of a liquid crystal display device according to the invention. In Fig. 1, 1 indicates a horizontal scanning line, 2 indicates a data signal line, 3 indicates a pixel signal line and 4 indicates a pixel. Fig. 2 is a circuit diagram showing a structure of one pixel. In Fig. 2, 21 indicates a control capacitor element (i.e., capacitor element for control), 22 indicates a second n-type TFT (second switching means) and 24 indicates a resistance element.

[0024] An operation will now be described. As already described, vertical and horizontal scanning circuits 1003 and 1006 cooperate to select one pixel, as already described. In the invention, horizontal scanning line 1 including the pixel to be turned on is supplied with a positive voltage, e.g., of 5 V from data signal line 2 via switch 1009 selected by horizontal scanning circuit 1006 so

that control capacitor element 21 is charged with a positive voltage on horizontal scanning line 1 via TFT 1101. In this state, control capacitor element 21 is connected to second n-type TFT 22 so that second n-type TFT 22 is turned on, and liquid crystal display element 1102 and capacitor 1103 are connected only to pixel signal line 3 (first reference line), and are charged with the voltage on pixel signal line 3. In a so-called dot sequential drive, vertical scanning circuit 1003 sets the voltage on vertical scanning line 1010 to zero or a negative value after all the column pixels in one row are scanned. Thereby, TFT 1101 is turned off to hold the voltage on control capacitor element 21, and n-type TFT 22 is kept on so that connection of liquid crystal display element 1102 and capacitor 1103 to pixel signal line 3 is always kept.

[0025] After vertical scanning circuit 1003 scans all the rows, a positive voltage is applied to vertical scanning line 1010 again, and the voltage is written into control capacitor element 21 from horizontal scanning line 1. In the first embodiment of the invention, the power consumption may be reduced by lowering the operation frequencies of the horizontal and vertical scanning circuits to increase the rewriting time interval of control capacitor element 21. In this case, the voltage on control capacitor element 21 lowers due to leakage and others. However, this voltage is used for turning on n-type TFT 22. As long as this voltage is higher than a so-called threshold voltage of n-type TFT 22, n-type TFT 22 is kept on so that the connection of liquid crystal display element 1102 and capacitor 1103 to pixel signal line 3 is kept. Therefore, a change in reflectance (brightness), e.g., shown at (b) in Fig. 2 does not occur. For the pixel in the off state, corresponding second n-type TFT 22 is off so that a current does not flow from pixel signal line 3, and the voltages on liquid crystal display element 1102 and capacitor 1103 are fixed by resistance element 24 to common line 1012 (second reference line). In this case, the reference potential on pixel signal line 3 is set such that the potential written to the pixel electrode is equal to a value obtained by adding or subtracting the liquid crystal drive voltage to or from the voltage on the opposed substrate. Therefore, it provides the maximum value (minimum value in the normally white mode) of the reflectance of the liquid crystal. At the same time, the potential on common line 1012 is set such that the potential written to the pixel electrode may be equal to the potential on the opposed substrate, and therefore it provides the minimum value (maximum value in the normally white mode) of the reflectance of liquid crystal. Accordingly, the maximum contract can be achieved by connection to pixel signal line 3 and common line 1012.

[0026] In this embodiment as described above, it is possible to achieve the liquid crystal display device, which allows lowering of the operation frequencies of the vertical and horizontal scanning circuits as well as intermittent driving of the vertical and horizontal scanning circuits, and can operate with low power consumption without impairing the display quality.

Second Embodiment

[0027] At (b) in Fig. 2 is shown a circuit of one pixel in a second embodiment of the invention. At (b) in Fig. 2, 23 indicates a p-type TFT.

[0028] An operation will now be described. In a second embodiment, a positive voltage (e.g., of 5 V) is applied to horizontal scanning line 1 of the pixel to be turned on so that control capacitor element 21 is charged with the positive voltage on horizontal scanning line 1 via TFT 1101. Since control capacitor element 21 is connected to second n-type TFT 22, second n-type TFT 22 is turned on. Meanwhile, p-type TFT 23 is supplied with a positive voltage, and therefore is off so that liquid crystal display element 1102 and capacitor 1103 are connected only to pixel signal line 3, and are charged with the voltage on pixel signal line 3, as already described.

[0029] In this state, since a zero or negative voltage (e.g., -2 V) is applied to horizontal scanning line 1 for the pixel in the off state, control capacitor element 21 is charged with the zero or negative voltage on horizontal scanning line 1 via TFT 1101. In this state, control capacitor element 21 is connected to second n-type TFT 22, which is off. At this time, however, p-type TFT 23 is supplied with the zero or negative voltage, and therefore is on. Therefore, liquid crystal display element 1102 and capacitor 1103 are connected to only common line 1012, and are fixed to the voltage on common line 1012. In this second embodiment, n-type TFT 22 and p-type TFT 23 are connected in a complementary manner so that the liquid crystal voltages for performing black display and white display can be reliably written, and display with high contrast can be achieved.

[0030] For the pixel in the off state, liquid crystal display element 1102 and capacitor 1103 are connected to common line 1012 via p-type TFT 23 so that the reflectance of the pixel in the off state can be completely kept low because charging from pixel signal line 3, which may be caused by leakage from n-type TFT or the like, does not occur. Therefore, the contrast can be kept sufficiently high, and it is possible to achieve the liquid crystal display device, which allows lowering of the operation frequencies of the vertical and horizontal scanning circuits as well as the intermittent drive of the vertical and horizontal scanning circuits without lowering the display quality, and can operate with low power consumption.

[0031] The second embodiment corresponds to the claim 3, and n-type TFT 22 and p-type TFT 23 form switching means, which arc complementary with each other. However, the claim 2 is not restricted to this, and includes various means for reliably supplying two kinds of reference voltages to the liquid crystal display element.

Third Embodiment

[0032] Fig. 3 shows a structure of a third embodiment

of the invention. In Fig. 3, 31 indicates a pixel formed of sub-pixels R1a and R1b. In this case, at least one circuit, which is the same as that shown in Fig. 2, is provided for each sub-pixel.

[0033] An operation will now be described. Owing to the circuit shown in Fig. 2, as already described, it is possible to provide the liquid crystal display device, which allows lowering of the operation frequencies of the vertical and horizontal scanning circuits as well as the intermittent operation thereof without lowering the display quality, and can operate with low power consumption. In this embodiment, each pixel includes the two sub-pixels, each of which is provided with the independent circuit, and therefore can be controlled independently of the other. Therefore, display at multi-levels can be performed.

[0034] Fig. 4 shows electrode areas of the sub-pixels. In Fig. 4, 32 indicates one (R1a) of sub-pixels, and 33 indicates the other sub-pixel R1b. Sub-pixels R1a and R1b have different electrode areas, respectively. When either of sub-pixels R1a and R1b is turned on independently of the other, display at different levels can be performed owing to the different turn-on areas so that display at further increased levels can be performed. The electrode may be formed of a metal film, whereby the liquid crystal display device of the reflection type can be achieved.

Fourth Embodiment

[0035] Fig. 5 shows a structure of a fourth embodiment of the invention. In Fig. 5, 51 indicates a second vertical scanning line A, and 52 indicates a switching element, which is provided in a one-to-one relationship for each of pixel signal lines 3 divided corresponding to the respective rows for arrangement in liquid crystal display portion 1002, and is controlled by a second vertical scanning line A51. 53 is a reference potential bus line, which is connected to all switching elements 52 for applying the potential to pixel signal line 3 via switching element 52. Fig. 6 is a circuit diagram of one pixel (sub-pixel) in the fourth embodiment. 61 indicates a third n-type TFT (third switching means), which is connected in series to second n-type TFT 22 to form a path extending from pixel signal line 3 to including liquid crystal display element 1102 and capacitor 1103. Third n-type TFT 61 is also connected in series to p-type TFT 23 to form a path extending from common line 1012 to liquid crystal display element 1102 and capacitor 1103.

[0036] An operation will now be described. Horizontal and vertical scanning lines 1 and 1010 selectively turn on/off the pixel. As already described, control capacitor element 21 maintains the on/off state of second n-type TFT 22 and third p-type TFT 23. Third n-type TFT 61 is controlled by second vertical scanning line A51, and is turned on only when the positive voltage is applied to second vertical scanning line 51. When turned on, it connects pixel signal line 3 to liquid crystal display element 1102 and capacitor 1103, and also connects common line 1012 to liquid crystal display element 1102 and capacitor 1103. As already shown in Fig. 5, pixel signal line 3 is connected via switching element 52, which is controlled by second vertical scanning line A51 similarly to third n-type TFT 61. When the positive voltage is placed on second vertical scanning line A51 and third n-type TFT 61 is on, the voltage is also placed on pixel signal line 3 so that liquid crystal display element 1102 and capacitor 1103 are charged with the voltage on pixel signal line 3 when the on state is selected, and are charged with the voltage on common line 1012 again when the off state is selected.

[0037] Since the fourth embodiment has the structure described above, only vertical scanning circuit 1003, which operates with a relatively low frequency and low power consumption, is driven to drive only second vertical scanning line A51 after stopping the horizontal and vertical scanning lines 1 and 1010 provided for selecting the on and off states for each pixel. Thus, the time intervals between the write operations for liquid crystal display element 1102 and capacitor 1103 are further reduced by control capacitor element 21. Thereby, liquid crystal display element 1102 and capacitor 1103 are recharged. The potential on pixel signal line 3 is required to be inverted with respect to that on the opposite substrate for preventing such a situation that the liquid crystal is always subjected to the potential in the same direction. By increasing the time interval between the writing operations for the pixel electrode, the times of the potential inversion are reduced, and thereby the power for charging pixel signal line 3 can be reduced. Accordingly, the change in reflectance (brightness) can be small owing to the low power consumption, and the lowering of display quality such as flicker and low contrast can be prevented.

[0038] In the first and second embodiments, all the pixels are simultaneously connected to pixel signal line 3 or common line 1012. If short-circuit occurs in the liquid crystal display element or capacitor of a certain pixel, the voltage on pixel signal line 3 lowers, which affects the whole display. In this embodiment, connection is made only in one row by pixel signal line 3 at a certain time. Therefore, even if short-circuit occurs in the liquid crystal display element or capacitor of a certain pixel, a failure occurs only in display by one row of the pixels, and thus a failure exceeding a so-called line defect does not occur. This improves the yield.

Fifth Embodiment

[0039] Fig. 7 is a circuit diagram of one pixel (sub-pixel) in a fifth embodiment. In Fig. 7, 71 indicates an n-type TFT (third switching means), which is connected in series to second n-type TFT 22 to form a path extending from pixel signal line 3 to liquid crystal display element 1102 and capacitor 1103. 72 indicates an n-type TFT (fourth switching means), which is connected in series

to p-type TFT 23 to form a path extending from common line 1012 to liquid crystal display element 1102 and capacitor 1103. 73 indicates a second vertical scanning line B for controlling switching of n-type TFT 71. 74 indicates a third vertical scanning line for controlling switching of n-type TFT 72.

[0040] An operation will now be described. First, description will now be given on the case where second and third vertical scanning lines 73 and 74 operate simultaneously. In this case, the operation is performed similarly to the third embodiment. By operating the second and third vertical scanning lines B73 and 74, the pixel in the on or off state, which is determined by the voltage on control capacitor element 21, is recharged to attain a predetermined state. Therefore, the change in reflectance (brightness) can be small owing to the low power consumption, and the lowering of display quality such as flicker and low contrast can be prevented. This is referred to as the low power consumption mode.

[0041] In a normal mode, fast moving pictures or the like are displayed at a rate of tens of frames per second, and the states of pixels always change between the on and off states (so that the control capacitor elements in the pixels must be always rewritten). In this mode, an analog voltage is applied to pixel signal line 3, and is written into liquid crystal display element 1102 and capacitor 1103 via second n-type TFT 22 and n-type TFT 71 so that the display at multi-levels depending on the levels of the analog voltage can be performed. Fig. 8 is a time chart showing a change in waveform applied to each control line with time in the case of the normal operation mode. In a waveform shown at (a) in Fig. 8, a positive voltage pulse is applied to vertical scanning line 1010 and second vertical scanning line B73 to select the pixels in one horizontal line or row, and TFT 1101 and n-type TFT 71 are on. The signal on horizontal scanning line 1 having a waveform shown at (c) in Fig. 8 rises simultaneously with the rising of the positive pulses on vertical scanning line 1010 and second vertical scanning line B73, and second n-type TFT 22 is turned on so that liquid crystal display element 1102 and capacitor 1103 are connected to pixel signal line 3. Since pixel signal line 3 is supplied with the voltage pulse, which makes a stepwise change with time as shown at (b) in Fig. 8, the voltages on liquid crystal display element 1102 and capacitor 1103 change in the corresponding manner as shown at (e) in Fig. 8. When the signal on horizontal scanning line 1 changes from a positive voltage to a zero or negative voltage, second n-type TFT 22 is turned off, and liquid crystal display element 1102 and capacitor 1103 are disconnected from pixel signal line 3. Therefore, even when the voltage on pixel signal line 3 changes, the voltage on liquid crystal display element 1102 and capacitor 1103 (i.e., voltage on the pixel electrode) is fixed to the voltage, which was appeared at the time of disconnection as shown at (e) in Fig. 8, and the pixel exhibits the reflectance corresponding to this voltage. In the normal mode, third vertical scanning line 74 is fixed to a zero or negative potential as shown at (d) in Fig. 8.

[0042] According to the fifth embodiment of the invention, as described above, the reflectance corresponding to the levels of the stepwise voltage can be produced in accordance with the timing of changing the signal on horizontal scanning line 1 to the zero or negative voltage, and the multi-level display can be achieved in the normal mode. Thereby, in the case of displaying, e.g., still images, which do not require the change between the on and off states of the pixels, the device is driven in the low power consumption mode, and the sub-pixels are used for achieving multi-level display. In the case of displaying, e.g., moving images by always changing pixels between the on and off states, the liquid crystal display device is driven in the normal mode, and can perform the multi-level display owing to the stepwise voltage applied to pixel signal line 3.

Sixth Embodiment

[0043] Fig. 9 is a circuit diagram showing a pixel (sub-pixel) in a sixth embodiment of the invention. In Fig. 9, 91 indicates an n-type TFT (fifth switching means), which is connected in series to second n-type TFT 22 to form a path extending from pixel signal line 3 to liquid crystal display element 1102 and capacitor 1103. 92 and 93 indicate an n-type TFT (sixth switching means), is connected in series to second n-type TFT 22 to form a path extending from pixel signal line 3 to liquid crystal display element 1102 and capacitor 1103, and is controlled by third vertical scanning line 74.

[0044] An operation will now be described. In the low power consumption mode, third vertical scanning line 74 operates to turn on n-type TFTs 92 and 93. Therefore, liquid crystal display element 1102 and capacitor 1103 are connected to either pixel signal line 3 or common line 1012 depending on the on or off states determined by the voltage on control capacitor element 21, and are recharged to the predetermined state. Therefore, the change in reflectance (brightness) can be small owing to the low power consumption, and the lowering of display quality such as flicker and low contrast can be prevented. In the normal mode, vertical scanning line 1010 simultaneously controls TFT 1101 and n-type TFT 91, and a positive voltage pulse is applied to vertical scanning line 1010 to select the pixels on one horizontal line so that TFTs 1101 and n-type TFTs 91 on the selected horizontal line are turned on. The signal on horizontal scanning line 1 rises simultaneously with the rising of the positive voltage pulse on vertical scanning line 1010, and second n-type TFT 22 is also turned on so that liquid crystal display element 1102 and capacitor 1103 are connected to pixel signal line 3. Since pixel signal line 3 is supplied with the voltage pulse changing stepwise with time as shown in Fig. 8, the voltages on liquid crystal display element 1102 and capacitor 1103 also change in accordance with the stepwise change. When

the signal on horizontal scanning line 1 is changed from the positive voltage to the zero or negative voltage, second n-type TFT 22 is turned off to disconnect liquid crystal display element 1102 and capacitor 1103 from pixel signal line 3. The voltages on liquid crystal display element 1102 and capacitor 1103 are fixed to the voltage, which was appeared at the time of disconnection, and the pixel exhibits the reflectance corresponding to this voltage so that the reflectance corresponding to the levels of the stepwise voltage can be produced in accordance with the timing of changing the signal on horizontal scanning line 1 to the zero or negative voltage.

[0045] In the sixth embodiment, as described above, the normal mode is achieved only by one vertical scanning line 1010, and the low consumption mode is achieved by third vertical scanning line 74 so that the required scanning lines can be small in number. Therefore, a failure due to line breakage can be suppressed, which improves the yield. Since the pixels (sub-pixels) can be arranged at a high density, high-resolution display can be performed.

Seventh Embodiment

[0046] Fig. 10 shows a structure of a seventh embodiment of the invention, in which a latch circuit 101 is used for forming horizontal scanning circuit 1006. Latch circuit 101 is configured to divide a pulse signal row (time-series binary control signals), which is supplied from data signal line 2 for selecting the horizontal scanning line, in accordance with the pixels.

Eighth Embodiment

[0047] Fig. 11 is a circuit diagram showing one pixel (sub-pixel) in an eighth embodiment. The eighth embodiment is a further improvement of the sixth embodiment shown in Fig. 9. In Fig. 11, 901 indicates an n-type TFT, which is arranged in a series path extending from liquid crystal display element 1102 and capacitor 1103 to n-type TFT 92 (fourth switching means), and is also arranged in series with respect to n-type TFT 93 (sixth switching means). Structures other than the above are the same as those in Fig. 9.

[0048] An operation will now be described. In the low power consumption mode, third vertical scanning line 74 operates to turn on n-type TFTs 92 and 93 as well as n-type TFT 901 (seventh switching). Therefore, liquid crystal display element 1102 and capacitor 1103 are connected to either pixel signal line 3 or common line 1012 depending on the on or off states determined by the voltage on control capacitor element 21, and are recharged to the predetermined state. Therefore, the change in reflectance (brightness) can be small owing to the low power consumption, and the lowering of display quality such as flicker and low contrast can be prevented. In the normal mode, vertical scanning line 1010 simultaneously controls TFT 1101 and n-type TFT 91, and a positive voltage pulse is applied to vertical scanning line 1010 to select the pixels on one horizontal line so that TFTs 1101 and n-type TFTs 91 on the selected horizontal line are turned on. The signal on horizontal scanning line 1 rises simultaneously with the rising of the positive voltage pulse on vertical scanning line 1010, and second n-type TFT 22 is also turned on so that liquid crystal display element 1102 and capacitor 1103 are connected to pixel signal line 3. Since pixel signal line 3 is supplied with the voltage pulse changing stepwise with time as shown in Fig. 8, the voltages on liquid crystal display element 1102 and capacitor 1103 also change in accordance with the stepwise change. When the signal on horizontal scanning line 1 changes from the positive voltage to the zero or negative voltage, second n-type TFT 22 is turned off to disconnect liquid crystal display element 1102 and capacitor 1103 from pixel signal line 3. The voltages on liquid crystal display element 1102 and capacitor 1103 are fixed to the voltage, which was appeared at the time of disconnection, and the pixel exhibits the reflectance corresponding to this voltage so that the reflectance corresponding to the levels of the stepwise voltage can be produced in accordance with the timing of changing the signal on horizontal scanning line 1 to the zero or negative voltage.

[0049] As described above, the eighth embodiment can achieve the effect similar to that by the sixth embodiment already described. Further, n-type TFTs 92 and 901 (fourth and seventh switching means) form the dual gate, and n-type TFTs 93 and 901 (sixth and seventh switching means) form the dual gate. Thus, n-type TFT 901 (seventh switching means) is commonly used. Owing to this common use, dual gate structures can be formed by n-type TFT 92 (fourth switching means) and n-type TFT 93 (sixth switching means) for preventing current leakage from liquid crystal display element 1102 while reducing the required space/

Ninth Embodiment

[0050] Fig. 12 is a waveform diagram showing a ninth embodiment. For simplicity reason, only portions of waveforms are shown at (b), (c) and (d) in Fig. 12.

[0051] As shown in a waveform diagram (Fig. 8) showing the normal mode in the fifth embodiment, pixel signal line 3 carries a voltage pulse changing stepwise with time as shown at (b) in Fig. 12. Waveforms shown at (a) and (b) in Fig. 12 are the same as those at (a) and (b) in Fig. 8, respectively. Fig. 13 shows on an enlarged scale a portion A of the stepwise voltage pulse at (b) in Fig. 12. As shown in Fig. 13, the voltage level does not perform stepwise rising from a voltage level corresponding to a certain display level or tone to a voltage level corresponding to a next display level, but exhibits, as shown at (a) in Fig. 13, steep voltage drop P as a result of the change, which occurs in voltage on horizontal scanning line 1 from the positive voltage to the zero or negative voltage due to the capacity couplings between

pixel signal line 3 and the plurality of horizontal scanning lines 1 crossing therewith. This voltage drop changes the voltage level applied to the liquid crystal, and thus lowers the quality of multi-level display. If the plurality of horizontal scanning lines 1 simultaneously change from the positive voltage to the zero or negative voltage (e. g., if all the pixels on one row perform the display at the same level), the capacity coupling, which is present between pixel signal line 3 and each of horizontal scanning lines 1 crossing therewith, is added so that the above steep voltage drop occurs. In view of this, the ninth embodiment is configured such that the voltage pulse, which is applied to horizontal scanning line 1 in each of the odd-numbered columns as shown at (c) in Fig. 12, changes to the zero or negative voltage in accordance with the timing shifted by a predetermined time □t from the change of the voltage pulse for each of the even-numbered columns shown at (d) in Fig. 12. This reduces the number of capacity couplings, which act on pixel signal line 3 at the same timing, and thereby substantially reduces the steep voltage drop in half. In connection with the above operation, K at (b) in Fig. 13 indicates the lowering of the voltage level, which is caused by the capacity coupling between pixel signal line 3 and horizontal scanning line 1 in each of the odd-numbered columns, and G at (b) in Fig. 13 indicates the lowering of the voltage level, which is caused by the capacity coupling between pixel signal line 3 and horizontal scanning line 1 in each of the even-numbered columns. As can be seen therefrom, the number of horizontal scanning lines is reduced in half by divining the horizontal scanning lines into the odd-numbered lines and even-numbered lines. Therefore, the sum of the capacity couplings for each line group can be reduced in half, and the variation in voltage level is reduced in half so that lowering of the image quality can be suppressed.

Industrial Applicability

[0052] The invention can be used as an image display device using liquid crystal, and particularly is suitable to a portable terminal such as a mobile telephone requiring lowering of power consumption.

Claims

1. A liquid crystal display device comprising:

a plurality of first vertical scanning lines and a plurality of horizontal scanning lines formed on a substrate in a matrix form;
first switching means connected to said horizontal scanning lines and being controllable by said first vertical scanning lines;
a control capacitor element for holding a control signal on said horizontal scanning line connected to the first switching means; and
second switching means for connecting a pixel signal line and a pixel electrode together to write the potential on the pixel signal lines to the pixel electrodes,
said second switching means being connected to said control capacitor elements.

2. A liquid crystal display device comprising:

a plurality of first vertical scanning lines and a plurality of horizontal scanning lines formed on a substrate in a matrix form;
a pixel electrode selected by said vertical scanning line and said horizontal scanning line; and
a control capacitor element for holding a control signal on said horizontal scanning line, wherein said pixel electrode is connected to first and second reference lines via independent switching means, respectively, and at least one of said switching means is a second switching means being controlled by said control capacitor element.

3. The liquid crystal display device according to claim 2, wherein

said second switching means is formed of n-type and p-type TFTs, and one and the other of said TFTs are connected to the different reference line potentials, respectively.

4. The liquid crystal display device according to any one of preceding claims 1 to 3, wherein

third switching means being controllable by a second vertical scanning line is connected in series between the second switching means and the pixel electrode.

5. The liquid crystal display device according to any one of preceding claims 1 to 3, wherein

third switching means is connected in series between the n-type TFT forming said second switching means and the pixel electrode, and fourth switching means being controllable by a third vertical scanning line is connected in series between the p-type TFT forming the second switching means and the pixel electrode.

6. A liquid crystal display device, wherein

fifth switch means being controllable by the first vertical scanning line is connected in series between the n-type TFT forming the second switching means and the pixel electrode, and sixth switching means being controllable by the third vertical scanning line is connected in series between the n- and p-type TFTs forming the second switching means and the pixel electrode.

7. The liquid crystal display device according to any

one of preceding claims 1 to 6, wherein

a drive circuit connected to the second vertical scanning line divides a row of externally supplied time-series binary control signals into signals corresponding to the pixel electrodes such that the control signal corresponding to the pixel electrode can be held until the end of writing to the control capacitor element.

8. The liquid crystal display device according to any one of preceding claims 1 to 7, wherein

the reference potential on the pixel signal line is set such that the potential written into the pixel electrode by the second switching means is equal to a value obtained by adding or subtracting a liquid crystal drive voltage to or from the potential on the opposed substrate, and the potential on the common line is set such that the potential written into the pixel electrode by the second switching means is equal to the potential on the opposed substrate.

9. The liquid crystal display device according to any one of preceding claims 1 to 8, wherein

the pixel signal line is connected by switching means to a reference potential bus line for externally supplying the reference potential into the device, and the switching means is configured to operate together with at least one of the first, second and third vertical scanning lines.

10. The liquid crystal display device according to any one of preceding claims 3 to 8, wherein

a time interval between the writing operations for the pixel electrode is shorter than the time interval between the writing operation for the control capacitor element.

11. The liquid crystal display device according to any one of preceding claims 4 to 10, wherein

a time interval between changes of the potential on the pixel signal line between the opposite sides of the potential on the opposite substrate is longer than a time interval between the writing operations for the pixel electrode.

12. The liquid crystal display device according to any one of preceding claims 1 to 11, wherein

the pixel electrode for one pixel is divided into a plurality of pixel electrodes, and first switching means connected to the first vertical scanning line and the horizontal scanning line, the control capacitor element for holding the control signal on the horizontal scanning line connected to the switching means, and the second switching means for writing the potential of the pixel signal to the pixel electrode are provided for each of the pixel electrodes.

13. The liquid crystal display device according to claim 12, wherein

at least one of the plurality of divided pixel electrodes has an area different from those of the other pixel electrodes.

14. The liquid crystal display device according to any one of preceding claims 1 to 13, wherein

the pixel electrode is formed of a metal film, and is of a reflection type.

FIG. 1

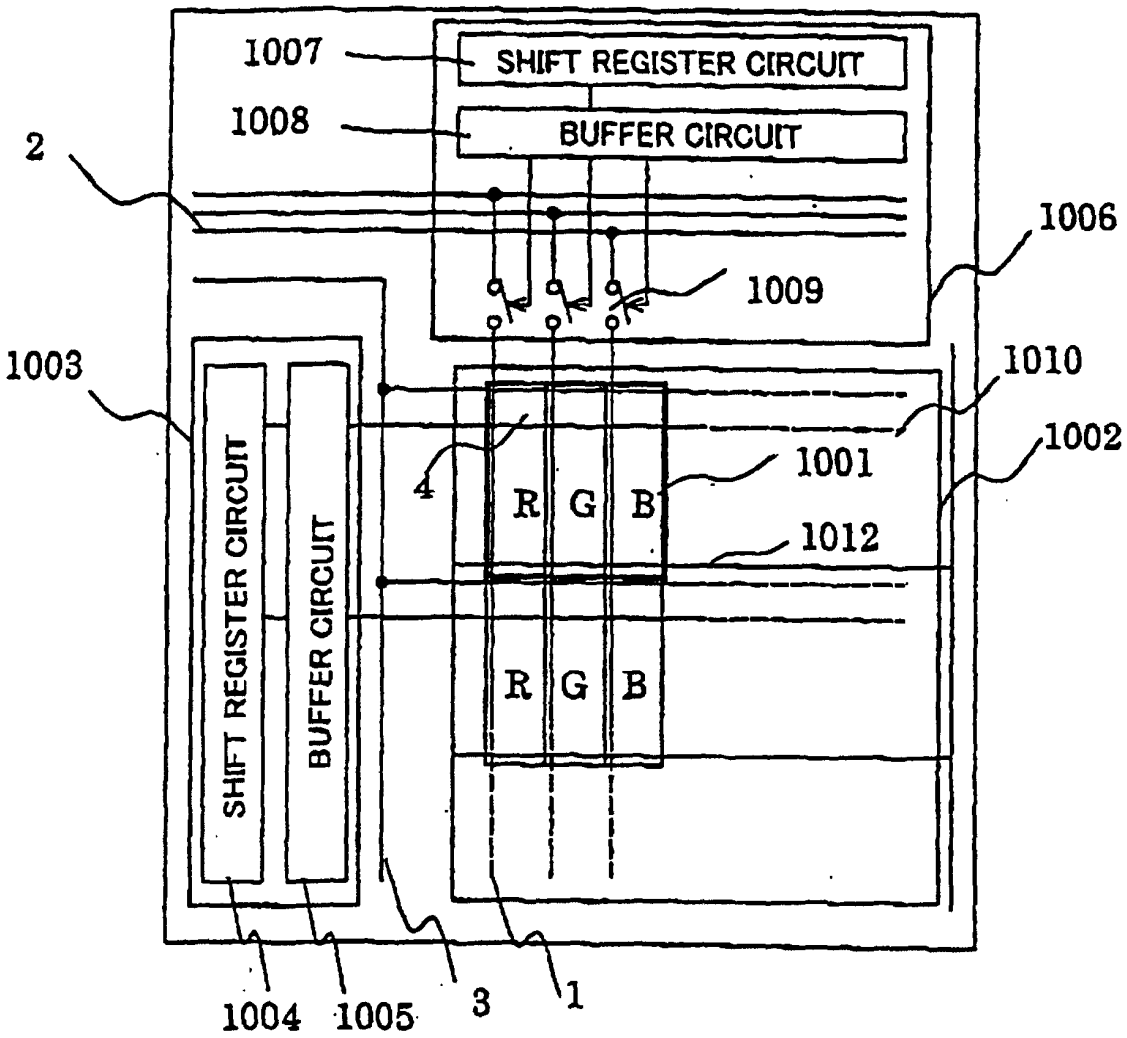

1007
SHIFT REGISTER CIRCUIT
1008
BUFFER CIRCUIT
2
1006
1009
1003
1010
1002
1001
4
R G B
1012
R G B
SHIFT REGISTER CIRCUIT
BUFFER CIRCUIT
1004
1005
3
1

FIG. 2(a)

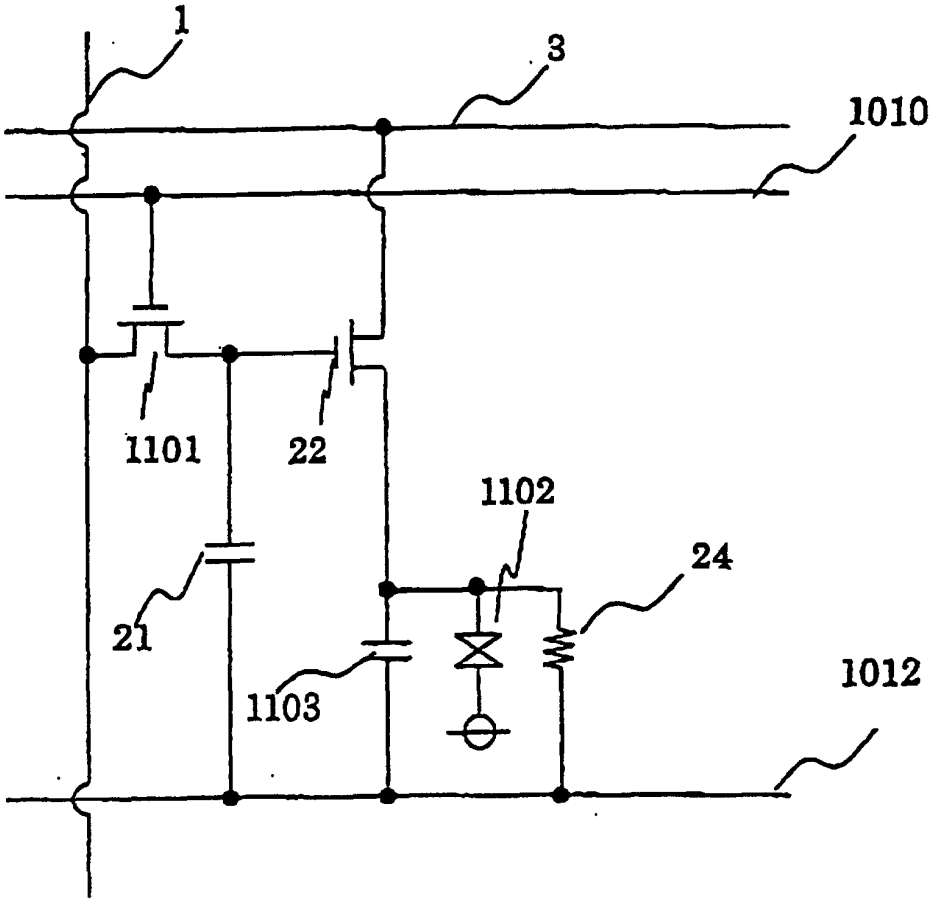


FIG. 2(b)

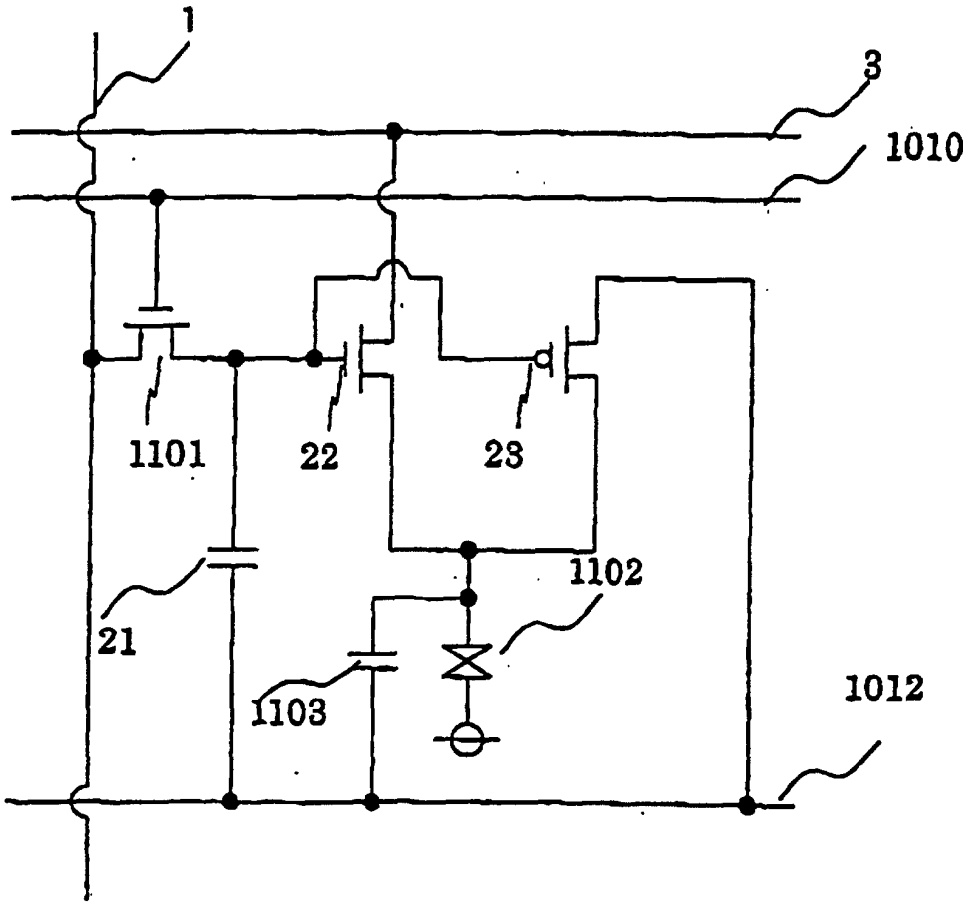


FIG. 3

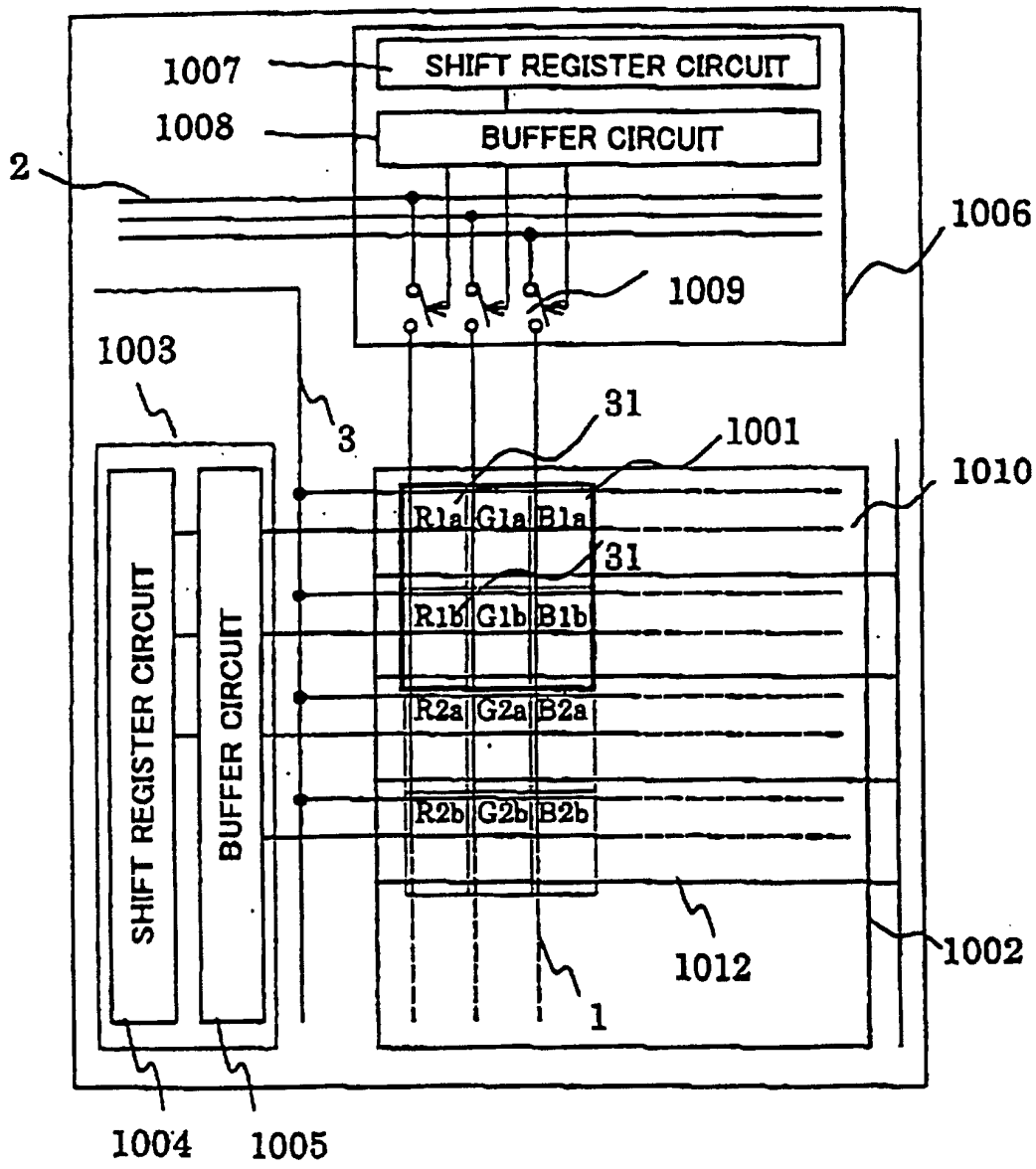

1007
SHIFT REGISTER CIRCUIT
1008
BUFFER CIRCUIT
2
1006
1009
1003
3
31
1001
1010
R1a G1a B1a
31
R1b G1b B1b
R2a G2a B2a
R2b G2b B2b
SHIFT REGISTER CIRCUIT
BUFFER CIRCUIT
1012
1002
1
1004
1005

FIG. 4

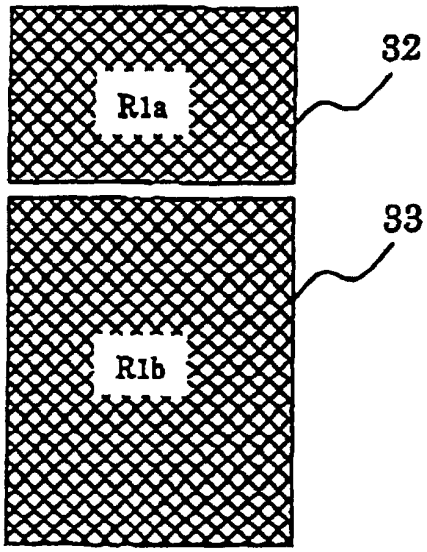


FIG. 5

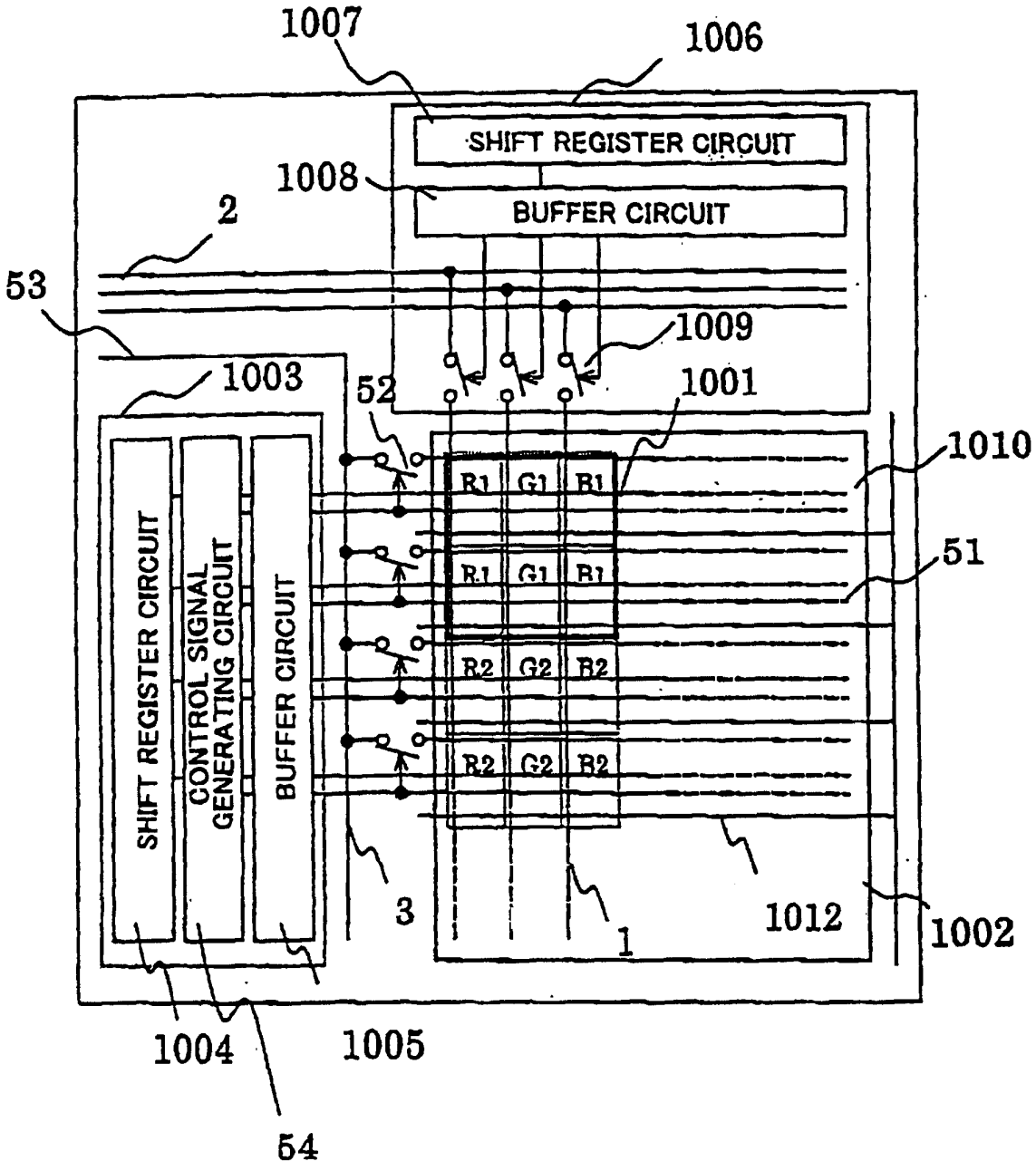

1007
1006
SHIFT REGISTER CIRCUIT
1008
BUFFER CIRCUIT
2
53
1009
1003
52
1001
1010
R1 G1 B1
R1 G1 B1
51
R2 G2 B2
R2 G2 B2
SHIFT REGISTER CIRCUIT
CONTROL SIGNAL GENERATING CIRCUIT
BUFFER CIRCUIT
3
1
1012
1002
1004
1005
54

FIG. 6

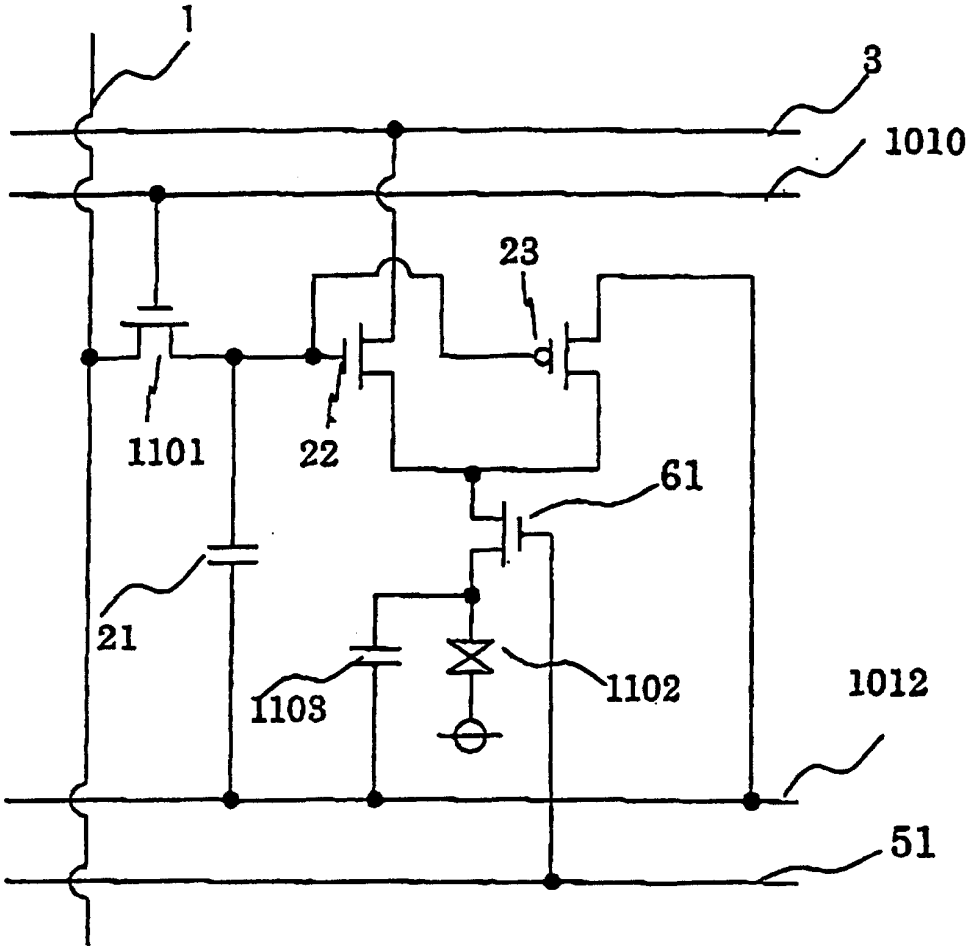


FIG. 7

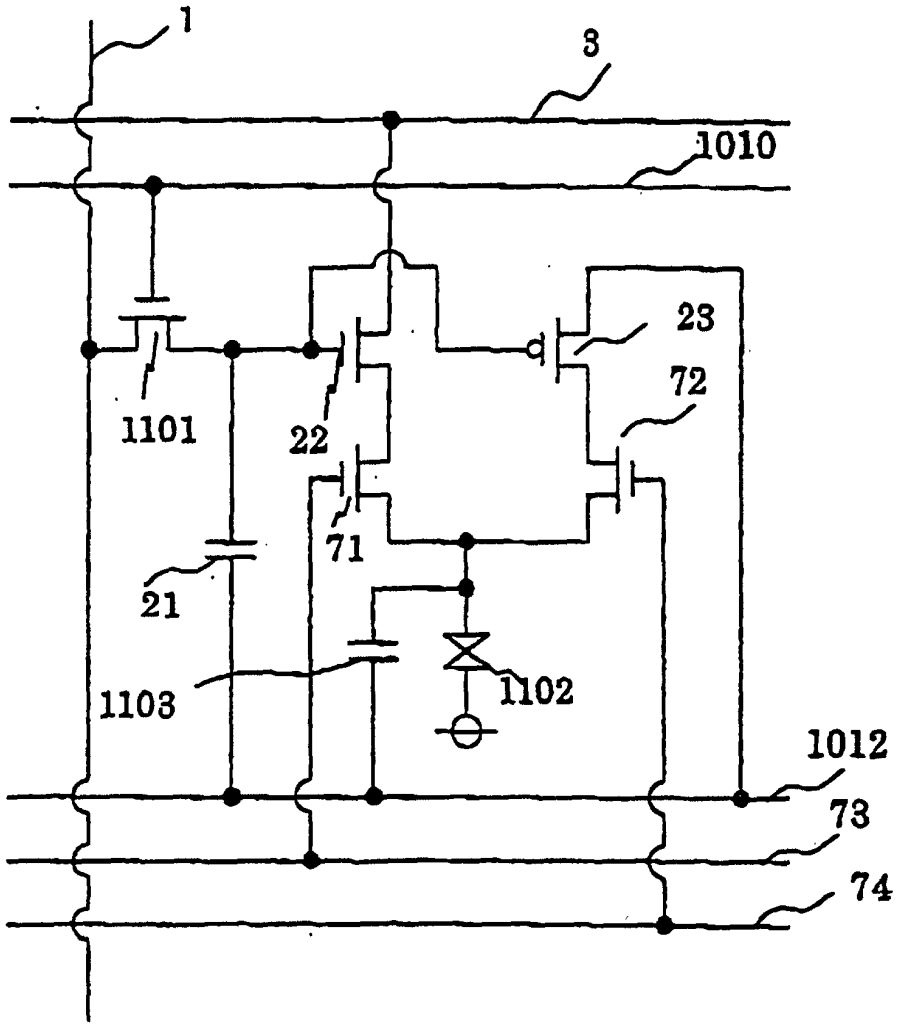


FIG. 8

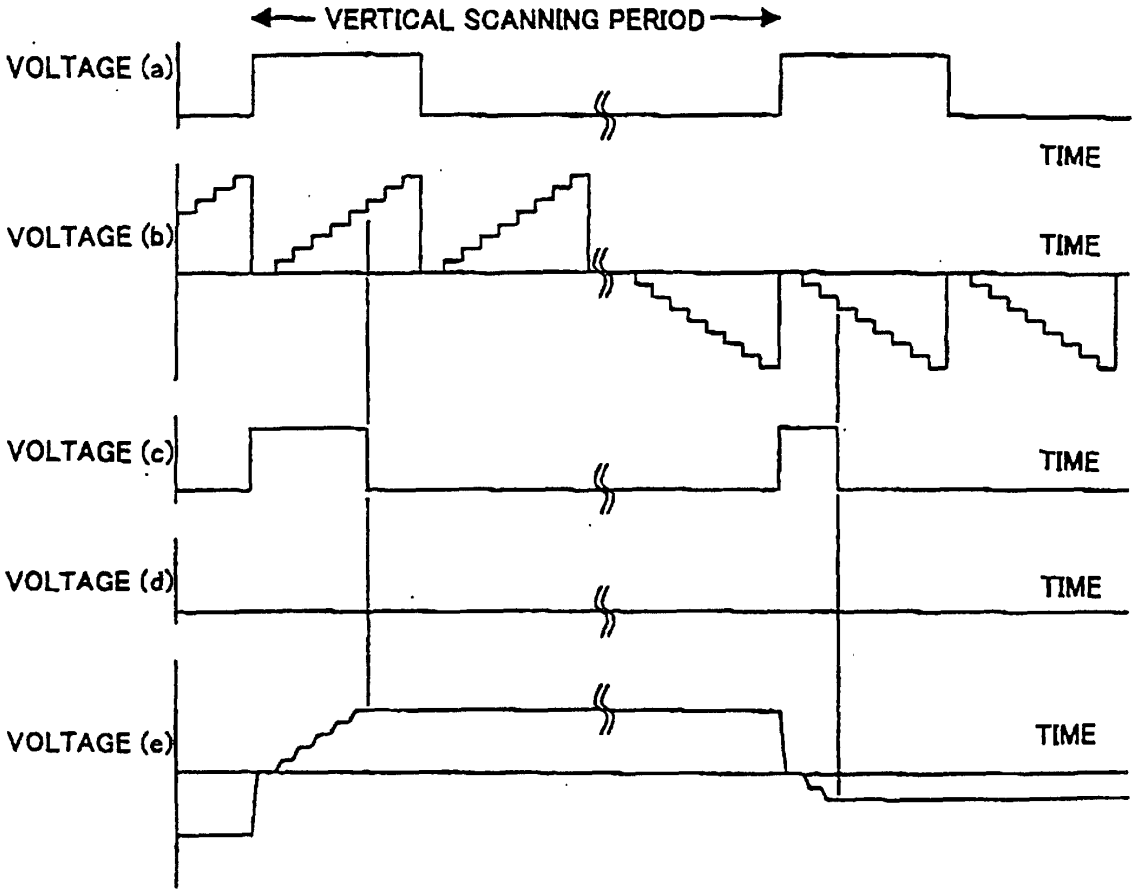

VERTICAL SCANNING PERIOD
VOLTAGE (a)
TIME
VOLTAGE (b)
TIME
VOLTAGE (c)
TIME
VOLTAGE (d)
TIME
VOLTAGE (e)
TIME

FIG. 9

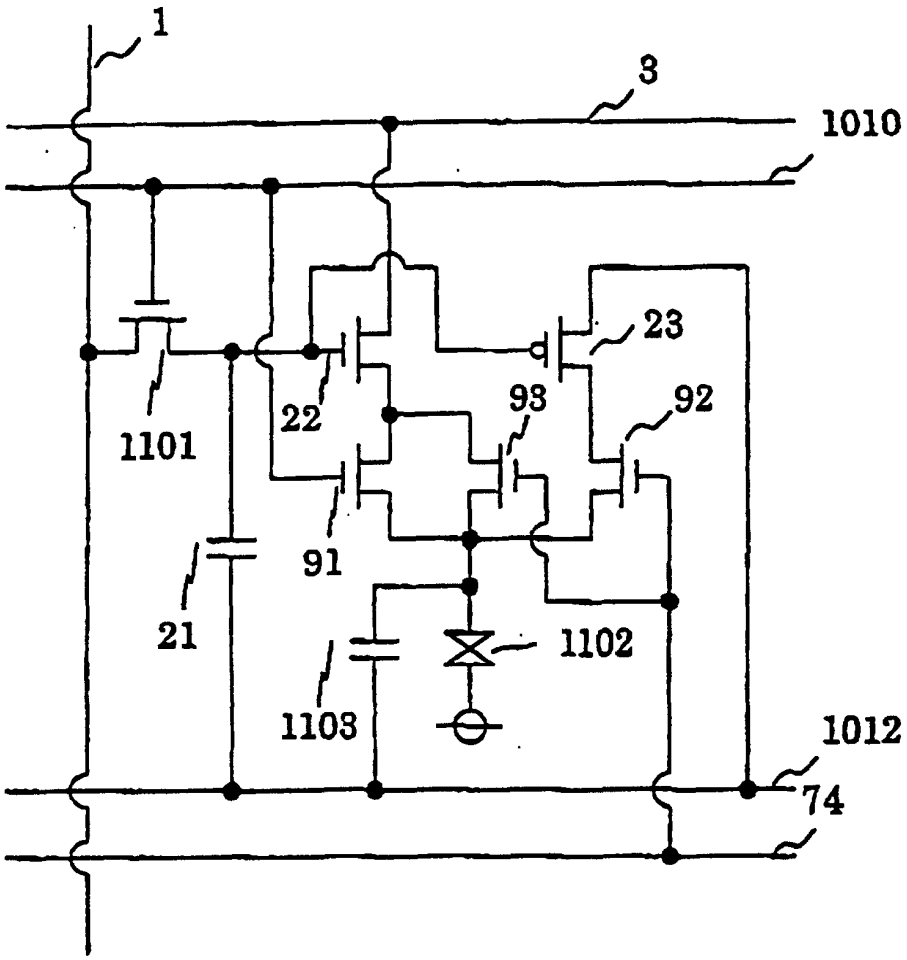


FIG. 10

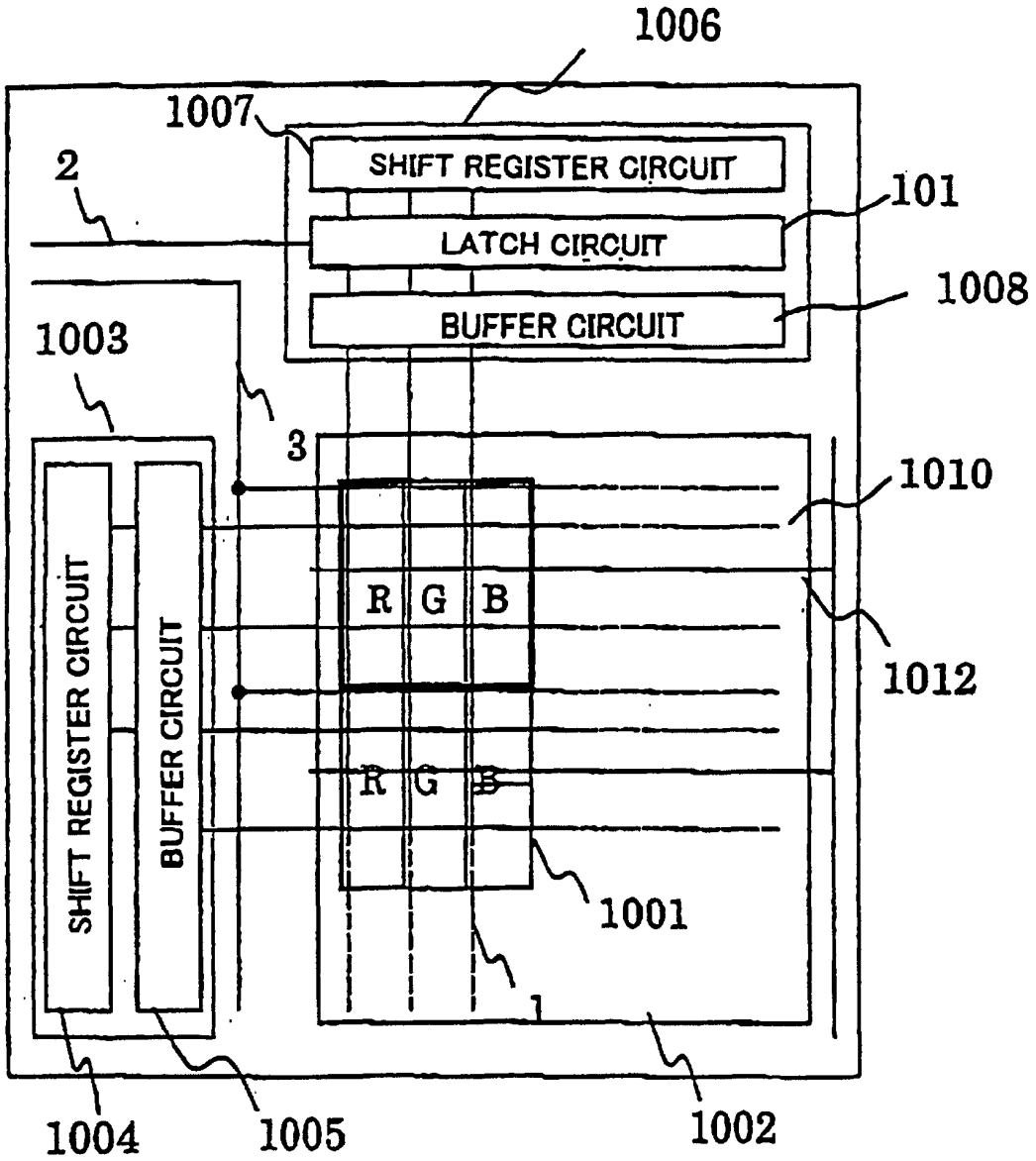

1006
1007
SHIFT REGISTER CIRCUIT
2
101
LATCH CIRCUIT
1008
BUFFER CIRCUIT
1003
3
1010
R G B
1012
R G B
SHIFT REGISTER CIRCUIT
BUFFER CIRCUIT
1001
1
1004
1005
1002

FIG. 11

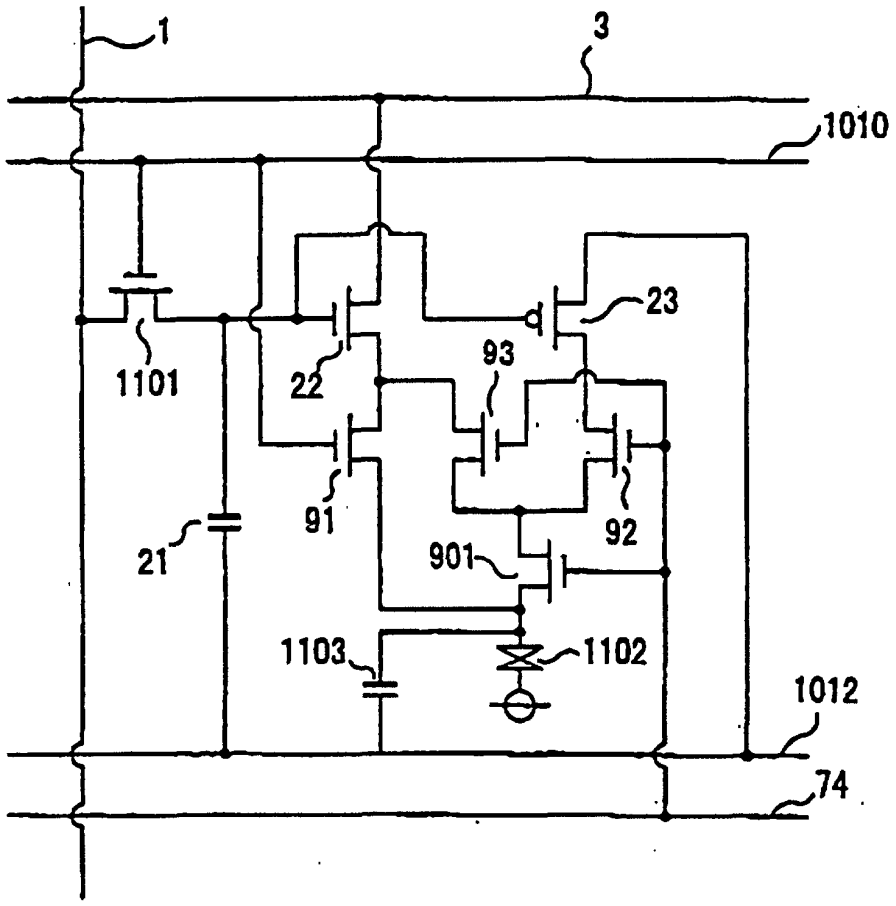


FIG. 12

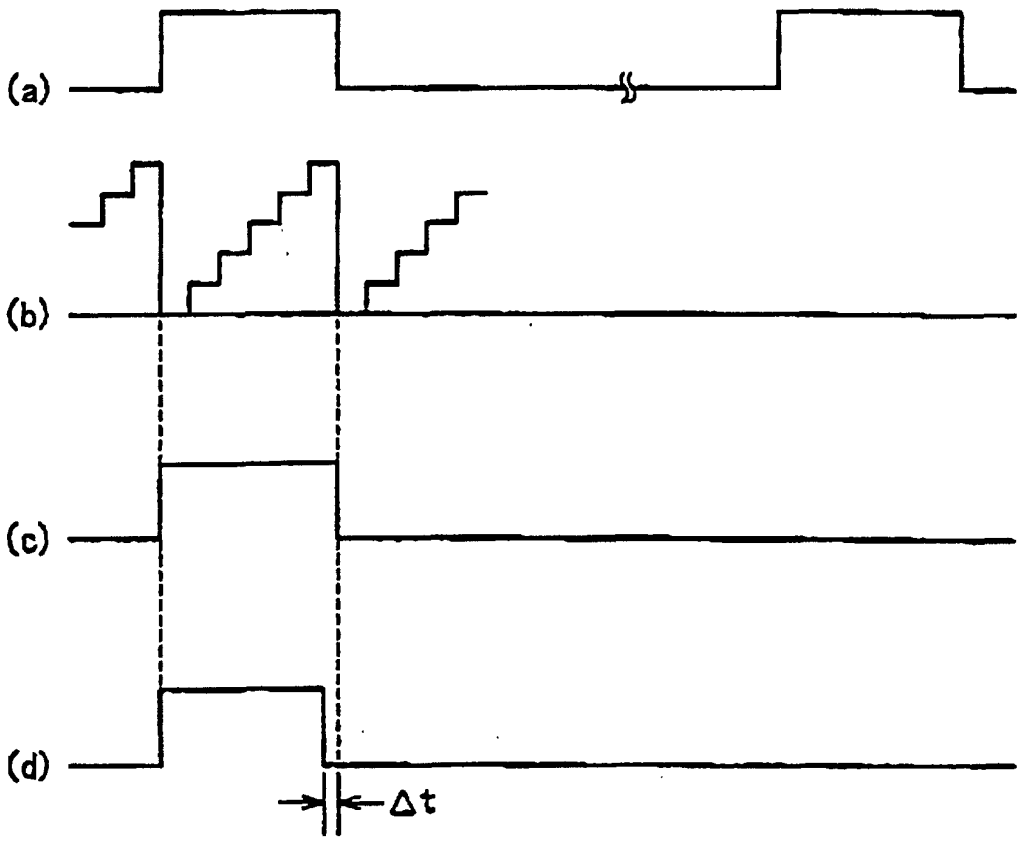


FIG. 13

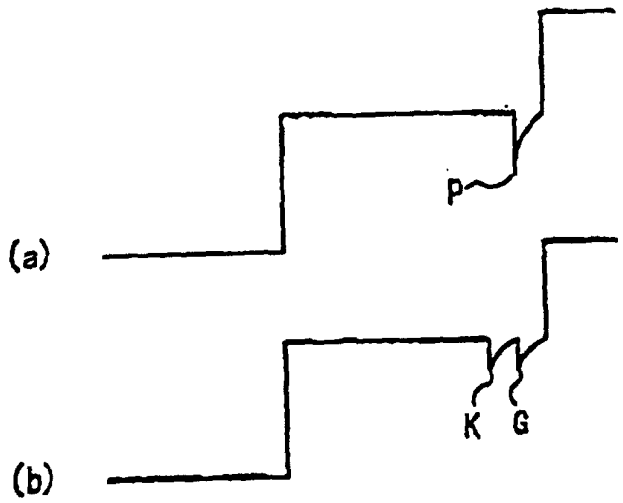


FIG. 14

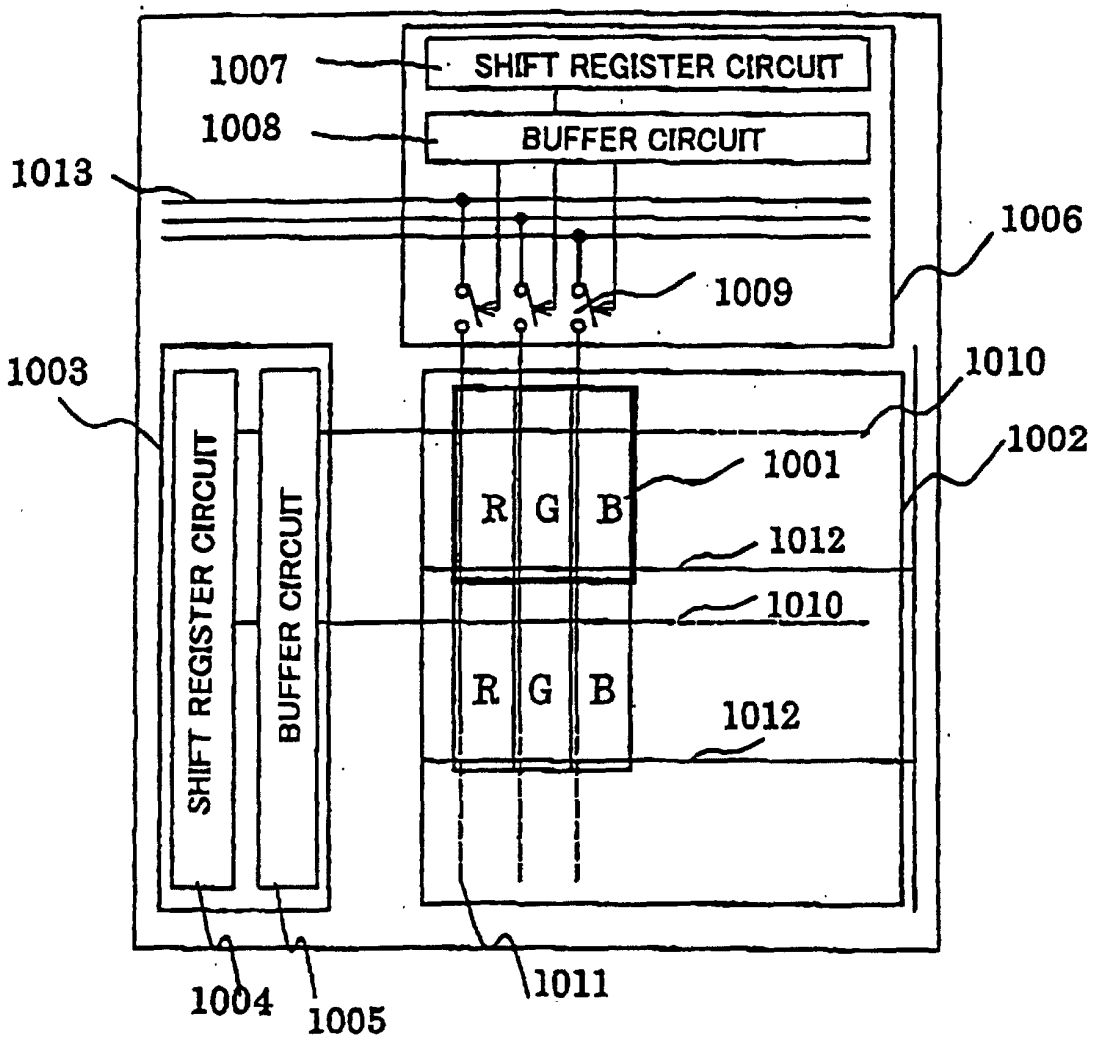

1007
SHIFT REGISTER CIRCUIT
1008
BUFFER CIRCUIT
1013
1006
1009
1003
1010
1002
1001
R G B
1012
1010
R G B
1012
SHIFT REGISTER CIRCUIT
BUFFER CIRCUIT
1004
1005
1011

FIG. 15

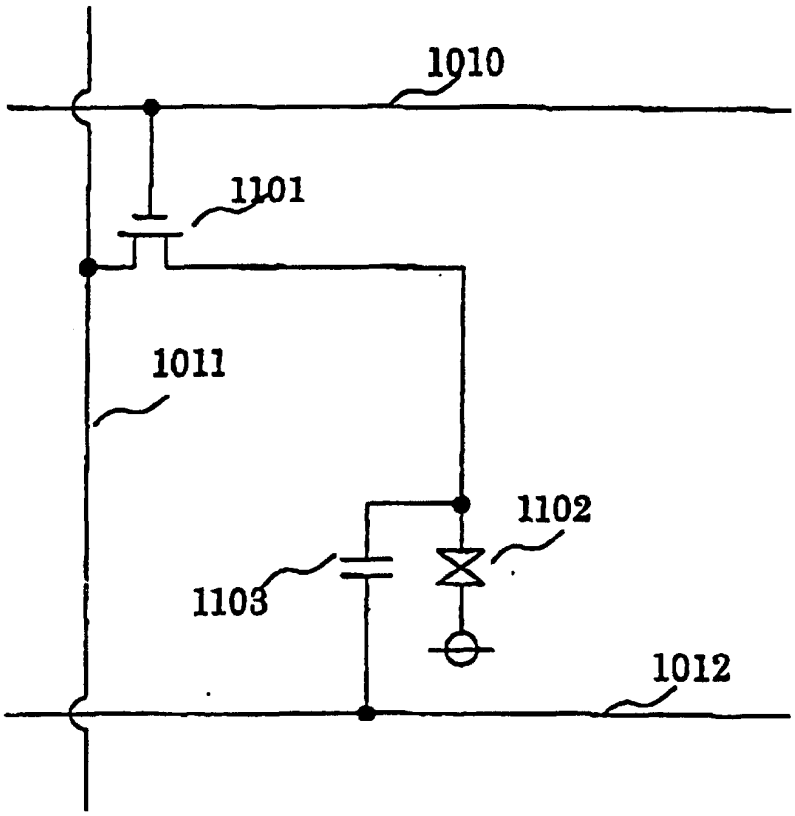


FIG. 16(a)

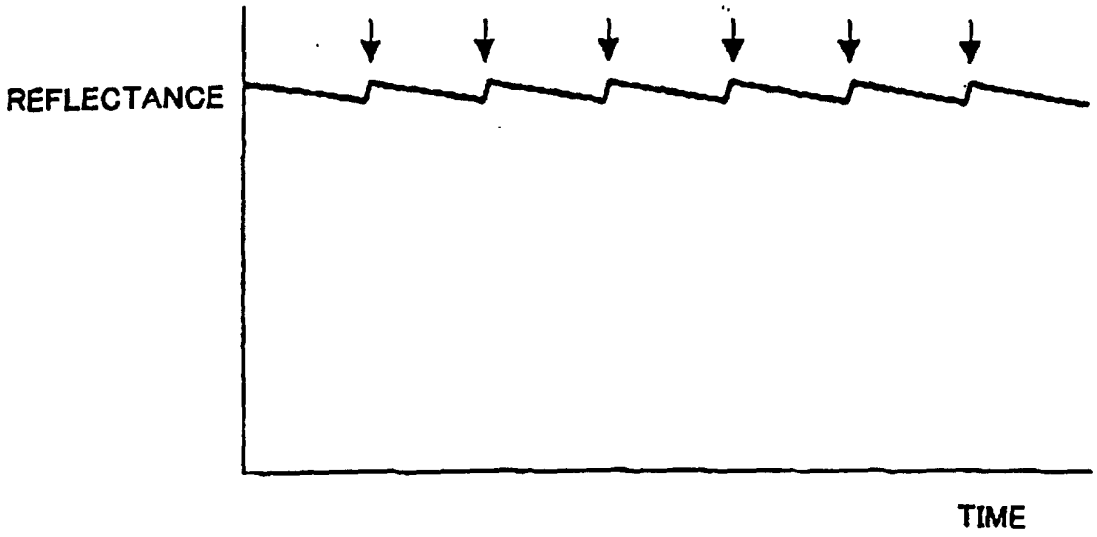
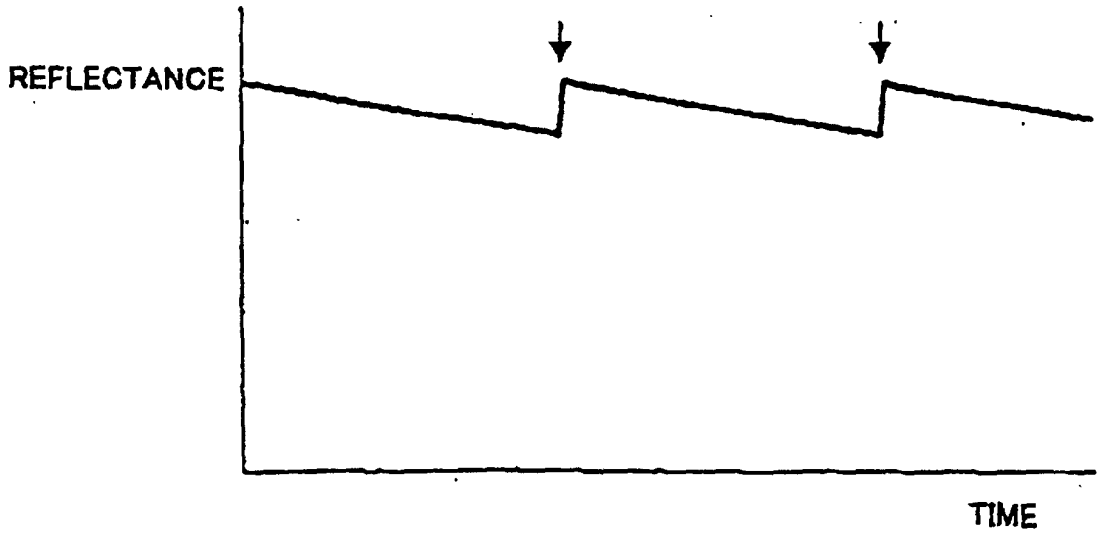


FIG. 16(b)



INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP00/08477

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl[7] G02F1/1368, G02F1/133, G09G3/36

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl[7] G02F1/1368, G02F1/133, G09G3/36

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1922-1996 Toroku Jitsuyo Shinan Koho 1994-2000
Kokai Jitsuyo Shinan Koho 1971-2000 Jitsuyo Shinan Toroku Koho 1996-2000

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP, 11-160676, A (Hitachi, Ltd.), 18 June, 1999 (18.06.99), Full text; all drawings (Family: none)	1-14
X	JP, 5-173175, A (Toshiba Corporation), 13 July, 1993 (13.07.93), Full text; all drawings (Family: none)	1-3,7-14
X	US, 5627557, A1 (Sharp Kabushiki Kaisha), 06 May, 1997 (06.05.97), Full text; all drawings & DE, 69324316, C & EP, 586155, A2 & JP, 6-118912, A & KR, 9709538, B	1-3,7-14
X	WO, 99/48078, A1 (Seiko Epson Corporation), 23 September, 1999 (23.09.99), Full text; all drawings & JP, 11-272233, A	1-3,7-14
X	JP, 11-326946, A (NEC Corporation), 26 November, 1999 (26.11.99), Full text; all drawings (Family: none)	1-3,7-14

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 February, 2001 (19.02.01)	06 March, 2001 (06.03.01)
Name and mailing address of the ISA/ Japanese Patent Office	Authorized officer
Facsimile No.	Telephone No.

Form PCT/ISA/210 (second sheet) (July 1992)

专利名称(译)	液晶显示器		
公开(公告)号	EP1174758A1	公开(公告)日	2002-01-23
申请号	EP2000979031	申请日	2000-11-30
[标]申请(专利权)人(译)	三菱电机株式会社		
申请(专利权)人(译)	三菱电机株式会社		
当前申请(专利权)人(译)	三菱电机株式会社		
[标]发明人	MURAI HIROYUKI MITSUBISHI DENKI KABUSHIKI KAISHA		
发明人	MURAI, HIROYUKI MITSUBISHI DENKI KABUSHIKI KAISHA		
IPC分类号	G02F1/133 G09G3/20 G09G3/36 G02F1/1368		
CPC分类号	G09G3/2011 G02F1/13306 G09G3/2074 G09G3/2077 G09G3/3648 G09G3/3659 G09G2300/0809 G09G2300/0842 G09G2300/0876 G09G2310/0259 G09G2320/0209 G09G2320/0247 G09G2330/021 G09G2330/08		
优先权	1999344832 1999-12-03 JP		
其他公开文献	EP1174758A4		
外部链接	Espacenet		

摘要(译)

一个目的是提供一种液晶显示装置，其可以在保持显示质量的同时以低功耗驱动。一种液晶显示装置，包括多个第一垂直扫描线和多个水平扫描线，所述多条水平扫描线以矩阵形式形成在基板上。第一开关装置连接到水平扫描线并且可由第一垂直扫描线控制;控制电容器元件，用于在连接到第一开关装置的水平扫描线上保持控制信号;第二开关装置，用于将像素信号线和像素电极连接在一起，将像素信号线上的电位写入像素电极，第二开关装置连接到控制电容元件。

FIG. 2(a)