(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 166 174 B1

(12) EUROPEAN PATENT SPECIFICATION

(45) Date of publication and mention of the grant of the patent:
16.04.2003 Bulletin 2003/16

(21) Application number: **00985051.2**

(22) Date of filing: **15.11.2000**

(51) Int Cl.7: **G02F 1/1362**, G02F 1/1368

(86) International application number:
PCT/EP00/11410

(87) International publication number:
WO 01/040856 (07.06.2001 Gazette 2001/23)

(54) ACTIVE MATRIX SUBSTRATE FOR LIQUID CRYSTAL DISPLAY AND METHOD FOR MAKING THE SAME

AKTIV-MATRIX-SUBSTRAT FÜR FLÜSSIGKRISTALLANZEIGE UND DESSEN HERSTELLUNGSVERFAHREN

SUBSTRAT DE MATRICE ACTIVE POUR AFFICHAGE A CRISTAUX LIQUIDES ET PROCEDE DE FABRICATION DE CEUX-CI

(84) Designated Contracting States:
DE FR GB NL

(30) Priority: **01.12.1999 GB 9928353**

(43) Date of publication of application:
02.01.2002 Bulletin 2002/01

(73) Proprietor: **Koninklijke Philips Electronics N.V.**
5621 BA Eindhoven (NL)

(72) Inventors:
- **BATTERSBY, Stephen, J.**
  NL-5656 AA Eindhoven (NL)
- **DEANE, Steven, C.**
  NL-5656 AA Eindhoven (NL)

(74) Representative: **Sharrock, Daniel John**
Philips
Corporate Intellectual Property
Cross Oak Lane
Redhill, Surrey RH1 5HA (GB)

(56) References cited:
US-A- 4 759 610

- **PATENT ABSTRACTS OF JAPAN vol. 1998, no. 12, 31 October 1998 (1998-10-31) & JP 10 186408 A (SAMSUNG ELECTRON CO LTD), 14 July 1998 (1998-07-14) & US 6 057 896 A (LEE JUNG-HO ET AL) 2 May 2000 (2000-05-02)**
- **PATENT ABSTRACTS OF JAPAN vol. 016, no. 568 (P-1458), 9 December 1992 (1992-12-09) & JP 04 219736 A (SHARP CORP), 10 August 1992 (1992-08-10) cited in the application**

Note: Within nine months from the publication of the mention of the grant of the European patent, any person may give notice to the European Patent Office of opposition to the European patent granted. Notice of opposition shall be filed in a written reasoned statement. It shall not be deemed to have been filed until the opposition fee has been paid. (Art. 99(1) European Patent Convention).

Printed by Jouve, 75001 PARIS (FR)

Description

[0001] This invention relates to active matrix liquid crystal displays, and particularly to a transistor substrate suitable for use in the manufacture of such a display. The invention particularly concerns transistor substrates for liquid crystal displays which provide a transistor and an associated charge storage capacitor for each pixel of the display. Thin film transistors (TFTs) are commonly employed in active matrix liquid crystal displays.

[0002] There is much interest in improving arrays of TFTs which are used to form the switching elements for flat panel liquid crystal displays. These TFT devices may be fabricated with portions of an amorphous or polycrystalline semiconductor film to form the body of the transistor devices. The thin film transistors define insulated gate structures, and it is known for the gate insulator to extend to the storage capacitor to form the dielectric of that capacitor.

[0003] It is also known to provide a two-layer gate insulating structure. This enables the insulating layer adjacent the semiconductor body of the transistor to be patterned together with the patterning of the semiconductor body of the transistor. The electrical properties of the interface between the semiconductor layer and the adjacent gate insulator layer are improved. For example, in the case of a top-gate TFT, the lower gate insulator layer is deposited over the silicon layer which is to define the transistor body, before the silicon layer is patterned to form the silicon regions of the individual TFTs.

[0004] It is also known for only one of the gate insulator layers to extend to the charge storage capacitor of the pixel to define the dielectric layer, and this enables the thickness of the gate insulator and the thickness of the capacitor dielectric layer to be set independently. JP-A-4-219736 discloses a transistor-capacitor arrangement of this type.

[0005] One problem with the use of a two-layer gate insulating structure, with the two layers patterned differently, is that separate vacuum deposition processes are required, giving rise to additional processing steps in the manufacture of the transistor substrate. JP-A-10-186408 discloses a two-layer gate insulating structure comprising a silicon nitride layer and a flowable insulating layer.

[0006] The present invention is directed at a liquid crystal display comprising a plurality of pixels each comprising a switching transistor, a storage capacitor of capacitance $C_{store,}$ and a pixel capacitor of capacitance C_{LC}, the transistors comprising insulated-gate staggered structures having substantially coplanar source and drain regions and a gate region, a gate insulator lying between the gate region and the source and drain regions, the storage capacitor comprising a stacked structure of two electrodes separated by a capacitor dielectric, wherein the gate insulator comprises first and second layers, of which layers only the second extends to the storage capacitor to define the capacitor dielectric. According to the invention, the thickness of the first layer d_1 and the thickness of the second layer d_2 are selected approximately to satisfy the relation:

$$d_2 = (C_{store}/C_{LC}) \,.\, (\varepsilon_2/\varepsilon_1) \,.\, d_1$$

in which ε_1 and ε_2 are the permittivity constants of the first and second layers, respectively.

[0007] The use of a polymer or spin-on glass layer as the second gate insulator layer avoids the need for two vacuum deposition steps in the production of the gate insulator structure.

[0008] One possible problem with the use of a polymer or spin-on glass layer is that the uniformity of the film is less accurately controllable than for inorganic layers deposited using vacuum processes. Therefore, the thickness of the first and second layers are selected in accordance with the invention such that the charging time constant of each pixel of the liquid crystal display is substantially independent of thickness variations in the polymer or spin-on glass layer.

[0009] The use of a polymer gate insulating layer has been described in GB 2311653.

[0010] The present invention is also directed at a method of manufacturing a liquid crystal display, comprising: providing an array of transistors and storage capacitors over a substrate, the transistors comprising insulated-gate staggered structures having substantially coplanar source and drain regions and a gate region, a gate insulator lying between the gate region and the source and drain regions, and the storage capacitors comprising a stacked structure of two electrodes separated by a capacitor dielectric, wherein the gate insulator is deposited as first and second layers, deposited by vacuum deposition process, and the second gate insulator layer is deposited by a non-vacuum process, the first layer being patterned to remove it from areas corresponding to the storage capacitors, and the second layer extending. to the areas corresponding to the storage capacitors to define the capacitor dielectric, and providing liquid crystal material over the substrate, wherein the first layer is deposited to a thickness d_1, the second layer is deposited to a thickness d_2, the capacitors have capacitance C_{store} and each pixel forms a pixel capacitor of capacitance C_{LC}. According to the invention the thicknesses of the first and second layers selected approximately to satisfy the relation:

$$d_2 = (C_{store}/C_{LC}) \,.\, (\varepsilon_2/\varepsilon_1) \,.\, d_1$$

in which ε_1 and ε_2 are the permittivity constants of the first and second layers, respectively.

[0011] Preferably, the first gate insulator layer is deposited by vacuum deposition process, and the second gate insulator layer is deposited by a non-vacuum process. The use of a non-vacuum process for one of the gate insulator layers simplifies the manufacturing process.

[0012] A liquid crystal display device and embodiments of the invention will now be described by way of example with reference to the accompanying drawings, in which:

Figure 1 shows in plan view a pixel of a known liquid crystal display device incorporating a transistor-capacitor arrangement using a top gate transistor;
Figure 2 illustrates the components of a liquid crystal display pixel, for explaining the operation of the display device;
Figure 3 shows a cross-section through a liquid crystal display taken along the line X-X in Figure 1, and showing a known arrangement;
Figure 4 shows a transistor substrate using top gate transistors, for use in a liquid crystal display according to the invention;
Figure 5 illustrates the operating characteristics of a thin film transistor; and
Figure 6 shows a transistor substrate using bottom gate transistors, for use in a liquid crystal display according to the invention.

[0013] It should be noted that these figures are diagrammatic and not drawn to scale. Relative dimensions and proportions of parts of these figures have been shown exaggerated or reduced in size, for the sake of clarity and convenience in the drawings.

[0014] By way of example, Figure 1 shows the whole area of one pixel of a known active matrix display device, to which the invention may be applied. A pixel comprises an electrode pattern 11 and 12 of, for example, ITO formed on an insulating substrate 10. The substrate 10 may comprise a back plate of the display, for example a glass plate or polymer film. Column conductors 11 of the pattern 11, 12 form common source lines of the switching TFTs in the matrix columns. Another part 12a of the pattern 11, 12 forms a drain electrode of the TFT. In this particular example, the bulk of part 12 of the pattern 11, 12 forms a pixel electrode 12b. This pixel electrode 12b is integral with the drain electrode part 12a and also, in this example, with a part 12c which forms the bottom electrode of a pixel storage-capacitor, the top electrode being defined by a row conductor 25 of a neighbouring pixel.

[0015] The row conductors 25 form common gate lines of the TFTs in the rows. The switching TFT of each cell comprises a silicon transistor body 20a. In the example of Figure 1, these bodies 20a are in the form of separate islands of a silicon film pattern. Typically, the silicon film 20 is of, for example, amorphous silicon. However, rather than amorphous silicon, polycrystalline silicon may be preferred for some displays.

[0016] Liquid crystal material is provided over the transistor substrate, the components of which are shown in Figure 1. Above the liquid crystal material, an additional substrate is provided defining a ground plane. This will be illustrated in further detail below.

[0017] Figure 2 shows the electrical components which make up the pixels shown in Figure 1. The row conductor 25 is connected to the gate of the TFT 30, and the column electrode 11 is coupled to the source electrode, as explained with reference to Figure 1. The liquid crystal material provided over the pixel effectively defines a liquid crystal cell 32 which extends between the drain of the transistor 30 and a common ground plane 34. The pixel storage capacitor 36 is connected between the drain of the transistor 30 and the row conductor 25a associated with the next row of pixels.

[0018] During operation of the display device, signals are applied to rows of pixels in turn. In order to address a row of pixels, an appropriate signal is applied to the associated row conductor 25 to turn on the transistors 30 of the row of pixels. This enables a display signal applied to the column conductor 11 to be fed to the liquid crystal cell 32, which results in charging of the liquid crystal cell to the desired voltage. The storage capacitor 36 is also charged and is provided to ensure that the signal on the liquid crystal cell 32 remains constant even after the addressing of that particular row has been completed, and the transistors 30 have been turned off. During addressing of the row of pixels, the row conductor 25a of the subsequent row of pixels is held at ground potential so that the storage capacitor 36 is charged to a voltage corresponding to that which is to be applied across the liquid crystal cell 32.

[0019] When the next row of pixels is addressed, there will be an increase in the voltage of the row conductor 25a, which will feed through the capacitor 36 by capacitive coupling to the liquid crystal cell 32. However, this increased voltage on the next row conductor 25a only lasts for one row address period, after which that row conductor 25a returns to ground. The liquid crystal material has slower response time and does not respond to these instantaneous voltage changes.

[0020] Figure 3 shows a known structure for a liquid crystal display, shown in cross section through the line X-X in Figure 1, which uses top gate TFTs. The manufacture of the known liquid crystal display shown in Figure 3 will now be described. A source and drain electrode pattern 11, 12 is provided on the substrate 10. For example, an ITO conductor layer may be deposited on a glass substrate 10, and wet etching may be performed in order to define the source and drain electrode pattern. A silicon film 20 is deposited on the source and drain electrode pattern 11, 12 to provide the transistor body 20a comprising the channel area 20c of the TFT. A first gate insulator layer 40 is provided over the semiconductor layer 20, and the first gate insulator layer 40 and the semiconductor layer 20 are patterned using the same mask to define the semiconductor island forming the transistor body 20a. The deposition of the first gate insulator layer 40 over the semiconductor layer 20 before patterning of the semiconductor 20 improves the electrical characteristics of the interface between the insulator layer 40 and the semiconductor layer 20.

[0021] A second, upper gate insulating layer 42 is then deposited over the array and a gate conductor 44 is provided over the upper gate insulator 42. The upper gate insulator layer 42 extends beyond the body of the transistor and defines the dielectric layer for the storage capacitor 36. This storage capacitor 36 is defined by the next row conductor 25a and a portion 12c of the drain electrode 12.

[0022] These layers complete the transistor substrate for the liquid crystal display. A layer of liquid crystal material 50 is provided over the transistor substrate, and a further substrate 52 overlies the layer of liquid crystal material. This further substrate 52 may be provided on one face with an arrangement of colour filters 54 and a plate defining the common electrode 34. A polarising plate 56 is provided on the opposite side of the substrate 52.

[0023] The operation and construction of known liquid crystal displays will not be described in any further detail as this will be apparent to those skilled in the art.

[0024] A top gate thin film transistor is represented in Figure 3, but it is equally possible to utilise bottom gate thin film transistors. The application of the invention to transistor substrates using top gate TFTs will first be described, and then the application of the invention to transistor substrates using bottom gate TFTs will also be described. The gate 44 is shown in Figure 3 as having a width less than the spacing between the source and drain electrodes 11, 12. Some processing of the semiconductor layer 20 between the channel area 20c and the source and drain electrodes 11, 12 respectively is preferred to reduce the resistance of that part of the semiconductor layer. For example, the source and drain regions of the semiconductor layer may be doped, for example using plasma doping with the gate conductor 44 masking the underlying intrinsic semiconductor channel area 20c. Alternatively, the source and drain regions of the semiconductor layer 20 may be subjected to ion implantation using the top gate structure as an implantation mask. As a further alternative, the source and drain regions of the semiconductor layer may be treated to form silicide material, again to reduce the resistance to the source and drain electrodes.

[0025] Additional layers to those described may be provided. For example, a planarising film may be provided over the entire structure. Additionally, a further electrode pattern may be defined over this planarising layer which contacts the drain 12 through a well provided in the second insulator 42. All of these possibilities, and others, will be apparent to those skilled in the art.

[0026] Conventionally, the first gate insulator layer 40 comprises a first silicon nitride layer of thickness approximately 80nm, and the second gate insulator layer 42 comprises a second silicon nitride layer of much greater thickness, for example 250nm. Since these two layers are patterned differently, separate vacuum deposition processes, for example plasma chemical vapour deposition, are required to define the two layers.

[0027] Figure 4 shows a transistor substrate for use with the liquid crystal display according to the invention, and using top gate TFTs. The comments made in connection with Figure 3 concerning the possible alternatives to the transistor design apply equally to the liquid crystal display of the invention. The same reference numerals have been used in Figure 4 to denote the same components as those shown in Figure 3.

[0028] In the structure shown in Figure 4, the first gate insulator layer 400 comprises an inorganic layer, deposited by a vacuum deposition process. For example, this layer may comprise silicon nitride deposited by plasma enhanced chemical vapour deposition (PECVD). The second gate insulator layer 420, however, comprises a polymer or spin-on glass layer which is deposited by a non-vacuum process. This non-vacuum process may comprise spinning, rolling or spraying, and this reduces the cost of that processing step. One potential problem with the use of a polymer or spin-on glass insulator layer is that the thickness control and uniformity is likely to be worse than that of a PECVD layer.

[0029] For given geometry and bias conditions of the thin film transistor, the current output of the transistor is proportional to the gate dielectric capacitance, and hence the current output falls if the polymer or glass layer is made thicker. However, the total load capacitance (the storage capacitance 36 and the capacitance of the liquid crystal material 50 associated with the pixel) is also reduced as the polymer layer thickens. The overall charging time of the pixel is therefore fairly insensitive to thickness variations.

[0030] It is this property which is exploited in accordance with the invention. Figure 5 shows the voltage-current characteristics of a MOSFET. As shown, the current axis is normalised with respect to a constant K which is derived from the channel width W, the channel length L, the gate insulator permittivity ε, the gate insulator thickness d and the electron mobility μ_η (for an n-type MOSFET). For given transistor dimensions (i.e. W and L), this constant is proportional to the gate dielectric capacitance:

$$C = \frac{A\varepsilon}{d}$$

[0031] Consequently, the effective transistor resistance for any given set of bias conditions and dimensions may be considered to vary inversely proportionally with respect to the gate capacitance C. For the double layer gate insulator the gate capacitance is given by :

$$\frac{1}{C_{gate}} = \frac{1}{C_1} + \frac{1}{C_2}$$

$$= \frac{d_1}{A\varepsilon_1} + \frac{d_2}{A\varepsilon_2}$$

$$C_{gate} = \frac{A\varepsilon_1\varepsilon_2}{d_1\varepsilon_2 + d_2\varepsilon_1}$$

in which d_1 and d_2 are the thicknesses of the first and second insulating layers, and ε_1 and ε_2 are their permittivity constants.

[0032] The transistor resistance is inversely proportional to the gate capacitance, and is thereby given by:

$$R_{TFT} \propto \frac{d_1\varepsilon_2 + d_2\varepsilon_1}{A\varepsilon_1\varepsilon_2}$$

[0033] For given insulator layers (i.e. ε_1 and ε_2 are constants) but with selectable thickness, the transistor resistance varies in proportion with:

$$R_{TFT} \propto d_1\varepsilon_2 + d_2\varepsilon_1$$

[0034] To evaluate the time constant for the TFT-capacitor pixel, the combined capacitance of the LC cell 32 and the storage capacitor 36 needs to be considered. The total pixel capacitance is:

$$C_{LC} + C_s = C_{LC} + \frac{A_S\varepsilon_2}{d_2}$$

where C_{LC} is the capacitance of the liquid crystal material associated with the pixel, C_s is the storage capacitance, and A_s is the area of the storage capacitor. Consequently, the charging time constant of the pixel is proportional to:

$$\tau_{RC} \propto C_{LC}d_1\varepsilon_2 + A_s\varepsilon_1\varepsilon_2 + C_{LC}d_2\varepsilon_1 + \frac{\varepsilon_2^{\,2}A_Sd_1}{d_2}$$

[0035] This charging time constant is invariable to the capacitor dielectric thickness d_2 when the following equation is satisfied:

$$\frac{\partial}{\partial d_2}\tau_{RC} = 0$$

This yields:

$$d_2 = \frac{A_S\varepsilon_2}{d_2C_{LC}}\cdot\frac{\varepsilon_2}{\varepsilon_1}\cdot d_1$$

$$d_2 = \frac{C_S}{C_{LC}}\cdot\frac{\varepsilon_2}{\varepsilon_1}\cdot d_1$$

[0036] This analysis enables the thickness of the two insulator layers to be selected such that variations in the thickness of the capacitor dielectric do not alter the charge timing constant of the pixel and thereby do not change the display operating characteristics. The kick-back behaviour is also invariant to small changes in thickness of the spin on or glass layer.

[0037] Figure 6 shows a transistor substrate for use with the liquid crystal display according to the invention, and using bottom gate TFTs. A gate electrode pattern 60 is provided on the substrate 10, and which also defines the lower terminal 37 of the storage capacitor 36. The gate of the transistor again forms part of the respective row conductor, and the lower terminal 37 of the storage capacitor may form part of the row conductor for the next adjacent row of pixels. For example, a conductor layer may be deposited on a glass substrate 10, and wet etching may be performed in order to define the conducting pattern.

[0038] The polymer or spin-on gate dielectric layer 420 is then deposited. For the sake of clarity, and consistency with the equations given above, this dielectric layer shall be referred to again as the "second" gate dielectric layer, and has thickness d_2. This second gate insulator layer 420 again extends beyond the body of the transistor, and defines the dielectric layer for the storage capacitor 36.

[0039] The first gate insulator layer 400 is then deposited comprising an inorganic material such as silicon nitride. The amorphous silicon layer 20 forming the body of the transistor is deposited before patterning of the first insulator layer 400, so that these two layers 20, 400 are patterned together using the same mask to define the semiconductor island forming the transistor body 20a. Again, this improves the electrical characteristics of the interface between the insulator layer 400 and the semiconductor layer 20.

[0040] It is preferred to have the semiconductor body of the transistor adjacent the inorganic gate dielectric layer, to enable a good quality interface. However, it may also be possible to implement the invention with the spin-on or polymer layer of the gate dielectric structure adjacent the semiconductor layer of the transistor.

[0041] An etch stop plug 62 is patterned overlying and aligned with the gate 60, and the source and drain electrodes 64,66 are then deposited. The layer defining the source and drain electrodes also defines the top contact 38 of the storage capacitor 36. In order for the display pixels to function in the same way as the pixel configuration described with reference to Figures 1 to 3, one of the source and drain needs to make contact with a respective column conductor, and the other needs to make contact with a liquid crystal contact pad and with the top contact of the storage capacitor 36. The possible ways of achieving this will be apparent to those skilled in the art. Of course, additional layers to those described may be required for this purpose.

[0042] Examples will now be given of the dimensions dictated by this approach for examples of gate insulator layers.

[0043] The relationship between the storage capacitor value and the capacitance of the liquid crystal cell is determined by the display design and type. For a transmissive display, the storage capacitor should be as small as possible, as it occupies aperture space of the display. For example, for an amorphous silicon transmissive display, C_{store}/C_{LC} may be as low as 1, whereas the ratio is likely to be nearer 3 for poly-silicon displays. For reflective displays, the storage capacitor can lie under the pixel without causing aperture loss, and ratios as high as 4 may be used.

[0044] The ratio of $\varepsilon_{poly}/\varepsilon_{inorg}$ depends on the dielectric layers chosen. Taking the first dielectric layer to be SiN, ε_{inorg} is about 6.4. ε_{poly} can take on a wide range of values. For example, Kapton is a commercially available form of polyimide which has a value of ε of about 3.4. A suitable spin-on polymer is Accuspin T-18, formulated by Allied Signal Advanced Microelectronic Materials (AMM), which has a dielectric constant of around 2.7. A range of values may be obtained using spin-on glass compositions. An example is the Accuglass P-TTY A Series family of phosphosilicate spin-on glasses from AMM. They exhibit dielectric constants of around 4.2.

[0045] As a result of these different possibilities, the required ratio of the thickness of the spin-on or glass layer to the inorganic layer will vary significantly as a function of the display and the materials selected. If polyimide and silicon nitride are selected the ratio will vary between approximately 0.5 and 2 depending on the type of display.

[0046] For example, if the liquid crystal capacitance and the charge storage capacitance have approximately equal values, which is approximately correct for a transmissive amorphous silicon display, the ratio of the insulator layer thicknesses must be inversely proportional to the ratio of their permittivity constants. Silicon nitride with permittivity of 6.4, and polyimide, of permittivity of 3.4, requires the polyimide insulator layer to have a thickness of approximately half of the thickness of the silicon nitride layer.

[0047] In this example, the thickness of the polymer layer may be impracticably thin, so a second insulator layer of higher permittivity constant is preferred, which may be achieved using glass insulators.

[0048] The combined thickness of the two dielectric layers (rather than the ratio of their individual thicknesses) may be selected to obtain desired transistor operating characteristics. For example, for a TFT with a single gate insulator layer of SiN, a typical thickness of 300 to 400nm is used. The double layer gate insulator dielectric may be designed to produce similar gate capacitance.

[0049] For given transistor dimensions, the gate capacitance of a silicon nitride gate insulator of 350nm thickness is:

$$C = \frac{A\varepsilon_1}{350x10^{-9}}$$

The gate capacitance of the double layer gate insulator is:

$$C = \frac{A\varepsilon_1\varepsilon_2}{d_1\varepsilon_2 + \frac{C_S}{C_{LC}}\varepsilon_2 d_2}$$

Equating these gives:

$$d_1 = \frac{350}{1+\frac{C_S}{C_{LC}}}nm$$

[0050] For the values above for polyimide and silicon nitride, and assuming equal storage and LC capacitance, d_1 is 175nm and d_2 is 93nm. Assuming the storage capacitance is 4 times the and LC capacitance, d_1 is 70nm and d_2 is 147nm. Of course, the thicknesses relate to the layer thicknesses in the gate region of the transistor, not elsewhere.

[0051] Various modifications to the specific layers used in the manufacture of the liquid crystal display will be apparent to those skilled in the art, which do not prohibit the use of the invention in those displays.

Claims

1. A liquid crystal display comprising a plurality of pixels each comprising a switching transistor (30), a storage capacitor (36) of capacitance C_{store}, and a pixel capacitor of capacitance C_{LC}, the transistors comprising insulated-gate staggered structures having substantiafly coplanar source and drain regions (11, 12; 64, 66) and a gate region (44; 62), a gate insulator (400, 420) lying between the gate region and the source and drain regions, and the storage capacitors (36) comprising a stacked structure of two electrodes separated by a capacitor dielectric, wherein the gate insulator comprises first and second layers (400, 420), of which layers only the second (420) extends to the storage capacitor (36) to define the capacitor dielectric,

   characterised in that

   the thickness of the first layer d_1 and the thickness of the second layer d_2 are selected approximately to satisfy the relation:

$$d_2 = (C_{store}/C_{LC})\cdot(\varepsilon_2/\varepsilon_1)\cdot d_1$$

in which ε_1 and ε_2 are the permittivity constants of the first and second layers (400, 420), respectively.

2. A display as claimed in claim 1, wherein the first layer (400) comprises an inorganic layer, and the second layer (420) comprises a polymer or spin-on glass layer.

3. A display as claimed in claim 2, wherein the second layer (420) comprises polyimide.

4. A display as claimed in any of claims 1 to 3, wherein the transistors (30) comprise top gate transistors.

5. A method of manufacturing a liquid crystal display, comprising:

providing an array of transistors (30) and storage capacitors (36) over a substrate (10), the transistors comprising insulated-gate staggered structures having substantially coplanar source and drain regions (11, 12; 64, 66) and a gate region (44; 62), a gate insulator (400, 420) lying between the gate region and the source and drain regions, and the storage capacitors comprising a stacked structure of two electrodes separated by a capacitor dielectric, wherein the gate insulator is deposited as first and second layers (400, 420), the first layer (400) being patterned to remove it from areas corresponding to the storage capacitors (36), and the second layer (420) extending to the areas corresponding to the storage capacitors to define the capacitor dielectric, and providing liquid crystal material (50) over the substrate (10), wherein

the first layer (400) is deposited to a thickness d_1, the second layer (420) is deposited to a thickness d_2, the storage capacitors (36) have capacitance C_{store} and each pixel forms a pixel capacitor of capacitance C_{LC}, **characterised in that** the thicknesses of the first and second layers (400, 420) are selected approximately to satisfy the relation:

$$d_2 = (C_{store}/C_{LC}).(\varepsilon_2/\varepsilon_1).\ d_1$$

in which ε_1 and ε_2 are the permittivity constants of the first and second layers (400, 420), respectively.

6. A method as claimed in Claim 5, wherein the first gate insulator layer (400) is deposited by vacuum deposition process, and the second gate insulator layer (420) is deposited by a non-vacuum process.

Patentansprüche

1. Flüssigkristall-Wiedergabeanordnung mit einer Anzahl Pixel, die je einen Schalttransistor (30), einen Speicherkondensator (36) mit einer Kapazität C_{store} und einen Pixelkondensator mit der Kapazität C_{LC} aufweisen, wobei die Transistoren gestaffelte Strukturen mit einer isolierten Gate-Elektrode aufweisen mit im Wesentlichen koplanaren Source- und Drain-Gebieten (11, 12; 64, 66) und einem Gate-Gebiet (44; 62), wobei ein Gate-Isolator (400, 420) zwischen dem Gate-Gebiet und den Source- und Drain-Gebieten liegt, und wobei die Speicherkondensatoren (36) eine gestapelte Struktur zweier Elektroden aufweisen, die durch ein Kondensatordielektrikum voneinander getrennt sind, wobei der Gate-Isolator eine erste und eine zweite Schicht (400, 420) aufweist, wobei nur die zweite Schicht (420) dieser Schichten sich bis an den Speicherkondensator (36) erstreckt zum Definieren des Kondensatordielektrikums, **dadurch gekennzeichnet, dass**

- die Dicke der ersten Schicht d_1 und die Dicke der zweiten Schicht d_2 sind derart gewählt worden, dass die nachfolgende Beziehung erfüllt wird:

$$d_2 = (C_{store}/C_{LC})\ .\ (\varepsilon_2/\varepsilon_1)\ .\ d_1$$

wobei ε_1 und ε_2 die Permittivitätskonstanten der ersten bzw. der zweiten Schicht (400, 420) sind.

2. Wiedergabeanordnung nach Anspruch 1, wobei die erste Schicht (400) eine anorganische Schicht aufweist und die zweite Schicht (420) eine Polymer- oder "spin-on"-Glasschicht aufweist.

3. Wiedergabeanordnung nach Anspruch 2, wobei die zweite Schicht (420) Polyimid aufweist.

4. Wiedergabeanordnung nach einem der Ansprüche 1 bis 3, wobei die Transistoren (30) Topgate-Transistoren sind.

5. Verfahren zum Herstellen einer Flüssigkristallwiedergabeanordnung, wobei dieses Verfahren die nachfolgenden Verfahrensschritte umfasst:

- das Anbringen einer Anordnung von Transistoren (30) und Speicherkondensatoren (36) über ein Substrat (10), wobei die Transistoren gestaffelte Strukturen mit isolierten Gate-Elektroden mit im Wesentlichen koplanaren Source-und Drain-Gebieten (11, 12; 64, 66) und einem Gate-Gebiet (44; 62) aufweisen, wobei zwischen dem Gate-Gebiet und den Source- und Drain-Gebieten ein Gate-Isolator (400, 420) liegt und wobei die Speicherkondensatoren eine gestapelte Struktur zweier Elektroden aufweisen, die durch ein Kondensatordielektrikum voneinander getrennt sind, wobei der Gate-Isolator als eine erste und eine zweite Schicht (400, 420) abgelagert wird, wobei die erste Schicht (400) mit einem Muster versehen wird zum Entfernen derselben aus Gebieten, die den Speicherkondensatoren (36) entsprechen, und wobei die zweite Schicht (420) sich bis an die Gebiete erstreckt, die den Speicherkondensatoren entsprechen zum Definieren des Kondensatordielektrikums, und

- das Anbringen von Flüssigkristallmaterial (50) über das Substrat (10), wobei die erste Schicht (400) bis zu einer Dicke d_1 angebracht wird, wobei die zweite Schicht (420) bis zu einer Dicke d_2 angebracht wird, wobei die Speicherkondensatoren (36) eine Kapazität C_{store} haben und jedes Pixel ein Pixel mit einer Kapazität C_{LC} bildet, **dadurch gekennzeichnet, dass** die Dicke der ersten und der zweiten Schicht (400, 420) derart gewählt wird, dass sie der nachfolgenden Beziehung nahezu erfüllt:

$$d_2 = (C_{store}/C_{LC})\cdot(\varepsilon_2/\varepsilon_1)\cdot d_1$$

wobei ε_1 und ε_2 die Permittivitätskonstanten der ersten bzw. der zweiten Schicht (400, 420) sind.

6. Verfahren nach Anspruch 5, wobei die erste Gate-Isolatorschicht (400) in einem Vakuum-Ablagerungsprozess abgelagert wird, und wobei die zweite Gate-Isolatorschicht (420) in einem Nicht-Vakuum-Prozess abgelagert wird.

Revendications

1. Affichage à cristaux liquides comprenant une pluralité de pixels comprenant chacun un transistor de commutation (30), un condensateur de stockage (36) de capacité C_{store} et un condensateur de pixel de capacité C_{LC}, les transistors comprenant des structures décalées à grille isolée ayant des zones de source et de drain (11, 12; 64, 66) et une zone de source (44; 62) sensiblement coplanaires, un isolant de grille (400, 420) étant situé entre la zone de grille et les zones de source et de drain, et les condensateurs de stockage (36) comprenant une structure superposée de deux électrodes séparées par un diélectrique de condensateur, dans lequel l'isolant de grille comprend une première et une deuxième couches (400, 420), desquelles couches, seule la deuxième (420), s'étend jusqu'au condensateur de stockage (36) afin de définir le diélectrique de condensateur,
caractérisé en ce que
l'épaisseur de la première couche d_1 et l'épaisseur de la deuxième couche d_2 sont sélectionnées approximativement pour satisfaire à la relation :

$$d_2 = (C_{store}/C_{LC})\ .\ (\varepsilon_2/\varepsilon_1).\ d_1$$

dans laquelle ε_1 *et* ε_2 sont les constantes de permittivité des première et deuxième couches (400, 420) respectivement.

2. Affichage suivant la revendication 1, dans lequel la première couche (400) comprend une couche inorganique, et la deuxième couche (420) comprend une couche de polymère ou de verre centrifugé.

3. Affichage suivant la revendication 2, dans lequel la deuxième couche (420) comprend un polyimide.

4. Affichage suivant l'une quelconque des revendications 1 à 3, dans lequel les transistors (30) comprennent des transistors à grille supérieure.

5. Procédé de fabrication d'un affichage à cristaux liquides,comprenant : la fourniture d'une matrice de transistors (30) et de condensateurs de stockage (36) sur un substrat (10), les transistors comprenant des structures décalées à grille isolée ayant des zones de source et de drain sensiblement coplanaires (11, 12; 64, 66) et une zone de grille (44; 62), un isolant de grille (400, 420) situé entre la zone de grille et les zones de source et de drain, et les condensateurs de stockage comprenant une structure superposée de deux électrodes séparées par un diélectrique de condensateur, dans lequel l'isolant de grille est déposé comme première et deuxième couches (400, 420), la première couche (400) étant configurée par un motif pour la retirer des zones qui correspondent aux condensateurs de stockage (36), et la deuxième couche (420) s'étendant jusqu'aux zones qui correspondent aux condensateurs de stockage pour définir le diélectrique de condensateur, et la fourniture de cristaux liquides (50) sur le substrat (10), dans lequel la première couche (400) est déposée jusqu'à une épaisseur d_1, la deuxième couche (420) est déposée jusqu'à une épaisseur d_2, les condensateurs de stockage (36) ont une capacité C_{store} et chaque pixel forme un condensateur de pixel de capacité C_{LC},
caractérisé en ce que
les épaisseurs des première et deuxième couches (400, 420) sont sélectionnées pour satisfaire approximativement à la relation :

$$d_2 = (C_{store}/C_{LC}) \cdot (\varepsilon_2/\varepsilon_1) \cdot d_1$$

dans laquelle ε_1 *et* ε_2 sont les constantes de permittivité des première et deuxième couches (400, 420), respectivement.

6. Procédé suivant la revendication 5, dans lequel la première couche d'isolant de grille (400) est déposée par un processus de dépôt sous vide, et la deuxième couche d'isolant de grille (420) est déposée par un processus qui ne fait pas appel au vide.

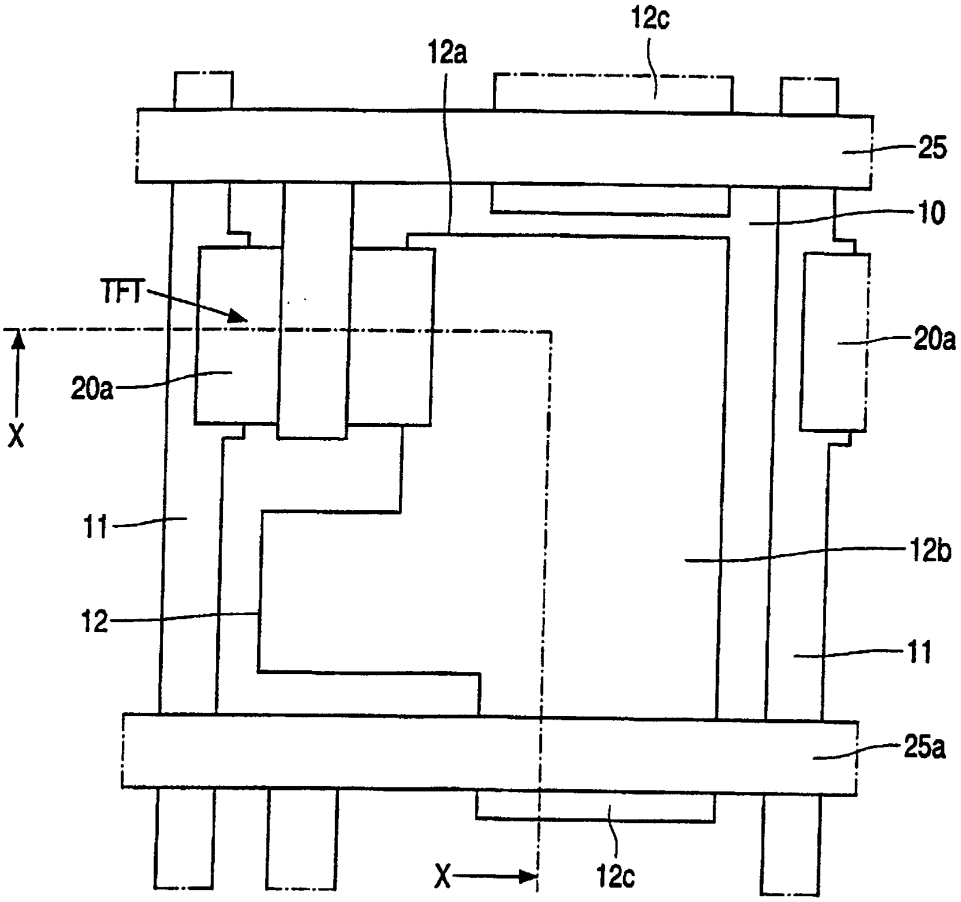
12c
12a
25
10
TFT
20a
20a
X
11
12b
12
11
25a
X
12c

FIG. 1

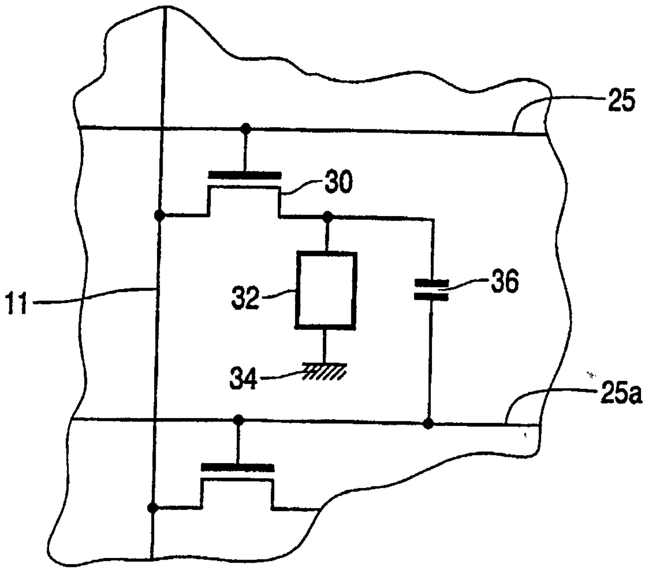
25
30
36
11
32
34
25a

FIG. 2

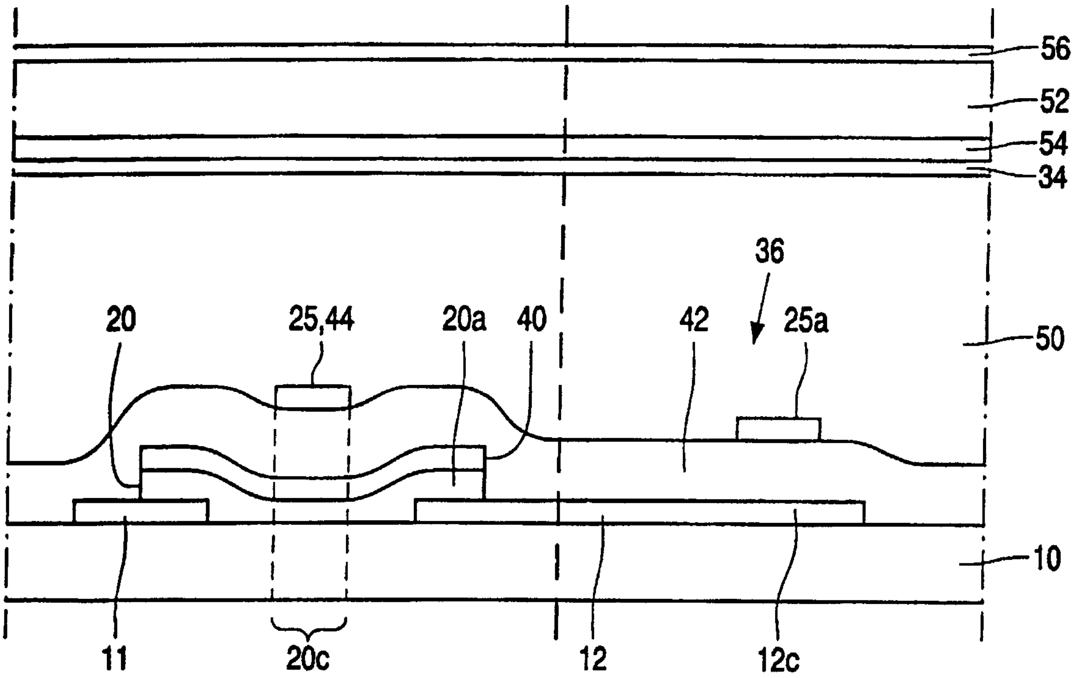
56
52
54
34
36
20
25,44
20a
40
42
25a
50
10
11
20c
12
12c

FIG. 3

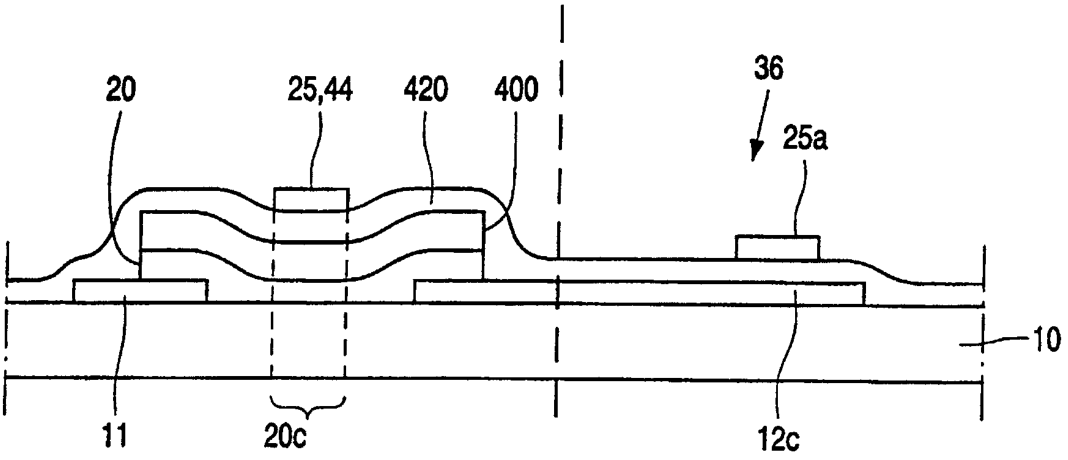
36
20
25,44
420
400
25a
10
11
20c
12c

FIG. 4

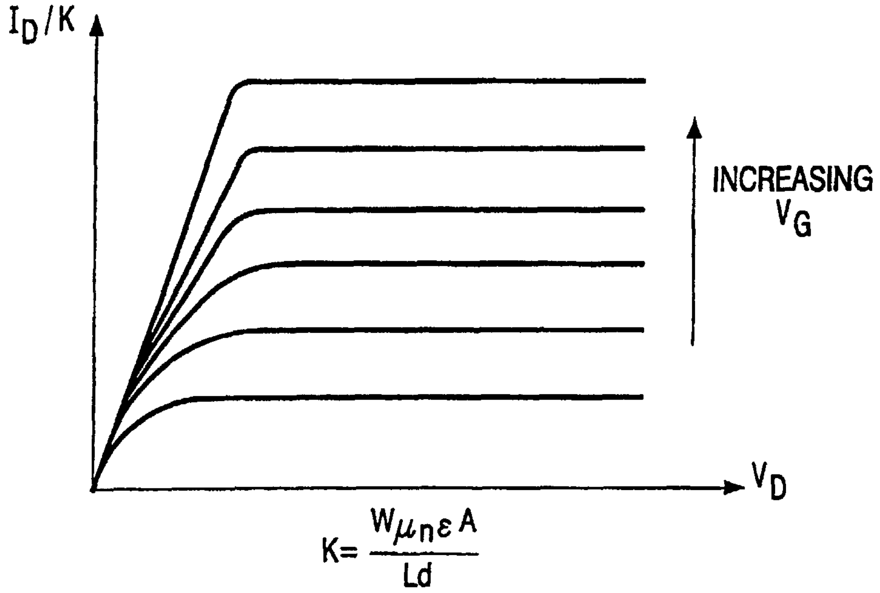
I_D/K
INCREASING V_G
V_D
$K = \frac{W \mu_n \varepsilon A}{Ld}$

FIG. 5

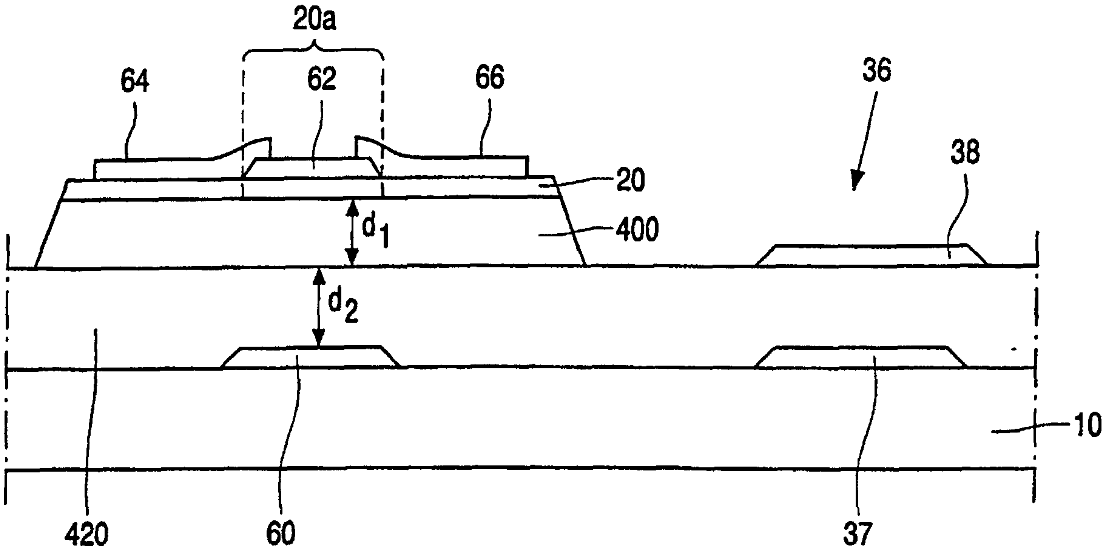
20a
64
62
66
36
38
20
d_1
400
d_2
10
420
60
37

FIG. 6

专利名称(译)	用于液晶显示器的有源矩阵基板及其制造方法		
公开(公告)号	EP1166174B1	公开(公告)日	2003-04-16
申请号	EP2000985051	申请日	2000-11-15
[标]申请(专利权)人(译)	皇家飞利浦电子股份有限公司		
申请(专利权)人(译)	皇家飞利浦电子N.V.		
当前申请(专利权)人(译)	皇家飞利浦电子N.V.		
[标]发明人	BATTERSBY STEPHEN J DEANE STEVEN C		
发明人	BATTERSBY, STEPHEN, J. DEANE, STEVEN, C.		
IPC分类号	G02F1/1333 G02F1/1362 G02F1/1368 H01L21/336 H01L29/786		
CPC分类号	G02F1/136213		
优先权	1999028353 1999-12-01 GB		
其他公开文献	EP1166174A1		
外部链接	Espacenet		

摘要(译)

用于液晶显示器的晶体管基板包括绝缘栅交错TFT阵列和与每个晶体管相关的电容器（36）。栅极绝缘体（400,420）包括第一无机层（400）和第二聚合物或旋涂玻璃层（420），其中仅层聚合物或旋涂玻璃层（420）延伸到电容器（36））定义电容器电介质。

$$d_2 = (C_{store}/C_{LC}) \, . \, (\varepsilon_2/\varepsilon_1) \, . \, d_1$$