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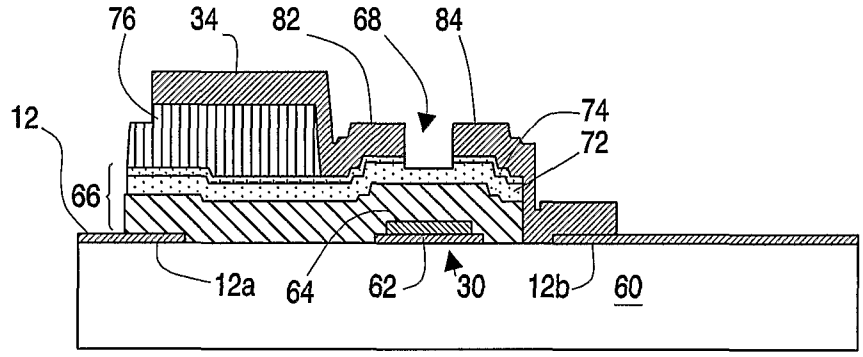
(54) Title: LIQUID CRYSTAL DISPLAYS



(57) Abstract: An active plate for a liquid crystal display has an insulating layer (76) arranged as a plurality of columns, each insulating layer column overlapping the pixel electrodes (12) of two adjacent columns of pixels. An opaque conductor layer is formed over the substrate and patterned to define column conductors (34) on top of the insulating layer, and source and drain electrodes for the transistor on top of thin film transistor layers (66). Thus, an insulating layer (76) is defined beneath the column conductors (34), so that it lies between the crossing row and column conductors. In addition, the columns of insulating layer (76) overlap adjacent pairs of pixel electrodes (12), so that the column conductors can overlap the pixel electrodes, thereby increasing the pixel aperture. The transparent pixel electrodes (12) are, however, the first layer to be deposited. This gives advantages in process simplification and corresponding cost reduction for manufacture of high quality active matrix LCD (AMLCD) displays.

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DESCRIPTION

LIQUID CRYSTAL DISPLAYS

This invention relates to active matrix liquid crystal displays, and particularly to the transistor substrate, known as the active plate, used in the manufacture of such a display.

A liquid crystal display typically comprises an active plate and a passive plate between which liquid crystal material is sandwiched. The active plate comprises an array of transistor switching devices, typically with one transistor associated with each pixel of the display. Each pixel is also associated with a pixel electrode on the active plate to which a signal is applied for controlling the brightness of the individual pixel.

Fig. 1 shows a typical view of the transmissive areas of an AMLCD. The basic pixels are square but divided into three vertical sub-pixels 10 coloured red 10a, green 10b and blue 10c. To increase the optical aperture (i.e. increase the area over which a modulated light output is provided), it is necessary to decrease the width of the black lines, H and W. Due to the 3:1 height to width ratio of the sub-pixels, decreasing the column width W by an amount (for example one micron) will increase the optical aperture by three times as much as a corresponding decrease in the row width H.

A large area of the active plate is at least partially transparent, and this is required because the display is typically illuminated by a backlight. Mainly, the areas covered by the opaque row and column conductors are the only opaque parts of the plate. If the pixel electrode does not cover the transparent area, then there will be an area of liquid crystal material not modulated by the pixel electrode but which does receive light from the backlight. This reduces the contrast ratio and blackness of the display.

Figure 2 shows an arrangement in which the pixel electrodes 12 are provided between the column conductors 14, so that there is a gap 16 between the pixels and columns on the active plate through which

unmodulated light 18 can pass. Regions 20 of the LC layer are shielded by the columns 14 whereas regions 22 are modulated by the pixel electrodes 12. This is a so-called "standard" display. In such a display, a black mask layer is typically provided for shielding these areas of the active plate, and additionally to shield the transistors as their operating characteristics are light-dependent. Conventionally, the black mask layer is located on the passive plate of the active matrix cell. Plate to plate alignment during cell manufacture is less accurate than layer to layer alignment on a substrate. This means that the black mask must be comparatively large to ensure that it blocks stray light at the edge of pixels. Figure 3 shows a cell with a black mask 24 on the passive plate and the required overlap is shown as 26. The width of the columns of black mask layer 24 define the width W in Figure 1.

This overlap reduces the aperture of the display pixels, which reduces the power efficiency of the display. This is particularly undesirable for battery-operated devices, such as portable products.

Figure 4 shows the electrical components which make up the sub pixels shown in Figure 1. A row conductor 30 is connected to the gate of a TFT 32, and a column electrode 34 is coupled to the source. The liquid crystal material provided over the pixel effectively defines a liquid crystal cell 36 which extends between the drain of the transistor 32 and a common ground plane 38. The ground plane 38 is defined by the passive plate and the other terminal of the LC cell is defined by the pixel electrodes 12. A pixel storage capacitor 40 is connected between the drain of the transistor 32 and the row conductor associated with an adjacent row of pixels or else to a separate line 41.

It has been proposed to use layers of the active plate to provide the required masking function. For example, one proposal is to define the pixel electrodes 12 to overlap the row and column conductors 30,34, so that there is no gap between the row and column conductors and the pixel electrodes, which would otherwise need to be shielded. This results in a high aperture pixel, and is called a Field Shielded Pixel (FSP) design.

Figure 5 shows a cross-section through the TFT of a FSP panel, and Figure 6 shows the cross-section through a column.

The pixel electrode 50 overlaps the row conductor as shown in Figure 5 and overlaps the column conductor 34 as shown in Figure 6. The row and column conductors block the passage of light as shown schematically in Figure 6. The pixel electrode is provided over a polymer layer 54 and contacts the drain 52 of the TFT 32 through a via 56 in the polymer layer 54.

The main functional requirements on the polymer layer are that it should be a uniform highly transparent layer with contact holes and low capacitance. It should also have good planarisation properties to remove steps over the edges of the column that could cause disclination lines in the LC cell. Typically a layer of benzocyclobutene (BCB) more than one micron thick is used due to its high transparency, low dielectric constant ($\varepsilon_R = 2.7$) and good planarisation properties.

The BCB layer is a very expensive layer to use because of high material and processing costs. It is possible to purchase photodefinable BCB, but it cannot be used for this application because it does not have high optical transparency. This means etch masking layers must be used during fabrication. It is difficult to use a photoresist etch layer because anything that etches BCB also etches photoresist. This limits the thickness of BCB to about 1 micron. If a combination of metal and photoresist layers is used to pattern the BCB then it becomes very expensive due to the extra processing equipment and processing needed.

According to the invention, there is provided a method of forming an active plate for a liquid crystal display, comprising:

depositing and patterning a substantially transparent conductor layer to define an array of pixel electrodes over an insulating substrate arranged in rows and columns;

defining row conductors and connected gate conductor portions over different areas of the insulating substrate to the pixel electrodes;

depositing and patterning thin film transistor layers over the gate conductor portions to form transistor bodies, the thin film transistor layers comprising at least a gate insulator and a semiconductor layer;

forming an insulating layer arranged as a plurality of columns, each insulating layer column overlapping the pixel electrodes of two adjacent columns of pixels; and

forming an opaque conductor layer over the substrate and patterning the opaque conductor layer to define column conductors on top of the insulating layer, and source and drain electrodes for the transistor on top of the thin film transistor layers, one of which is connected to a column conductor and the other of which is connected to an associated pixel electrode.

In this method, an insulating layer is defined beneath the column conductors, so that it lies between the crossing row and column conductors. In addition, the columns of insulating layer overlap adjacent pairs of pixel electrodes, so that the column conductors can overlap the pixel electrodes, thereby increasing the pixel aperture. The transparent pixel electrodes are, however, the first layer to be deposited. This gives advantages in process simplification and corresponding cost reduction for manufacture of high quality active matrix LCD (AMLCD) displays. The invention provides an efficient, low cost way of decreasing the width W shown in Figure 1.

The thin film transistor layers of each transistor body may also overlap an adjacent pixel electrode. In this way, the transistor layer also lie beneath the column conductors and provide additional separation between the row and column conductors. In particular, the gate insulator layer provides additional capacitive separation.

The insulating layer preferably comprises a polymer for example a photo-acrylic polymer, and acts as a field shield layer.

Defining the array of pixel electrodes and the row conductors can be performed with a first, single-mask process. Forming the transistor bodies and the insulating layer can be performed with a second, single-mask process. Forming the column conductors and source and drain electrodes can be performed with a third, single-mask process. Thus, a three-mask process can be used for manufacture of the display. Each single mask process may use a half-tone photo-mask.

The invention also provides an active matrix liquid crystal display device, comprising an active plate and a passive plate with liquid crystal sandwiched between, wherein the active plate comprises:

an insulating substrate;

an array of rows and columns of pixel electrodes and an array of row conductors, occupying different areas over the over the substrate, the pixel electrodes being substantially transparent and the row conductors having gate conductor portions;

thin film transistor layers over the gate conductor portions to define transistor bodies,

an insulating layer arranged as a plurality of columns, each insulating layer column overlapping the pixel electrodes of two adjacent columns of pixels;

opaque column conductors provided on top of the insulating layer; and

source and drain electrodes for the transistor on top of the thin film transistor layers one of which is connected to a column conductor and the other of which is connected to an associated pixel electrode.

This device is formed by the method of the invention, and has rows of insulator separating the column conductors from the row conductors and enabling the row conductors to overlap (and thereby completely fill the space between) adjacent columns of pixel electrodes.

Again, the thin film transistor layers may define, in addition to the transistor bodies, columns which lie beneath the insulating layer.

An example of the invention will now be described in detail with reference to the accompanying drawings, in which:

Figure 1 shows a plan view of a known colour AMLCD;

Figure 2 shows a cross section through a known standard AMLCD;

Figure 3 shows how a black mask layer is used to improve the performance of the AMLCD of Figure 2;

Figure 4 shows the electrical elements of each pixel;

Figure 5 shows a known Field Shielded Pixel design, in cross section through the transistor;

Figure 6 shows the known Field Shielded Pixel design, in cross section through the column;

Figure 7 shows the active plate of the display of the invention, in cross section through the transistor;

Figure 8 shows the active plate of the display of the invention, in cross section through the column;

Figures 9A to 9D show the steps of producing the pixel electrodes and row conductors in the method of the invention;

Figure 10 shows in plan view the structure resulting from the method of Figures 9A to 9D;

Figures 11A to 11D show the steps of producing the transistor bodies and insulating layer in the method of the invention;

Figure 12 shows in plan view the shape of the transistor layers and insulating layer deposited in the method steps of Figures 11A to 11D;

Figure 13 shows in plan view the structure resulting from the method of Figures 11A to 11D;

Figures 14A to 14E show the steps of producing the column conductors and source and drain electrodes in the method of the invention;

Figure 15 shows in plan view the shape of the column conductors and source and drain electrodes deposited in the method steps of Figures 14A to 14D; and

Figure 16 shows the complete device structure in plan view.

Figures 7 and 8 show the active plate of the display of the invention, in cross section through the transistor (Figure 7) and in cross section through the column (Figure 8). The locations of the cross sections can be seen in Figure 16.

The active plate comprises an insulating substrate 60 over which the array of pixel electrodes 12 is directly deposited. The array of row conductors 30 is also provided directly over the substrate, and occupying different areas to

the pixel electrodes. The pixel electrodes are substantially transparent, preferably formed from ITO, whereas the row conductors comprise the ITO layer 62 of the pixel electrodes and an additional layer 64 for increasing the conductivity and which renders the row conductors opaque. The row conductors 30 have portions defining gate conductors, as can be seen in Figure 7.

Thin film transistor layers 66 are provided over the gate conductor to define transistor bodies 68. These layers comprise a silicon nitride gate insulator 70 an amorphous silicon layer 72 and an n-type doped silicon contact layer 74. These layers 66 not only define the transistor body but also extend to an adjacent pixel electrode (12a in Figure 7). In this example, the transistor layers also extend beneath the columns, as can be seen in Figure 8.

A polymer insulating layer 76 is defined as a plurality of columns, each insulating layer column overlapping the pixel electrodes 12 of two adjacent columns of pixels, as shown in Figure 8. The opaque column conductors 34 are provided on top of the polymer insulating layer 76, and the metal layer which defines the column conductors 34 also defines the source 82 and drain 84 electrodes for the transistor 68 on top of the thin film transistor layers 66. One of the source and drain 82 is connected to a column conductor 80 and the other 84 is connected to an associated pixel electrode 12b.

Without the polymer field shield layer 76, the capacitance between the pixel and columns 34 becomes too high. It is not possible to use the silicon nitride gate insulator layer on its own because it has a dielectric constant of 6.4 and an unrealistically thick layer would be needed to give sufficiently low capacitance.

There are several advantages to this design of high optical aperture ratio array. The first is that the polymer does not need to be transparent. This means that a large range of polymers can be used, including ones that are photodefinable. This can lead to lower cost and opens the way for shorter, simpler manufacturing processes. The polymer layer also does not need to have such good planarisation properties because it does not cross over the edge of the visible pixel. The combination of greater polymer choice and

simpler manufacturing processes leads to substantial cost savings in manufacturing. Several different polymers can be used, such as photodefinable polyimide or acrylic layers.

The method of manufacturing the device shown in Figures 7 and 8 will now be described, with an additional capacitor electrode. A three mask process can be used as will be apparent from the following, in particular by using half-tone photo-masks. Half-tone masks can be made with diffraction gratings or silicon rich silicon nitride as a grey mask. Both techniques reduce light throughput to produce areas in which the illumination intensity is intermediate between clear areas of the mask and areas covered with metal. In this way the half tone mask can be used to define areas where there is two different thicknesses of photopolymer, as well as areas in which the photopolymer is totally removed. This can be used to reduce the total number of photomasks that are needed.

In Figures 9, 11 and 14, the left column of cross sections are the cross sections through the TFT, corresponding to Figure 7, and the right column of cross sections are the cross sections through the column, corresponding to Figure 8. The thickness and widths of layers has been exaggerated or otherwise distorted in the Figures for the purposes of clarity.

Each of Figures 9, 11 and 14 shows one of the three mask processes of the method of the invention.

Figures 9A to 9D show the initial steps of producing the pixel electrodes and row conductors.

In Figure 9A, a sputter deposition technique is used to deposit an ITO layer 62 and a gate metal layer 64. A half-tone mask 81 is used to etch the metal and ITO. As shown, the half tone mask is thicker over the portion of the layers 62, 64 to define the row conductors and gate conductor. In Figure 9B, oxygen plasma is used to etch away the thin layers of photoresist, only leaving photoresist in the areas that originally had thick photoresist, namely the gate conductor regions 30. In Figure 9C, the gate metal is etched away from the pixel electrode areas. Removal of the photoresist in Figure 9D leaves the ITO

pixel electrodes and the row conductors 30 which are in the form of a two layer ITO and gate metal stack.

Figure 10 shows in plan view the structure resulting from the method of Figures 9A to 9D. As shown, an array of rows and columns of pixel electrodes 12 are provided, with an array of row conductors 30, occupying spaces between the rows of pixel electrodes. The row conductors 30 have gate conductor portions 30b as well as row portions 30a. In this example, the row portion 30b has a wider portion 30c which acts as a capacitor terminal as will be apparent further below.

The cross section arrows in Figure 10 show where the left and right columns of Figure 9 are viewed.

Figures 11A to 11D show the steps of producing the transistor bodies and insulating layer in the method of the invention.

In Figure 11A plasma deposition is used to define the TFT stack 66 of silicon nitride (SiN) 70, amorphous silicon 72 and n+ doped amorphous silicon 74.

In Figure 11B a photopolymer 80, such as photo-acrylic, is patterned to two levels corresponding to the desired shaped of the SiN gate insulator layer and the field shield insulator shape. As explained above, the field shield insulator is arranged as columns, and thus columns are provided with thicker regions 80a of photopolymer.

In Figure 11C, the TFT stack is plasma etched so that the TFT layers 66 define columns as well as the TFT transistor body.

In Figure 11D, the photo-polymer is partially etched to leave only a pattern 76 where there had originally been a thick layer of polymer, namely over the columns.

It is noted that the width of the photopolymer 76 is in fact the same in the two cross sections of Figure 11D, but the Figures have been distorted for convenience. The columns are in fact of constant width.

Figure 12 shows in plan view the shape of the transistor layers and insulating layer deposited in the method steps of Figures 11A to 11D. In Figure 12, the photopolymer, which has formed the insulating layer 76, is

shown slightly narrower than the TFT layers 66 beneath. This is simply so that both can be seen, but in fact the left side has been etched to the same pattern and they will be aligned. The TFT area has also only been shown for the left column but in fact the pixel pattern will repeat.

Figure 13 shows in plan view the combined structure resulting from the method steps of Figures 9 and 11.

Figures 14A to 14E show the steps of producing the column conductors and source and drain electrodes.

In Figure 14A, a top metal layer 90 is deposited (sputtered) over the substrate and a half-tone mask 92 is used to define a photoresist layer to two thicknesses. The lower thickness 92a is for the TFT, where part of the n+ amorphous silicon layer is to be removed in the region of the gate of the TFT, and the thicker part 92b is for the column conductors and source and drain contacts.

In Figure 14B, the top metal 90 is etched to leave metal columns and source and drain contacts (but no gap over the gate yet).

In Figure 14C, the photoresist layer is thinned using an O_2 plasma, until the area above the gate is exposed.

In Figure 14D, the top metal is etched again only in the TFT channel region. Plasma etching is then used to also removes the underlying n+ amorphous silicon layer, so that the n+ layer forms only contact portions for the source and drain.

In Figure 14E, the top photoresist layer 92 is removed.

Figure 15 shows in plan view the shape of the column conductors and source and drain electrodes deposited in the method steps of Figures 14A to 14D. The exposed amorphous silicon transistor body 72 is also shown. The top metal layer 90 is also patterned to define a capacitor top contact 94.

Figure 16 shows the complete device structure in plan view. The TFT can either be passivated by a separate polymer or SiN layer, or the LC polyimide alignment layer can be used.

The invention can be applied to any high optical aperture transmissive TN AMLCD.

In the examples above, the polymer field shield layer 76 lies above the TFT stack (silicon nitride and amorphous silicon layers), but the TFT stack could be omitted from beneath the columns and the design will still work. The critical features needed for the polymer stack is that it has low enough capacitance to reduce cross-talk to an acceptable level.

Only one specific example has been given above. It will be appreciated that the materials used to form the various layers are conventional. The processing conditions as well as various optional additional layers to those shown in the specific example, will be apparent to those skilled in the art.

CLAIMS

1. A method of forming an active plate for a liquid crystal display, comprising:

depositing and patterning a substantially transparent conductor layer to define an array of pixel electrodes (12) over an insulating substrate arranged in rows and columns;

defining row conductors (30) and connected gate conductor portions (30b) over different areas of the insulating substrate to the pixel electrodes;

depositing and patterning thin film transistor layers (66) over the gate conductor portions to form transistor bodies, the thin film transistor layers comprising at least a gate insulator (70) and a semiconductor layer (72);

forming an insulating layer (76) arranged as a plurality of columns, each insulating layer column overlapping the pixel electrodes (12) of two adjacent columns of pixels; and

forming an opaque conductor layer over the substrate and patterning the opaque conductor layer to define column conductors (34) on top of the insulating layer (76) , and source (82) and drain (84) electrodes for the transistor on top of the thin film transistor layers (66), one of which is connected to a column conductor and the other of which is connected to an associated pixel electrode.

2. A method as claimed in claim 1, wherein the thin film transistor layers (66) of each transistor body also overlap an adjacent pixel electrode (12).

3. A method as claimed in any preceding claim, wherein the insulating layer (76) comprises a polymer.

4. A method as claimed in claim 3, wherein the polymer comprises a photo-acrylic polymer.

5. A method as claimed in claims 1 or 2, wherein defining the array of pixel electrodes (12) and the row conductors (30) is performed with a first, single-mask process.

6. A method as claimed in claim 5, wherein forming transistor bodies and the insulating layer is performed with a second, single-mask process.

7. A method as claimed in claim 6, wherein forming the column conductors (34) and source and drain electrodes (82,84) is performed with a third, single-mask process.

8. A method as claimed in claim 7, wherein each single mask process uses a half-tone photo-mask.

9. An active matrix liquid crystal display device, comprising an active plate and a passive plate with liquid crystal sandwiched between, wherein the active plate comprises:

an insulating substrate (60);

an array of rows and columns of pixel electrodes (12) and an array of row conductors (30), occupying different areas over the over the substrate, the pixel electrodes being substantially transparent and the row conductors (30) having gate conductor portions (30b);

thin film transistor layers (66) over the gate conductor portions to define transistor bodies,

an insulating layer (76) arranged as a plurality of columns, each insulating layer column overlapping the pixel electrodes (12) of two adjacent columns of pixels;

opaque column conductors (34) provided on top of the insulating layer (76); and

source and drain electrodes (82,84) for the transistor on top of the thin film transistor layers (66) one of which is connected to a column conductor (34) and the other of which is connected to an associated pixel electrode (12).

10. A device as claimed in claim 9, wherein the thin film transistor layers (66) define, in addition to the transistor bodies, columns which lie beneath the insulating layer.

11. A device as claimed in claims 9 or 10, wherein the insulating layer (76) comprises a polymer.

12. A device as claimed in claim 11, wherein the polymer comprises a photo-acrylic polymer.

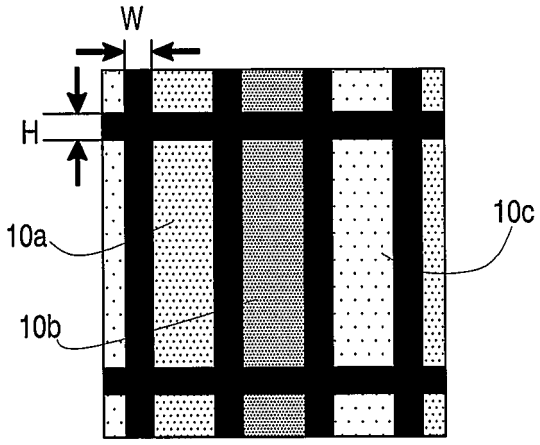

FIG.1

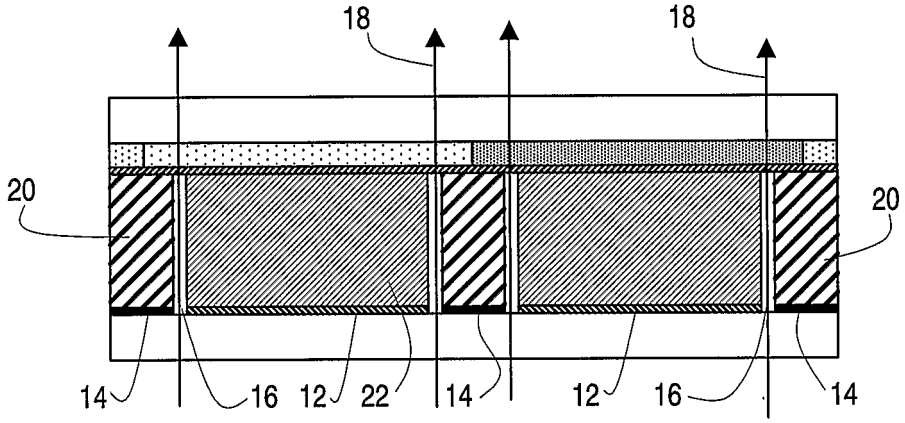

FIG.2

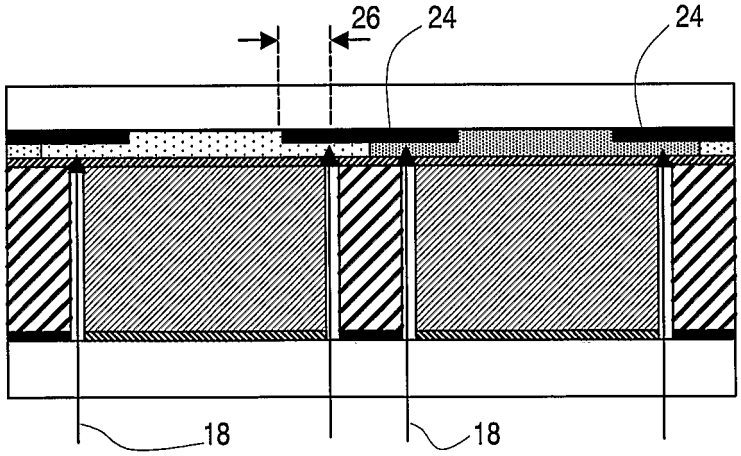

FIG.3

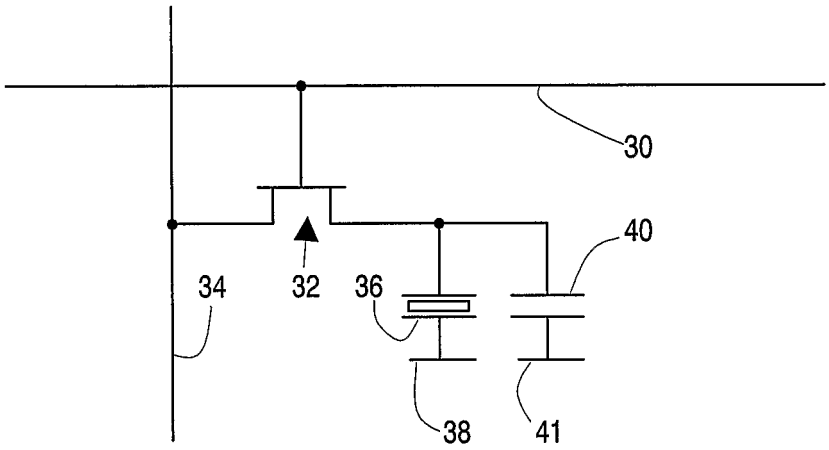

FIG.4

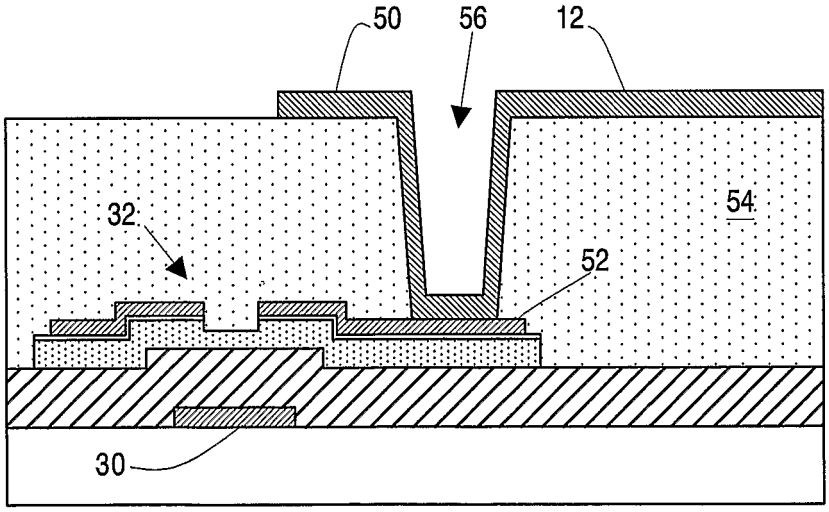

FIG.5

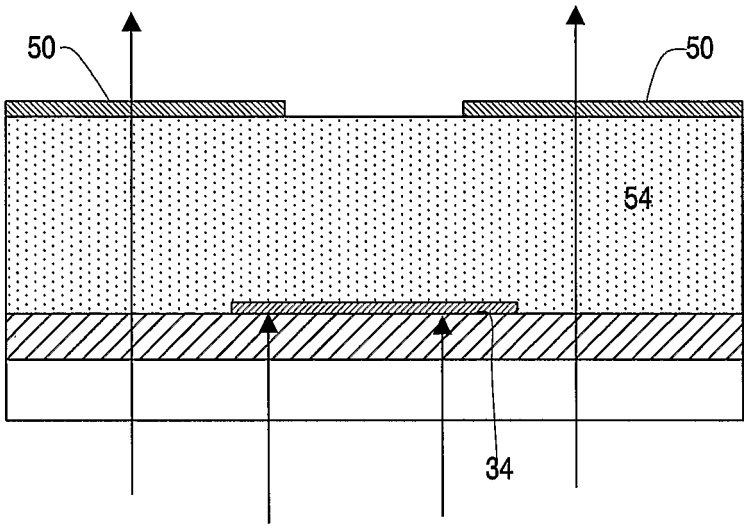

FIG.6

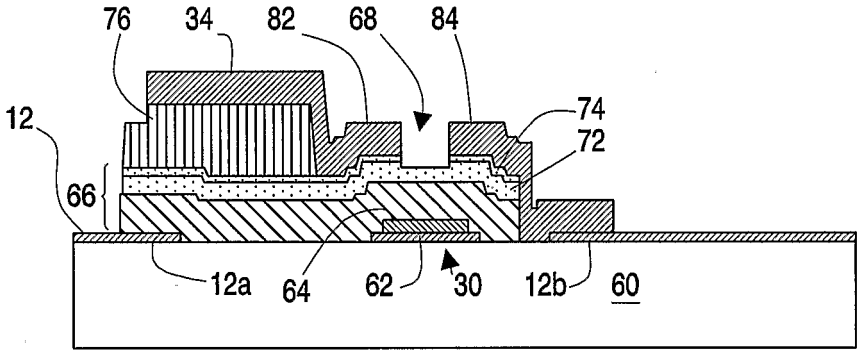

FIG.7

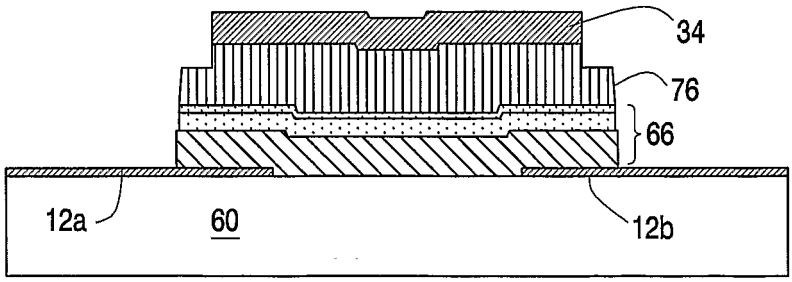

FIG.8

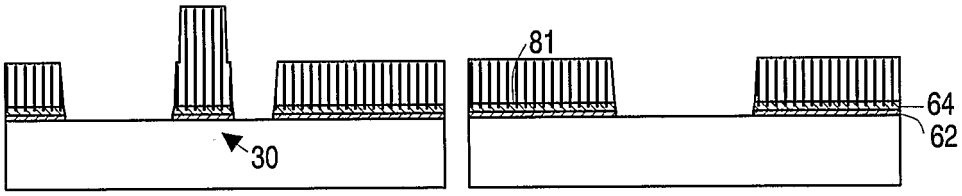

FIG.9A

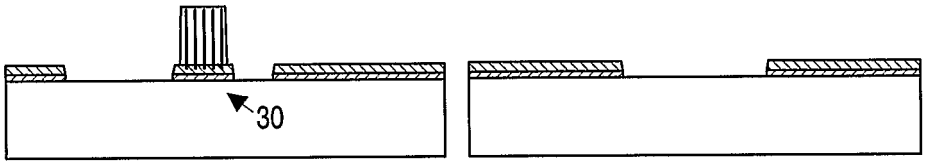

FIG.9B

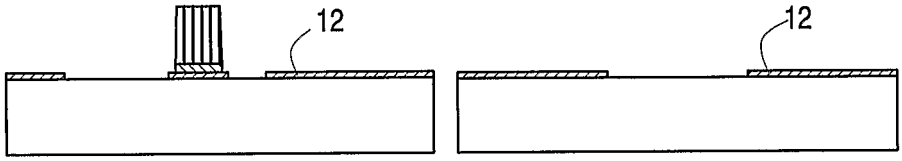

FIG.9C

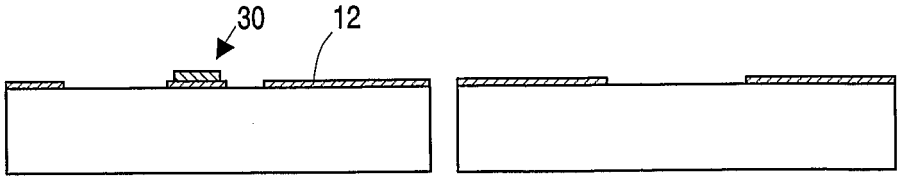

FIG.9D

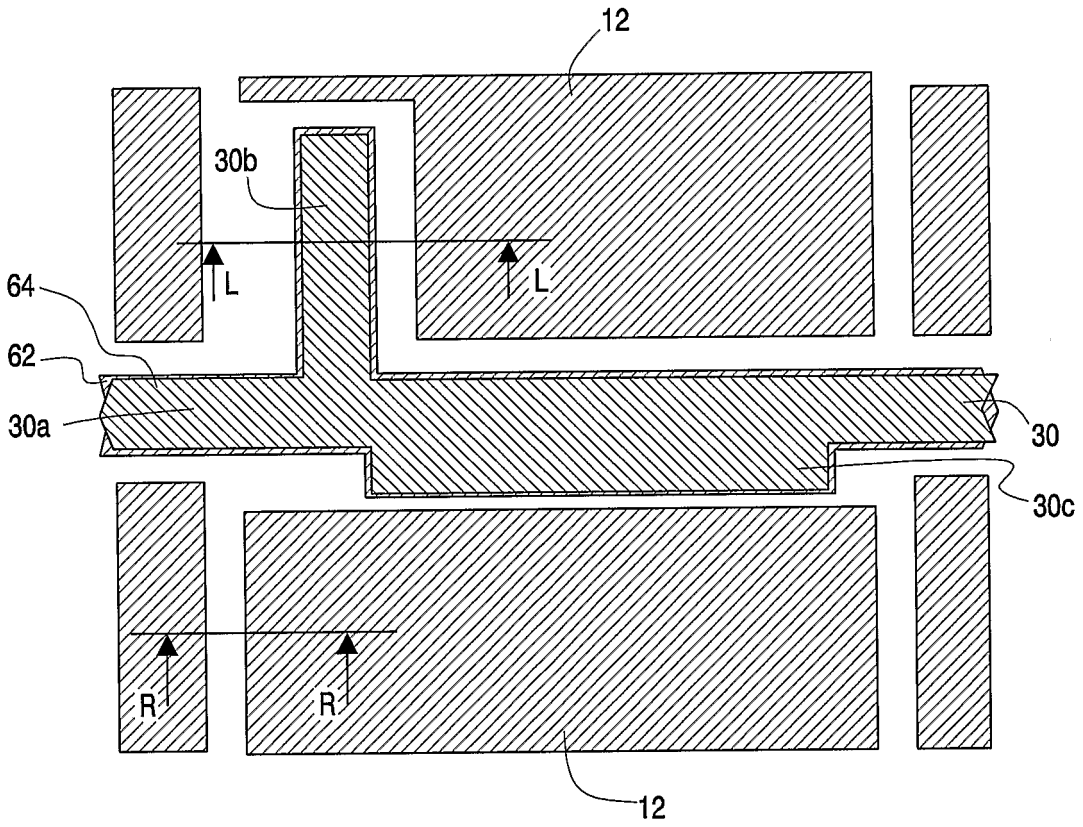

FIG.10

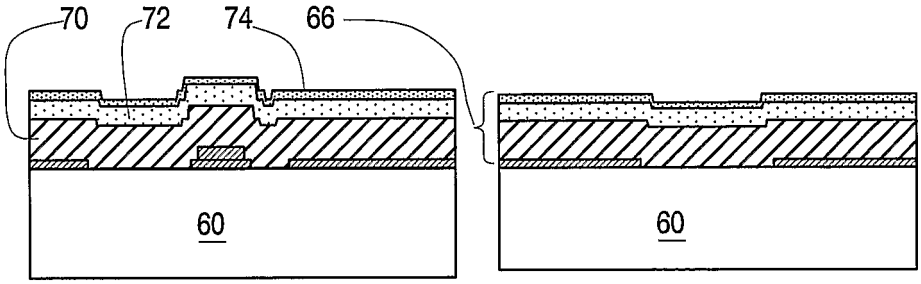

FIG.11A

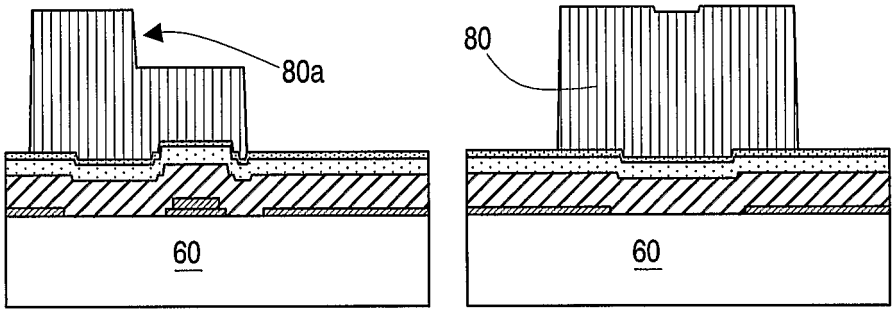

FIG.11B

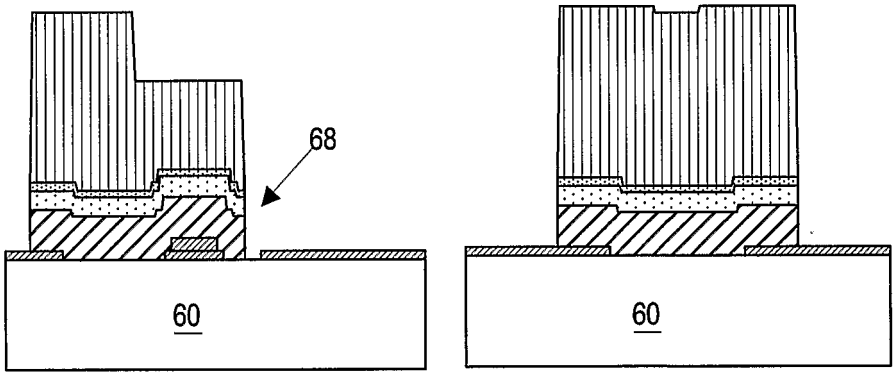

FIG.11C

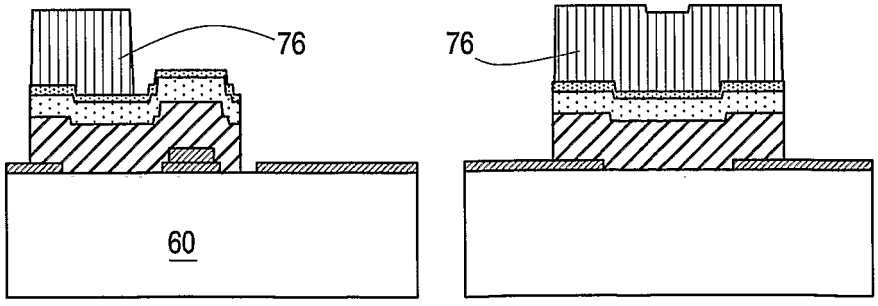

FIG.11D

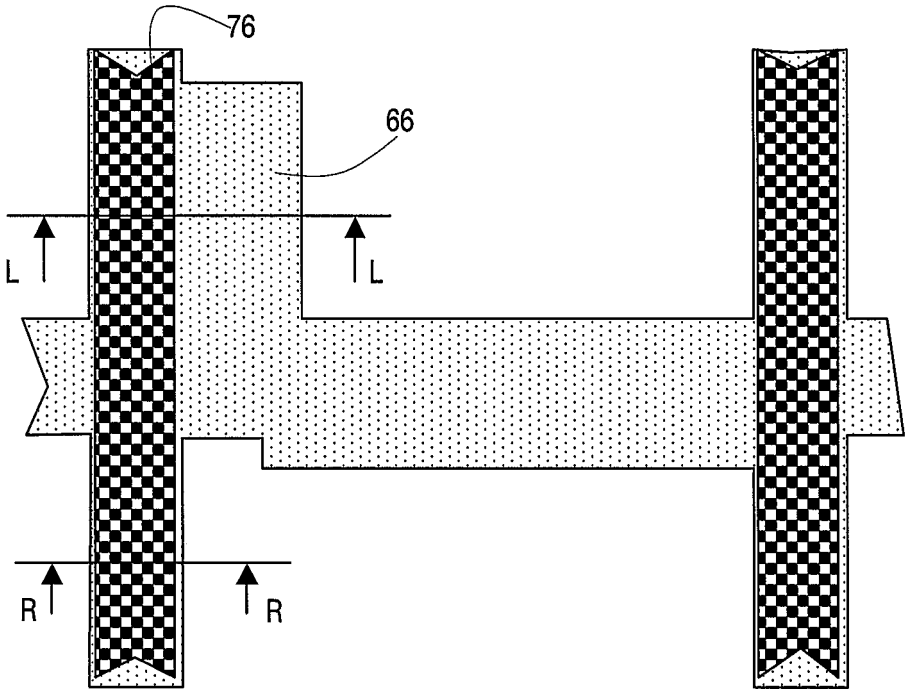

FIG.12

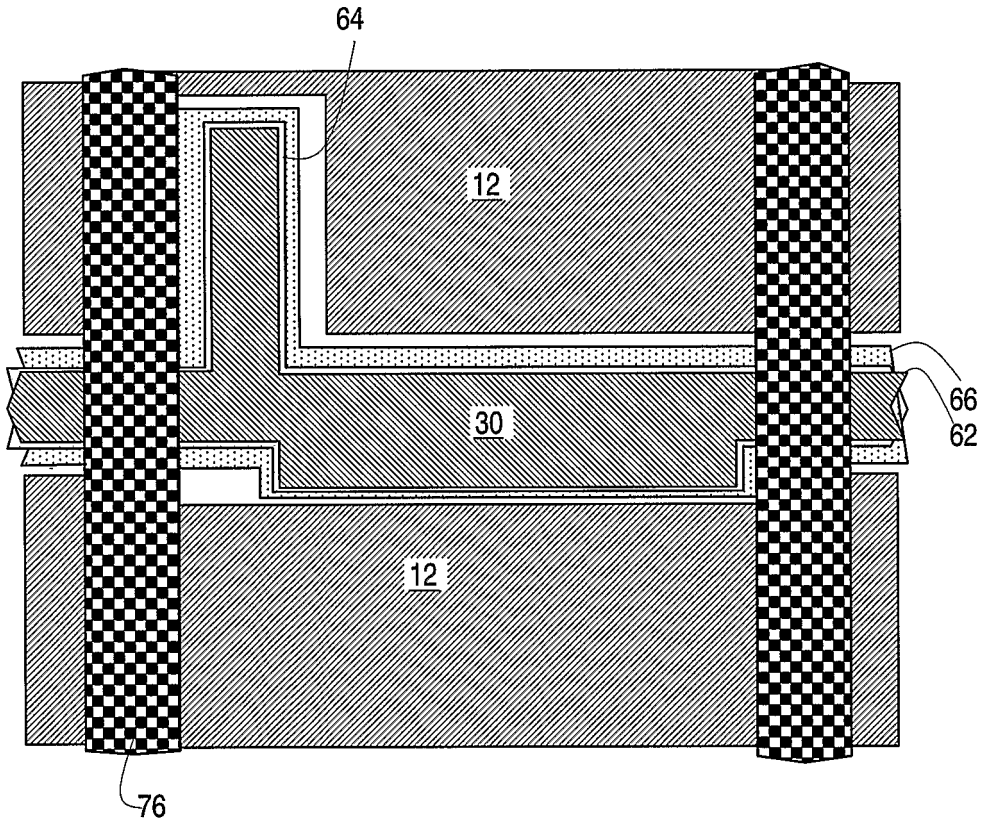

FIG.13

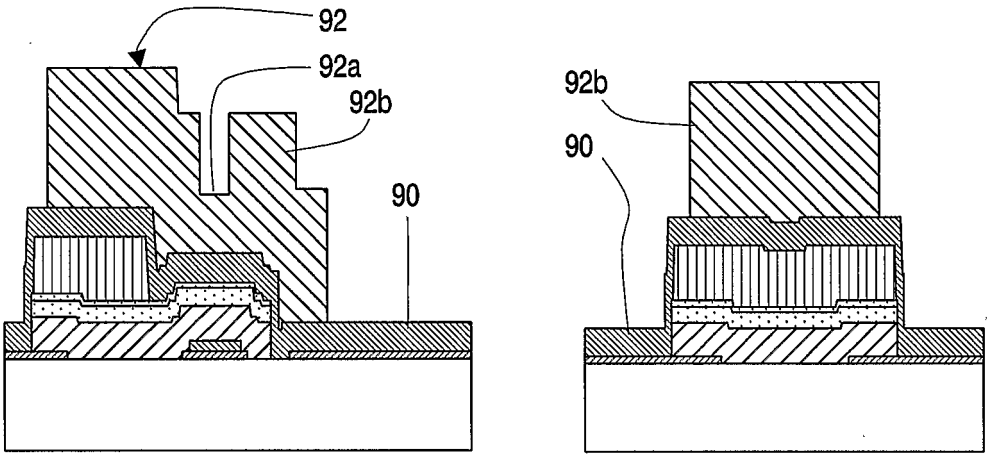

FIG.14A

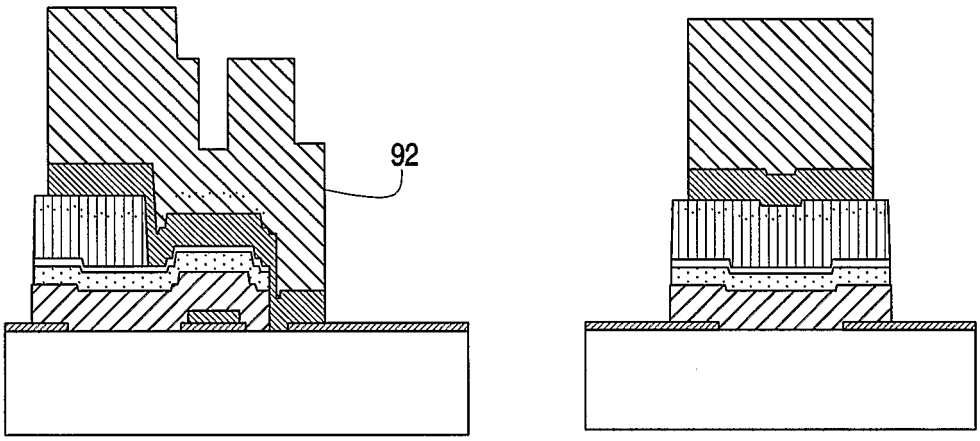

FIG.14B

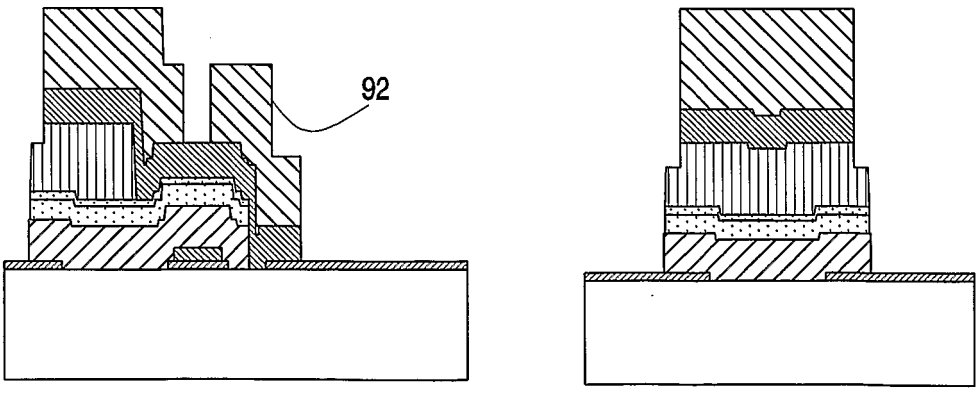

FIG.14C

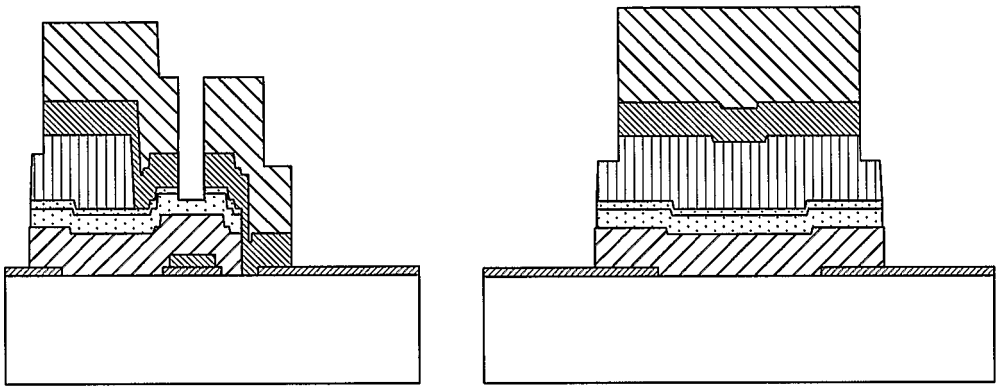

FIG.14D

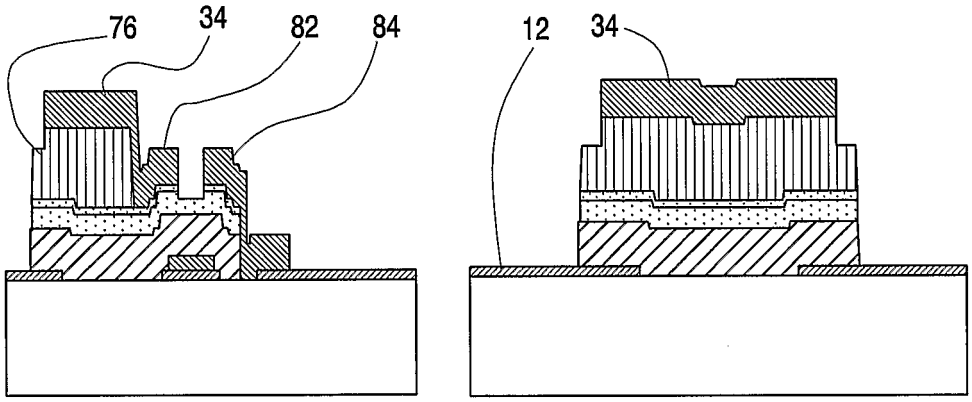

FIG.14E

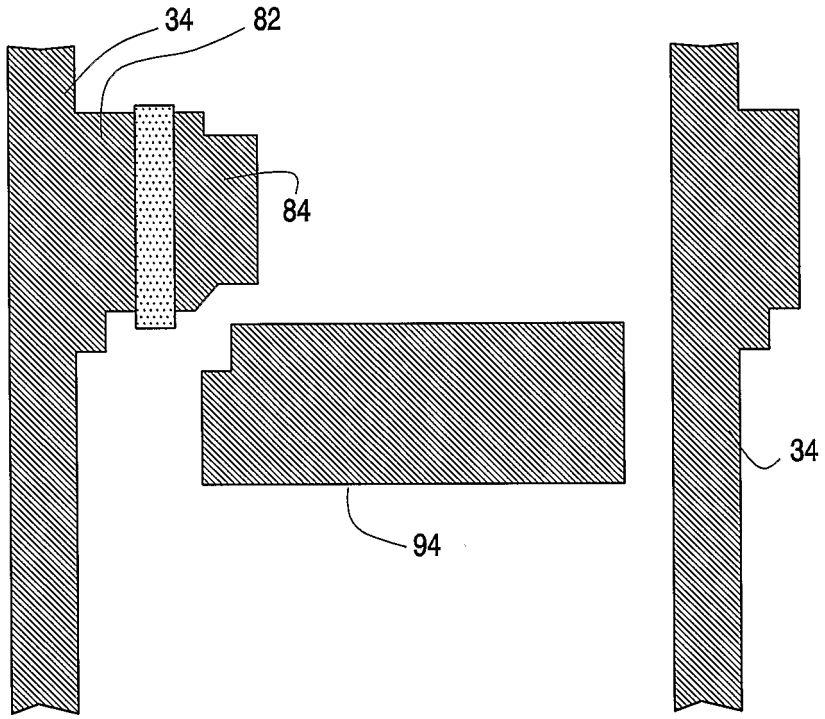

FIG.15

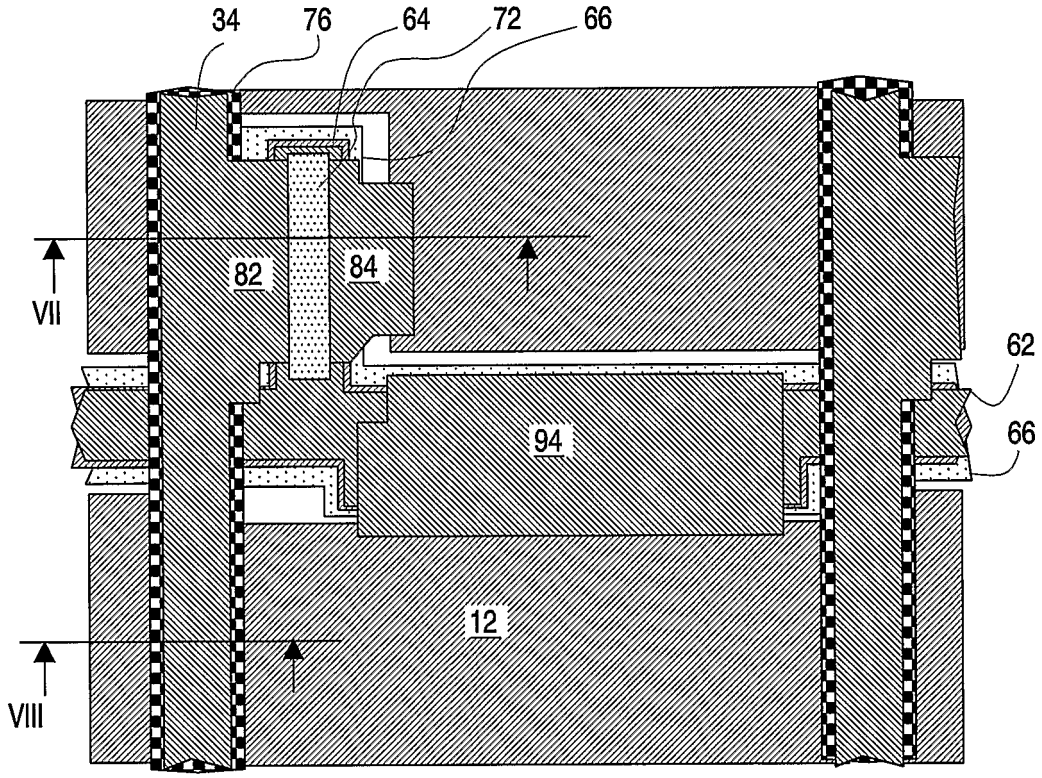

FIG.16

INTERNATIONAL SEARCH REPORT

International Application No
PCT/IB 03/05886

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G02F1/1362

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G02F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 650 358 A (GU TIEER ET AL) 22 July 1997 (1997-07-22) the whole document	1,9
A	US 5 724 111 A (KANOH HIROSHI ET AL) 3 March 1998 (1998-03-03) figure 3; example 1	1,9
A	US 6 372 534 B1 (DEN BOER WILLEM ET AL) 16 April 2002 (2002-04-16) column 5, line 56 - column 7, line 49; figure 4	1,9
A	US 5 682 211 A (YAO WILLIAM ET AL) 28 October 1997 (1997-10-28) column 4, line 3 - line 67; figures 3,4	1,9

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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Date of the actual completion of the international search	Date of mailing of the international search report
17 March 2004	25/03/2004

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Lord, R

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	US 6 097 454 A (TAKEMURA YASUHIKO ET AL) 1 August 2000 (2000-08-01) column 6, line 18 - column 8, line 17; figures 1,2	1,9
A	"PIXEL STRUCTURE FOR HIGH APRTURE RATIO ACTIVE MACTRIX LIQUID CRYSTAL DISPLAYS" IBM TECHNICAL DISCLOSURE BULLETIN, IBM CORP. NEW YORK, US, vol. 40, no. 11, 1 November 1997 (1997-11-01), pages 3-5, XP000739901 ISSN: 0018-8689 the whole document	1,9

INTERNATIONAL SEARCH REPORT

International lication No
PCT/IB 03/05886

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专利名称(译)	液晶显示器		
公开(公告)号	EP1576415A1	公开(公告)日	2005-09-21
申请号	EP2003775755	申请日	2003-12-09
[标]申请(专利权)人(译)	皇家飞利浦电子股份有限公司 法国IANĐ		
申请(专利权)人(译)	皇家飞利浦电子N.V. 法国，IAN D.		
当前申请(专利权)人(译)	LG.飞利浦液晶CO.LTD. 皇家飞利浦电子N.V.		
[标]发明人	FRENCH IAN D C O PHILIPS I P & STANDARDS		
发明人	FRENCH, IAN, D.,C/O PHILIPS I.P. & STANDARDS PARK, SUNG-IL,C/O PHILIPS I.P. & STANDARDS		
IPC分类号	G02F1/136 G02F1/1333 G02F1/1362		
CPC分类号	G02F1/136286 G02F1/133345 G02F1/136209 G02F2001/136295 G02F2201/40		
优先权	2002029699 2002-12-19 GB		
其他公开文献	EP1576415B1		
外部链接	Espacenet		

摘要(译)

用于液晶显示器的有源板具有布置为多个列的绝缘层（76），每个绝缘层列与两个相邻列的像素的像素电极（12）重叠。在衬底上形成不透明导体层并对其进行图案化以在绝缘层的顶部上限定列导体（34），并在薄膜晶体管层（66）的顶部上限定晶体管的源极和漏极。因此，绝缘层（76）限定在列导体（34）下方，使得它位于交叉的行和列导体之间。另外，绝缘层（76）的列与相邻的像素电极对（12）重叠，使得列导体可以与像素电极重叠，从而增加像素孔径。然而，透明像素电极（12）是要沉积的第一层。这为制造高质量有源矩阵LCD（AMLCD）显示器的工艺简化和相应的成本降低提供了优势。