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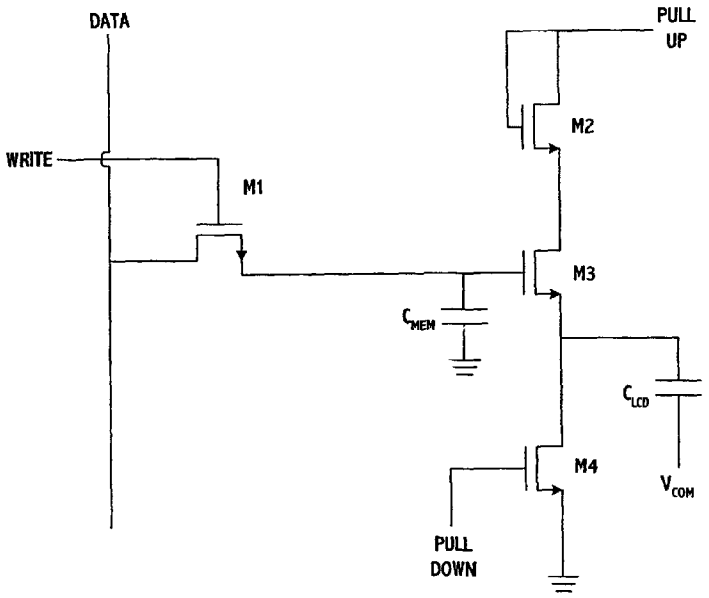

(57) Abstract: An enhanced frame buffer pixel circuit with two control transistors (Fig. 6) and a separate capacitor put in as a memory capacitor before the memory transistor yields a high contrast ratio by removing induced charge and solving a charge sharing problem between the memory CAPACITOR and the liquid crystal display (LCD) capacitor. The memory transistor may be made of either CMOS or PMOS. The frame buffer pixel can be used to drive binary displays which expresses ON and OFF only if a comparator is put in after the pixel electrode circuit to represent gray levels with reduced sub-frame frequency.

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

FRAME BUFFER PIXEL CIRCUIT FOR LIQUID CRYSTAL DISPLAY

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to pixel circuits for display systems, and more particularly relates to a frame buffer pixel circuit for a liquid crystal display.

Background of the Related Art

Figure 1 shows a related art display device 10. It includes a pixel circuit display panel 20 controlled by a display control circuit 30 having a frame memory 40. The related art pixel circuit display requires a grayscale representation of more than 8 bits per color, and an operating voltage low enough to enable a better powered display device, such as a laptop computer or a personal digital assistant (PDA). The related art pixel circuit utilizes an address driver for address selection and a scan driver for image writing and reading cycles during displaying.

Figure 2 illustrates a related art of an early stage frame buffer pixel for liquid crystal display. Initially, a voltage proportional to the Data level is stored at the Cmem memory capacitor during data write time when the Write signal is ON. Then, the stored voltage is transferred to the Cpixel capacitor when the Read signal is applied after data writing is finished. The frame buffer pixels enable a previously stored image to be displayed while new data for a new image is loading into the Cmem.

The related art frame buffer pixel circuit has various disadvantages. For example, there is a charge sharing between the Cmem memory capacitor and the Clcd capacitor, the two capacitors are shorted when the Read signal turned ON, as shown in Figure 3 (C)-(E). The voltage levels of the Cmem memory capacitor, shown in Figure 3(C), and the Clcd capacitor, shown in Figure 3(E), become equal after the Read signal is applied, shown in Figure 3(D). Hence, the capacitance of the Cmem memory capacitor has to be much larger than the capacitance of Clcd capacitor in order to minimize the charge sharing problem. However, even with a much larger Cmem memory capacitor, there is always some voltage drop due to the charge sharing effect.

Additionally, there is no charge drain at the Clcd capacitor. That is, the remaining charge at the Clcd node from the previous image interferes with the new voltage that is written for a new image. Specifically, the actual voltage level of the Clcd capacitor varies depending on the previous image voltage, as shown in Figure 3(E).

Moreover, the Clcd capacitor is driven not by power, but is driven by the charge from the Cmem memory capacitor. Thus, the Clcd capacitor needs to be optimized first in terms of its holding time and the capacitance of the Cmem memory capacitor. Due to these disadvantages, the related art frame buffer pixel provides poor brightness and contrast ratio.

Figure 4 illustrates a second related art frame buffer pixel circuit. The frame buffer pixel utilizes gate oxide of NMOS transistor M3 as a memory capacitor. The voltage according to Data level is stored at the gate capacitor of M3 during data writing time when Write signal is ON. When the data writing is finished, the Pullup signal corresponding to Read signal is turned ON and charging the pixel electrode (e.g., C_{lcd} capacitor). Before Pullup signal is applied, the Pulldown signal drains all charge previously stored in the pixel electrode. The charge drain of the C_{lcd} capacitor ensures the right voltage gets displayed, especially when the data level for the new image is lower than the previous image data level.

The simulation results of the frame buffer pixel of Figure 4 are shown in Figure 5. As shown in Figure 5(E), undesired charge is induced at the pixel electrode due to the intrinsic gate capacitor of M3 which makes another path to the ground with the C_{lcd} capacitor. These two capacitors working as a voltage divider determines the induced voltage at the C_{lcd} capacitor during data writing time. Referring to Figure 5, with the parameters used in the simulation, about one third of the voltage at the memory capacitor is induced during data writing time, as shown in Figures 5(C) and 5(E). The induced charge affects the image quality, especially the contrast ratio. To reduce the charge induction problem, the ratio of the gate capacitance C_{gs} to the C_{lcd} capacitance should be increased, and the stored charge should be kept for at least one frame time. Therefore, in order to achieve a high contrast ratio, the pixel circuit requires considerable space for the gate capacitance value which is much higher than the liquid crystal display (LCD) capacitor to hold the stored voltage in most mili-second frame time applications.

The above references are incorporated by reference herein where appropriate for appropriate teachings of additional or alternative details, features and/or technical background.

SUMMARY OF THE INVENTION

An object of the invention is to solve at least the above problems and/or disadvantages and to provide at least the advantages described hereinafter.

It is another object of the claimed invention to provide an enhanced frame buffer pixel circuit that can achieve high contrast ratio and display high quality images with shorter writing time.

In the preferred embodiment of the frame buffer pixel circuit, two separate capacitors are utilized to yield higher contrast ratio by minimizing the induced charge during data writing or reading time, keeping the dark level at its lowest brightness and therefore saving data writing time. The capacitance of the separate capacitor does not depend on that of each other and, therefore, can be designed independently such that the time constant is long enough to hold the stored charge for one frame time. The capacitance of the separate capacitors is not voltage-dependent contrary to the gate capacitance. The lcd capacitor Clcd is directly driven by the power source, the current flowing into the lcd capacitor is controlled by the voltage level stored at the memory capacitor. Furthermore, there is no charge sharing between the memory capacitor Cmem and the lcd capacitor Clcd. There is charge induced only when data read signal is on, however the amount of charge induction is same for all data level. Thus the charge induction does not alter the gray level and the charge induced at the lcd capacitor can also be minimized by using minimum-sized transistor. In the preferred embodiment of the frame buffer pixel circuit, an analog to pulse width modulation (PWM) converter can be put after the pixel electrode (i.e., lcd capacitor) Clcd. Specifically, a pixel capacitor Cpixel is preferably connected to a comparator with a reference voltage Vref to generate PWM pulses to drive binary displays such as ferroelectric liquid crystal displays and digital mirror displays (DMDs), reducing the sub-frame frequency significantly.

This pixel circuit with above described advantages can be applied in most displays which use active driving, such as TFT LCDs, liquid crystal on silicones (LCOSs), electro luminescence (EL) display, plasma display panels (PDPs) and field emission displays (FEDs), field sequential color display, projection display, and direct view display, such as a head mount display (HMD). This technique can also be used in LCOS beam deflector, phased-array beam deflector, and is especially effective in reflective display that adopt silicon substrate backplanes.

Additional advantages, objects, and features of the invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from practice of the invention. The objects and advantages of the invention may be realized and attained as particularly pointed out in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be described in detail with reference to the following drawings in which like reference numerals refer to like elements wherein:

Figure 1 is a diagram illustrating a general structure of a related art pixel panel display.

Figure 2 is a diagram illustrating a first related art frame buffer pixel circuit.

Figure 3 shows simulation results for the frame buffer pixel circuit of Figure 2.

Figure 4 is a diagram illustrating a second related art frame buffer pixel circuit.

Figure 5 shows simulation results for the frame buffer pixel circuit of Figure 4.

Figure 6 shows a refined frame buffer pixel circuit.

Figure 7 shows a frame buffer pixel circuit in accordance with another preferred embodiment of the present invention.

Figure 8 shows simulation results for the frame buffer pixel circuit of Figure 6.

Figure 9 shows a table of the Gate capacitance depending on the voltage applied to the gate.

Figure 10 shows a frame buffer pixel circuit with CMOS in accordance with a preferred embodiment of the present invention.

Figure 11 shows simulation results for the preferred embodiment frame buffer pixel of Figure 10, illustrating voltage levels at nodes with respect to time.

Figure 12 is a diagram of an embodiment of the present invention implemented using NMOS and PMOS transistors.

Figure 13 shows a frame buffer pixel circuit with PMOS in accordance with a preferred embodiment of the present invention.

Figure 14 is a circuit diagram illustrating a frame buffer pixel circuit with a comparator in accordance with a preferred embodiment of the present invention.

Figure 15 is a diagram showing how PWM wafer may be generated in accordance with one embodiment of the present invention.

Figure 16 shows a diagram illustrating PWM waveform generated from the pixel voltage and reference voltage of Figure 13.

Figure 17 shows a diagram illustrating the waveform of the reference voltage varied to apply gamma corrections.

Figure 18 shows a 1-panel projection display with field sequential color according to a preferred embodiment of the present invention.

Figure 19 shows a 2-panel projection display with partial field sequential color according to a preferred embodiment of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Preferred embodiments of the present invention will now be described with reference to the accompanying drawings. Figure 6 shows a first refined frame buffer pixel circuit. In this refined frame buffer pixel circuit, a memory capacitor Cmem is put in the related art frame buffer pixel circuit of Figure 4, eliminating the charge induction problem caused by the gate capacitance of transistor M3 with the Clcd capacitor, which forms an additional path to the ground. The image quality is greatly improved after the capacitor Cmem put in the related art frame buffer circuit and transistor M3 is preferably made from a minimum-sized transistor. Furthermore, as described below, the values of capacitors Cgs and Clcd can be optimized to achieve best image quality.

Figure 7 shows a second refined frame buffer pixel circuit. In this second refined frame buffer pixel circuit, two field effect transistors (FETs), M1 and M2, are used as control or pass transistors. A pullup transistor M4 with an input signal corresponding to the Read signal is coupled between in after the memory transistor M3 and the LCD capacitor Clcd and a Pulldown transistor M5. In this circuit, when the Write signal is ON, the pass transistors, M1 and M2, pass the pixel data value through to the gate of the M3 transistor. At this time, the M3 transistor is not in a conducting state since the Pullup signal is kept low so that no current is flowing through the source and drain electrodes of either M4 or M5 transistors.

After loading the data value, the M1 and M2 transistors are preferably turned off. This will keep the new pixel data value stored on the gate of M3. Subsequently, at the end of the display of previous data value, the Pulldown signal is switched to high and turns on the M5 transistor, which then discharges any charge on the pixel electrode, Clcd. Afterwards, the Pulldown signal is turned low and turns off the M5 transistor. Then, the Pullup signal is switched to high and turns on the M4 transistor, which causes current to flow through the M3 transistor. The data value stored on the gate of the M3 transistor controls the amount of current, which determines the voltage charged at the pixel electrode, C_{lcd} proportionally to the voltage level when the Read signal is applied. The two pass transistor arrangement of this embodiment is advantageous in a number of respects. First, the use of two pass transistors guarantees that all voltage in one node is transferred to the other node. In contrast, if only one transistor is used, there is voltage drop at a lower or upper range of the applied voltage. For example, if NMOS is used, when upper rail voltage VDD is applied, VDD-Vth is transferred to the other node. Vth=threshold voltage of the NMOS. For PMOS, VSS+Vth is transferred to the other node as with lower rail voltage input.

Second, the charge-sharing and charge-inducing problems are eliminated because transistor M4 disconnects the gate capacitor M3 and the pixel capacitor C_{lcd}. Voltage according to

the Data level is first stored in the memory capacitor, the gate capacitor of transistor M3, during data writing time. Since the two capacitors are isolated due to M4 transistor, there is no charge induced during data writing time, which is clearly shown in Figure 8(C) and (D).

Figure 8 shows simulation results performed for the refined frame buffer pixel Figure 7. In Figure 8(E), the voltage at the C_{lcd} capacitor remains stable over an entire frame time for each Data level, and there is no induced charge at the LCD when Write signal is on. Especially, the value of C_{gs} of the M3 transistor and C_{lcd} can be optimized independently to hold the charge stored in each capacitor for one frame time since there is no parasitic path connecting the two capacitors. The darkest level remains at its lowest brightness level with no change for the entire frame time, and the contrast ratio increases with no brightness change. Particularly, the contrast ratio does not depend on whether a separate capacitor is used or a gate capacitor is used. A previously stored image can therefore be displayed with no significant deterioration. Regarding optimization, it is noted that the C_{gs} to the M3 and C_{lcd} can be optimized independently since the M4 transistor between the two disconnects any possible parasitic electrical path. However there is an additional electrical path with the C_{gs} of M4 and C_{lcd} and charge is induced at the C_{lcd} when Read signal is turned on. The charge induced at the C_{lcd} during data read time is same no matther what voltage is stored at the Cgs of M3. It is not critical to optimize the Cgs of M4 and the C_{lcd}. Using minimum sized transistor for M4 is therefore desirable.

Furthermore, the gate capacitance used in this pixel circuit depends on the voltage applied to the gate, as shown in Figure 9. In Figure 9, the values of gate capacitor are acquired from the particular simulation shown in Figure 8 with NMOS and PMOS having widths of 7.5 μm and 7.3 μm respectively, and lengths of 9.2 μm and 9.5 μm respectively. The threshold voltage of the PMOS and NMOS are 0.94 V and 0.77 V respectively. If the voltage applied to the gate of a device becomes close to the threshold voltage of the device, the gate capacitance starts to decrease. Therefore, a pixel with a gate capacitor as a storage capacitor has the disadvantage of inconsistent capacitance, requiring that the stored voltage at M3 be larger than the threshold voltage of M3.

Also, it is noted that there could be a charge induced at the C_{lcd} capacitor when the Read signal is on, if the ratio of the V_{gs} of M4 to the C_{lcd} capacitance is comparable, even though there is no induced charge at the C_{lcd} capacitor due to the voltage applied at the memory capacitor. The induced charge is same regardless of the voltage stored at the memory thus causing no decrease of contrast ratio.

Figure 8(E) shows the charge induced at the C_{lcd} capacitor during data reading time when the displaying Data level is zero. This results from the parasite capacitance of M4, which makes an electrical path to the ground with the C_{lcd} capacitor. But this induced charge can be removed easily by minimizing the gate capacitor of M4 and maximizing the C_{lcd} capacitance. Still, the optimization of the C_{lcd} capacitor and C_{gs} of M3 can still be done independently.

Figure 10 shows a first preferred embodiment of a frame buffer pixel circuit of the present invention. In this preferred embodiment, the pixel circuit includes a separate capacitor, C_{mem}, which is put in before the transistor M3. The C_{mem} is a memory capacitor, and is used to replace the parasitic gate capacitor of the CMOS transistors. This pixel circuit with a separate capacitor C_{mem} yields higher contrast ratio by removing the induced charge at C_{lcd} during data writing and reading time, keeping the dark level at its lowest brightness. Thus, the design of a frame buffer pixel becomes easier because of the added separate capacitor. The optimization of the two capacitors, C_{mem} and C_{lcd}, can be done independently. Further, the capacitance of C_{mem} does not depend on the stored voltage while the gate capacitance changes its value according to the stored voltage. The stored voltage can be kept for the same duration regardless of the voltage level. Any suitable capacitor can be used to form C_{mem}. It is preferable, however, that C_{mem} be made by using typical CMOS processes that have double POLY layers, such as the AMI 0.5 um double-poly triple-metal CMOS process. For this circuit, the sub-frame frequency and the pixel size are correlated. For a field sequential color display with frame frequency of 60 Hz, the total sub-frame frequency will be 180 Hz and the sub-frame time is about 5.5 msec. With higher sub-frame frequency the voltage holding time, RC time is reduced. Thus, the pixel is also decreased since the RC time which is proportional to the capacitor size is decreased. The size of capacitor take major area in a pixel. Also, in this circuit the capacitors may be optimized. Determining the size of capacitor to hold the stored voltage for a certain period of time will achieve this optimization. Since C_{mem} and C_{lcd} can be independently determined to hold the stored voltages for the same sub-frame time the capacitor can be same. For a TFT display which requires the frame frequency of 60 Hz, about 100 ff capacitance may be used to hold 95% of the stored voltage for 16.7 msec. A field sequential color display which has three times larger sub-frame frequency requires about 30 ff capacitance, which is one-third of the capacitance for the TFT display.

According to this embodiment, there is no charge sharing between the storage capacitor, C_{mem}, and the LCD capacitor, C_{lcd}, as shown in Figure 11 (A)-(E). A charge induced at the LCD electrode can be minimized by using minimum-sized transistor. The LCD electrode

is directly driven by the power source and the charged voltage is controlled by the voltage level stored at the memory capacitor, C_{mem}. In this pixel circuit, each capacitor can be designed independently such that the time constant is long enough to hold the stored charge for one frame time. Particularly, the capacitance of the separate capacitor is not dependent on the stored voltage level. Additionally, there is no trade off between brightness and contrast ratio. The brightness and contrast ratio can thus be improved at the same time. Data writing time is also limited only by the entire frame time since the data writing and displaying previous image is per formed simultaneously. This data writing time limitation releases the burden of data processing time, especially the operation speed of shift registers while non-frame buffer pixel requires as fast data write time as possible to get more viewing time. The frame buffer pixel circuit thus provides high quality image by saving data writing time.

Further, this embodiment of the frame buffer pixel circuit complements the low brightness of displays, especially the Field Sequential Color displays. The frame buffer pixel technology can also be used with any form of analog liquid crystal (LC) modes, such as HAN (hybrid aligned nematic), OCB (optically compensated birefringence), ECB (electrically controlled birefringence), FLC (ferro-electric liquid crystal). Most of all, there is tremendous flexibility in designing the frame buffer pixel circuit, almost any type of capacitor can be used for the memory capacitor and the liquid crystal capacitor.

For example, a combination of NMOS and PMOS transistors can be used as a capacitor that compensates the voltage dependent characteristic of the NMOS and PMOS transistors. If the gate capacitors of PMOS and NMOS are used in parallel for the memory, the total capacitance is the sum of the two capacitor and the combined capacitor will not experience abrupt decrease near threshold voltage. For example an NMOS capacitor will only experience capacitance drop near a threshold voltage of NMOS, about 0.7 V, but the combined is tolerant over the decrease of NMOS gate capacitor at the threshold of NMOS, thanks to that of PMOS since the gate capacitance is not affected. Figure 12 shows a circuit constructed in this manner.

Figure 13 illustrates a frame buffer pixel circuit according to another preferred embodiment of the present invention. Referring to Figure 13, the M3 transistor is preferably a PMOS. The PMOS is connected to the opposite signal of Pullup and Read respectively because these transistors work as a gate transistor supplying the current source in the circuit. In this embodiment, transistors M3, M4, and M5 may be PMOS transistors. In this case, the pixel voltage will vary from VSS to GND, where V22<0. And, the polarity of the pulses for M3,

M4, and M5 need to be reversed for appropriate operation. Further, the data will also be negative too. In addition, both the first embodiment and the second embodiment, the M2 transistor can be omitted without loss of any general functions or performance of the frame buffer circuit and any of the advantages over the conventional frame buffer circuit.

Figure 14 shows the third preferred embodiment of the claimed invention. In this scheme, a frame buffer pixel circuit with an analog to PWM (pulse width modulation) converter is illustrated. A comparator is put in after the pixel electrode. The comparator compares the voltage stored at pixel capacitor and a voltage, V_{ref}, supplied globally at the same time when the pixel electrode is charged. If $V_{pixel} > V_{ref}$, the voltage at the pixel electrode is 5 volt or the driving voltage (VDD) and if $V_{pixel} < V_{ref}$, the voltage at the pixel electrode is 0 volt or ground (GND). The PWM pulses generated from the comparator is used to drive binary displays such as ferroelctric liquid crystal display(FLCD) and digital mirror display(DMD) in a reduced sub-frame frequency. In this embodiment, the addition of the comparator is designed to drive an analog displays. The shape of Vref, as shown in Figure 15, determines how long 5 volt level and 0 volt level are maintained respectively.

Figure 16 shows the PWM waveforms generated by the global reference voltage V_{ref} and the stored pixel voltage V_{pixel}. The PWM waveform at the pixel electrode with a common electrode held at either VDD or GND switches a binary device either ON or OFF. Depending on the pixel voltage the ON time and OFF time are determined, enabling gray level representation in binary with reduced sub-frame frequency. The typical binary devices are devices like deformable micro mirror device (DMD) and ferro-electric liquid crystal display (FLCD) which use Field Sequential Color method to implement full color images. The PWM waveform significantly reduces the number of switching, as a result, the reduced number of switching increases the life time of the DMD and lessen the burden of switching time for the FLCD, allowing more gray scale levels. In other word, a higher quality of image display is achieved due to the reduced switching time. Further, the waveform of the V_{ref} can be varied by applying gamma correction, as shown in Figure 17. Since light intensity is not typically linearly proportional to the analog voltage, gamma compensation is preferable for generating better image.

The frame buffer pixel circuit of the claimed invention can be applied to the Field Sequential Color display which has lower brightness than 3-panel display but whose optical structure is very compact. The circuit can also be applied to the reflective and transmission display. It will be more effective in the reflective display that usually adopts silicon substrate

backplanes, such as liquid crystal on silicon (LCOS). Further, the circuit can be applied to the direct view display and projection display, such as a phosphate buffered saline (PBS) display system. Direct view display includes head mount display (HMD), displays for monitor, personal digital assistant (PDA), view finder, and etc. Examples of projection display with field sequential color are shown in Figures 18 and 19. In Figure 18, a 1-panel projection display with field sequential color is illustrated. In Figure 19, a 2-panel projection display with partial field sequential color is illustrated. The main purpose of the frame buffer pixel circuit is to increase the brightness of the display with no loss of contrast ratio. This invention will be effective in these applications yet it can be applied to 3-panel projection display to increase the brightness of the system more.

The present invention has been described relative to a preferred embodiment. Improvements or modifications that become apparent to persons of ordinary skill in the art only after reading this disclosure are deemed within the spirit and scope of the application.

The foregoing embodiments and advantages are merely exemplary and are not to be construed as limiting the present invention. The present teaching can be readily applied to other types of apparatuses. The description of the present invention is intended to be illustrative, and not to limit the scope of the claims. Many alternatives, modifications, and variations will be apparent to those skilled in the art. In the claims, means-plus-function clauses are intended to cover the structures described herein as performing the recited function and not only structural equivalents but also equivalent structures.

WHAT IS CLAIMED IS:

1. A frame buffer pixel systems, comprising:

a storage unit for storing a first data value charged during a frame time;

a first controller for enabling the storage of the first data value;

a second storage unit for displaying a second data during a frame;

a display for displaying the second data value stored in the second storage;

a second controller to enable the second storage, initiating the display;

a drain for draining the data value after displaying; and

a third controller for enabling the drain.

2. The system according to claim 1, wherein the first storage unit comprises a capacitor, whose capacitance is independent from the stored data value, and a gate transistor.

3. The system according to claim 2, wherein the capacitor comprises a complementary metal oxide semiconductor (CMOS) having double POLY layers.

4. The system according to claim 2, wherein the gate transistor comprises a NMOS transistor or a PMOS transistor.

5. The system according to claim 1, wherein the first controller comprises a field effect transistor (FET).

6. The system according to claim 5, wherein the first controller comprises a pass gate consisting of an NMOS transistor and a PMOS transistor controlled by Write and Inverted Write signals respectively.

7. The system according to claim 1, wherein the second controller comprises a gate to a Read signal.

8. The system according to claim 1, wherein the display comprises a capacitor, which can be independently optimized to hold the stored charge for one frame time.

9. The system according to claim 1, wherein the third controller comprises a gate connected to a Pulldown signal.

10. The system according to claim 1, wherein the display is a liquid crystal display capacitor.

11. A frame buffer pixel system, comprising:

a first storage unit for storing a first data value charged during a frame time;

a first controller for enabling the storage of the first data value;

a second storage unit for displaying a second data value during a frame;

a display for displaying the second data value stored in the second storage unit;

a second controller to enable the second storage, initiating the display;

a drain for draining the data value after displaying;

a third controller for enabling the drain; and

an analog to pulse width modulation (PWM) converter inserted after the second storage.

12. The system according to claim 11, wherein the first storage unit comprises a capacitor, whose capacitance is independent from the stored data value, and a gate transistor.

13. The system according to claim 12, wherein the capacitor comprises a complementary metal oxide semiconductor (CMOS) having double POLY layers.

14. The system according to claim 12, wherein the gate transistor comprises a NMOS transistor or a PMOS transistor.

15. The system according to claim 11, wherein the first controller comprises a field effect transistor (FET).

16. The system according to claim 15, wherein the first controller comprises a pass gate consisting of an NMOS transistor and a PMOS transistor controlled by Write and Inverted Write signals respectively.

17. The system according to claim 11, wherein the second controller comprises a gate connected to a Read signal.

AMENDED CLAIMS

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18. The system according to claim 11, wherein the display comprises a capacitor, which can be independently optimized to hold the stored charge for one frame time.

19. The system according to claim 11, wherein the third controller comprises a gate-connected to a Pulldown signal.

20. The system according to claim 11, wherein the converter comprises a pixel capacitor, a reference voltage and a comparator.

21. The system according to claim 20, wherein the reference voltage swing within the voltage range generated from the frame buffer pixel.

22. An analog frame buffer pixel system, comprising:

a first storage unit for storing first analog data;

a first controller for enabling storage of the first analog data in the first storage unit;

a second storage unit for storing second analog data proportional to the first analog data and corresponding to a grayscale pixel value to be displayed;

a display for displaying the pixel value corresponding to the second analog data stored in the second storage unit;

a second controller to enable storage of the second analog data into the second storage unit; and

a drain unit for draining voltage from the second storage unit after the pixel value is displayed.

23. The system according to claim 22, wherein the first storage unit comprises a capacitor having a capacitance independent from the first data stored in the first storage unit, said capacitor being coupled to a pass gate.

24. The system according to claim 23, wherein the capacitor comprises a complementary metal oxide semiconductor (CMOS) having double POLY layers.

25. The system according to claim 23, wherein the pass gate includes at least one of an NMOS transistor and a PMOS transistor.

26. The system according to claim 22, wherein the first controller comprises a field effect transistor (FET).

27. The system according to claim 26, wherein the first controller comprises a pass gate including an NMOS transistor and a PMOS transistor controlled by Write and Inverted Write signals respectively.

28. The system according to claim 22, wherein the second controller comprises a transistor having a gate coupled to a Read signal.

29. The system according to claim 22, wherein the display comprises a pixel electrode and a capacitor, the capacitor being independently optimized to hold a charge corresponding to the pixel value for one frame time.

30. The system according to claim 22, wherein the drain unit comprises a transistor having a gate connected to a Pulldown signal.

31. The system according to claim 22, wherein the display is a liquid crystal display.

32. The system of claim 22, further comprising:

an analog to pulse width modulation (PWM) converter coupled to an output of the second storage unit.

33. The system according to claim 22, further comprising:

a power source coupled to the second storage unit which includes a capacitor,

wherein the second controller allows the power source to charge the capacitor of the second storage unit to a value which corresponds to the second analog data, the second controller allowing the power source to charge the capacitor of the second storage unit through the first storage unit based on the first analog value.

34. A frame buffer pixel circuit for a display system, comprising:

a first storage unit which stores first analog data;

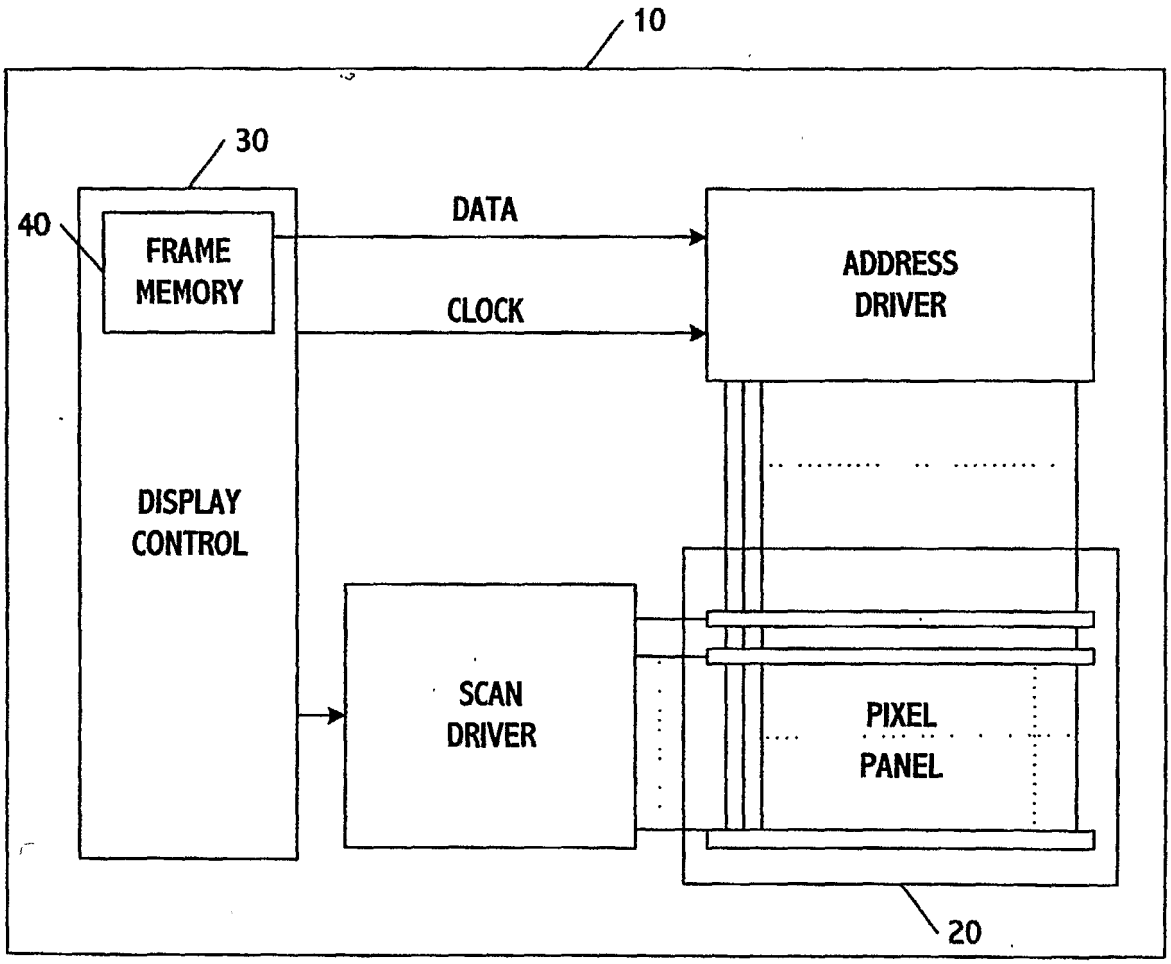
a second storage unit which stores second analog data proportional to the first analog data in the first storage unit;

a controller which couples the first storage unit to the second storage unit to enable storage of the second analog data in the second storage unit; and

a pixel electrode for displaying a pixel value corresponding to the second analog data stored in the second storage unit.

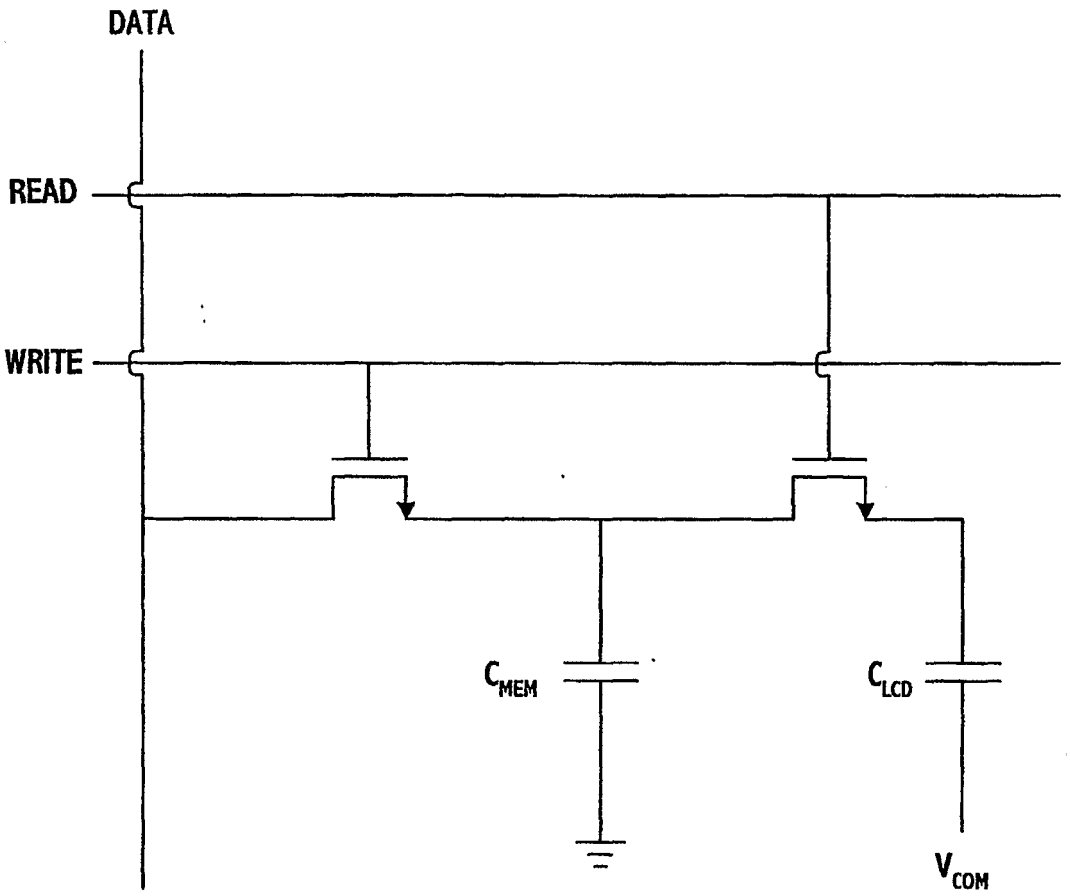
35. The circuit according to claim 34, further comprising:

a power source coupled to the second storage unit which includes a capacitor, wherein the controller allows the power source to charge the capacitor of the second storage unit to a value which corresponds to the second analog data based on the first analog value.



DISPLAY DEVICE

FIG. 1
BACKGROUND ART



FRAME BUFFER PIXEL

FIG. 2
BACKGROUND ART

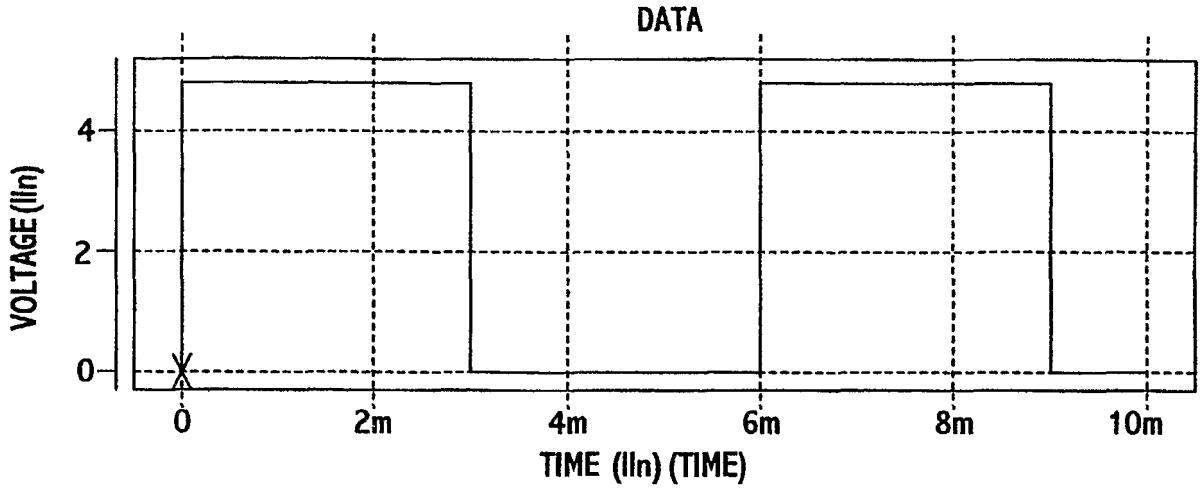


FIG. 3(A)

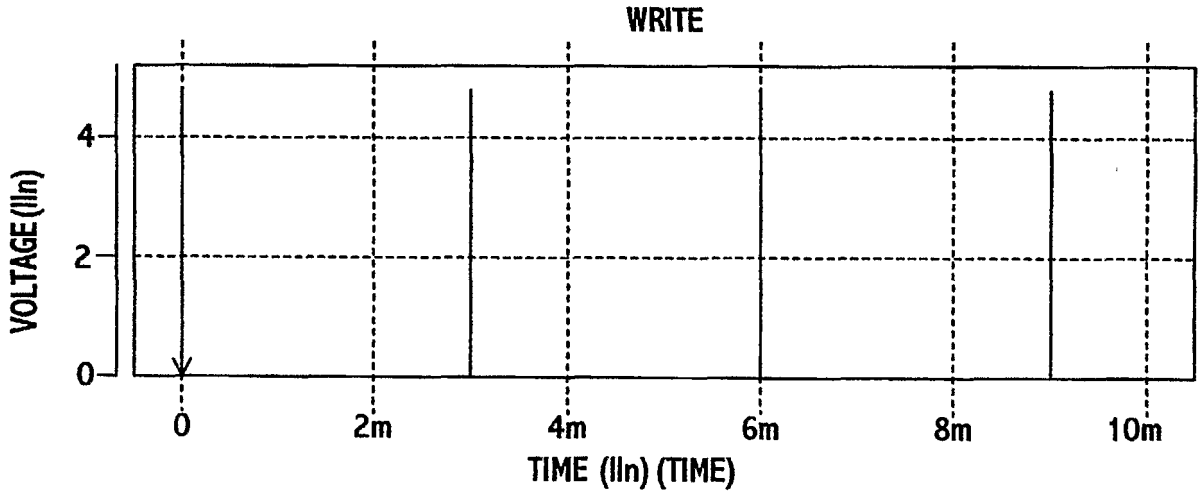


FIG. 3(B)

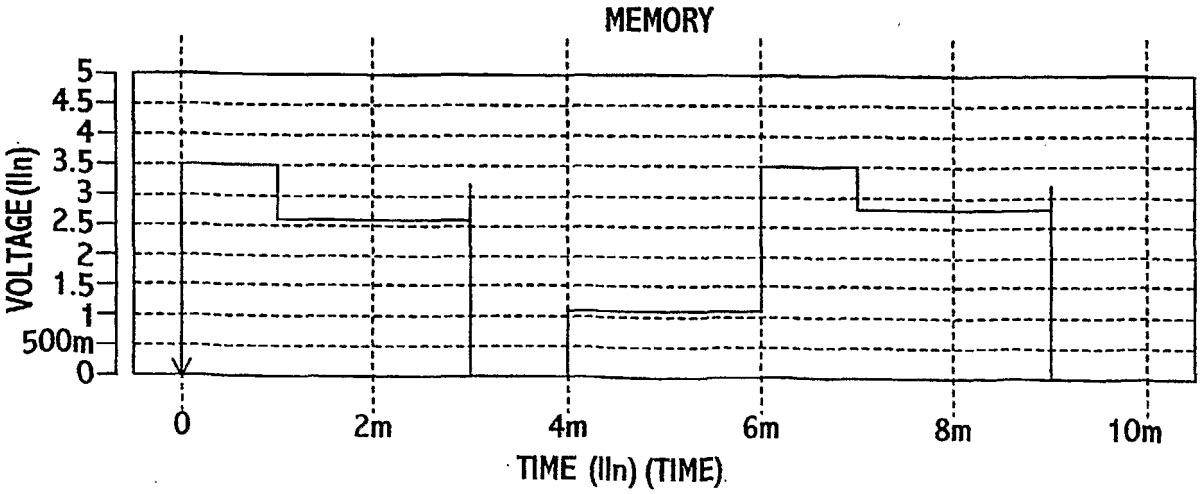


FIG. 3(C)

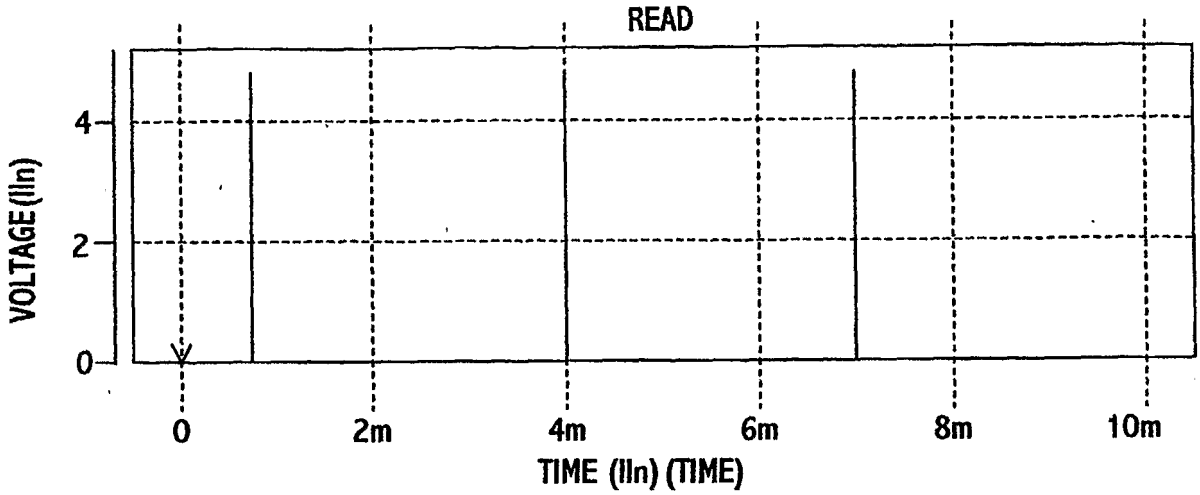

READ
VOLTAGE (lln)
4
2
0
0
2m
4m
6m
8m
10m
TIME (lln) (TIME)

FIG. 3(D)

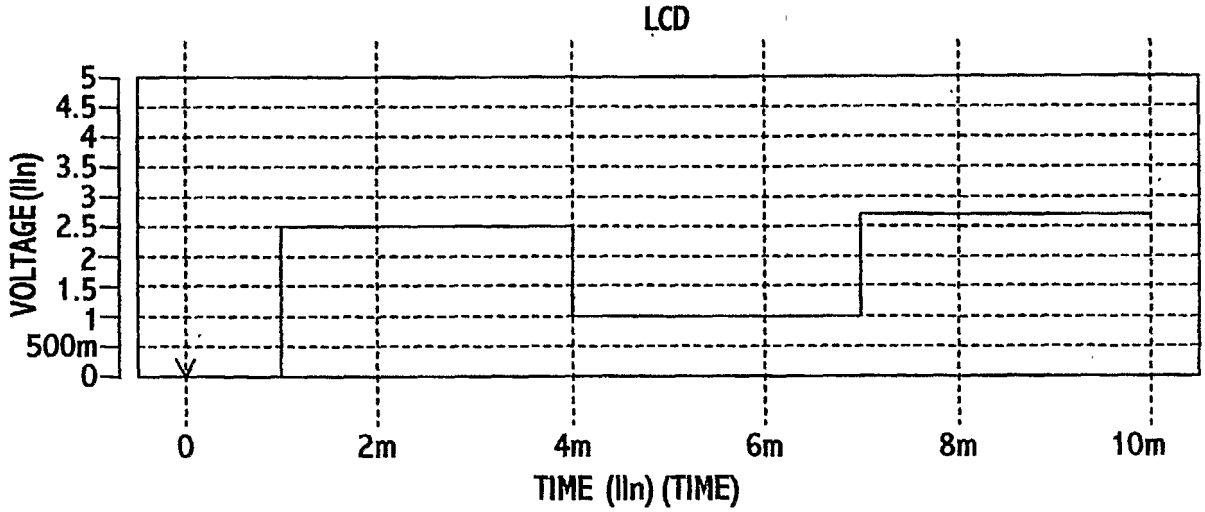
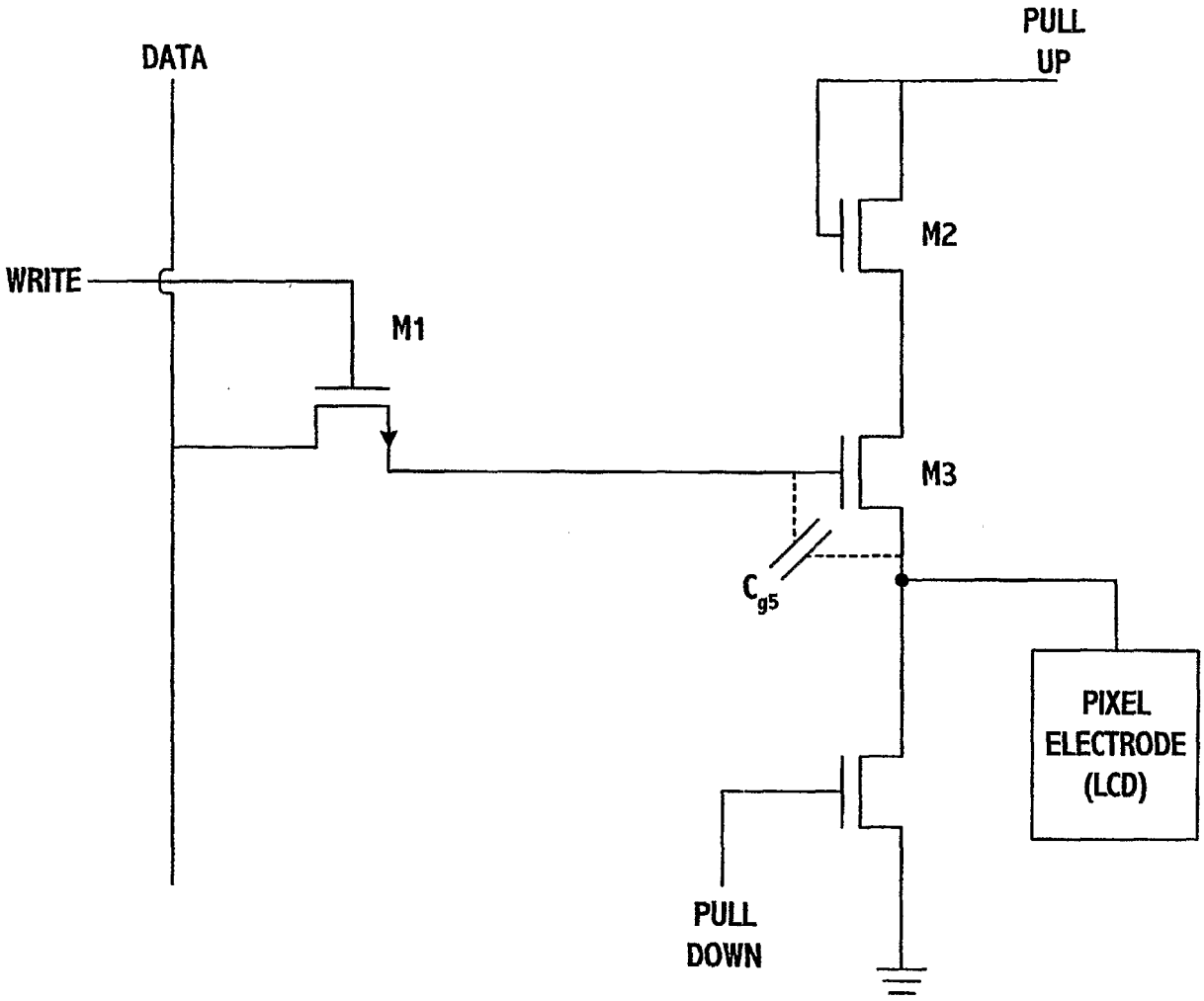

LCD
VOLTAGE (lln)
5
4.5
4
3.5
3
2.5
2
1.5
1
500m
0
0
2m
4m
6m
8m
10m
TIME (lln) (TIME)

FIG. 3(E)



FRAME BUFFER PIXEL

FIG. 4
BACKGROUND ART

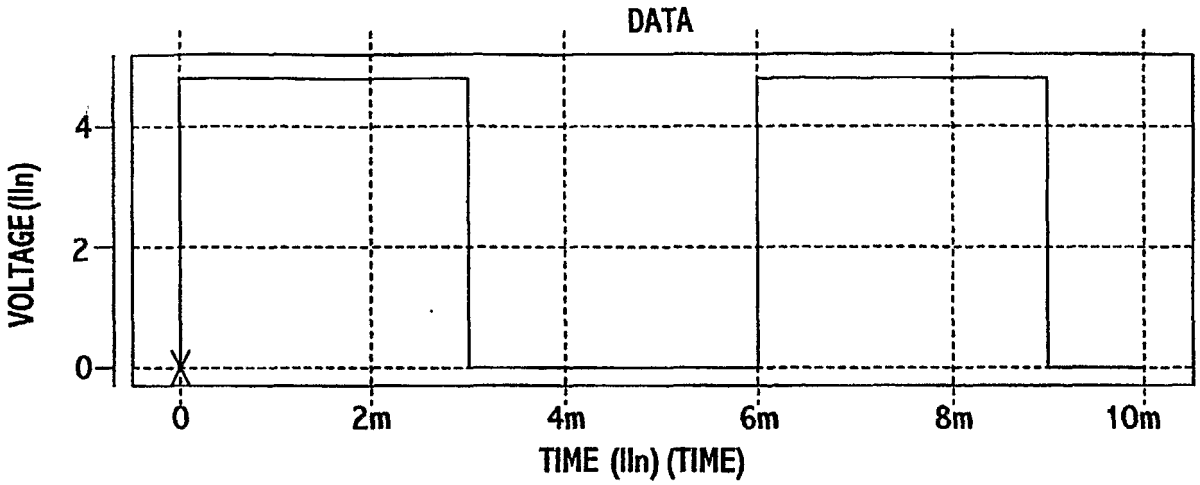


FIG. 5(A)

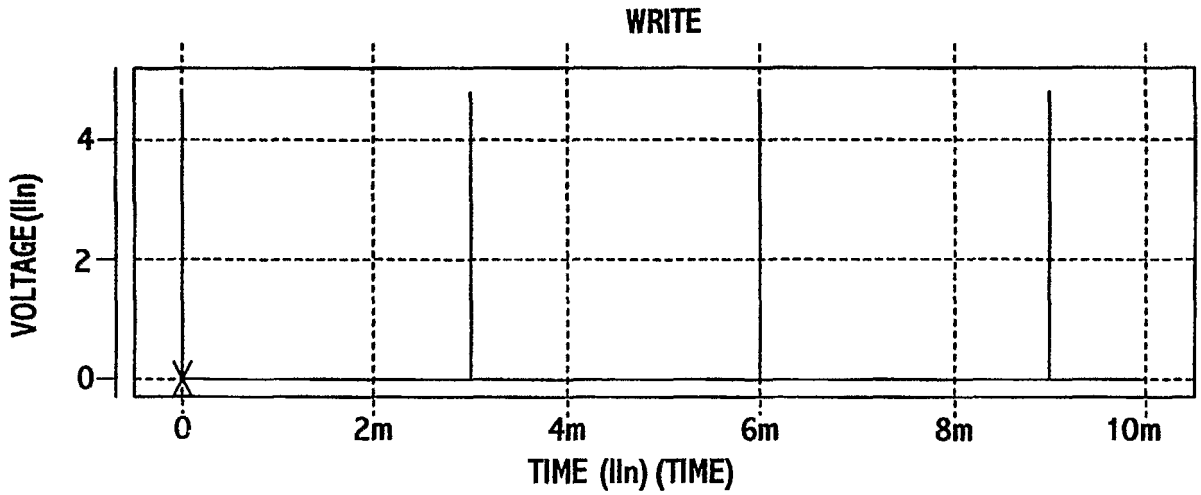


FIG. 5(B)

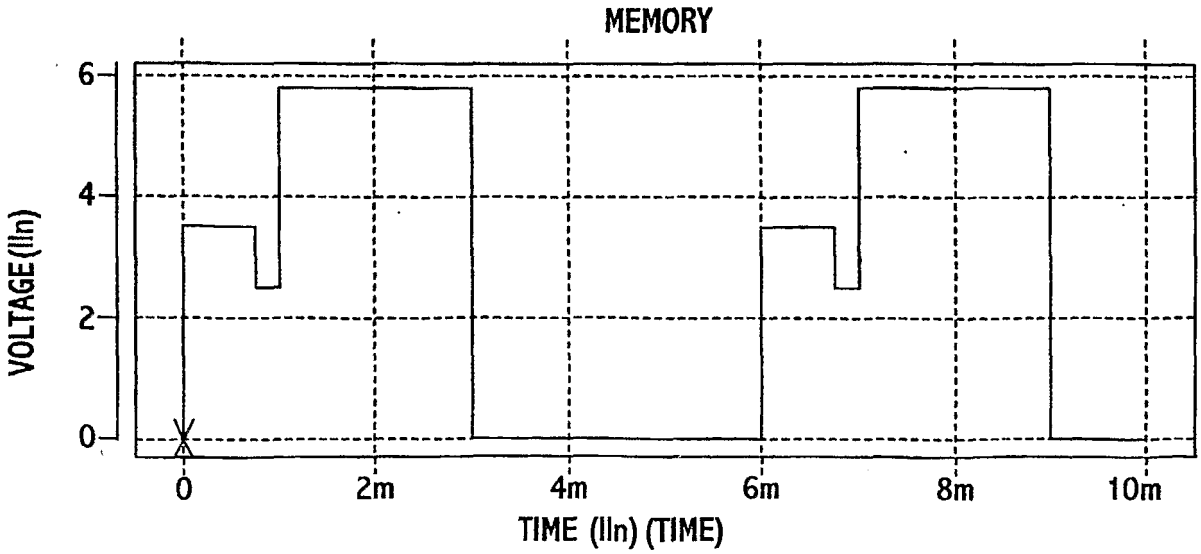


FIG. 5(C)

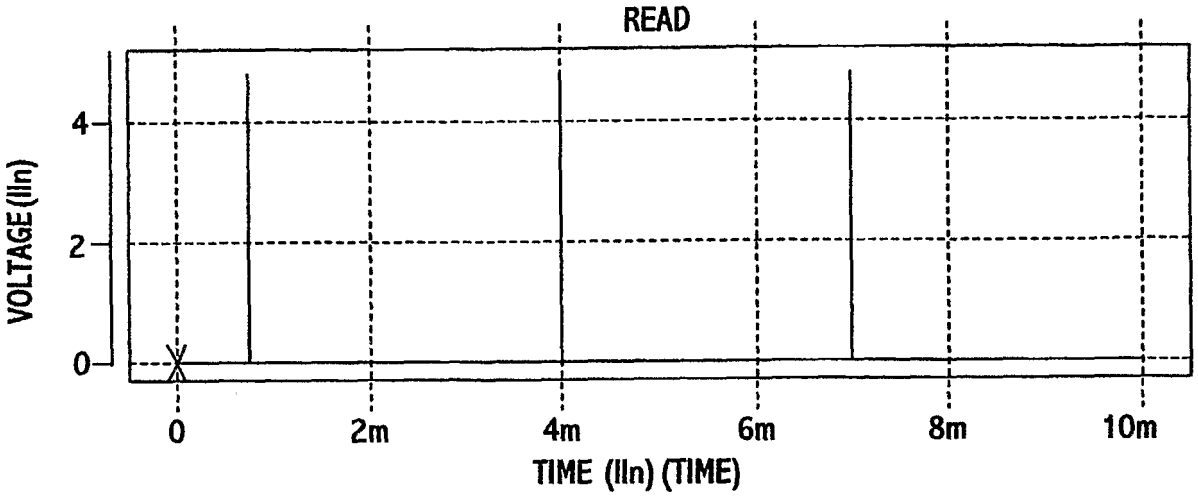

READ
VOLTAGE (lln)
4
2
0
0
2m
4m
6m
8m
10m
TIME (lln) (TIME)

FIG. 5(D)

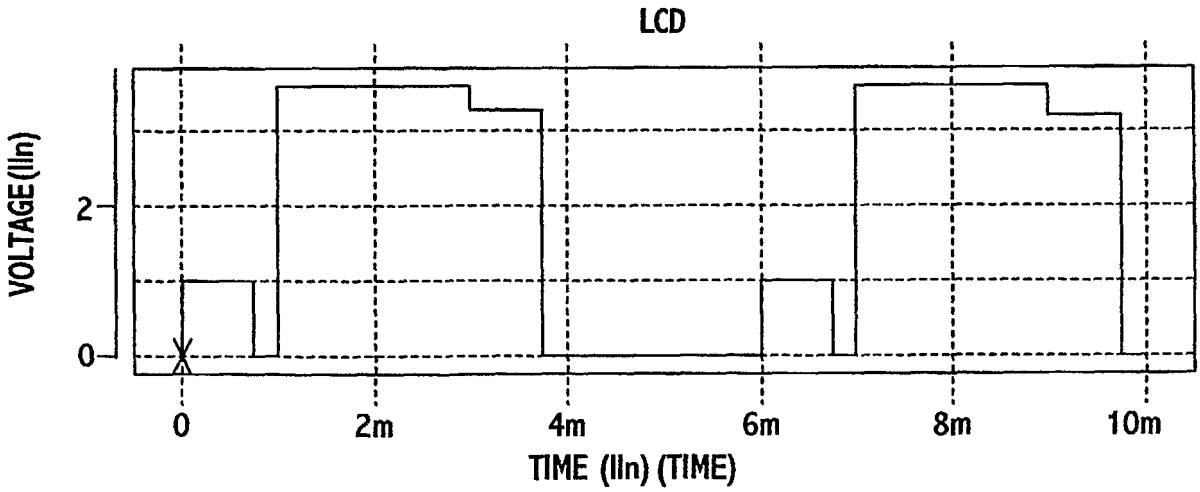

LCD
VOLTAGE (lln)
2
0
0
2m
4m
6m
8m
10m
TIME (lln) (TIME)

FIG. 5(E)

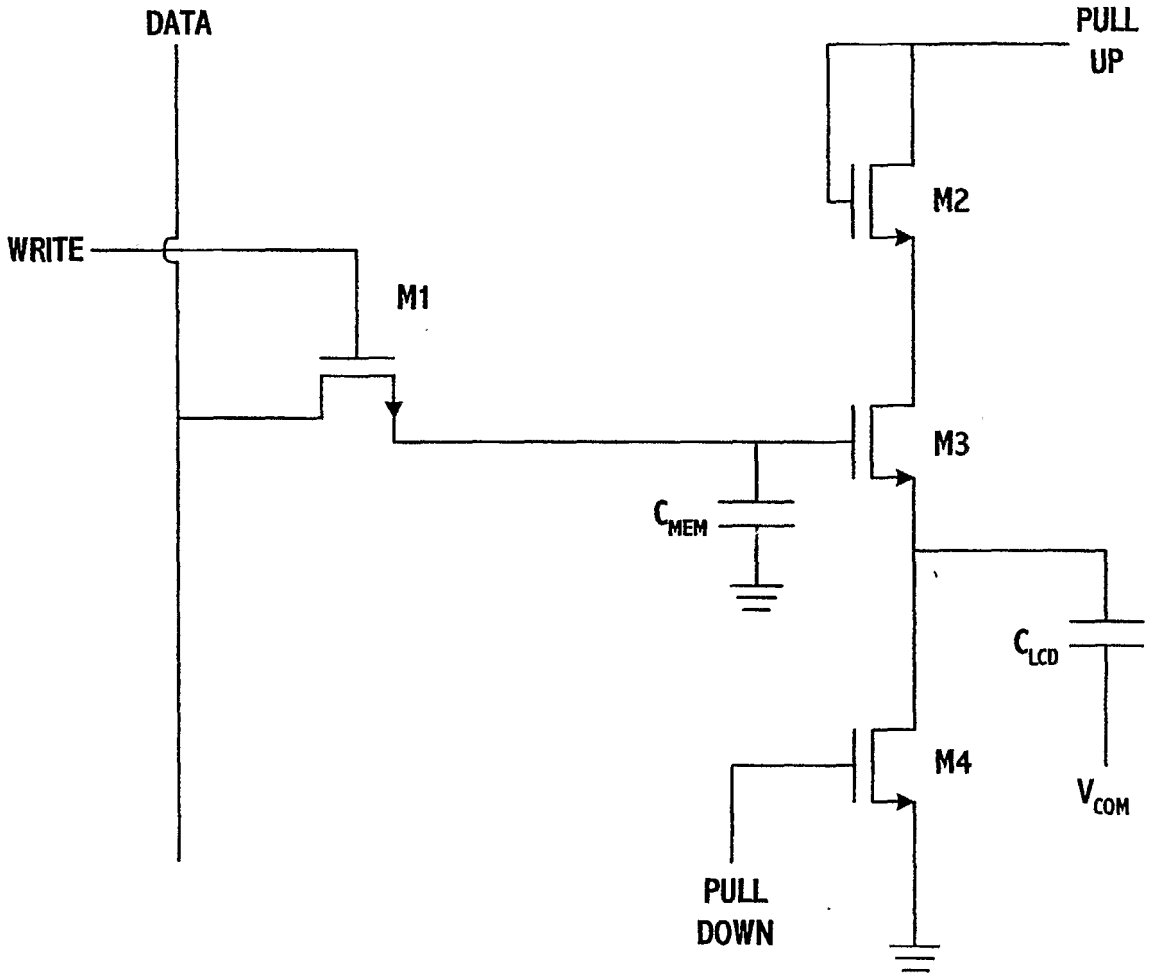
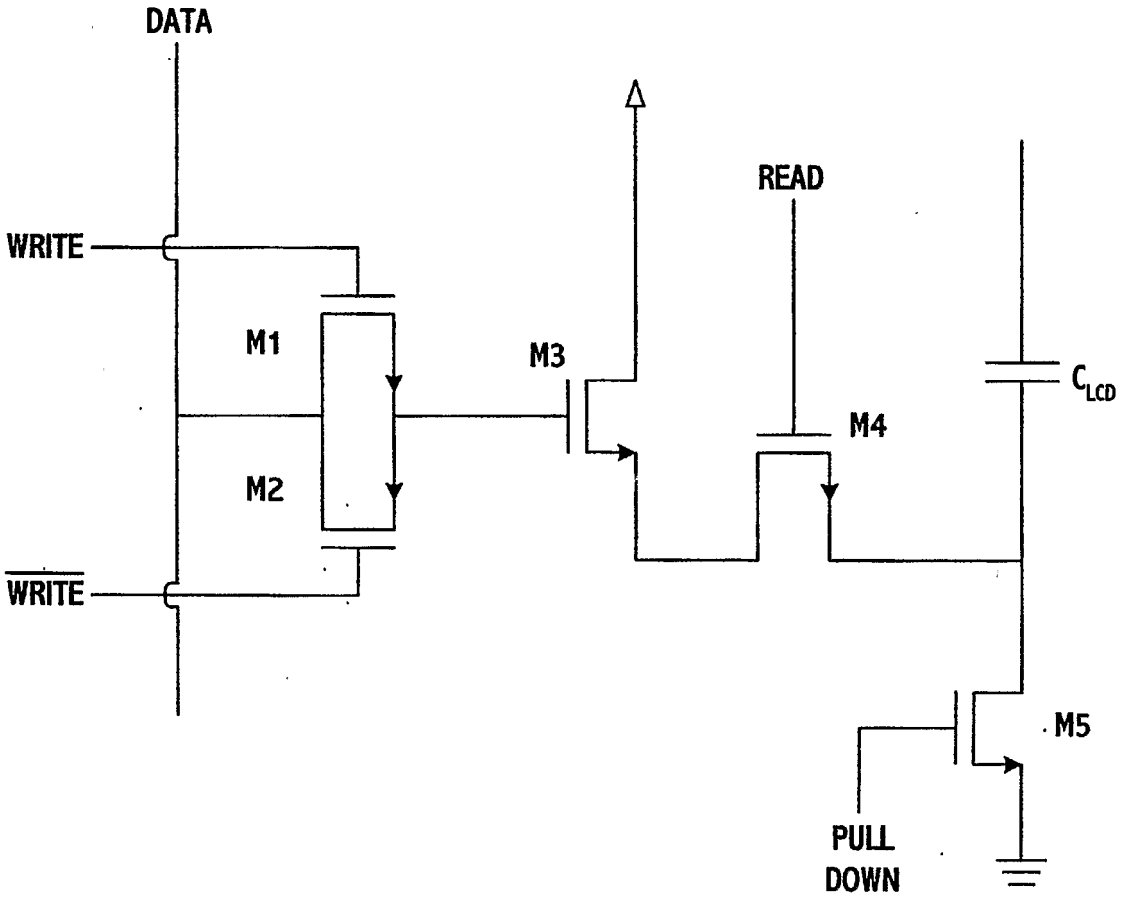


FIG. 6



A REFINED FRAME BUFFER PIXEL CIRCUIT

FIG. 7

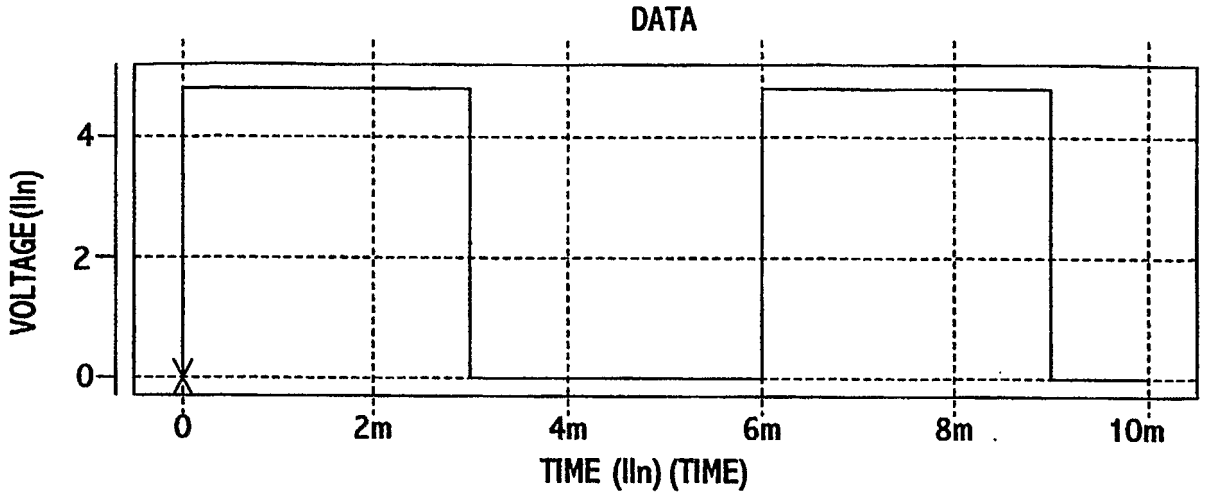


FIG. 8(A)

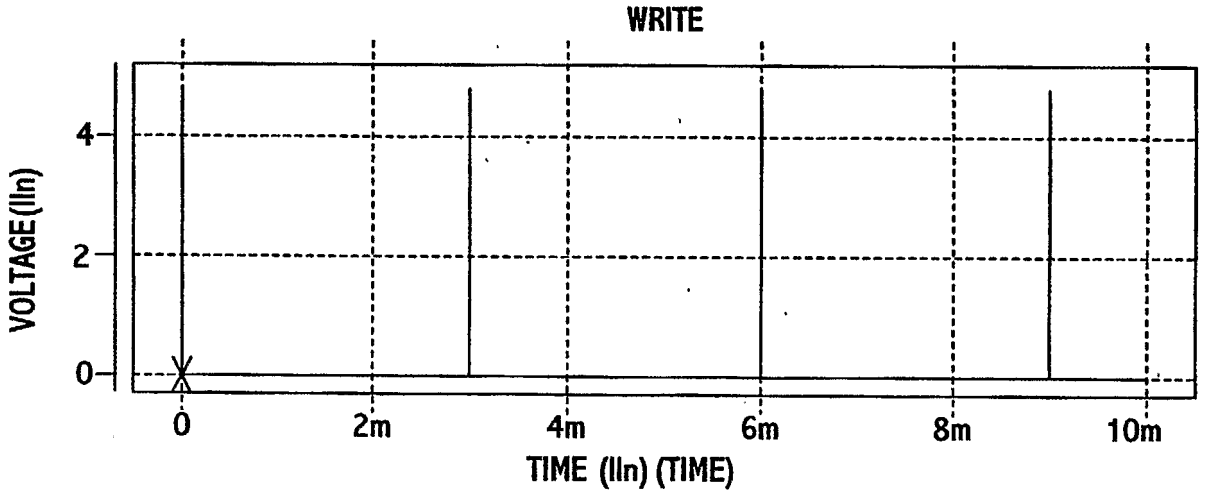


FIG. 8(B)

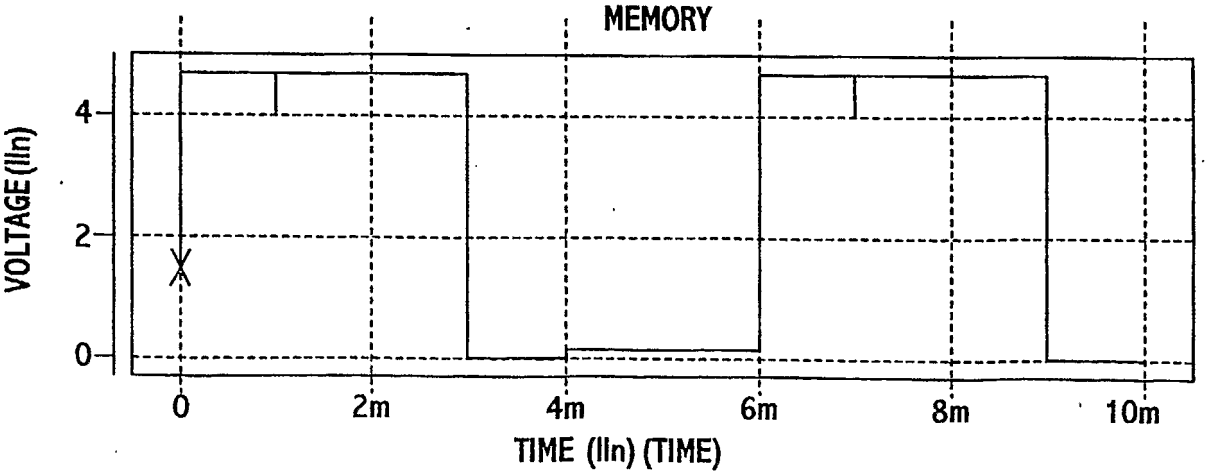


FIG. 8(C)

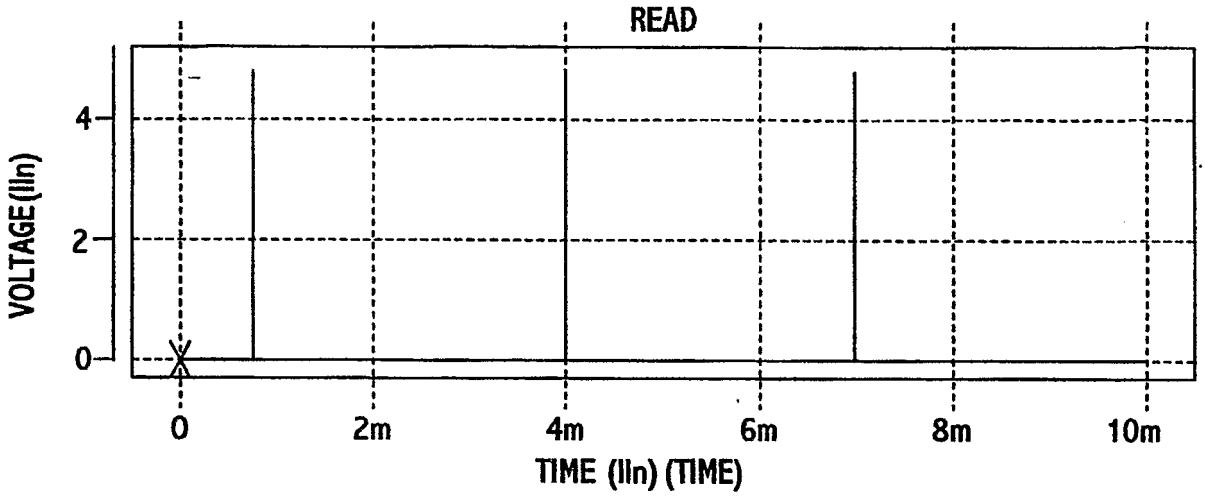

READ
VOLTAGE(lln)
4
2
0
0
2m
4m
6m
8m
10m
TIME (lln) (TIME)

FIG. 8(D)

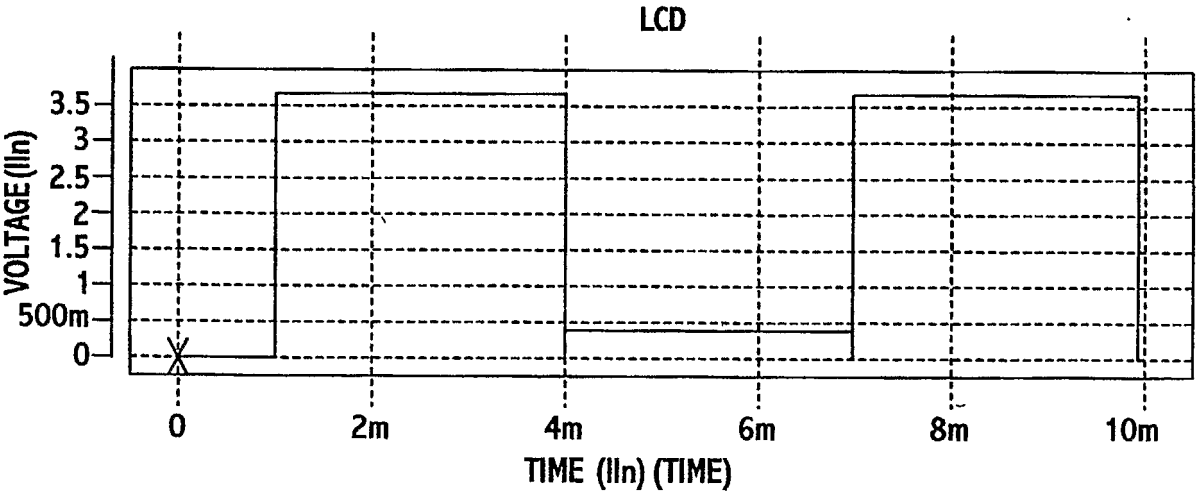
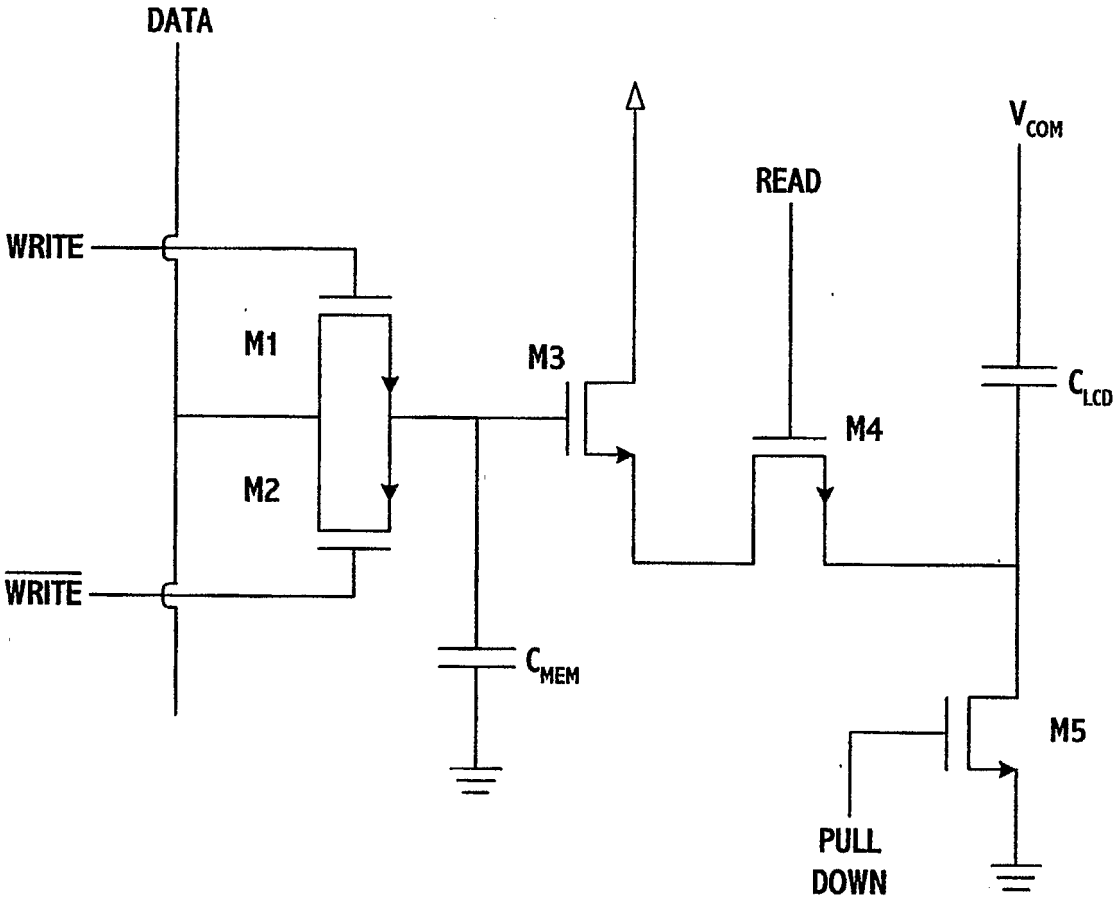

LCD
VOLTAGE(lln)
3.5
3
2.5
2
1.5
1
500m
0
0
2m
4m
6m
8m
10m
TIME (lln) (TIME)

FIG. 8(E)

VOLTAGE	0 V	0.8 V	2 V	3 V	4 V	5 V
PMOS	165.9	165.9	165.9	166	150.6	75.7
NMOS	76	137.3	167.6	167.5	167.4	167.4

GATE CAPACITANCE DEPENDING ON THE VOLTAGE APPLIED TO THE GATE (CAPACITANCE: ff)

FIG. 9



FRAME BUFFER PIXEL CIRCUIT IN CMOS

FIG. 10

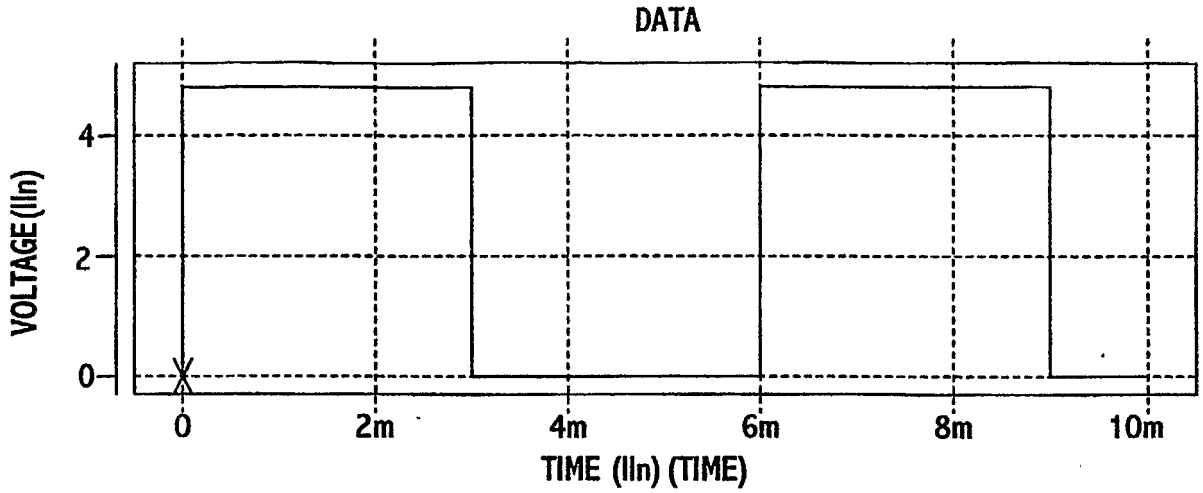


FIG. 11(A)

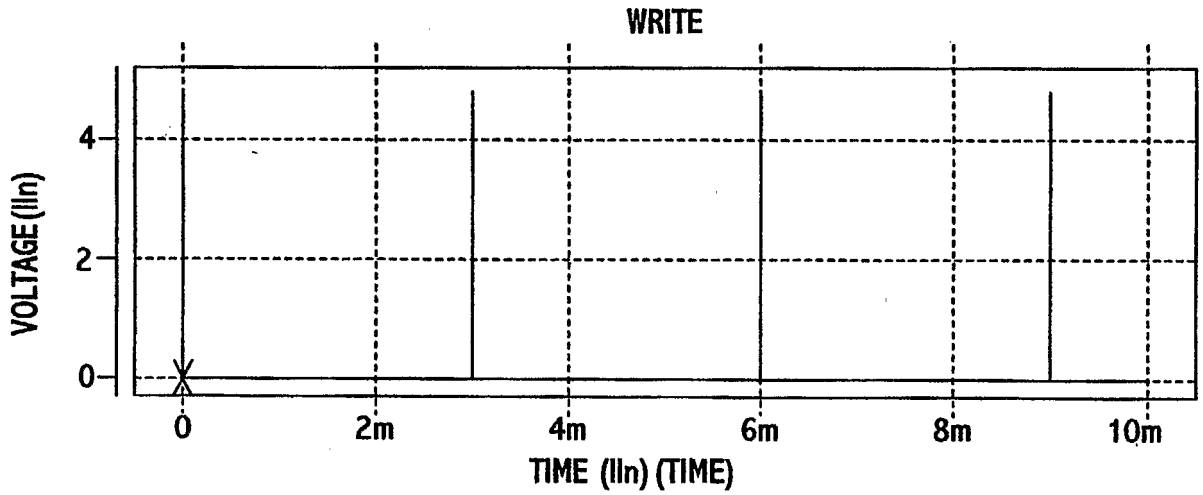


FIG. 11(B)

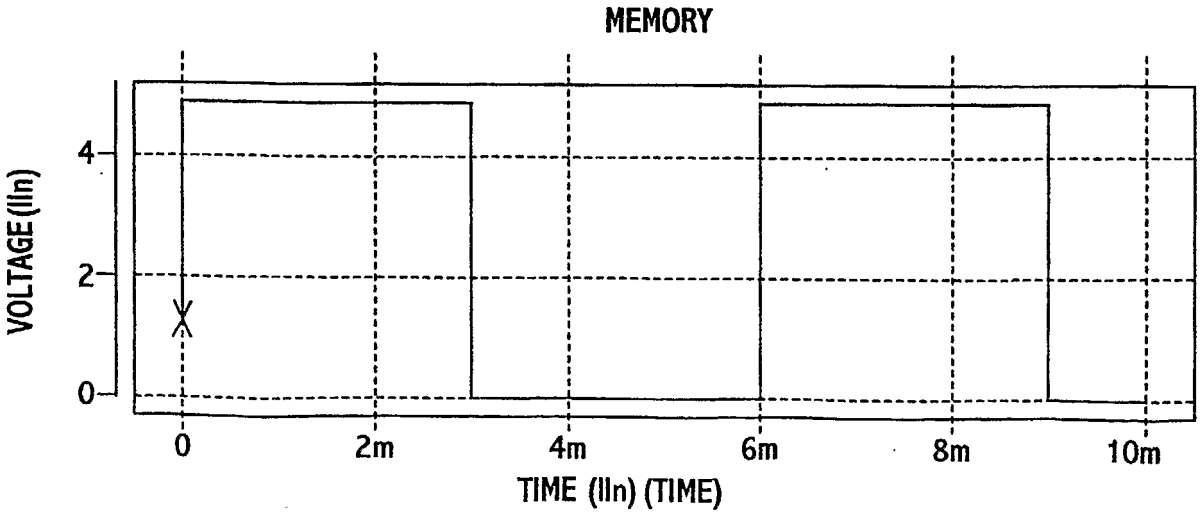


FIG. 11(C)

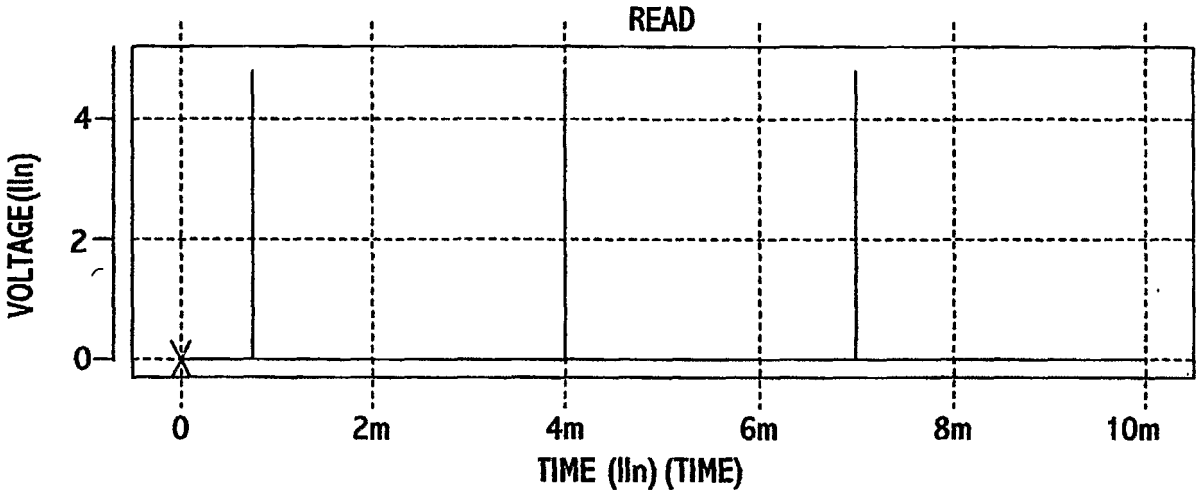


FIG. 11(D)

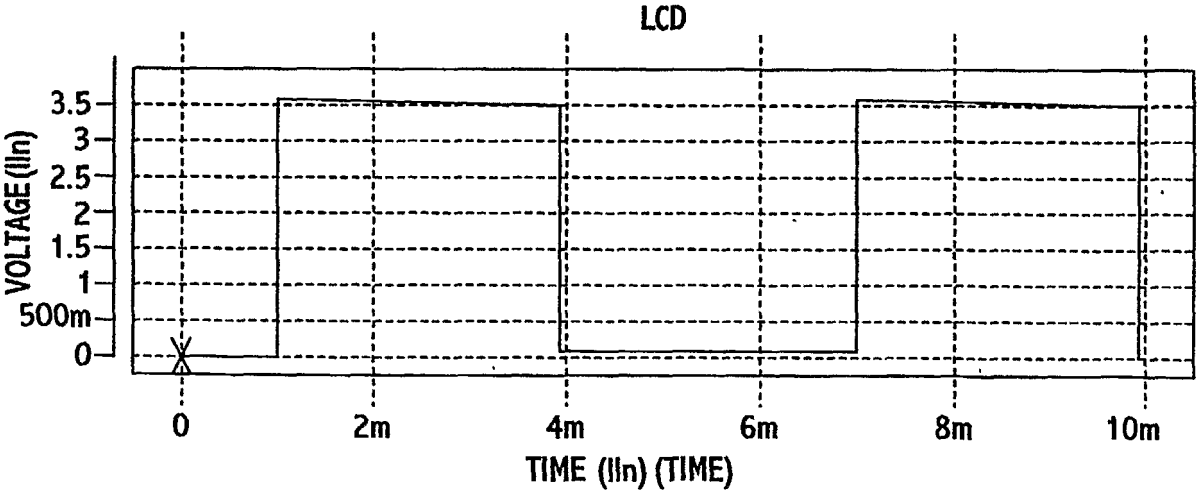


FIG. 11(E)

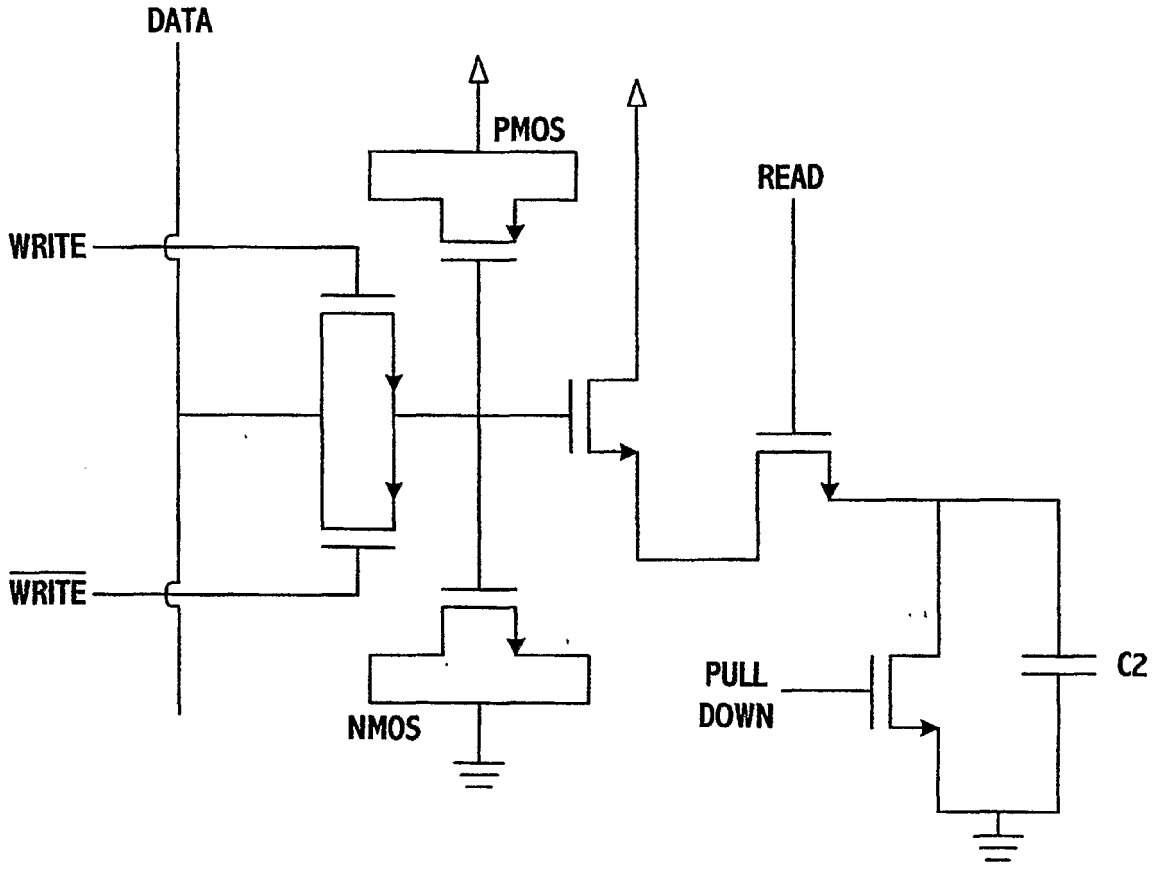
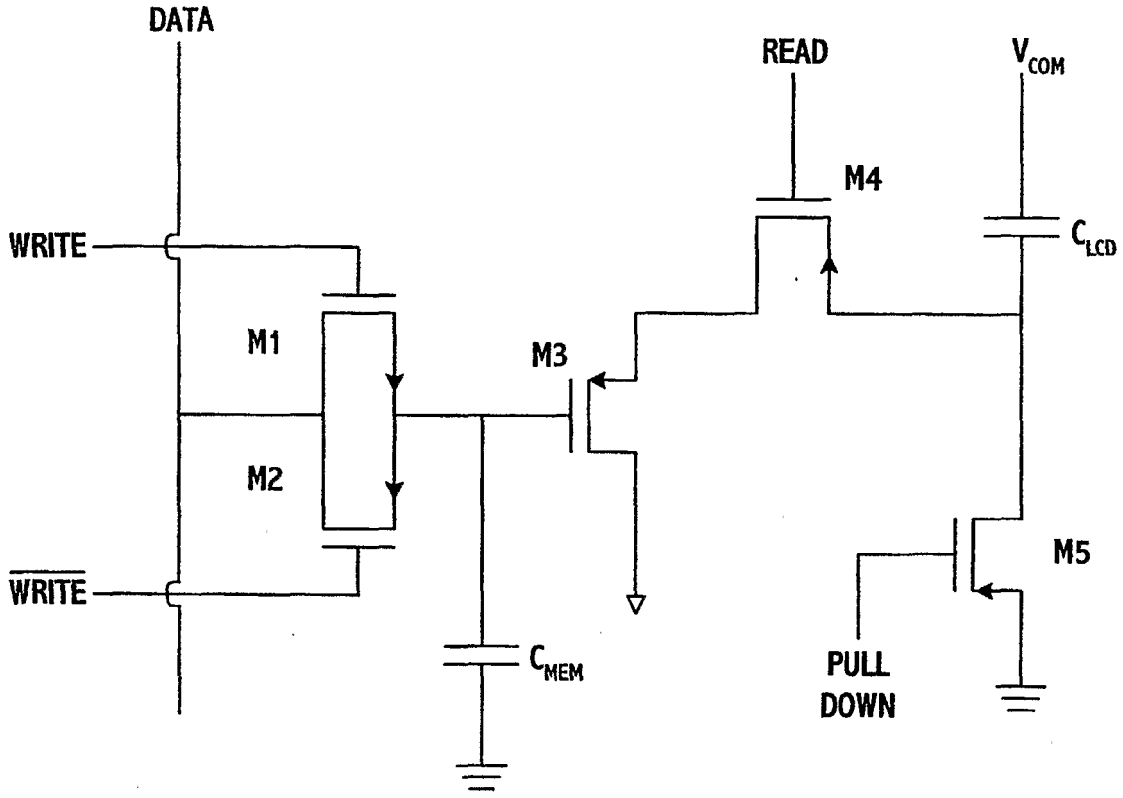
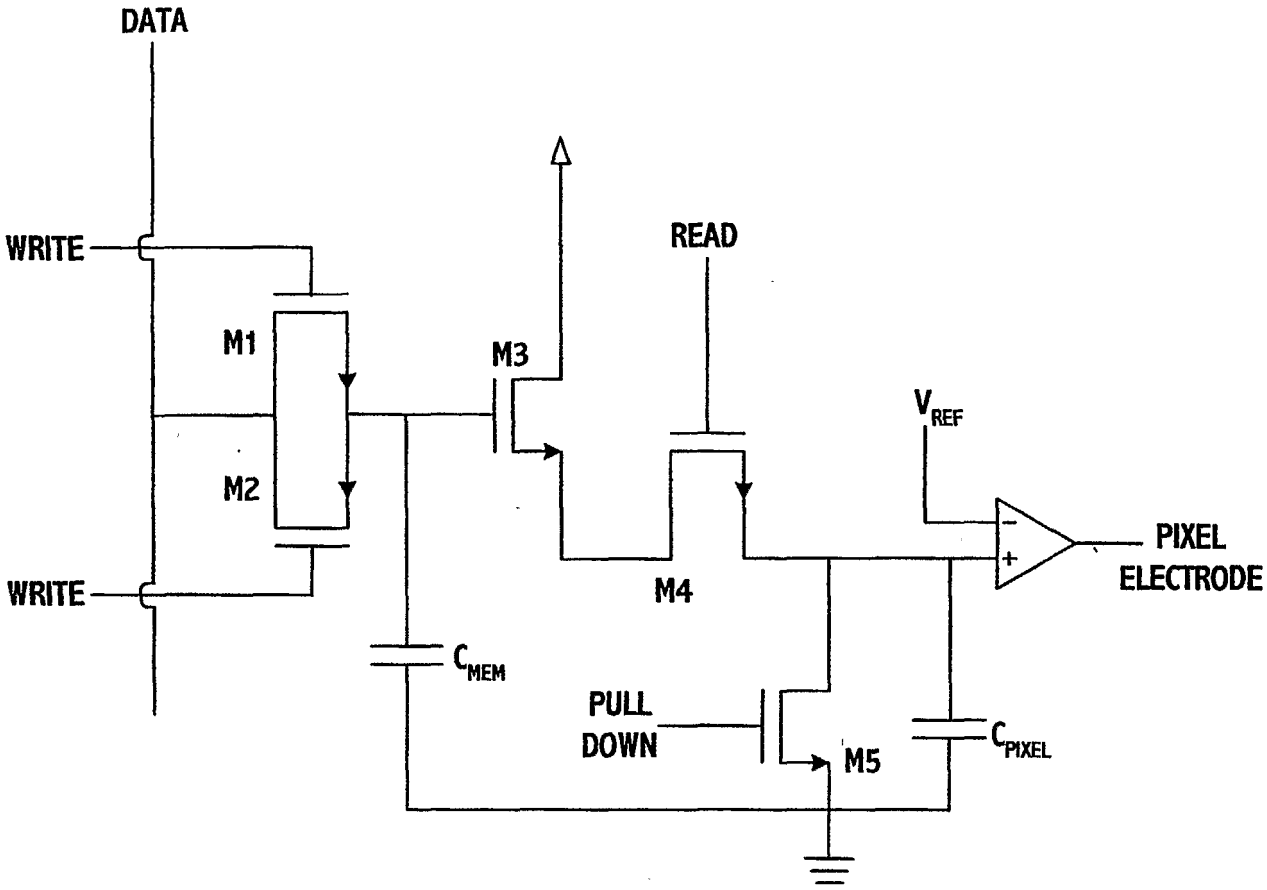


FIG. 12



FRAME BUFFER PIXEL CIRCUIT IN PMOS

FIG. 13



FRAME BUFFER PIXEL WITH A COMPARATOR

FIG. 14

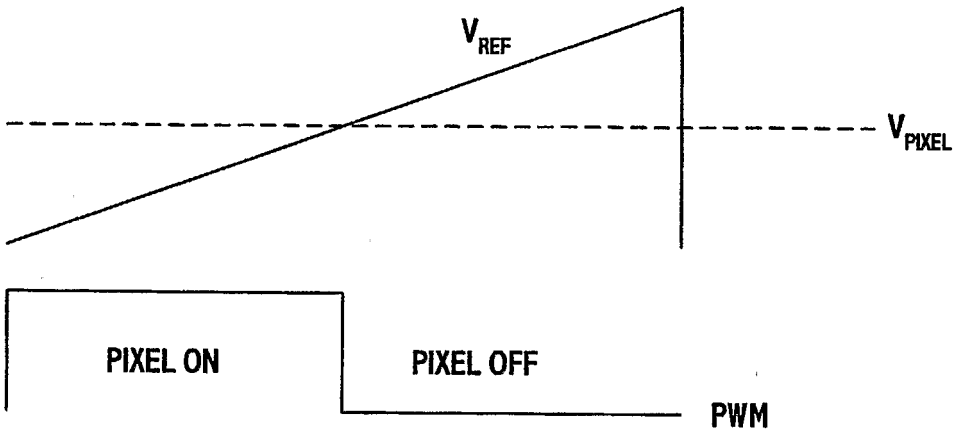
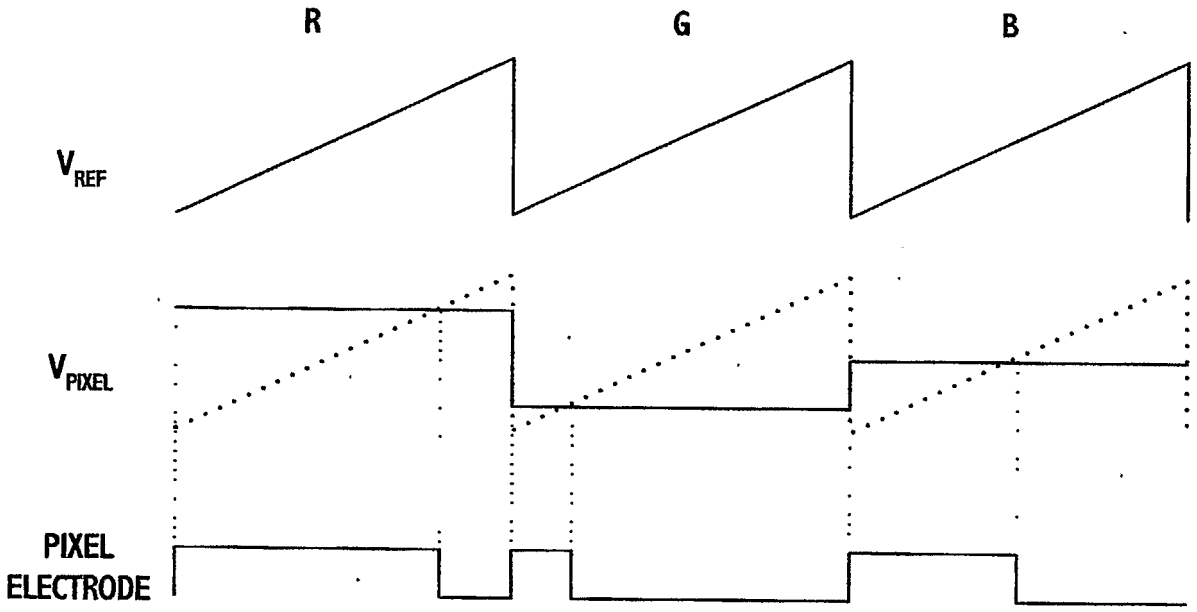
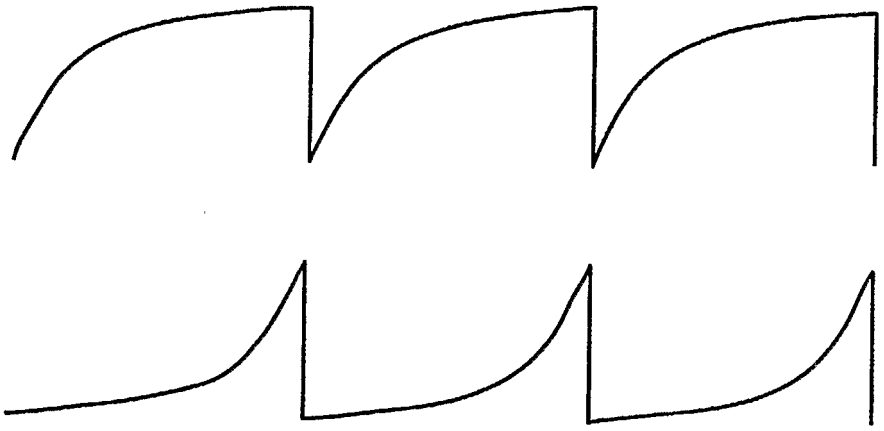


FIG. 15



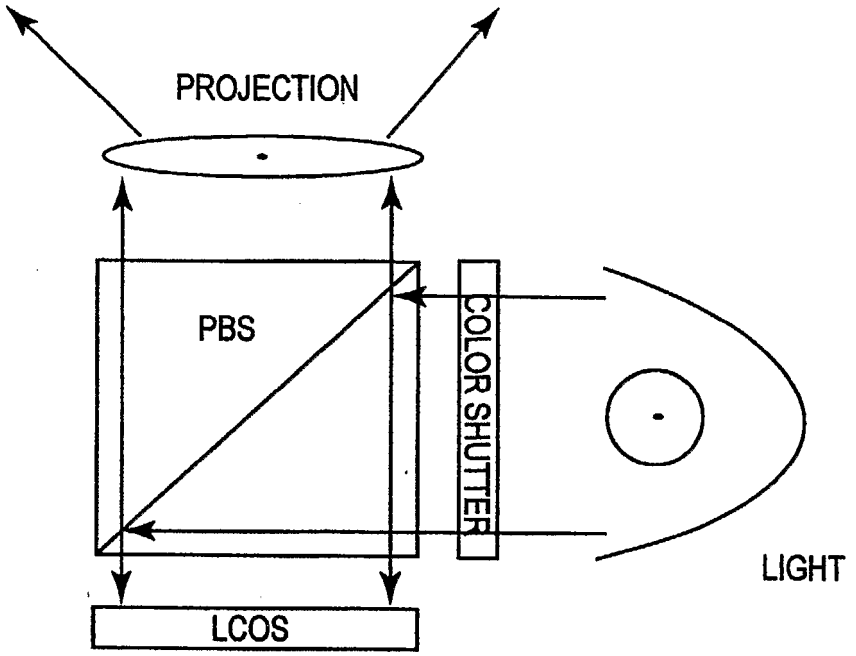
PWM WAVEFORM GENERATED FROM THE PIXEL VOLTAGE AND REFERENCE VOLTAGE.

FIG. 16



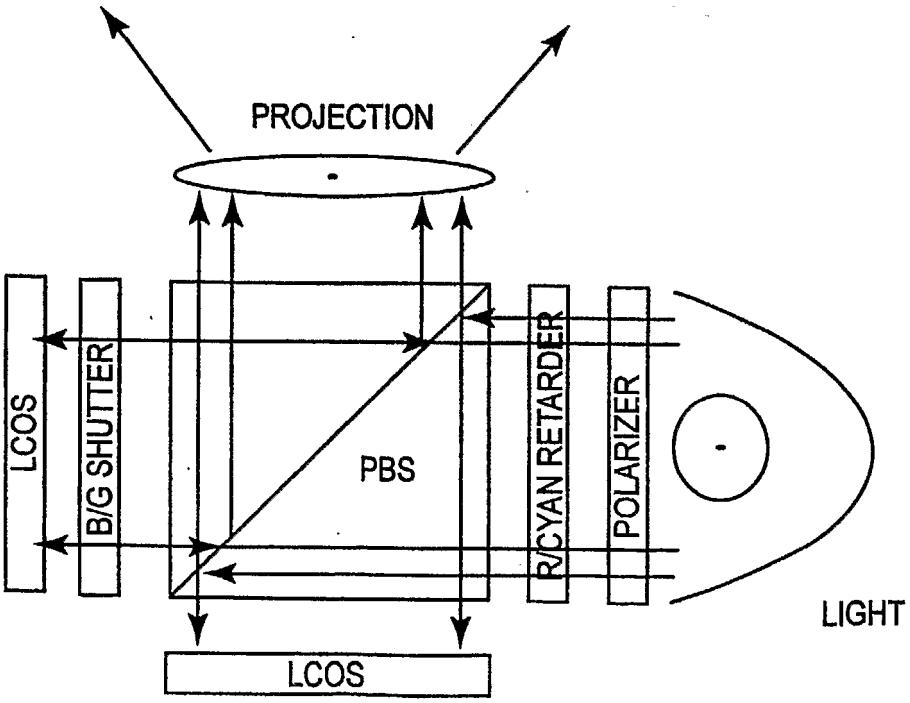
WAVEFORM OF THE REFERENCE VOLTAGE VARIED
TO APPLY GAMMA CORRECTIONS.

FIG. 17



1-PANEL PROJECTION DISPLAY WITH FIELD SEQUENTIAL COLOR.

FIG. 18



2-PANEL PROJECTION DISPLAY WITH FIELD SEQUENTIAL COLOR.

FIG. 19

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US03/11389

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : G09G 3/36

US CL : 345/90, 92, 98

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 345/90, 92, 98

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US 5,959,598 A (MCKNIGHT) 28 September 1999 (28.09.1999), column 16, lines 58-67, column 17, lines 1-17, column 19, lines 1-42, figures 7-10	1-2, 4-9 --- 3, 10-21
Y	US 6,440,811 B1 (COOLBAUGH et al) 27 August 2002 (27.08.2002), abstract, column 1, lines 6-60.	3, 13
Y, P	US 6,525,709 B1 (O'CALLAGHAN) 25 February 2003 (25.02.2003), column 5, lines 24-67, column 6, lines 13-40, figures 3.	10-12, 14-21

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 June 2003 (15.06.2003)	30 JUL 2003
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450 Facsimile No. (703)305-3230	Authorized officer Michael J. Moyer Telephone No. (703) 305-0899 Evgenia Zogan

Form PCT/ISA/210 (second sheet) (July 1998)

专利名称(译)	用于液晶显示器的帧缓冲像素电路		
公开(公告)号	EP1559091A1	公开(公告)日	2005-08-03
申请号	EP2003721652	申请日	2003-04-14
[标]申请(专利权)人(译)	杜克大学		
申请(专利权)人(译)	杜克大学		
当前申请(专利权)人(译)	杜克大学		
[标]发明人	LEE SANGROK MORIZIO JAMES C JOHNSON KRISTINA M		
发明人	LEE, SANGROK MORIZIO, JAMES C. JOHNSON, KRISTINA M.		
IPC分类号	G09G3/20 G09G3/36		
CPC分类号	G09G3/3648 G09G3/2014 G09G2300/0809 G09G2300/0842 G09G2300/0847 G09G2310/0251 G09G2310/0259 G09G2320/0223		
优先权	10/289459 2002-11-07 US		
其他公开文献	EP1559091A4		
外部链接	Espacenet		

摘要(译)

增强型帧缓冲器像素电路具有两个控制晶体管（图6）和一个单独的电容器作为存储器电容器，在存储器晶体管之前通过去除感应电荷产生高对比度并解决存储器电容器和存储器之间的电荷共享问题液晶显示器（LCD）电容器。存储晶体管可以由CMOS或PMOS制成。只有在像素电极电路之后放入比较器以表示具有降低的子帧频率的灰度级时，帧缓冲器像素才可用于驱动表示ON和OFF的二进制显示器。