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(54) **DISPLAY PANEL AND DRIVE METHOD THEREOF, AND LIQUID CRYSTAL DISPLAY DEVICE**

(57) The present invention provides a display panel and a driving method thereof, as well as a liquid crystal display device, which relates to the field of liquid crystal display technology, and can reduce the power consumption of the display panel. The display panel comprises a source driver, a plurality of pixel units defined by a plurality of gate lines and a plurality of data lines arranged crossly, and a common voltage output driver, the common voltage output driver is used for, at a Nth frame, inputting a negative common voltage to a first pixel unit, and at an adjacent frame of the Nth frame, inputting a positive common voltage to the first pixel unit, the first pixel unit is one of the plurality of pixel units, N is a positive integer; the source driver is used for, when the common voltage output driver inputs the negative common voltage to the first pixel unit, inputting a data voltage greater than or equal to the negative common voltage to the first pixel unit, and, when the common voltage output driver inputs the positive common voltage to the first pixel unit, inputting a data voltage less than or equal to the positive common voltage to the first pixel unit. The display panel can be applied in a liquid crystal display device.

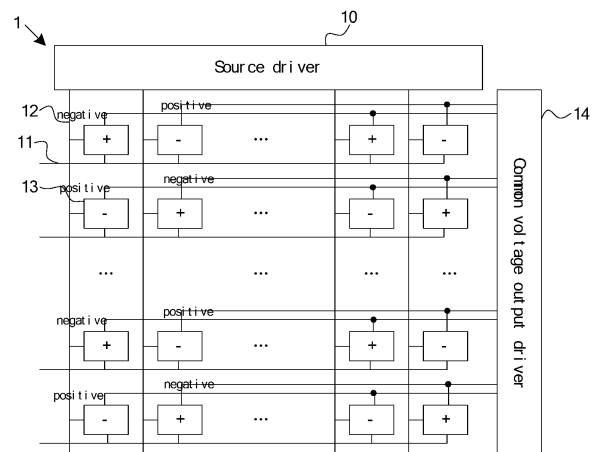


Fig. 2

Description

FIELD OF THE INVENTION

[0001] The present invention relates to the field of liquid crystal display technology, particularly to a display panel and a driving method thereof, as well as a liquid crystal display device.

BACKGROUND OF THE INVENTION

[0002] With the continuous development of the liquid crystal display technology, the liquid crystal display device has been more and more widely applied. During operation of the liquid crystal display device, the display is generally accomplished by rotation of the liquid crystal molecules driven by a voltage difference (i.e., a driving voltage) of the data voltage outputted by the source driver and the common voltage outputted by the common voltage output driver. In order to avoid the liquid crystal molecules from being driven by a certain fixed driving voltage for a long time, and the rotational characteristic of the liquid crystal molecules from being destroyed, the polarity (including positive polarity and negative polarity) of the driving voltage needs to be reversed generally, i.e., the polarity of the driving voltage varies alternately between the positive polarity and the negative polarity. As shown in Fig. 1, when the data voltage is higher than the common voltage, the polarity of the driving voltage is positive polarity, vice versa, the polarity of the driving voltage is negative polarity.

[0003] During operation of the liquid crystal display device, since the common voltage outputted by the common voltage output driver is generally a constant voltage, in order to ensure polarity of the driving voltage of the liquid crystal molecules to be reversed, the variation range of the data voltage has to be twice of the driving voltage, for example, if the driving voltage is V_0 , the variation range of the data voltage is $2V_0$.

[0004] In order to ensure the source driver to output the data voltage normally, the maximum working voltage of the source driver has to be $2V_0$, hence, the maximum working voltage of the display panel has to be $2V_0$, i.e., the maximum working voltage of the display panel is twice of the driving voltage of the liquid crystal molecules, such that the actual power consumption of the display panel would be twice of the theoretical power consumption.

SUMMARY OF THE INVENTION

[0005] The present invention provides a display panel and a driving method thereof, as well as a liquid crystal display device, which can reduce the power consumption of the display panel.

[0006] In order to achieve the above purpose, the present invention adopts the following technical solutions:

[0007] The present invention provides a display panel

comprising a source driver and a plurality of pixel units defined by a plurality of gate lines and a plurality of data lines arranged crossly, wherein the display panel further comprises a common voltage output driver,

the common voltage output driver is used for, at a Nth frame, inputting a negative common voltage to a first pixel unit, and at an adjacent frame of the Nth frame, inputting a positive common voltage to the first pixel unit, the first pixel unit is one of the plurality of pixel units, N is a positive integer;

the source driver is used for, when the common voltage output driver inputs the negative common voltage to the first pixel unit, inputting a data voltage greater than or equal to the negative common voltage to the first pixel unit, and, when the common voltage output driver inputs the positive common voltage to the first pixel unit, inputting a data voltage less than or equal to the positive common voltage to the first pixel unit.

[0008] Optionally, the common voltage output driver is further used for receiving a polarity control signal, a logic level of the polarity control signal at the Nth frame is contrary to a logic level of the polarity control signal at the adjacent frame of the Nth frame;

wherein, at the Nth frame, when the polarity control signal is of a high level, the common voltage output driver inputs the negative common voltage to the first pixel unit, and at the adjacent frame of the Nth frame, when the polarity control signal is of a low level, the common voltage output driver inputs the positive common voltage to the first pixel unit; or

at the Nth frame, when the polarity control signal is of a low level, the common voltage output driver inputs the negative common voltage to the first pixel unit, and at the adjacent frame of the Nth frame, when the polarity control signal is of a high level, the common voltage output driver inputs the positive common voltage to the first pixel unit.

[0009] Optionally, the polarity control signal comprises a first polarity control signal for controlling output of the common voltage output driver in pixel units of odd rows and pixel units of even rows, a logic level of the first polarity control signal in the pixel units of odd rows is contrary to a logic level of the first polarity control signal in the pixel units of even rows within the same frame, or, the polarity control signal comprises a second polarity control signal for controlling output of the common voltage output driver in pixel units of odd rows and a third polarity control signal for controlling output of the common voltage output driver in pixel units of even rows, a logic level of the second polarity control signal is contrary to a logic level of the third polarity control signal within the same frame, the logical levels of the second polarity control signal and the third polarity control signal are contrary within two adjacent frames;

the common voltage output driver comprises a plurality of groups of output terminals, each group of output terminals comprise an odd output terminal and an even output terminal respectively, wherein when the odd output terminal outputs a negative common voltage, the even

output terminal outputs a positive common voltage, or, when the odd output terminal outputs a positive common voltage, the even output terminal outputs a negative common voltage;

in the plurality of pixel units, pixel units of odd columns in each row of pixel units are connected with an odd output terminal in a corresponding group of output terminals of the common voltage output driver respectively, pixel units of even columns in each row of pixel units are connected with an even output terminal of the corresponding group of output terminals of the common voltage output driver respectively.

[0010] Optionally, the polarity control signal is used for controlling output of the common voltage output driver in pixel units of odd rows and pixel units of even rows, the logical level of the polarity control signal is contrary within two adjacent frames, the common voltage output driver comprises a plurality of groups of output terminals, each group of output terminals comprises an odd output terminal and an even output terminal respectively, wherein, when the odd output terminal outputs a negative common voltage, the even output terminal outputs a positive common voltage, or, when the odd output terminal outputs a positive common voltage, the even output terminal outputs a negative common voltage;

in the plurality of pixel units, pixel units of odd columns in one row of pixel units of any two adjacent rows of pixel units are connected with an odd output terminal in a corresponding group of output terminals of the common voltage output driver, the pixel units of even columns of the one row of pixel units are connected with an even output terminal in the group of output terminals of the common voltage output driver;

pixel units of odd columns of the other row of pixel units in any two adjacent rows of pixel units are connected with an even output terminal in the other group of output terminals of the common voltage output driver, pixel units of even columns of the other row of pixel units are connected with an odd output terminal in the other group of output terminals of the common voltage output driver.

[0011] Optionally, the display panel further comprises a timing controller,

the timing controller is used for generating the polarity control signal and outputting the polarity control signal to the common voltage output driver.

Optionally, the timing controller is further used for storing a common voltage adjustment parameter and outputting the common voltage adjustment parameter to the common voltage output driver;

the common voltage output driver is further used for adjusting common voltages of pixel units having display defects based on the common voltage adjustment parameter.

[0012] The present invention provides a liquid crystal display device comprising the display panel stated above.

[0013] The present invention provides a driving method of a display panel for driving the display panel stated

above, the driving method comprising:

at a Nth frame, a common voltage output driver inputting a negative common voltage to a first pixel unit, the first pixel unit being one of a plurality of pixel units defined by a plurality of gate lines and a plurality of data lines arranged crossly, N being a positive integer, when the common voltage output driver inputs the negative common voltage to the first pixel unit, the source driver inputting a data voltage greater than or equal to the negative common voltage to the first pixel unit;

at an adjacent frame of the Nth frame, the common voltage output driver inputting a positive common voltage to the first pixel unit, when the common voltage output driver inputs the positive common voltage to the first pixel unit, the source driver inputting a data voltage less than or equal to the positive common voltage to the first pixel unit.

[0014] Optionally, the driving method further comprises: the common voltage output driver receiving a polarity control signal, a logic level of the polarity control signal at the Nth frame being contrary to a logic level of the polarity control signal at an adjacent frame of the Nth frame;

wherein, at the Nth frame, the common voltage output driver inputting a negative common voltage to the first pixel unit comprises: at the Nth frame, when the polarity control signal is of a high level, the common voltage output driver inputting the negative common voltage to the first pixel unit,

at the adjacent frame of the Nth frame, the common voltage output driver inputting a positive common voltage to the first pixel unit comprises: at the adjacent frame of the Nth frame, when the polarity control signal is of a low level, the common voltage output driver inputs the positive common voltage to the first pixel unit; or,

wherein, at the Nth frame, the common voltage output driver inputting a negative common voltage to the first pixel unit comprises: at the Nth frame, when the polarity control signal is of a low level, the common voltage output driver inputting the negative common voltage to the first pixel unit,

at the adjacent frame of the Nth frame, the common voltage output driver inputting a positive common voltage to the first pixel unit comprises: at the adjacent frame of the Nth frame, when the polarity control signal is of a high level, the common voltage output driver inputting the positive common voltage to the first pixel unit.

[0015] Optionally, the polarity control signal comprises a first polarity control signal for controlling output of the common voltage output driver in pixel units of odd rows and pixel units of even rows, a logic level of the first polarity control signal in the pixel units of odd rows is contrary to a logic level of the first polarity control signal in the pixel units of even rows within the same frame, or, the polarity control signal comprises a second polarity

control signal for controlling output of the common voltage output driver in pixel units of odd rows and a third polarity control signal for controlling output of the common voltage output driver in pixel units of even rows, a logic level of the second polarity control signal is contrary to a logic level of the third polarity control signal within the same frame, the logical levels of the second polarity control signal and the third polarity control signal are contrary within two adjacent frames;

the common voltage output driver comprises a plurality of groups of output terminals, each group of output terminals comprise an odd output terminal and an even output terminal respectively, wherein when the odd output terminal outputs a negative common voltage, the even output terminal outputs a positive common voltage, or, when the odd output terminal outputs a positive common voltage, the even output terminal outputs a negative common voltage;

in the plurality of pixel units, pixel units of odd columns in each row of pixel units are connected with an odd output terminal in a corresponding group of output terminals of the common voltage output driver respectively, pixel units of even columns in each row of pixel units are connected with an even output terminal of the corresponding group of output terminals of the common voltage output driver respectively.

[0016] Optionally, the polarity control signal is used for controlling output of the common voltage output driver in pixel units of odd rows and pixel units of even rows, the logic level of the polarity control signal is contrary within two adjacent frames, the common voltage output driver comprises a plurality of groups of output terminals, each group of output terminals comprises an odd output terminal and an even output terminal respectively, wherein, when the odd output terminal outputs a negative common voltage, the even output terminal outputs a positive common voltage, or, when the odd output terminal outputs a positive common voltage, the even output terminal outputs a negative common voltage;

in the plurality of pixel units, pixel units of odd columns in one row of pixel units of any two adjacent rows of pixel units are connected with an odd output terminal in a corresponding group of output terminals of the common voltage output driver, the pixel units of even columns of the one row of pixel units are connected with an even output terminal in the group of output terminals of the common voltage output driver;

pixel units of odd columns of the other row of pixel units in any two adjacent rows of pixel units are connected with an even output terminal in the other group of output terminals of the common voltage output driver, pixel units of even columns of the other row of pixel units are connected with an odd output terminal in the other group of output terminals of the common voltage output driver.

[0017] Optionally, the display panel further comprises a timing controller, the driving method further comprises:

the timing controller generating the polarity control

signal and outputting the polarity control signal to the common voltage output driver.

[0018] Optionally, the driving method further comprises:

the timing controller storing a common voltage adjustment parameter and outputting the common voltage adjustment parameter to the common voltage output driver;

the common voltage output driver adjusting common voltages of pixel units having display defects based on the common voltage adjustment parameter.

[0019] The present invention provides a display panel and a driving method thereof, as well as a liquid crystal display device, the display panel comprises a source driver and a plurality of pixel units defined by a plurality of gate lines and a plurality of data lines arranged crossly, the display panel further comprises a common voltage output driver, the common voltage output driver is used for, at a Nth frame, inputting a negative common voltage to a first pixel unit, and at an adjacent frame of the Nth frame, inputting a positive common voltage to the first pixel unit, the first pixel unit is one of the plurality of pixel units, N is a positive integer; the source driver is used for, when the common voltage output driver inputs the negative common voltage to the first pixel unit, inputting a data voltage greater than or equal to the negative common voltage to the first pixel unit, and, when the common voltage output driver inputs the positive common voltage to the first pixel unit, inputting a data voltage less than or equal to the positive common voltage to the first pixel unit.

[0020] Based on the above technical solutions, since the common voltage output driver inputs alternately varying negative common voltages and positive common voltages to a same pixel unit within two adjacent frames respectively, and when the common voltage output driver inputs a negative common voltage to a certain pixel unit, the source driver inputs a data voltage greater than or equal to the negative voltage to this pixel unit, and when the common voltage output driver inputs a positive common voltage to a certain pixel unit, the source driver inputs a data voltage less than or equal to the positive common voltage to this pixel unit, such that: on the one hand, within two adjacent frames, the polarity of the driving voltage (which is the difference value of the data voltage and the common voltage) of the same pixel unit is reversed; on the other hand, compared with the prior art, since the common voltage is a voltage varying between positive and negative, in the event that the driving voltage of the liquid crystal molecules is invariable, the variation range of the data voltage outputted by the source driver is reduced, i.e., the maximum working voltages of the source driver and the display panel are both reduced also, thereby reducing the power consumption of the display panel.

BRIEF DESCRIPTION OF THE DRAWINGS

[0021]

Fig. 1 is a schematic view of polarity of a driving voltage and variation range of a data voltage provided by the prior art;

Fig. 2 is a structural schematic view I of a display panel provided by an embodiment of the present invention;

Fig. 3 is a schematic view of polarity of a driving voltage and variation range of a data voltage provided by an embodiment of the present invention;

Fig. 4 is a structural schematic view II of a display panel provided by an embodiment of the present invention;

Fig. 5 is a timing diagram I of pixel units of a display panel provided by an embodiment of the present invention;

Fig. 6 is a schematic view of point reversion provided by an embodiment of the present invention;

Fig. 7 is a circuit schematic view of a common voltage output driver provided by an embodiment of the present invention;

Fig. 8 is a structural schematic view III of a display panel provided by an embodiment of the present invention;

Fig. 9 is a timing diagram II of pixel units of a display panel provided by an embodiment of the present invention;

Fig. 10 is a structural schematic view IV of a display panel provided by an embodiment of the present invention;

Fig. 11 is a flow chart of a driving method of a display panel provided by an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0022] Next, the display panel and the driving method thereof, as well as the liquid crystal display device provided by the embodiments of the present invention will be described in detail with reference to the drawings.

[0023] As shown in Fig. 2, an embodiment of the present invention provides a display panel 1, the display panel 1 comprises a source driver 10 and a plurality of pixel units 13 defined by a plurality of gate lines 11 and a plurality of data lines 12 arranged crossly, the display panel 1 further comprises a common voltage output driver 14.

[0024] The common voltage output driver 14 is used for, at a Nth frame, inputting a negative common voltage to a first pixel unit, and at an adjacent frame of the Nth frame, inputting a positive common voltage to the first pixel unit, the first pixel unit is one of the plurality of pixel units 13, N is a positive integer.

[0025] The source driver 10 is used for, when the common voltage output driver 14 inputs the negative common

voltage to the first pixel unit, inputting a data voltage greater than or equal to the negative common voltage to the first pixel unit, and, when the common voltage output driver 14 inputs the positive common voltage to the first pixel unit, inputting a data voltage less than or equal to the positive common voltage to the first pixel unit.

[0026] In an embodiment of the present invention, the common voltage outputted by the common voltage output driver 14 comprises a negative common voltage and a positive common voltage. Wherein, as shown in Fig. 3, take 0V as the reference voltage, the common voltage along the direction A is a positive common voltage, the common voltage along the direction B is a negative common voltage.

[0027] Further, when the common voltage output driver 14 inputs the negative common voltage to the first pixel unit, the source driver 10 inputs a data voltage greater than or equal to the negative common voltage to the first pixel unit, so as to ensure that the polarity of the driving voltage of the first pixel unit is positive polarity; when the common voltage output driver 14 inputs the positive common voltage to the first pixel unit, the source driver 10 inputs a data voltage less than or equal to the positive common voltage to the first pixel unit, so as to ensure that the polarity of the driving voltage of the first pixel unit is negative polarity.

[0028] Exemplarily, if the common voltage of this pixel unit is -V, the data voltage inputted by the source driver 10 to this pixel unit will be greater than or equal to -V, and the polarity of the driving voltage of this pixel unit will be positive polarity; if the common voltage of this pixel unit is V, the data voltage inputted by the source driver 10 to this pixel unit will be less than or equal to V, and the polarity of the driving voltage of this pixel unit will be negative polarity, wherein V can be a positive integer.

[0029] It needs to be explained that the size of the common voltage inputted by the common voltage output driver to the pixel unit can be set based on actual use requirements, which will not be defined specifically in the present invention.

[0030] In an embodiment of the present invention, since the common voltage output driver inputs alternately varying negative common voltages and positive common voltages to a same pixel unit within two adjacent frames respectively, and when the common voltage output driver inputs a negative common voltage to a certain pixel unit, the source driver inputs a data voltage greater than or equal to the negative voltage to this pixel unit, and when the common voltage output driver inputs a positive common voltage to a certain pixel unit, the source driver inputs a data voltage less than or equal to the positive common voltage to this pixel unit, such that: on the one hand, within two adjacent frames, the polarity of the driving voltage (which is the difference value of the data voltage and the common voltage) of the same pixel unit is reversed; on the other hand, compared with the prior art, since the common voltage is a voltage varying between positive and negative, in the event that the driving voltage

of the liquid crystal molecules is invariable, the variation range of the data voltage outputted by the source driver is reduced, i.e., the maximum working voltages of the source driver and the display panel are both reduced also, thereby reducing the power consumption of the display panel.

[0031] Optionally, the common voltage output driver 14 is further used for receiving a polarity control signal, a logic level of the polarity control signal at the Nth frame is contrary to a logic level of the polarity control signal at the adjacent frame of the Nth frame.

[0032] For example, the common voltage output driver 14 is used for, at the Nth frame, when the polarity control signal is of a high level, inputting the negative common voltage to the first pixel unit, and at the adjacent frame of the Nth frame, when the polarity control signal is of a low level, inputting the positive common voltage to the first pixel unit; or

the common voltage output driver 14, at the Nth frame, when the polarity control signal is of a low level, inputs the negative common voltage to the first pixel unit, and at the adjacent frame of the Nth frame, when the polarity control signal is of a high level, inputs the positive common voltage to the first pixel unit.

[0033] Wherein a logic level of the polarity control signal at the Nth frame being contrary to a logic level of the polarity control signal at the adjacent frame of the Nth frame can be understood as: if the logic level of the polarity control signal is a high level at the Nth frame, the logic level of the polarity control signal will be a low level at the adjacent frame of the Nth frame; on the contrary, if the logic level of the polarity control signal is a low level at the Nth frame, the logic level of the polarity control signal will be a high level at the adjacent frame of the Nth frame.

[0034] In an embodiment of the present invention, by changing the polarity of the driving voltage of each pixel unit within two adjacent frames (i.e., the polarity of the driving voltage of each pixel unit within two adjacent frames is not the same), i.e., realizing polarity reversion of the driving voltage, it can be ensured that the rotational characteristics of the liquid crystal molecules are not destroyed.

[0035] The display panel provided by an embodiment of the present invention can be applied in driving manners such as row reversion, column reversion and point reversion based on frame reversion (the reversions in this embodiment are all polarity reversion of the driving voltage of the pixel unit), which will not be defined specifically in the present invention.

[0036] The skilled person in the art can understand that compared with the driving manners of row reversion and column reversion, the driving manner of point reversion can increase the stabilized speed of the pixel unit voltage, and reduce cross talk between the pixels, hence, it can improve the display quality of the display panel so as to enable the display panel to have a high quality display effect.

[0037] Specifically, the structure of the display panel provided by an embodiment of the present invention will be explained in detail in the following through two possible implementing modes provided by an embodiment of the present invention respectively by taking the driving manner of point reversion as the example.

[0038] Optionally, in a possible implementing mode, the polarity control signal comprises a first polarity control signal for controlling output of the common voltage output driver 14 in pixel units of odd rows and pixel units of even rows, a logic level of the first polarity control signal in the pixel units of odd rows is contrary to a logic level of the first polarity control signal in the pixel units of even rows within the same frame.

[0039] Or, the polarity control signal comprises a second polarity control signal for controlling output of the common voltage output driver 14 in pixel units of odd rows and a third polarity control signal for controlling output of the common voltage output driver 14 in pixel units of even rows, a logic level of the second polarity control signal is contrary to a logic level of the third polarity control signal within the same frame, the logical levels of the second polarity control signal and the third polarity control signal are contrary within two adjacent frames.

[0040] The common voltage output driver 14 comprises a plurality of groups of output terminals, each group of output terminals comprise an odd output terminal and an even output terminal respectively, wherein when the odd output terminal outputs a negative common voltage, the even output terminal outputs a positive common voltage, or, when the odd output terminal outputs a positive common voltage, the even output terminal outputs a negative common voltage.

[0041] In the plurality of pixel units 13, pixel units of odd columns in each row of pixel units are connected with an odd output terminal in a corresponding group of output terminals of the common voltage output driver 14 respectively, pixel units of even columns in each row of pixel units are connected with an even output terminal of the corresponding group of output terminals of the common voltage output driver 14 respectively.

[0042] Specifically, as shown in Fig. 4, take the example that the polarity control signal 15 comprises a first polarity control signal 150, the first polarity control signal 150 controls output of the common voltage output driver 14. Each output terminal of the source driver 10 is connected with one column of pixel units, and inputs a data voltage to each column of pixel units under the control effect of a source polarity control signal 18; each group of output terminals of the common voltage output driver 14 is connected with one row of pixel units, wherein the odd output terminal in each group of output terminals of the common voltage output driver 14 is connected with pixel units of odd columns in one row of pixel units, the even output terminal in each group of output terminals of the common voltage output driver 14 is connected with pixel units of even columns in this row of pixel units. Each output terminal of a gate driver 16 is connected with one

row of pixel units, for controlling ON and OFF of each row of pixel units.

[0043] Wherein the method of the source driver 10, under the control effect of the source polarity control signal 18, to input a data voltage to each column of pixel units is similar as the method of the source driver 10 in the prior art to input a data voltage to each column of pixel units, i.e., the source driver, under the control effect of the source polarity control signal 18, inputs a corresponding data voltage to a corresponding pixel unit based on the output of the common voltage output driver 14, so as to ensure that the polarity of the driving voltage of this pixel unit realizes corresponding reversion. For example, in the driving manner of row reversion, the polarities of any two adjacent rows of pixel units are contrary; in the driving manner of point reversion, the polarities of any two adjacent pixel units are contrary.

[0044] Further, in Fig. 4, each pixel unit has a thin film transistor (TFT), an equivalent capacitance C_{lc} of the pixel unit, a pixel electrode and a common electrode line, a storage capacitance C_{st} is formed between the pixel electrode and the common electrode line. Wherein, one end of C_{lc} is connected with the drain of the TFT and the pixel electrode, the other end of C_{lc} is connected with an odd output terminal or an even output terminal (i.e., the common electrode line) of the common voltage output driver 14, the gate of the TFT is connected with one output terminal of the gate driver 15, the source of the TFT is connected with one output terminal of the source driver 10.

[0045] Exemplarily, as shown in Fig. 5, this figure is a working timing diagram of a pixel unit in the circuit as shown in Fig. 4. It can be seen from combination of Fig. 4 and Fig. 5 that at the moment T1 within the Nth frame, the gate driver 16 (the gate line scan signal of the gate driver is represented as G_{n-1}) opens the n-1th row of pixel units, the first polarity control signal 150 (represented as POL) is of a high level, the odd output terminal (represented as $V_{n-1,o}$) in the n-1th group of output terminals of the common voltage output driver 14 outputs a negative common voltage, the even output terminal (represented as $V_{n-1,e}$) in the n-1th group of output terminals of the common voltage output driver 14 outputs a positive common voltage. A plurality of output terminals of the source driver are under control of the source polarity control signal 18, when the $V_{n-1,o}$ outputs a negative common voltage, the corresponding output terminal in the plurality of output terminals of the source driver outputs a data voltage greater than or equal to the negative common voltage; when the $V_{n-1,e}$ outputs a positive common voltage, the corresponding output terminal in the plurality of output terminals of the source driver outputs a data voltage less than or equal to the positive common voltage, thereby enabling the polarity of the driving voltage of the n-1th row of pixel units to be "+" (representing positive polarity), "-" (representing negative polarity), "+, -" from left to right successively (for example, the output of the source driver in pixel units of odd col-

umns in the n-1th row of pixel units is represented as $S_{n-1,o}$, the polarity of the driving voltage in pixel units of odd columns in the n-1th row of pixel units is positive polarity; the output of the source driver in pixel units of the even columns in the n-1th row of pixel units is represented as $S_{n-1,e}$, the polarity of the driving voltage in pixel units of even columns in the n-1th row of pixel units is negative polarity).

[0046] At the moment T2 within the Nth frame, the gate driver 16 (the gate line scan signal of the gate driver is represented as G_n) opens the nth row of pixel units, the first polarity control signal 150 (represented as POL) becomes a low level, the odd output terminal (represented as $V_{n,o}$) in the nth group of output terminals of the common voltage output driver 14 outputs a positive common voltage, the even output terminal (represented as $V_{n,e}$) in the nth group of output terminals of the common voltage output driver 14 outputs a negative common voltage. A plurality of output terminals of the source driver are under control of the source polarity control signal 18, when the $V_{n,o}$ outputs a positive common voltage, the corresponding output terminal in the plurality of output terminals of the source driver outputs a data voltage less than or equal to the positive common voltage; when the $V_{n,e}$ outputs a negative common voltage, the corresponding output terminal in the plurality of output terminals of the source driver outputs a data voltage greater than or equal to the negative common voltage, thereby enabling the polarity of the driving voltage of the nth row of pixel units to be "-", "+, -, +" from left to right successively (for example, the output of the source driver in pixel units of odd columns of the nth row of pixel units is represented as $S_{n,o}$, the polarity of the driving voltage in pixel units of odd columns in the nth row of pixel units is negative polarity; the output of the source driver in pixel units of even columns in the nth row of pixel units is represented as $S_{n,e}$, the polarity of the driving voltage in pixel units of even columns in the nth row of pixel units is positive polarity).

[0047] The above description on the circuit as shown in Fig. 4 is only exemplary description made by taking one frame (e.g., the Nth frame) as the example, at the adjacent frame of this frame, the polarities of the common voltage outputted by each output terminal of the common voltage output driver, the data voltage outputted by the source driver and the driving voltage of each pixel unit are all contrary to those in this frame. Since the implementing principle of the adjacent frame of this frame is same as the implementing principle of this frame, it will not be repeated here.

[0048] It can be seen that in the circuit as shown in Fig. 4, the output of the source driver 10 is controlled through the source polarity control signal 18, and the output of the common voltage output driver 14 is controlled through the first polarity control signal 150, such that the polarity of the driving voltage of any two adjacent pixel units can be reversed, for example, as shown in Fig. 6, thus it can be ensured that the display panel has a high quality display effect; in addition, compared with the prior art, since

the common voltage is a voltage varying between positive and negative, in the event that the driving voltage of the liquid crystal molecules is invariable, the variation range of the data voltage outputted by the source driver is reduced, i.e., the maximum working voltages of the source driver and the display panel are both reduced also, thereby reducing the power consumption of the display panel.

[0049] Through the above solution, the display panel provided by an embodiment of the present invention can reduce the power consumption of the display panel while ensuring a high quality display effect.

[0050] In order to explain further that the technical solution provided by an embodiment of the present invention, relative to the prior art, can reduce the variation range of the data voltage outputted by the source driver, i.e., enabling the maximum working voltage of the source driver and the maximum working voltage of the display panel to be both reduced, exemplary explanations will be made with reference to Fig. 1 and Fig. 3 respectively in the following. Wherein Fig. 1 is a relationship diagram of the data voltage and the common voltage provided by the prior art, i.e., a schematic view of variation range of the data voltage provided by the prior art; Fig. 3 is a relationship diagram of the data voltage and the common voltage provided by an embodiment of the present invention, i.e., a schematic view of variation range of the data voltage provided by an embodiment of the present invention.

[0051] As shown in Fig. 1, assume that the voltage value of the driving voltage required by the pixel unit is 5V, the common voltage is 0V, it can be seen that since the common voltage is a constant voltage, in order to ensure the polarity of the driving voltage of the pixel unit to be reversed, the voltage variation range of the data voltage V_0 outputted by the source driver is 5V to -5V. In order to ensure the source driver to output the data voltage normally, the working voltage of the source driver needs to be $5V - (-5V) = 10V$, hence, the working voltage of the display panel also needs to be 10V. In addition, because the voltage value of the driving voltage required by the pixel unit is 5V, the theoretical working voltage of the display panel is also 5V, thus the actual working power consumption of the display panel is twice of the theoretical power consumption, which results in great waste of energy sources.

[0052] As shown in Fig. 3, assume that the voltage value of the driving voltage required by the pixel unit is 5V, the common voltage is -8V to 8V, it can be seen that since the common voltage is a voltage varying between positive and negative, in order to ensure the polarity of the driving voltage of the pixel unit to be reversed, the voltage variation range of the data voltage outputted by the source driver is -3V to 3V. In order to ensure the source driver to output the data voltage normally, the working voltage of the source driver can be $3V - (-3V) = 6V$, hence, the working voltage of the display panel is also 6V. Compared with the prior art, the actual working

power consumption of the display panel provided by an embodiment of the present invention is greatly reduced, thereby saving the energy sources.

[0053] It needs to be explained that the principle of the second polarity control signal and the third polarity control signal for controlling the common voltage output driver to output the common voltage is same as the principle of the first polarity control signal for controlling the common voltage output driver to output the common voltage, reference can be made to the principle of the above first polarity control signal for controlling the common voltage output driver to output the common voltage specifically, which will not be repeated here.

[0054] Further, the difference between the process of the second polarity control signal and the third polarity control signal for controlling the common voltage output driver to output the common voltage and the process of the first polarity control signal for controlling the common voltage output driver to output the common voltage lies in: the second polarity control signal controls output of the common voltage output driver in pixel units of odd rows, the third polarity control signal controls output of the common voltage output driver in pixel units of even rows, moreover, the logic level of the second polarity control signal is contrary to the logic level of the third polarity control signal within the same frame, and the logic levels of the second polarity control signal and the third polarity control signal are contrary within each of two adjacent frames; whereas the first polarity control signal controls output of the common voltage output driver in pixel units of odd rows and pixel units of even rows, and the logic level of the first polarity control signal in pixel units of odd rows is contrary to the logic level of the first polarity control signal in pixel units of even rows within the same frame.

[0055] Optionally, in an embodiment of the present invention, the circuit as shown in Fig. 7 can be used for the first polarity control signal (or the second polarity control signal and the third polarity control signal) to control the odd output terminal and the even output terminal in each group of output terminals in the common voltage output driver to output different common voltages.

[0056] As shown in Fig. 7, when the first polarity control signal (represented as POL) is of a high level, point B and point D are turned on, when the point B is turned on, the even output terminal outputs a positive voltage V_{in+} ; when the point D is turned on, the odd output terminal outputs a negative voltage V_{in-} . When the first polarity control signal is of a low level, point A and point C are turned on, when the point A is turned on, the odd output terminal outputs a positive voltage V_{in+} ; when the point C is turned on, the even output terminal outputs a negative voltage V_{in-} .

[0057] It needs to be explained that in Fig. 7, the control of the first polarity control signal to the odd output terminal and the even output terminal of the common voltage output driver can be realized through a NOT gate exemplarily, certainly, such a control effect of the first polarity control signal can also be realized through other circuit,

which will not be defined in the present invention specifically. Any circuit that can realize such a control effect of the first polarity control signal to the odd output terminal and the even output terminal of the common voltage output driver should fall within the protection scope of the present invention.

[0058] The above descriptions on that the common voltage inputted by the common voltage output driver to each pixel unit in the circuit as shown in Fig. 4 is a positive common voltage or a negative common voltage are all exemplary explanations made on the basis of the circuit as shown in Fig. 7, if the control effect of the first polarity control signal in Fig. 7 is realized by other circuits, the common voltage inputted by the common voltage output driver to each pixel unit in the circuit as shown in Fig. 4 will also vary accordingly, which will not be defined specifically in the present invention.

[0059] Optionally, in another possible implementing mode, the polarity control signal is used for controlling output of the common voltage output driver 14 in pixel unit of odd rows and pixel unit of even rows, the logic level of the polarity control signal is contrary within two adjacent frames, the common voltage output driver 14 comprises a plurality of groups of output terminals, each group of output terminals comprises an odd output terminal and an even output terminal respectively, wherein, when the odd output terminal outputs a negative common voltage, the even output terminal outputs a positive common voltage, or, when the odd output terminal outputs a positive common voltage, the even output terminal outputs a negative common voltage.

[0060] In the plurality of pixel units 13, pixel units of odd columns in one row of pixel units of any two adjacent rows of pixel units are connected with an odd output terminal in a corresponding group of output terminals of the common voltage output driver 14, the pixel units of even columns of the one row of pixel units are connected with an even output terminal in the group of output terminals of the common voltage output driver 14.

[0061] Pixel units of odd columns of the other row of pixel units in any two adjacent rows of pixel units are connected with an even output terminal in the other group of output terminals of the common voltage output driver 14, pixel units of even columns of the other row of pixel units are connected with an odd output terminal in the other group of output terminals of the common voltage output driver 14.

[0062] Wherein the logic level of the polarity control signal being contrary within two adjacent frames can be understood as: if the logic level of the polarity control signal is a high level at a certain frame, the logic level of the polarity control signal will be a low level at the adjacent frame of the frame; on the contrary, if the logic level of the polarity control signal is a low level at a certain frame, the logic level of the polarity control signal will be a high level at the adjacent frame of the frame.

[0063] Specifically, as shown in Fig. 8, the polarity control signal 15 controls output of the common voltage out-

put driver 14. Each output terminal of the source driver 10 is connected with one column of pixel units, and inputs a data voltage to each column of pixel units under the control effect of the source polarity control signal 18; each group of output terminals of the common voltage output driver 14 is connected with one row of pixel units, wherein in one row of pixel units of any two adjacent rows of pixel units, the odd output terminal in each group of output terminals of the common voltage output driver 14 is connected with pixel units of odd columns in this row of pixel units, the even output terminal in each group of output terminals of the common voltage output driver 14 is connected with pixel units of even columns in this row of pixel units; in the other row of pixel units in any two adjacent rows of pixel units, the odd output terminal in each group of output terminals of the common voltage output driver 14 is connected with pixel units of even columns in this row of pixel units, the even output terminal in each group of output terminals of the common voltage output driver 14 is connected with pixel units of odd columns in this row of pixel units. Each output terminal of the gate driver 16 is connected with one row of pixel units, for controlling ON and OFF of each row of pixel units.

[0064] Further, in the circuit as shown in Fig. 8, the structure of each pixel unit is same as the structure of the pixel unit in the embodiment as shown in Fig. 4, reference can be made to the structure of the pixel unit in the embodiment as shown in Fig. 4 specifically, which will not be repeated here.

[0065] Wherein, the method of the source driver 10, under the control effect of the source polarity control signal 18, for inputting a data voltage to each column of pixel units is similar as the method of the source driver 10 for inputting a data voltage to each column of pixel units in the prior art, reference can be made to the above related description on that the source driver 10 inputs a data voltage to each column of pixel units under the control effect of the source polarity control signal 18 in the embodiment as shown in Fig. 4 specifically, which will not be repeated here.

[0066] Exemplarily, as shown in Fig. 9, this figure is a working timing diagram of a pixel unit in the circuit as shown in Fig. 8 at the Nth frame. It can be seen from combination of Fig. 8 and Fig. 9 that at the moment T1 within the Nth frame, the gate driver 16 (the gate line scan signal of the gate driver is represented as Gn-1) opens the n-1th row of pixel units, the first polarity control signal 150 (represented as POL) is of a high level, the odd output terminal (represented as Vn-1,o) in the n-1th group of output terminals of the common voltage output driver 14 outputs a negative common voltage, the even output terminal (represented as Vn-1,e) in the n-1th group of output terminals of the common voltage output driver 14 outputs a positive common voltage. A plurality of output terminals of the source driver are under control of the source polarity control signal 18, when the Vn-1,o outputs a negative common voltage, the corresponding output terminal in the plurality of output terminals of the source

driver outputs a data voltage greater than or equal to the negative common voltage; when the $V_{n-1,e}$ outputs a positive common voltage, the corresponding output terminal in the plurality of output terminals of the source driver outputs a data voltage less than or equal to the positive common voltage, thereby enabling the polarity of the driving voltage of the $n-1$ th row of pixel units to be "+" (representing positive polarity), "-" (representing negative polarity), "+, -" from left to right successively (for example, the output of the source driver in pixel units of odd columns in the $n-1$ th row of pixel units is represented as $S_{n-1,o}$, the polarity of the driving voltage in pixel units of odd columns in the $n-1$ th row of pixel units is positive polarity; the output of the source driver in pixel units of even columns in the $n-1$ th row of pixel units is represented as $S_{n-1,e}$, the polarity of the driving voltage in pixel units of even columns in the $n-1$ th row of pixel units is negative polarity).

[0067] At the moment T_2 within the N th frame, the gate driver 16 (the gate line scan signal of the gate driver is represented as G_n) opens the n th row of pixel units, the first polarity control signal 150 becomes a low level. The odd output terminal (represented as $V_{n,o}$) in the n th group of output terminals of the common voltage output driver 14 outputs a positive common voltage, the even output terminal (represented as $V_{n,e}$) in the n th group of output terminals of the common voltage output driver 14 outputs a negative common voltage. A plurality of output terminals of the source driver are under control of the source polarity control signal 18, when the $V_{n,o}$ outputs a positive common voltage, the corresponding output terminal in the plurality of output terminals of the source driver outputs a data voltage less than or equal to the positive common voltage; when the $V_{n,e}$ outputs a negative common voltage, the corresponding output terminal in the plurality of output terminals of the source driver outputs a data voltage greater than or equal to the negative common voltage, thereby enabling the polarity of the driving voltage of the n th row of pixel units to be "-", "+, -, +" from left to right successively (for example, the output of the source driver in pixel units of odd columns in the n th row of pixel units is represented as $S_{n,o}$, the polarity of the driving voltage in pixel units of odd columns in the n th row of pixel units is negative polarity; the output of the source driver in pixel units of even columns in the n th row of pixel units is represented as $S_{n,e}$, the polarity of the driving voltage in pixel units of even columns in the n th row of pixel units is positive polarity).

[0068] The above description on the circuit as shown in Fig. 8 is only exemplary description made by taking one frame (e.g., the N th frame) as the example, at the adjacent frame of this frame, the polarities of the common voltage outputted by each output terminal of the common voltage output driver, the data voltage outputted by the source driver and the driving voltage of each pixel unit are all contrary to those in this frame. Since the implementing principle of the adjacent frame of this frame is same as the implementing principle of this frame, it will

not be repeated here.

[0069] It can be seen that in the circuit as shown in Fig. 8, the output of the source driver 10 is controlled through the source polarity control signal 18, and the output of the common voltage output driver 14 is controlled through the polarity control signal 15, such that the polarity of the driving voltage of any two adjacent pixel units can be reversed, for example, as shown in Fig. 6, thus it can be ensured that the display panel has a high quality display effect; in addition, compared with the prior art, since the common voltage is a voltage varying between positive and negative, in the event that the driving voltage of the liquid crystal molecules is invariable, the variation range of the data voltage outputted by the source driver is reduced, i.e., the maximum working voltages of the source driver and the display panel are both reduced also, thereby reducing the power consumption of the display panel.

[0070] Through the above solution, the display panel provided by an embodiment of the present invention can reduce the power consumption of the display panel while ensuring a high quality display effect.

[0071] The technical solution provided by an embodiment of the present invention, relative to the prior art, can reduce the variation range of the data voltage outputted by the source driver, i.e., enabling the maximum working voltage of the source driver and the maximum working voltage of the display panel to be both reduced. Specific description can make reference to the related descriptions on Fig. 1 and Fig. 3 in the above embodiments, which will not be repeated here.

[0072] Optionally, in an embodiment of the present invention, as stated above, a column of pixel units can be connected with a same data line (i.e., an output terminal of the source driver). Certainly, in a column of pixel units, the pixel units of odd rows can be connected with a same data line, pixel units of even rows can be connected with another data line adjacent to this data line, i.e., a column of pixel units are crossly connected with two adjacent data lines from up to down successively; when a column of pixel units are crossly connected with two adjacent data lines from up to down successively, in the display panel provided by an embodiment of the present invention, the variation of the logic level of the polarity control signal and the connecting manner of the pixel units and the common voltage output driver are all same as the related contents in the embodiment as shown in Fig. 8, which will not be repeated here.

[0073] It can be understood that no matter what kind of connecting manner is adopted for the pixel units and the common voltage output driver and how the direction of the polarity control signal is controlled in an embodiment of the present invention, as long as the common voltage output driver can input a common voltage varying between positive and negative to the pixel units, and when the common voltage output driver inputs a positive common voltage to a pixel unit, the source driver input a data voltage less than or equal to the positive common voltage to the pixel unit, and when the common voltage

output driver inputs a negative common voltage to the pixel unit, the source driver inputs a data voltage greater than or equal to the negative common voltage to the pixel unit, these implementing modes are all covered within the protection scope of the present invention.

[0074] Optionally, in an embodiment of the present invention, the polarity control signal controlling the odd output terminal and the even output terminal in each group of output terminals in the common voltage output driver to output different common voltage can be realized by using the circuit as shown in Fig. 7.

[0075] The related description on the circuit as shown in Fig. 7 can make reference to the description of the circuit as shown in Fig. 7 in the above embodiments, which will not be repeated here.

[0076] The above descriptions on that the common voltage inputted by the common voltage output driver to each pixel unit in the circuit as shown in Fig. 8 is a positive common voltage or a negative common voltage are all exemplary explanations made on the basis of the circuit as shown in Fig. 7, if the control effect of the first polarity control signal in Fig. 7 is realized by other circuits, the common voltage inputted by the common voltage output driver to each pixel unit in the circuit as shown in Fig. 8 will also vary accordingly, which will not be defined specifically in the present invention.

[0077] Optionally, combined with Fig. 2, as shown in Fig. 10, the display panel 1 provided by an embodiment of the present invention may further comprise a timing controller 17.

[0078] The timing controller 17 is used for generating a polarity control signal 15 and outputting the polarity control signal 15 to the common voltage output driver.

[0079] Optionally, the timing controller 17 is further used for generating a source polarity control signal 18 and outputting the source polarity control signal 18 to the source driver 10.

[0080] Optionally, the timing controller 17 is further used for storing a common voltage adjustment parameter and outputting the common voltage adjustment parameter to the common voltage output driver 14, the common voltage adjustment parameter is used for adjusting common voltages of pixel units having display defects.

[0081] The common voltage output driver 14 is further used for adjusting common voltages of pixel units having display defects based on the common voltage adjustment parameter.

[0082] In an embodiment of the present invention, when a certain pixel unit has display defects, the common voltage adjustment parameter stored in the timing controller can be used for adjusting the common voltage of the pixel unit having display defects. For example, the timing controller can output the common voltage adjustment parameter to the common voltage output driver to adjust the common voltage of the pixel unit having display defects by the common voltage output driver based on the common voltage adjustment parameter. The common voltages of some pixel units can be adjusted through

the common voltage adjustment parameter, thereby realizing local adjustment of the common voltage, so as to improve the problem of nonuniform image display of the liquid crystal display panel caused by influence of parasitic capacitance on the liquid crystal display panel to the common voltage, i.e., by adjusting the common voltage of the pixel unit having display defects, the image display of the pixel unit having display defects can be improved.

[0083] The embodiment of the present invention provides a display panel, the display panel comprises a source driver and a plurality of pixel units defined by a plurality of gate lines and a plurality of data lines arranged crossly, the display panel further comprises a common voltage output driver, the common voltage output driver is used for, at a Nth frame, inputting a negative common voltage to a first pixel unit, and at an adjacent frame of the Nth frame, inputting a positive common voltage to the first pixel unit, the first pixel unit is one of the plurality of pixel units, N is a positive integer; the source driver is used for, when the common voltage output driver inputs the negative common voltage to the first pixel unit, inputting a data voltage greater than or equal to the negative common voltage to the first pixel unit, and, when the common voltage output driver inputs the positive common voltage to the first pixel unit, inputting a data voltage less than or equal to the positive common voltage to the first pixel unit.

[0084] Based on the above technical solutions, since the common voltage output driver inputs alternately varying negative common voltages and positive common voltages to a same pixel unit within two adjacent frames respectively, and when the common voltage output driver inputs a negative common voltage to a certain pixel unit, the source driver inputs a data voltage greater than or equal to the negative voltage to this pixel unit, and when the common voltage output driver inputs a positive common voltage to a certain pixel unit, the source driver inputs a data voltage less than or equal to the positive common voltage to this pixel unit, such that: on the one hand, within two adjacent frames, the polarity of the driving voltage (which is the difference value of the data voltage and the common voltage) of the same pixel unit is reversed; on the other hand, compared with the prior art, since the common voltage is a voltage varying between positive and negative, in the event that the driving voltage of the liquid crystal molecules is invariable, the variation range of the data voltage outputted by the source driver is reduced, i.e., the maximum working voltages of the source driver and the display panel are both reduced also, thereby reducing the power consumption of the display panel.

[0085] An embodiment of the present invention provides a liquid crystal display device, the liquid crystal display device can comprise the display panel 1 stated in the above embodiment. The related description on the display panel 1 can make reference to the description on the display panel 1 in any one of the above Fig. 2 to Fig. 10, which will not be repeated here.

[0086] As shown in Fig. 11, an embodiment of the present invention further provides a driving method of a display panel, the driving method can be used for driving the display panel as stated in any of the above Fig. 2 to Fig. 10, the method may comprise:

S101, at a Nth frame, a common voltage output driver inputting a negative common voltage to a first pixel unit, the first pixel unit being one of a plurality of pixel units defined by a plurality of gate lines and a plurality of data lines arranged crossly, N being a positive integer, when the common voltage output driver inputs the negative common voltage to the first pixel unit, the source driver inputting a data voltage greater than or equal to the negative common voltage to the first pixel unit.

S102, at an adjacent frame of the Nth frame, the common voltage output driver inputting a positive common voltage to the first pixel unit, when the common voltage output driver inputs the positive common voltage to the first pixel unit, the source driver inputting a data voltage less than or equal to the positive common voltage to the first pixel unit.

[0087] The driving method of a display panel provided by an embodiment of the present invention can be applied in driving manners such as row reversion, column reversion and point reversion based on frame reversion (the reversions in this embodiment are all polarity reversion of the driving voltage of the pixel unit), which will not be defined specifically in the present invention.

[0088] The skilled person in the art can understand that compared with the driving manners of row reversion and column reversion, the driving manner of point reversion can increase the steady speed of the pixel unit voltage, and reduce cross talk between the pixels, hence, it can improve the display quality of the display panel so as to enable the display panel to have a high quality display effect.

[0089] Optionally, before the above S101, the driving method of a display panel provided by an embodiment of the present invention may further comprise:

S103, the common voltage output driver receiving a polarity control signal, a logic level of the polarity control signal at the Nth frame being contrary to a logic level of the polarity control signal at an adjacent frame of the Nth frame.

[0090] Wherein, a logic level of the polarity control signal at the Nth frame being contrary to a logic level of the polarity control signal at the adjacent frame of the Nth frame can be understood as: if the logic level of the polarity control signal is a high level at the Nth frame, the logic level of the polarity control signal will be a low level at the adjacent frame of the Nth frame; on the contrary,

if the logic level of the polarity control signal is a low level at the Nth frame, the logic level of the polarity control signal will be a high level at the adjacent frame of the Nth frame.

5 **[0091]** Further, the above S101 and S102 specifically may comprise:

10 S101a, at the Nth frame, when the polarity control signal is of a high level, the common voltage output driver inputting the negative common voltage to the first pixel unit.

15 S102a, at the adjacent frame of the Nth frame, when the polarity control signal is of a low level, the common voltage output driver inputting the positive common voltage to the first pixel unit.

[0092] Or, the above S101 and S102 specifically may comprise:

20 S101a, at the Nth frame, when the polarity control signal is of a low level, the common voltage output driver inputting the negative common voltage to the first pixel unit.

25 S102a, at the adjacent frame of the Nth frame, when the polarity control signal is of a high level, the common voltage output driver inputting the positive common voltage to the first pixel unit.

30 **[0093]** Specifically, the embodiment of the present invention can drive the display panel in the driving manner of point reversion, for example, refer to the above exemplary explanations made by taking the display panel as shown in Fig. 4 and Fig. 8 as the example. The related descriptions of Fig. 4 and Fig. 8 may refer to the related descriptions in the above embodiment, which will not be repeated here.

35 **[0094]** Optionally, one possible implementing mode of the driving method of a display panel provided by an embodiment of the present invention is that the polarity control signal comprises a first polarity control signal for controlling output of the common voltage output driver in pixel units of odd rows and pixel units of even rows, a logic level of the first polarity control signal in the pixel units of odd rows is contrary to a logic level of the first polarity control signal in the pixel units of even rows within the same frame.

40 **[0095]** Or, the polarity control signal comprises a second polarity control signal for controlling output of the common voltage output driver in pixel units of odd rows and a third polarity control signal for controlling output of the common voltage output driver in pixel units of even rows, a logic level of the second polarity control signal is contrary to a logic level of the third polarity control signal within the same frame, the logic levels of the second polarity control signal and the third polarity control signal are contrary within two adjacent frames.

45 **[0096]** The common voltage output driver comprises a plurality of groups of output terminals, each group of out-

put terminals comprise an odd output terminal and an even output terminal respectively, wherein when the odd output terminal outputs a negative common voltage, the even output terminal outputs a positive common voltage, or, when the odd output terminal outputs a positive common voltage, the even output terminal outputs a negative common voltage.

[0097] In the plurality of pixel units, pixel units of odd columns in each row of pixel units are connected with an odd output terminal in a corresponding group of output terminals of the common voltage output driver respectively, pixel units of even columns in each row of pixel units are connected with an even output terminal of the corresponding group of output terminals of the common voltage output driver respectively.

[0098] Specifically, in the one possible implementing mode stated above, the related descriptions on the structure of the pixel unit and the connecting manners of the pixel unit and the common voltage output driver can make reference to the above descriptions on the structure of the pixel unit and the connecting manners of the pixel unit and the common voltage output driver in the embodiment as shown in Fig. 4, which will not be repeated here.

[0099] Optionally, the other possible implementing mode of the driving method of a display panel provided by an embodiment of the present invention is that the polarity control signal is used for controlling output of the common voltage output driver in pixel units of odd rows and pixel units of even rows, the logic level of the polarity control signal is contrary within two adjacent frames.

[0100] The common voltage output driver comprises a plurality of groups of output terminals, each group of output terminals comprises an odd output terminal and an even output terminal respectively, wherein, when the odd output terminal outputs a negative common voltage, the even output terminal outputs a positive common voltage, or, when the odd output terminal outputs a positive common voltage, the even output terminal outputs a negative common voltage;

[0101] In the plurality of pixel units, pixel units of odd columns in one row of pixel units of any two adjacent rows of pixel units are connected with an odd output terminal in a group of output terminals of the common voltage output driver, the pixel units of even columns of the one row of pixel units are connected with an even output terminal in the group of output terminals of the common voltage output driver.

[0102] Pixel units of odd columns of the other row of pixel units in any two adjacent rows of pixel units are connected with an even output terminal in another group of output terminals of the common voltage output driver, pixel units of even columns of the other row of pixel units are connected with an odd output terminal in the other group of output terminals of the common voltage output driver

[0103] Specifically, in the other possible implementing mode stated above, the related descriptions on the structure of the pixel unit and the connecting manners of the

pixel unit and the common voltage output driver can make reference to the above descriptions on the structure of the pixel unit and the connecting manners of the pixel unit and the common voltage output driver in the embodiment as shown in Fig. 8, which will not be repeated here.

[0104] Optionally, the above display panel may further comprise a timing controller, before the above S101, the driving method of a display panel provided by an embodiment of the present invention may further comprise:

S103, the timing controller generating the polarity control signal and outputting the polarity control signal to the common voltage output driver.

[0105] Optionally, the driving method of a display panel provided by an embodiment of the present invention may further comprise:

S104, the timing controller outputting the common voltage adjustment parameter stored by it to the common voltage output driver.

S105, the common voltage output driver adjusting common voltages of pixel units having display defects based on the common voltage adjustment parameter.

[0106] In an embodiment of the present invention, when a certain pixel unit has display defects, e.g., non-uniform image display of the liquid crystal display panel caused by the influence of the parasitic capacitance on the liquid crystal display panel to the common voltage, the timing controller can output the voltage adjustment parameter stored by it to the common voltage output driver to adjust the common voltage of the pixel unit having display defects by the common voltage output driver based on the common voltage adjustment parameter, and provide the adjusted common voltage to the corresponding pixel unit. Thus, the common voltages of some pixel units can be adjusted through the common voltage adjustment parameter, thereby realizing local adjustment of the common voltage, so as to improve the problem of nonuniform image display of the liquid crystal display panel caused by influence of parasitic capacitance on the liquid crystal display panel to the common voltage, i.e., by adjusting the common voltage of the pixel unit having display defects, the image display of the pixel unit having display defects can be improved.

[0107] In an embodiment of the present invention, not only S101-S102 but also S104-S105 can be performed. For example, for part of the pixel units, e.g. pixel units having display defects, S104-S105 can be performed firstly, then S101-S102 are performed; for other pixel units, e.g., pixel units without display defects, S101-S102 can be performed only.

[0108] The embodiment of the present invention provides a driving method of a display panel, at a Nth frame, the common voltage output driver inputs a negative common voltage to a first pixel unit, the first pixel unit is one

of the plurality of pixel units defined by a plurality of gate lines and a plurality of data lines arranged crossly, N is a positive integer, when the common voltage output driver inputs the negative common voltage to the first pixel unit, the source driver inputs a data voltage greater than or equal to the negative common voltage to the first pixel unit; at an adjacent frame of the Nth frame, the common voltage output driver inputs a positive common voltage to the first pixel unit, when the common voltage output driver inputs the positive common voltage to the first pixel unit, the source driver inputs a data voltage less than or equal to the positive common voltage to the first pixel unit.

[0109] Based on the above technical solutions, since the common voltage output driver inputs alternately varying negative common voltages and positive common voltages to a same pixel unit within two adjacent frames respectively, and when the common voltage output driver inputs a negative common voltage to a certain pixel unit, the source driver inputs a data voltage greater than or equal to the negative voltage to this pixel unit, and when the common voltage output driver inputs a positive common voltage to a certain pixel unit, the source driver inputs a data voltage less than or equal to the positive common voltage to this pixel unit, such that: on the one hand, within two adjacent frames, the polarity of the driving voltage (which is the difference value of the data voltage and the common voltage) of the same pixel unit is reversed; on the other hand, compared with the prior art, since the common voltage is a voltage varying between positive and negative, in the event that the driving voltage of the liquid crystal molecules is invariable, the variation range of the data voltage outputted by the source driver is reduced, i.e., the maximum working voltages of the source driver and the display panel are both reduced also, thereby reducing the power consumption of the display panel.

[0110] The skilled person in the art can understand clearly that in order to describe the present invention conveniently and concisely, illustrations are only made through the above descriptions, in actual applications, it can also be implemented in other similar manners.

[0111] It should be understood that in several embodiments provided by the present invention, the disclosed circuit modules can also be implemented in other manners. That is, the circuit modules described above are only schematic.

[0112] Moreover, the unit explained as a separate component can be either physically separated or not physically separated, the component shown as a unit can be either a physical unit or not a physical unit. That is, the component can be located at a place, or can be distributed on a plurality of units. Part or all of the units thereof can be selected to carry out the embodiments of the present invention based on actual requirements.

[0113] In addition, the functional units in the respective embodiments of the present invention can be integrated in a processing unit, or, the respective units can be separate physical existence, or, two or more units can be

integrated in one unit. The above integrated units can be implemented in the form of hardware or in the form of software functional units.

[0114] What are stated above are only specific implementing modes of the present invention, however, the protection scope of the present invention is not limited to this. Any modifications or replacements that can be easily conceived by the skilled person familiar with the present technical field within the technical scope disclosed by the present invention should be encompassed within the protection scope of the present invention. Therefore, the protection scope of the present invention should be subject to the protection scopes of the claims attached.

Claims

1. A display panel comprising a source driver and a plurality of pixel units defined by a plurality of gate lines and a plurality of data lines arranged crossly, wherein the display panel further comprises a common voltage output driver, the common voltage output driver is used for, at a Nth frame, inputting a negative common voltage to a first pixel unit, and at an adjacent frame of the Nth frame, inputting a positive common voltage to the first pixel unit, the first pixel unit is one of the plurality of pixel units, N is a positive integer; the source driver is used for, when the common voltage output driver inputs the negative common voltage to the first pixel unit, inputting a data voltage greater than or equal to the negative common voltage to the first pixel unit, and, when the common voltage output driver inputs the positive common voltage to the first pixel unit, inputting a data voltage less than or equal to the positive common voltage to the first pixel unit.
2. The display panel according to claim 1, wherein, the common voltage output driver is further used for receiving a polarity control signal, a logic level of the polarity control signal at the Nth frame is contrary to a logic level of the polarity control signal at the adjacent frame of the Nth frame; wherein, at the Nth frame, when the polarity control signal is of a high level, the common voltage output driver inputs the negative common voltage to the first pixel unit, and at the adjacent frame of the Nth frame, when the polarity control signal is of a low level, the common voltage output driver inputs the positive common voltage to the first pixel unit; or at the Nth frame, when the polarity control signal is of a low level, the common voltage output driver inputs the negative common voltage to the first pixel unit, and at the adjacent frame of the Nth frame, when the polarity control signal is of a high level, the common voltage output driver inputs the positive common voltage to the first pixel unit.

3. The display panel according to claim 2, wherein, the polarity control signal comprises a first polarity control signal for controlling output of the common voltage output driver in pixel units of odd rows and pixel units of even rows, a logic level of the first polarity control signal in the pixel units of odd rows is contrary to a logic level of the first polarity control signal in the pixel units of even rows within the same frame, or, the polarity control signal comprises a second polarity control signal for controlling output of the common voltage output driver in pixel units of odd rows and a third polarity control signal for controlling output of the common voltage output driver in pixel units of even rows, a logic level of the second polarity control signal is contrary to a logic level of the third polarity control signal within the same frame, the logic levels of the second polarity control signal and the third polarity control signal are contrary within two adjacent frames; the common voltage output driver comprises a plurality of groups of output terminals, each group of output terminals comprise an odd output terminal and an even output terminal respectively, wherein when the odd output terminal outputs a negative common voltage, the even output terminal outputs a positive common voltage, or, when the odd output terminal outputs a positive common voltage, the even output terminal outputs a negative common voltage; in the plurality of pixel units, pixel units of odd columns in each row of pixel units are connected with an odd output terminal in a corresponding group of output terminals of the common voltage output driver respectively, pixel units of even columns in each row of pixel units are connected with an even output terminal of the corresponding group of output terminals of the common voltage output driver respectively.
4. The display panel according to claim 2, wherein the polarity control signal is used for controlling output of the common voltage output driver in pixel units of odd rows and pixel units of even rows, the logic level of the polarity control signal is contrary within two adjacent frames, the common voltage output driver comprises a plurality of groups of output terminals, each group of output terminals comprises an odd output terminal and an even output terminal respectively, wherein, when the odd output terminal outputs a negative common voltage, the even output terminal outputs a positive common voltage, or, when the odd output terminal outputs a positive common voltage, the even output terminal outputs a negative common voltage; in the plurality of pixel units, pixel units of odd columns in one row of pixel units of any two adjacent rows of pixel units are connected with an odd output terminal in a corresponding group of output terminals of the common voltage output driver, the pixel units of even columns of the one row of pixel units are connected with an even output terminal in the group of output terminals of the common voltage output driver; pixel units of odd columns of the other row of pixel units in any two adjacent rows of pixel units are connected with an even output terminal in the other group of output terminals of the common voltage output driver, pixel units of even columns of the other row of pixel units are connected with an odd output terminal in the other group of output terminals of the common voltage output driver.
5. The display panel according to any one of claims 2 to 4, wherein the display panel further comprises a timing controller, the timing controller is used for generating the polarity control signal and outputting the polarity control signal to the common voltage output driver.
6. The display panel according to claim 5, wherein, the timing controller is further used for storing a common voltage adjustment parameter and outputting the common voltage adjustment parameter to the common voltage output driver; the common voltage output driver is further used for adjusting common voltages of pixel units having display defects based on the common voltage adjustment parameter.
7. A liquid crystal display device comprising a display panel as claimed in any one of claims 1 to 6.
8. A driving method of a display panel for driving the display panel as claimed in claim 1, the driving method comprising:
at a Nth frame, a common voltage output driver inputting a negative common voltage to a first pixel unit, the first pixel unit being one of a plurality of pixel units defined by a plurality of gate lines and a plurality of data lines arranged crossly, N being a positive integer, when the common voltage output driver inputs the negative common voltage to the first pixel unit, the source driver inputting a data voltage greater than or equal to the negative common voltage to the first pixel unit;
at an adjacent frame of the Nth frame, the common voltage output driver inputting a positive common voltage to the first pixel unit, when the common voltage output driver inputs the positive common voltage to the first pixel unit, the source driver inputting a data voltage less than or equal to the positive common voltage to the first pixel unit.

9. The driving method according to claim 8, further comprising: the common voltage output driver receiving a polarity control signal, a logic level of the polarity control signal at the Nth frame being contrary to a logic level of the polarity control signal at an adjacent frame of the Nth frame;
 wherein, at the Nth frame, the common voltage output driver inputting a negative common voltage to the first pixel unit comprises: at the Nth frame, when the polarity control signal is of a high level, the common voltage output driver inputting the negative common voltage to the first pixel unit,
 at the adjacent frame of the Nth frame, the common voltage output driver inputting a positive common voltage to the first pixel unit comprises: at the adjacent frame of the Nth frame, when the polarity control signal is of a low level, the common voltage output driver inputting the positive common voltage to the first pixel unit; or,
 wherein, at the Nth frame, the common voltage output driver inputting a negative common voltage to the first pixel unit comprises: at the Nth frame, when the polarity control signal is of a low level, the common voltage output driver inputting the negative common voltage to the first pixel unit,
 at the adjacent frame of the Nth frame, the common voltage output driver inputting a positive common voltage to the first pixel unit comprises: at the adjacent frame of the Nth frame, when the polarity control signal is of a high level, the common voltage output driver inputting the positive common voltage to the first pixel unit.
10. The driving method according to claim 9, wherein the polarity control signal comprises a first polarity control signal for controlling output of the common voltage output driver in pixel units of odd rows and pixel units of even rows, a logic level of the first polarity control signal in the pixel units of odd rows is contrary to a logic level of the first polarity control signal in the pixel units of even rows within the same frame, or,
 the polarity control signal comprises a second polarity control signal for controlling output of the common voltage output driver in pixel units of odd rows and a third polarity control signal for controlling output of the common voltage output driver in pixel units of even rows, a logic level of the second polarity control signal is contrary to a logic level of the third polarity control signal within the same frame, the logic levels of the second polarity control signal and the third polarity control signal are contrary within two adjacent frames;
 the common voltage output driver comprises a plurality of groups of output terminals, each group of output terminals comprise an odd output terminal and an even output terminal respectively, wherein when the odd output terminal outputs a negative

common voltage, the even output terminal outputs a positive common voltage, or, when the odd output terminal outputs a positive common voltage, the even output terminal outputs a negative common voltage;

in the plurality of pixel units, pixel units of odd columns in each row of pixel units are connected with an odd output terminal in a corresponding group of output terminals of the common voltage output driver respectively, pixel units of even columns in each row of pixel units are connected with an even output terminal of the corresponding group of output terminals of the common voltage output driver respectively.

11. The driving method according to claim 9, wherein the polarity control signal is used for controlling output of the common voltage output driver in pixel units of odd rows and pixel units of even rows, the logic level of the polarity control signal is contrary within two adjacent frames, the common voltage output driver comprises a plurality of groups of output terminals, each group of output terminals comprises an odd output terminal and an even output terminal respectively, wherein, when the odd output terminal outputs a negative common voltage, the even output terminal outputs a positive common voltage, or, when the odd output terminal outputs a positive common voltage, the even output terminal outputs a negative common voltage;
 in the plurality of pixel units, pixel units of odd columns in one row of pixel units of any two adjacent rows of pixel units are connected with an odd output terminal in a corresponding group of output terminals of the common voltage output driver, the pixel units of even columns of the one row of pixel units are connected with an even output terminal in the group of output terminals of the common voltage output driver;
 pixel units of odd columns of the other row of pixel units in any two adjacent rows of pixel units are connected with an even output terminal in the other group of output terminals of the common voltage output driver, pixel units of even columns of the other row of pixel units are connected with an odd output terminal in the other group of output terminals of the common voltage output driver.

12. The driving method according to any one of claims 9 to 11, wherein the display panel further comprises a timing controller, the driving method further comprises:

the timing controller generating the polarity control signal and outputting the polarity control signal to the common voltage output driver.

13. The driving method according to claim 12, further comprising:

the timing controller storing a common voltage adjustment parameter and outputting the common voltage adjustment parameter to the common voltage output driver;
the common voltage output driver adjusting common voltages of pixel units having display defects based on the common voltage adjustment parameter.

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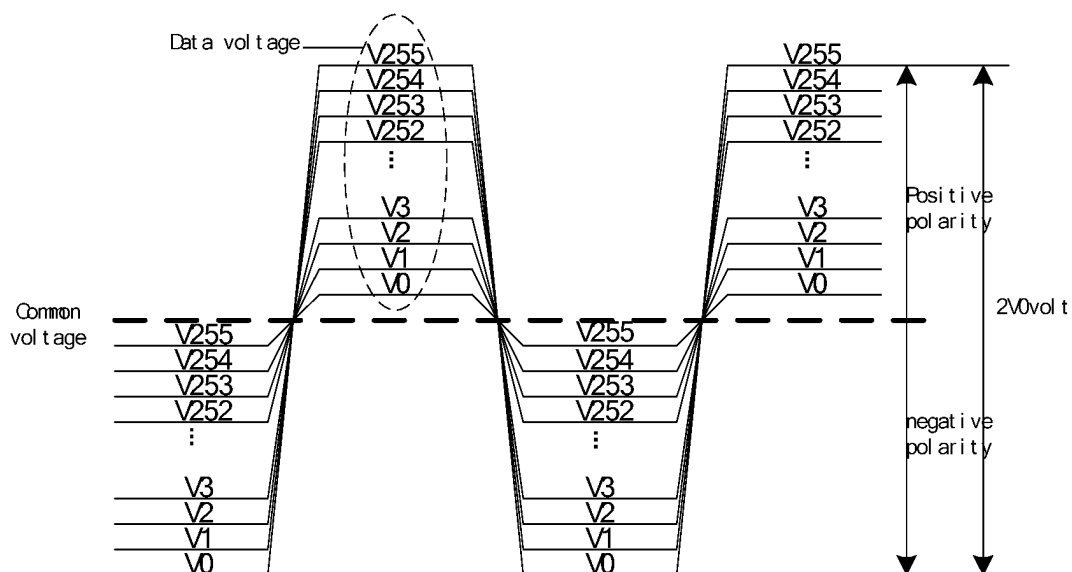


Fig. 1

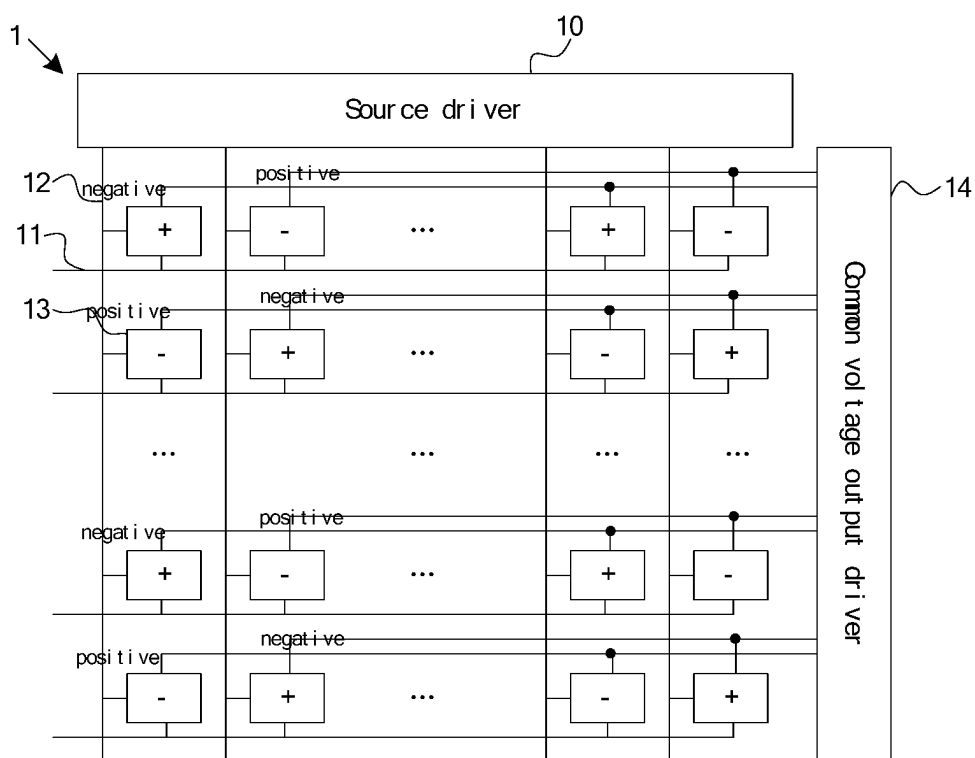


Fig. 2

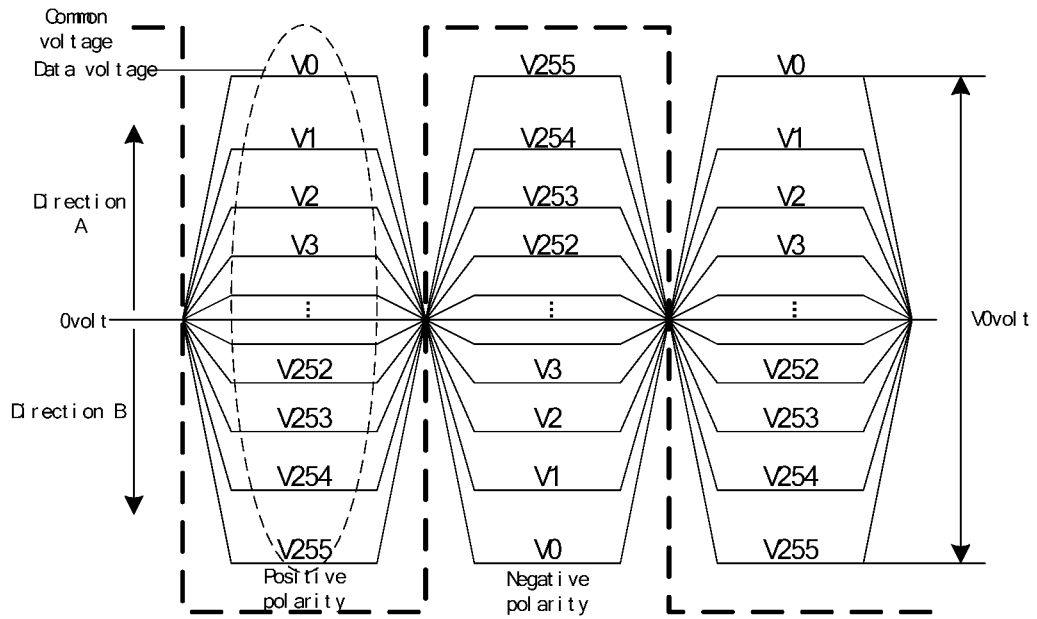


Fig. 3

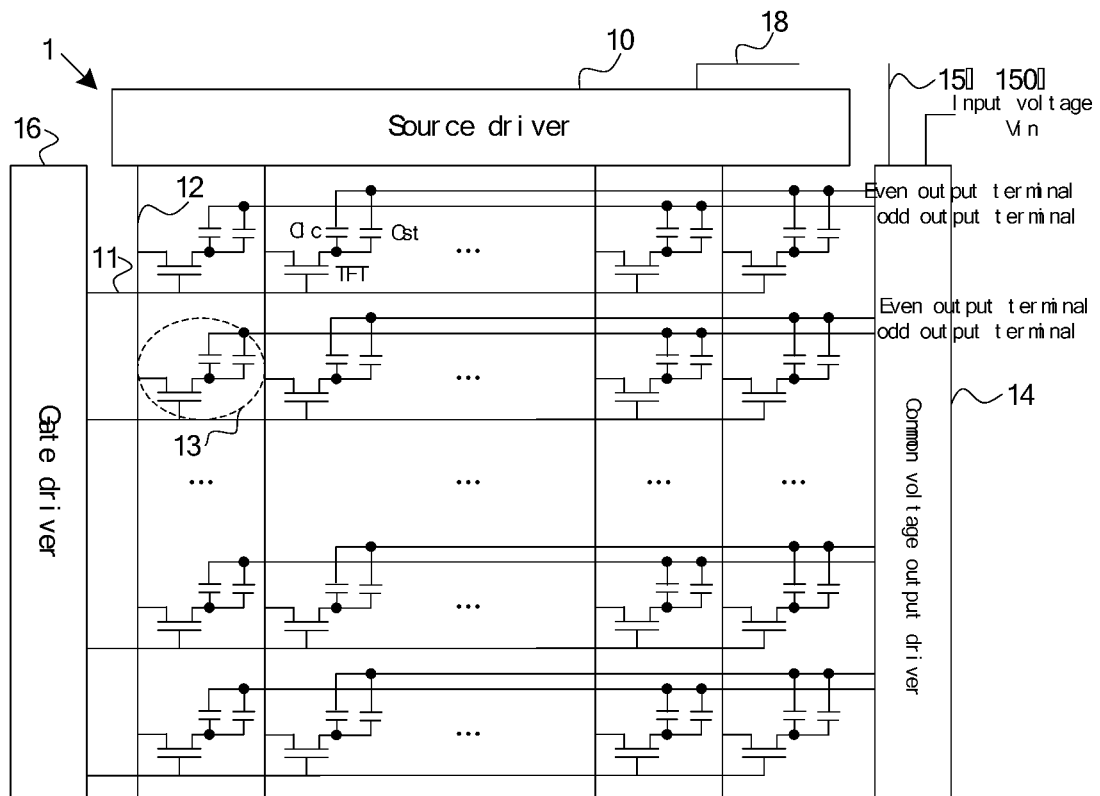


Fig. 4

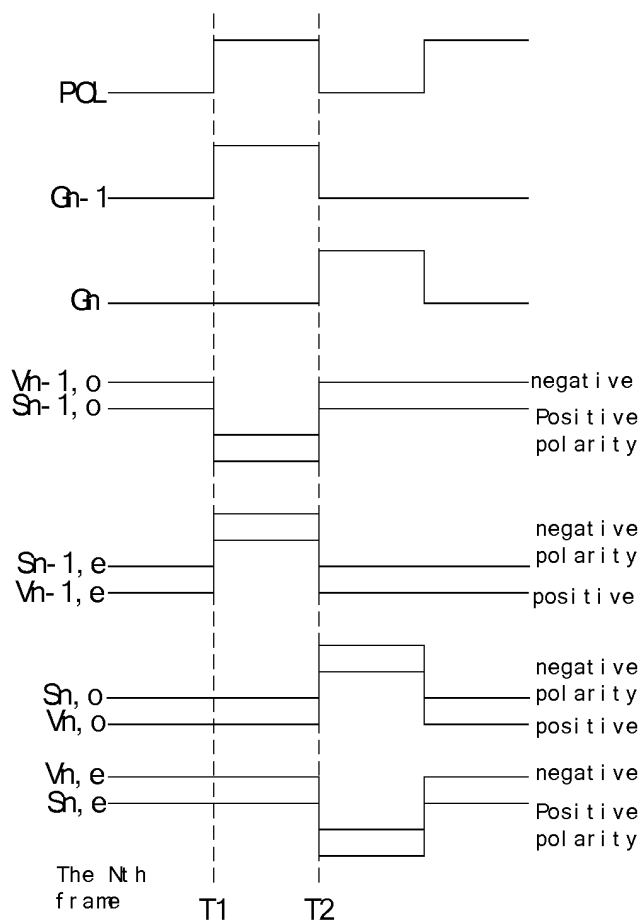


Fig. 5

+	-	+	-	+	-	+	-	+
-	+	-	+	-	+	-	+	-
+	-	+	-	+	-	+	-	+
-	+	-	+	-	+	-	+	-
+	-	+	-	+	-	+	-	+
-	+	-	+	-	+	-	+	-
+	-	+	-	+	-	+	-	+
-	+	-	+	-	+	-	+	-
+	-	+	-	+	-	+	-	+

Fig. 6

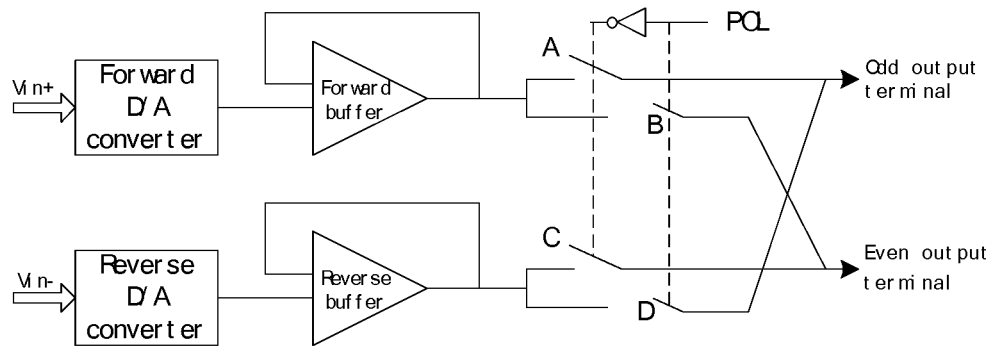


Fig. 7

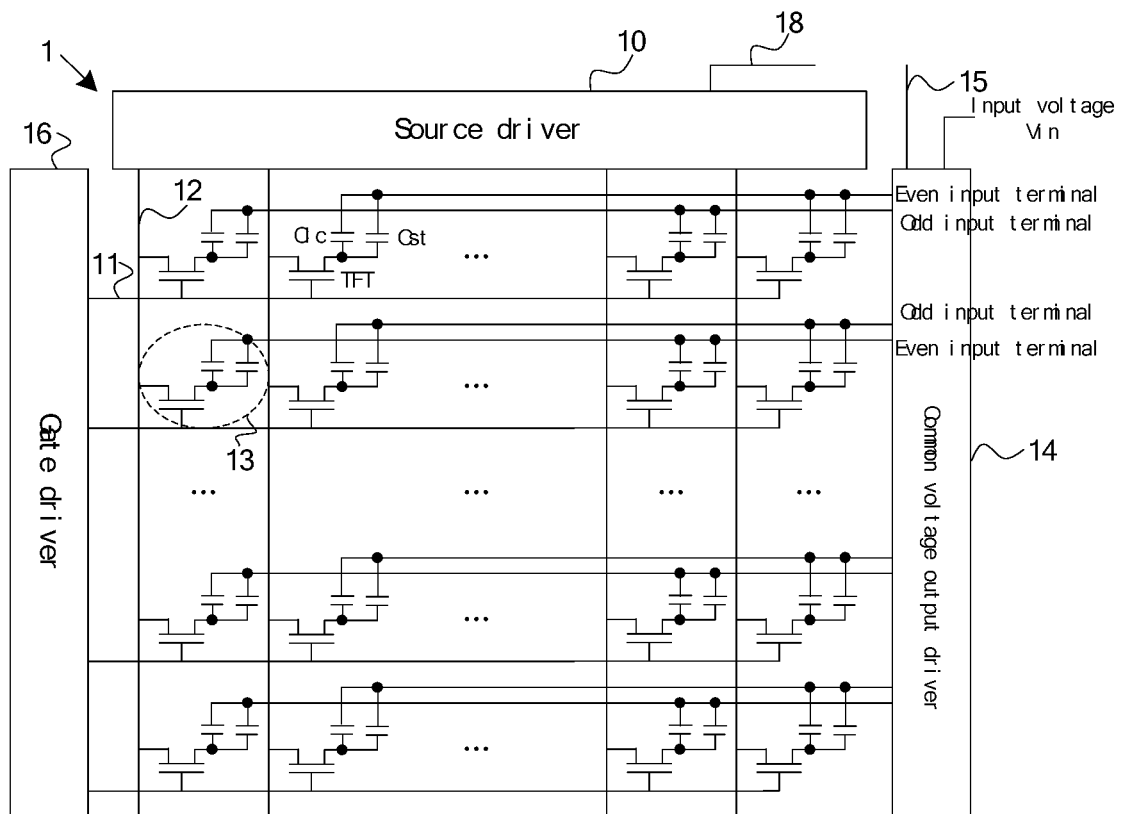


Fig. 8

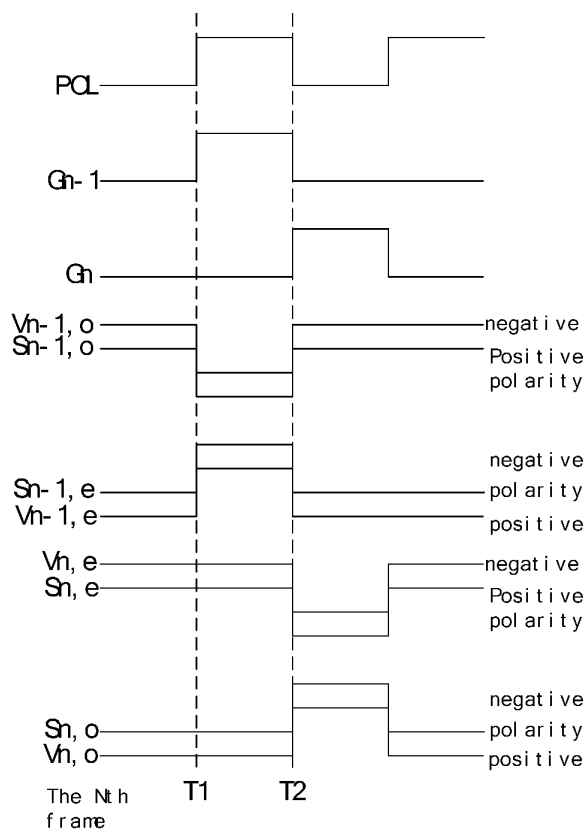


Fig. 9

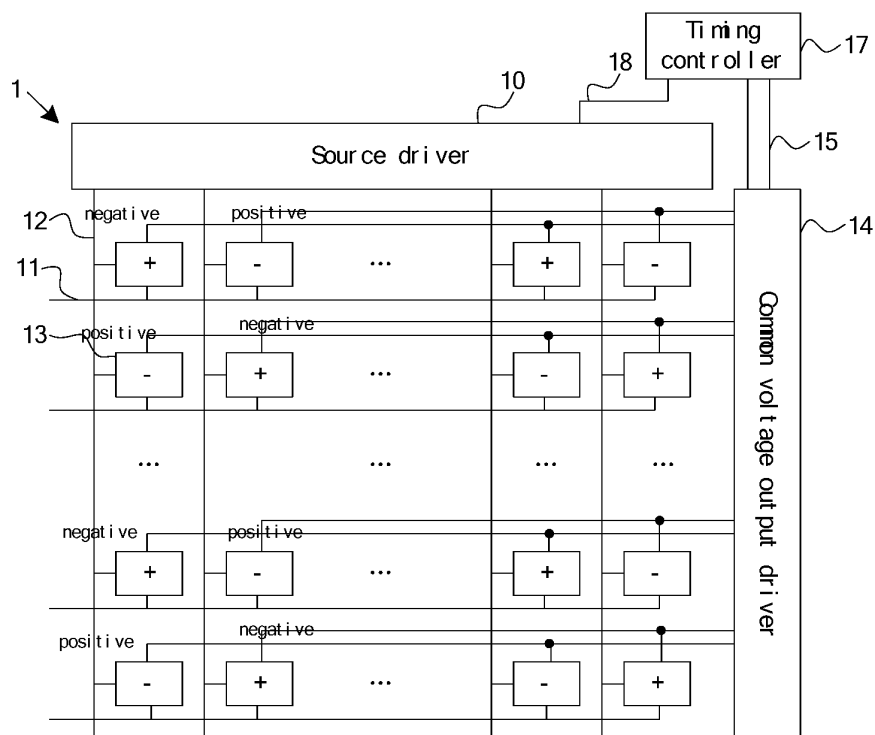


Fig. 10

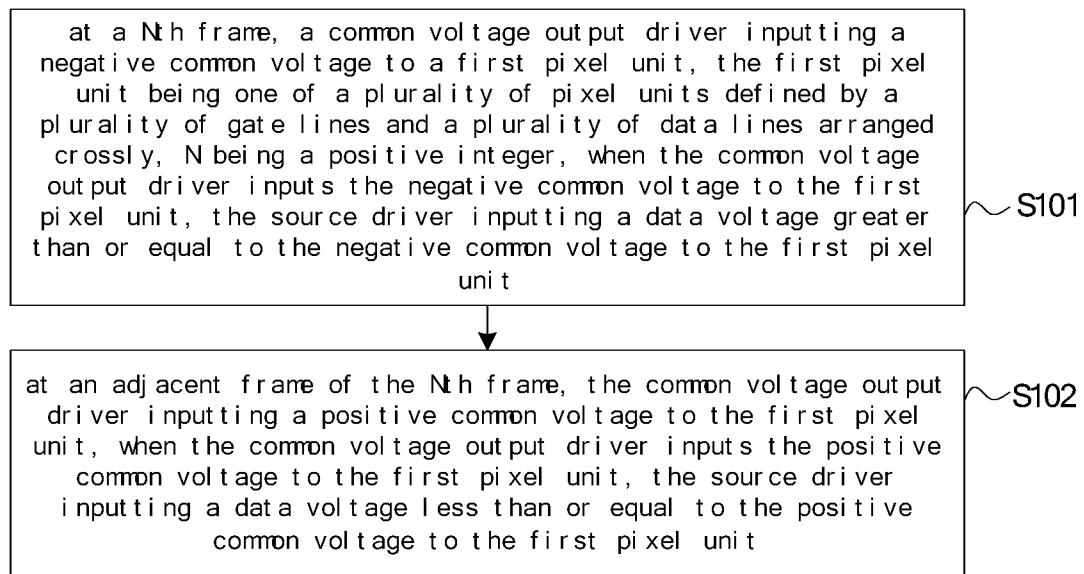


Fig. 11

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2015/084783

A. CLASSIFICATION OF SUBJECT MATTER

G09G 3/36 (2006.01) i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G09G 3; G02F 1

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT, CNKI, WPI, EPODOC: HUANG, Jiacheng; electrode voltage, two times, invert, common voltage, common signal, even number, odd number, sequential control, timing occurrence, polarity, Vcom, VCOM2, Vcomh, VCOMB, TCON, (tim??? w control+), tim???control+, odd, even, neighbo?r+, adjacent

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
PX	CN 104698645 A (HEFEI BOE OPTOELECTRONICS TECHNOLOGY CO., LTD. et al.), 10 June 2015 (10.06.2015), claims 1-13	1-13
X	US 2005088392 A1 (KIM, C.G. et al.), 28 April 2005 (28.04.2005), description, paragraphs 0052-0068, and figures 5-9B	1-5, 7-12
Y	US 2005088392 A1 (KIM, C.G. et al.), 28 April 2005 (28.04.2005), description, paragraphs 0052-0068, and figures 5-9B	6, 13
X	CN 102081245 A (INNOCOM TECHNOLOGY (SHENZHEN) CO., LTD. et al.), 01 June 2011 (01.06.2011), description, paragraphs 0018-0039, and figures 2-4	1-5, 7-12
Y	CN 102081245 A (INNOCOM TECHNOLOGY (SHENZHEN) CO., LTD. et al.), 01 June 2011 (01.06.2011), description, paragraphs 0018-0039, and figures 2-4	6, 13
Y	US 2008266222 A1 (INNOCOM TECHNOLOGY SHENZHEN CO., LTD. et al.), 30 October 2008 (30.10.2008), description, paragraphs 0025-0029 and 0033-0034, and figures 1-3 and 5	6, 13

☒ Further documents are listed in the continuation of Box C.☒ See patent family annex.

* Special categories of cited documents:

“A” document defining the general state of the art which is not considered to be of particular relevance

“E” earlier application or patent but published on or after the international filing date

“L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

“O” document referring to an oral disclosure, use, exhibition or other means

“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search

18 November 2015 (18.11.2015)

Date of mailing of the international search report

01 December 2015 (01.12.2015)

Name and mailing address of the ISA/CN:

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2015/084783

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C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	CN 101174397 A (NEC ELECTRONICS CORP.), 07 May 2008 (07.05.2008), the whole document	1-13
A	US 2002018035 A1 (SONG, J.K. et al.), 14 February 2002 (14.02.2002), the whole document	1-13
A	JP 2009223167 A (EPSON IMAGING DEVICES CORP.), 01 October 2009 (01.10.2009), the whole document	1-13

Form PCT/ISA/210 (continuation of second sheet) (July 2009)

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INTERNATIONAL SEARCH REPORT
 Information on patent family members

International application No.

PCT/CN2015/084783

Patent Documents referred in the Report	Publication Date	Patent Family	Publication Date
CN 104698645 A	10 June 2015	None	
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		KR 20050039017 A	29 April 2005
		KR 100561946 B1	21 March 2006
CN 102081245 A	01 June 2011	US 2011128272 A1	02 June 2011
US 2008266222 A1	30 October 2008	CN 101295110 A	29 October 2008
		CN 100582902 C	20 January 2010
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		US 2008174462 A1	24 July 2008
		JP 2008116654 A	22 May 2008
		US 7545305 B2	09 June 2009
		CN 101174397 B	05 September 2012
US 2002018035 A1	14 February 2002	KR 20020009900 A	02 February 2002
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		JP 2002055325 A	20 February 2002
		US 7068330 B2	27 June 2006
		JP 5025047 B2	12 September 2012
		KR 100338012 B	24 May 2002
JP 2009223167 A	01 October 2009	JP 5082960 B2	28 November 2012

Form PCT/ISA/210 (patent family annex) (July 2009)

专利名称(译)	显示面板及其驱动方法和液晶显示装置		
公开(公告)号	EP3279890A1	公开(公告)日	2018-02-07
申请号	EP2015834706	申请日	2015-07-22
[标]申请(专利权)人(译)	京东方科技集团股份有限公司 合肥京东方光电科技有限公司		
申请(专利权)人(译)	京东方科技集团股份有限公司. 合肥京东方光电科技有限公司.		
当前申请(专利权)人(译)	京东方科技集团股份有限公司. 合肥京东方光电科技有限公司.		
[标]发明人	HUANG JIACHENG		
发明人	HUANG, JIACHENG		
IPC分类号	G09G3/36		
CPC分类号	G02F1/13306 G09G3/3614 G09G3/3655 G09G3/3688 G09G3/3696 G09G2310/027 G09G2310/0291 G09G2310/0297 G09G2310/08 G09G2330/021 G09G2310/0213		
代理机构(译)	Fritzsche 也, THOMAS		
优先权	201510147865.5 2015-03-31 CN		
其他公开文献	EP3279890A4		
外部链接	Espacenet		

摘要(译)

本发明提供一种显示面板及其驱动方法，以及液晶显示装置，涉及液晶显示技术领域，可以降低显示面板的功耗。显示面板包括源极驱动器，由多条栅极线和多条交叉排列的数据线限定的多个像素单元，以及公共电压输出驱动器，公共电压输出驱动器用于第N帧，输入负公共电压到第一像素单元，并且在第N帧的相邻帧处，向第一像素单元输入正公共电压，第一像素单元是多个像素单元中的一个，N是正整数；当公共电压输出驱动器将负公共电压输入到第一像素单元时，将源驱动器用于输入大于或等于负公共电压的数据电压到第一像素单元，并且当公共电压输出时驱动器将正公共电压输入到第一像素单元，将小于或等于正公共电压的数据电压输入到第一像素单元。显示面板可以应用于液晶显示装置中。

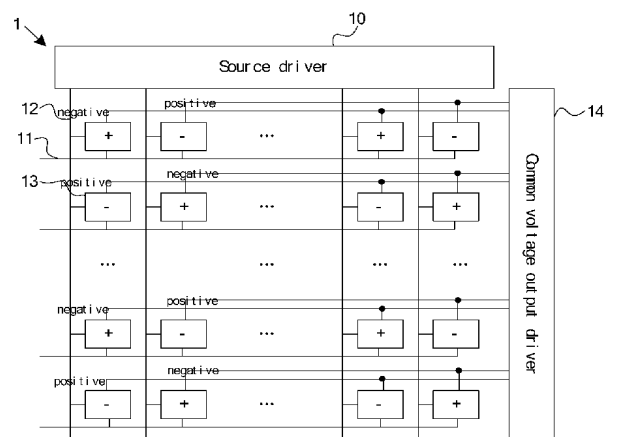


Fig. 2