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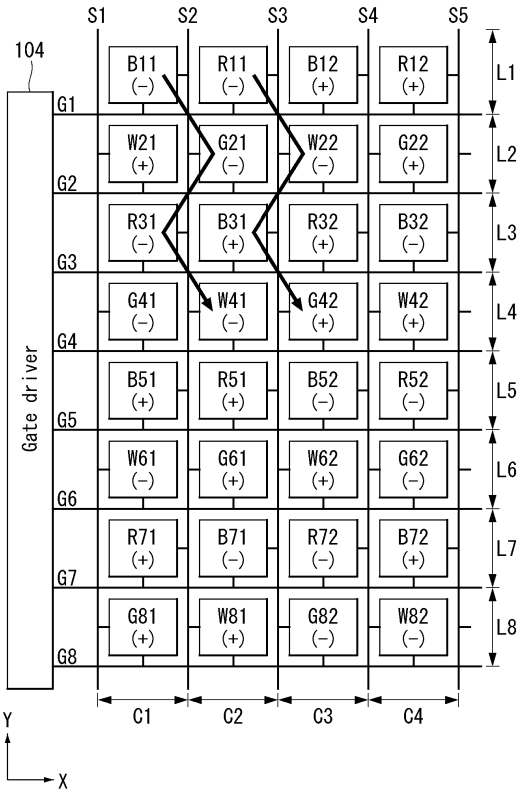
(54) LIQUID CRYSTAL DISPLAY DEVICE AND METHOD FOR DRIVING THE SAME

(57) A liquid crystal display device and a method for driving the same are disclosed. The first-color subpixels are arranged at positions where (4i+1)th row lines (i is a positive integer) and odd-numbered column lines intersect, and the second-color subpixels are arranged at positions where the (4i+1)th row lines and even-numbered column lines intersect. The third-color subpixels are arranged at positions where (4i+2)th row lines and the odd-numbered column lines intersect, and the fourth-color subpixels are arranged at positions where the (4i+2)th row lines and the even-numbered column lines intersect.

FIG. 3



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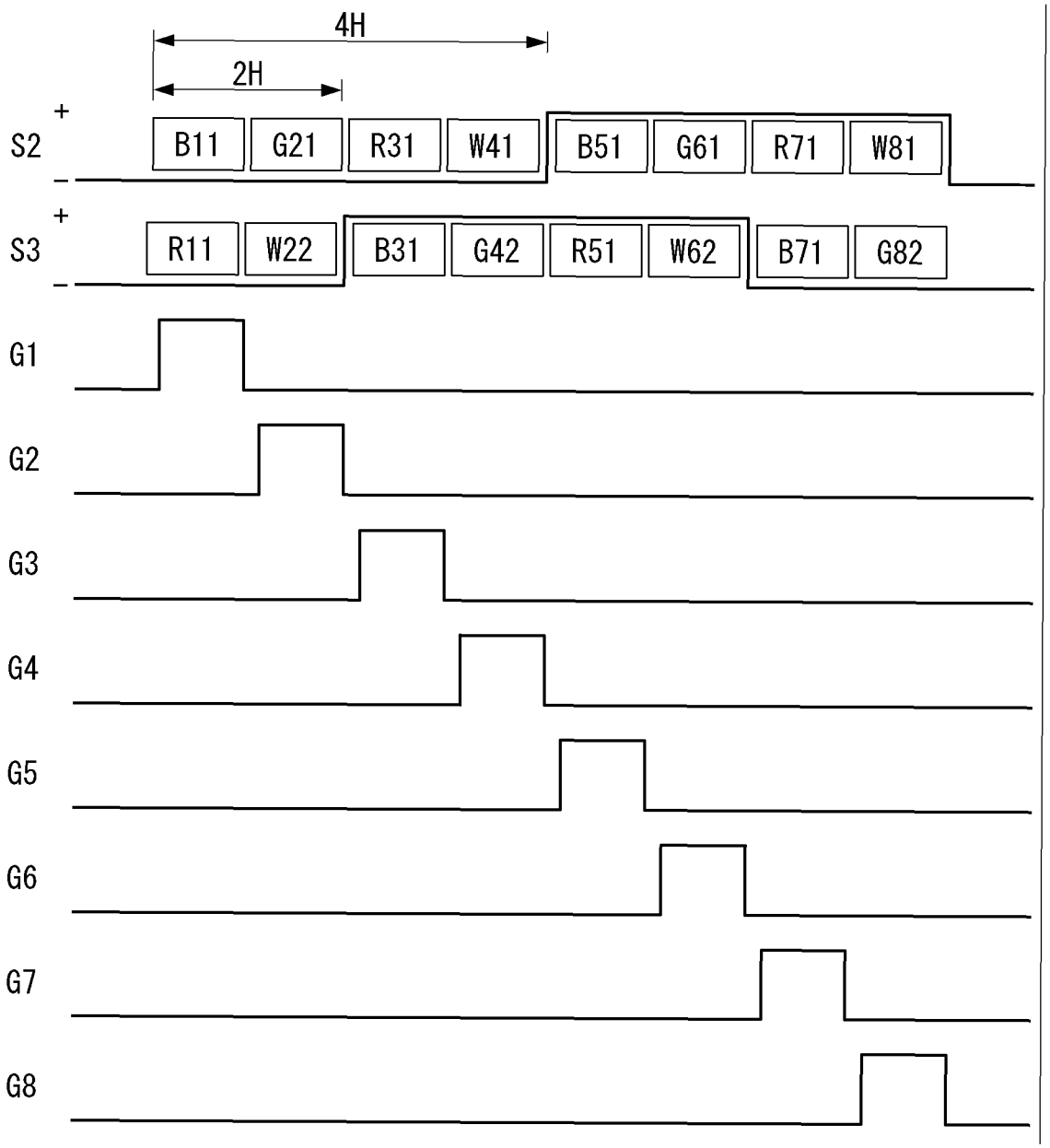
(Cont. next page)

FIG. 4


4H
2H
S2
+
−
B11
G21
R31
W41
B51
G61
R71
W81
S3
+
−
R11
W22
B31
G42
R51
W62
B71
G82
G1
G2
G3
G4
G5
G6
G7
G8

Description

[0001] This application claims the benefit of Korean Patent Application No. 10-2016-0067776 filed on May 31, 2016.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention relates to a display device comprising red (R) subpixels, green (G) subpixels, blue (B) subpixels, and white (W) subpixels and a method for driving the same.

Discussion of the Related Art

[0003] A liquid crystal display displays an image by controlling an electric field applied to liquid crystal molecules according to a data voltage. Driven by the development of processing technology and driving technology, active-matrix liquid-crystal displays have dropped in price and increased in performance, and thus are one of the most widely used displays across almost all display applications, from small mobile devices to large televisions.

[0004] A liquid crystal display has a liquid crystal display panel, a backlight unit for illuminating the liquid crystal display panel, a source drive integrated circuit (hereinafter also referred to as integrated circuit, IC) for supplying data voltages to data lines of the liquid crystal display panel, a gate drive IC for supplying gate pulses (or scan pulses) to gate lines (or scan lines) of the liquid crystal display panel, a control circuit for controlling the ICs, and a light source drive circuit for driving the light source of the backlight unit.

[0005] A liquid crystal display comprising red (R) subpixels, green (G) subpixels, blue (B) subpixels, and white (W) subpixels is now being developed. Hereinafter, such a display device will be referred to as an "RGBW-type display device". In the following, a white (W) subpixel will be referred as a white-colored subpixel. So, the RGBW-type display device preferably comprises subpixels of four different colors, namely red, green, blue and white. The W subpixels can adjust the brightness of the backlight unit. By increasing the brightness of individual pixels, the brightness of the backlight unit can be lowered, thus resulting in lower power consumption of the liquid crystal display.

[0006] Triple Rate Driving, short: TRD, is known as a technology that triples the data driving frequency of a pixel array, in order to reduce the number of source drive ICs (IC) in a liquid crystal display.

[0007] In a liquid crystal display with a typical pixel structure, RGB data voltages are supplied to one pixel's subpixels through three data lines during one horizontal period. In contrast, in the TRD technology, RGB data voltages are sequentially supplied to RGB subpixels though one data line. For example, an R data voltage is supplied to a red subpixel during a 1/3 horizontal period. Subsequently, a G data voltage is supplied to a green subpixel during a 1/3 horizontal period, and a B data voltage is then supplied to a blue subpixel during a 1/3 horizontal period. Thus, the TRD technology enables to reduce the number of data lines to 1/3, as compared to the typical pixel structure.

[0008] The TRD technology has the following problems when used in RGBW-type display devices.

[0009] First of all, data voltages supplied to subpixels of the same color connected to the same gate line may be dominated to one polarity. Due to this, a common voltage, which is a reference voltage for liquid crystals, may be shifted to the dominant polarity, thus causing horizontal crosstalk.

[0010] Secondly, if the polarity of a data voltage is reversed by column inversion to reduce heat generated from the source drive ICs, polarity banding phenomenon may occur. Polarity banding phenomenon means that neighboring subpixels are charged with data voltages of the same polarity. Polarity banding phenomenon causes uneven brightness. If there is polarity banding phenomenon, especially in neighboring subpixels of the same color, it leads to unevenness in brightness and color reproduction.

[0011] Thirdly, the source drive ICs generate more heat since more data voltage transitions occur with a specific color.

SUMMARY

[0012] Accordingly, the present invention is directed to a liquid crystal display device, preferably RGBW-type display device, which can reduce heat generation from source drive ICs and improve picture quality, in order to drive a display panel comprising subpixels of different colors, e.g. RGBW subpixels.

[0013] An exemplary embodiment of the present invention provides a liquid crystal display device comprising: a data driver that reverses the polarity of data voltages for charging subpixels on a preset cycle and supplies the data voltages to data lines; and a gate driver that supplies gate pulses to gate lines in synchronization with the data voltages.

[0014] In a pixel array where the pixels are arranged, the first-color subpixels are arranged at positions where (4i+1)th row lines (i is a positive integer) and odd-numbered column lines intersect, the second-color subpixels are arranged at positions where the (4i+1)th row lines and even-numbered column lines intersect. The third-color subpixels are arranged

at positions where (4i+2)th row lines and the odd-numbered column lines intersect, and the fourth-color subpixels are arranged at positions where the (4i+2)th row lines and the even-numbered column lines intersect. The second-color subpixels are arranged at positions where (4i+3)th row lines and the odd-numbered column lines intersect, and the first-color subpixels are arranged at positions where the (4i+3)th row lines and the even-numbered column lines intersect. The fourth-color subpixels are arranged at positions where (4i+4)th row lines and the odd-numbered column lines intersect, and the third-color subpixels are arranged at positions where the (4i+4)th row lines and the even-numbered column lines intersect.

[0015] In the following description the term "first side" is referred to a "right side (=right)" of a subpixel arrangement and the term "second side" is referred to a "left side (=left)" of the same subpixel arrangement when considered its top/bottom view. The "right side (=first side)" is arranged on an opposite side of the "left side (second side)" of the same subpixel or the same subpixels or the same subpixel arrangement. The term "side" is referred to a "lateral side" of the subpixel that is located in parallel to "column lines" of signal lines on the display panel and that is located vertical to "row lines" in that display panel when considered its top/bottom view.

[0016] In the following description the term "column line" is referred to an orientation of a signal line, preferably a data line, in the display panel that is in parallel to the "first side" or the "second side". Respectively the term "row line" is referred to an orientation of another signal line, preferably a gate line, in the same display panel that is arranged vertical to the first side or the second side in that display panel.

[0017] According to a preferred embodiment, the first color- and second-color subpixels may be arranged on the (4i+1)th row lines comprise thin-film transistors, TFTs, that supply data voltages from the data lines to the right of the subpixels to the pixel electrodes. The third-color- and fourth-color subpixels are preferably arranged on the (4i+2)th row lines comprise TFTs that supply data voltages from the data lines to the left of the subpixels to the pixel electrodes. The first color- and second-color subpixels are preferably arranged on the (4i+3)th row lines comprise TFTs that supply data voltages from the data lines to the right of the subpixels to the pixel electrodes. The third-color- and fourth-color subpixels may be arranged on the (4i+4)th row lines comprise TFTs that supply data voltages from the data lines to the left of the subpixels to the pixel electrodes.

[0018] According to a preferred exemplary embodiment, the data driver may supply the data lines with data voltages whose polarity is reversed on a cycle of every 4 horizontal periods. Preferably, the gate driver sequentially supplies the gate pulses to the gate lines in order: first gate line, second gate line, third gate line, and fourth gate line. Preferably, the polarity of the data voltages supplied to the data lines is reversed on data voltages of the first color, and there is a difference of 2 horizontal periods between the polarity reversal timing of data voltages supplied to the odd-numbered data lines and the polarity reversal timing of data voltages supplied to the even-numbered data lines.

[0019] According to a preferred exemplary embodiment, the first color is blue, the second color is red, the third color is white, and the fourth color is green.

[0020] According to a preferred exemplary embodiment, the first color- and second-color subpixels arranged on the (4i+1)th row lines may comprise TFTs (thin-film transistors) that supply data voltages from the data lines to the right of the subpixels to the pixel electrodes. Preferably, the third-color- and fourth-color subpixels arranged on the (4i+2)th row lines may comprise TFTs that supply data voltages from the data lines to the right of the subpixels to the pixel electrodes. Preferably, the first color- and second-color subpixels arranged on the (4i+3)th row lines may comprise TFTs that supply data voltages from the data lines to the left of the subpixels to the pixel electrodes. Preferably, the third-color- and fourth-color subpixels arranged on the (4i+4)th row lines may comprise TFTs that supply data voltages from the data lines to the left of the subpixels to the pixel electrodes.

[0021] According to a preferred exemplary embodiment, the data driver supplies the data lines with data voltages whose polarity is reversed on a cycle of every 4 horizontal periods, and simultaneously reverses the polarity of the data voltages supplied to the odd-numbered data lines and the polarity of the data voltages supplied to the even-numbered data lines. Preferably, the polarity of the data voltages supplied to the odd-numbered data lines is reversed on data voltages of the fourth color, and the polarity of the data voltages supplied to the even-numbered data lines is reversed on data voltages of the third color. Preferably, the gate driver outputs the gate pulses in order: first gate pulse, second gate pulse, third gate pulse, and fourth gate pulse. Preferably, among link lines connecting output channels of the gate driver and the gate lines, the link lines connecting the output channels of the second and third gate pulses and the second and third gate lines intersect so that the third gate pulse is applied to the second gate line after the second gate pulse is applied to the third gate line.

[0022] According to a preferred exemplary embodiment, the first color- and second-color subpixels arranged on the (4i+1)th row lines may comprise TFTs (thin-film transistors) that supply data voltages from the data lines to the right of the subpixels to the pixel electrodes. Preferably, the third-color- and fourth-color subpixels arranged on the (4i+2)th row lines may comprise TFTs that supply data voltages from the data lines to the right of the subpixels to the pixel electrodes. Preferably, the first color- and second-color subpixels arranged on the (4i+3)th row lines may comprise TFTs that supply data voltages from the data lines to the right of the subpixels to the pixel electrodes. Preferably, the third-color- and fourth-color subpixels arranged on the (4i+4)th row lines may comprise TFTs that supply data voltages from the data

lines to the left of the subpixels to the pixel electrodes.

[0023] According to a preferred exemplary embodiment, the data driver supplies the data lines with data voltages whose polarity is reversed on a cycle of every 4 horizontal periods. Preferably, the polarity of the data voltages is supplied to the odd-numbered data lines is reversed on data voltages of the fourth color, and the polarity of the data voltages supplied to the even-numbered data lines is reversed on data voltages of the second color, the fourth data voltage after reversal of the polarity of a data voltage supplied to each data line is a data voltage of the fourth color, and there is a difference of 1 horizontal period between the polarity reversal timing of data voltages supplied to the odd-numbered data lines and the polarity reversal timing of data voltages supplied to the even-numbered data lines. Preferably, the gate driver may output the gate pulses in order: first gate pulse, second gate pulse, third gate pulse and fourth gate pulse. Preferably, among link lines connecting output channels of the gate driver and the gate lines, the link lines connecting the output channels of the second and third gate pulses and the second and third gate lines intersect so that the third gate pulse is applied to the second gate line after the second gate pulse is applied to the third gate line.

[0024] According to a preferred exemplary embodiment, the first color- and second-color subpixels arranged on the (4i+1)th row lines may comprise TFTs (thin-film transistors) that supply data voltages from the data lines to the left of the subpixels to the pixel electrodes. Preferably, the third-color- and fourth-color subpixels arranged on the (4i+2)th row lines may comprise TFTs that supply data voltages from the data lines to the right of the subpixels to the pixel electrodes. Preferably, the first color- and second-color subpixels arranged on the (4i+3)th row lines may comprise TFTs that supply data voltages from the data lines to the right of the subpixels to the pixel electrodes. Preferably, the third-color- and fourth-color subpixels arranged on the (4i+4)th row lines may comprise TFTs that supply data voltages from the data lines to the right of the subpixels to the pixel electrodes.

[0025] According to a preferred exemplary embodiment, the data driver supplies the data lines with data voltages whose polarity is reversed on a cycle of every 4 horizontal periods. Preferably, the polarity of the data voltages supplied to the data lines is reversed on data voltages of the fourth color, and there is a difference of 1 horizontal period between the polarity reversal timing of data voltages supplied to the odd-numbered data lines and the polarity reversal timing of data voltages supplied to the even-numbered data lines. Preferably, the gate driver outputs the gate pulses in order: first gate pulse, second gate pulse, third gate pulse, and fourth gate pulse. Preferably, among link lines connecting output channels of the gate driver and the gate lines, the link lines connecting the output channels of the second and third gate pulses and the second and third gate lines intersect so that the third gate pulse is applied to the second gate line after the second gate pulse is applied to the third gate line.

[0026] According to a preferred exemplary embodiment, the first color is white, the second color is green, the third color is red, and the fourth color is blue.

[0027] According to an exemplary embodiment there is provided a method for driving a liquid crystal display device that comprises a plurality of data lines, a plurality of gate lines intersecting the data lines, a plurality of first-color subpixels, a plurality of second-color subpixels, a plurality of third-color subpixels, and a plurality of fourth-color subpixels according to one of the preceding claims, comprising the steps of: Supplying the data lines with data voltages whose polarity is reversed on a cycle of every 4 horizontal periods by means of a data driver; Suppling gate pulses to the gate lines in synchronization with the data voltages in the order: first gate line, second gate line, third gate line, and fourth gate line by means of a data driver, wherein the data driver supplies the data lines with data voltages whose polarity is reversed on a cycle of every 4 horizontal periods; and wherein, among link lines connecting output channels of the gate driver and the gate lines, the link lines connecting the output channels of the second and third gate pulses and the second and third gate lines intersect so that the third gate pulse is applied to the second gate line after the second gate pulse is applied to the third gate line.

BRIEF DESCRIPTION OF THE DRAWINGS

[0028] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention. In the drawings:

FIG. 1 is a block diagram of a liquid crystal display device according to an exemplary embodiment of the present invention;

FIGS. 2 and 3 are views showing a pixel array structure and a data voltage charging sequence according to a first exemplary embodiment of the present invention;

FIG. 4 is a waveform diagram showing output signals from source drive ICs and a gate driver for driving the pixel array of FIGS. 2 and 3;

FIGS. 5A to 5G are views showing which subpixels are lit up and their polarity, when white, red, green, blue, yellow, cyan, and magenta patterns are displayed on the pixel array according to the first exemplary embodiment of the present invention;

FIGS. 6A to 6G are views showing data voltages when the colors of FIGS. 5A to 5G are displayed on the pixel array;
FIGS. 7 and 8 are views showing a pixel array structure and a data voltage charging sequence according to a second exemplary embodiment of the present invention;
FIG. 9 is a waveform diagram showing output signals from source drive ICs and a gate driver for driving the pixel array of FIGS. 7 and 8;
FIGS. 10A to 10G are views showing which subpixels are lit up and their polarity, when white, red, green, blue, yellow, cyan, and magenta patterns are displayed on the pixel array according to the second exemplary embodiment of the present invention;
FIGS. 11A to 11G are views showing data voltages when the colors of FIGS. 10A to 10G are displayed on the pixel array;
FIGS. 12 and 13 are views showing a pixel array structure and a data voltage charging sequence according to a third exemplary embodiment of the present invention;
FIG. 14 is a waveform diagram showing output signals from source drive ICs and a gate driver for driving the pixel array of FIGS. 12 and 13;
FIGS. 15A to 15G are views showing which subpixels are lit up and their polarity, when white, red, green, blue, yellow, cyan, and magenta patterns are displayed on the pixel array according to the third exemplary embodiment of the present invention;
FIGS. 16A to 16G are views showing data voltages when the colors of FIGS. 15A to 15G are displayed on the pixel array;
FIGS. 17 and 18 are views showing a pixel array structure and a data voltage charging sequence according to a fourth exemplary embodiment of the present invention;
FIG. 19 is a waveform diagram showing output signals from source drive ICs and a gate driver for driving the pixel array of FIGS. 17 and 18;
FIGS. 20A to 20G are views showing which subpixels are lit up and their polarity, when white, red, green, blue, yellow, cyan, and magenta patterns are displayed on the pixel array according to the fourth exemplary embodiment of the present invention; and
FIGS. 21A to 21G are views showing data voltages when the colors of FIGS. 20A to 20G are displayed on the pixel array.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

[0029] Hereinafter, exemplary embodiments of the present invention will be described in detail with reference to the attached drawings. Throughout the specification, like reference numerals denote substantially like components. In describing the present invention, detailed descriptions of known functions or configurations related to the present invention will be omitted when it is deemed that they may unnecessarily obscure the subject matter of the present invention.

[0030] Referring to FIG. 1, a liquid crystal display device according to the present invention has a display panel 100 with a pixel array and a display panel drive circuit for writing data for an input image to the display panel 100. A backlight unit for evenly illuminating the display panel 100 may be disposed under the display panel 100.

[0031] In order to reduce the number of source drive ICs, this display device supplies red data (hereinafter, "R data"), green data (hereinafter, "G data"), blue data (hereinafter, "B data), and white data (hereinafter, "W data") to pixels through one data line, preferably only one data line.

[0032] The display panel 100 comprises an upper substrate and a lower substrate that face each other with a liquid crystal layer in between. A pixel array on the display panel 100 comprises pixels that are arranged in a matrix by the intersections of data lines S1 to Sm and gate lines G1 to Gn.

[0033] Each pixel may comprise subpixels of two colors, three colors, or four colors, among an R subpixel for R data to be written to it, a G subpixel for G data to be written to it, a B subpixel for B data to be written to it, and a W subpixel for W data to be written to it. In a case where one pixel comprises subpixels of four colors, each pixel may comprise RGBW subpixels. In a case where one pixel comprises subpixels of three colors, a first pixel may comprise WRG subpixels and a second pixel neighboring the first pixel may comprise BWR subpixels. In this case, a preset subpixel rendering algorithm may be used to distribute a data value for the color each pixel lacks among one or more surrounding pixels to compensate for the color. Each subpixel is longer along the row line X than along the column line Y and has a TFT.

[0034] An arrangement of colors in the pixel array are as shown in FIGS 2 and 3, FIGS. 7 and 8, FIGS. 12 and 13, and FIGS. 17 and 18. In this pixel array, first-color subpixels and second-color subpixels are alternately arranged on the (4i+1)th row lines L1 and L5 (i is a positive integer). The first-color subpixels are arranged at positions where the (4i+1)th row lines L1 and L5 and the odd-numbered column lines C1 and C3 intersect. The second-color subpixels are arranged at positions where the (4i+1)th row lines L1 and L5 and the even-numbered column lines C2 and C4 intersect.

[0035] Third-color subpixels and fourth-color subpixels are alternately arranged on the (4i+2)th row lines L2 and L6. The third-color subpixels are arranged at positions where the (4i+2)th row lines L2 and L6 and the odd-numbered column

lines C1 and C3 intersect. The fourth-color subpixels are arranged at positions where the (4i+2)th row lines L2 and L6 and the even-numbered column lines C2 and C4 intersect.

[0036] Second-color subpixels and first-color subpixels are alternately arranged on the (4i+3)th row lines L3 and L7. The second-color subpixels are arranged at positions where the (4i+3)th row lines L3 and L7 and the odd-numbered column lines C1 and C3 intersect. The first-color subpixels are arranged at positions where the (4i+3)th row lines L3 and L7 and the even-numbered column lines C2 and C4 intersect.

[0037] Fourth-color subpixels and third-color subpixels are alternately arranged on the (4i+4)th row lines L4 and L8. The fourth-color subpixels are arranged at positions where the (4i+4)th row lines L4 and L8 and the odd-numbered column lines C1 and C3 intersect. The third-color subpixels are arranged at positions where the (4i+4)th row lines L4 and L8 and the even-numbered column lines C2 and C4 intersect.

[0038] The structure and driving method of the pixel array will be described in detail in conjunction with FIGS. 2 to 21G.

[0039] The lower substrate of the display panel 100 comprises data lines S 1 to Sm, gate lines G1 to Gn, TFTs (Thin-Film Transistors), pixel electrodes PXL connected to the TFTs, and storage capacitors Cst connected to the pixel electrodes PXL. Each pixel displays an image of video data by adjusting the amount of light transmission by using liquid crystal molecules, which are driven by a voltage difference between the pixel electrode PXL charged with a data voltage through the TFT and a common electrode COM to which a common voltage Vcom is applied.

[0040] A black matrix and a color filter array comprising color filters ae formed on the upper substrate of the display panel 100. The common electrode COM may be formed on the upper substrate in the case of vertical electric field-driven type, such as TN (Twisted Nematic) mode and VA (Vertical Alignment) mode, and may be formed on the lower substrate, along with the pixel electrodes, in the case of horizontal electric field-driven type, such as IPS (In-Plane Switching) mode and FFS (Fringe Field Switching) mode. Polarizers are attached to the upper and lower substrates of the display panel 100, respectively, and alignment films for setting a pre-tilt angle of liquid crystals are formed on them.

[0041] The liquid crystal display device of this invention may be implemented in any form, including a transmissive liquid crystal display, a semi-transmissive liquid crystal display, and a reflective liquid crystal display. The transmissive liquid crystal display and the semi-transmissive liquid crystal display require a backlight unit. The backlight unit may be implemented as a direct-type backlight unit or an edge-type backlight unit.

[0042] The display panel drive circuit writes data for an input image to the pixels. The display panel drive circuit comprises a data driver 102, a gate driver 104, a timing controller 20, etc.

[0043] The data driver 102 comprises at least one source drive IC. Data output channels of the source drive ICs are connected to the data lines S1 to Sm of the pixel array. The source drive ICs receive data for an input image from the timing controller 20. Digital video data transmitted to the source drive ICs comprises R data, G data, B data, and W data. The source drive ICs convert the data to positive/negative gamma compensation voltages under the control of the timing controller 20 and output positive/negative data voltages. The source drive ICs reverse the polarity of data voltages on a predetermined cycle under the control of the timing controller 20 and output the data voltages to the data lines S 1 to Sm. The predetermined cycle is 4 horizontal periods, for example, in the following embodiments, but the present invention is not limited to this.

[0044] The source drive ICs reverse the polarity of data voltages supplied through one data line, once for every 4 dots, in response to a polarity control signal POL from the timing controller 20. Here, a dot refers to a subpixel. The source drive ICs keep the same polarity for data voltages of four colors sequentially supplied through one data line, then reverse their polarity by 4-dot inversion, and then output data voltages of reversed polarity. Thus, the polarity reversal cycle for data voltages output from the source drive ICs is long, which leads to less data voltage transitions and lower power consumption. Consequently, the power consumption and heat generation of the source drive ICs can be reduced.

[0045] An R data voltage, a G data voltage, a B data voltage, and a W data voltage are supplied to RGBW subpixels through one data line. Accordingly, the liquid crystal display device of the present invention can reduce the number of data lines and the number of source drive ICs compared to the conventional art, even with the same resolution on the display panel.

[0046] Because of the correlation between the polarity reversal cycle of the source drive ICs and the pixel array structure, neighboring subpixels of the same color along the row line direction (x) and the column line direction (y) have opposite polarity. Since neighboring subpixels of the same color have opposite polarity, there is no polarity banding phenomenon between neighboring subpixels of the same color. Moreover, for subpixels of the same color, the sum of subpixels with positive polarity (+) is equal to the sum of subpixels with negative polarity (-). Thus, the sum of subpixels with positive polarity (+) and the sum of subpixels with negative polarity (-) may cancel each other out when added together, thereby attaining the balance of polarity without dominant polarity. As a result, the display device of this invention has no noise such as vertical lines since there is no polarity banding phenomenon in which neighboring subpixels of the same color have the same polarity, and no common voltage shift occurs because of the balance of polarity, thereby reproducing an input image with a picture quality that is crosstalk-free.

[0047] The gate driver 104 sequentially supplies gate pulses to the gate lines G1 to Gn under the control of the timing controller 20. The gate pulses output from the gate driver 104 are synchronized with positive/negative video data voltages

with which the pixels are charged. To reduce the IC cost, the gate driver 104 may be formed directly on the lower substrate of the display panel 100, along with the pixel array, in the manufacturing process.

[0048] Output channels of the gate driver 104 and the gate lines G1 to Gn of the pixel array are connected one to one through link lines. In the following embodiments, the output sequence of gate pulses may be different on some gate lines. In this case, some of the link lines that connect the output channels of the gate driver 104 to the gate lines may intersect so that gate pulses are supplied to the pixel array in a non-sequential manner, without changing the output channels of the gate driver 104. Thus, although the gate driver 104 outputs gate pulses sequentially, starting from the first output channel, the gate pulses may be applied non-sequentially to the gate lines 14 of the pixel array.

[0049] The timing controller 20 converts an input image's RGB data received from a host system 24 to RGBW data and transmits it to the data driver 102. A mini LVDS (low-voltage differential signaling) interface or an EPI (embedded panel interface) interface may be used as an interface for data transmission between the timing controller 20 and the source drive ICs of the data driver 102. The EPI interface may use the interface technologies which were proposed in Korean Patent Application No. 10-2008-0127458 (2008-12-15), U.S. Patent Application No. 12/543,996 (2009-08-19), Korean Patent Application No. 10-2008-0127456 (2008-12-15), U.S. Patent Application No. 12/461,652 (2009-08-19), Korean Patent Application No. 10-2008-0132466 (2008-12-23), and U.S. Patent Application No. 12/537,341 (2009-08-07) field by the applicant of this patent application.

[0050] The timing controller 20 receives timing signals synchronized with input image data from the host system 24. The timing signals include a vertical synchronization signal Vsync, a horizontal synchronization signal Hsync, a data enable signal DE, a dot clock DCLK, etc. The timing controller 20 controls the operation timings of the data driver 102 and gate driver 104 based on timing signals Vsync, Hsync, DE, and DCLK that are received along with pixel data for an input image. The timing controller 20 may transmit a polarity control signal POL for controlling the polarity of the pixel array to each of the source drive ICs of the data driver 102. The mini LVDS interface transmits the polarity control signal through a separate control line. The EPI interface is an interface technology that encodes polarity control information into a control data packet transmitted between a clock training pattern for CDR (Clock and Data Recovery) and an RGBW data packet, and that transmits the encoded polarity control information to each of the source drive ICs.

[0051] The timing controller 20 may convert RGB data for an input image to RGBW data by using a well-known gain calculation algorithm. Any well-known gain calculation algorithm may be used. For example, the white calculation algorithms proposed in Korean Patent Application No. 10-2005-0039728 (2005. 05. 12), Korean Patent Application No. 10-2005-0052906 (2005. 06. 20), Korean Patent Application No. 10-2005-0066429 (2007. 07. 21), and Korean Patent Application No. 10-2006-0011292 (2006. 02. 06) filed by the applicant of this patent application are applicable. Moreover, the timing controller 20 may execute a preset subpixel rendering algorithm to distribute a data value among neighboring pixels.

[0052] The host system 24 may be any one of the following: a television system, a set-top box, a navigation system, a DVD player, a personal computer (PC), a home theater system, and a phone system.

[0053] FIGS. 2 and 3 are views showing a pixel array structure and a data voltage charging sequence according to a first exemplary embodiment of the present invention. FIG. 4 is a waveform diagram showing output signals from source drive ICs and a gate driver for driving the pixel array of FIGS. 2 and 3. The pixel array on the display panel 100 has a repeating structure of 4*8 subpixels as in FIG. 3.

[0054] ①, ②, ③, and ④ in FIG. 2 represent a charging sequence of subpixels. In FIGS. 2 and 3, "L1~ L8" represent row lines on the display panel 100. Subpixels of two colors are arranged on each of the row lines along a horizontal direction (x-axis direction). "C1~C4" represent column lines on the display panel 100. Subpixels of four colors are arranged on each of the column lines along a vertical direction (y-axis direction). Rxy, Gxy, Bxy, and Wxy in FIG. 3 represent an R subpixel at an xy position, a G subpixel at an xy position, a B subpixel at an xy position, and a W subpixel at an xy position.

[0055] Referring to FIGS. 2 and 3, B subpixels B11, B12, B51, and B52 and R subpixels R11, R12, R51, and R52 are alternately arranged on the (4i+1)th row lines L1 and L5 (i is a positive integer). The B subpixels B11, B12, B51, and B52 are arranged at positions where the (4i+1)th row lines L1 and L5 and the odd-numbered column lines C1 and C3 intersect. The R subpixels R11, R12, R51, and R52 are arranged at positions where the (4i+1)th row lines L1 and L5 and the even-numbered column lines C2 and C4 intersect.

[0056] The subpixels of first and second colors B and R arranged on the (4i+1)th row lines L1 and L5 comprise TFTs arranged at the intersections of the data lines to the right and the (4i+1)th gate lines G1 and G5, respectively. Each TFT supplies a data voltage from the data line to the right of the subpixel to the pixel electrode. The TFT of the B11 subpixel is referred to as a first TFT, the TFT of the R11 subpixel as a second TFT, the TFT of the B12 subpixel as a third TFT, and the TFT of the R12 subpixel as a fourth TFT. The first TFT supplies a B data voltage from the second data line S2 to the pixel electrode PXL of the B11 subpixel, in response to a first gate pulse from the first gate line G1. The second TFT supplies an R data voltage from the third data line S3 to the pixel electrode PXL of the R11 subpixel, in response to the first gate pulse from the first gate line G1. The third TFT supplies a B data voltage from the fourth data line S4 to the pixel electrode PXL of the B12 subpixel, in response to the first gate pulse from the first gate line G1. The fourth TFT supplies an R data voltage from the fifth data line S5 to the pixel electrode PXL of the R12 subpixel, in response to the

first gate pulse from the first gate line G1.

[0057] W subpixels W21, W22, W61, and W62 and G subpixels G21, G22, G61, and G62 are alternately arranged on the (4i+2)th row lines L2 and L6. The W subpixels W21, W22, W61, and W62 are arranged at positions where the (4i+2)th row lines L2 and L6 and the odd-numbered column lines C1 and C3 intersect. The G subpixels G21, G22, G61, and G62 are arranged at positions where the (4i+2)th row lines L2 and L6 and the even-numbered column lines C2 and C4 intersect.

[0058] In the following description the term "first side" is referred to a "right side (=right)" of a subpixel arrangement and the term "second side" is referred to a "left side (=left)" of the same subpixel arrangement when considered its top/bottom view. The "right side (=first side)" is arranged on an opposite side of the "left side (second side)" of the same subpixel or the same subpixels or the same subpixel arrangement. The term "side" is referred to a "lateral side" of the subpixel that is located in parallel to "column lines" of signal lines on the display panel and that is located vertical to "row lines" in that display panel when considered its top/bottom view.

[0059] In the following description the term "column line" is referred to an orientation of a signal line, preferably a data line, in the display panel that is in parallel to the "first side" or the "second side". Respectively the term "row line" is referred to an orientation of another signal line, preferably a gate line, in the same display panel that is arranged vertical to the first side or the second side in that display panel.

[0060] The subpixels of third and fourth colors W and G arranged on the (4i+2)th row lines L2 and L6 comprise TFTs arranged at the intersections of the data lines to the left (second side) and the (4i+2)th gate lines G2 and G6, respectively. Each TFT supplies a data voltage from the data line to the left (second side) of the subpixel to the pixel electrode. The TFT of the W21 subpixel is referred to as a fifth TFT, the TFT of the G21 subpixel as a sixth TFT, the TFT of the W22 subpixel as a seventh TFT, and the TFT of the G22 subpixel as an eighth TFT. The fifth TFT supplies a W data voltage from the first data line S 1 to the pixel electrode PXL of the W21 subpixel, in response to a second gate pulse from the second gate line G2. The sixth TFT supplies a G data voltage from the second data line S2 to the pixel electrode PXL of the G21 subpixel, in response to the second gate pulse from the second gate line G2. The seventh TFT supplies a W data voltage from the third data line S3 to the pixel electrode PXL of the W22 subpixel, in response to the second gate pulse from the second gate line G2. The eighth TFT supplies a G data voltage from the fourth data line S4 to the pixel electrode PXL of the G22 subpixel, in response to the second gate pulse from the second gate line G2.

[0061] R subpixels R31, R32, R71, and R72 and B subpixels B31, B32, B71, and B72 are alternately arranged on the (4i+3)th row lines L3 and L7. The R subpixels R31, R32, R71, and R72 are arranged at positions where the (4i+3)th row lines L3 and L7 and the odd-numbered column lines C1 and C3 intersect. The B subpixels B31, B32, B71, and B72 are arranged at positions where the (4i+3)th row lines L3 and L7 and the even-numbered column lines C2 and C4 intersect.

[0062] The subpixels of the first and second colors B and R arranged on the (4i+3)th row lines L3 and L7 comprise TFTs arranged at the intersections of the data lines to the right (first side) and the (4i+3)th gate lines G3 and G7, respectively. Each TFT supplies a data voltage from the data line to the right (first side) of the subpixel to the pixel electrode. The TFT of the R31 subpixel is referred to as a ninth TFT, the TFT of the B31 subpixel as a tenth TFT, the TFT of the R32 subpixel as an eleventh TFT, and the TFT of the B32 subpixel as a twelfth TFT. The ninth TFT supplies an R data voltage from the second data line S2 to the pixel electrode PXL of the R31 subpixel, in response to a third gate pulse from the third gate line G3. The tenth TFT supplies a B data voltage from the third data line S3 to the pixel electrode PXL of the B31 subpixel, in response to the third gate pulse from the third gate line G3. The eleventh TFT supplies an R data voltage from the fourth data line S4 to the pixel electrode PXL of the R32 subpixel, in response to the third gate pulse from the third gate line G3. The twelfth TFT supplies a B data voltage from the fifth data line S5 to the pixel electrode PXL of the B32 subpixel, in response to the third gate pulse from the third gate line G3.

[0063] G subpixels G41, G42, G81, and G82 and W subpixels W41, W42, W81, and W82 are alternately arranged on the (4i+4)th row lines L4 and L8. The G subpixels G41, G42, G81, and G82 are arranged at positions where the (4i+4)th row lines L4 and L8 and the odd-numbered column lines C1 and C3 intersect. The W subpixels W41, W42, W81, and W82 are arranged at positions where the (4i+4)th row lines L4 and L8 and the even-numbered column lines C2 and C4 intersect.

[0064] The subpixels of the third and fourth colors W and G arranged on the (4i+4)th row lines L4 and L8 comprise TFTs arranged at the intersections of the data lines to the left (second side) and the (4i+4)th gate lines G4 and G8, respectively. Each TFT supplies a data voltage from the data line to the left (second side) of the subpixel to the pixel electrode. The TFT of the G41 subpixel is referred to as a thirteenth TFT, the TFT of the W41 subpixel as a fourteenth TFT, the TFT of the G42 subpixel as a fifteenth TFT, and the TFT of the W42 subpixel as a sixteenth TFT. The thirteenth TFT supplies a G data voltage from the first data line S1 to the pixel electrode PXL of the G41 subpixel, in response to a fourth gate pulse from the fourth gate line G4. The fourteenth TFT supplies a W data voltage from the second data line S2 to the pixel electrode PXL of the W41 subpixel, in response to the fourth gate pulse from the fourth gate line G4. The fifteenth TFT supplies a G data voltage from the third data line S3 to the pixel electrode PXL of the G42 subpixel, in response to the fourth gate pulse from the fourth gate line G4. The sixteenth TFT supplies a W data voltage from the fourth data line S4 to the pixel electrode PXL of the W42 subpixel, in response to the fourth gate pulse from the fourth

gate line G4.

[0065] In order to reverse the polarity of data voltages once for every 4 dots, the source drive ICs output data voltages of the four colors with first polarity during 4 horizontal periods 4H, in order: B data, G data, R data, and W data, and then output data voltages of the four colors with second polarity in the above order during the next 4 horizontal periods 4H. The polarity of the data voltages supplied to the data lines S1 to Sm is reversed on the B data voltages. Once the data voltage polarity is reversed on the B data voltages, data voltages of the same polarity are supplied to the data lines, in order: B data voltage, G data voltage, R data voltage, and W data voltage. The polarity of the data voltage may be reversed every frame by the source drive ICs.

[0066] As shown in FIG. 4, the timing controller 20 controls in such a way that there is a difference of 2 horizontal periods between the polarity reversal timing of data voltages supplied to the odd-numbered data lines S1, S3, and S5 and the polarity reversal timing of data voltages supplied to the even-numbered data lines S2 and S4, in order to keep the balance of polarity between subpixels of the same color on each row line and each column line.

[0067] Gate pulses output from the gate driver 104 are sequentially supplied to the gate lines G1 to G8. Link lines connecting output channels of the gate driver 104 and the gate lines G1 to G8 do not intersect. Thus, gate pulses are sequentially applied to the gate lines G1 to G8, starting from the first gate line G1.

[0068] In order to write data for an input image to the pixels of the pixel array shown in FIGS. 2 and 3, the polarity of data voltages is reversed on a cycle of every 4 horizontal periods by the source drive ICs, and gate pulses are sequentially applied to the gate lines G1 to Gn in order: G1, G2, ... G8.

[0069] FIGS. 5A to 6G show how data voltage transitions occur when a test pattern of various colors is displayed on the pixel array according to the first exemplary embodiment of the present invention. It is assumed that the white-level voltage (or highest voltage) for data voltages before polarity reversal is 1 V. In this case, the data voltages begin their transition from 1 V. Here, a data voltage transition means that a large amount of electric current is generated when a data voltage output from the source drive ICs changes, causing the source drive IC to consume current and generate heat. When a polarity reversal occurs in a way that the white-level voltage changes its polarity from first polarity to second polarity, a data voltage transition occurs with a voltage swing of 2 V.

[0070] FIGS. 5A to 5G are views showing which subpixels are lit up and their polarity, when white, red, green, blue, yellow, cyan, and magenta patterns are displayed on the pixel array according to the first exemplary embodiment of the present invention. FIGS. 6A to 6G are views showing data voltages when the colors of FIGS. 5A to 5G are displayed on the pixel array. The arrows in FIGS. 6A to 6G indicate data voltage transitions.

[0071] Referring to FIGS. 5A and 6A, when a white pattern is displayed on the pixels of the pixel array, the R subpixels, G subpixels, B subpixels, and W subpixels are all lit up at the white level. In the white pattern, the RGBW data voltages are the white-level voltage. For the white pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 3 change twice with a voltage swing of 2 V during 8 horizontal periods 8H. At these data voltages, the temperature of heat generated from the source drive ICs is 246 °C, as seen from Table 1.

[0072] Referring to FIGS. 5B and 6B, when a red pattern is displayed on the pixels of the pixel array, only the R subpixels are lit up at the white level. In the red pattern, the R data voltage is the white-level voltage (or highest voltage), and the data voltages of the other colors are the black-level voltage (or lowest voltage). For the red pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 3 change twice with a voltage swing of 1 V during 8 horizontal periods 8H. At these data voltages, the temperature of heat generated from the source drive ICs is 201 °C, as seen from Table 1.

[0073] Referring to FIGS. 5C and 6C, when a green pattern is displayed on the pixels of the pixel array, only the G subpixels are lit up at the white level. In the green pattern, the G data voltage is the white-level voltage (or highest voltage), and the data voltages of the other colors are the black-level voltage (or lowest voltage). For the green pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 3 change twice with a voltage swing of 1 V during 8 horizontal periods 8H. At these data voltages, the temperature of heat generated from the source drive ICs is 201 °C, as seen from Table 1.

[0074] Referring to FIGS. 5D and 6D, when a blue pattern is displayed on the pixels of the pixel array, only the B subpixels are lit up at the white level. In the blue pattern, the B data voltage is the white-level voltage (or highest voltage), and the data voltages of the other colors are the black-level voltage (or lowest voltage). For the blue pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 3 change twice with a voltage swing of 1 V during 8 horizontal periods 8H. At these data voltages, the temperature of heat generated from the source drive ICs is 201 °C, as seen from Table 1.

[0075] Referring to FIGS. 5E and 6E, when a yellow pattern is displayed on the pixels of the pixel array, the G subpixels and the R subpixels are lit up at the white level. In the yellow pattern, the G data voltage and the R data voltage are the white-level voltage (or highest voltage), and the data voltages of the other colors are the black-level voltage (or lowest voltage). For the yellow pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 3 change twice with a voltage swing of 1 V during 8 horizontal periods 8H. At these data voltages, the temperature of heat generated from the source drive ICs is 201 °C, as seen from Table 1.

[0076] Referring to FIGS. 5F and 6F, when a cyan pattern is displayed on the pixels of the pixel array, the G subpixels and the B subpixels are lit up at the white level. In the cyan pattern, the G data voltage and the B data voltage are the white-level voltage, and the data voltages of the other colors are the black-level voltage. For the cyan pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 3 change twice with a voltage swing of 1 V during 8 horizontal periods 8H. At these data voltages, the temperature of heat generated from the source drive ICs is 201 °C, as seen from Table 1.

[0077] Referring to FIGS. 5G and 6G, when a magenta pattern is displayed on the pixels of the pixel array, the B subpixels and the R subpixels are lit up at the white level. In the magenta pattern, the B data voltage and the R data voltage are the white-level voltage (or highest voltage), and the data voltages of the other colors are the black-level voltage (or lowest voltage). For the magenta pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 3 change four times with a voltage swing of 1 V during 8 horizontal periods 8H. At these data voltages, the temperature of heat generated from the source drive ICs is 355 °C, as seen from Table 1.

[0078] In the first exemplary embodiment (FIGS. 2 to 4) of the present invention, the balance of polarity may be attained for each color without polarity banding phenomenon, and therefore input images may be reproduced with high picture quality. In the first exemplary embodiment (FIGS. 2 to 4) of the present invention, the power consumption and heat generation of the source drive ICs may be kept at moderate levels for every color except for magenta.

[0079] FIGS. 7 and 8 are views showing a pixel array structure and a data voltage charging sequence according to a second exemplary embodiment of the present invention. FIG. 9 is a waveform diagram showing output signals from source drive ICs and a gate driver for driving the pixel array of FIGS. 7 and 8. The pixel array on the display panel 100 has a repeating structure of 4*8 subpixels as in FIG. 8.

[0080] Referring to FIGS. 7 and 8, W subpixels W11, W12, W51, and W52 and G subpixels G11, G12, G51, and G52 are alternately arranged on the (4i+1)th row lines L1 and L5. The W subpixels W11, W12, W51, and W52 are arranged at positions where the (4i+1)th row lines L1 and L5 and the odd-numbered column lines C1 and C3 intersect. The G subpixels G11, G12, G51, and G52 are arranged at positions where the (4i+1)th row lines L1 and L5 and the even-numbered column lines C2 and C4 intersect.

[0081] The subpixels of first and second colors W and G arranged on the (4i+1)th row lines L1 and L5 comprise TFTs arranged at the intersections of the data lines to the right (first side) and the (4i+1)th gate lines G1 and G5, respectively. Each TFT supplies a data voltage from the data line to the right (first side) of the subpixel to the pixel electrode. The TFT of the W11 subpixel is referred to as a first TFT, the TFT of the G11 subpixel as a second TFT, the TFT of the W12 subpixel as a third TFT, and the TFT of the G12 subpixel as a fourth TFT. The first TFT supplies a W data voltage from the second data line S2 to the pixel electrode PXL of the W11 subpixel, in response to a first gate pulse from the first gate line G1. The second TFT supplies a G data voltage from the third data line S3 to the pixel electrode PXL of the G11 subpixel, in response to the first gate pulse from the first gate line G1. The third TFT supplies a W data voltage from the fourth data line S4 to the pixel electrode PXL of the W12 subpixel, in response to the first gate pulse from the first gate line G1. The fourth TFT supplies a G data voltage from the fifth data line S5 to the pixel electrode PXL of the G12 subpixel, in response to the first gate pulse from the first gate line G1.

[0082] R subpixels R21, R22, R61, and R62 and B subpixels B21, B22, B61, and B62 are alternately arranged on the (4i+2)th row lines L2 and L6. The R subpixels R21, R22, R61, and R62 are arranged at positions where the (4i+2)th row lines L2 and L6 and the odd-numbered column lines C1 and C3 intersect. The B subpixels B21, B22, B61, and B62 are arranged at positions where the (4i+2)th row lines L2 and L6 and the even-numbered column lines C2 and C4 intersect.

[0083] The subpixels of third and fourth colors R and B arranged on the (4i+2)th row lines L2 and L6 comprise TFTs arranged at the intersections of the data lines to the right (first side) and the (4i+2)th gate lines G2 and G6, respectively. Each TFT supplies a data voltage from the data line to the right (first side) of the subpixel to the pixel electrode. The TFT of the R21 subpixel is referred to as a fifth TFT, the TFT of the B21 subpixel as a sixth TFT, the TFT of the R22 subpixel as a seventh TFT, and the TFT of the B22 subpixel as an eighth TFT. The fifth TFT supplies an R data voltage from the second data line S2 to the pixel electrode PXL of the R21 subpixel, in response to a third gate pulse from the second gate line G2. The sixth TFT supplies a B data voltage from the third data line S3 to the pixel electrode PXL of the B21 subpixel, in response to the third gate pulse from the second gate line G2. The seventh TFT supplies an R data voltage from the fourth data line S4 to the pixel electrode PXL of the R22 subpixel, in response to the third gate pulse from the second gate line G2. The eighth TFT supplies a B data voltage from the fifth data line S5 to the pixel electrode PXL of the B22 subpixel, in response to the third gate pulse from the second gate line G2.

[0084] G subpixels G31, G32, G71, and G72 and W subpixels W31, W32, W71, and W72 are alternately arranged on the (4i+3)th row lines L3 and L7. The G subpixels G31, G32, G71, and G72 are arranged at positions where the (4i+3)th row lines L3 and L7 and the odd-numbered column lines C1 and C3 intersect. The W subpixels W31, W32, W71, and W72 are arranged at positions where the (4i+3)th row lines L3 and L7 and the even-numbered column lines C2 and C4 intersect.

[0085] The subpixels of the first and second colors W and G arranged on the (4i+3)th row lines L3 and L7 comprise TFTs arranged at the intersections of the data lines to the left (second side) and the (4i+3)th gate lines G3 and G7,

respectively. Each TFT supplies a data voltage from the data line to the left (second side) of the subpixel to the pixel electrode. The TFT of the G31 subpixel is referred to as a ninth TFT, the TFT of the W31 subpixel as a tenth TFT, the TFT of the G32 subpixel as an eleventh TFT, and the TFT of the W32 subpixel as a twelfth TFT. The ninth TFT supplies a G data voltage from the first data line S1 to the pixel electrode PXL of the G31 subpixel, in response to a second gate pulse from the third gate line G3. The tenth TFT supplies a W data voltage from the second data line S2 to the pixel electrode PXL of the W31 subpixel, in response to the second gate pulse from the third gate line G3. The eleventh TFT supplies a G data voltage from the third data line S3 to the pixel electrode PXL of the G32 subpixel, in response to the second gate pulse from the third gate line G3. The twelfth TFT supplies a W data voltage from the fourth data line S4 to the pixel electrode PXL of the W32 subpixel, in response to the second gate pulse from the third gate line G3.

[0086] B subpixels B41, B42, B81, and B82 and R subpixels R41, R42, R81, and R82 are alternately arranged on the (4i+4)th row lines L4 and L8. The B subpixels B41, B42, B81, and B82 are arranged at positions where the (4i+4)th row lines L4 and L8 and the odd-numbered column lines C1 and C3 intersect. The R subpixels R41, R42, R81, and R82 are arranged at positions where the (4i+4)th row lines L4 and L8 and the even-numbered column lines C2 and C4 intersect.

[0087] The subpixels of the third and fourth colors R and B arranged on the (4i+2)th row lines L4 and L8 comprise TFTs arranged at the intersections of the data lines to the left (second side) and the (4i+4)th gate lines G4 and G8, respectively. Each TFT supplies a data voltage from the data line to the left (second side) of the subpixel to the pixel electrode. The TFT of the B41 subpixel is referred to as a thirteenth TFT, the TFT of the R41 subpixel as a fourteenth TFT, the TFT of the B42 subpixel as a fifteenth TFT, and the TFT of the R42 subpixel as a sixteenth TFT. The thirteenth TFT supplies a B data voltage from the first data line S1 to the pixel electrode PXL of the B41 subpixel, in response to a fourth gate pulse from the fourth gate line G4. The fourteenth TFT supplies an R data voltage from the second data line S2 to the pixel electrode PXL of the R41 subpixel, in response to the fourth gate pulse from the fourth gate line G4. The fifteenth TFT supplies a B data voltage from the third data line S3 to the pixel electrode PXL of the B42 subpixel, in response to the fourth gate pulse from the fourth gate line G4. The sixteenth TFT supplies an R data voltage from the fourth data line S4 to the pixel electrode PXL of the R42 subpixel, in response to the fourth gate pulse from the fourth gate line G4.

[0088] In order to reverse the polarity of data voltages once for every 4 dots, the source drive ICs output data voltages with first polarity during 4 horizontal periods 4H, and then output data voltages with second polarity during the next 4 horizontal periods 4H.

[0089] The data voltages supplied to the odd-numbered data lines S1, S3, and S5 are output from the source drive ICs during 4 horizontal periods 4H, in order: first data voltage of the fourth color B, second data voltage of the fourth color B, first data voltage of the second color G, and second data voltage of the second color G, and then their polarity is reversed. The first and second data voltages of the fourth color B are sequentially supplied to the B subpixels B21 and B42. The first and second data voltages of the second color G are sequentially supplied to the G subpixels G51 and G72. The polarity of the data voltages supplied to the odd-numbered data lines S1, S3, and S5 is reversed on the data voltages of the fourth color B.

[0090] The data voltages supplied to the even-numbered data lines S2 and S4 are output from the source drive ICs during 4 horizontal periods 4H, in order: first data voltage of the third color R, second data voltage of the third color R, first data voltage of the first color W, and second data voltage of the first color W, and then their polarity is reversed. The first and second data voltages of the third color R are sequentially supplied to the R subpixels R21 and R41. The first and second data voltages of the first color W are sequentially supplied to the W subpixels W51 and W71. The polarity of the data voltages supplied to the even-numbered data lines S2 and S4 is reversed on the data voltages of the third color R.

[0091] As shown in FIG. 8 and 9, the source drive ICs simultaneously reverse the polarity of the data voltages supplied to the odd-numbered data lines S1, S3, and S5 and the polarity of the data voltages supplied to the even-numbered data lines S2 and S4, under the control of the timing controller 20.

[0092] Link lines LNK connecting (4i+2)th and (4i+3)th output channels 2 and 3 of the gate driver 104 and the (4i+2)th and (4i+3)th gate lines G2, G3, G6, and G7 intersect, with an insulating layer in between. Due to this, as shown in FIG. 9, although the gate driver 104 outputs a third gate pulse through the third output channel 3 after outputting a second gate pulse through the second output channel 2, the third gate pulse is applied to the second gate line G2 after the second gate pulse is applied to the third gate line G3. Accordingly, gate pulses are applied to the gate lines G1 to G8 in order: G1, G3, G2, G4, G5, G7, G6, and G8.

[0093] FIGS. 10A to 11G show how data voltage transitions occur when a test pattern of various colors is displayed on the pixel array according to the second exemplary embodiment of the present invention.

[0094] FIGS. 10A to 10G are views showing which subpixels are lit up and their polarity, when white, red, green, blue, yellow, cyan, and magenta patterns are displayed on the pixel array according to the second exemplary embodiment of the present invention. FIGS. 11A to 11G are views showing data voltages when the colors of FIGS. 10A to 10G are displayed on the pixel array. The arrows in FIGS. 11A to 11G indicate data voltage transitions.

[0095] Referring to FIGS. 10A and 11A, when a white pattern is displayed on the pixels of the pixel array, the R

subpixels, G subpixels, B subpixels, and W subpixels are all lit up at the white level. In the white pattern, the RGBW data voltages are the white-level voltage. For the white pattern to be displayed on the pixel array, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 8 change twice with a voltage swing of 2 V during 8 horizontal periods 8H. At these data voltages, the temperature of heat generated from the source drive ICs is 246 °C, as seen from Table 1.

[0096] Referring to FIGS. 10B and 11B, when a red pattern is displayed on the pixels of the pixel array, only the R subpixels are lit up at the white level. In the red pattern, the R data voltage is the white-level voltage, and the data voltages of the other colors are the black-level voltage. For the red pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 8 change once with a voltage swing of 1 V during 8 horizontal periods 8H. Since the data voltages applied to the odd-numbered data lines S1, S3, and S5 undergo no transition to the white-level voltage, the average number of transitions in data voltage applied to the data lines S1 to S5 during the 8 horizontal periods is 1. At these data voltages, the temperature of heat generated from the source drive ICs is 150 °C, as seen from Table 1.

[0097] Referring to FIGS. 10C and 11C, when a green pattern is displayed on the pixels of the pixel array, only the G subpixels are lit up at the white level. In the green pattern, the G data voltage is the white-level voltage, and the data voltages of the other colors are the black-level voltage. For the green pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 8 change twice with a voltage swing of 1 V during 8 horizontal periods 8H. Since the data voltages applied to the even-numbered data lines S2 and S4 undergo no transition to the white-level voltage while the data voltages applied to the odd-numbered data lines S1, S3, and S5 undergo four transitions, the average number of transitions in data voltage applied to the data lines S 1 to S5 during the 8 horizontal periods is 2. At these data voltages, the temperature of heat generated from the source drive ICs is 201 °C, as seen from Table 1.

[0098] Referring to FIGS. 10D and 11D, when a blue pattern is displayed on the pixels of the pixel array, only the B subpixels are lit up at the white level. In the blue pattern, the B data voltage is the white-level voltage (or highest voltage), and the data voltages of the other colors are the black-level voltage (or lowest voltage). For the blue pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 8 change once with a voltage swing of 1 V during 8 horizontal periods 8H. Since the data voltages applied to the even-numbered data lines S2 and S4 undergo no transition to the white-level voltage, the average number of transitions in data voltage applied to the data lines S1 to S5 during the 8 horizontal periods is 1. At these data voltages, the temperature of heat generated from the source drive ICs is 142 °C, as seen from Table 1.

[0099] Referring to FIGS. 10E and 11E, when a yellow pattern is displayed on the pixels of the pixel array, the G subpixels and the R subpixels are lit up at the white level. In the yellow pattern, the G data voltage and the R data voltage are the white-level voltage, and the data voltages of the other colors are the black-level voltage. For the yellow pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 8 change three times with a voltage swing of 1 V during 8 horizontal periods 8H. Since the data voltages applied to the odd-numbered data lines S1, S3, and S5 undergo four transitions while the data voltages applied to the even-numbered data lines S2 and S4 undergo two transitions, the average number of transitions in data voltage applied to the data lines S1 to S5 during the 8 horizontal periods is 3. At these data voltages, the temperature of heat generated from the source drive ICs is 222 °C, as seen from Table 1.

[0100] Referring to FIGS. 10F and 11F, when a cyan pattern is displayed on the pixels of the pixel array, the G subpixels and the B subpixels are lit up at the white level. In the cyan pattern, the G data voltage and the B data voltage are the white-level voltage, and the data voltages of the other colors are the black-level voltage. For the cyan pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 8 change once with a voltage swing of 1 V during 8 horizontal periods 8H. Since the data voltages applied to the even-numbered data lines S2 and S4 undergo no transition to the white-level voltage, the average number of transitions in data voltage applied to the data lines S1 to S5 during the 8 horizontal periods is 1. At these data voltages, the temperature of heat generated from the source drive ICs is 150 °C, as seen from Table 1.

[0101] Referring to FIGS. 10G and 11G, when a magenta pattern is displayed on the pixels of the pixel array, the B subpixels and the R subpixels are lit up at the white level. In the magenta pattern, the B data voltage and the R data voltage are the white-level voltage, and the data voltages of the other colors are the black-level voltage. For the magenta pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 8 change twice with a voltage swing of 1 V during 8 horizontal periods 8H. At these data voltages, the temperature of heat generated from the source drive ICs is 201 °C, as seen from Table 1.

[0102] In the second exemplary embodiment (FIGS. 7 to 9) of the present invention, the balance of polarity may be attained for each color without polarity banding phenomenon, and therefore input images may be reproduced with high picture quality. However, the data voltages supplied to the data lines are applied simultaneously and hence the amount of charge in the pixels varies with each row line, which may create horizontal lines visible along the row line direction. In the second exemplary embodiment (FIGS. 7 to 9) of the present invention, the power consumption and heat generation of the source drive ICs may be reduced for every color.

[0103] FIGS. 12 and 13 are views showing a pixel array structure and a data voltage charging sequence according

to a third exemplary embodiment of the present invention. FIG. 14 is a waveform diagram showing output signals from source drive ICs and a gate driver for driving the pixel array of FIGS. 12 and 13. The pixel array on the display panel 100 has a repeating structure of 4*8 subpixels as in FIG. 13.

[0104] Referring to FIGS. 12 and 13, W subpixels W11, W12, W51, and W52 and G subpixels G11, G12, G51, and G52 are alternately arranged on the (4i+1)th row lines L1 and L5. The W subpixels W11, W12, W51, and W52 are arranged at positions where the (4i+1)th row lines L1 and L5 and the odd-numbered column lines C1 and C3 intersect. The G subpixels G11, G12, G51, and G52 are arranged at positions where the (4i+1)th row lines L1 and L5 and the even-numbered column lines C2 and C4 intersect.

[0105] The subpixels of first and second colors W and G arranged on the (4i+1)th row lines L1 and L5 comprise TFTs arranged at the intersections of the data lines to the right (first side) and the (4i+1)th gate lines G1 and G5, respectively. Each TFT supplies a data voltage from the data line to the right (first side) of the subpixel to the pixel electrode. The TFT of the W11 subpixel is referred to as a first TFT, the TFT of the G11 subpixel as a second TFT, the TFT of the W12 subpixel as a third TFT, and the TFT of the G12 subpixel as a fourth TFT. The first TFT supplies a W data voltage from the second data line S2 to the pixel electrode PXL of the W11 subpixel, in response to a first gate pulse from the first gate line G1. The second TFT supplies a G data voltage from the third data line S3 to the pixel electrode PXL of the G11 subpixel, in response to the first gate pulse from the first gate line G1. The third TFT supplies a W data voltage from the fourth data line S4 to the pixel electrode PXL of the W12 subpixel, in response to the first gate pulse from the first gate line G1. The fourth TFT supplies a G data voltage from the fifth data line S5 to the pixel electrode PXL of the G12 subpixel, in response to the first gate pulse from the first gate line G1.

[0106] R subpixels R21, R22, R61, and R62 and B subpixels B21, B22, B61, and B62 are alternately arranged on the (4i+2)th row lines L2 and L6. The R subpixels R21, R22, R61, and R62 are arranged at positions where the (4i+2)th row lines L2 and L6 and the odd-numbered column lines C1 and C3 intersect. The B subpixels B21, B22, B61, and B62 are arranged at positions where the (4i+2)th row lines L2 and L6 and the even-numbered column lines C2 and C4 intersect.

[0107] The subpixels of third and fourth colors R and B arranged on the (4i+2)th row lines L2 and L6 comprise TFTs arranged at the intersections of the data lines to the right and the (4i+2)th gate lines G2 and G6, respectively. Each TFT supplies a data voltage from the data line to the right of the subpixel to the pixel electrode. The TFT of the R21 subpixel is referred to as a fifth TFT, the TFT of the B21 subpixel as a sixth TFT, the TFT of the R22 subpixel as a seventh TFT, and the TFT of the B22 subpixel as an eighth TFT.

[0108] The fifth TFT supplies an R data voltage from the second data line S2 to the pixel electrode PXL of the R21 subpixel, in response to a third gate pulse from the second gate line G2. The sixth TFT supplies a B data voltage from the third data line S3 to the pixel electrode PXL of the B21 subpixel, in response to the third gate pulse from the second gate line G2. The seventh TFT supplies an R data voltage from the fourth data line S4 to the pixel electrode PXL of the R22 subpixel, in response to the third gate pulse from the second gate line G2. The eighth TFT supplies a B data voltage from the fifth data line S5 to the pixel electrode PXL of the B22 subpixel, in response to the third gate pulse from the second gate line G2.

[0109] G subpixels G31, G32, G71, and G72 and W subpixels W31, W32, W71, and W72 are alternately arranged on the (4i+3)th row lines L3 and L7. The G subpixels G31, G32, G71, and G72 are arranged at positions where the (4i+3)th row lines L3 and L7 and the odd-numbered column lines C1 and C3 intersect. The W subpixels W31, W32, W71, and W72 are arranged at positions where the (4i+3)th row lines L3 and L7 and the even-numbered column lines C2 and C4 intersect.

[0110] The subpixels of the first and second colors W and G arranged on the (4i+3)th row lines L3 and L7 comprise TFTs arranged at the intersections of the data lines to the right (first side) and the (4i+3)th gate lines G3 and G7, respectively. Each TFT supplies a data voltage from the data line to the right (first side) of the subpixel to the pixel electrode. The TFT of the G31 subpixel is referred to as a ninth TFT, the TFT of the W31 subpixel as a tenth TFT, the TFT of the G32 subpixel as an eleventh TFT, and the TFT of the W32 subpixel as a twelfth TFT. The ninth TFT supplies a G data voltage from the second data line S2 to the pixel electrode PXL of the G31 subpixel, in response to a second gate pulse from the third gate line G3. The tenth TFT supplies a W data voltage from the third data line S3 to the pixel electrode PXL of the W31 subpixel, in response to the second gate pulse from the third gate line G3. The eleventh TFT supplies a G data voltage from the fourth data line S4 to the pixel electrode PXL of the G32 subpixel, in response to the second gate pulse from the third gate line G3. The twelfth TFT supplies a W data voltage from the fifth data line S5 to the pixel electrode PXL of the W32 subpixel, in response to the second gate pulse from the third gate line G3.

[0111] B subpixels B41, B42, B81, and B82 and R subpixels R41, R42, R81, and R82 are alternately arranged on the (4i+4)th row lines L4 and L8. The B subpixels B41, B42, B81, and B82 are arranged at positions where the (4i+4)th row lines L4 and L8 and the odd-numbered column lines C1 and C3 intersect. The R subpixels R41, R42, R81, and R82 are arranged at positions where the (4i+4)th row lines L4 and L8 and the even-numbered column lines C2 and C4 intersect.

[0112] The subpixels of the third and fourth colors R and B arranged on the (4i+4)th row lines L4 and L8 comprise TFTs arranged at the intersections of the data lines to the left (second side) and the (4i+4)th gate lines G4 and G8, respectively. Each TFT supplies a data voltage from the data line to the left (second side) of the subpixel to the pixel

electrode. The TFT of the B41 subpixel is referred to as a thirteenth TFT, the TFT of the R41 subpixel as a fourteenth TFT, the TFT of the B42 subpixel as a fifteenth TFT, and the TFT of the R42 subpixel as a sixteenth TFT. The thirteenth TFT supplies a B data voltage from the first data line S1 to the pixel electrode PXL of the B41 subpixel, in response to a fourth gate pulse from the fourth gate line G4. The fourteenth TFT supplies an R data voltage from the second data line S2 to the pixel electrode PXL of the R41 subpixel, in response to the fourth gate pulse from the fourth gate line G4. The fifteenth TFT supplies a B data voltage from the third data line S3 to the pixel electrode PXL of the B42 subpixel, in response to the fourth gate pulse from the fourth gate line G4. The sixteenth TFT supplies an R data voltage from the fourth data line S4 to the pixel electrode PXL of the R42 subpixel, in response to the fourth gate pulse from the fourth gate line G4.

[0113] In order to reverse the polarity of data voltages once for every 4 dots, the source drive ICs output data voltages with first polarity during 4 horizontal periods 4H, and then output data voltages with second polarity during the next 4 horizontal periods 4H.

[0114] The data voltages supplied to the odd-numbered data lines S1, S3, and S5 are output from the source drive ICs during 4 horizontal periods 4H, in order: data voltage of the second color G, data voltage of the first color W, data voltage of the fourth color B, and data voltage of the fourth color B, and then their polarity is reversed. The polarity of the data voltages supplied to the odd-numbered data lines S1, S3, and S5 is reversed on the data voltages of the fourth color B.

[0115] The data voltages supplied to the even-numbered data lines S2 and S4 are output from the source drive ICs during 4 horizontal periods 4H, in order: data voltage of the first color W, data voltage of the second color G, data voltage of the third color R, and data voltage of the third color R, and then their polarity is reversed. The polarity of the data voltages supplied to the even-numbered data lines S2 and S4 is reversed on the data voltages of the second color G. Among the data voltages supplied to the data lines S1 to Sm, the fourth data voltage after polarity change - that is, the data voltage immediately before polarity reversal - is a data voltage of the first color W.

[0116] As shown in FIG. 14, the timing controller 20 controls in such a way that there is a difference of 1 horizontal period 1H between the polarity reversal timing of data voltages supplied to the odd-numbered data lines S1, S3, and S5 and the polarity reversal timing of data voltages supplied to the even-numbered data lines S2 and S4.

[0117] Link lines LNK connecting (4i+2)th and (4i+3)th output channels 2 and 3 of the gate driver 104 and the (4i+2)th and (4i+3)th gate lines G2, G3, G6, and G7 intersect, with an insulating layer in between. Due to this, as shown in FIG. 14, although the gate driver 104 outputs a third gate pulse through the third output channel 3 after outputting a second gate pulse through the second output channel 2, the third gate pulse is applied to the second gate line G2 after the second gate pulse is applied to the third gate line G3. Accordingly, gate pulses are applied to the gate lines G1 to G8 in order: G1, G3, G2, G4, G5, G7, G6, and G8.

[0118] FIGS. 15A to 16G show how data voltage transitions occur when a test pattern of various colors is displayed on the pixel array according to the third exemplary embodiment of the present invention.

[0119] FIGS. 15A to 15G are views showing which subpixels are lit up and their polarity, when white, red, green, blue, yellow, cyan, and magenta patterns are displayed on the pixel array according to the third exemplary embodiment of the present invention. FIGS. 16A to 16G are views showing data voltages when the colors of FIGS. 15A to 15G are displayed on the pixel array. The arrows in FIGS. 16A to 16G indicate data voltage transitions.

[0120] Referring to FIGS. 15A and 16A, when a white pattern is displayed on the pixels of the pixel array, the R subpixels, G subpixels, B subpixels, and W subpixels are all lit up at the white level. In the white pattern, the RGBW data voltages are the white-level voltage. For the white pattern to be displayed on the pixel array, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 13 change twice with a voltage swing of 2 V during 8 horizontal periods 8H. At these data voltages, the temperature of heat generated from the source drive ICs is 246 °C, as seen from Table 1.

[0121] Referring to FIGS. 15B and 16B, when a red pattern is displayed on the pixels of the pixel array, only the R subpixels are lit up at the white level. In the red pattern, the R data voltage is the white-level voltage, and the data voltages of the other colors are the black-level voltage. For the red pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 13 change once with a voltage swing of 1 V during 8 horizontal periods 8H. Since the data voltages applied to the odd-numbered data lines S1, S3, and S5 undergo no transition to the white-level voltage, the average number of transitions in data voltage applied to the data lines S1 to S5 during the 8 horizontal periods is 1. At these data voltages, the temperature of heat generated from the source drive ICs is 150 °C, as seen from Table 1.

[0122] Referring to FIGS. 15C and 16C, when a green pattern is displayed on the pixels of the pixel array, only the G subpixels are lit up at the white level. In the green pattern, the G data voltage is the white-level voltage, and the data voltages of the other colors are the black-level voltage. For the green pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 13 change twice with a voltage swing of 1 V during 8 horizontal periods 8H. At these data voltages, the temperature of heat generated from the source drive ICs is 201 °C, as seen from Table 1.

[0123] Referring to FIGS. 15D and 16D, when a blue pattern is displayed on the pixels of the pixel array, only the B subpixels are lit up at the white level. In the blue pattern, the B data voltage is the white-level voltage, and the data

voltages of the other colors are the black-level voltage. For the blue pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 13 change once with a voltage swing of 1 V during 8 horizontal periods 8H. Since the data voltages applied to the even-numbered data lines S2 and S4 undergo no transition to the white-level voltage, the average number of transitions in data voltage applied to the data lines S1 to S5 during the 8 horizontal periods is 1. At these data voltages, the temperature of heat generated from the source drive ICs is 142 °C, as seen from Table 1.

[0124] Referring to FIGS. 15E and 16E, when a yellow pattern is displayed on the pixels of the pixel array, the G subpixels and the R subpixels are lit up at the white level. In the yellow pattern, the G data voltage and the R data voltage are the white-level voltage, and the data voltages of the other colors are the black-level voltage. For the yellow pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 13 change twice with a voltage swing of 1 V during 8 horizontal periods 8H. At these data voltages, the temperature of heat generated from the source drive ICs is 203 °C, as seen from Table 1.

[0125] Referring to FIGS. 15F and 16F, when a cyan pattern is displayed on the pixels of the pixel array, the G subpixels and the B subpixels are lit up at the white level. In the cyan pattern, the G data voltage and the B data voltage are the white-level voltage, and the data voltages of the other colors are the black-level voltage. For the cyan pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 13 change twice with a voltage swing of 1 V during 8 horizontal periods 8H. At these data voltages, the temperature of heat generated from the source drive ICs is 194 °C, as seen from Table 1.

[0126] Referring to FIGS. 15G and 16G, when a magenta pattern is displayed on the pixels of the pixel array, the B subpixels and the R subpixels are lit up at the white level. In the magenta pattern, the B data voltage and the R data voltage are the white-level voltage, and the data voltages of the other colors are the black-level voltage. For the magenta pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 13 change twice with a voltage swing of 1 V during 8 horizontal periods 8H. At these data voltages, the temperature of heat generated from the source drive ICs is 202 °C, as seen from Table 1.

[0127] As can be seen from above, in the third exemplary embodiment (FIGS. 12 to 14) of the present invention, the balance of polarity may be attained for each color without polarity banding phenomenon, and therefore input images may be reproduced with high picture quality. In the third exemplary embodiment (FIGS. 12 to 14) of the present invention, the power consumption and heat generation of the source drive ICs may be reduced for every color.

[0128] FIGS. 17 and 18 are views showing a pixel array structure and a data voltage charging sequence according to a fourth exemplary embodiment of the present invention. FIG. 19 is a waveform diagram showing output signals from source drive ICs and a gate driver for driving the pixel array of FIGS. 17 and 18. The pixel array on the display panel 100 has a repeating structure of 4*8 subpixels as in FIG. 18. In FIGS. 17 and 18, the B and R above the first row line L1 indicate dummy subpixels that are charged with dummy data voltages prior to charging the first row line L1.

[0129] Referring to FIGS. 17 and 18, W subpixels W11, W12, W51, and W52 and G subpixels G11, G12, G51, and G52 are alternately arranged on the (4i+1)th row lines L1 and L5. The W subpixels W11, W12, W51, and W52 are arranged at positions where the (4i+1)th row lines L1 and L5 and the odd-numbered column lines C1 and C3 intersect. The G subpixels G11, G12, G51, and G52 are arranged at positions where the (4i+1)th row lines L1 and L5 and the even-numbered column lines C2 and C4 intersect.

[0130] The subpixels of first and second colors W and G arranged on the (4i+1)th row lines L1 and L5 comprise TFTs arranged at the intersections of the data lines to the left (second side) and the (4i+1)th gate lines G1 and G5, respectively. Each TFT supplies a data voltage from the data line to the left (second side) of the subpixel to the pixel electrode. The TFT of the W11 subpixel is referred to as a first TFT, the TFT of the G11 subpixel as a second TFT, the TFT of the W12 subpixel as a third TFT, and the TFT of the G12 subpixel as a fourth TFT. The first TFT supplies a W data voltage from the first data line S1 to the pixel electrode PXL of the W11 subpixel, in response to a first gate pulse from the first gate line G1. The second TFT supplies a G data voltage from the second data line S2 to the pixel electrode PXL of the G11 subpixel, in response to the first gate pulse from the first gate line G1. The third TFT supplies a W data voltage from the third data line S3 to the pixel electrode PXL of the W12 subpixel, in response to the first gate pulse from the first gate line G1. The fourth TFT supplies a G data voltage from the fourth data line S4 to the pixel electrode PXL of the G12 subpixel, in response to the first gate pulse from the first gate line G1.

[0131] R subpixels R21, R22, R61, and R62 and B subpixels B21, B22, B61, and B62 are alternately arranged on the (4i+2)th row lines L2 and L6. The R subpixels R21, R22, R61, and R62 are arranged at positions where the (4i+2)th row lines L2 and L6 and the odd-numbered column lines C1 and C3 intersect. The B subpixels B21, B22, B61, and B62 are arranged at positions where the (4i+2)th row lines L2 and L6 and the even-numbered column lines C2 and C4 intersect.

[0132] The subpixels of third and fourth colors R and B arranged on the (4i+2)th row lines L2 and L6 comprise TFTs arranged at the intersections of the data lines to the right (first side) and the (4i+2)th gate lines G2 and G6, respectively. Each TFT supplies a data voltage from the data line to the right (first side) of the subpixel to the pixel electrode. The TFT of the R21 subpixel is referred to as a fifth TFT, the TFT of the B21 subpixel as a sixth TFT, the TFT of the R22 subpixel as a seventh TFT, and the TFT of the B22 subpixel as an eighth TFT. The fifth TFT supplies an R data voltage from the second data line S2 to the pixel electrode PXL of the R21 subpixel, in response to a third gate pulse from the

second gate line G2. The sixth TFT supplies a B data voltage from the third data line S3 to the pixel electrode PXL of the B21 subpixel, in response to the third gate pulse from the second gate line G2. The seventh TFT supplies an R data voltage from the fourth data line S4 to the pixel electrode PXL of the R22 subpixel, in response to the third gate pulse from the second gate line G2. The eighth TFT supplies a B data voltage from the fifth data line S5 to the pixel electrode PXL of the B22 subpixel, in response to the third gate pulse from the second gate line G2.

[0133] G subpixels G31, G32, G71, and G72 and W subpixels W31, W32, W71, and W72 are alternately arranged on the (4i+3)th row lines L3 and L7. The G subpixels G31, G32, G71, and G72 are arranged at positions where the (4i+3)th row lines L3 and L7 and the odd-numbered column lines C1 and C3 intersect. The W subpixels W31, W32, W71, and W72 are arranged at positions where the (4i+3)th row lines L3 and L7 and the even-numbered column lines C2 and C4 intersect.

[0134] The subpixels of the first and second colors W and G arranged on the (4i+3)th row lines L3 and L7 comprise TFTs arranged at the intersections of the data lines to the right (first side) and the (4i+3)th gate lines G3 and G7, respectively. Each TFT supplies a data voltage from the data line to the right (first side) of the subpixel to the pixel electrode. The TFT of the G31 subpixel is referred to as a ninth TFT, the TFT of the W31 subpixel as a tenth TFT, the TFT of the G32 subpixel as an eleventh TFT, and the TFT of the W32 subpixel as a twelfth TFT. The ninth TFT supplies a G data voltage from the second data line S2 to the pixel electrode PXL of the G31 subpixel, in response to a second gate pulse from the third gate line G3. The tenth TFT supplies a W data voltage from the third data line S3 to the pixel electrode PXL of the W31 subpixel, in response to the second gate pulse from the third gate line G3. The eleventh TFT supplies a G data voltage from the fourth data line S4 to the pixel electrode PXL of the G32 subpixel, in response to the second gate pulse from the third gate line G3. The twelfth TFT supplies a W data voltage from the fifth data line S5 to the pixel electrode PXL of the W32 subpixel, in response to the second gate pulse from the third gate line G3.

[0135] B subpixels B41, B42, B81, and B82 and R subpixels R41, R42, R81, and R82 are alternately arranged on the (4i+4)th row lines L4 and L8. The B subpixels B41, B42, B81, and B82 are arranged at positions where the (4i+4)th row lines L4 and L8 and the odd-numbered column lines C1 and C3 intersect. The R subpixels R41, R42, R81, and R82 are arranged at positions where the (4i+4)th row lines L4 and L8 and the even-numbered column lines C2 and C4 intersect.

[0136] The subpixels of the third and fourth colors R and B arranged on the (4i+4)th row lines L4 and L8 comprise TFTs arranged at the intersections of the data lines to the right (first side) and the (4i+4)th gate lines G4 and G8, respectively. Each TFT supplies a data voltage from the data line to the right (first side) of the subpixel to the pixel electrode. The TFT of the B41 subpixel is referred to as a thirteenth TFT, the TFT of the R41 subpixel as a fourteenth TFT, the TFT of the B42 subpixel as a fifteenth TFT, and the TFT of the R42 subpixel as a sixteenth TFT. The thirteenth TFT supplies a B data voltage from the second data line S2 to the pixel electrode PXL of the B41 subpixel, in response to a fourth gate pulse from the fourth gate line G4. The fourteenth TFT supplies an R data voltage from the third data line S3 to the pixel electrode PXL of the R41 subpixel, in response to the fourth gate pulse from the fourth gate line G4. The fifteenth TFT supplies a B data voltage from the fourth data line S4 to the pixel electrode PXL of the B42 subpixel, in response to the fourth gate pulse from the fourth gate line G4. The sixteenth TFT supplies an R data voltage from the fifth data line S5 to the pixel electrode PXL of the R42 subpixel, in response to the fourth gate pulse from the fourth gate line G4.

[0137] In order to reverse the polarity of data voltages once for every 4 dots, the source drive ICs output data voltages with first polarity during 4 horizontal periods 4H, and then output data voltages with second polarity during the next 4 horizontal periods 4H.

[0138] The data voltages supplied to the odd-numbered data lines S1, S3, and S5 are output from the source drive ICs during 4 horizontal periods 4H, in order: data voltage of the third color R, data voltage of the first color W, data voltage of the first color W, and data voltage of the fourth color B, and then their polarity is reversed. The polarity of the data voltages supplied to the odd-numbered data lines S1, S3, and S5 is reversed on the data voltages of the fourth color B.

[0139] The data voltages supplied to the even-numbered data lines S2 and S4 are output from the source drive ICs during 4 horizontal periods 4H, in order: data voltage of the fourth color B, data voltage of the second color G, data voltage of the second color G, and data voltage of the third color R, and then their polarity is reversed. The polarity of the data voltages supplied to the even-numbered data lines S2 and S4 is reversed on the data voltages of the fourth color B.

[0140] As shown in FIG. 19, the timing controller 20 controls in such a way that there is a difference of 1 horizontal period 1H between the polarity reversal timing of data voltages supplied to the odd-numbered data lines S1, S3, and S5 and the polarity reversal timing of data voltages supplied to the even-numbered data lines S2 and S4.

[0141] Link lines LNK connecting (4i+2)th and (4i+3)th output channels 2 and 3 of the gate driver 104 and the (4i+2)th and (4i+3)th gate lines G2, G3, G6, and G7 intersect, with an insulating layer in between. Due to this, as shown in FIG. 19, although the gate driver 104 outputs a third gate pulse through the third output channel 3 after outputting a second gate pulse through the second output channel 2, the third gate pulse is applied to the second gate line G2 after the second gate pulse is applied to the third gate line G3. Accordingly, gate pulses are applied to the gate lines G1 to G8 in order: G1, G3, G2, G4, G5, G7, G6, and G8.

[0142] FIGS. 20A to 21G show how data voltage transitions occur when a test pattern of various colors is displayed

on the pixel array according to the fourth exemplary embodiment of the present invention.

[0143] FIGS. 20A to 20G are views showing which subpixels are lit up and their polarity, when white, red, green, blue, yellow, cyan, and magenta patterns are displayed on the pixel array, according to the fourth exemplary embodiment of the present invention. FIGS. 21A to 21G are views showing data voltages when the colors of FIGS. 20A to 20G are displayed on the pixel array. The arrows in FIGS. 21A to 21G indicate data voltage transitions.

[0144] Referring to FIGS. 20A and 21A, when a white pattern is displayed on the pixels of the pixel array, the R subpixels, G subpixels, B subpixels, and W subpixels are all lit up at the white level. In the white pattern, the RGBW data voltages are the white-level voltage. For the white pattern to be displayed on the pixel array, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 18 change twice with a voltage swing of 2 V during 8 horizontal periods 8H. At these data voltages, the temperature of heat generated from the source drive ICs is 246 °C, as seen from Table 1.

[0145] Referring to FIGS. 20B and 21B, when a red pattern is displayed on the pixels of the pixel array, only the R subpixels are lit up at the white level. In the red pattern, the R data voltage is the white-level voltage, and the data voltages of the other colors are the black-level voltage. For the red pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 18 change three times with a voltage swing of 1 V during 8 horizontal periods 8H. At these data voltages, the temperature of heat generated from the source drive ICs is 222 °C, as seen from Table 1.

[0146] Referring to FIGS. 20C and 21C, when a green pattern is displayed on the pixels of the pixel array, only the G subpixels are lit up at the white level. In the green pattern, the G data voltage is the white-level voltage, and the data voltages of the other colors are the black-level voltage. For the green pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 18 change once with a voltage swing of 1 V during 8 horizontal periods 8H. At these data voltages, the temperature of heat generated from the source drive ICs is 150 °C, as seen from Table 1.

[0147] Referring to FIGS. 20D and 21D, when a blue pattern is displayed on the pixels of the pixel array, only the B subpixels are lit up at the white level. In the blue pattern, the B data voltage is the white-level voltage, and the data voltages of the other colors are the black-level voltage. For the blue pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 18 change twice with a voltage swing of 1 V during 8 horizontal periods 8H. At these data voltages, the temperature of heat generated from the source drive ICs is 201 °C, as seen from Table 1.

[0148] Referring to FIGS. 20E and 21E, when a yellow pattern is displayed on the pixels of the pixel array, the G subpixels and the R subpixels are lit up at the white level. In the yellow pattern, the G data voltage and the R data voltage are the white-level voltage (or highest voltage), and the data voltages of the other colors are the black-level voltage (or lowest voltage). For the yellow pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 18 change three times with a voltage swing of 1 V during 8 horizontal periods 8H. At these data voltages, the temperature of heat generated from the source drive ICs is 222 °C, as seen from Table 1.

[0149] Referring to FIGS. 20F and 21F, when a cyan pattern is displayed on the pixels of the pixel array, the G subpixels and the B subpixels are lit up at the white level. In the cyan pattern, the G data voltage and the B data voltage are the white-level voltage, and the data voltages of the other colors are the black-level voltage. For the cyan pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 18 change twice with a voltage swing of 1 V during 8 horizontal periods 8H. At these data voltages, the temperature of heat generated from the source drive ICs is 201 °C, as seen from Table 1.

[0150] Referring to FIGS. 20G and 21G, when a magenta pattern is displayed on the pixels of the pixel array, the B subpixels and the R subpixels are lit up at the white level. In the magenta pattern, the B data voltage and the R data voltage are the white-level voltage, and the data voltages of the other colors are the black-level voltage. For the magenta pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 18 change three times with a voltage swing of 1 V during 8 horizontal periods 8H. At these data voltages, the temperature of heat generated from the source drive ICs is 255 °C, as seen from Table 1.

[0151] As can be seen from above, in the fourth exemplary embodiment (FIGS. 17 to 19) of the present invention, the balance of polarity may be attained for each color without polarity banding phenomenon, and therefore input images may be reproduced with high picture quality. In the fourth exemplary embodiment (FIGS. 17 to 19) of the present invention, the power consumption and heat generation of the source drive ICs may be reduced for every color.

[0152] The following Table 1 shows the number of transitions in data voltage supplied to 8 lines during 8 horizontal periods, the data voltage swing, and the resulting temperature of heat generated from the source drive ICs in the first through fourth exemplary embodiment of the present invention, when colors of white, red, green, blue, yellow, cyan, and magenta are displayed.

[Table 1]

Color Pattern	First Exemplar Embodiment (FIGS. 2~4)		Second Exemplary Embodiment (FIGS. 7~9)		Third Exemplary Embodiment (FIGS. 12~14)		Fourth Exemplary Embodiment (FIGS. 17~19)	
	Number of Transitions within 8 lines	Expected Temperature of Heat Generation (°C)	Number of Transitions within 8 lines	Expected Temperature of Heat Generation (°C)	Number of Transitions within 8 lines	Expected Temperature of Heat Generation (°C)	Number of Transitions within 8 lines	Expected Temperature of Heat Generation (°C)
White	2(2V)/8 H	246	2(2V)/8 H	246	2(2V)/8 H	246	2(2V)/8 H	246
Red	2/8H	201	1/8H	150	1/8H	150	3/8H	222
Green	2/8H	201	2/8H	201	2/8H	201	1/8H	150
Blue	2/8H	201	1/8H	142	1/8H	142	2/8H	201
Yellow	2/8H	201	3/8H	222	2/8H	203	3/8H	222
Cyan	2/8H	201	1/8H	150	2/8H	194	2/8H	201
Magenta	4/8H	355	2/8H	201	2/8H	202	3/8H	255

[0153] As described previously, in the present invention, the balance of polarity can be attained for each color without polarity banding phenomenon by optimizing an arrangement of colors on a display panel comprising subpixels of four colors, and therefore input images can be reproduced with high picture quality. Moreover, the power consumption and heat generation of the source drive ICs can be improved.

[0154] Although embodiments have been described with reference to a number of illustrative embodiments thereof, it should be understood that numerous other modifications and embodiments can be devised by those skilled in the art that will fall within the scope of the principles of this disclosure. More particularly, various variations and modifications are possible the component parts and/or arrangements of the subject combination arrangement within the scope of the disclosure, the drawings and the appended claims. In addition to variations and modifications in the component parts and/or arrangements, alternative uses will also be apparent to those skilled in the art.

Claims

1. A liquid crystal display device that comprises a plurality of data lines (S1 to Sm), a plurality of gate lines (G1 to Gn) intersecting the data lines (S1 to Sm), a plurality of first-color subpixels, a plurality of second-color subpixels, a plurality of third-color subpixels, and a plurality of fourth-color subpixels, the liquid crystal display comprising:

   a data driver (102) configured to reverse the polarity of data voltages for charging subpixels on a preset cycle and configured to supply the data voltages to the data lines (S 1 to Sm),
   wherein, in a pixel array where the subpixels are arranged, the first-color subpixels are arranged at positions where (4i+1)th row lines (L1, L5), wherein i is a positive integer, and odd-numbered column lines (C1, C3) intersect, the second-color subpixels are arranged at positions where the (4i+1)th row lines (L1, L5) and even-numbered column lines (C2, C4) intersect, the third-color subpixels are arranged at positions where (4i+2)th row lines (L2, L6) and the odd-numbered column lines (C1, C3) intersect, the fourth-color subpixels are arranged at positions where the (4i+2)th row lines (L2, L6) and the even-numbered column lines (C2, C4) intersect, the second-color subpixels are arranged at positions where (4i+3)th row lines (L3, L7) and the odd-numbered column lines (C1, C3) intersect, the first-color subpixels are arranged at positions where the (4i+3)th row lines (L3, L7) and the even-numbered column lines (C2, C4) intersect, the fourth-color subpixels are arranged at positions where (4i+4)th row lines (L4, L8) and the odd-numbered column lines (C1, C3) intersect, and the third-color subpixels are arranged at positions where the (4i+4)th row lines (L4, L8) and the even-numbered column lines (C2, C4) intersect.

2. The liquid crystal display device of claim 1, wherein the liquid crystal display further comprising a gate driver (104) configured to supply gate pulses to the gate lines (G1 to Gn) in synchronization with the data voltages.

3. The liquid crystal display device of claim 2, wherein the gate driver (104) is configured to sequentially supply gate pulses to the gate lines (G1 to Gn) in order: first gate line (G1), second gate line (G2), third gate line (G3), and fourth gate line (G4).

4. The liquid crystal display device of one of the preceding claims, wherein the data driver (102) is configured to supply the data lines (S1 to Sm) with data voltages whose polarity is reversed on a cycle of every 4 horizontal periods.

5. The liquid crystal display device of one of the preceding claims, wherein
the first color- and second-color subpixels arranged on the (4i+1)th row lines (L1, L5) comprise thin-film transistors, TFTs, that are configured to supply data voltages from the data lines (S1 to Sm) to the first side of the subpixels to the pixel electrodes, and
the third-color- and fourth-color subpixels arranged on the (4i+4)th row lines (L4, L8) comprise TFTs that are configured to supply data voltages from the data lines (S 1 to Sm) to the second side of the subpixels to the pixel electrodes, wherein the second side of the subpixels is opposite to the first side of that subpixel.

6. The liquid crystal display device of one of the preceding claims, wherein the third-color- and fourth-color subpixels arranged on the (4i+2)th row lines (L2, L6) comprise TFTs that are configured to supply data voltages from the data lines (S1 to Sm) to the second side of the subpixels to the pixel electrodes, and wherein the first color- and second-color subpixels arranged on the (4i+3)th row lines (L3, L7) comprise TFTs that are configured to supply data voltages from the data lines (S1 to Sm) to the first side of the subpixels to the pixel electrodes, wherein the second side of the subpixels is opposite to the first side of that subpixel.

7. The liquid crystal display device of one of the claims 4 to 6,
wherein the polarity of the data voltages supplied to the data lines (S1 to Sm) is reversed on data voltages of the first-color, and there is a difference of 2 horizontal periods between the polarity reversal timing of data voltages supplied to the odd-numbered data lines (S1, S3, S5) and the polarity reversal timing of data voltages supplied to the even-numbered data lines (S2, S4).

8. The liquid crystal display device of one of the claims 1 to 5, wherein the third-color- and fourth-color subpixels arranged on the (4i+2)th row lines (L2, L6) comprise TFTs that are configured to supply data voltages from the data lines (S1 to Sm) to the first side of the subpixels to the pixel electrodes, and the first-color- and second-color subpixels arranged on the (4i+3)th row lines (L3, L7) comprise TFTs that are configured to supply data voltages from the data lines (S1 to Sm) to the second side of the subpixels to the pixel electrodes, wherein the second side of the subpixels is opposite to the first side of that subpixels.

9. The liquid crystal display device of claim 8, wherein the data driver (102) is configured to supply the data lines (S1 to Sm) with the data voltages whose polarity is reversed on a cycle of every 4 horizontal periods, and is configured to simultaneously reverse the polarity of the data voltages supplied to the odd-numbered data lines (S1, S3, S5) and the polarity of the data voltages supplied to the even-numbered data lines (S2, S4),
wherein the polarity of the data voltages supplied to the odd-numbered data lines (S1, S3, S5) is reversed on data voltages of the fourth color, and the polarity of the data voltages supplied to the even-numbered data lines (S2, S4) is reversed on data voltages of the third color,
wherein, among link lines (LNK) connecting output channels of the gate driver (104) and the gate lines (G1 to Gn), the link lines (LNK) connecting the output channels of the second and third gate pulses and the second and third gate lines (G2, G3) intersect so that the third gate pulse is applied to the second gate line (G2) after the second gate pulse is applied to the third gate line (G3).

10. The liquid crystal display device of one of the claims 1 to 5, wherein the third-color- and fourth-color subpixels arranged on the (4i+2)th row lines (L2, L6) comprise TFTs that are configured to supply data voltages from the data lines (S1 to Sm) to the first side of the subpixels to the pixel electrodes, and the first color- and second-color subpixels arranged on the (4i+3)th row lines (L3, L7) comprise TFTs that are configured to supply data voltages from the data lines (S1 to Sm) to the first side of the subpixels to the pixel electrodes.

11. The liquid crystal display device of claim 10, wherein the polarity of the data voltages is supplied to the odd-numbered data lines (S1, S3, S5) is reversed on data voltages of the fourth color, and the polarity of the data voltages supplied to the even-numbered data lines (S2, S4) is reversed on data voltages of the second color, the fourth data voltage after reversal of the polarity of a data voltage supplied to each data line is a data voltage of the fourth color, and there is a difference of 1 horizontal period between the polarity reversal timing of data voltages supplied to the odd-

numbered data lines (S1, S3, S5) and the polarity reversal timing of data voltages supplied to the even-numbered data lines (S2, S4),
wherein, among link lines (LNK) connecting output channels of the gate driver (104) and the gate lines (G1 to Gn), the link lines (LNK) connecting the output channels of the second and third gate pulses and the second and third gate lines (G2, G3) intersect so that the third gate pulse is applied to the second gate line (G2) after the second gate pulse is applied to the third gate line (G3).

12. The liquid crystal display device of one of the claims 1 to 4, wherein the first color- and second-color subpixels arranged on the (4i+1)th row lines (L1, L5) comprise TFTs (thin-film transistors) that are configured to supply data voltages from the data lines (S1 to Sm) to the second side of the subpixels to the pixel electrodes, the third-color- and fourth-color subpixels arranged on the (4i+2)th row lines (L2, L6) comprise TFTs that are configured to supply data voltages from the data lines (S1 to Sm) to the first side of the subpixels to the pixel electrodes, the first color- and second-color subpixels arranged on the (4i+3)th row lines (L3, L7) comprise TFTs that are configured to supply data voltages from the data lines (S 1 to Sm) to the first side of the subpixels to the pixel electrodes, and the third-color- and fourth-color subpixels arranged on the (4i+4)th row lines (L4, L8) comprise TFTs that are configured to supply data voltages from the data lines (S1 to Sm) to the first side of the subpixels to the pixel electrodes, wherein the second side of the subpixels is opposite to the first side of that subpixels.

13. The liquid crystal display device of claim 12, wherein the polarity of the data voltages supplied to the data lines (S 1 to Sm) is reversed on data voltages of the fourth color, and there is a difference of 1 horizontal period between the polarity reversal timing of data voltages supplied to the odd-numbered data lines (S1, S3, S5) and the polarity reversal timing of data voltages supplied to the even-numbered data lines (S2, S4),
wherein, among link lines (LNK) connecting output channels of the gate driver (104) and the gate lines (G1 to Gn), the link lines (LNK) connecting the output channels of the second and third gate pulses and the second and third gate lines (G2, G3) intersect so that the third gate pulse is applied to the second gate line (G2) after the second gate pulse is applied to the third gate line (G3).

14. The liquid crystal display device of one of the preceding claims, wherein the first color is white (W), the second color is green (G), the third color is red (R), and the fourth color is blue (B).

15. A method for driving a liquid crystal display device that comprises a plurality of data lines (S1 to Sm), a plurality of gate lines (G1 to Gn) intersecting the data lines (S1 to Sm), a plurality of first-color subpixels, a plurality of second-color subpixels, a plurality of third-color subpixels, and a plurality of fourth-color subpixels according to one of the preceding claims, comprising the steps of:

Supplying the data lines (S 1 to Sm) with data voltages whose polarity is reversed on a cycle of every 4 horizontal periods by means of a data driver (102);
Suppling gate pulses to the gate lines (G1 to Gn) in synchronization with the data voltages in the order: first gate line (G1), second gate line (G2), third gate line (G3), and fourth gate line (G4) by means of a data driver (102), wherein the data driver (102) supplies the data lines (S1 to Sm) with data voltages whose polarity is reversed on a cycle of every 4 horizontal periods; and
wherein, among link lines connecting output channels of the gate driver (104) and the gate lines (G1 to Gn), the link lines connecting the output channels of the second and third gate pulses and the second and third gate lines (G2, G3) intersect so that the third gate pulse is applied to the second gate line (G2) after the second gate pulse is applied to the third gate line (G3).

FIG. 1

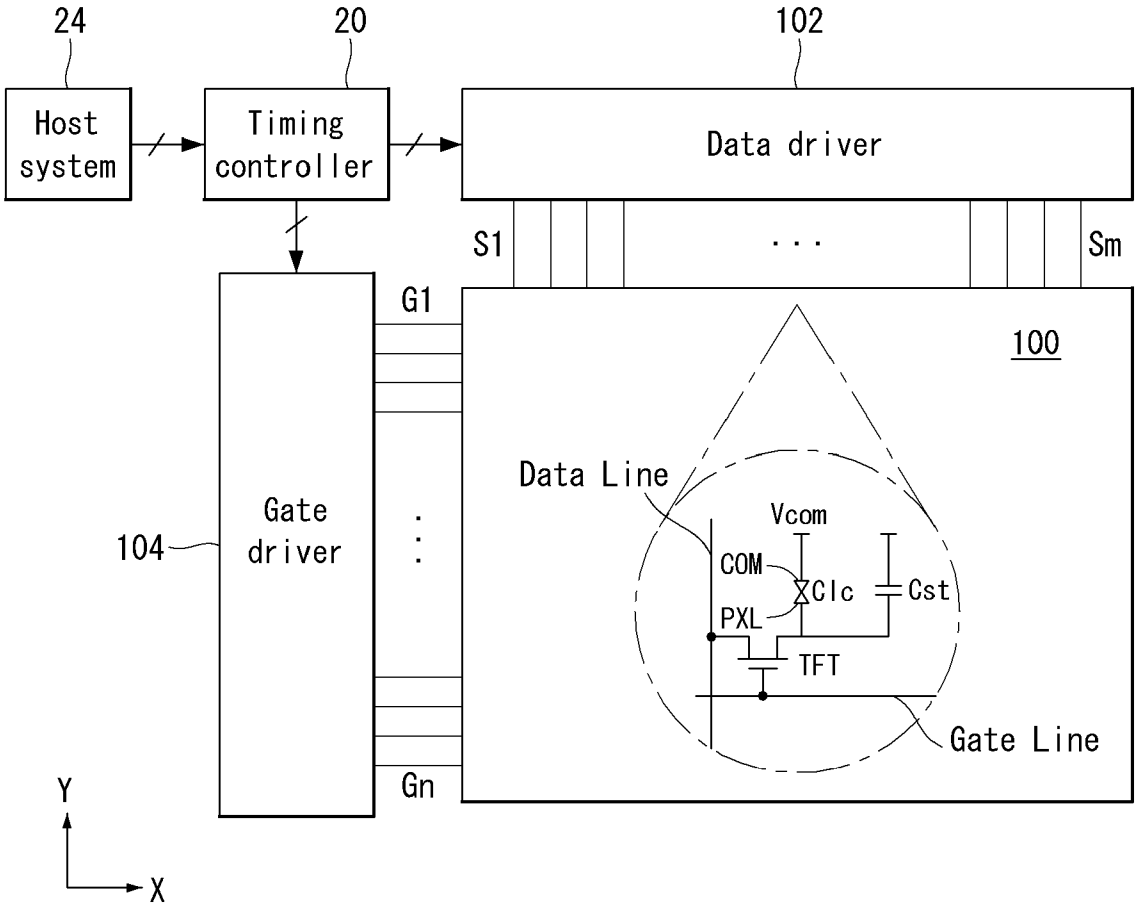

24
20
102
Host system
Timing controller
Data driver
S1
Sm
G1
Gn
Gate driver
104
100
Data Line
Vcom
COM
Clc
Cst
PXL
TFT
Gate Line
Y
X

FIG. 2

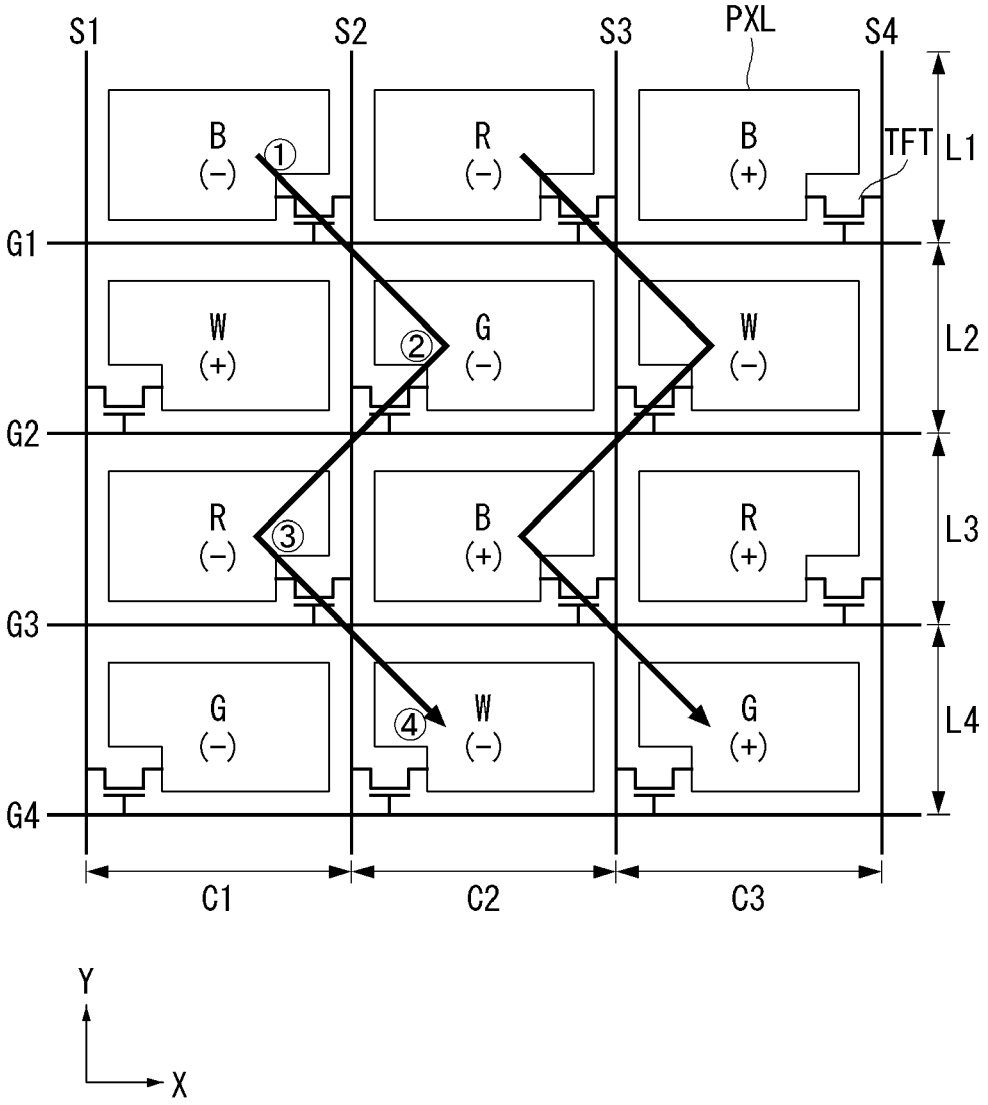

S1
S2
S3
PXL
S4
TFT
L1
L2
L3
L4
G1
G2
G3
G4
C1
C2
C3
B (−)
R (−)
B (+)
W (+)
G (−)
W (−)
R (−)
B (+)
R (+)
G (−)
W (−)
G (+)
①
②
③
④
Y
X

FIG. 3

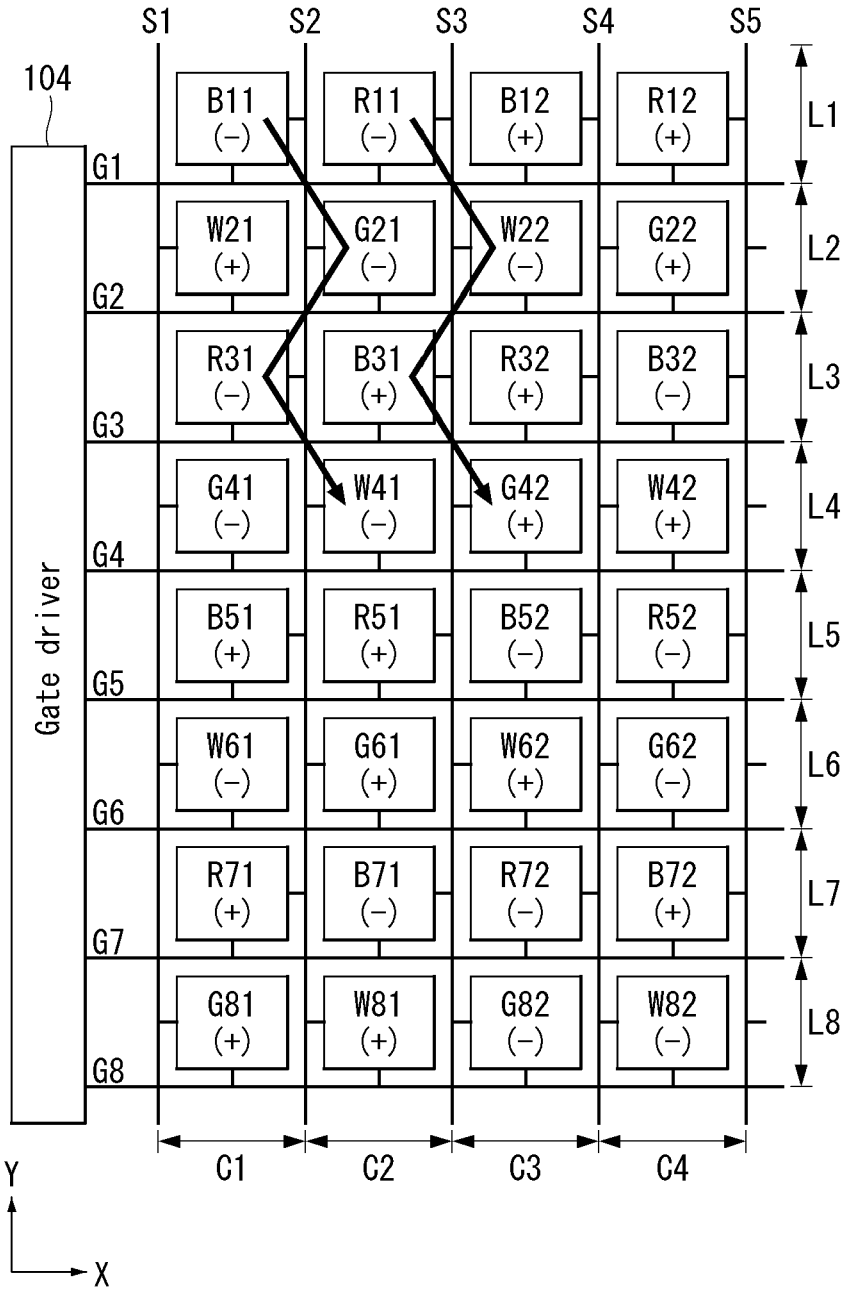

S1
S2
S3
S4
S5
104
Gate driver
G1
G2
G3
G4
G5
G6
G7
G8
B11 (−)
R11 (−)
B12 (+)
R12 (+)
W21 (+)
G21 (−)
W22 (−)
G22 (+)
R31 (−)
B31 (+)
R32 (+)
B32 (−)
G41 (−)
W41 (−)
G42 (+)
W42 (+)
B51 (+)
R51 (+)
B52 (−)
R52 (−)
W61 (−)
G61 (+)
W62 (+)
G62 (−)
R71 (+)
B71 (−)
R72 (−)
B72 (+)
G81 (+)
W81 (+)
G82 (−)
W82 (−)
L1
L2
L3
L4
L5
L6
L7
L8
C1
C2
C3
C4
Y
X

FIG. 4

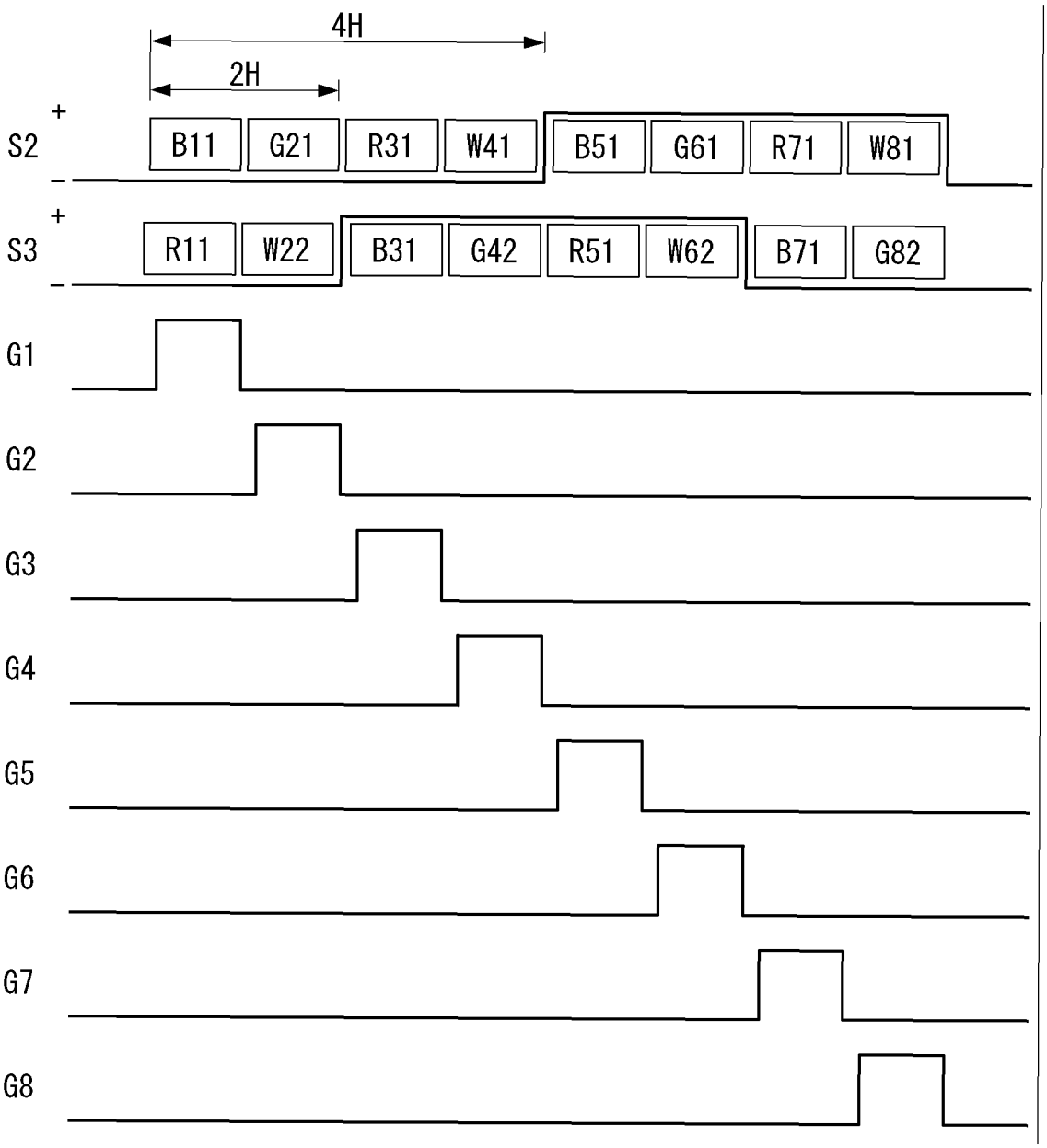
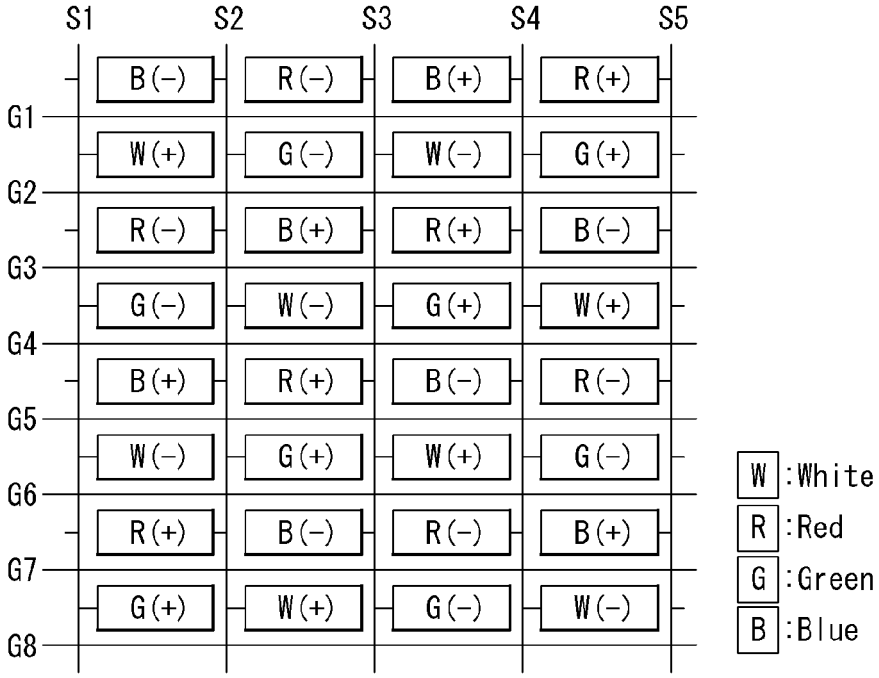
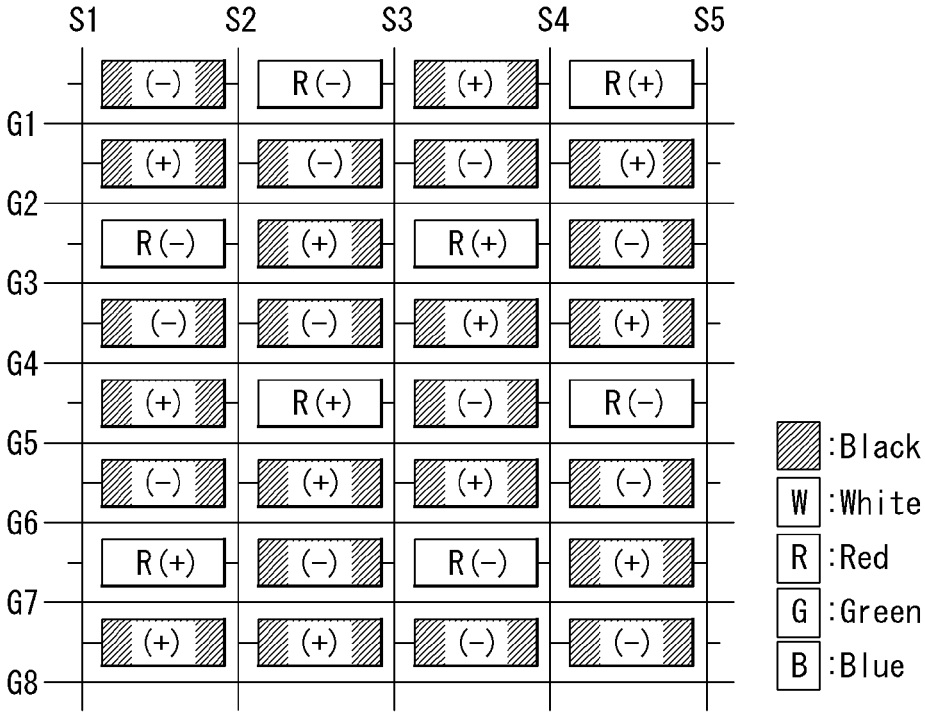

4H
2H
S2
+
−
B11
G21
R31
W41
B51
G61
R71
W81
S3
+
−
R11
W22
B31
G42
R51
W62
B71
G82
G1
G2
G3
G4
G5
G6
G7
G8

FIG. 5A



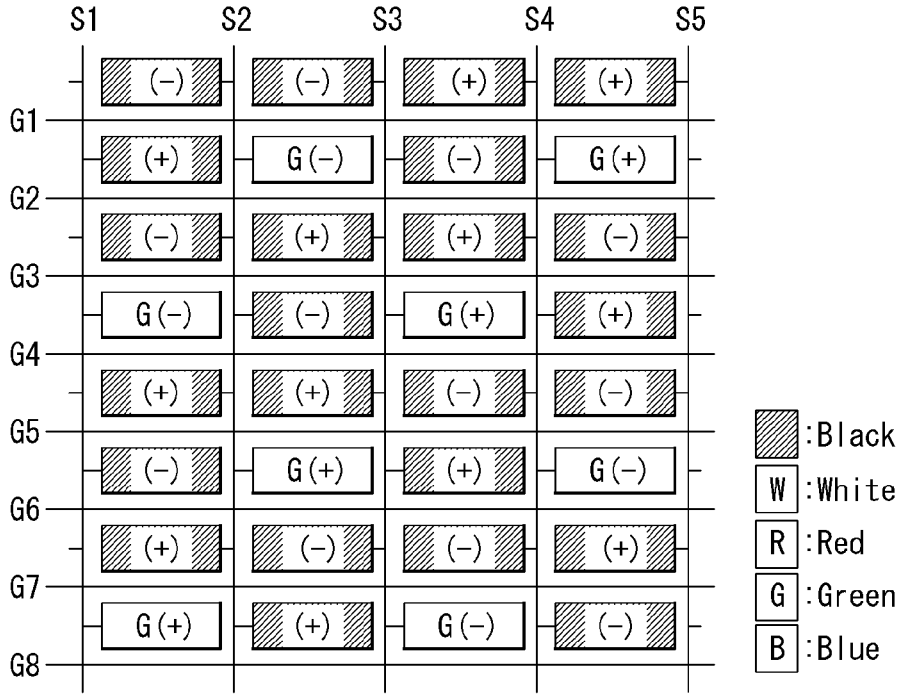
<White>

FIG. 5B



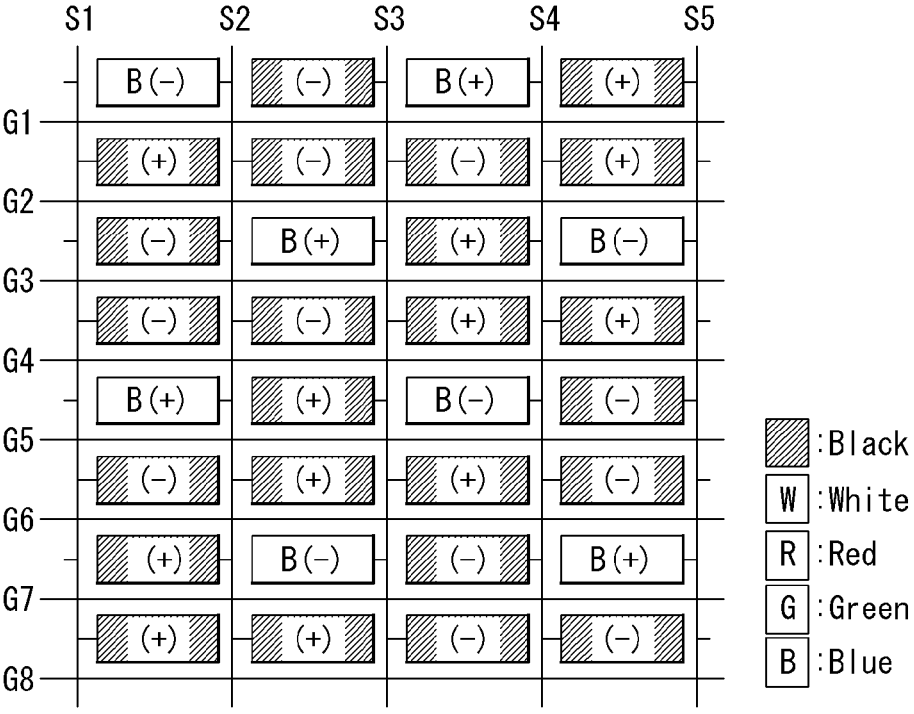
<Red>

FIG. 5C



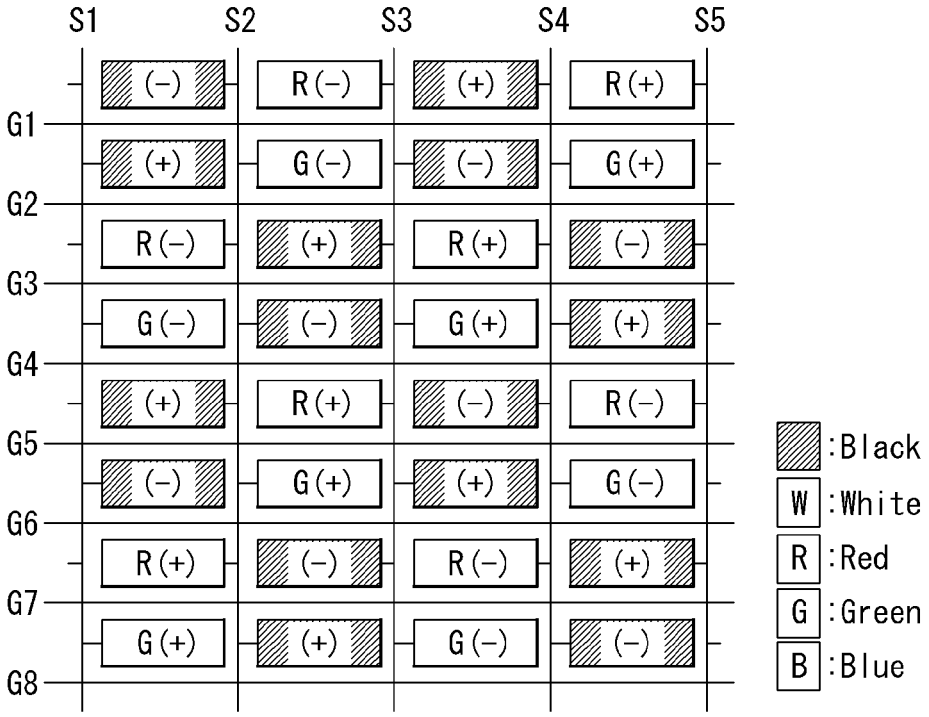
<Green>

FIG. 5D



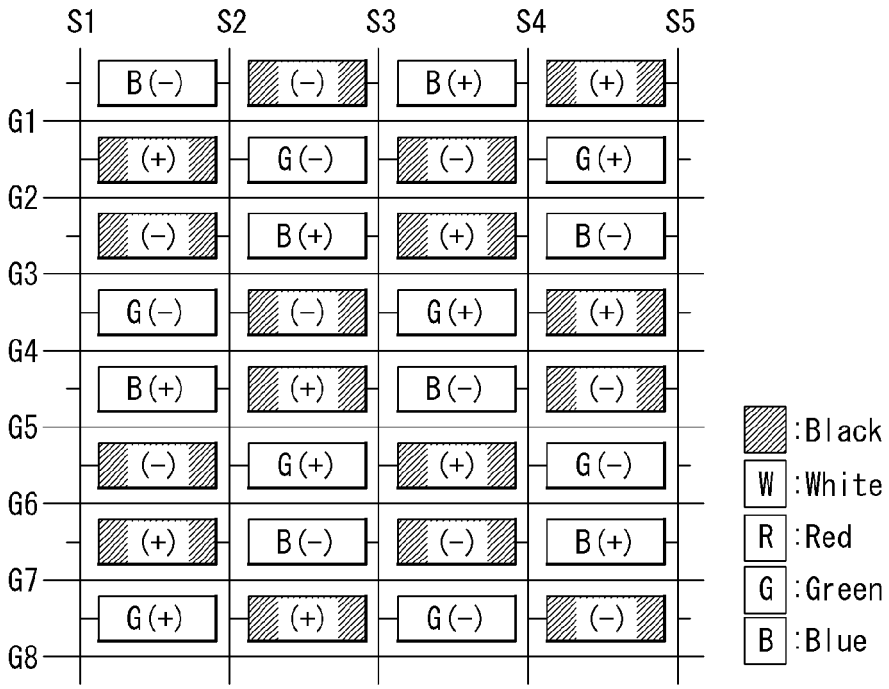
<Blue>

FIG. 5E



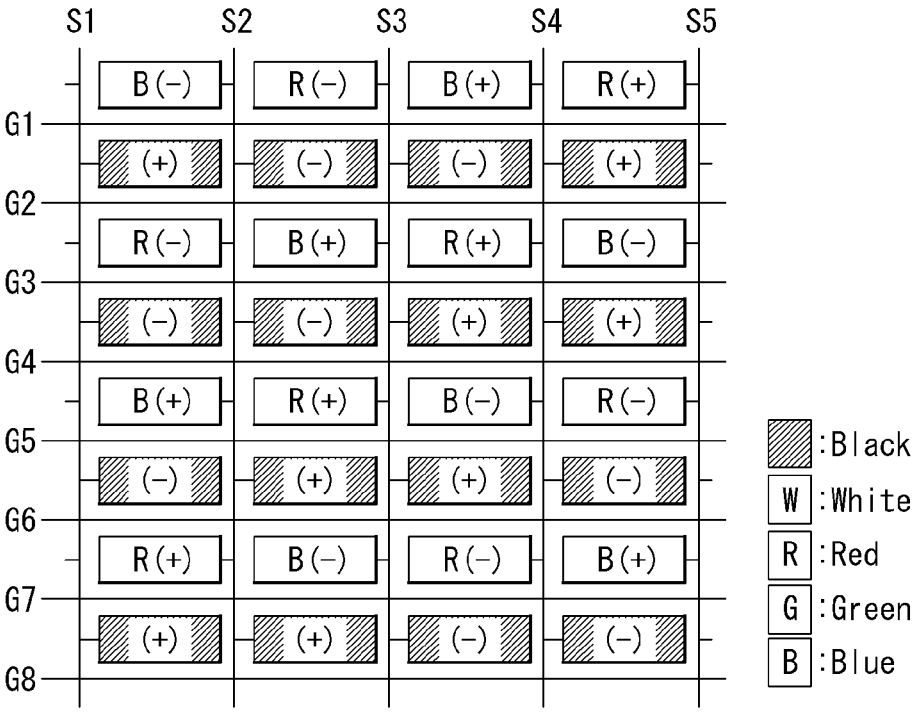
<Yellow>

FIG. 5F



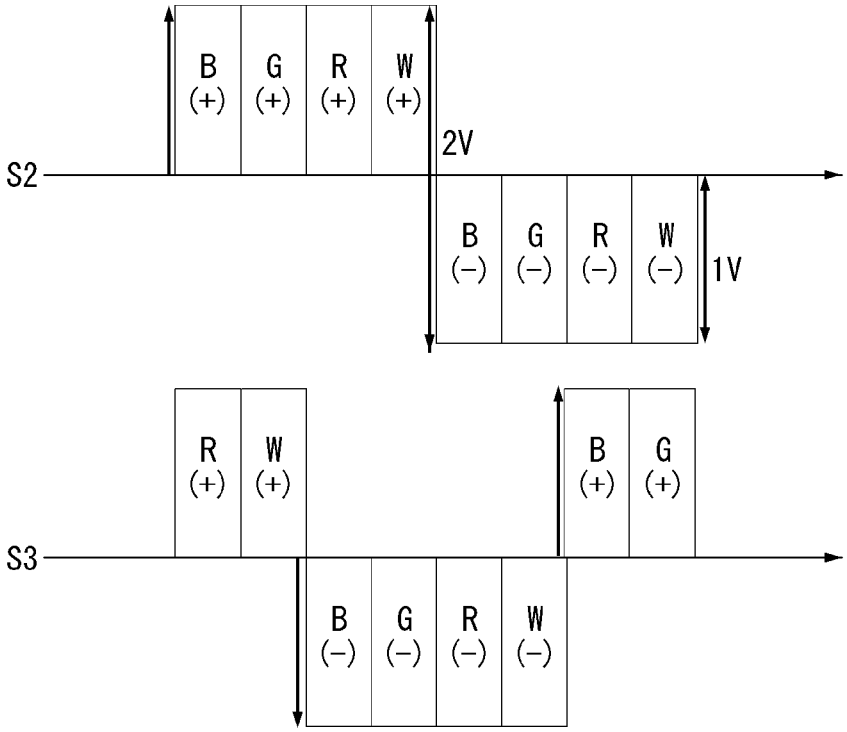
<Cyan>

FIG. 5G



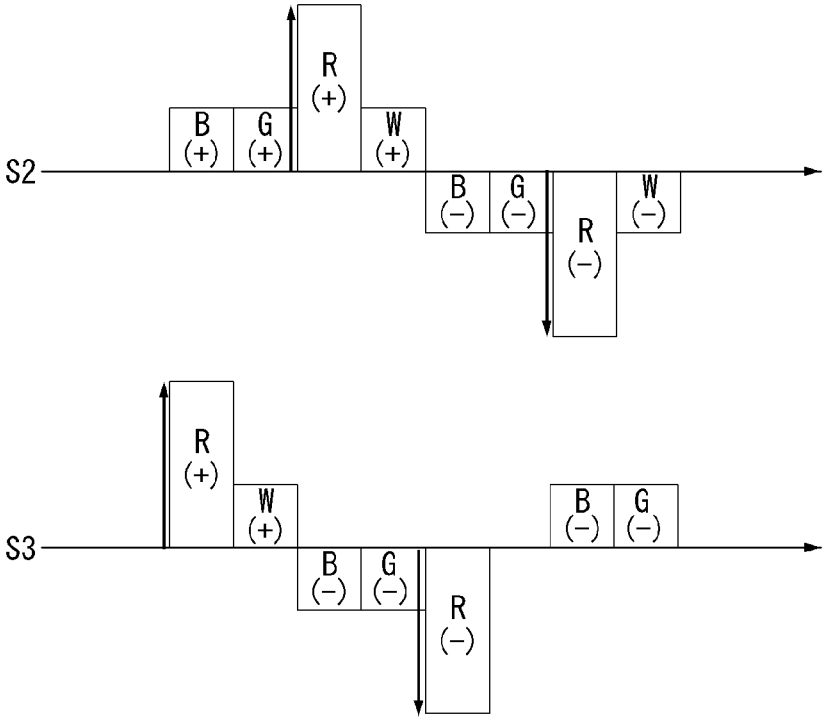
<Magenta>

FIG. 6A



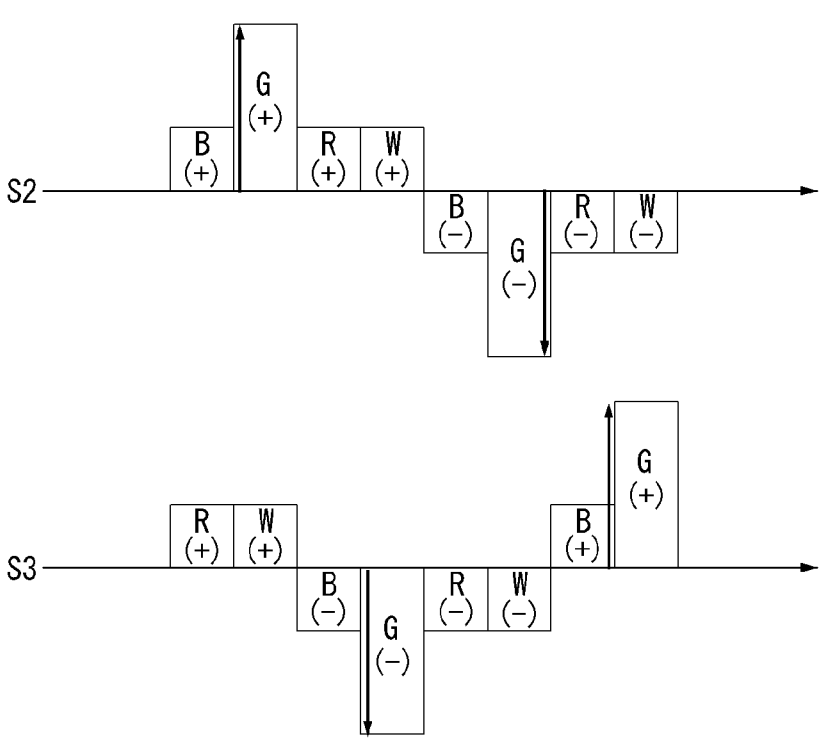
<White>

FIG. 6B



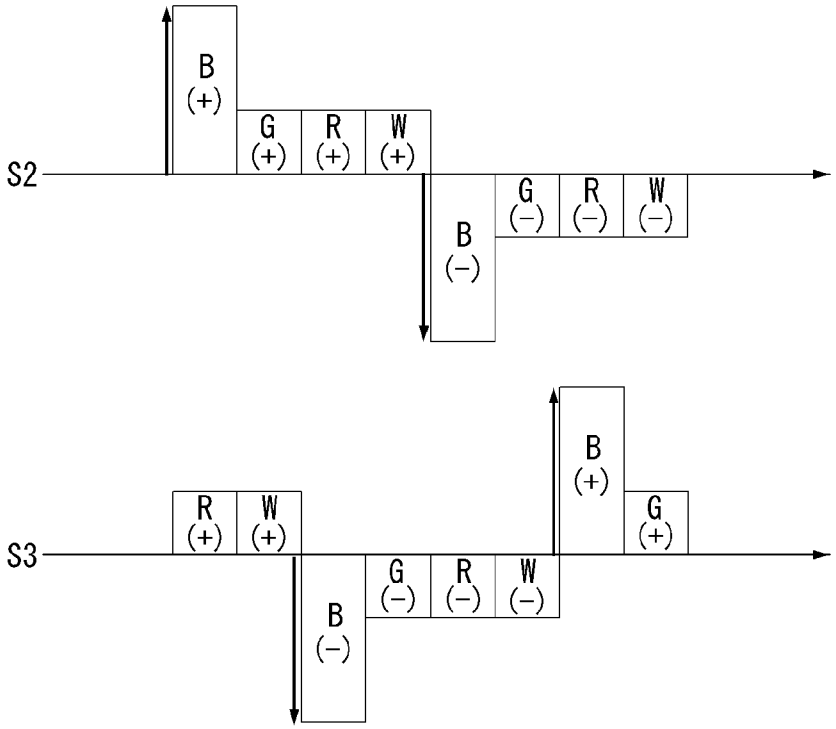
<Red>

FIG. 6C



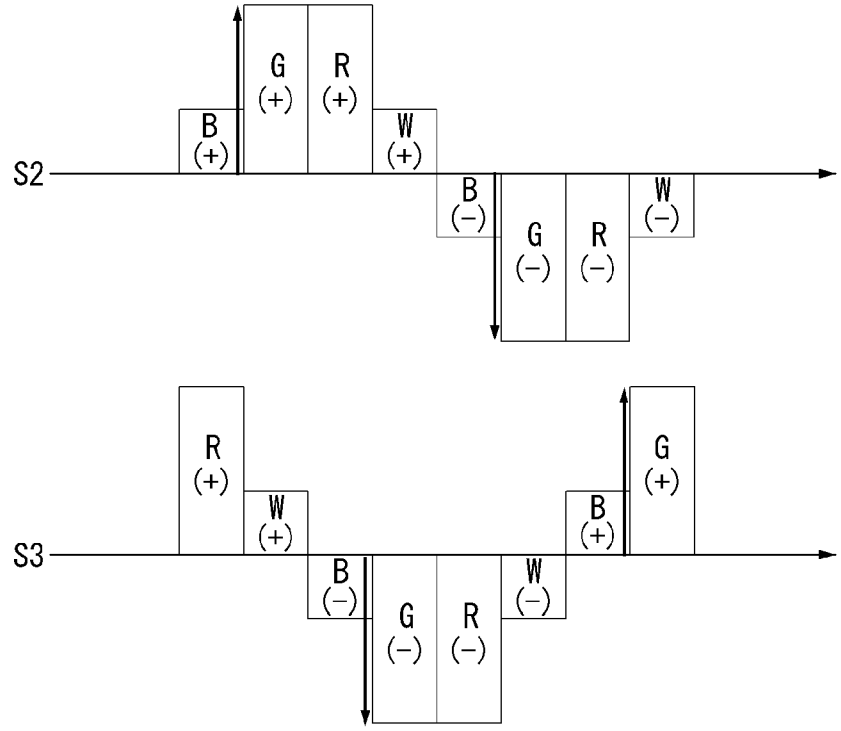
<Green>

FIG. 6D



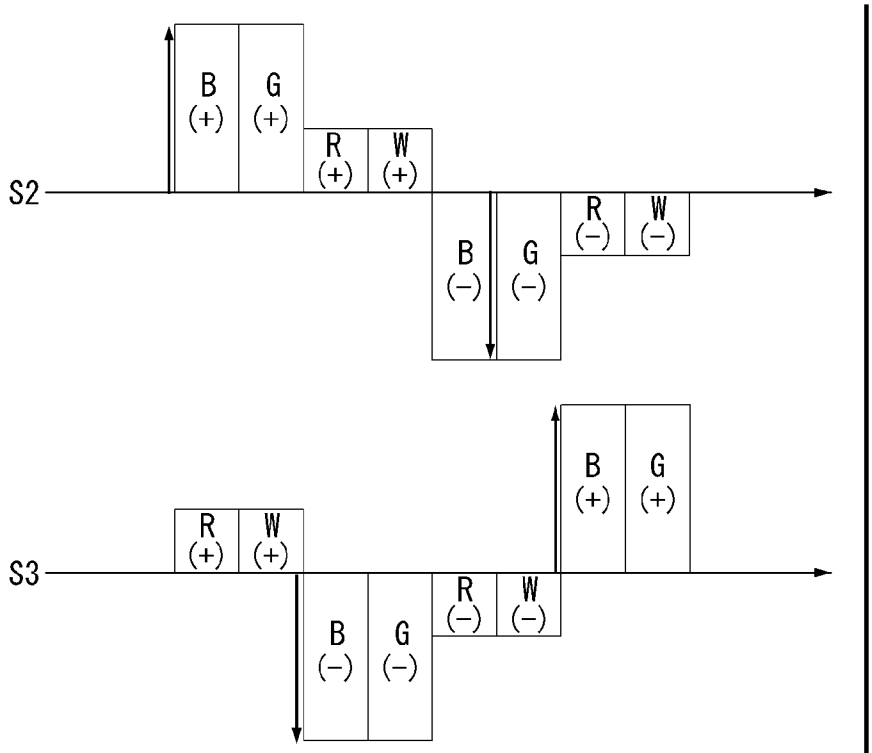
<Blue>

FIG. 6E



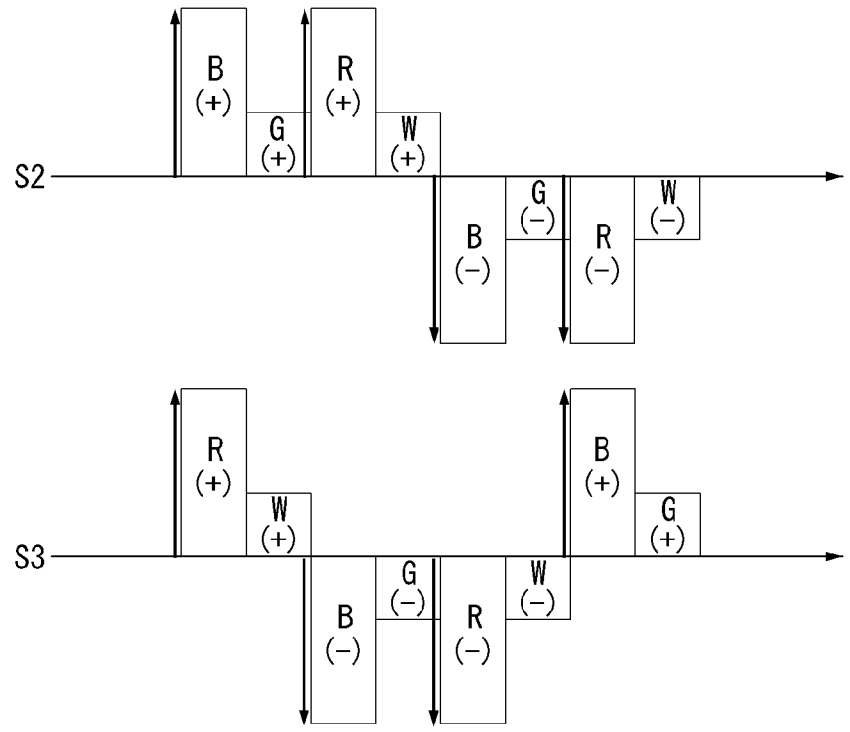
<Yellow>

FIG. 6F



<Cyan>

FIG. 6G



<Magenta>

FIG. 7

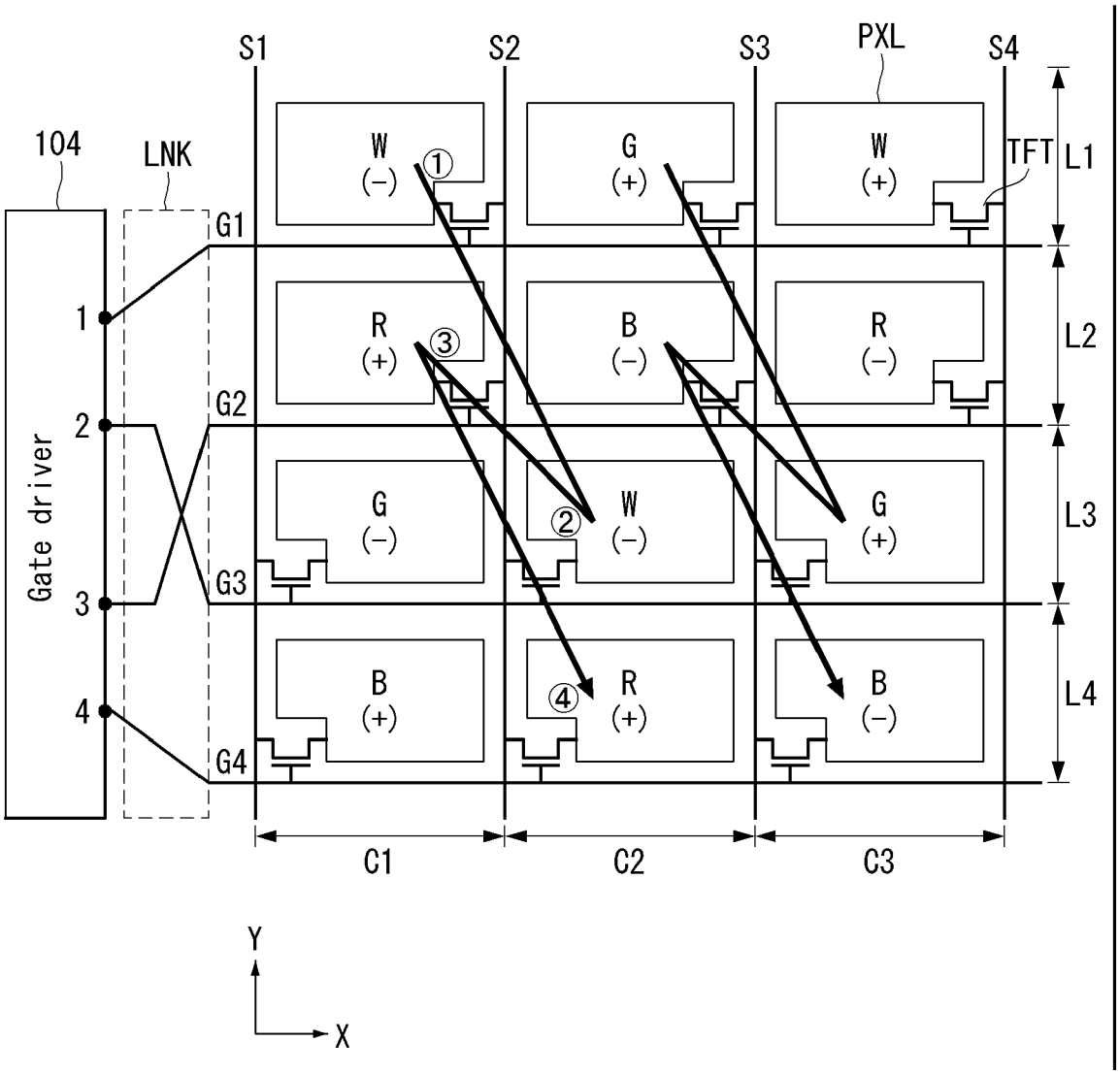

S1
S2
S3
PXL
S4
104
LNK
TFT
L1
L2
L3
L4
G1
G2
G3
G4
Gate driver
1
2
3
4
W (−)
G (+)
W (+)
R (+)
B (−)
R (−)
G (−)
W (−)
G (+)
B (+)
R (+)
B (−)
①
②
③
④
C1
C2
C3
Y
X

FIG. 8

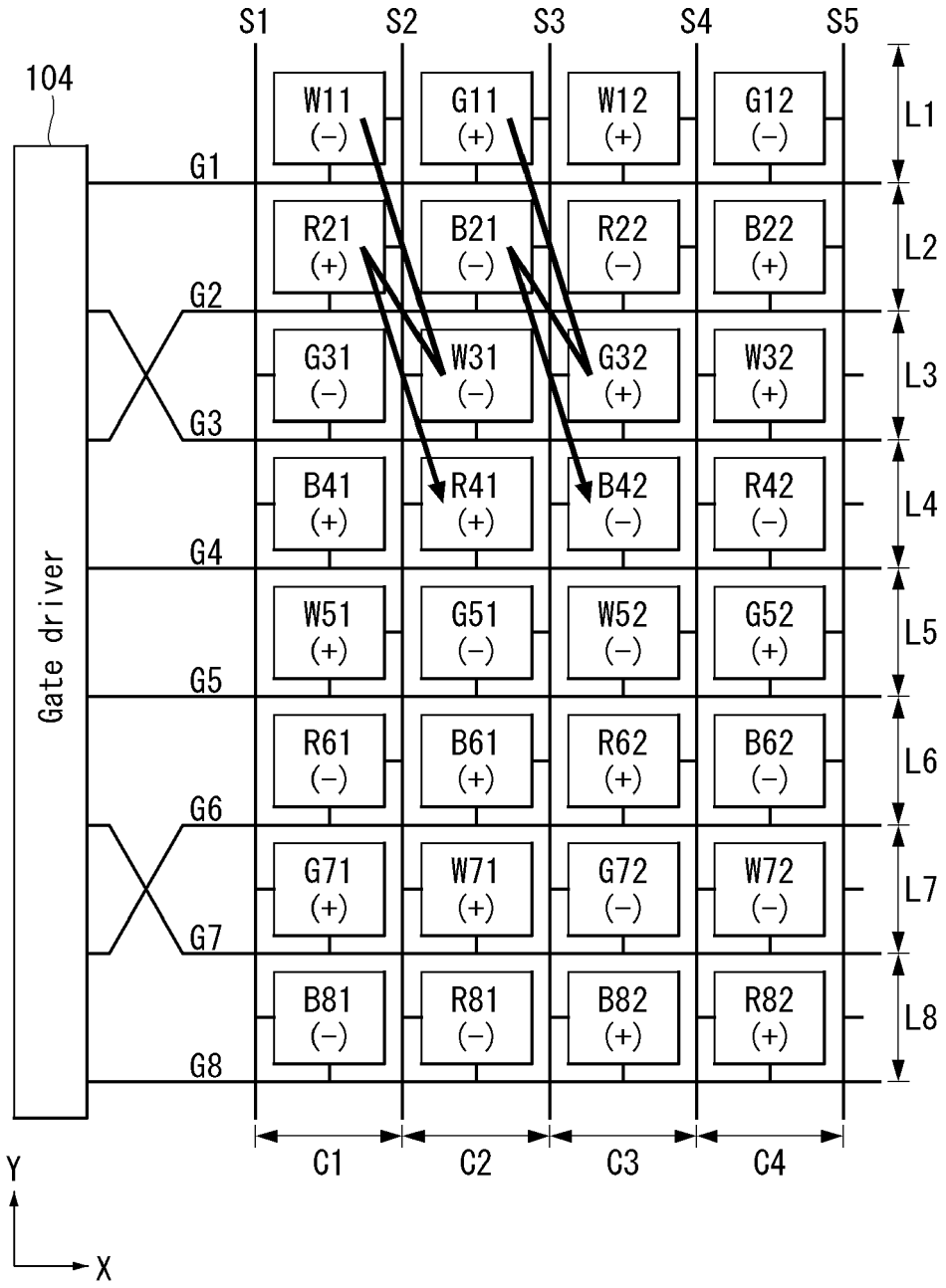

S1
S2
S3
S4
S5
104
Gate driver
G1
G2
G3
G4
G5
G6
G7
G8
W11 (−)
G11 (+)
W12 (+)
G12 (−)
R21 (+)
B21 (−)
R22 (−)
B22 (+)
G31 (−)
W31 (−)
G32 (+)
W32 (+)
B41 (+)
R41 (+)
B42 (−)
R42 (−)
W51 (+)
G51 (−)
W52 (−)
G52 (+)
R61 (−)
B61 (+)
R62 (+)
B62 (−)
G71 (+)
W71 (+)
G72 (−)
W72 (−)
B81 (−)
R81 (−)
B82 (+)
R82 (+)
L1
L2
L3
L4
L5
L6
L7
L8
C1
C2
C3
C4
Y
X

FIG. 9

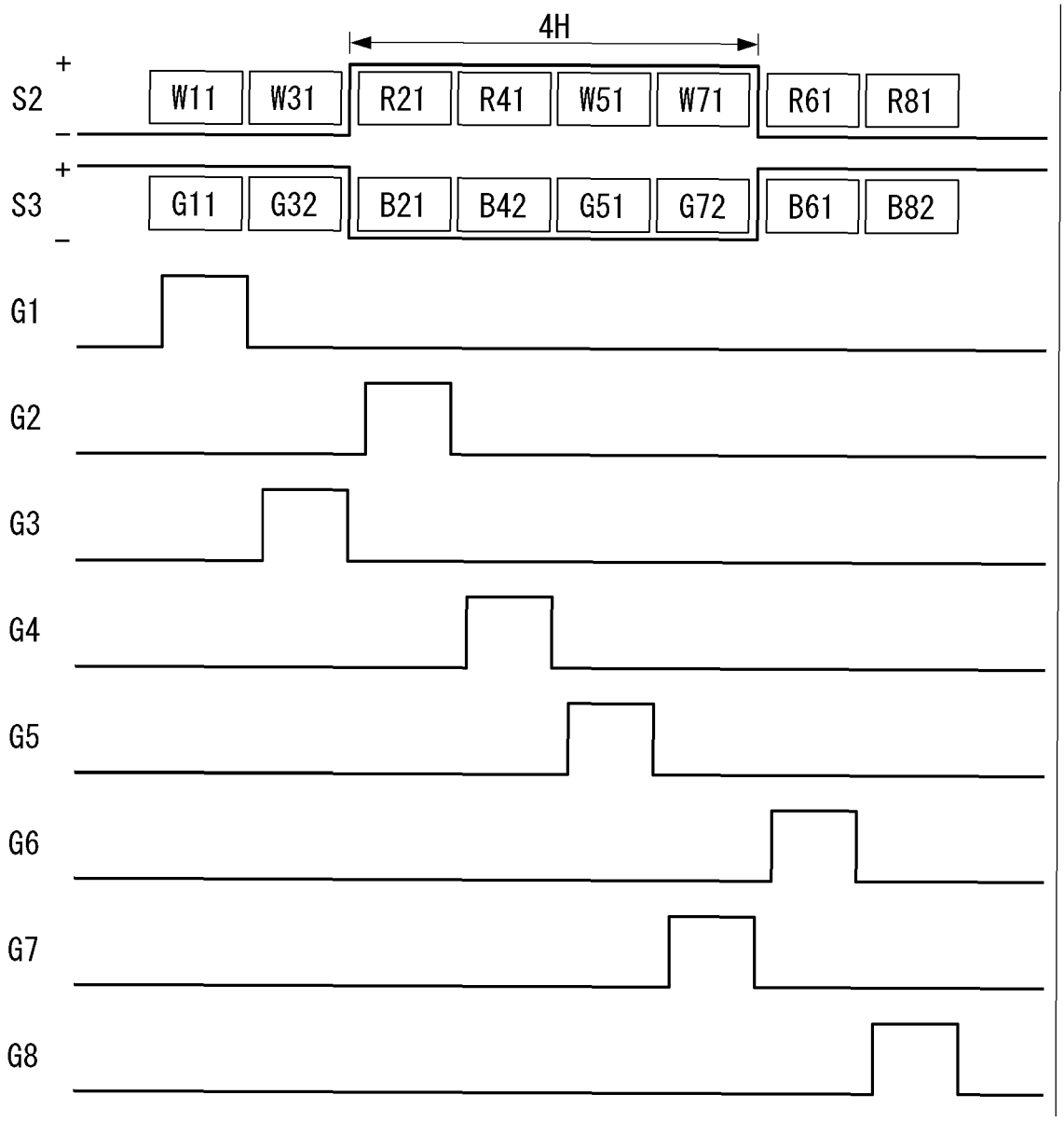
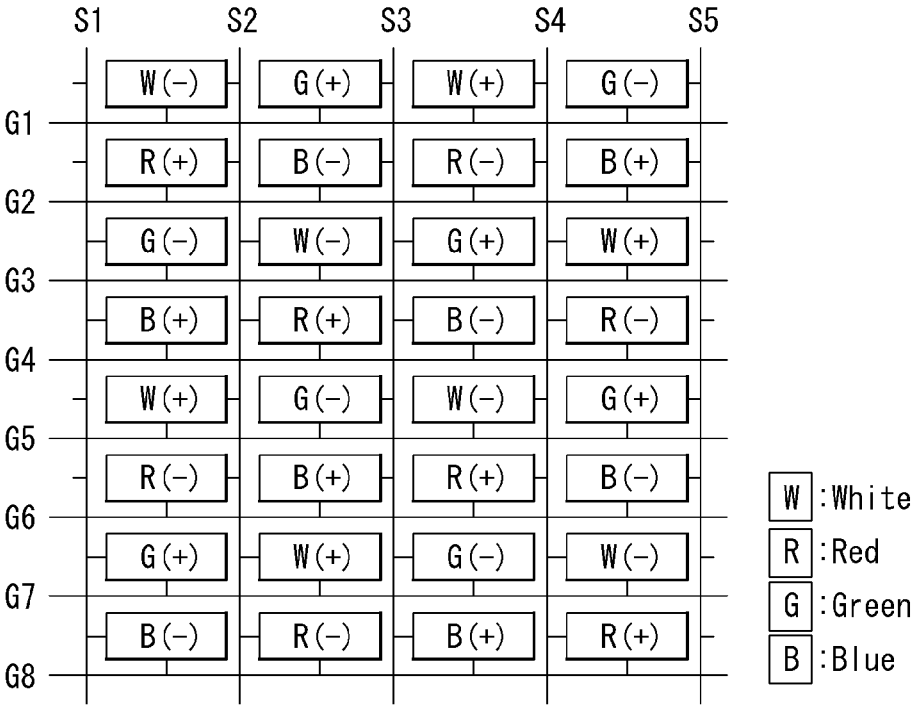
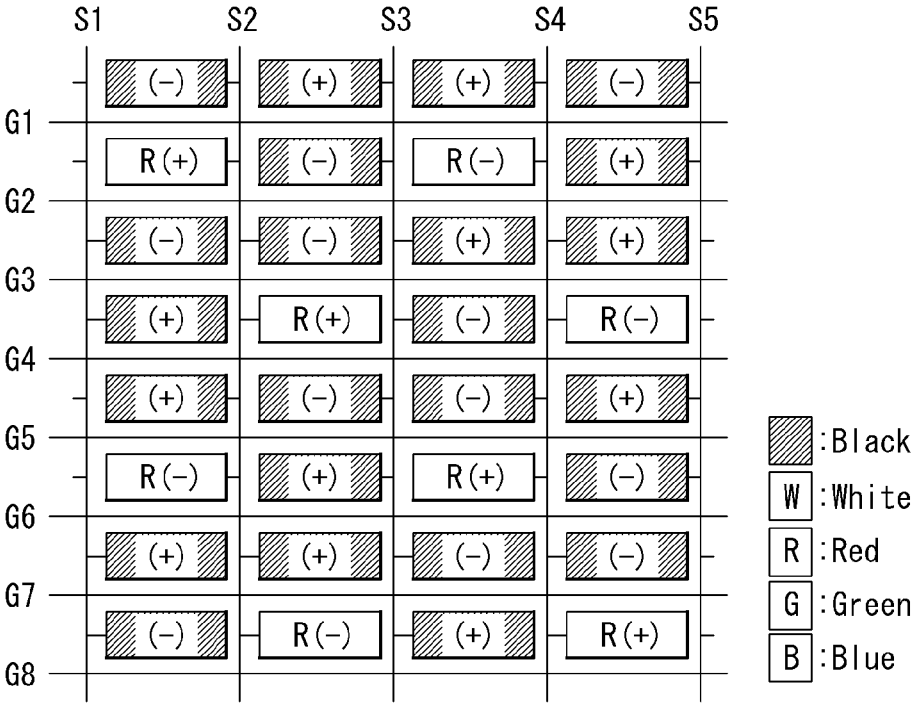

4H
S2
+
−
W11
W31
R21
R41
W51
W71
R61
R81
S3
+
−
G11
G32
B21
B42
G51
G72
B61
B82
G1
G2
G3
G4
G5
G6
G7
G8

FIG. 10A



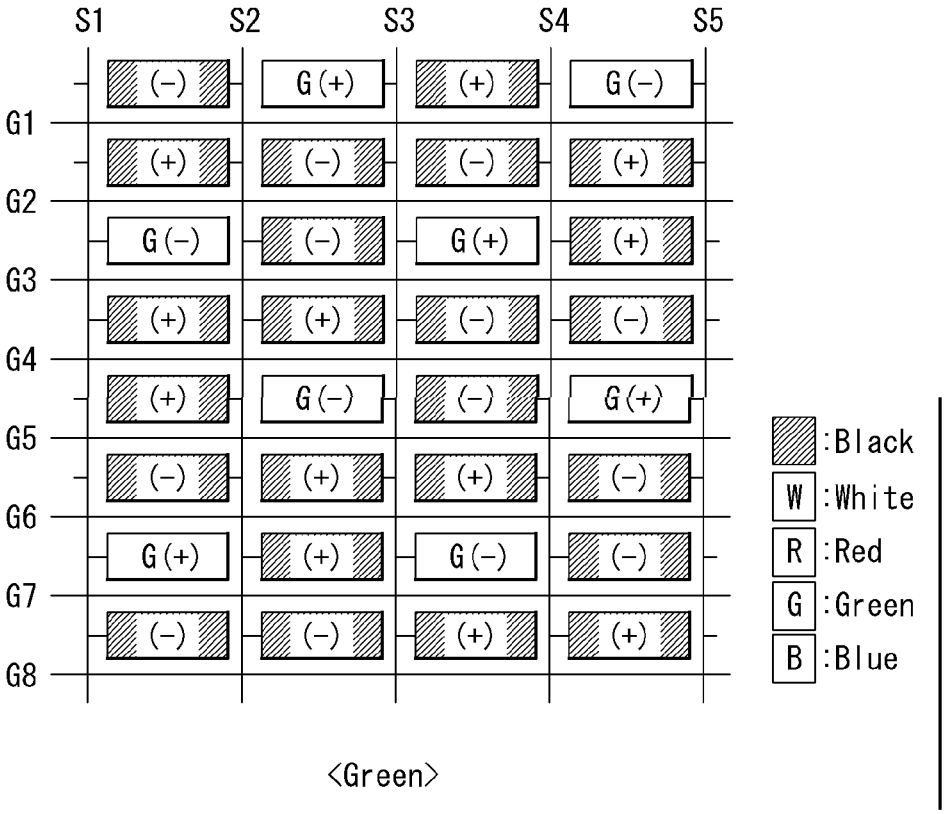
<White>

FIG. 10B



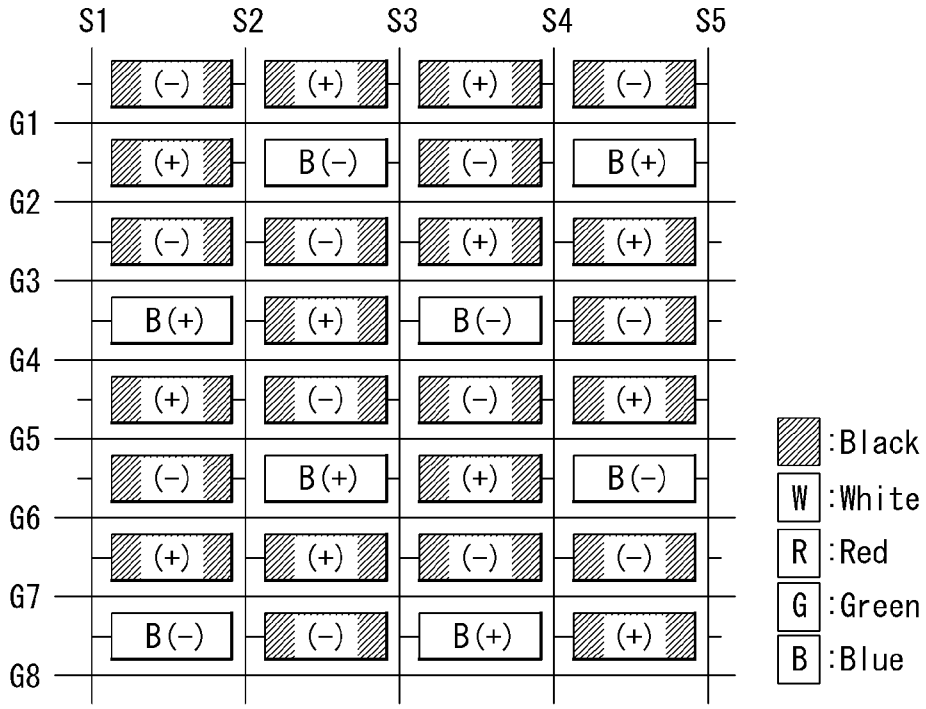
<Red>

FIG. 10C



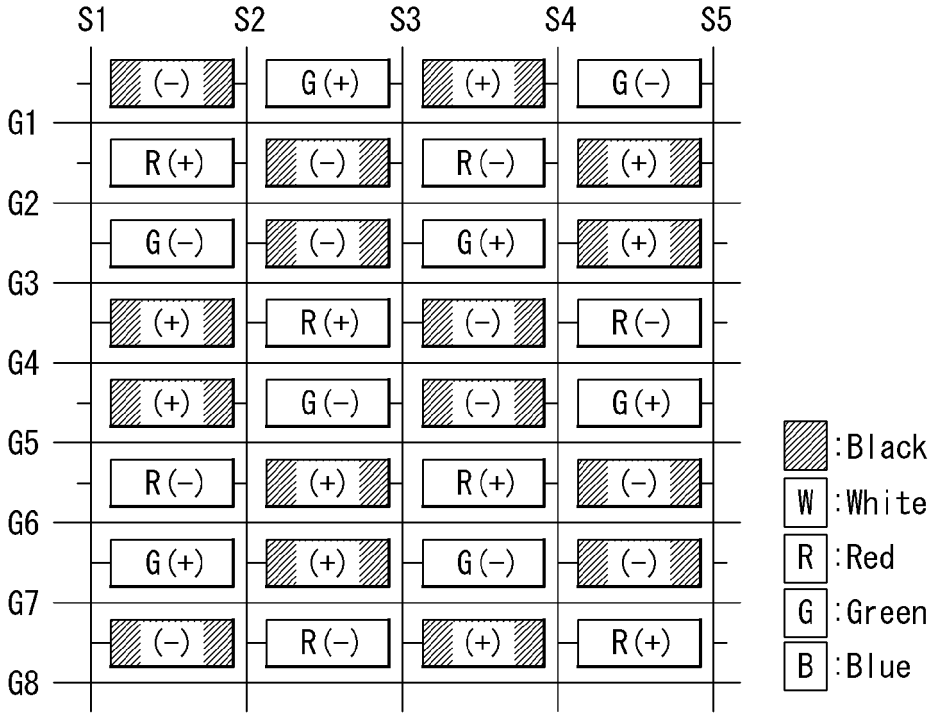
<Green>

FIG. 10D



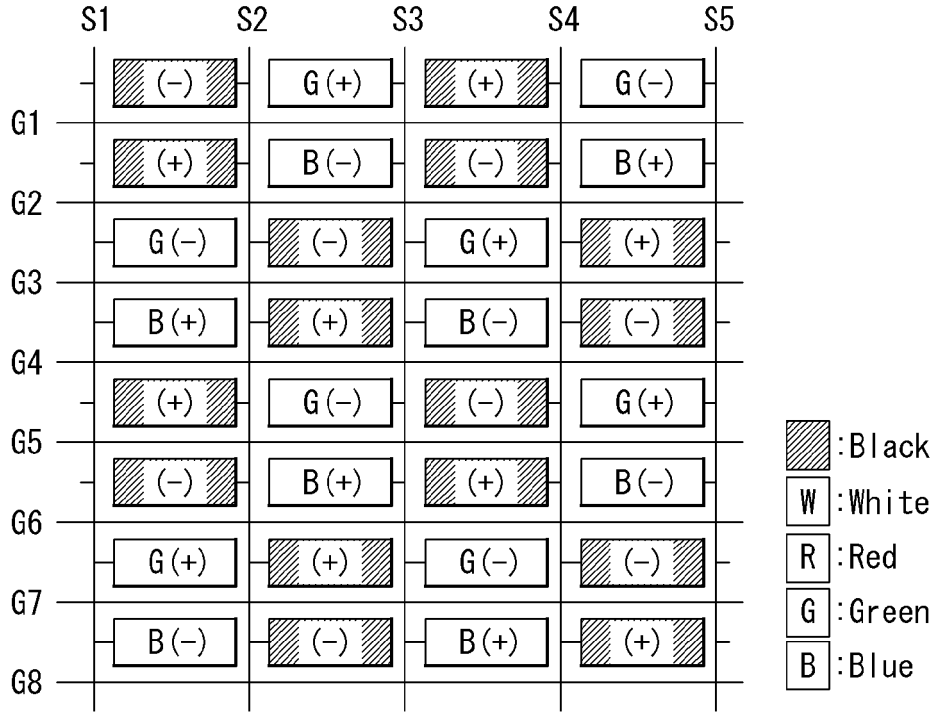
<Blue>

FIG. 10E



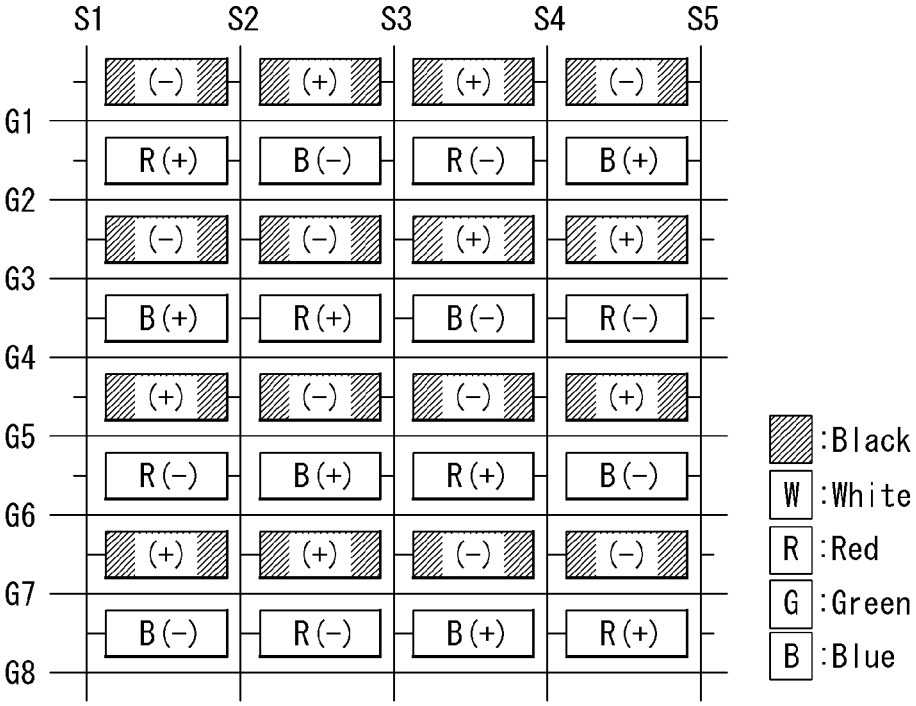
<Yellow>

FIG. 10F



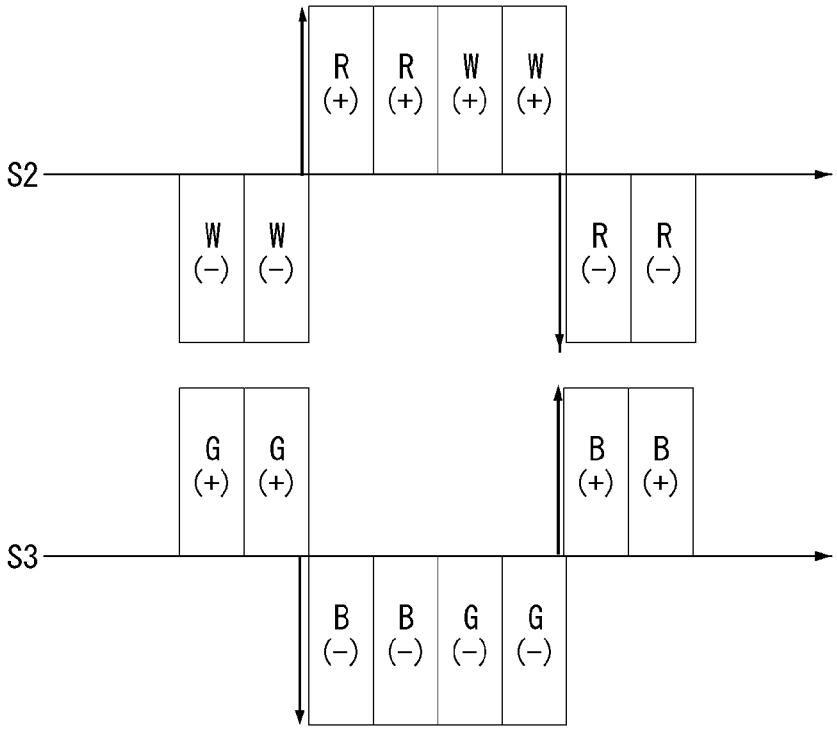
<Cyan>

FIG. 10G



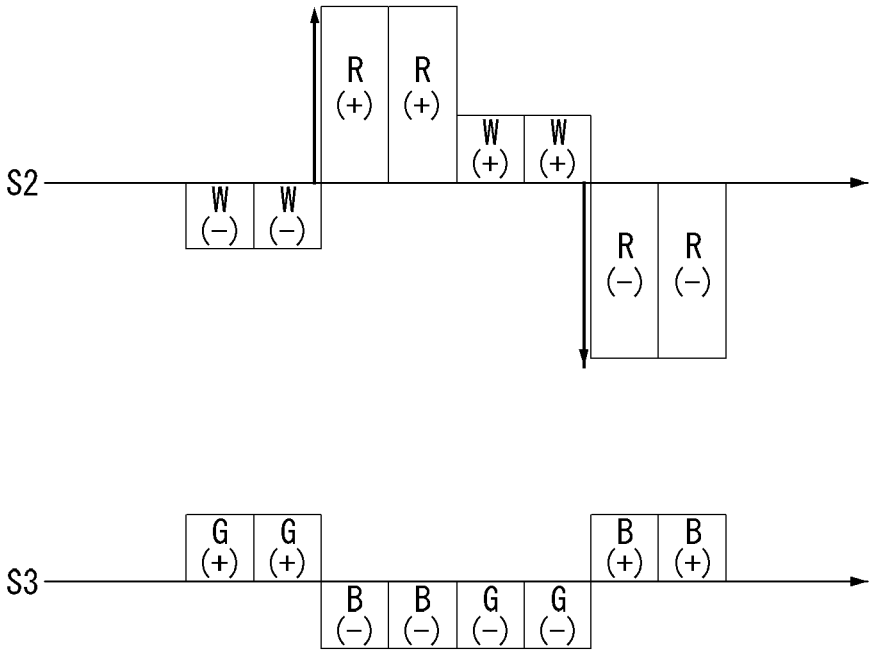
<Magenta>

FIG. 11A



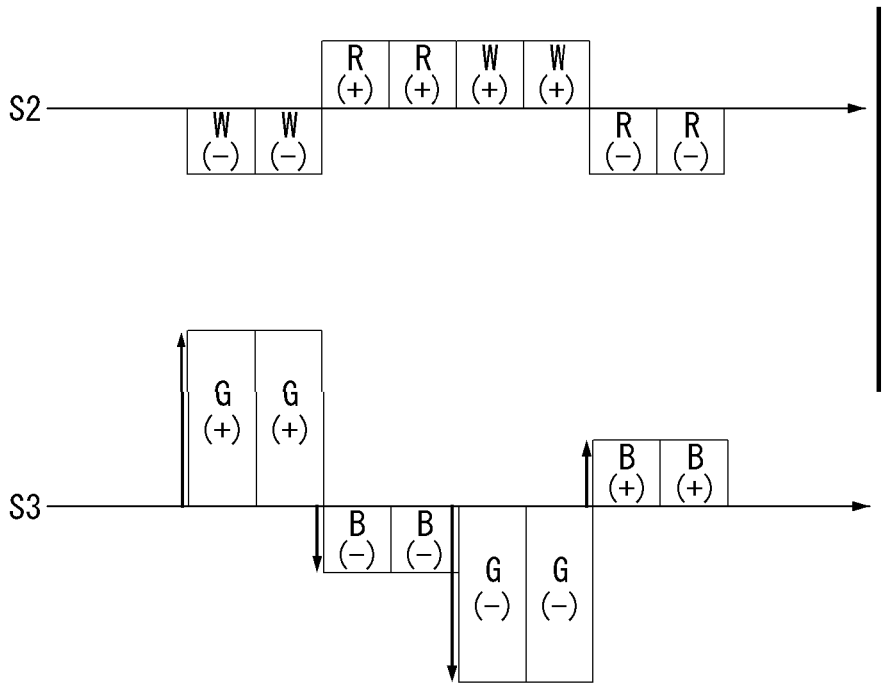
<White>

FIG. 11B



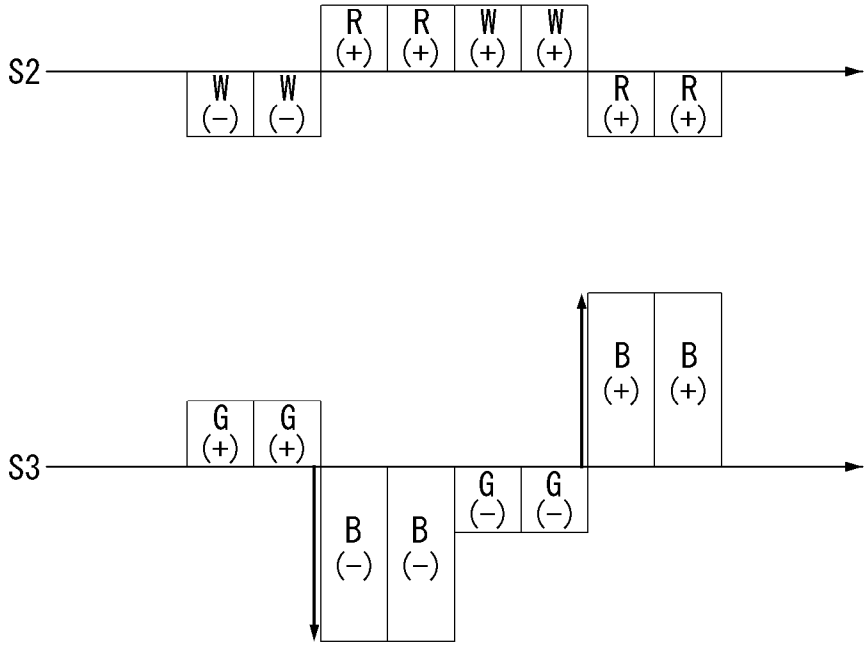
<Red>

FIG. 11C



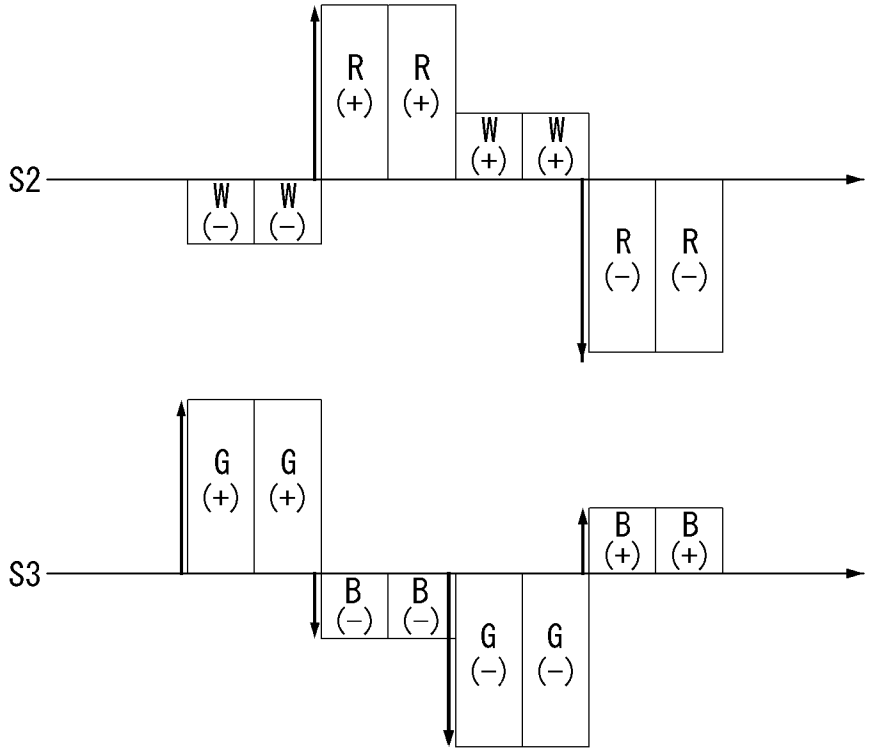
<Green>

FIG. 11D



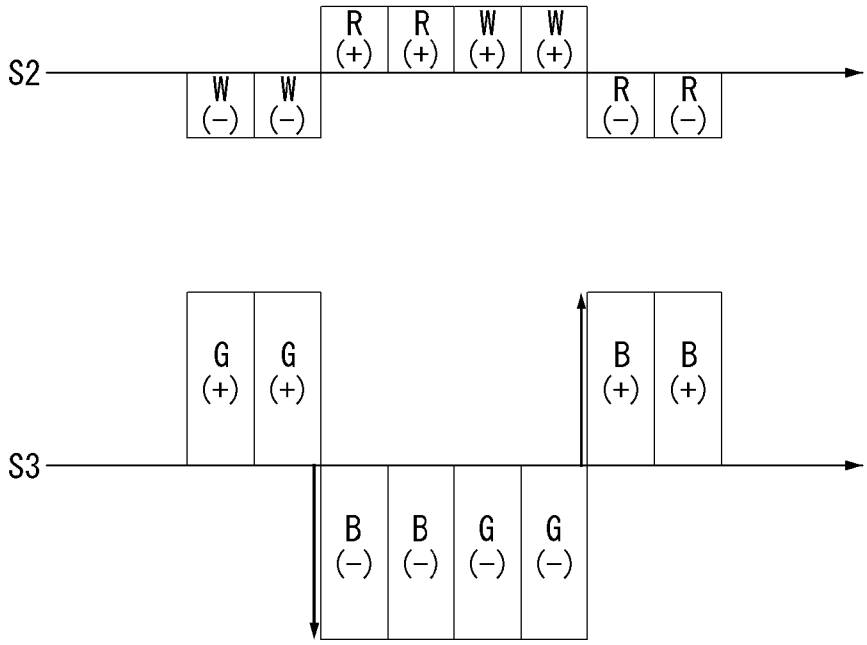
<Blue>

FIG. 11E



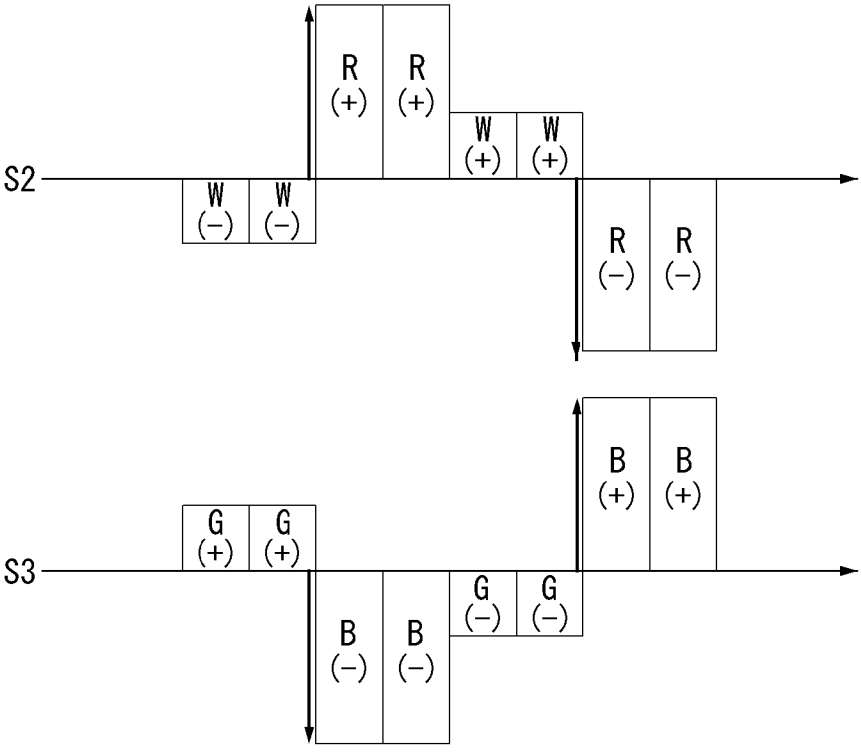
<Yellow>

FIG. 11F



<Cyan>

FIG. 11G



<Magenta>

FIG. 12

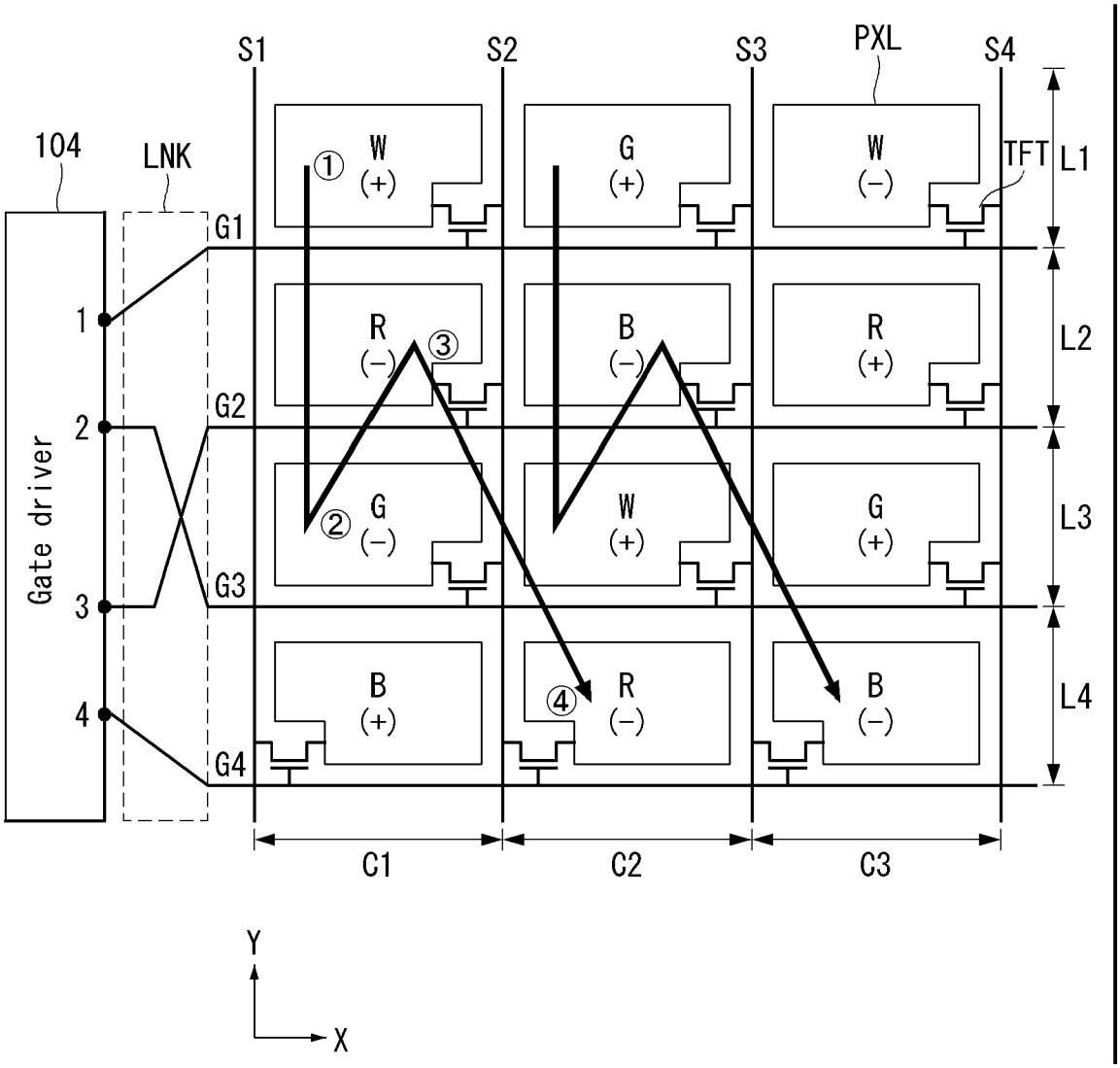

S1
S2
S3
PXL
S4
104
LNK
TFT
L1
L2
L3
L4
G1
G2
G3
G4
Gate driver
1
2
3
4
W (+)
G (+)
W (−)
R (−)
B (−)
R (+)
G (−)
W (+)
G (+)
B (+)
R (−)
B (−)
①
②
③
④
C1
C2
C3
Y
X

FIG. 13

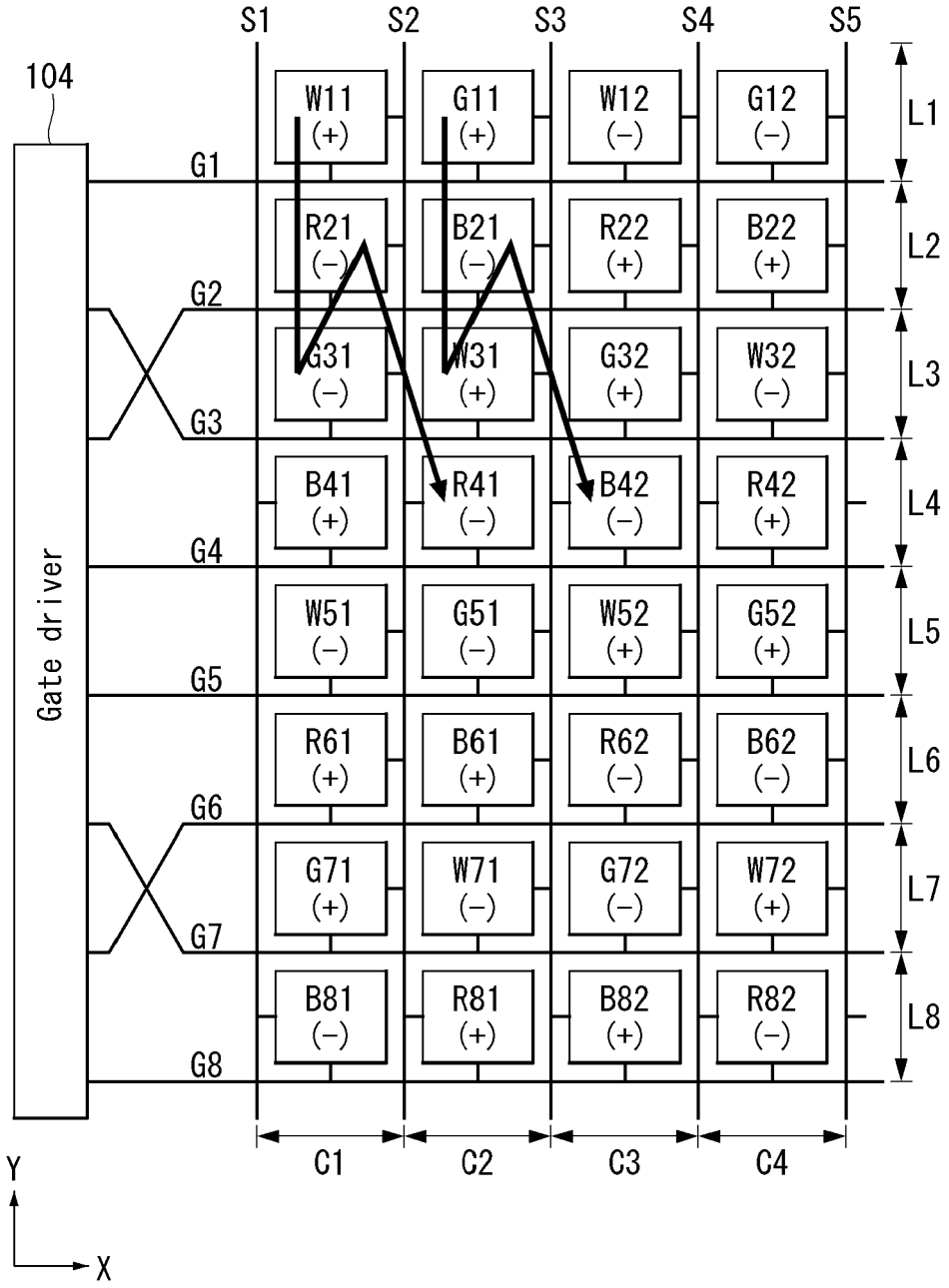

S1
S2
S3
S4
S5
104
Gate driver
G1
G2
G3
G4
G5
G6
G7
G8
W11 (+)
G11 (+)
W12 (−)
G12 (−)
R21 (−)
B21 (−)
R22 (+)
B22 (+)
G31 (−)
W31 (+)
G32 (+)
W32 (−)
B41 (+)
R41 (−)
B42 (−)
R42 (+)
W51 (−)
G51 (−)
W52 (+)
G52 (+)
R61 (+)
B61 (+)
R62 (−)
B62 (−)
G71 (+)
W71 (−)
G72 (−)
W72 (+)
B81 (−)
R81 (+)
B82 (+)
R82 (−)
L1
L2
L3
L4
L5
L6
L7
L8
C1
C2
C3
C4
Y
X

FIG. 14

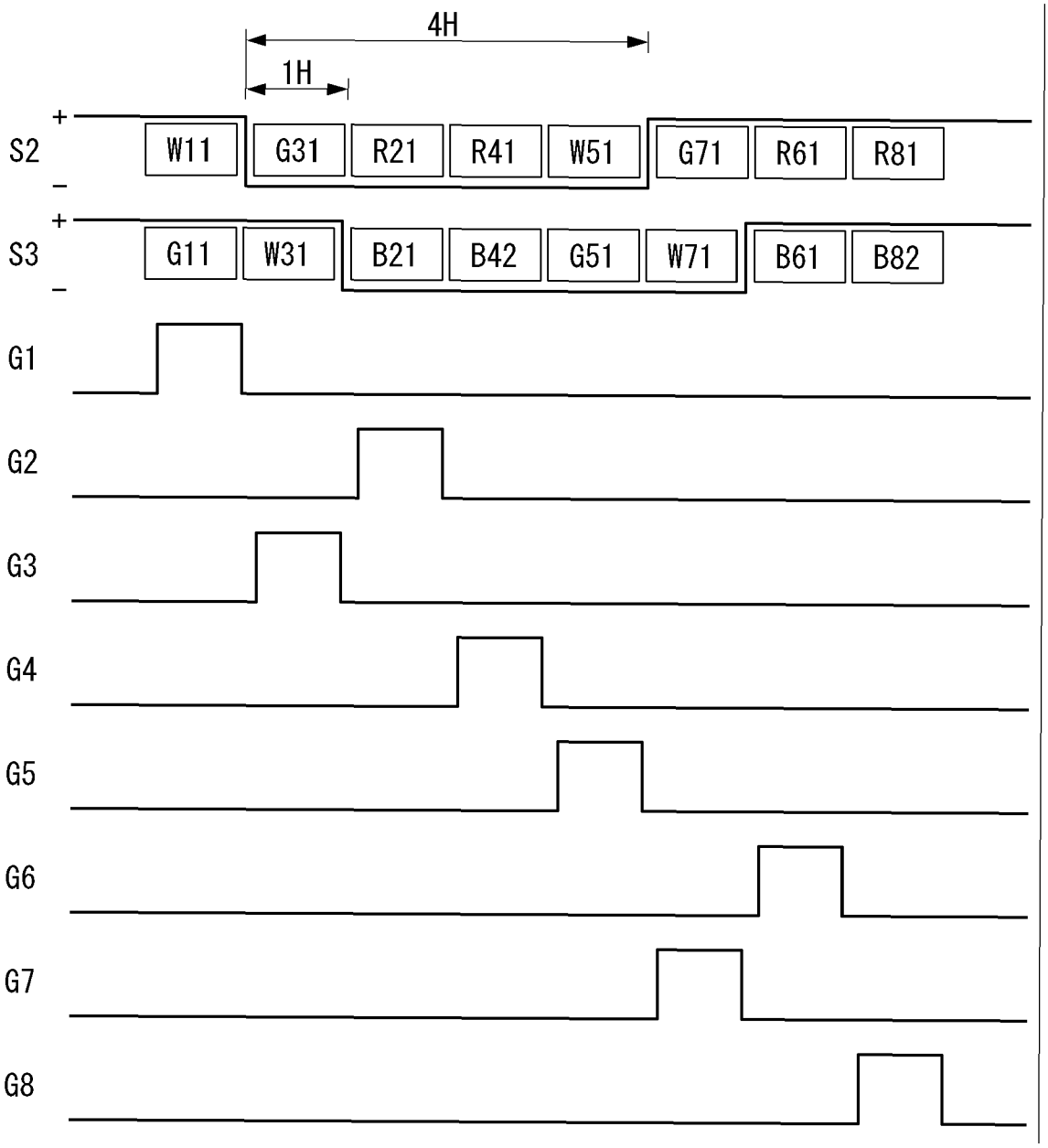
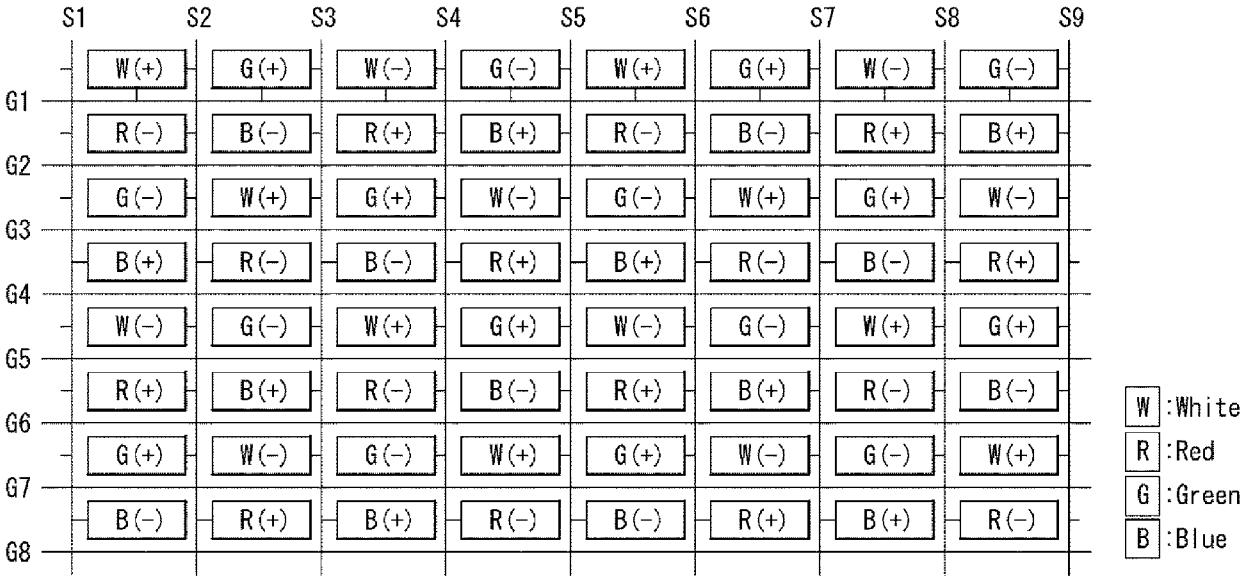
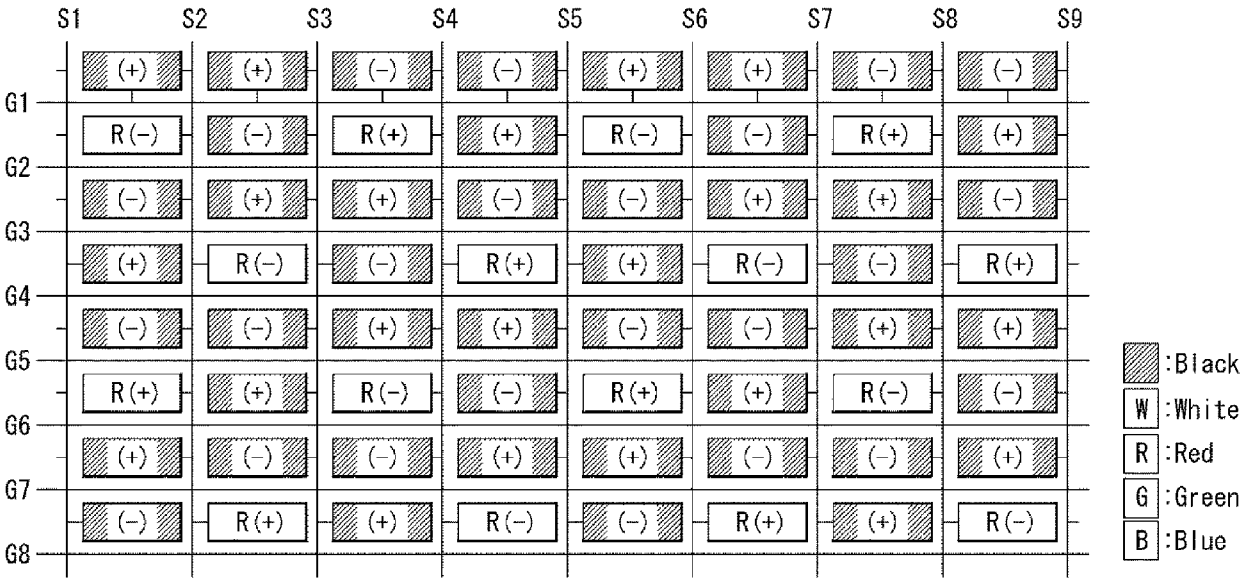

4H
1H
S2
+
−
W11
G31
R21
R41
W51
G71
R61
R81
S3
+
−
G11
W31
B21
B42
G51
W71
B61
B82
G1
G2
G3
G4
G5
G6
G7
G8

FIG. 15A



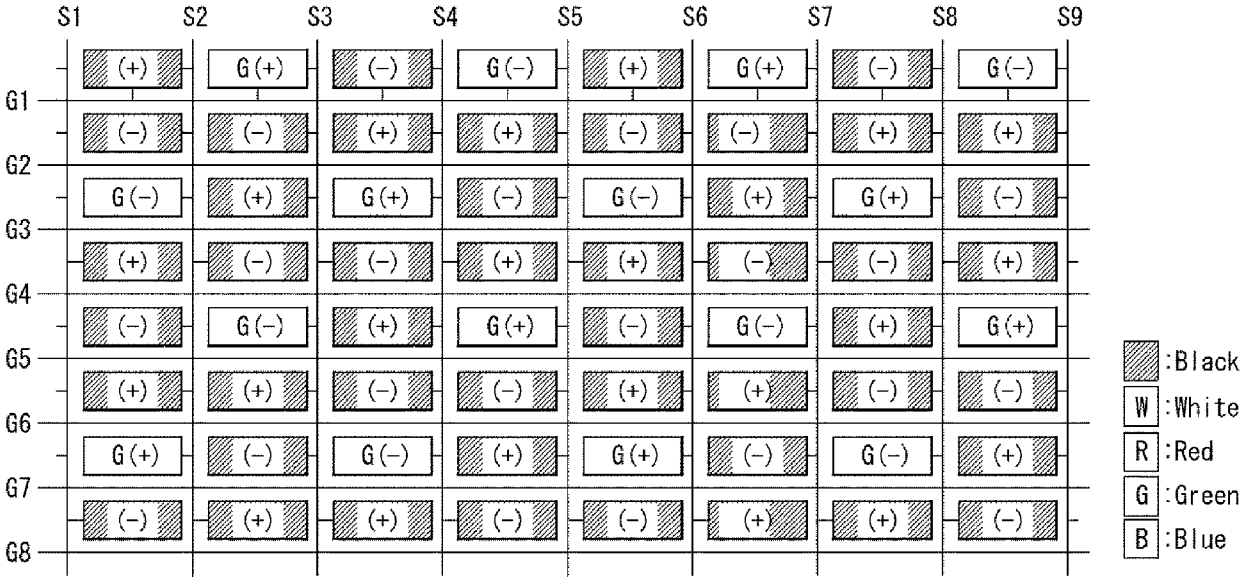
<White>

FIG. 15B


S1
S2
S3
S4
S5
S6
S7
S8
S9
G1
G2
G3
G4
G5
G6
G7
G8
:Black
W :White
R :Red
G :Green
B :Blue

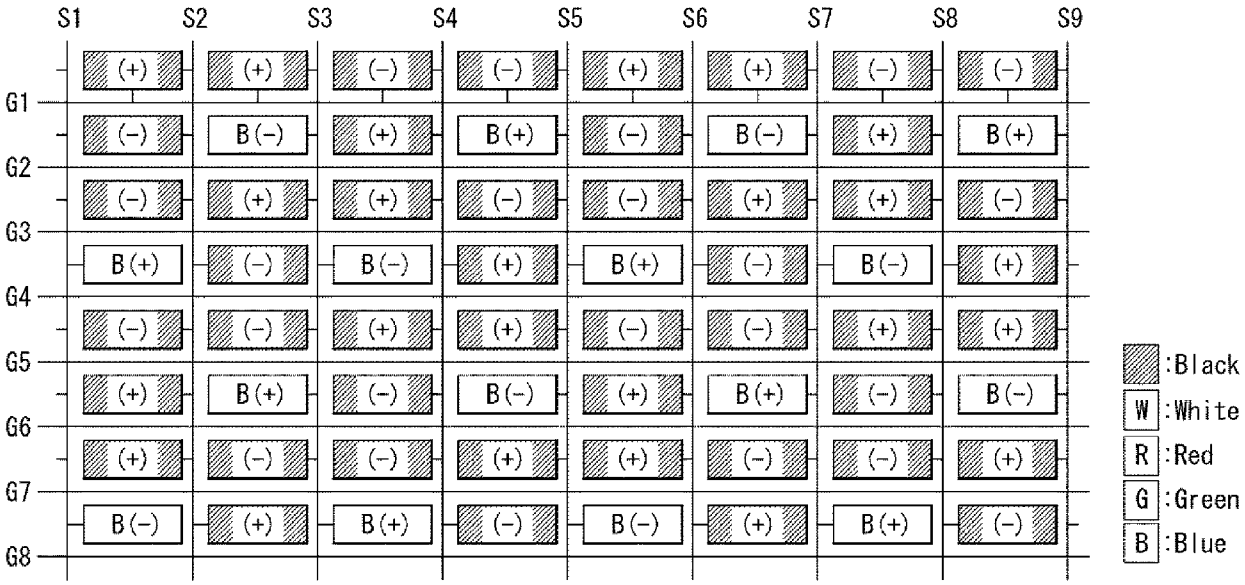
<Red>

FIG. 15C



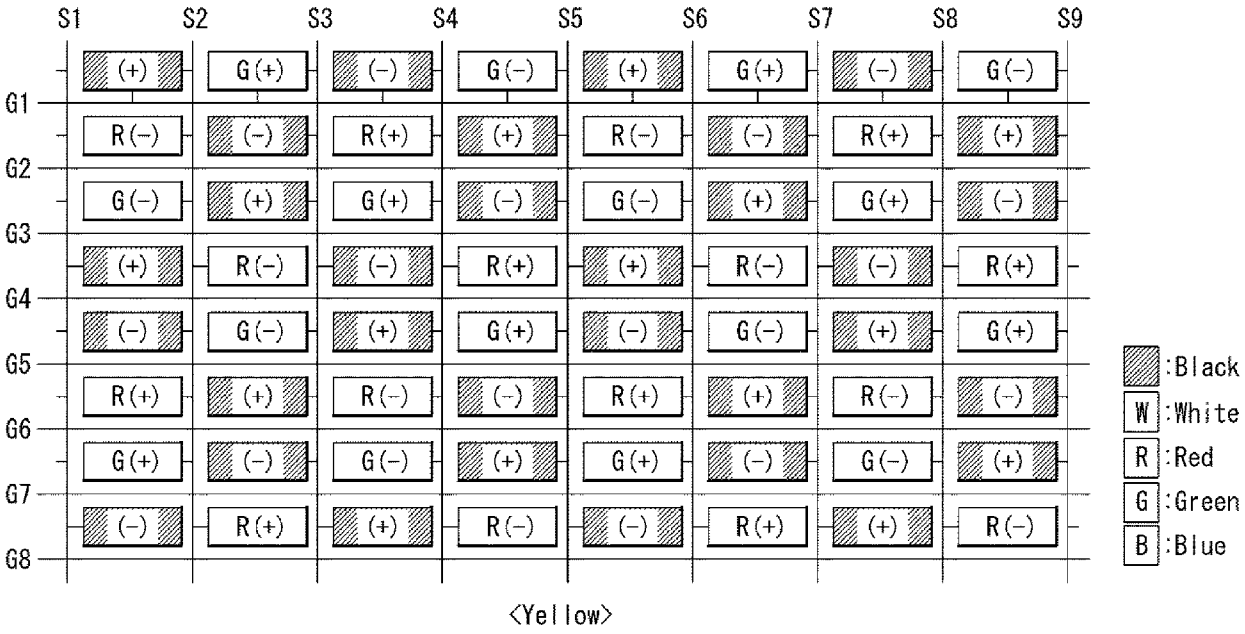
<Green>

FIG. 15D


S1
S2
S3
S4
S5
S6
S7
S8
S9
G1
G2
G3
G4
G5
G6
G7
G8
(+)
(-)
B(+)
B(-)
:Black
W :White
R :Red
G :Green
B :Blue

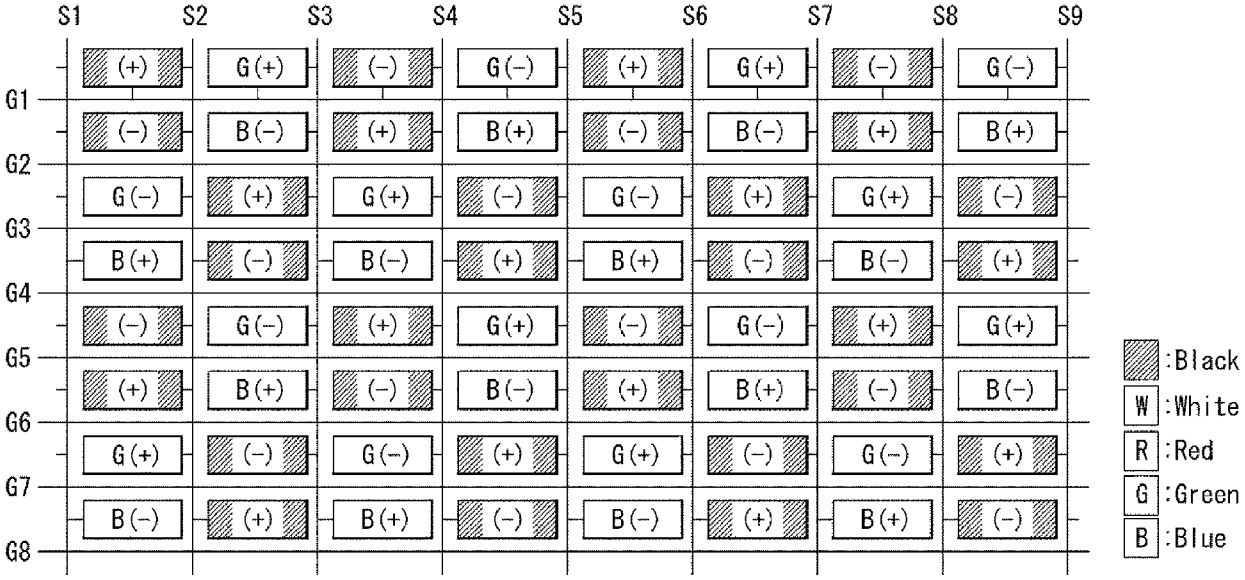
<Blue>

FIG. 15E



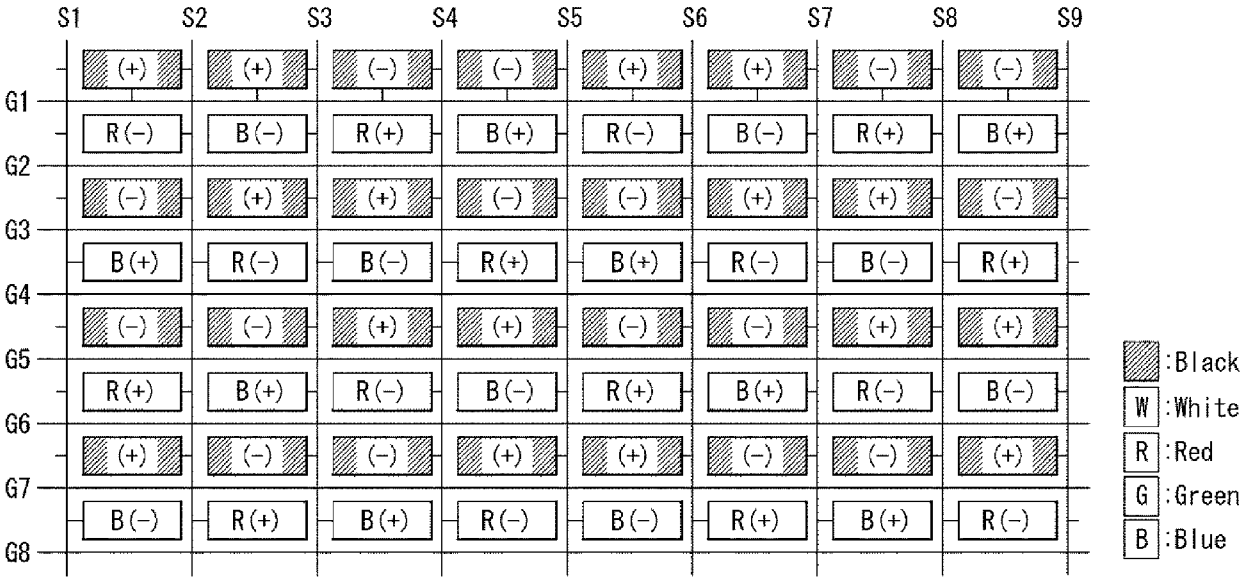
<Yellow>

FIG. 15F


S1
S2
S3
S4
S5
S6
S7
S8
S9
G1
G2
G3
G4
G5
G6
G7
G8
:Black
W :White
R :Red
G :Green
B :Blue

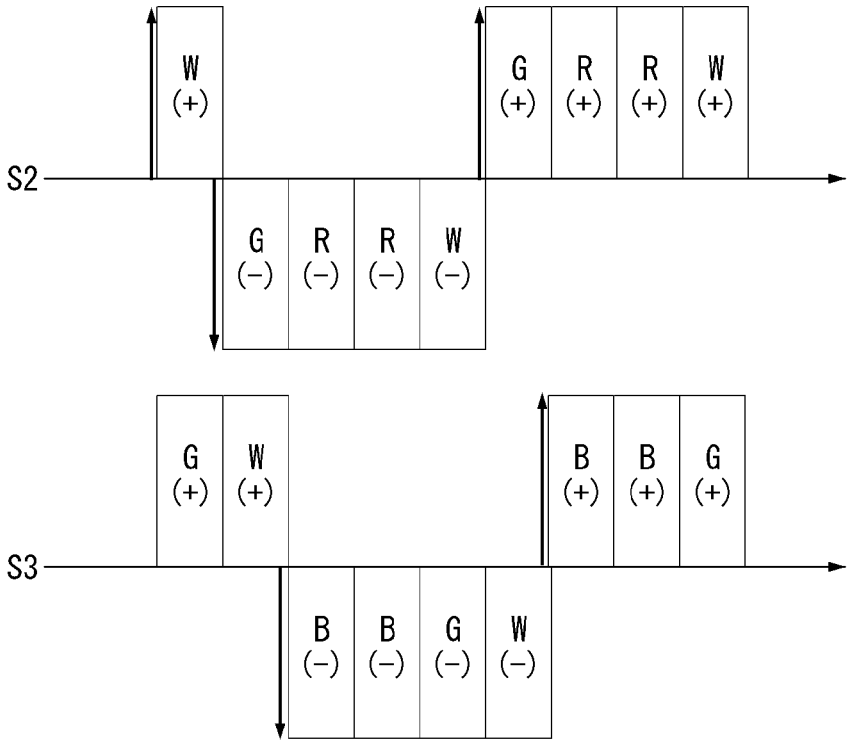
<Cyan>

FIG. 15G



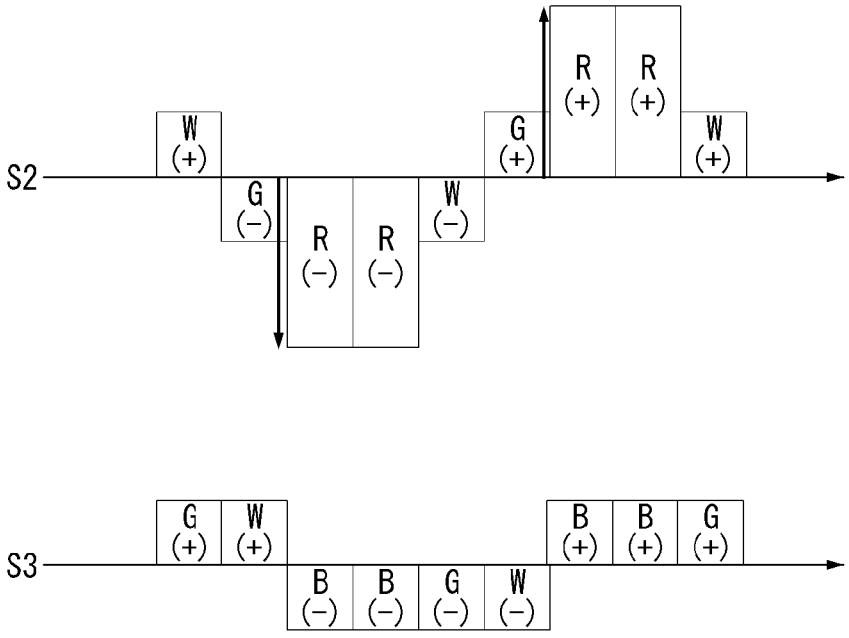
<Magenta>

FIG. 16A



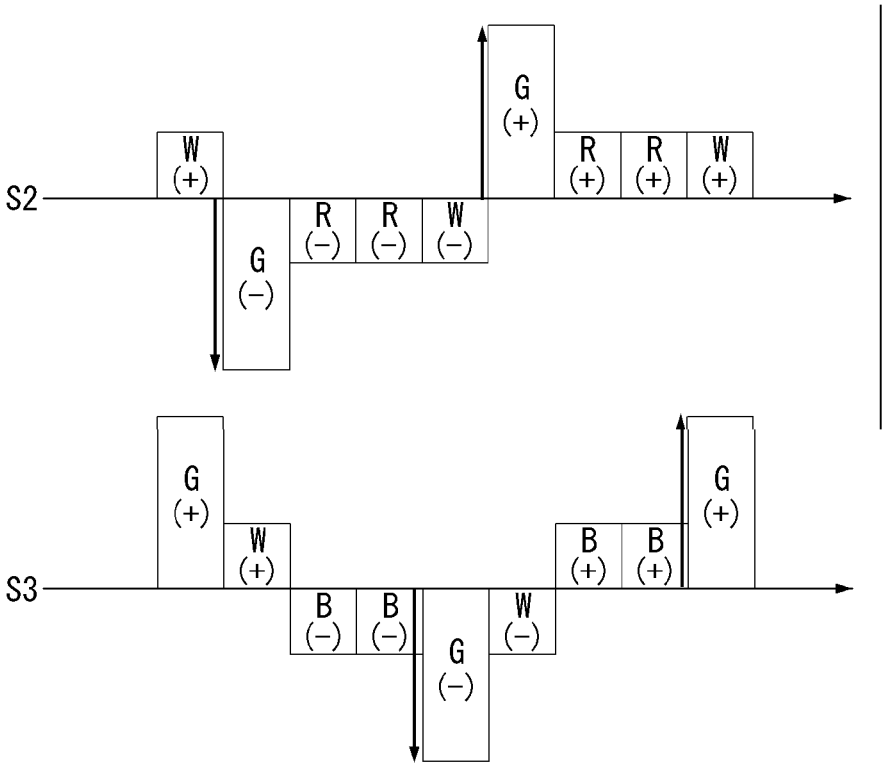
<White>

FIG. 16B



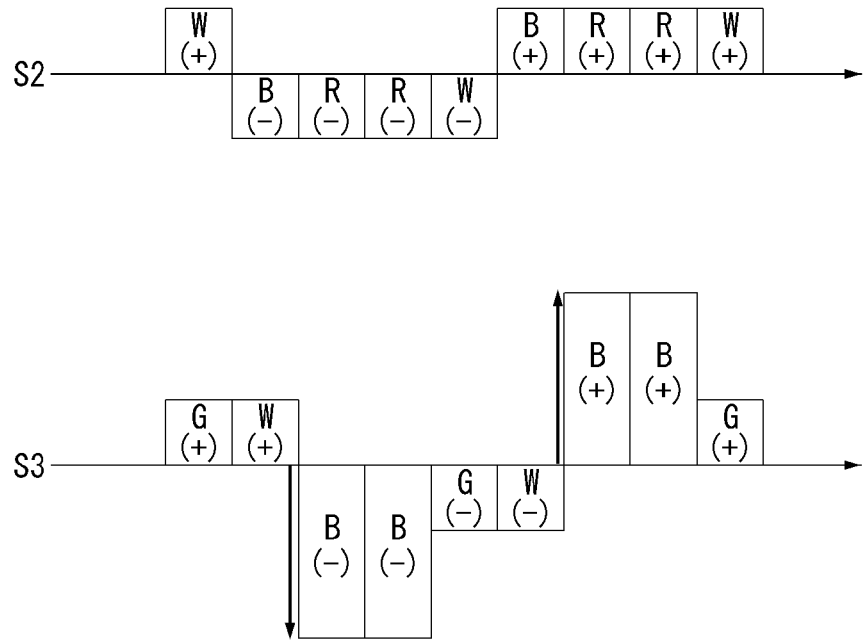
<Red>

FIG. 16C



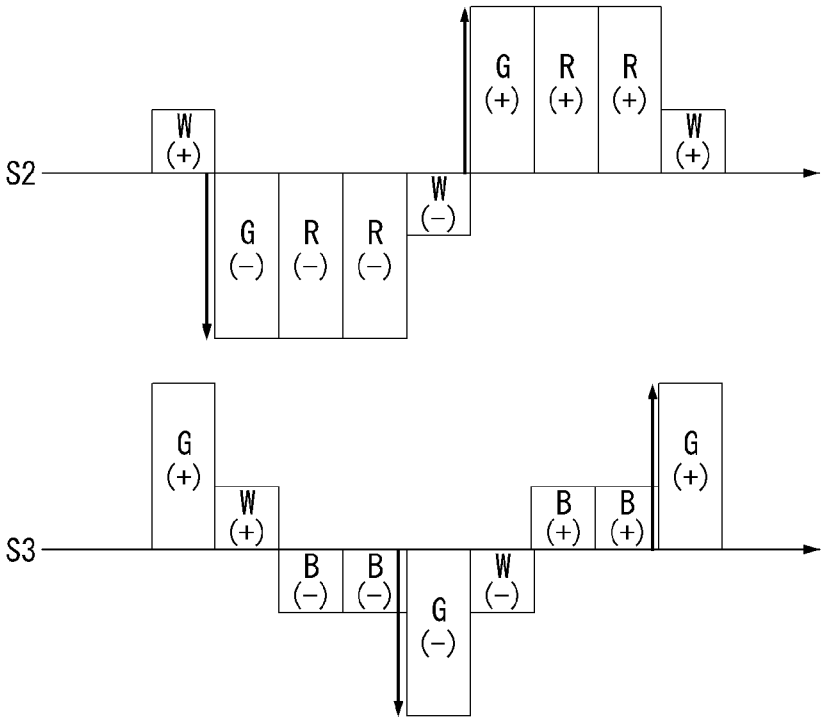
<Green>

FIG. 16D



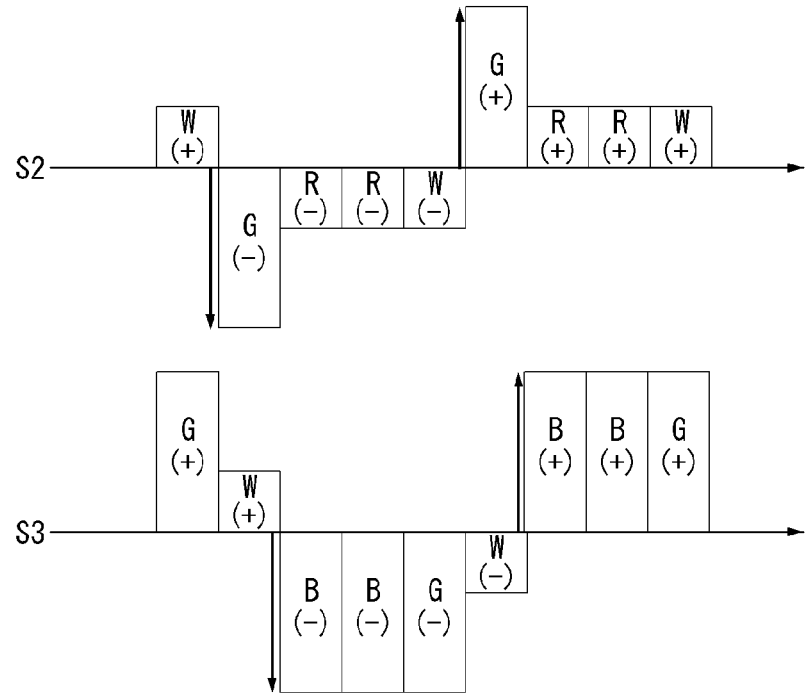
<Blue>

FIG. 16E



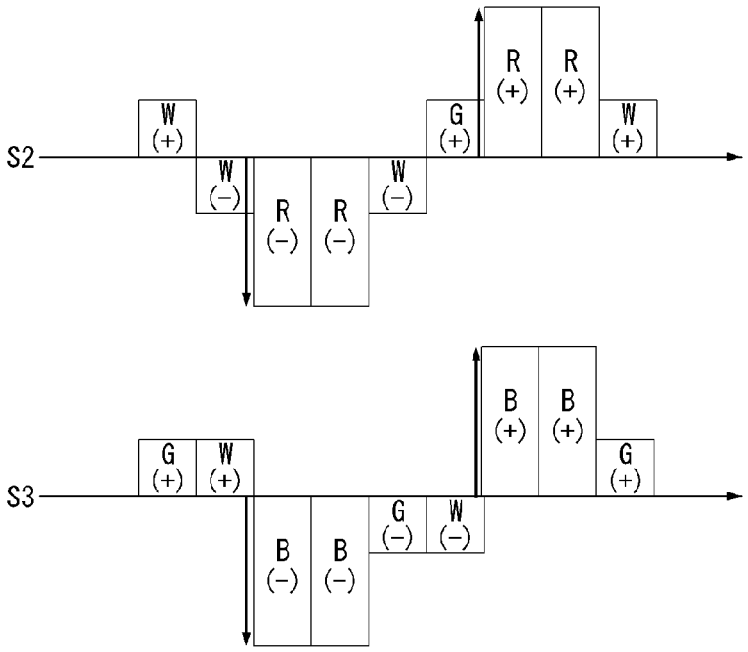
<Yellow>

FIG. 16F



<Cyan>

FIG. 16G



<Magenta>

FIG. 17

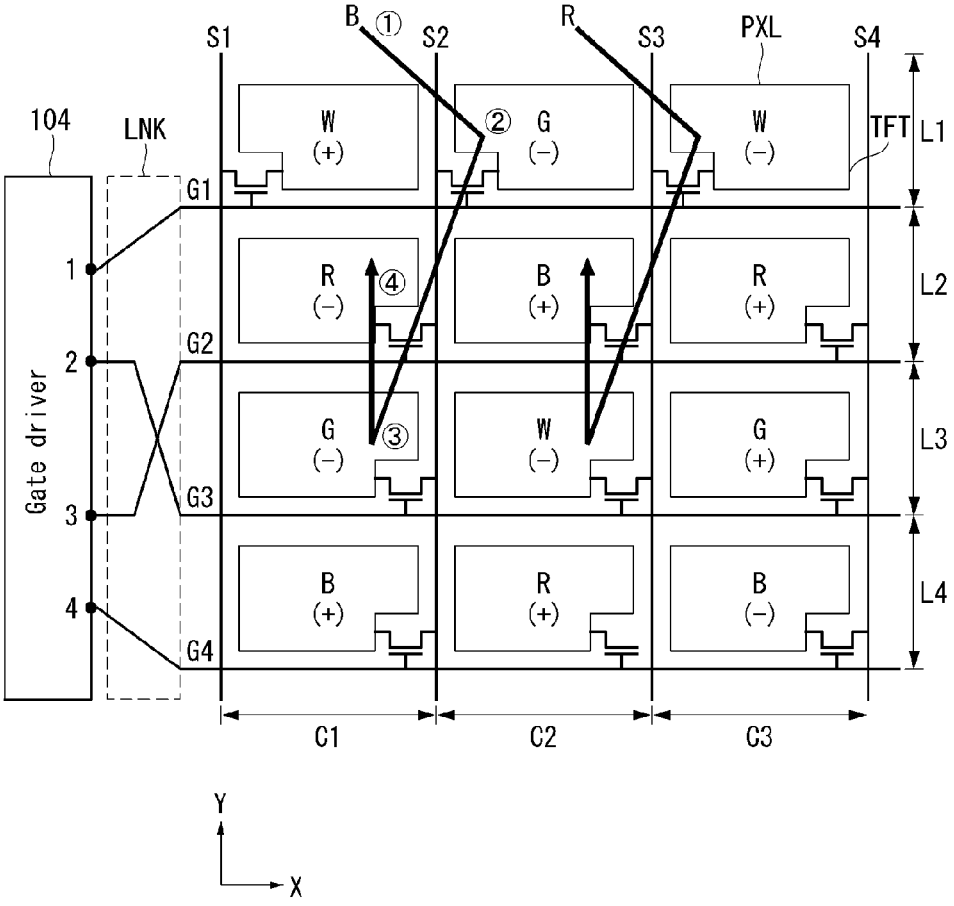


FIG. 18

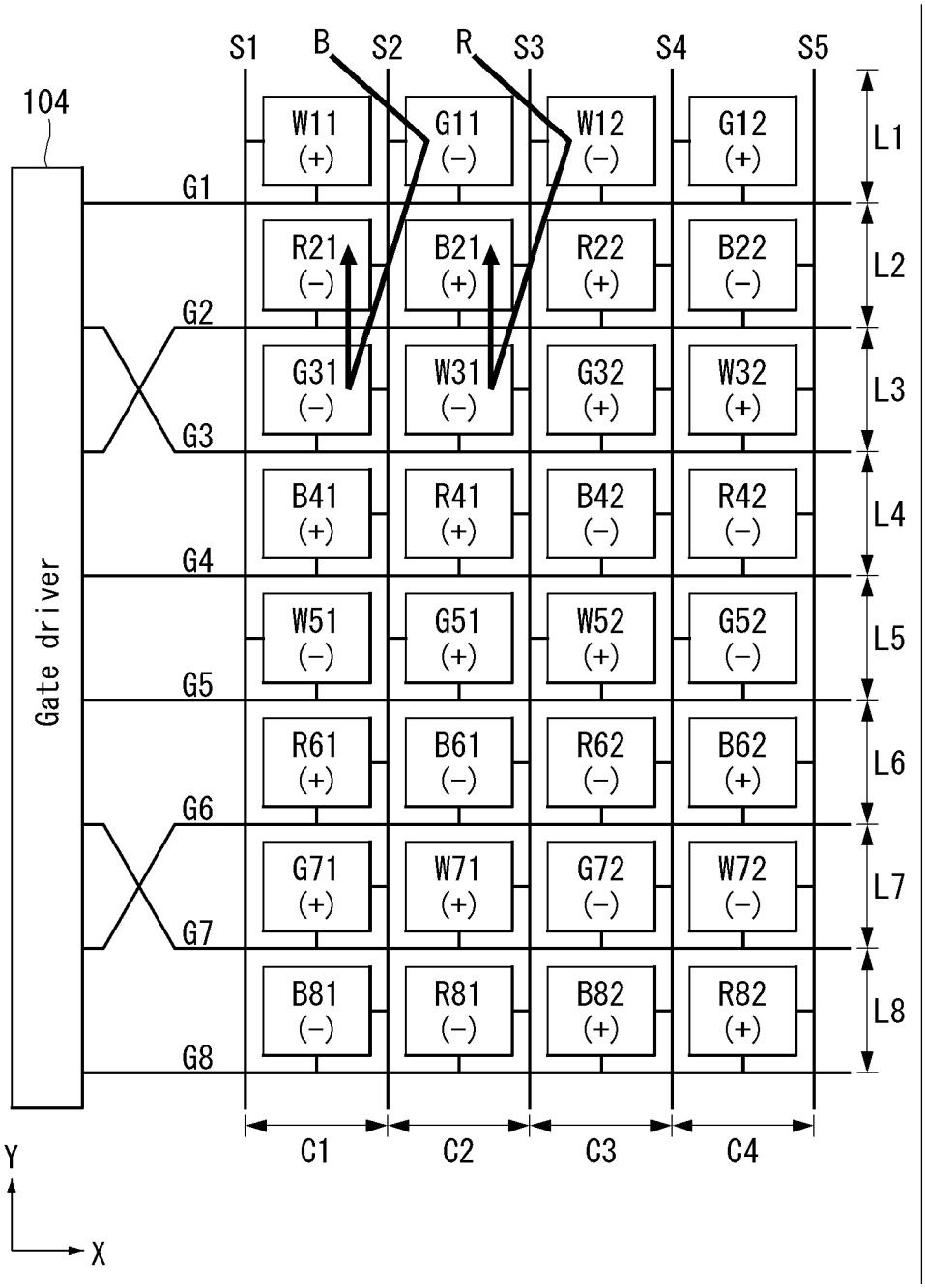

S1
B
S2
R
S3
S4
S5
104
W11 (+)
G11 (−)
W12 (−)
G12 (+)
L1
G1
R21 (−)
B21 (+)
R22 (+)
B22 (−)
L2
G2
G31 (−)
W31 (−)
G32 (+)
W32 (+)
L3
G3
B41 (+)
R41 (+)
B42 (−)
R42 (−)
L4
G4
W51 (−)
G51 (+)
W52 (+)
G52 (−)
L5
G5
R61 (+)
B61 (−)
R62 (−)
B62 (+)
L6
G6
G71 (+)
W71 (+)
G72 (−)
W72 (−)
L7
G7
B81 (−)
R81 (−)
B82 (+)
R82 (+)
L8
G8
Gate driver
C1
C2
C3
C4
Y
X

FIG. 19

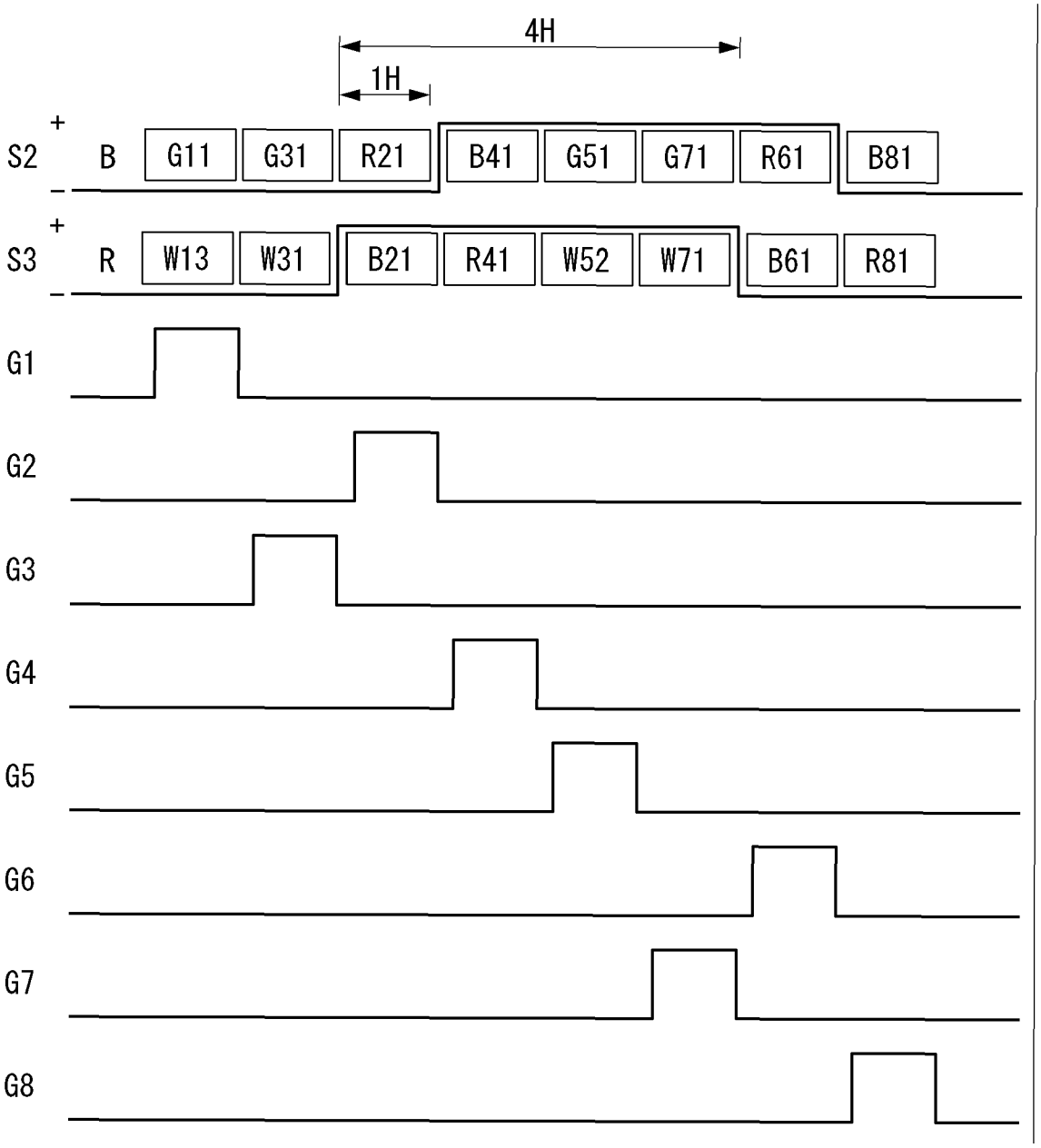
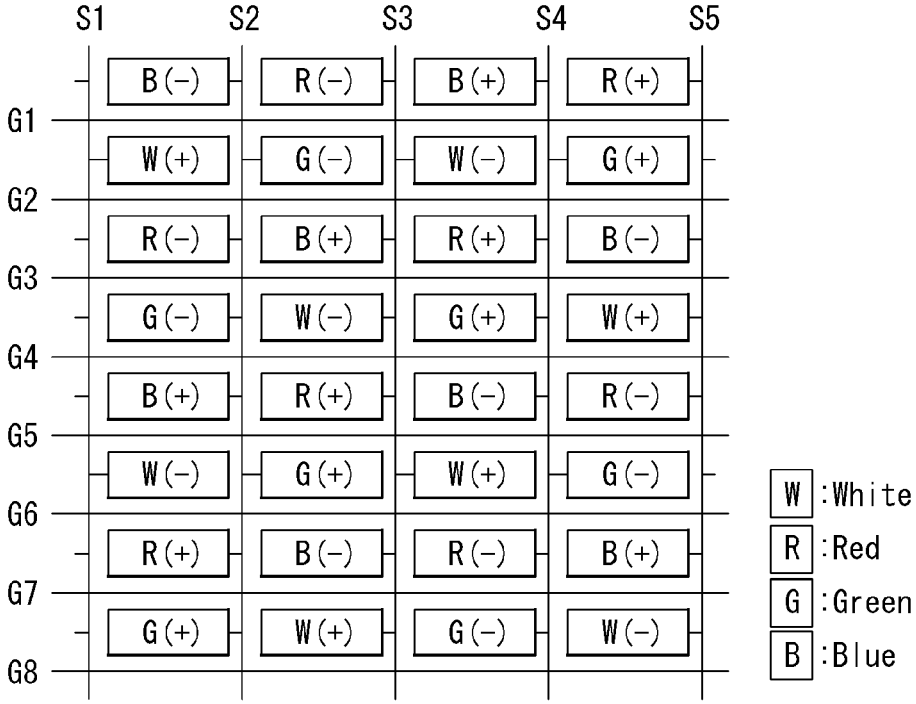
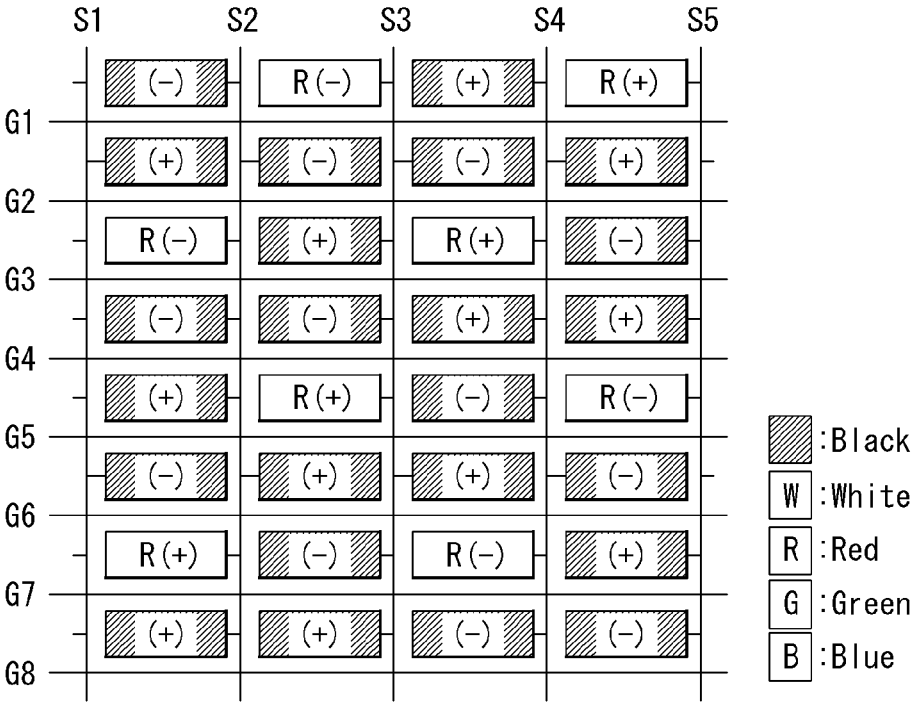

4H
1H
S2
+
B
G11
G31
R21
B41
G51
G71
R61
B81
−
S3
+
R
W13
W31
B21
R41
W52
W71
B61
R81
−
G1
G2
G3
G4
G5
G6
G7
G8

FIG. 20A



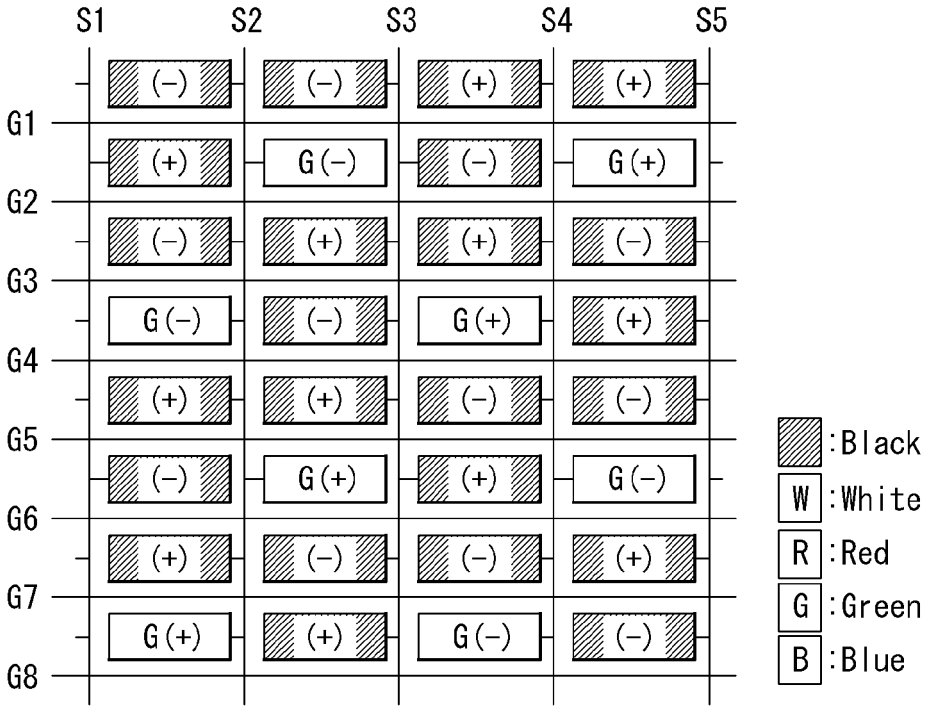
<White>

FIG. 20B



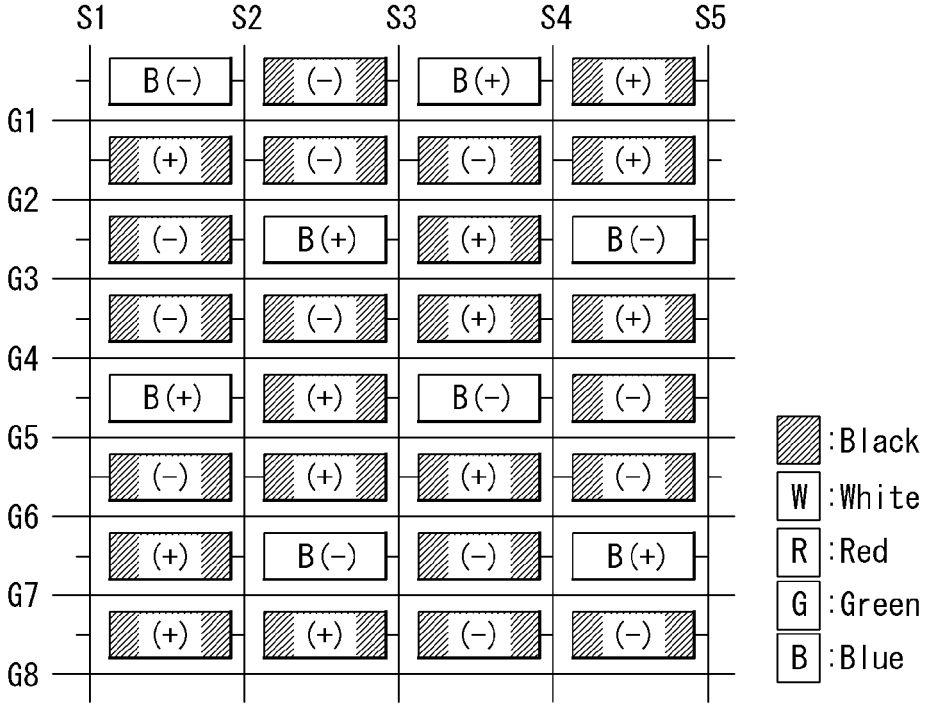
<Red>

FIG. 20C



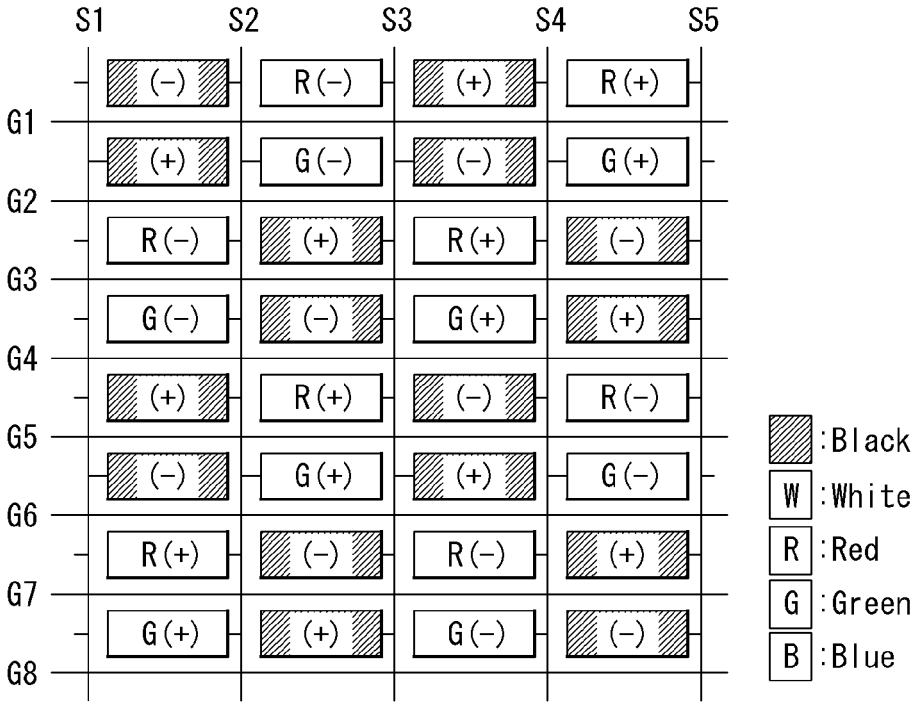
<Green>

FIG. 20D



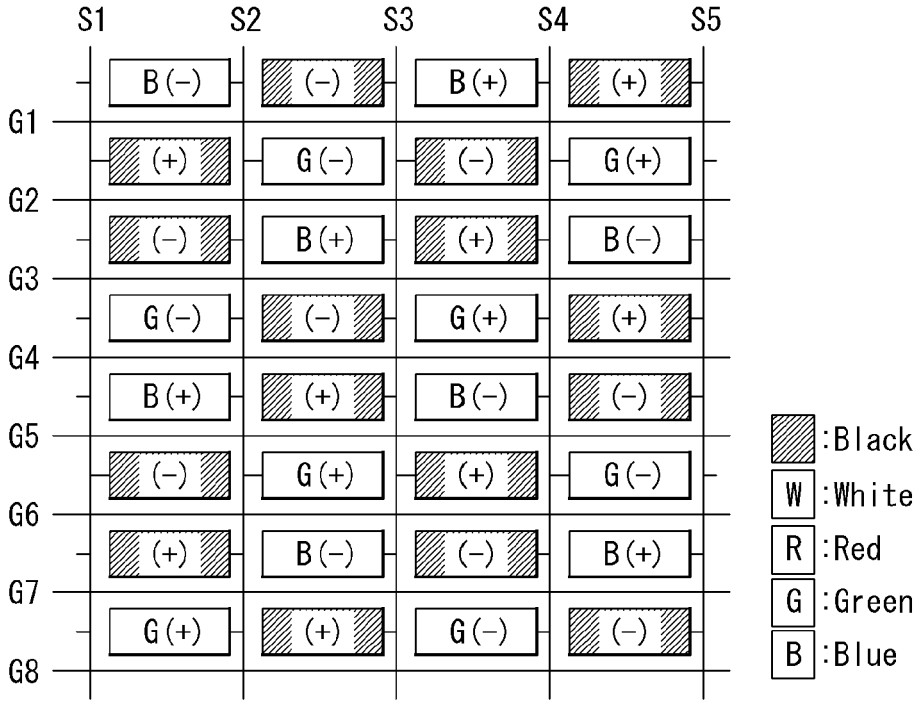
<Blue>

FIG. 20E



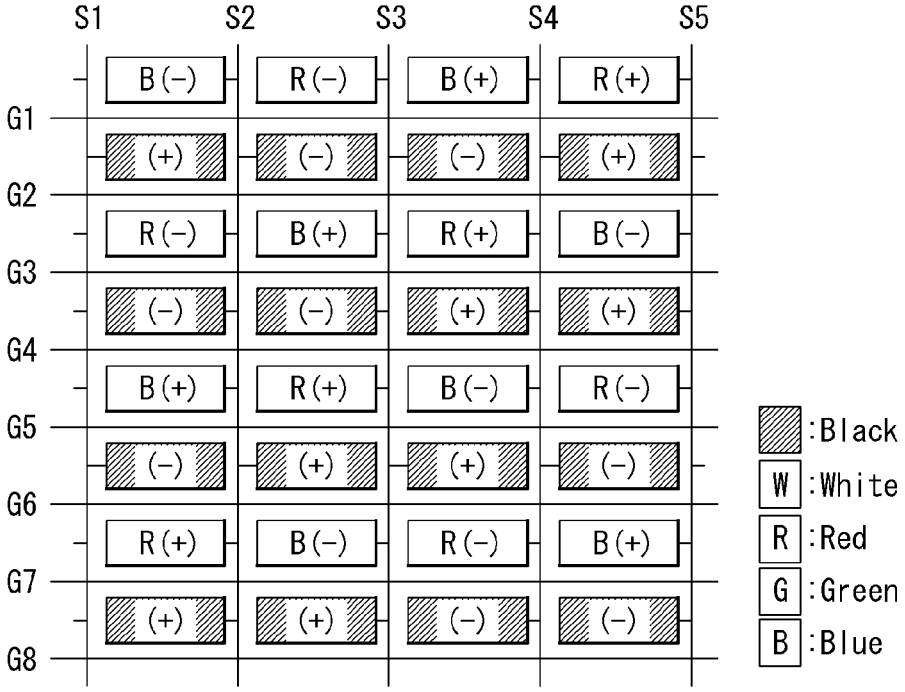
<Yellow>

FIG. 20F



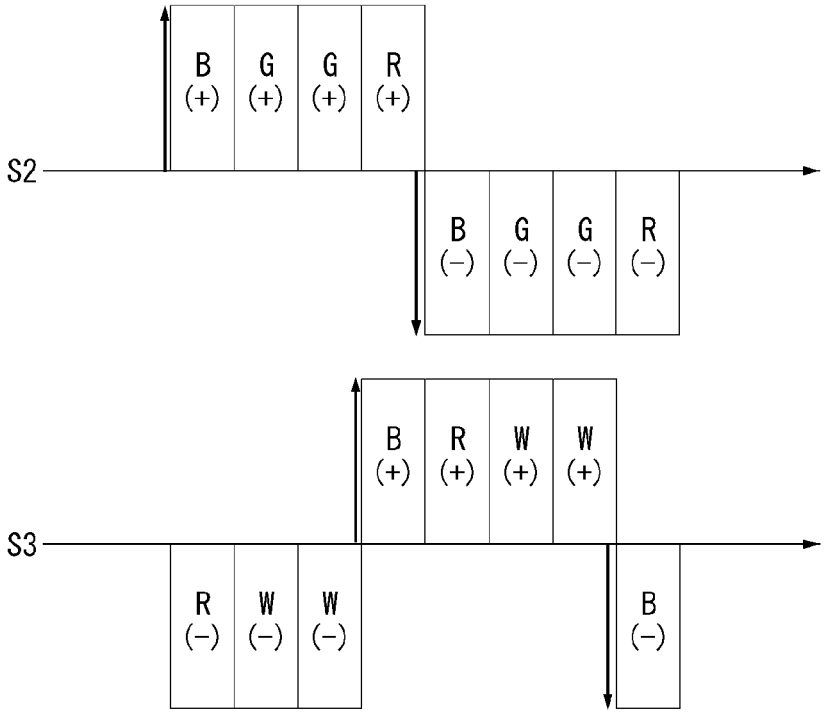
<Cyan>

FIG. 20G



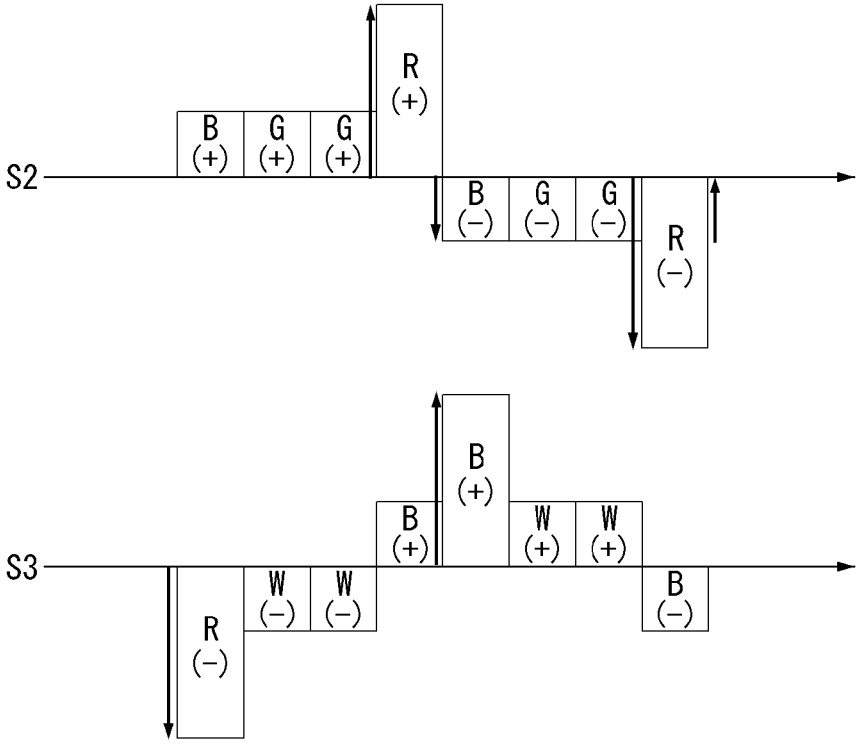
<Magenta>

FIG. 21A



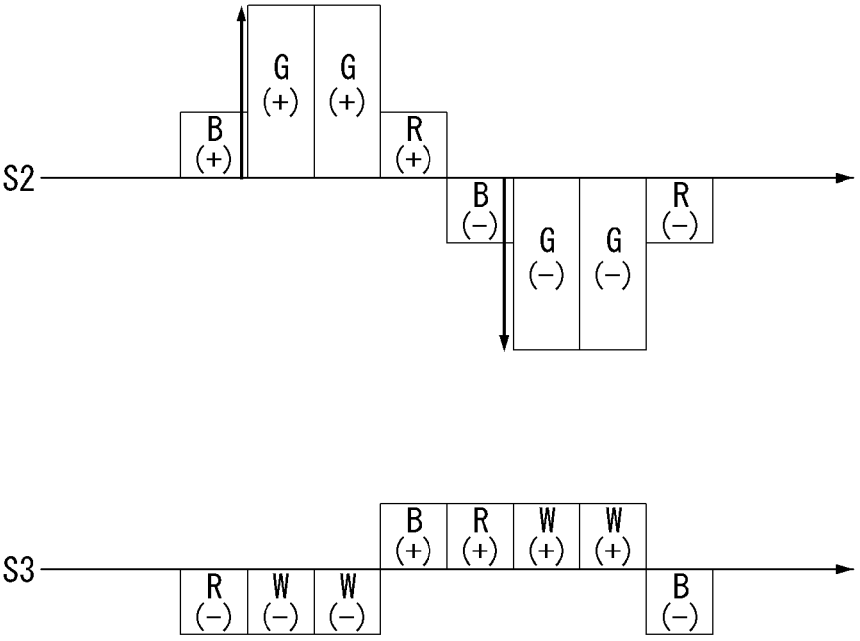
<White>

FIG. 21B



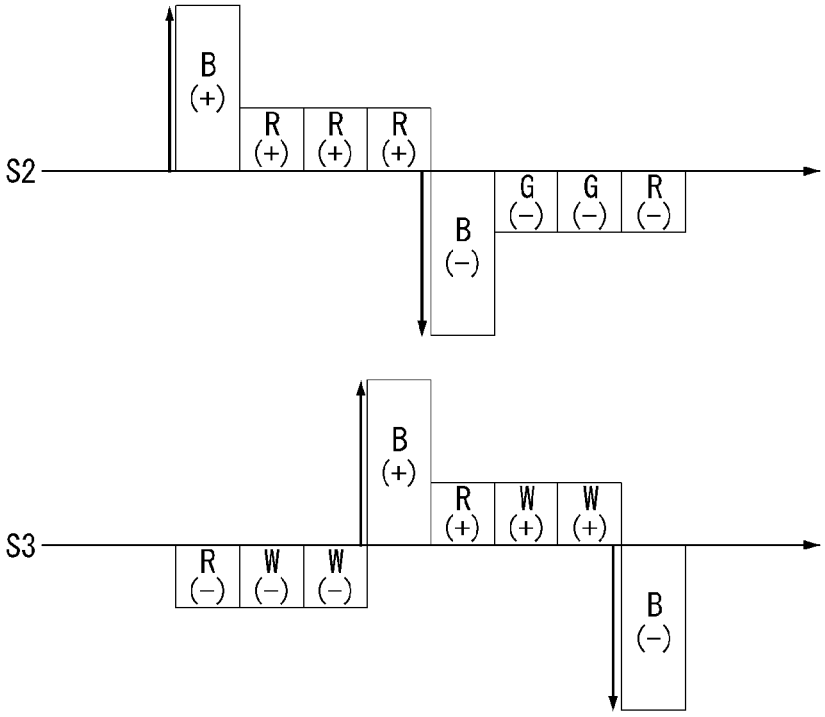
<Red>

FIG. 21C



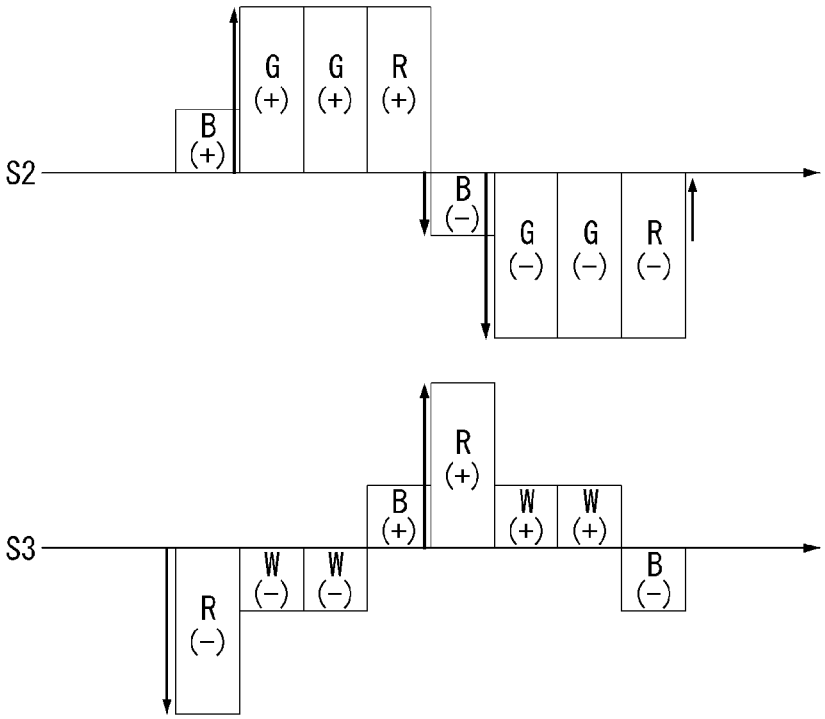
<Green>

FIG. 21D



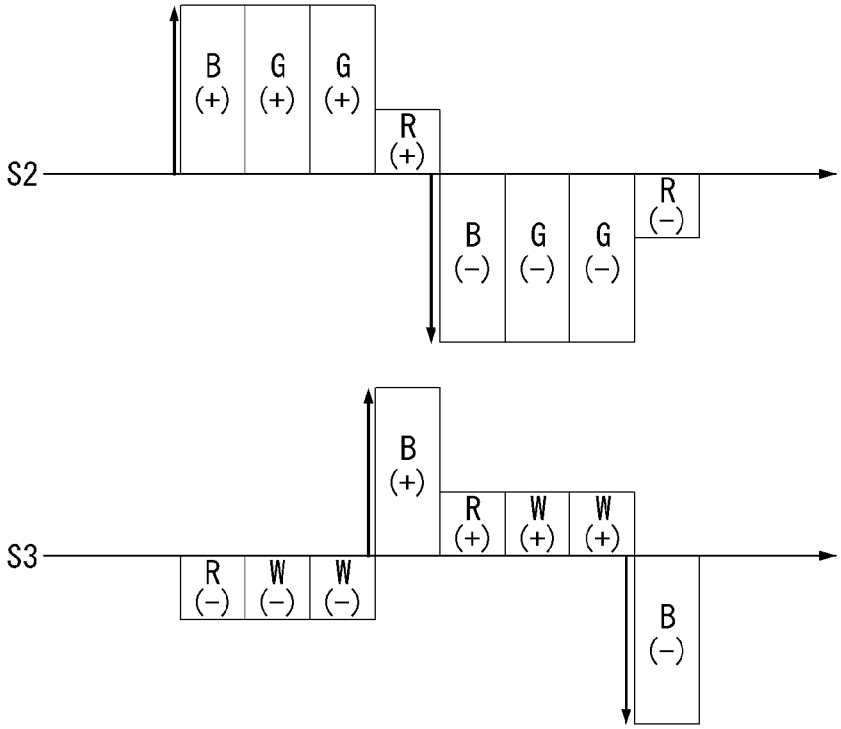
<Blue>

FIG. 21E



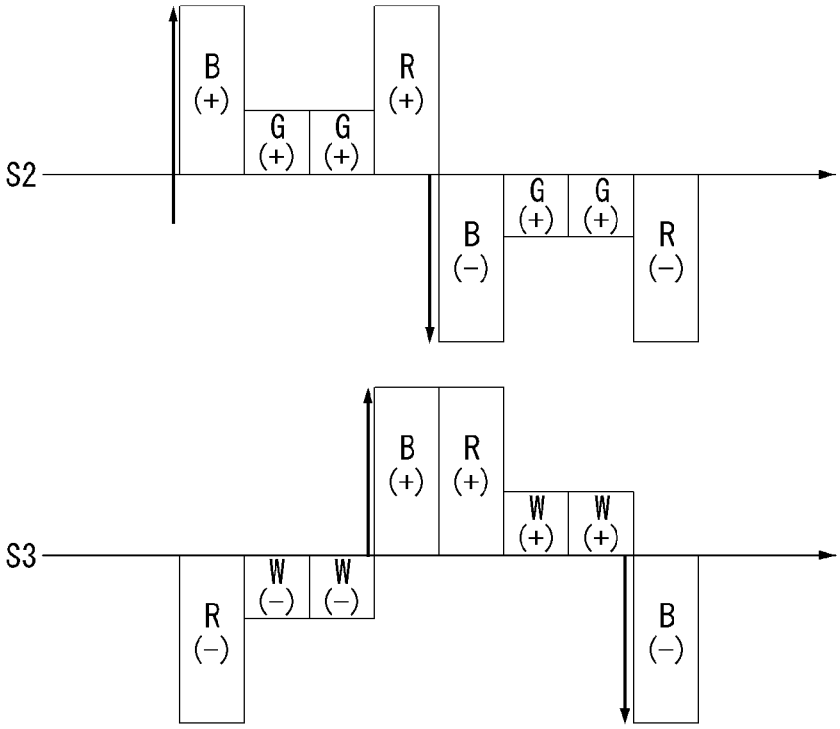
<Yellow>

FIG. 21F



<Cyan>

FIG. 21G



<Magenta>

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EUROPEAN SEARCH REPORT

Application Number
EP 17 17 3175

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X Y	CN 103 185 996 A (SHANGHAI AVIC OPTOELECTRONICS) 3 July 2013 (2013-07-03) * paragraph [0001] - paragraph [0039]; figures 1,2 * -----	1-3,10, 14 4-9, 11-13,15	INV. G09G3/36
Y	US 2015/379947 A1 (SANG WOOKYU [KR] ET AL) 31 December 2015 (2015-12-31) * paragraph [0051] - paragraph [0143]; figures 3, 10, 12, 19-20 * -----	11,13	
Y	EP 2 953 127 A2 (SAMSUNG DISPLAY CO LTD [KR]) 9 December 2015 (2015-12-09) * paragraph [0024] - paragraph [0093]; figures 3-15 * -----	5-9,12, 13	
Y	EP 2 998 955 A2 (LG DISPLAY CO LTD [KR]) 23 March 2016 (2016-03-23) * paragraph [0047]; figure 3 * * paragraph [0056]; figure 5 * -----	4,15	
			TECHNICAL FIELDS SEARCHED (IPC) G09G

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
Munich	9 October 2017	Gartlan, Michael

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

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Application Number
EP 17 17 3175

CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing claims for which payment was due.

☐ Only part of the claims have been paid within the prescribed time limit. The present European search report has been drawn up for those claims for which no payment was due and for those claims for which claims fees have been paid, namely claim(s):

☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for those claims for which no payment was due.

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

see sheet B

☒ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.

☐ As all searchable claims could be searched without effort justifying an additional fee, the Search Division did not invite payment of any additional fee.

☐ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid, namely claims:

☐ None of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims, namely claims:

☐ The present supplementary European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims (Rule 164 (1) EPC).

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LACK OF UNITY OF INVENTION
SHEET B

Application Number
EP 17 17 3175

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

1. claims: 1-3, 10, 14

   a gate driver configured to supply gate pulses to the gate lines in synchronization with the data voltages, solving the problem of enabling a proper loading of the sub-pixels (par. 70)

   ---

2. claims: 4, 15

   the data driver is configured to supply the data lines with data voltages whose polarity is reversed on a cycle of every 4 horizontal periods, solving the problem of reducing heat/power (par. 61).

   ---

3. claims: 5-9, 12, 13

   the third-color- and fourth-color subpixels arranged on the (4i+4)th row lines comprise TFTs that are configured to supply data voltages from the data lines to the second side of the subpixels to the pixel electrodes, wherein the second side of the subpixels is opposite to the first side of that subpixel, solving the problem of improving image quality during polarity inversion (par. 63).

   ---

4. claim: 11

   the polarity of the data voltages is supplied to the odd-numbered data lines is reversed on data voltages of the fourth color, and the polarity of the data voltages supplied to the even-numbered data lines is reversed on data voltages of the second color, the fourth data voltage after reversal of the polarity of a data voltage supplied to each data line is a data voltage of the fourth color, and there is a difference of 1 horizontal period between the polarity reversal timing of data voltages supplied to the odd-numbered data lines and the polarity reversal timing of data voltages supplied to the even-numbered data lines ,wherein, among link lines connecting output channels of the gate driver and the gate lines , the link lines connecting the output channels of the second and third gate pulses and the second and third gate lines intersect so that the third gate pulse is applied to the second gate line after the second gate pulse is applied to the third gate line , solving the problem of applying gate pulses in a non-sequential manner efficiently (par.65).

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 17 17 3175

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
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09-10-2017

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		KR 20160033289 A	28-03-2016
		US 2016078826 A1	17-03-2016

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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

REFERENCES CITED IN THE DESCRIPTION

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- KR 1020050066429 **[0051]**
- KR 1020060011292 **[0051]**

专利名称(译)	液晶显示装置及其驱动方法		
公开(公告)号	EP3252753A1	公开(公告)日	2017-12-06
申请号	EP2017173175	申请日	2017-05-29
[标]申请(专利权)人(译)	乐金显示有限公司		
申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
当前申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
[标]发明人	SANG WOOKYU		
发明人	SANG, WOOKYU		
IPC分类号	G09G3/36		
CPC分类号	G02F1/1362 G09G3/3674 G09G3/3685 G09G3/3607 G09G3/3614 G09G3/3648 G09G3/3677 G09G3/3688 G09G2300/0426 G09G2300/0452 G09G2310/0213 G09G2310/0218 G02F1/13 G02F2001/1635 G09G3/3406 G09G3/3413 G09G3/364 G09G3/3659 G09G2320/0646		
审查员(译)	GARTLAN，MICHAEL		
优先权	1020160067776 2016-05-31 KR		
其他公开文献	EP3252753B1		
外部链接	Espacenet		

摘要(译)

公开了一种液晶显示装置及其驱动方法。第一颜色子像素布置在第（4i + 1）行线（i是正整数）和奇数列线相交的位置处，并且第二颜色子像素布置在（4i + 1）的位置处第n行和偶数列线相交。第三颜色子像素布置在第（4i + 2）行线和奇数列线相交的位置处，第四颜色子像素布置在第（4i + 2）行和偶数的位置处 - 编号的列线相交。

FIG. 3