(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 3 035 116 B1

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
04.03.2020 Bulletin 2020/10

(21) Application number: **15196000.2**

(22) Date of filing: **24.11.2015**

(51) Int Cl.:
G02F 1/1343 *(2006.01)* ***G02F 1/1362*** *(2006.01)*

(54) **FRINGE FIELD SWITCHING MODE LIQUID CRYSTAL DISPLAY DEVICE WITH RGBW PIXELS**

FRINGE-FELD-SCHALTMODUS-FLÜSSIGKRISTALLANZEIGETAFEL MIT RGBW-PIXELN

DISPOSITIF D'AFFICHAGE À CRISTAUX LIQUIDES EN MODE DE COMMUTATION DE CHAMP DE DISPERSION, COMPRENANT DES PIXELS RGBW

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR

(30) Priority: **17.12.2014 KR 20140182059**

(43) Date of publication of application:
22.06.2016 Bulletin 2016/25

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Description

[0001] The present application claims priority from Korean Patent Application No. 10-2014-0182059 filed on December 17, 2014.

BACKGROUND

Field of the Disclosure

[0002] The present application relates to a liquid crystal display device, and more particularly, to a fringe field switching mode liquid crystal display device.

Description of the Related Art

[0003] In general, an LCD device displays images by controlling light transmittance of liquid crystal with dielectric anisotropy using an electric field. Such an LCD device includes a color filter array substrate and a thin film transistor array substrate combined with having a liquid crystal layer therebetween. The color filter array substrate is provided with a color filter array, and the thin film transistor array substrate is provided with a thin film transistor array.

[0004] In order to improve a narrow viewing angle of the LCD device, a variety of new modes applicable to the LCD device are being researched and developed. In accordance therewith, LCD devices being driven in one of an in-plane switching (IPS) mode, an optically compensated birefringence (OCB) mode, a fringe field switching (FFS) mode and so on, are being used as wide viewing angle LCD devices.

[0005] Among the wide viewing angle LCD devices, the IPS mode LCD device enables a lateral electric field to be generated between a pixel electrode and a common electrode which are arranged on the same substrate. As such, major axes of liquid crystal molecules are aligned along a lateral direction parallel to the substrate. In accordance therewith, the IPS mode LCD device can provide a wider viewing angle compared to a twisted nematic (TN) mode LCD device of the related art.

[0006] Such an LCD device includes an LCD panel, a gate driver, a data driver and so on. The LCD panel includes a plurality of pixels arranged in a matrix shape. The gate driver is used to drive gate lines on the LCD panel. The data driver is used to drive data lines on the LCD panel.

[0007] Also, the FFS mode LCD device has been derived from the IPS mode LCD device. The FFS mode LCD device allows a pixel electrode and a common electrode to be formed from a transparent conductive material. As such, the FFS mode LCD device can optimize transmittance of a pixel region.

[0008] **Fig. 1A** is a planar view showing a pixel structure of an FFS mode LCD device according to the related art. **Fig. 1B** is a planar view showing a pixel structure of the related art which further includes a white sub-pixel and secures transmittance.

[0009] Referring to Fig. 1A, an LCD panel of the FFS mode LCD device according to the related art allows a single pixel to be configured with a red (R) sub-pixel SP (hereinafter, "red sub-pixel RSP"), a green (G) sub-pixel SP (hereinafter, "green sub-pixel GSP") and a blue (B) sub-pixel SP (hereinafter, "blue sub-pixel BSP) . A thin film transistor TFT used as a switching element is disposed in each of the sub-pixels SP.

[0010] Such an LCD panel adjusts light transmittances of the red, green and blue sub-pixels RSP, GSP and BSP, which are included in the single pixel P, by applying data signals to the red, green and blue sub-pixels RSP, GSP and BSP. In accordance therewith, the single pixel can display (or realize) a desired color.

[0011] Meanwhile, a recently required high definition LCD panel with the pixel structure of Fig. 1A cannot secure a sufficient transmittance. To address this matter, it is proposed another pixel structure which further includes a white (W) sub-pixel SP (hereinafter, "white sub-pixel WSP") as shown in Fig. 1B.

[0012] Actually, an FFS mode LCD device allows a single pixel to be configured with white, red, green and blue sub-pixels WSP, RSP, GSP and BSP as shown in Fig. 1B. The light transmittances of the sub-pixels SP are adjusted on the basis of data signals applied to the sub-pixels SP. As such, the FFS mode LCD device can display a full color image.

[0013] In this case, the white sub-pixel WSP is used to secure transmittance rather than enhance color reproduction properties. As such, the single pixel can secure sufficient brightness.

[0014] However, the related art LCD panel with the pixel structure of Fig. 1B must reduce areas of the red, green and blue sub-pixels RSP, GSP and BSP because of further including the white sub-pixel WSP. Due to this, it is difficult to reproduce desired colors.

[0015] In other words, the pixel P further including the white sub-pixel WSP can secure a sufficient transmittance, but must deteriorate color reproduction properties due to the area-reduced of each sub-pixel SP.

[0016] US 2006/0262262 A1 is entitled *"Liquid Crystal Display Device"* and discloses a pixel (P) (Figure 5) comprising a white sub-pixel (WSP) which is smaller than red, green and blue sub-pixels (RSP, GSP, BSP) in order to increase the

brightness and purity of the color sub-pixels. A thin film transistor (Tr) is formed in each sub-pixel area. Common electrodes (115) and pixel electrodes (163) are formed on the same substrate so that liquid crystal molecules are driven by an electric field parallel with the substrate to thereby improve the viewing angle. The common electrodes (115) and pixel electrodes (163) overlap each other (Figure 6).

[0017] US 2010/0002162 A1 is entitled *"Liquid Crystal Display Device"* and discloses asymmetric pixels (A, B) having different widths (AA, BB). The prior art document addresses the problem of capacitance imbalance caused by the different pixel sizes and solves that problem by increasing the size of the pixel electrode of the smaller pixel (B): *"branch electrodes"* are formed extending from the pixel electrode of the smaller pixel (B). The extending portions are covered by a light blocking film so as not to influence the image formation.

[0018] KR 2011 0044 107 A is entitled *"In-plane switching mode reflection and transmission type LCD device"* (translation) . According to Figure 3 of KR'107, the area of a white pixel electrode (160a) is smaller than the respective area of red, green and blue pixel electrodes (160b, 160c, 160d). Four thin film transistors (Tr1, Tr2, Tr3, Tr4) are arranged in regions adjacent to the top and bottom edges of the white (W) sub-pixel, i.e. in the four corners of the white sub-pixel.

SUMMARY

[0019] Accordingly, the present invention is directed to an FFS mode LCD device that substantially obviates one or more of problems due to the limitations and disadvantages of the related art.

[0020] An object of the present invention is to provide an FFS mode LCD device that is adapted to enhance a transmittance property of a pixel region by asymmetrically forming the area of a white sub-pixel WSP with respect to the areas of red, green and blue sub-pixels RSP, GSP and BSP.

[0021] Another object of the present invention is to provide an FFS mode LCD device that is adapted to prevent image quality defects due to different kickback voltages ΔVp from one another by enabling white, red, green and blue sub-pixels WSP, RSP, GSP and BSP with asymmetric areas to have the same storage capacitance through a compensation of a storage capacitor.

[0022] Another object of the present invention is to provide a fringe field switching mode liquid crystal display device that is adapted to prevent deterioration of the image quality by compensating for a storage capacitance of a white sub-pixel region.

[0023] Additional features and advantages of the embodiments will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0024] To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described, an FFS mode LCD device comprises the features of claim 1. As such, the white, red, green and blue sub-pixels with asymmetric areas can have the same storage capacitance through a compensation of a storage capacitor. Therefore, the image quality defects caused by different kickback voltages ΔVp can be prevented.

[0025] The areas of the red, green and blue sub-pixels are larger than that of the white sub-pixel.

[0026] In one or more embodiments, the white and green sub-pixels are disposed alternately with each other in a vertical direction.

[0027] In one or more embodiments, the first through fourth thin film transistors are arranged between the white and green sub-pixels.

[0028] The white pixel electrode includes: two horizontal bars disposed parallel to the gate lines, including a first horizontal bar disposed in a bottom edge region of the white sub-pixel adjacent to one gate line and a second horizontal bar disposed in a top edge region of the white sub-pixel adjacent to another gate line; vertical bars disposed between the horizontal bars in parallel with the data lines; a first extensive portion configured to extend from the first horizontal bar along the downward direction of the white sub-pixel parallel to the data lines, and a second extensive portion configured to extend from the second horizontal bar along the upward direction of the white sub-pixel parallel to the data lines.

[0029] Thus, the white sub-pixel includes a storage capacitor formed between the white pixel electrode, which includes the horizontal bars, the vertical bars and the first and second extensive portions, and the common electrode disposed under the white pixel electrode.

[0030] In one or more embodiments, the first extensive portion overlaps with the gate line used to drive the white sub-pixel, and the second extensive portion overlaps with the gate line used to drive the green sub-pixel.

[0031] The first and second thin film transistors are disposed in an adjacent region to a bottom edge of the white sub-pixel, and the third and fourth thin film transistors are disposed in another adjacent region to a top edge of the white sub-pixel.

[0032] In one or more embodiments, the first and second thin film transistors are disposed in an overlapping manner with the gate line which is used to drive the white sub-pixel, and the third and fourth thin film transistors are disposed in

an overlapping manner with the gate line which is used to drive the green sub-pixel.

[0033] In one or more embodiments, the first thin film transistor is connected to the white pixel electrode, the second thin film transistor is connected to the red pixel electrode, the third thin film transistor is connected to the green pixel electrode, and the fourth thin film transistor is connected to the blue pixel electrode.

[0034] In one or more embodiments, the gate lines are used as gate electrodes of the first through fourth thin film transistors.

[0035] In one or more embodiments, each of the first through fourth thin film transistors includes a source electrode formed in a semicircular ring shape.

[0036] In one or more embodiments, each of the source electrodes of the first through fourth thin film transistors includes a first source electrode portion parallel to the data lines and a second source electrode portion parallel to the gate lines and is disposed to surround a drain electrode of the respective thin film transistor.

[0037] In one or more embodiments, the common electrodes are formed in a single body shape.

[0038] In one or more embodiments, the common electrode of the single body shape is formed in a plate shape.

[0039] In one or more embodiments, the common electrode with the plate shape is formed to have an opening opposite to each of the first through fourth thin film transistors.

[0040] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0041] The accompanying drawings, which are included to provide a further understanding of the embodiments and are incorporated herein and constitute a part of this application, illustrate embodiment(s) of the present disclosure and together with the description serve to explain the disclosure. In the drawings:

Fig. 1A is a planar view showing a pixel structure of an FFS mode LCD device according to the related art;

Fig. 1B is a planar view showing a pixel structure of the related art which further includes a white sub-pixel in order to secure transmittance;

Fig. 2 is a planar view showing a pixel structure of an FFS mode LCD device according to an example embodiment of the present disclosure;

Fig. 3 is a planar view showing a white sub-pixel structure of an FFS mode LCD device according to an example embodiment of the present disclosure; and

Fig. 4 is a cross-sectional view showing a white sub-pixel of an FFS mode LCD device taken along lines I-I' and II-II' in Fig. 3.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

[0042] Advantages and features of the present disclosure, and implementation methods thereof will be clarified through the following embodiments described with reference to the accompanying drawings. These embodiments introduced hereinafter are provided as examples to the ordinary skilled person in the art. As such, these embodiments might be embodied in a different shape, so are not limited to these embodiments described here. Therefore, the present disclosure must be defined by scopes of claims.

[0043] In the following description, numerous specific details are set forth, such as particular structures, sizes, ratios, angles, coefficients and so on, in order to provide an understanding of the various embodiments of the present disclosure. However, it will be appreciated by one of ordinary skill in the art that the various embodiments of the present disclosure may be practiced without these specific details. The same reference numbers will be used throughout this disclosure to refer to the same or like parts. In other instances, well-known technologies have not been described in detail in order to avoid obscuring the present disclosure.

[0044] It will be further understood that the terms "comprises", "comprising,", "has", "having", "includes" and/or "including", when used herein, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof. As used herein, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise.

[0045] Elements used in the present disclosure without additional specific details must be considered to include tolerance.

[0046] In the description of embodiments, when a structure is described as being positioned "on or above" or "under or below" another structure, this description should be construed as including a case in which the structures contact each other as well as a case in which a third structure is disposed therebetween.

[0047] The temporal terms of "after", "subsequently", "next", "before" and so on used in this disclosure without specifying

"immediately" or "directly" can include other discontinuously temporal relations.

[0048] Moreover, although some of the elements are designated with numerical terms (e.g., first, second, third, etc.), it should be understood that such designations are only used to specify one element from a group of similar elements, but not to limit the element in any specific order. As such, an element designated as a first element could be termed as a second element or as third element without departing from the scope of exemplary embodiments.

[0049] The features of various exemplary embodiments of the present disclosure may be partially or entirely bound or combined with each other, and be technically engaged and driven using various methods as apparent to those skilled in the art, and the exemplary embodiments may be independently practiced alone or in combination.

[0050] Reference will now be made in detail to the embodiments of the present disclosure, examples of which are illustrated in the accompanying drawings. Also, the size and thickness of the device might be expressed to be exaggerated for the sake of convenience in the drawings. Wherever possible, the same reference numbers will be used throughout this disclosure including the drawings to refer to the same or like parts.

[0051] **Fig. 2** is a planar view showing a pixel structure of an FFS mode LCD device according to an example embodiment of the present disclosure.

[0052] Referring to Fig. 2, An FFS mode LCD device is defined into a plurality of sub-pixel (SP) regions (hereinafter, "sub-pixel regions SP") by a plurality of gate lines (101 in **Fig. 3**) and a plurality of data lines (103 in Fig. 3). A single pixel P is configured with white, red, green and blue sub-pixels WSP, RSP, GSP and BSP.

[0053] The white, red, green and blue sub-pixels WSP, RSP, GSP and BSP are defined by being opposite to white (W), red (R), green (G) and blue (B) color filter layers (not shown) which are formed on an upper substrate (not shown) . As such, no color filter layer may be formed on the upper substrate opposite to the white sub-pixel WSP.

[0054] In order to realize high definition LCD device, the present disclosure allows not only the white sub-pixel WSP to be additionally included in the single pixel P but also the area of the white sub-pixel WSP to be asymmetric with respect to those of the red, green and blue sub-pixels RSP, GSP and BSP. Also, the area of the white sub-pixel WSP can be different from those of the red, green and blue sub-pixels RSP, GSP and BSP.

[0055] More specifically, in order to secure a sufficient transmittance rather than enhance color reproduction properties, the white sub-pixel WSP has a relatively small area. As such, the red, green and blue sub-pixels RSP, GSP and BSP can be defined in such a manner as to each have a maximized area.

[0056] In this manner, although the white sub-pixel WSP is included for securing a sufficient transmittance, the red, green and blue sub-pixels RSP, GSP and BSP of the LCD device of the present disclosure can be almost the same area as those of the pixel of the related art LCD device.

[0057] Also, the LCD device of the present disclosure allows thin film transistors TFT assigned to the white, red, green and blue sub-pixels WSP, RSP, GSP and BSP to be arranged between the green sub-pixel GSP and the white sub-pixel WSP opposite to each other. As such, the areas of the red, green and blue sub-pixels RSP, GSP and BSP can be more sufficiently secured.

[0058] In detail, the present disclosure distributively arranges the thin film transistors TFT, which are assigned to the white, red, green and blue sub-pixel regions WSP, RSP, GSP and BSP, in regions adjacent to the top and bottom edges of the white sub-pixel WSP. As such, the thin film transistors TFT assigned to the white, red, green and blue sub-pixels WSP, RSP, GSP and BSP can be arranged alternately with the green sub-pixels GSP and the white sub-pixels WSP along a vertical direction.

[0059] Although the white sub-pixel WSP is additionally included for securing a sufficient transmittance, the present disclosure can allow the areas of the red, green and blue sub-pixels to be sufficiently secured. In accordance therewith, deterioration of color reproduction properties which is caused in the related art LCD device due to enhancement of transmittance can be prevented.

[0060] In the LCD device of the present disclosure, the red sub-pixel RSP and the white sub-pixel WSP with a relatively small area are arranged adjacent to each other. Also, the blue sub-pixel BSP and the green sub-pixel GSP are arranged adjacently to each other in a horizontal direction.

[0061] Also, the red sub-pixel RSP and the blue sub-pixel BSP are adjacent to each other in a vertical direction. Also, the green sub-pixel GSP and the white sub-pixel WSP are adjacent to each other in the vertical direction.

[0062] Among the thin film transistors TFT assigned to the sub-pixels SP of the single pixel, two thin film transistors TFT are disposed adjacent to the bottom edge of the white sub-pixel WSP. The two thin film transistors TFT disposed adjacent to the bottom edge of the white sub-pixel WSP are connected to pixel electrodes which are disposed in the white sub-pixel WSP and the red sub-pixel RSP adjacent thereto.

[0063] On the other hand, the other two thin film transistors TFT are disposed adjacently to the top edge of the white sub-pixel WSP. Also, the two thin film transistors TFT disposed adjacently to the top edge of the white sub-pixel WSP are connected to pixel electrodes which are disposed in the green sub-pixel GSP and the blue sub-pixel BSP adjacent thereto.

[0064] In this manner, the FFS mode LCD device according to the embodiment of the present disclosure allows the area of the white sub-pixel WSP to be asymmetric with respect to those of the red, green and blue sub-pixels RSP, GSP

and BSP. As such, the transmittance property of the pixel can be enhanced.

[0065] Moreover, the areas of the red, green and blue sub-pixels RSP, GSP and BSP can be sufficiently secured. Therefore, color reproduction properties of the FFS mode LCD device can be enhanced.

[0066] **Fig. 3** is a planar view showing a white sub-pixel structure of an FFS mode LCD device according to an example embodiment of the present disclosure. **Fig. 4** is a cross-sectional view showing a white sub-pixel of an FFS mode LCD device taken along lines I-I' and II-II' in Fig. 3.

[0067] Referring to Figs. 3 and 4, the FFS mode LCD device according to an embodiment of the present disclosure includes gate lines 101 and data lines 103 crossing each other. As such, white, red, green and blue sub-pixel regions WSP, RSP, GSP and BSP are defined.

[0068] The green sub-pixel GSP and the blue sub-pixel BSP are adjacent to each other in a horizontal direction. The white sub-pixel WSP and the red sub-pixel RSP are adjacent to each other in the horizontal direction.

[0069] Also, the green sub-pixel GSP and the white sub-pixel WSP are adjacent to each other in a vertical direction. The blue sub-pixel BSP and the red sub-pixel RSP are adjacent to each other in the vertical direction.

[0070] The LCD device includes a first thin film transistor TFT1 and a second thin film transistor TFT2 which are arranged parallel to a gate line 101 in an adjacent region to a bottom edge of the white sub-pixel WSP. The first thin film transistor TFT1 is connected to a white pixel electrode WP of the white sub-pixel WSP. The second thin film transistor TFT2 is connected to a red pixel electrode RP adjacent to the white sub-pixel WSP.

[0071] Also, the LCD device further includes a third thin film transistor TFT3 and a fourth thin film transistor TFT4 are arranged parallel to another gate line 301, which is used to drive the green sub-pixel GSP, in an adjacent region to the top edge of the white sub-pixel WSP. The third thin film transistor TFT3 is connected to a green pixel electrode GP of the green sub-pixel GSP. The fourth thin film transistor TFT4 is connected to a blue pixel electrode BP adjacent to the green sub-pixel GSP.

[0072] The present disclosure allows the white sub-pixel WSP to be formed in a small area compared to the red, green and blue sub-pixels RSP, GSP and BSP. In accordance therewith, not only the transmittance of a single pixel (or a color pixel) can be sufficiently secured but also the areas of the red, green and blue sub-pixels can be sufficiently secured.

[0073] The first through fourth thin film transistors TFT1, TFT2, TFT3 and TFT4 are arranged between the white sub-pixel WSP and the green sub-pixel GSP and along a parallel direction with the gate line 103. In detail, the first through fourth thin film transistors TFT1, TFT2, TFT3 and TFT4 are disposed on one gate line 101, which is used to drive the white sub-pixel WSP, and another gate line 301 which is used to drive the green sub-pixel GSP adjacent to the white sub-pixel WSP. As such, the area occupied by the thin film transistors TFT1 ~ TFT4 can be minimized.

[0074] For the convenience of explanation, the present disclosure will be explained with the first thin film transistor TFT1, which is assigned to the white sub-pixel WSP, as a center.

[0075] The first thin film transistor TFT1 is disposed on the gate line. As such, the first thin film transistor TFT1 uses the gate line 101 as its gate electrode.

[0076] Also, a drain electrode 118 of the first thin film transistor is disposed in overlapping with a part of the gate line 101. A source electrode 117 of the first thin film transistor TFT1 includes a first source electrode portion 117a and a second source electrode portion 117b. Such a source electrode 117 of the first thin film transistor TFT1 is formed in a semicircular ring shape surrounding the drain electrode 118.

[0077] The first source electrode portion 117a is disposed in a direction of the data line 103. The second source electrode portion 117b is disposed in a direction of the gate line 101.

[0078] As such, a channel layer region 114 between the source electrode 117 and the drain electrode 118 can be sufficiently secured. In accordance therewith, response characteristics of the first thin film transistor TFT1 can be enhanced.

[0079] Meanwhile, the second through fourth thin film transistors TFT2, TFT3 and TFT4 are formed in the same structure as the first thin film transistor TFT1.

[0080] The white pixel electrode WP electrically connected to the first thin film transistor TFT1 is disposed in the white sub-pixel region WSP. A common electrode 150 is disposed under the white pixel electrode WP.

[0081] The common electrode 150 disposed under the white pixel electrode 150 is formed on the entire surface of a substrate 100. However, openings OP are formed in regions of the common electrode 150 opposite to the first through fourth thin film transistors TFT1 through TFT4. The openings OP can enable parasitic capacitances generated between the thin film transistors TFT1 through TFT4 and the common electrode 150 to be reduced.

[0082] Such a common electrode 150 can have a plate shape. As such, the common electrode 150 is formed in the sub-pixel regions SP and non-display regions between the sub-pixel regions SP. A part of the common electrode 150 overlapping with the data line 103 can be used as a common wiring 151.

[0083] In other words, the common electrode 150 and the common wiring 151 are united with each other in a single plate shape. As such, the common electrode 150 and the common wiring 151 can be formed in the single plate shape opposite to all the white, red, green and blue sub-pixel regions WSP, RSP, GSP and BSP.

[0084] Such a white pixel electrode WP includes horizontal bars 203a parallel to the gate lines 101 and 301 and a

plurality of vertical bars 203 perpendicular to the horizontal bar 203a. Also, the white pixel electrode WP further includes first and second extensive portions 201 and 202 and a connection portion 204. The first and second extensive portions 201 and 202 each extend from the respective horizontal bar 203a toward the adjacent gate line 101 or 301 thereto. The connection portion 204 is connected to the drain electrode 118 via a contact hole C.

[0085] The horizontal bars 203a are disposed parallel to one gate line 101 and another gate line 301, which is disposed in the region of the adjacent green sub-pixel GSP, with having the vertical bars 203. In other words, the horizontal bars 203a are disposed in a bottom edge region of the white sub-pixel WSP adjacent to one gate line 101 and a top edge region of the white sub-pixel region WSP adjacent to another gate line 301.

[0086] The first extensive portion 201 is formed in a single body united with the respective horizontal bar 203a. Also, the first extensive portion 201 is disposed to cross the gate line 101. Similarly, the second extensive portion 202 is formed in a single body 203 united with the respective horizontal bar 203a. Also, the second extensive portion 203 is disposed to cross the gate line 301 within the region of the adjacent green sub-pixel GSP.

[0087] In other words, the first and second extensive portions 201 and 202 extend from outer edges of the horizontal bars 203a toward downward and upward directions of the white sub-pixel WSP parallel to the data line 103.

[0088] Such first and second extensive portions 201 and 202 partially overlap with the common electrode 150 corresponding to the regions of the gate lines 101 and 301. As such, the storage capacitance of the white sub-pixel WSP can be additional secured.

[0089] This results from the fact that the present disclosure must enable storage capacitance in the region of the white sub-pixel WSP to be smaller than those of the other sub-pixel regions due to the area of the white sub-pixel WSP being smaller than those of the other sub-pixels.

[0090] In general, a kickback voltage ΔVp in each of the sub-pixels SP is determined by the following equation 1.

【Equation 1】

$$\Delta Vp = \frac{Cgs}{(Cgs + Cst + Clc)} \Delta Vg$$

[0091] In the equation 1, 'Clc' is a capacitance of a liquid crystal cell, 'Cst' is a storage capacitance, 'Cgs' is a parasitic capacitance, and 'ΔVg' is a gate voltage difference.

[0092] The kickback voltage ΔVp is varied with the storage capacitance Cst of the sub-pixel SP. As such, a data voltage applied to the sub-pixel SP must be varied with the kickback voltage ΔVp. Due to this, image quality of the LCD device must deteriorate.

[0093] Actually, the present disclosure allows the white sub-pixel WSP to be formed in a smaller area compared to those of the other sub-pixels SP. As such, the kickback voltages ΔVp generated in the white, red, green and blue sub-pixels WSP, RSP, GSP and BSP cannot have the same value.

[0094] In other words, because the white sub-pixel WSP is formed in a smaller area than those of the red, green and blue sub-pixels RSP, GSP and BSP, the kickback voltage ΔVp generated in the white sub-pixel WSP is developed larger than the kickback voltages ΔVp generated in the red, green and blue sub-pixels RSP, GSP and BSP. As such, deviation of the data voltages applied to the sub-pixels SP can become larger. Due to this, image quality defects can be generated.

[0095] In this manner, the LCD device of the present disclosure not only enhances transmittance and color reproduction properties but also the sub-pixel region with an asymmetrically formed area to secure an additional storage capacitance. As such, the kickback voltages ΔVp generated in the white, red, green and blue sub-pixels WSP, RSP, GSP and BSP can have the same value. In other words, the kickback voltages ΔVp generated in the sub-pixels SP can have the same value or similar values for one another. In accordance therewith, the image quality defects can be prevented or reduced.

[0096] A method of fabricating an FFS mode LCD device according to an embodiment of the present disclosure will now be described.

[0097] First, gate lines are formed on a substrate 100 which is defined into white, red, green and blue sub-pixel regions WSP, RSP, GSP and BSP and formed from a transparent insulation material. The gate line is prepared by forming a gate metal film on the substrate 100 and patterning the gate metal film through a photolithography procedure.

[0098] In the LCD device of the present disclosure, gate electrodes of first through fourth thin film transistor TFT1~TFT4 are formed on the gate line 101. As such, it is not necessary for any separate gate electrode pattern. In other words, the gate line 101 can be used as the gate electrode of the thin film transistor.

[0099] The gate metal film can be formed in one of a single metal film of an opaque low-resistive conductor material and a double film structure. The double film structure can include a first metal film formed from an opaque low-resistive

conductor material film and a second metal film formed from an alloy of the opaque low-resistive conductor material. The opaque low-resistive conductor material can be one of aluminum Al, an aluminum alloy, tungsten W, copper Cu, nickel Ni, chromium Cr, molybdenum Mo, titanium Ti, platinum Pt, tantalum or other metals. Alternatively, the gate metal film can be formed in a multi-layered structure including at least two stacked metal films.

[0100] When the gate line 101 is formed on the substrate 100, a gate insulation film 102 is formed on the entire surface of the substrate 100. The gate insulation film 102 can be formed in a single layer of silicon oxide SiOx. Alternatively, the gate insulation film 102 can be formed by alternately depositing a silicon nitride SiNx and a silicon oxide SiOx.

[0101] Then, a channel 104 is formed on the gate insulation film 102 opposite to a part of the gate line 101. The channel 104 can be prepared by forming a semiconductor layer on the gate insulation film 102 and patterning the semiconductor layer using a mask procedure.

[0102] The semiconductor layer can include one of crystalline and amorphous silicon films and an ohmic contact layer. Alternatively, the semiconductor layer can be an oxide semiconductor layer.

[0103] The oxide semiconductor layer can be formed from an amorphous oxide which includes at least one of Indium In, zinc Zn, gallium Ga and hafnium Hf. For example, if the oxide semiconductor layer is formed from the oxide semiconductor of Ga-In-Zn-O through a sputtering process, three targets formed of In_2O_3, Ga_2O_3 and ZnO or a single target formed from Ga-In-Zn oxide can be used in the sputtering process. Alternatively, the oxide semiconductor layer can be formed through the sputtering process which uses either three targets formed from HfO_2, In_2O_3 and ZnO or a single target formed from Hf-In-Zn oxide.

[0104] When the channel layer 104 is formed on the substrate 100 as described above, source and drain electrodes 117 and 118 partially contacting the channel 104 and a data line 103 are formed. The source and drain electrode 117 and 118 and the data line 103 can be prepared by forming a source/drain metal film on the entire surface of the above-mentioned substrate 100 and then performing a photolithography procedure for the source/drain metal film.

[0105] The source/drain metal film can be formed from an opaque low-resistive conductor material. For example, the source/drain metal film can be formed from one of aluminum Al, an aluminum alloy, tungsten W, copper Cu, nickel Ni, chromium Cr, molybdenum Mo, titanium Ti, platinum Pt, tantalum Ta and so on. Alternatively, the source/drain metal film can be formed in a double layered structure which includes stacked transparent conductive material layer and opaque conductive material layer. The transparent conductive material layer can be formed from one of indium-tin-oxide ITO and indium-zinc-oxide IZO.

[0106] Thereafter, a planarization film 106 is formed on the entire surface of the above-mentioned substrate 100. Also, a transparent conductive film is formed on the planarization film 106. The transparent conductive film can be formed from one of indium-tin-oxide ITO, indium-zinc-oxide IZO and indium-tin-zinc-oxide ITZO.

[0107] After the transparent conductive film is formed on the substrate 100, a photolithography procedure is performed for the transparent conductive film. Then, a common electrode 150 and a common wiring 151 are formed in a single body united with each other. As described above, the common electrode 150 is formed on the entire surface of the substrate 100 in a plate shape. In this case, a part of the common electrode 150 opposite to the data line 103 can be used as the common wiring 151. As such, the common electrode 150 and the common wiring 151 united with each other can have the plate shape.

[0108] When the common electrode 150 is formed on the substrate 100 as described above, a protective film 109 is formed on the entire surface of the substrate 100. Subsequently, a contact hole C exposing a part of the drain electrode 118 is formed through a contact hole formation process.

[0109] After the formation of the contact hole C, another transparent conductive film is formed on the entire surface of the above-mentioned substrate 100. Then, a photolithography procedure is performed for another transparent conductive film, thereby forming a white pixel electrode WP, a red pixel electrode RP, a green pixel electrode GP and a blue pixel electrode BP in the sub-pixel regions SP.

[0110] As described above, the white pixel electrode WP includes horizontal bars 203a, vertical bars 203, first and second extensive portions 201 and 202 and a connection portion 204. The connection portion 204 is connected to the drain electrode 118 through the contact hole C.

[0111] As shown in the cross-sectional structure of Fig. 4 taken along a line I-I', the vertical bars 203 arranged in the white sub-pixel region WSP overlap with the common electrode 150 with the protective film 109 therebetween.

[0112] Also, the first extensive portion 201 of the white pixel electrode WP overlaps with a gate line 101 which is used to drive the white sub-pixel WSP, as shown in the cross-sectional structure of Fig. 4 taken along another line II-II'. As such, the first extensive portion 201 together with the common electrode 150 disposed thereunder can form an additional storage capacitor Cst.

[0113] Similarly, the second extensive portion 202 of the white pixel electrode WP is disposed in an overlapping manner with another gate line 301 which is used to drive the adjacent green sub-pixel region GSP. As such, the second extensive portion 202 together with the common electrode 150 disposed thereunder can form another additional storage capacitor Cst.

[0114] In other words, the present disclosure allows the first and second extensive portions 201 and 202, vertical bars

203 and horizontal bars 203a of the white pixel electrode WP together with the common electrode 150 disposed thereunder to form a storage capacitor Cst. As such, the white sub-pixel region WSP can have the same storage capacitance as those of the red, green and blue sub-pixel regions RSP, GSP and BSP. In accordance therewith, the image quality defects can be prevented.

[0115] In this manner, in the FFS mode LCD device according to the embodiment of the present disclosure, the area of the white sub-pixel WSP is asymmetrically formed with respect to those of the red, green and blue sub-pixels RSP, GSP and BSP. As such, the transmittance property of the pixel region can be enhanced.

[0116] In the FFS mode LCD device according to the embodiment of the present disclosure, the white, red, green and blue sub-pixels WSP, RSP, GSP and BSP with the asymmetric areas can have the same storage capacitance through a compensation of a storage capacitor. Therefore, the image quality defects caused by different kickback voltages ΔVp can be prevented.

[0117] It will be apparent to those skilled in the art that various modifications and variations can be made in the FFS mode LCD device of the present invention within the scope of the claims.

Claims

1. A fringe field switching mode liquid crystal display device, comprising:

a substrate (100);
gate and data lines (101, 301; 103) arranged to cross each other on the substrate (100) and define white (W), red (R), green (G) and blue (B) sub-pixels (SP);
first through fourth thin film transistors (TFT1, TFT2, TFT3, TFT4) connected to the white (W), red (R), green (G) and blue (B) sub-pixels (SP), respectively;
common electrodes (150) disposed in the white (W), red (R), green (G) and blue (B) sub-pixels (SP); and
white, red, green and blue pixel electrodes (WP, RP, GP, BP) disposed to overlap with the common electrodes (150) within the white (W), red (R), green (G) and blue (B) sub-pixels (SP);
wherein the areas of the red (R), green (G) and blue (B) sub-pixels (SP) are larger than that of the white (W) sub-pixel (SP);
wherein the first and second thin film transistors (TFT1, TFT2) are disposed in an adjacent region to a bottom edge of the white (W) sub-pixel (SP), and
the third and fourth thin film transistors (TFT3, TFT4) are disposed in another adjacent region to a top edge of the white (W) sub-pixel (SP);

and wherein the white pixel electrode (WP) includes:

two horizontal bars (203a) disposed parallel to the gate lines (101, 301), including a first horizontal bar disposed in a bottom edge region of the white sub-pixel (WP) adjacent to one gate line (101) and a second horizontal bar disposed in a top edge region of the white sub-pixel (WP) adjacent to another gate line (301);
vertical bars (203) disposed between the horizontal bars (203a) in parallel with the data lines (103);
a first extensive portion (201) configured to extend from the first horizontal bar (203a) along the downward direction of the white (W) sub-pixel (SP) parallel to the data lines (103), and a second extensive portion (202) configured to extend from the second horizontal bar (203a) along the upward direction of the white (W) sub-pixel (SP) parallel to the data lines (103),
wherein the white sub-pixel (W) includes a storage capacitor formed between the white pixel electrode (WP) and the common electrode (150) disposed under the white pixel electrode (WP).

2. The fringe field switching mode liquid crystal display device of claim 1, wherein the white (W) and green (G) sub-pixels (SP) are disposed alternately with each other in a vertical direction.

3. The fringe field switching mode liquid crystal display device of claim 2, wherein the first through fourth thin film transistors (TFT1, TFT2, TFT3, TFT4) are arranged between the white (W) and green (G) sub-pixels (SP).

4. The fringe field switching mode liquid crystal display device of claim 1, wherein

the first extensive portion (201) overlaps with the gate line (101) used to drive the white (W) sub-pixel (SP), and the second extensive portion (202) overlaps with the gate line (301) used to drive the green (G) sub-pixel (SP).

5. The fringe field switching mode liquid crystal display device of claim 1, wherein

the first and second thin film transistors (TFT1, TFT2) are disposed in an overlapping manner with the gate line (101) which is used to drive the white (W) sub-pixel (SP), and
the third and fourth thin film transistors (TFT3, TFT4) are disposed in an overlapping manner with the gate line (301) which is used to drive the green (G) sub-pixel (SP).

6. The fringe field switching mode liquid crystal display device of claim 1 or 5, wherein

the first thin film transistor (TFT1) is connected to the white pixel electrode (WP),
the second thin film transistor (TFT2) is connected to the red pixel electrode (RP),
the third thin film transistor (TFT3) is connected to the green pixel electrode (GP), and
the fourth thin film transistor (TFT4) is connected to the blue pixel electrode (BP).

7. The fringe field switching mode liquid crystal display device of claim 6, wherein the gate lines (101, 301) are used as gate electrodes of the first through fourth thin film transistors (TFT1, TFT2, TFT3, TFT4).

8. The fringe field switching mode liquid crystal display device of any one of claims 1 to 7, wherein each of the first through fourth thin film transistors (TFT1, TFT2, TFT3, TFT4) includes a source electrode (117) formed in a semi-circular ring shape.

9. The fringe field switching mode liquid crystal display device of claim 8, wherein each of the source electrodes (117) of the first through fourth thin film transistors (TFT1, TFT2, TFT3, TFT4) includes a first source electrode portion (117a) parallel to the data lines (103) and a second source electrode portion (117b) parallel to the gate lines (101, 301) and is disposed to surround a drain electrode (118) of the respective thin film transistor (TFT1, TFT2, TFT3, TFT4) .

10. The fringe field switching mode liquid crystal display device of any one of claims 1 to 9, wherein the common electrodes (150) are formed in a single body shape.

11. The fringe field switching mode liquid crystal display device of claim 10, wherein the common electrode (150) of the single body shape is formed in a plate shape.

12. The fringe field switching mode liquid crystal display device of claim 11, wherein the common electrode (150) with the plate shape is formed to have an opening opposite to each of the first through fourth thin film transistors (TFT1, TFT2, TFT3, TFT4).

Patentansprüche

1. Flüssigkristall-Anzeigevorrichtung für Randfeld-Schaltbetrieb, aufweisend:

ein Substrat (100);
Gate- und Datenleitungen (101, 301; 103), die so angeordnet sind, dass sie einander auf dem Substrat (100) kreuzen und ein weißes (W), ein rotes (R), ein grünes (G) und ein blaues (B) Sub-Pixel (SP) begrenzen;
einen ersten Dünnschichttransistor (TFT1), einen zweiten Dünnschichttransistor (TFT2), einen dritten Dünnschichttransistor (TFT3) und einen vierten Dünnschichttransistor (TFT4), die mit dem weißen (W), dem roten (R), dem grünen (G) bzw. dem blauen Sub-Pixel (SP) verbunden sind;
Elektroden (150) für ein gemeinsames Potenzial, die im weißen (W), im roten (R), im grünen (G) und im blauen (B) Sub-Pixel (SP) angeordnet sind; und
eine Weiß-, eine Rot-, eine Grün- und eine Blau-Pixelelektrode (WP, RP, GP, BP), die so angeordnet sind, dass sie sich in dem weißen (W), dem roten (R), dem grünen (G) bzw. dem blauen Sub-Pixel (SP) mit den für ein gemeinsames Potenzial bestimmten Elektroden (150) überlappen;
wobei die Flächen des roten (R), des grünen (G) und des blauen (B) Sub-Pixels (SP) größer sind als die Fläche des weißen (W) Sub-Pixels (SP);
wobei der erste Dünnschichttransistor (TFT1) und der zweite Dünnschichttransistor (TFT2) in einer Zone angeordnet sind, die einem unteren Rand des weißen (W) Sub-Pixels (SP) benachbart ist, und
der dritte Dünnschichttransistor (TFT3) und der vierte Dünnschichttransistor (TFT4) in einer anderen Zone

angeordnet sind, die einem oberen Rand des weißen (W) Sub-Pixels (SP) benachbart ist;
und wobei die Weiß-Pixelelektrode (WP) aufweist:

zwei horizontale Streifen (203a), die parallel zu den Gate-Leitungen (101, 301) angeordnet sind, einschließlich eines erstens horizontalen Streifens, der in einem unteren Randbereich des weißen Sub-Pixels (WP) in Nachbarschaft zu einer Gate-Leitung (101) angeordnet ist, und eines zweiten horizontalen Streifens, der in einem oberen Randbereich des weißen Sub-Pixels (WP) in Nachbarschaft zu einer weiteren Gate-Leitung (301) angeordnet ist;
vertikale Streifen (203), die zwischen den horizontalen Streifen (203a) parallel zu den Datenleitungen (103) angeordnet sind;
einen ersten abstehenden Abschnitt (201), der so angeordnet ist, dass er von dem ersten horizontalen Streifen (203a) in Abwärtsrichtung des weißen (W) Sub-Pixels (SP) parallel zu den Datenleitungen (103) absteht, und einen zweiten abstehenden Abschnitt (202), der so angeordnet ist, dass er von dem zweiten horizontalen Streifen (203a) in Aufwärtsrichtung des weißen (W) Sub-Pixels (SP) parallel zu den Datenleitungen (103) absteht,

wobei das weiße Sub-Pixel (W) eine Speicherkapazität aufweist, die zwischen der Weiß-Pixelelektrode (WP) und der für ein gemeinsames Potenzial bestimmten Elektrode (150), die unter der Weiß-Pixelelektrode (WP) angeordnet ist, gebildet ist.

2. Flüssigkristall-Anzeigevorrichtung für Randfeld-Schaltbetrieb nach Anspruch 1, wobei das weiße (W) und das grüne (G) Sub-Pixel (SP) in Vertikalrichtung einander abwechselnd angeordnet sind.

3. Flüssigkristall-Anzeigevorrichtung für Randfeld-Schaltbetrieb nach Anspruch 2, wobei der erste, der zweite, der dritte und der vierte Dünnschichttransistor (TFT1, TFT2, TFT3, TFT4) zwischen dem weißen (W) und dem grünen (G) Sub-Pixel (SP) angeordnet sind.

4. Flüssigkristall-Anzeigevorrichtung für Randfeld-Schaltbetrieb nach Anspruch 1, wobei
der erste abstehende Abschnitt (201) sich mit der Gate-Leitung (101) überlappt, die dazu dient, das weiße (W) Sub-Pixel (SP) zu betreiben, und
der zweite abstehende Abschnitt (202) sich mit der Gate-Leitung (301) überlappt, die dazu dient, das grüne (G) Sub-Pixel (SP) zu betreiben.

5. Flüssigkristall-Anzeigevorrichtung für Randfeld-Schaltbetrieb nach Anspruch 1, wobei
der erste und der zweite Dünnschichttransistor (TFT1, TFT2) sich mit der Gate-Leitung (101) überlappen, die dazu dient, das weiße (W) Sub-Pixel (SP) zu betreiben, und
der dritte und der vierte Dünnschichttransistor (TFT3, TFT4) sich mit der Gate-Leitung (301) überlappen, die dazu dient, das grüne (G) Sub-Pixel (SP) zu betreiben.

6. Flüssigkristall-Anzeigevorrichtung für Randfeld-Schaltbetrieb nach Anspruch 1 oder 5, wobei
der erste Dünnschichttransistor (TFT1) mit der Weiß-Pixelelektrode (WP) verbunden ist,
der zweite Dünnschichttransistor (TFT2) mit der Rot-Pixelelektrode (RP) verbunden ist,
der dritte Dünnschichttransistor (TFT3) mit der Grün-Pixelelektrode (GP) verbunden ist, und
der vierte Dünnschichttransistor (TFT4) mit der Blau-Pixelelektrode (BP) verbunden ist.

7. Flüssigkristall-Anzeigevorrichtung für Randfeld-Schaltbetrieb nach Anspruch 6, wobei die Gate-Leitungen (101, 301) als Gate-Elektroden des ersten, des zweiten, des dritten bzw. des vierten Dünnschichttransistors (TFT1, TFT2, TFT3, TFT4) dienen.

8. Flüssigkristall-Anzeigevorrichtung für Randfeld-Schaltbetrieb nach einem der Ansprüche 1 bis 7, wobei jeder der vier Dünnschichttransistoren (TFT1, TFT2, TFT3, TFT4) eine Source-Elektrode (117) aufweist, die in einer halbkreisförmigen Ringform ausgebildet ist.

9. Flüssigkristall-Anzeigevorrichtung für Randfeld-Schaltbetrieb nach Anspruch 8, wobei jede der Source-Elektroden (117) der vier Dünnschichttransistoren (TFT1, TFT2, TFT3, TFT4) einen ersten Source-Elektrodenabschnitt (117a) parallel zu den Datenleitungen (103) und einen zweiten Source-Elektrodenabschnitt (117b) parallel zu den Gate-Leitungen (101, 301) aufweist und in der Weise angeordnet ist, dass sie eine Drain-Elektrode (118) des jeweiligen Dünnschichttransistors (TFT1, TFT2, TFT3, TFT4) umgibt.

10. Flüssigkristall-Anzeigevorrichtung für Randfeld-Schaltbetrieb nach einem der Ansprüche 1 bis 9, wobei die für ein gemeinsames Potenzial bestimmten Elektroden (150) einstückig ausgebildet sind.

11. Flüssigkristall-Anzeigevorrichtung für Randfeld-Schaltbetrieb nach Anspruch 10, wobei die für ein gemeinsames Potenzial bestimmte einstückige Elektrode (150) plattenförmig ausgebildet ist.

12. Flüssigkristall-Anzeigevorrichtung für Randfeld-Schaltbetrieb nach Anspruch 11, wobei die für ein gemeinsames Potenzial bestimmte plattenförmige Elektrode (150) in der Weise ausgebildet ist, dass sie eine Öffnung aufweist, die jedem der vier Dünnschichttransistoren (TFT1, TFT2, TFT3, TFT4) gegenüberliegt.

Revendications

1. Dispositif d'affichage à cristaux liquides en mode de commutation de champ de franges, comprenant :

un substrat (100) ;
des lignes de grille et de données (101, 301 ; 103) agencées pour se croiser sur le substrat (100) et définir des sous-pixels (SP) blanc (W), rouge (R), vert (G) et bleu (B) ;
des premier à quatrième transistors en couches minces (TFT1, TFT2, TFT3, TFT4) connectés respectivement aux sous-pixels (SP) blanc (W), rouge (R), vert (G) et bleu (B) ;
des électrodes communes (150) disposées dans les sous-pixels (SP) blanc (W), rouges(R), vert (G) et bleu (B) ; et
des électrodes de pixels blanc, rouge, vert et bleu (WP, RP, GP, BP) disposées de manière à chevaucher les électrodes communes (150) à l'intérieur des sous-pixels (SP) blanc (W), rouge (R), vert (G) et bleu (B) ;
dans lequel les surfaces des sous-pixels (SP) rouge (R), vert (G) et bleu (B) sont plus importantes que celle du sous-pixel (SP) blanc (W) ;
dans lequel les premier et deuxième transistors en couches minces (TFT1, TFT2) sont disposés dans une région adjacente à un bord inférieur du sous-pixel (SP) blanc (W), et
les troisième et quatrième transistors en couches minces (TFT3, TFT4) sont disposés dans une autre région adjacente à un bord supérieur du sous-pixel (SP) blanc (W) ;
et dans lequel l'électrode de pixel blanc (WP) inclut :

deux barres horizontales (203a) disposées parallèlement aux lignes de grille (101, 301), incluant une première barre horizontale disposée dans une région de bord inférieur du sous-pixel blanc (WP) adjacent à une ligne de grille (101) et une seconde barre horizontale disposée dans une région de bord supérieur du sous-pixel blanc (WP) adjacent à une autre ligne de grille (301) ;
des barres verticales (203) disposées entre les barres horizontales (203a) parallèlement aux lignes de données (103) ;
une première partie étendue (201) configurée pour s'étendre à partir de la première barre horizontale (203a) le long de la direction descendante du sous-pixel (SP) blanc (W) parallèlement aux lignes de données (103), et une seconde partie étendue (202) configurée pour s'étendre à partir de la seconde barre horizontale (203a) le long de la direction ascendante du sous-pixel (SP) blanc (W) parallèlement aux lignes de données (103),

dans lequel le sous pixel blanc (W) inclut un condensateur de stockage formé entre l'électrode de pixel blanc (WP) et l'électrode commune (150) disposée sous l'électrode de pixel blanc (WP).

2. Dispositif d'affichage à cristaux liquides en mode de commutation de champ de franges selon la revendication 1, dans lequel les sous-pixels (SP) blanc (W) et vert (G) sont disposés en alternance les uns avec les autres dans une direction verticale.

3. Dispositif d'affichage à cristaux liquides en mode de commutation de champ de franges selon la revendication 2, dans lequel les premier à quatrième transistors en couches minces (TFT1, TFT2, TFT3, TFT4) sont agencés entre les sous-pixels (SP) blanc (W) et vert (G).

4. Dispositif d'affichage à cristaux liquides en mode de commutation de champ de franges selon la revendication 1, dans lequel
la première partie étendue (201) chevauche la ligne de grille (101) utilisée pour entraîner le sous-pixel (SP) blanc

(W), et
la seconde partie étendue (202) chevauche la ligne de grille (301) utilisée pour entraîner le sous-pixel (SP) vert (G).

5. Dispositif d'affichage à cristaux liquides en mode de commutation de champ de franges selon la revendication 1, dans lequel
les premier et deuxième transistors en couches minces (TFT1, TFT2) sont disposés de manière à chevaucher la ligne de grille (101) qui est utilisée pour entraîner le sous-pixel (SP) blanc (W), et
les troisième et quatrième transistors en couches minces (TFT3, TFT4) sont disposés de manière à chevaucher la ligne de grille (301) qui est utilisée pour entraîner le sous-pixel (SP) vert (G).

6. Dispositif d'affichage à cristaux liquides en mode de commutation de champ de franges selon la revendication 1 ou 5, dans lequel
le premier transistor en couches minces (TFT1) est connecté à l'électrode de pixel blanc (WP),
le deuxième transistor en couches minces (TFT2) est connecté à l'électrode de pixel rouge (RP),
le troisième transistor en couches minces (TFT3) est connecté à l'électrode de pixel vert (GP) et
le quatrième transistor en couches minces (TFT4) est connecté à l'électrode de pixel bleu (BP).

7. Dispositif d'affichage à cristaux liquides en mode de commutation de champ de franges selon la revendication 6, dans lequel les lignes de grille (101, 301) sont utilisées en tant qu'électrodes de grille des premier à quatrième transistors en couches minces (TFT1, TFT2, TFT3, TFT4).

8. Dispositif d'affichage à cristaux liquides en mode de commutation de champ de franges selon l'une quelconque des revendications 1 à 7, dans lequel chacun des premier à quatrième transistors en couches minces (TFT1, TFT2, TFT3, TFT4) inclut une électrode de source (117) en forme d'anneau semi-circulaire.

9. Dispositif d'affichage à cristaux liquides en mode de commutation de champ de franges selon la revendication 8, dans lequel chacune des électrodes de source (117) des premier à quatrième transistors en couches minces (TFT1, TFT2, TFT3, TFT4) inclut une première partie d'électrode de source (117a) parallèle aux lignes de données (103) et une seconde partie d'électrode de source (117b) parallèle aux lignes de grille (101, 301) et est disposée de sorte à entourer une électrode de drain (118) du transistor en couches minces (TFT1, TFT2, TFT3, TFT4) respectif.

10. Dispositif d'affichage à cristaux liquides en mode de commutation de champ de franges selon l'une quelconque des revendications 1 à 9, dans lequel les électrodes communes (150) sont formées d'un seul tenant.

11. Dispositif d'affichage à cristaux liquides en mode de commutation de champ de franges selon la revendication 10, dans lequel l'électrode commune (150) du corps d'un seul tenant a une forme plate.

12. Dispositif d'affichage à cristaux liquides en mode de commutation de champ de franges selon la revendication 11, dans lequel l'électrode commune (150) à la forme plate est formée de manière à avoir une ouverture face à chacun des premier à quatrième transistors en couches minces (TFT1, TFT2, TFT3, TFT4).

Fig. 1A

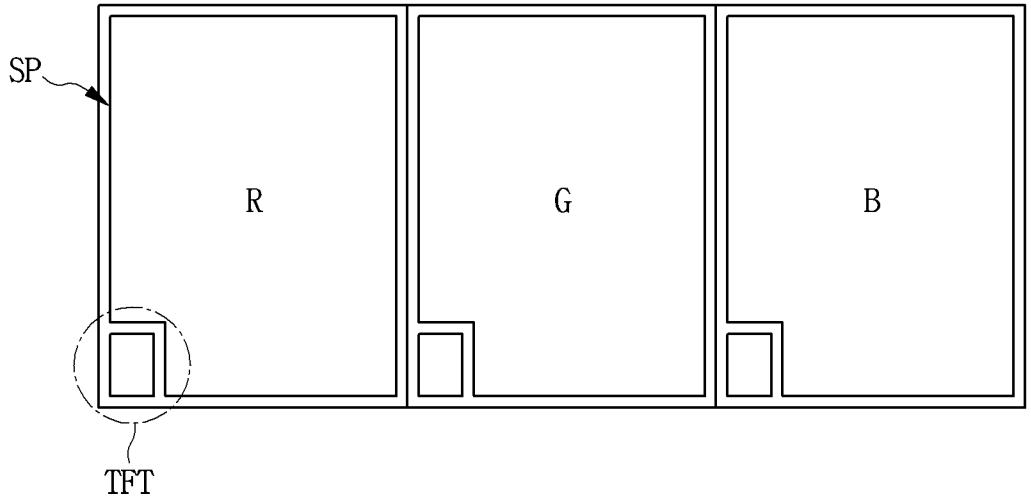


Fig. 1B

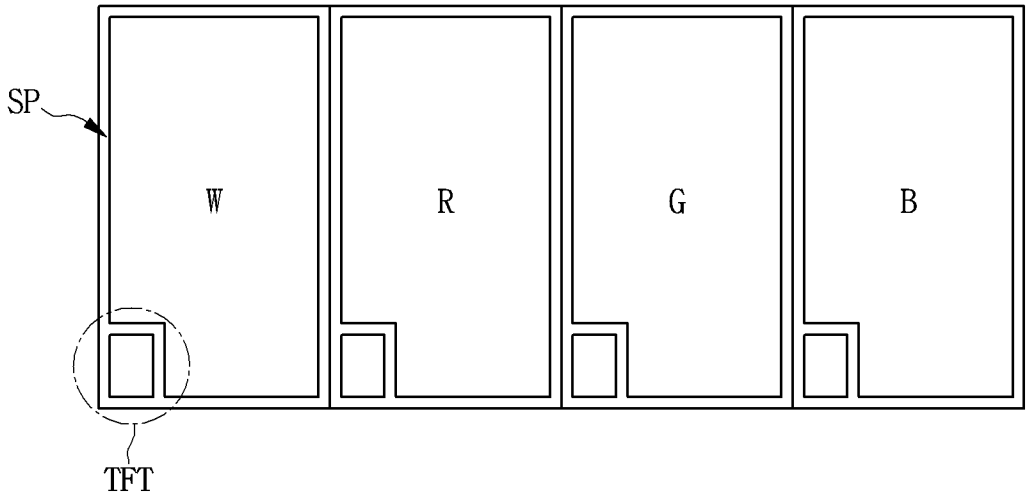


Fig. 2

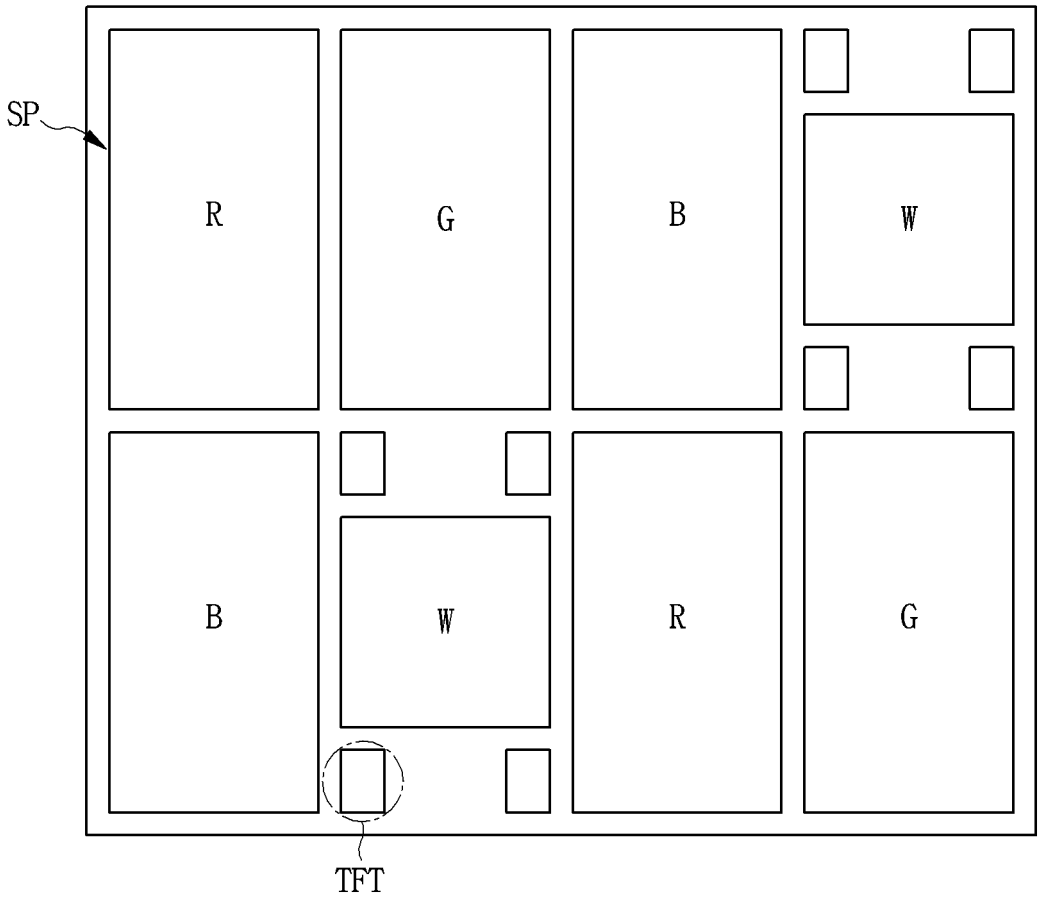


Fig. 3

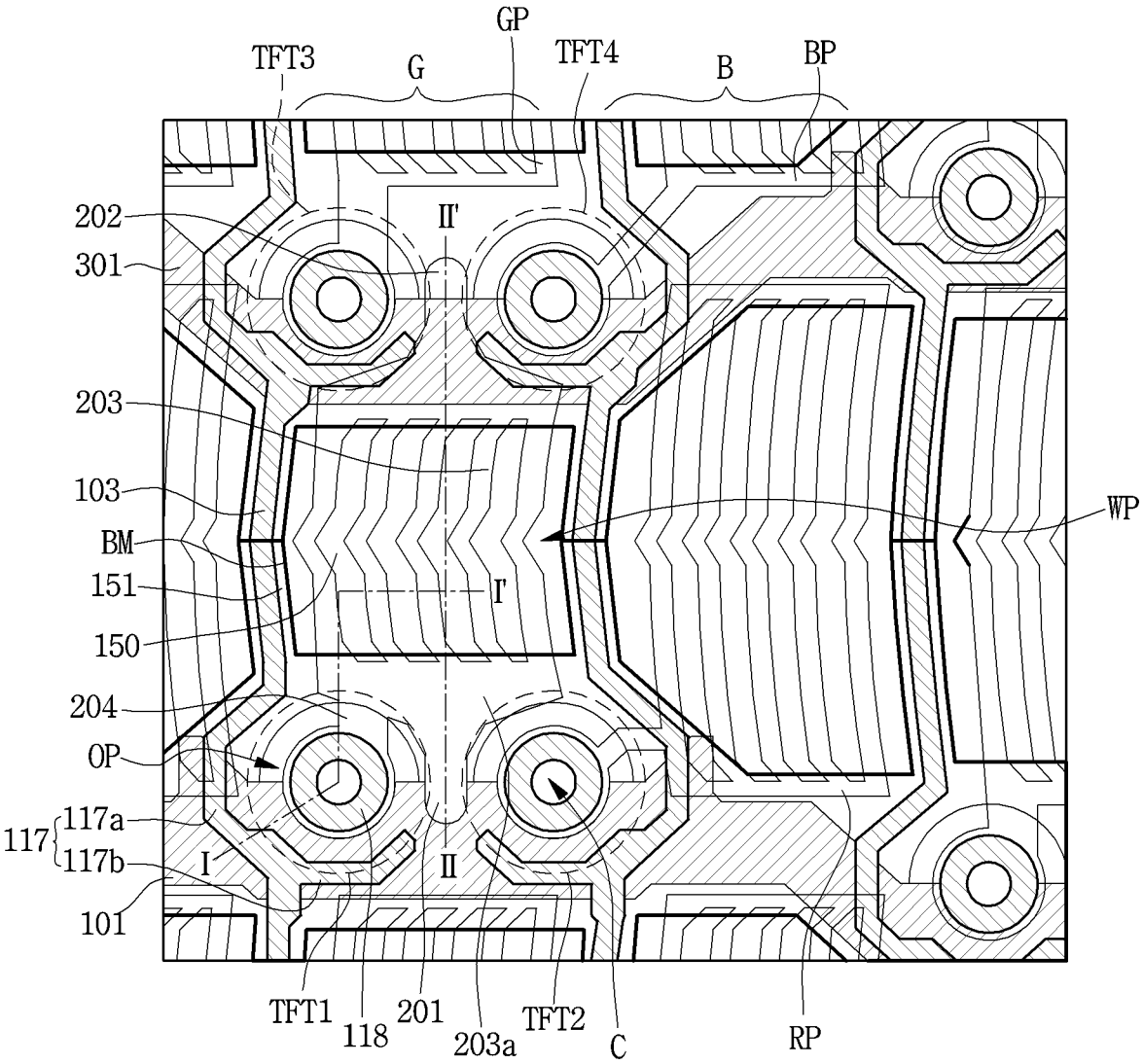
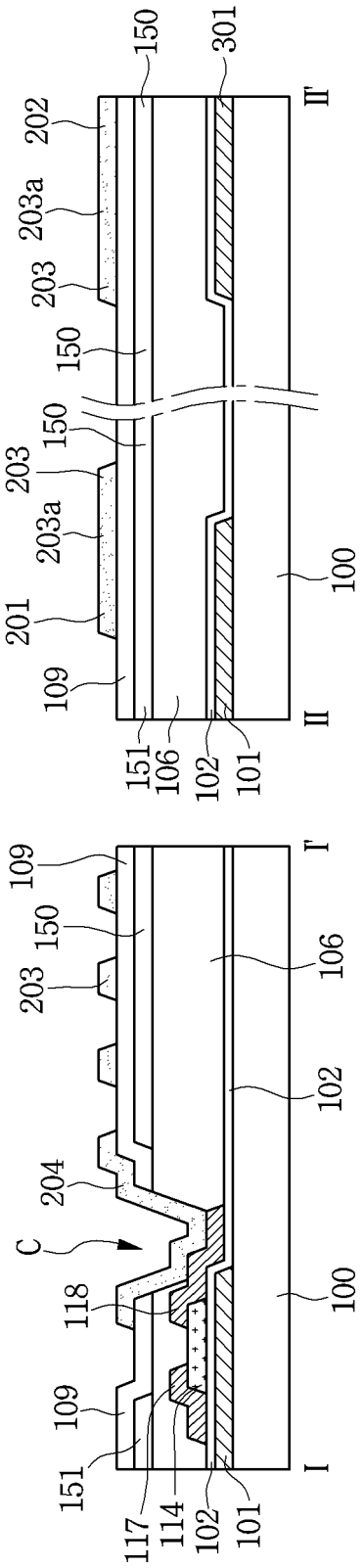

GP
TFT3
G
TFT4
B
BP
202
II'
301
203
103
WP
BM
151
I'
150
204
OP
117
117a
117b
I
II
101
TFT1
118
201
203a
TFT2
C
RP

Fig. 4


150
301
II'
202
203a
203
150
150
203
203a
201
109
100
II
151
106
102
101
109
I'
150
106
203
102
204
C
118
100
109
I
151
117
114
102
101

REFERENCES CITED IN THE DESCRIPTION

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专利名称(译)	带有RGBW PIXELS的边缘场切换模式液晶显示面板		
公开(公告)号	EP3035116B1	公开(公告)日	2020-03-04
申请号	EP2015196000	申请日	2015-11-24
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IPC分类号	G02F1/1343 G02F1/1362		
CPC分类号	G02F1/136213 G02F1/136286 G02F1/1368 G02F2001/134372 G02F2201/52 G02F1/1343 G02F1/1362 Y10S359/90 G02F1/134309 G02F2001/134345		
优先权	1020140182059 2014-12-17 KR		
其他公开文献	EP3035116A1		
外部链接	Espacenet		

摘要(译)

公开了一种FFS模式LCD装置，其包括：基板（100）；以及基板（100）。 栅极和数据线（101、301; 103）布置为在基板（100）上彼此交叉，并定义白色（W），红色（R），绿色（G）和蓝色（B）子像素（SP） 不对称区域； 连接至白色（W），红色（R），绿色（G）和蓝色（B）子像素（SP）的第一至第四薄膜晶体管（TFT1，TFT2，TFT3，TFT4）； 设置在白色（W），红色（R），绿色（G）和蓝色（B）子像素（SP）中的公共电极（150）； 设置成与白色（W），红色（R），绿色（G）和蓝色（B）内的公共电极（150）重叠的白色，红色，绿色和蓝色像素电极（WP，RP，GP，BP） 亚像素（SP）。

【Equation 1】

$$\Delta Vp = \frac{Cgs}{(Cgs+Cst+Clc)}\Delta Vg$$