



(12) **EUROPEAN PATENT APPLICATION**

(43) Date of publication:
31.12.2014 Bulletin 2015/01

(51) Int Cl.:
G02F 1/1362 (2006.01)

(21) Application number: **13195263.2**

(22) Date of filing: **02.12.2013**

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR
Designated Extension States:
BA ME

- **Song, Tae-Joon**
413-833 Gyeonggi-do (KR)
- **Lee, Kyu-Hwang**
138-747 Seoul (KR)
- **Lee, Kyung-Ha**
442-190 Gyeonggi-do (KR)

(30) Priority: **28.06.2013 KR 20130075901**

(74) Representative: **Viering, Jentschura & Partner**
Patent- und Rechtsanwälte
Am Brauhaus 8
01099 Dresden (DE)

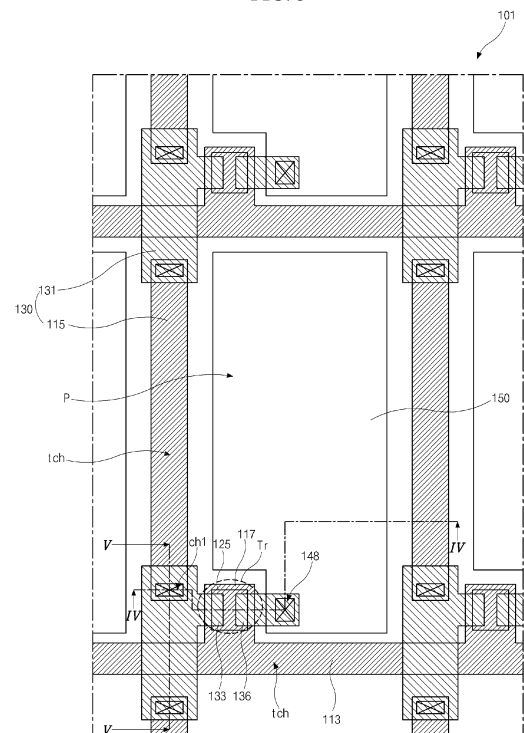
(71) Applicant: **LG Display Co., Ltd.**
Seoul 150-721 (KR)

(72) Inventors:
• **Moon, Tae-Hyoung**
411-764 Gyeonggi-do (KR)

(54) **Array substrate for liquid crystal display and method of fabricating the same**

(57) An array substrate includes: a trench having a depth from a surface of a substrate; a gate line, a gate electrode and a data pattern filling the respective trenches, wherein the data pattern is between the adjacent gate lines; a gate insulating layer on the gate line, the gate electrode and the data pattern, substantially flat over the substrate, and including contact holes that expose both ends of the data pattern, respectively; a data connection portion on the gate insulating layer and contacting the adjacent data patterns through the contact holes; a source electrode extending from the data connection portion, and a drain electrode spaced apart from the source electrode; a passivation layer on the source and drain electrodes and including a drain contact hole exposing the drain electrode; and a pixel electrode on the passivation layer and contacting the drain electrode through the drain contact hole.

FIG. 3



Description

[0001] The present invention claims the benefit of Korean Patent Application No. 10-2013-0075901, filed in Korea on June 28, 2013, which is hereby incorporated by reference for all purposes as if fully set forth herein.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention relates to an array substrate for a liquid crystal display, and more particularly, to an array substrate for a liquid crystal display and a method of fabricating the same.

Discussion of the Related Art

[0003] Recently, with the advent of an information-oriented society, the field of display devices configured to process and display a large amount of information has rapidly been developed. In particular, liquid crystal displays (LCDs) or organic light emitting diodes (OLEDs) have lately been developed as flat panel displays (FPDs) having excellent performance, such as a small thickness, light weight, and low power consumption, and has superseded conventional cathode-ray tubes (CRTs).

[0004] Among LCDs, an active matrix (AM)-type LCD including an array substrate having a TFT serving as a switching element capable of controlling on/off voltages of each of pixels may have excellent resolution and capability of embodying moving images.

[0005] Generally, the LCD is fabricated by fabricating an array substrate and a color filter substrate and interposing a liquid crystal layer between the array substrate and the color filter substrate.

[0006] FIG. 1 is an exploded perspective view illustrating an LCD or an OLED according to the related art.

[0007] Referring to FIG. 1, an array substrate 10 and a color filter substrate 20 is attached to each other with a liquid crystal layer 30 therebetween. The array substrate 10 includes a plurality of gate lines 14 and a plurality of data lines 16 to define a plurality of pixel regions P on a first substrate 12. A thin film transistor T is formed at the crossing portion of the gate and data lines 14 and 16 and is connected to a pixel electrode 18 in the pixel region P.

[0008] The color filter substrate 20 includes a black matrix 25 corresponding to the gate and data lines 14 and 16 and the thin film transistor T and surrounding the pixel region P, a color filter layer 26 including red (R), green (G) and blue (B) 26a, 26b and 26c arranged in the respective pixel regions P, and a common electrode 28 on the black matrix 25 and the color filter layer 26.

[0009] Although not shown in the drawings, a sealant is formed between the array substrate 10 and the color filter substrate 20 to prevent leakage of liquid crystal, alignment layers are formed on inner surfaces of the array

substrate 10 and the color filter substrate 20, respectively, and polarizers are located on outer surfaces of the array substrate 10 and the color filter substrate 20, respectively.

[0010] Moreover, a backlight unit is provided below the array substrate 10. A gate signal is sequentially supplied to the gate lines 14, then the corresponding thin film transistor T is turned on and a data signal is supplied to the data line 16 and then to the pixel electrode 18, and thus an electric field is produced between the pixel electrode 18 and the common electrode 28 to operate liquid crystal molecules of the liquid crystal layer 30, thereby displaying images.

[0011] FIG. 2 is a cross-sectional view illustrating an array substrate according to the related art.

[0012] Referring to FIG. 2, in the array substrate 10, a gate line (not shown) and a data line 16 cross each other to define a pixel region P, and a gate electrode 55 is formed in a switching region TrA of the pixel region P on a first substrate 11.

[0013] A gate insulating layer 58 is formed on the gate electrode 50, and a semiconductor layer 68 including an active layer 62 made of intrinsic amorphous silicon and an ohmic contact layer 66 made of impurity-doped amorphous silicon is formed on the gate insulating layer 58.

[0014] Source and drain electrodes 76 and 78 are spaced apart from each other and formed on the ohmic contact layer 66. The gate electrode 55, the gate insulating layer 58, the semiconductor layer 68 and the source and drain electrodes 76 and 78 form a thin film transistor Tr.

[0015] A passivation layer 82 is on the source and drain electrodes 76 and 78 and includes a drain contact hole 85 exposing the drain electrode 78. A pixel electrode 18 is formed on the passivation layer 82 in the pixel region P contacts the drain electrode 78 through the drain contact hole 85.

[0016] The gate line has predetermined thickness and width, and the data line 16 has predetermined thickness and width.

[0017] As size of the LCD increases, the gate line and the data line become longer. This causes increase of resistance of signal line, and thus signal delay occurs. Accordingly, signal deformation and operation defect are caused, and display quality is degraded.

[0018] To prevent such the signal delay, signal line is required to increase in thickness and/or width. However, in case of increase in width, aperture ratio is reduced. In case of increase in thickness, step portion becomes great, and this causes disconnection of a component over the signal line. Moreover, such the step portion causes vacant space at sides of the signal line, insulation capability is thus degraded, and thus short-circuit between the signal line and a conductive component to be formed later may occur.

SUMMARY OF THE INVENTION

[0019] Accordingly, the present invention is directed to an array substrate for an LCD and a method of fabricating the same which substantially obviates one or more of the problems due to limitations and disadvantages of the related art.

[0020] An advantage of the present invention is to provide an array substrate for an LCD and a method of fabricating the same that can reduce signal delay and step portion with increase of thickness of signal line.

[0021] Additional features and advantages of the present invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. These and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims thereof as well as the appended drawings.

[0022] To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described herein, an array substrate includes: a layer arrangement including a pixel region; a trench having a depth from a surface of the layer arrangement; a gate line, a gate electrode and a data pattern filling the respective trenches, wherein the data pattern is between the adjacent gate lines; a gate insulating layer on the gate line, the gate electrode and the data pattern, substantially flat over the layer arrangement, and including contact holes that expose both ends of the data pattern, respectively; a semiconductor layer on the gate insulating layer over the gate electrode; a data connection portion on the gate insulating layer and contacting the adjacent data patterns through the contact holes; a source electrode connected to the data connection portion, and a drain electrode spaced apart from the source electrode; a pixel electrode connected to the drain electrode.

[0023] In one or more embodiments, the layer arrangement comprises a substrate including the pixel region, wherein the surface of the layer arrangement is a surface of the substrate, and wherein the gate insulating layer is substantially flat over the substrate.

[0024] In one or more embodiments, the layer arrangement comprises a substrate including the pixel region, and a buffer layer on the substrate, wherein the surface of the layer arrangement is a surface of the buffer layer, and wherein the gate insulating layer is substantially flat over the substrate.

[0025] In one or more embodiments, the depth is equal to or less than a thickness of the buffer layer.

[0026] In one or more embodiments, the array substrate further comprises: a passivation layer on the source and drain electrodes and including a drain contact hole exposing the drain electrode, wherein the pixel electrode is on the passivation layer and contacts the drain electrode through the drain contact hole, and wherein the source electrode extends from the data connection

portion and on the semiconductor layer.

[0027] In one or more embodiments, the depth is about 0.5 μm to about 5 μm , and the gate line, the gate electrode and the data pattern have a thickness equal to the depth.

[0028] In another aspect, a method of fabricating an array substrate includes: providing a layer arrangement including a pixel region; etching the layer arrangement including the pixel region to form a trench having a depth from a surface of the layer arrangement; forming a gate line, a gate electrode and a data pattern filling the respective trenches, wherein the data pattern is between the adjacent gate lines; forming a gate insulating layer on the gate line, the gate electrode and the data pattern, the gate insulating layer being substantially flat over the layer arrangement; forming a semiconductor layer on the gate insulating layer over the gate electrode; patterning the gate insulating layer to form contact holes that expose both ends of the data pattern, respectively; forming a data connection portion on the gate insulating layer, the data connection portion contacting the adjacent data patterns through the contact holes, a source electrode connected to the data connection portion, and a drain electrode spaced apart from the source electrode; and forming a pixel electrode connected to the drain electrode.

[0029] In one or more embodiments, providing the layer arrangement comprises providing a substrate including the pixel region, wherein etching the layer arrangement comprises etching the substrate including the pixel region to form the trench having the depth from a surface of the substrate, and wherein the gate insulating layer is substantially flat over the substrate.

[0030] In one or more embodiments, etching the substrate including the pixel region to form the trench having the depth from the surface of the substrate, and forming the gate line, the gate electrode and the data pattern filling the respective trenches comprises: forming a photoresist pattern on the substrate and exposing a portion corresponding to the trench; etching the substrate using the photoresist pattern to form the trench; forming a catalytic layer on the trench and the photoresist pattern; removing the photoresist pattern, whereby the catalytic layer remains in the trench; and immersing the substrate having the catalytic layer remaining in the trench into a plating solution in which a metal material is dissolved and performing an electroless plating, thereby plating the metal material in the trench.

[0031] In one or more embodiments, providing the layer arrangement comprises forming a buffer layer on a substrate including the pixel region, wherein etching the layer arrangement comprises etching the buffer layer to form the trench having the depth from a surface of the buffer layer, and wherein the gate insulating layer is substantially flat over the buffer layer.

[0032] In one or more embodiments, etching the buffer layer to form the trench having the depth from the surface of the buffer layer, and forming the gate line, the gate electrode and the data pattern filling the respective

trenches comprises: forming a photoresist pattern on the buffer layer which exposes a portion corresponding to the trench; etching the buffer layer using the photoresist pattern to form the trench; forming a catalytic layer on the trench and the photoresist pattern; removing the photoresist pattern, whereby the catalytic layer remains in the trench; and immersing the substrate having the catalytic layer remaining in the trench into a plating solution in which a metal material is dissolved and performing an electroless plating, thereby plating the metal material in the trench.

[0033] In one or more embodiments, the depth is equal to or less than a thickness of the buffer layer.

[0034] In one or more embodiments, the catalytic layer is formed by coating Pd-Sn colloid or depositing Pd ion.

[0035] In one or more embodiments, the method further comprises: after forming a data connection portion on the gate insulating layer, forming a passivation layer on the source and drain electrodes, the passivation layer including a drain contact hole exposing the drain electrode, wherein the pixel electrode is on the passivation layer and contacts the drain electrode through the drain contact hole, and wherein the source electrode extends from the data connection portion and on the semiconductor layer.

[0036] In one or more embodiments, the depth is 0.5 μm to 5 μm .

[0037] In another aspect, an array substrate includes: a substrate including a pixel region; a trench having a depth from a surface of the substrate; a gate line, a gate electrode and a data pattern filling the respective trenches, wherein the data pattern is between the adjacent gate lines; a gate insulating layer on the gate line, the gate electrode and the data pattern, substantially flat over the substrate, and including contact holes that expose both ends of the data pattern, respectively; a semiconductor layer on the gate insulating layer over the gate electrode; a data connection portion on the gate insulating layer and contacting the adjacent data patterns through the contact holes; a source electrode connected to the data connection portion, and a drain electrode spaced apart from the source electrode; a pixel electrode connected to the drain electrode.

[0038] In one or more embodiments, the array substrate further comprises: a passivation layer on the source and drain electrodes and including a drain contact hole exposing the drain electrode, wherein the pixel electrode is on the passivation layer and contacts the drain electrode through the drain contact hole, and wherein the source electrode extends from the data connection portion and on the semiconductor layer.

[0039] In one or more embodiments, the depth is about 0.5 μm to about 5 μm , and the gate line, the gate electrode and the data pattern have a thickness equal to the depth.

[0040] In another aspect, an array substrate includes: a substrate including a pixel region; a buffer layer on the substrate and including a trench having a depth from a

surface of the buffer layer; a gate line, a gate electrode and a data pattern filling the respective trenches, wherein the data pattern is between the adjacent gate lines; a gate insulating layer on the gate line, the gate electrode and the data pattern, substantially flat over the substrate, and including contact holes that expose both ends of the data pattern, respectively; a semiconductor layer on the gate insulating layer over the gate electrode; a data connection portion on the gate insulating layer and contacting the adjacent data patterns through the contact holes; a source electrode connected to the data connection portion, and a drain electrode spaced apart from the source electrode; a pixel electrode connected to the drain electrode.

[0041] In one or more embodiments, the array substrate further comprises: a passivation layer on the source and drain electrodes and including a drain contact hole exposing the drain electrode, wherein the pixel electrode is on the passivation layer and contacts the drain electrode through the drain contact hole, and wherein the source electrode extends from the data connection portion and on the semiconductor layer.

[0042] In one or more embodiments, the depth is 0.5 μm to 5 μm , and the gate line, the gate electrode and the data pattern have a thickness that is the same as the depth.

[0043] In one or more embodiments, the depth is equal to or less than a thickness of the buffer layer.

[0044] In another aspect, a method of fabricating an array substrate includes: etching a substrate including a pixel region to form a trench having a depth from a surface of the substrate; forming a gate line, a gate electrode and a data pattern filling the respective trenches, wherein the data pattern is between the adjacent gate lines; forming a gate insulating layer on the gate line, the gate electrode and the data pattern, the gate insulating layer being substantially flat over the substrate; forming a semiconductor layer on the gate insulating layer over the gate electrode; patterning the gate insulating layer to form contact holes that expose both ends of the data pattern, respectively; forming a data connection portion on the gate insulating layer, the data connection portion contacting the adjacent data patterns through the contact holes, a source electrode connected to the data connection portion, and a drain electrode spaced apart from the source electrode; and forming a pixel electrode connected to the drain electrode.

[0045] In one or more embodiments, the method further comprises: after forming a data connection portion on the gate insulating layer, forming a passivation layer on the source and drain electrodes, the passivation layer including a drain contact hole exposing the drain electrode, wherein the pixel electrode is on the passivation layer and contacts the drain electrode through the drain contact hole, and wherein the source electrode extends from the data connection portion and on the semiconductor layer.

[0046] In one or more embodiments, etching the sub-

strate including the pixel region to form the trench having the depth from a surface of the substrate, and forming the gate line, the gate electrode and the data pattern filling the respective trenches comprises: forming a photoresist pattern on the substrate and exposing a portion corresponding to the trench; etching the substrate using the photoresist pattern to form the trench; forming a catalytic layer on the trench and the photoresist pattern; removing the photoresist pattern, whereby the catalytic layer remains in the trench; and immersing the substrate having the catalytic layer remaining in the trench into a plating solution in which a metal material is dissolved and performing an electroless plating, thereby plating the metal material in the trench.

[0047] In one or more embodiments, the depth is 0.5 μm to 5 μm .

[0048] In one or more embodiments, the catalytic layer is formed by coating Pd-Sn colloid or depositing Pd ion.

[0049] In another aspect, a method of fabricating an array substrate comprises: forming a buffer layer on a substrate including a pixel region; etching the buffer layer to form a trench having a depth from a surface of the buffer layer; forming a gate line, a gate electrode and a data pattern filling the respective trenches, wherein the data pattern is between the adjacent gate lines; forming a gate insulating layer on the gate line, the gate electrode and the data pattern, and substantially flat over the substrate; forming a semiconductor layer on the gate insulating layer over the gate electrode; patterning the gate insulating layer to form contact holes that expose both ends of the data pattern, respectively; forming a data connection portion on the gate insulating layer, which contacts the adjacent data patterns through the contact holes, a source electrode connected to the data connection portion, and a drain electrode spaced apart from the source electrode; and forming a pixel electrode connected to the drain electrode.

[0050] In one or more embodiments, the method further comprises: after forming a data connection portion on the gate insulating layer, forming a passivation layer on the source and drain electrodes, the passivation layer including a drain contact hole exposing the drain electrode, wherein the pixel electrode is on the passivation layer and contacts the drain electrode through the drain contact hole, and wherein the source electrode extends from the data connection portion and on the semiconductor layer.

[0051] In one or more embodiments, etching the buffer layer to form the trench having the depth from a surface of the buffer layer, and forming the gate line, the gate electrode and the data pattern filling the respective trenches comprises: forming a photoresist pattern on the buffer layer which exposes a portion corresponding to the trench; etching the buffer layer using the photoresist pattern to form the trench; forming a catalytic layer on the trench and the photoresist pattern; removing the photoresist pattern, whereby the catalytic layer remains in the trench; and immersing the substrate having the cat-

alytic layer remaining in the trench into a plating solution in which a metal material is dissolved and performing an electroless plating, thereby plating the metal material in the trench.

[0052] In one or more embodiments, the depth is equal to or less than a thickness of the buffer layer.

[0053] In one or more embodiments, the depth is 0.5 μm to 5 μm .

[0054] In one or more embodiments, the catalytic layer is formed by coating Pd-Sn colloid or depositing Pd ion.

[0055] In another aspect, an array substrate includes: a substrate including a pixel region; a trench having a depth from a surface of the substrate; a gate line, a gate electrode and a data pattern filling the respective trenches, wherein the data pattern is between the adjacent gate lines; a gate insulating layer on the gate line, the gate electrode and the data pattern, substantially flat over the substrate, and including contact holes that expose both ends of the data pattern, respectively; a semiconductor layer on the gate insulating layer over the gate electrode; a data connection portion on the gate insulating layer and contacting the adjacent data patterns through the contact holes; a source electrode extending from the data connection portion and on the semiconductor layer, and a drain electrode spaced apart from the source electrode; a passivation layer on the source and drain electrodes and including a drain contact hole exposing the drain electrode; and a pixel electrode on the passivation layer and contacting the drain electrode through the drain contact hole.

[0056] In another aspect, an array substrate includes: a substrate including a pixel region; a buffer layer on the substrate and including a trench having a depth from a surface of the buffer layer; a gate line, a gate electrode and a data pattern filling the respective trenches, wherein the data pattern is between the adjacent gate lines; a gate insulating layer on the gate line, the gate electrode and the data pattern, substantially flat over the substrate, and including contact holes that expose both ends of the data pattern, respectively; a semiconductor layer on the gate insulating layer over the gate electrode; a data connection portion on the gate insulating layer and contacting the adjacent data patterns through the contact holes; a source electrode extending from the data connection portion and on the semiconductor layer, and a drain electrode spaced apart from the source electrode; a passivation layer on the source and drain electrodes and including a drain contact hole exposing the drain electrode; and a pixel electrode on the passivation layer and contacting the drain electrode through the drain contact hole.

[0057] In yet another aspect, a method of fabricating an array substrate includes: etching a substrate including a pixel region to form a trench having a depth from a surface of the substrate; forming a gate line, a gate electrode and a data pattern filling the respective trenches, wherein the data pattern is between the adjacent gate lines; forming a gate insulating layer on the gate line, the gate electrode and the data pattern, and the gate insu-

lating layer being substantially flat over the substrate; forming a semiconductor layer on the gate insulating layer over the gate electrode; patterning the gate insulating layer to form contact holes that expose both ends of the data pattern, respectively; forming a data connection portion on the gate insulating layer and contacting the adjacent data patterns through the contact holes, a source electrode extending from the data connection portion and on the semiconductor layer, and a drain electrode spaced apart from the source electrode; forming a passivation layer on the source and drain electrodes and including a drain contact hole exposing the drain electrode; and forming a pixel electrode on the passivation layer and contacting the drain electrode through the drain contact hole.

[0058] In yet another aspect, a method of fabricating an array substrate includes: forming a buffer layer on a substrate including a pixel region; etching the buffer layer to form a trench having a depth from a surface of the buffer layer; forming a gate line, a gate electrode and a data pattern filling the respective trenches, wherein the data pattern is between the adjacent gate lines; forming a gate insulating layer on the gate line, the gate electrode and the data pattern, and substantially flat over the substrate; forming a semiconductor layer on the gate insulating layer over the gate electrode; patterning the gate insulating layer to form contact holes that expose both ends of the data pattern, respectively; forming a data connection portion on the gate insulating layer and contacting the adjacent data patterns through the contact holes, a source electrode extending from the data connection portion and on the semiconductor layer, and a drain electrode spaced apart from the source electrode; forming a passivation layer on the source and drain electrodes and including a drain contact hole exposing the drain electrode; and forming a pixel electrode on the passivation layer and contacting the drain electrode through the drain contact hole.

[0059] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0060] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention.

[0061] In the drawings:

FIG. 1 is an exploded perspective view illustrating an LCD or an OLED according to the related art;

FIG. 2 is a cross-sectional view illustrating an array substrate according to the related art;

FIG. 3 is a plan view illustrating an array substrate of an LCD according to a first embodiment of the present invention;

FIG. 4 is a cross-sectional view taken along a line, IV-IV of FIG. 3;

FIG. 5 is a cross-sectional view taken along a line, V-V of FIG. 3;

FIG. 6 is a cross-sectional view illustrating an array substrate of an LCD according to a second embodiment of the present invention;

FIGs. 7A to 7G are plan views illustrating a method of fabricating the array substrate of the LCD according to the first embodiment;

FIGs. 8A to 8K are cross-sectional views taken along a line VIII-VIII of FIGs. 7A to 7G;

FIGs. 9A to 9K are cross-sectional views taken along a line IX-IX of FIGs. 7A to 7G; and

FIGs. 10A to 10E are cross-sectional views illustrating a method of fabricating the array substrate of the LCD according to the second embodiment.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

[0062] Reference will now be made in detail to the illustrated embodiments of the present invention, which are illustrated in the accompanying drawings.

[0063] FIG. 3 is a plan view illustrating an array substrate of an LCD according to a first embodiment of the present invention, FIG. 4 is a cross-sectional view taken along a line, IV-IV of FIG. 3, and FIG. 5 is a cross-sectional view taken along a line, V-V of FIG. 3. For the purpose of explanation, a region where a thin film transistor Tr as a switching element is formed in a pixel region P is referred to as a switching region TrA.

[0064] Referring to FIGs. 3 to 5, trenches tch are formed in an insulation substrate 110 as a base of an array substrate 101. For example, the trenches tch are located at a region where a gate line 113 and a gate electrode 117 are formed, and a part, except for a crossing part of the gate line 113 and the data line 130 and a part to a predetermined distance from the crossing portion, out of a region where a data line 130 is formed.

[0065] It is preferred, but not required that the trench tch may have a depth of about 0.5 to 5 μm , and the trenches tch for the gate line 113 and the data line 130 may have respective widths which a gate line or data line of a common array substrate has.

[0066] In the substrate 110, the gate line 113, the gate electrode 117 and a data pattern 115 fill the respective trenches tch. The gate line 113, the gate electrode 117

and the data pattern 115 may have a single-layered structure made of the same material, for example, one of aluminum (Al), aluminum alloy (e.g., AlNd), copper (Cu) and copper alloy. The data pattern 115 is located between adjacent gate lines 113.

[0067] The gate line 113, the gate electrode 117 and the data pattern 115 may have a thickness which is the same as the depth of the trench tch. Accordingly, the surface of the gate line 113, the gate electrode 117 and a data pattern 115 may be substantially even with respect to the surface of the substrate 110.

[0068] Accordingly, even when the gate line 113, the gate electrode 117 and the data pattern 115 have a thickness much greater than that of the gate line and the data line the related art, a step portion protruding upward from the surface of the substrate 110 is hardly formed. Thus, components to be formed later are not substantially affected by the gate line 113, the gate electrode 117 and the data pattern 115.

[0069] A gate insulating layer 120 is formed on the entire surface of the substrate 110 having the gate line 113, the gate electrode 117 and the data pattern 115 therein. The gate insulating layer 120 may be made of an inorganic insulating material, for example, silicon oxide (SiO₂) or silicon nitride (SiNx).

[0070] The gate insulating layer 120 is substantially even because the surface of the substrate therebelow having the gate line 113, the gate electrode 117 and the data pattern 115 is substantially even. The gate insulating layer 120 has first contact holes ch1 exposing ends of the data pattern 115.

[0071] A semiconductor layer 125 is formed on the gate insulating layer in the switching region TrA corresponding to the gate electrode 117.

[0072] The semiconductor layer 125 includes an active layer 125a made of intrinsic amorphous silicon, and an ohmic contact layer 125b made of impurity-doped amorphous silicon exposing a center portion of the active layer 125a.

[0073] A data connection portion 131, and source and drain electrodes 133 and 136 are formed on the gate insulating layer 120 and the semiconductor layer 125. The data connection portion 131, and the source and drain electrodes 133 and 136 may have a single-layered or multi-layered structure using at least one of aluminum (Al), aluminum alloy (e.g., AlNd), copper (Cu), copper alloy, molybdenum (Mo), and molybdenum alloy (e.g., MoTi). The data connection portion 131 may be a data connection pattern, for example. The data connection portion 131 overlap the adjacent data patterns 115 at both sides thereof and the gate line 113, and contacts the data patterns 115 at both sides thereof through the first contact holes ch1. The source electrode 133 is connected to the data connection portion 131. More particularly, the source electrode 133 extends from the data connection portion 131 and is located on the ohmic contact layer 125b. The drain electrode 136 is spaced apart from the source electrode 133 and located on the ohmic

contact layer 125b.

[0074] The data patterns 115 formed at the trenches tch and the data connection portion 131 form the data line 130 extending along a direction crossing the gate line 113.

[0075] The gate electrode 117, the gate insulating layer 120, the semiconductor layer 125, and the source and drain electrodes 133 and 136 form the thin film transistor Tr.

[0076] A passivation layer is formed on the data connection portion 131 and the source and drain electrodes 133 and 136. The passivation layer includes a drain contact hole 148 exposing the drain electrode 136.

[0077] The passivation layer may a single-layered structure using inorganic insulating material or organic insulating material, or a double-layered structure made using inorganic insulating material and organic insulating material. In this embodiment, for the purpose of explanation, the passivation layer has a double-layered structure with a first layer 140 made of inorganic insulating material, and a second layer 145 made of organic insulating material and thus having an even surface.

[0078] In this regard, when the active layer 125a contacts organic insulating material, a channel portion of the active layer 125a is contaminated by the organic insulating material, and thus property of the thin film transistor Tr may be degraded. To prevent this problem, the first layer 140 of inorganic insulating material is first formed and then the second layer 145 of organic insulating material is formed thereon.

[0079] Further, using the second layer 145 of organic insulating material may be advantageous to operation of particular LCDs. In this regard, among various modes of LCDs such as twist nematic mode, in-plane switching mode, fringe field mode, etc., the in-plane switching mode LCD and fringe field mode LCD prefer a pixel electrode formed on a flat surface for uniformity and efficiency of production of electric field, and in consideration of this, the second layer 145 is employed to produce a flat surface.

[0080] A pixel electrode 150 is formed on the second layer 145 and contacts the drain electrode 136 through the drain contact hole 148. The pixel electrode 150 may be made of a transparent conductive material, for example, indium-tin-oxide (ITO) or indium-zinc-oxide (IZO).

[0081] However, the passivation layer can be omitted. And in this case, the pixel electrode 150 can be formed on, e.g., drain electrode 136 and connected to the drain electrode 136.

[0082] The pixel electrode 150 may have a plate shape in the pixel region P, and in this case, the array substrate 110 may be used as an array substrate for a twist nematic mode LCD.

[0083] However, the pixel electrode 150 may have other shapes according to the modes of LCDs. For example, in case that the array substrate 101 is used for an in-plane switching mode LCD, the pixel electrode 150 may be configured to have a plurality of bars spaced apart

from one another, and a common electrode may be configured to have a plurality of another bars alternating with the bars of the pixel electrode 150 to produce an in-plane electric field. In this case, the common electrode is connected to a common line, and the common line may be formed in the substrate 110 filling a corresponding trench that is spaced apart from and parallel with the gate line 113.

[0084] Alternatively, in case that the array substrate 110 is used for a fringe field mode LCD, the pixel electrode 150 may be configured to have a plate shape, and a common electrode may be configured to have a plurality of bar-shaped openings to produce an in-plane electric field. In this case, the common electrode may be formed over the pixel electrode 150 with an insulating layer therebetween.

[0085] As described above, because of the trench tch, the array substrate 101 can use the gate line 113 and the data line 130 several times to tens of times thicker than those of the related art. Accordingly, even when display area increases and the signal line becomes longer, thickness increases and thus resistance is reduced. Therefore, signal delay can be prevented.

[0086] Moreover, even when the thickness of the gate line 113 and the data line 130 increases, a step portion due to this is not produced. Accordingly, disconnection of a component over the signal line or a vacant space near the signal line due to the step portion is prevented. Therefore, product defect rate and production cost can be reduced.

[0087] FIG. 6 is a cross-sectional view illustrating an array substrate of an LCD according to a second embodiment of the present invention.

[0088] The array substrate 202 of the second embodiment is similar to the array substrate 101 of the first embodiment but is different in the trench tch. Explanation of parts similar to parts of the first embodiment may be omitted.

[0089] The trench tch of the first embodiment is formed in the substrate 110 while the trench tch of the second embodiment is formed in a buffer layer 112 on the substrate 110. The buffer layer 112 may be made of inorganic or organic insulating material.

[0090] A gate line 113, a gate electrode 117 and a data pattern 115 fill the corresponding trenches tch in the buffer layer 112. The surface of the gate line 113, the gate electrode 117 and the data pattern 115 may be substantially even with respect to the surface of the buffer layer 112.

[0091] The trench tch may be configured to open the surface of the substrate 110 therebelow. Alternatively, the trench tch may be configured to have a depth less than a thickness of the buffer layer 112.

[0092] The layered structure over the gate line 113, the gate electrode 117 and the data pattern 115 is similar to that of the first embodiment.

[0093] The array substrate 201 of the second embodiment can have the same advantages as that of the first

embodiment 101.

[0094] Methods of fabricating the array substrates according to the first and second embodiments are explained as below.

[0095] FIGs. 7A to 7G are plan views illustrating a method of the array substrate of the LCD according to the first embodiment, FIGs. 8A to 8K are cross-sectional views taken along a line VIII-VIII of FIGs. 7A to 7G, and FIGs. 9A to 9K are cross-sectional views taken along a line IX-IX of FIGs. 7A to 7G.

[0096] Referring to FIGs. 7A, 8A and 9A, a first photoresist layer is formed on a substrate 110 which is made of, for example, glass or plastic, and then light exposure and developing are performed to form a first photoresist pattern 181 at regions except for regions where a gate line 113, a gate electrode 117 and a data pattern 115 are formed. In other words, the first photoresist pattern 181 exposes the regions where the gate line 113, the gate electrode 117 and the data pattern 115 are formed.

[0097] Referring to FIGs. 7A, 8B and 9B, the substrate 110 is etched using the first photoresist pattern 181 to form trenches tch. The trench tch may have a width of about 5 μm to about 15 μm and a depth 0.5 μm to 5 μm .

[0098] The trench tch corresponding to the gate line 113 extends without disconnection along a first direction that is an extension direction of the gate line 113. The trench tch corresponding to the data pattern 115 extends along a second direction crossing the first direction and is separated with respect to each trench tch for the gate line 113.

[0099] Referring to FIGs. 7A, 8C and 9C, a catalytic layer 185 is formed entirely on the substrate 110 having the first photoresist pattern 181. For example, the catalytic layer 185 may be made of palladium (Pd) group material, and may be formed by coating Pd-Sn colloid or depositing Pd ion (e.g., Pd^{2+}).

[0100] Referring to FIGs. 7A, 8D and 9D, a stripping process is performed to remove the first photoresist layer 181.

[0101] Accordingly, the catalytic layer 185 on the first photoresist pattern 181 is removed, and thus the catalytic layer 185 remains on an inner surface of the trench tch, and the surface of the substrate 110 outside the trench tch is exposed without the catalytic layer 185 thereon.

[0102] Referring to FIGs. 7B, 8E and 9E, the substrate 110 having the catalytic layer 185 in the trench tch is immersed in a tank 195 containing a plating solution in which at least one metal material of low resistance, for example, at least one of aluminum (Al), aluminum alloy, copper and copper alloy ion is dissolved, and electroless plating is performed.

[0103] Through the electroless plating, metal ion is selectively plated in the trench tch having the catalytic layer 185 therein but is not plated on the surface of the substrate 110 not having the catalytic layer 185.

[0104] Accordingly, when the electroless plating is finished, the gate line 113, the gate electrode 117 and the data pattern 115 are formed filling the corresponding

trenches tch.

[0105] Referring to FIGs. 7B, 8F and 9F, a gate insulating layer 120 is formed entirely on the substrate 110 having the gate line 113, the gate electrode 117 and the data pattern 115. The gate insulating layer 120 may be made of inorganic insulating material, for example, silicon oxide (SiO₂) or silicon nitride (SiN_x).

[0106] The gate insulating layer 120 is substantially flat without a step portion on the substrate 110 because the surface of the gate line 113, the gate electrode 117 and the data pattern 115 below the gate insulating layer is substantially even with the surface of the substrate 110.

[0107] Referring to FIGs. 7C, 8G and 9G, intrinsic amorphous silicon layer and impurity-doped amorphous silicon layer are formed on the gate insulating layer 120, and then a mask process is performed to form an active layer 125a and an impurity-doped amorphous silicon pattern 124 on the active layer 125a.

[0108] Referring to FIGs. 7D, 8H and 9H, a mask process is performed for the substrate 110 having the active layer 125a and the impurity-doped amorphous silicon pattern 124 to remove portions of the gate insulating layer 120 corresponding to ends of the data pattern 115 and form a first contact hole ch1 exposing each of both ends of the data pattern 115.

[0109] Referring to FIG. 7E, 8I and 9I, a second metal layer is formed on the substrate 110 having the first contact hole ch1. The second metal layer may be formed by depositing at least one from a metal material group including aluminum (Al), aluminum alloy, copper, copper alloy, molybdenum and molybdenum alloy.

[0110] A mask process is performed for the second metal layer to form a data connection portion 131, and source and drain electrodes 133 and 136. The data connection portion 131 crosses the corresponding gate line 113, and contacts the data patterns 115 at both sides thereof through the respective first contact hole ch1 to connect the data patterns 115. The source electrode 133 branches off from the data connection portion 131, and the drain electrode 136 is spaced apart from the source electrode 133. The source and drain electrodes 133 and 136 are formed on the impurity-doped amorphous silicon pattern 124.

[0111] The data pattern 115 and the data connection portion 131 are alternated and connected along the second direction to form each data line 130.

[0112] Then, a portion of the impurity-doped amorphous silicon pattern 124 exposed between the source and drain electrodes 133 and 136 are removed to form an ohmic contact layer 125b below each of the source and drain electrodes 133 and 136 and expose a center portion of the active layer 125a.

[0113] The active layer 125a and the ohmic contact layer 125b form a semiconductor layer 125. The gate electrode 117, the gate insulating layer 120, the semiconductor layer 125 and the source and drain electrodes 133 and 136 in the switching region TrA form a thin film transistor Tr.

[0114] Referring to FIGs. 7F, 8J and 9J, a first passivation layer 140 is formed on the substrate 110 having the source and drain electrodes 133 and 136, and then a second passivation layer 145 is formed on the first passivation layer 140. The first passivation layer 140 may be made of inorganic insulating material, for example, silicon oxide (SiO₂) or silicon nitride (SiN_x), and the second passivation layer 145 may be made of organic insulating material, for example, photo acryl.

[0115] A mask process is performed for the first and second passivation layer 140 and 145 to form a drain contact hole 148 exposing the drain electrode 136.

[0116] Referring to FIGs. 7G, 8K and 9K, a transparent conductive material layer is formed on the second passivation layer 145 and patterned in a mask process to form a pixel electrode 150 in the pixel region P. The pixel electrode 150 contacts the drain electrode 136 through the drain contact hole 148.

[0117] However, the passivation layers can be omitted. And in this case, the transparent conductive material layer can be formed on, e.g., drain electrode 136 and patterned in a mask process to form a pixel electrode 150 in the pixel region P. The pixel electrode 150 is connected to the drain electrode 136.

[0118] Through the above-described processes, the array substrate 101 can be fabricated. The array substrate 101 as above may be used for a twisted nematic mode LCD.

[0119] Alternatively, the pixel electrode 150 is formed to have a plurality of bars in the pixel region and a common electrode may be formed, in the same process of forming the pixel electrode 150, to have a plurality of another bars alternating with the bars of the pixel electrode 150. The array substrate 110 having such the configuration may be used for an in-plane switching mode LCD.

[0120] In case of the array substrate 110 for the in-plane switching mode LCD, a common line may be formed in the process of forming the gate line 113, a common contact hole may be formed in the process of forming the drain contact hole 148 of the passivation layers 140 and 145, and the common electrode may contact the common line through the common contact hole.

[0121] Alternatively, after forming the pixel electrode 150, then an insulating layer is formed on the pixel electrode 150, and then a common electrode is formed on the insulating layer to have a plurality of bar-shaped openings over the pixel electrode 150. The array substrate 110 having such the configuration may be used for a fringe field mode LCD.

[0122] FIGs. 10A to 10E are cross-sectional views illustrating a method of the array substrate of the LCD according to the second embodiment.

[0123] The method of fabricating the array substrate of the second embodiment includes forming a trench in a buffer layer other than a substrate, and the processes after forming the trench in the buffer layer is similar to are similar to those of the first embodiment and explanations thereof may be omitted.

[0124] Referring to FIG. 10A, a buffer layer 112 is formed on a substrate 110. The buffer layer 112 may be made of inorganic insulating material, for example, silicon oxide (SiO₂) or silicon nitride (SiN_x), or organic insulating material, for example, photo acryl, polyimide or polystyrene.

[0125] The buffer layer 112 may have a thickness equal to or more than that of a gate line 113, a gate electrode 117 and a data pattern 115 to be formed later.

[0126] Then, a photoresist layer is formed on the buffer layer 112 and patterned in a mask process to form a first photoresist pattern 181 at regions except for regions where the gate line 113, the gate electrode 117 and the data pattern 115 are formed. In other words, the first photoresist pattern 181 exposes the regions where the gate line 113, the gate electrode 117 and the data pattern 115 are formed.

[0127] Referring to FIG. 10B, the buffer layer 112 is etched using the first photoresist pattern 181 as an etching mask to form a trench tch. The trench tch may have a depth about 0.5 μm to 5 μm. The trench tch may expose the substrate 110 by completely removing the buffer layer 112 or may not expose the substrate 110 by partially removing the buffer layer 112.

[0128] Referring to FIG. 10C, a catalytic layer 185 is formed entirely on the first photoresist pattern 181 and in the trench tch. For example, the catalytic layer 185 may be made of palladium (Pd) group material, and may be formed by coating Pd-Sn colloid or depositing Pd ion (e.g., Pd²⁺).

[0129] Referring to FIG. 10D, a stripping process is performed to remove the first photoresist layer 181.

[0130] Accordingly, the catalytic layer 185 on the first photoresist pattern 181 is removed, and thus the catalytic layer 185 remains on an inner surface of the trench tch, and the surface of the buffer layer 112 outside the trench tch is exposed without the catalytic layer 185 thereon.

[0131] Referring to FIGs. 10E, the substrate 110 having the catalytic layer 185 in the trench tch is immersed in a tank 195 containing a plating solution in which at least one metal material of low resistance, for example, at least one of aluminum (Al), aluminum alloy, copper and copper alloy ion is dissolved, and electroless plating is performed.

[0132] Through the electroless plating, metal ion is selectively plated in the trench tch having the catalytic layer 185 therein but is not plated on the surface of the buffer layer 112 not having the catalytic layer 185.

[0133] Accordingly, when the electroless plating is finished, the gate line 113, the gate electrode 117 and the data pattern 115 are formed filling the corresponding trenches tch.

[0134] The post processes may be described with reference to the method of the first embodiment.

[0135] As described above, because of the trench tch, the array substrate 101 can use the gate line and the data line several times to tens of times thicker than those of the related art. Accordingly, even when display area

increases and the signal line becomes longer, thickness increases and thus resistance is reduced. Therefore, signal delay can be prevented.

[0136] Moreover, even when the thickness of the gate line and the data line increases, a step portion due to this is not produced. Accordingly, disconnection of a component over the signal line or a vacant space near the signal line due to the step portion is prevented. Therefore, product defect rate and production cost can be reduced.

[0137] It will be apparent to those skilled in the art that various modifications and variations can be made in the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

Claims

1. An array substrate comprising:

a layer arrangement including a pixel region;
a trench having a depth from a surface of the layer arrangement;
a gate line, a gate electrode and a data pattern filling the respective trenches, wherein the data pattern is between the adjacent gate lines;
a gate insulating layer on the gate line, the gate electrode and the data pattern, substantially flat over the layer arrangement, and including contact holes that expose both ends of the data pattern, respectively;
a semiconductor layer on the gate insulating layer over the gate electrode;
a data connection portion on the gate insulating layer and contacting the adjacent data patterns through the contact holes;
a source electrode connected to the data connection portion, and a drain electrode spaced apart from the source electrode;
a pixel electrode connected to the drain electrode.

2. The array substrate of claim 1, wherein the layer arrangement comprises a substrate including the pixel region, wherein the surface of the layer arrangement is a surface of the substrate, and wherein the gate insulating layer is substantially flat over the substrate.

3. The array substrate of claim 1, wherein the layer arrangement comprises a substrate including the pixel region, and a buffer layer on the substrate, wherein the surface of the layer arrangement is a surface of the buffer layer, and wherein the gate insulating layer is substantially flat

over the substrate.

4. The array substrate according to claim 3, wherein the depth is equal to or less than a thickness of the buffer layer.

5. The array substrate according to any one of claims 1 to 4, further comprising:

a passivation layer on the source and drain electrodes and including a drain contact hole exposing the drain electrode, wherein the pixel electrode is on the passivation layer and contacts the drain electrode through the drain contact hole, and wherein the source electrode extends from the data connection portion and on the semiconductor layer.

6. The array substrate according to any one of claims 1 to 5, wherein the depth is about 0.5 μm to about 5 μm , and the gate line, the gate electrode and the data pattern have a thickness equal to the depth.

7. A method of fabricating an array substrate comprising:

providing a layer arrangement including a pixel region;
etching the layer arrangement including the pixel region to form a trench having a depth from a surface of the layer arrangement;
forming a gate line, a gate electrode and a data pattern filling the respective trenches, wherein the data pattern is between the adjacent gate lines;
forming a gate insulating layer on the gate line, the gate electrode and the data pattern, the gate insulating layer being substantially flat over the layer arrangement;
forming a semiconductor layer on the gate insulating layer over the gate electrode;
patterning the gate insulating layer to form contact holes that expose both ends of the data pattern, respectively;
forming a data connection portion on the gate insulating layer, the data connection portion contacting the adjacent data patterns through the contact holes, a source electrode connected to the data connection portion, and a drain electrode spaced apart from the source electrode;
and
forming a pixel electrode connected to the drain electrode.

8. The method of claim 7, wherein providing the layer arrangement comprises providing a substrate including the pixel region,

wherein etching the layer arrangement comprises etching the substrate including the pixel region to form the trench having the depth from a surface of the substrate, and wherein the gate insulating layer is substantially flat over the substrate.

9. The method according to claim 8, wherein etching the substrate including the pixel region to form the trench having the depth from the surface of the substrate, and forming the gate line, the gate electrode and the data pattern filling the respective trenches comprises:

forming a photoresist pattern on the substrate and exposing a portion corresponding to the trench;
etching the substrate using the photoresist pattern to form the trench;
forming a catalytic layer on the trench and the photoresist pattern;
removing the photoresist pattern, whereby the catalytic layer remains in the trench; and
immersing the substrate having the catalytic layer remaining in the trench into a plating solution in which a metal material is dissolved and performing an electroless plating, thereby plating the metal material in the trench.

10. The method of claim 7, wherein providing the layer arrangement comprises forming a buffer layer on a substrate including the pixel region, wherein etching the layer arrangement comprises etching the buffer layer to form the trench having the depth from a surface of the buffer layer, and wherein the gate insulating layer is substantially flat over the buffer layer.

11. The method according to claim 10, wherein etching the buffer layer to form the trench having the depth from the surface of the buffer layer, and forming the gate line, the gate electrode and the data pattern filling the respective trenches comprises:

forming a photoresist pattern on the buffer layer which exposes a portion corresponding to the trench;
etching the buffer layer using the photoresist pattern to form the trench;
forming a catalytic layer on the trench and the photoresist pattern;
removing the photoresist pattern, whereby the catalytic layer remains in the trench; and
immersing the substrate having the catalytic layer remaining in the trench into a plating solution in which a metal material is dissolved and performing an electroless plating, thereby plating the metal material in the trench.

12. The method according to claim 10 or 11, wherein the depth is equal to or less than a thickness of the buffer layer.
13. The method of claim 9 or 11, wherein the catalytic layer is formed by coating Pd-Sn colloid or depositing Pd ion. 5
14. The method according to any one of claims 7 to 13, further comprising: 10
- after forming a data connection portion on the gate insulating layer, forming a passivation layer on the source and drain electrodes, the passivation layer including a drain contact hole exposing the drain electrode, 15
- wherein the pixel electrode is on the passivation layer and contacts the drain electrode through the drain contact hole, and
- wherein the source electrode extends from the data connection portion and on the semiconductor layer. 20
15. The method according to any one of claims 7 to 14, wherein the depth is 0.5 μm to 5 μm . 25

30

35

40

45

50

55

FIG. 1
RELATED ART

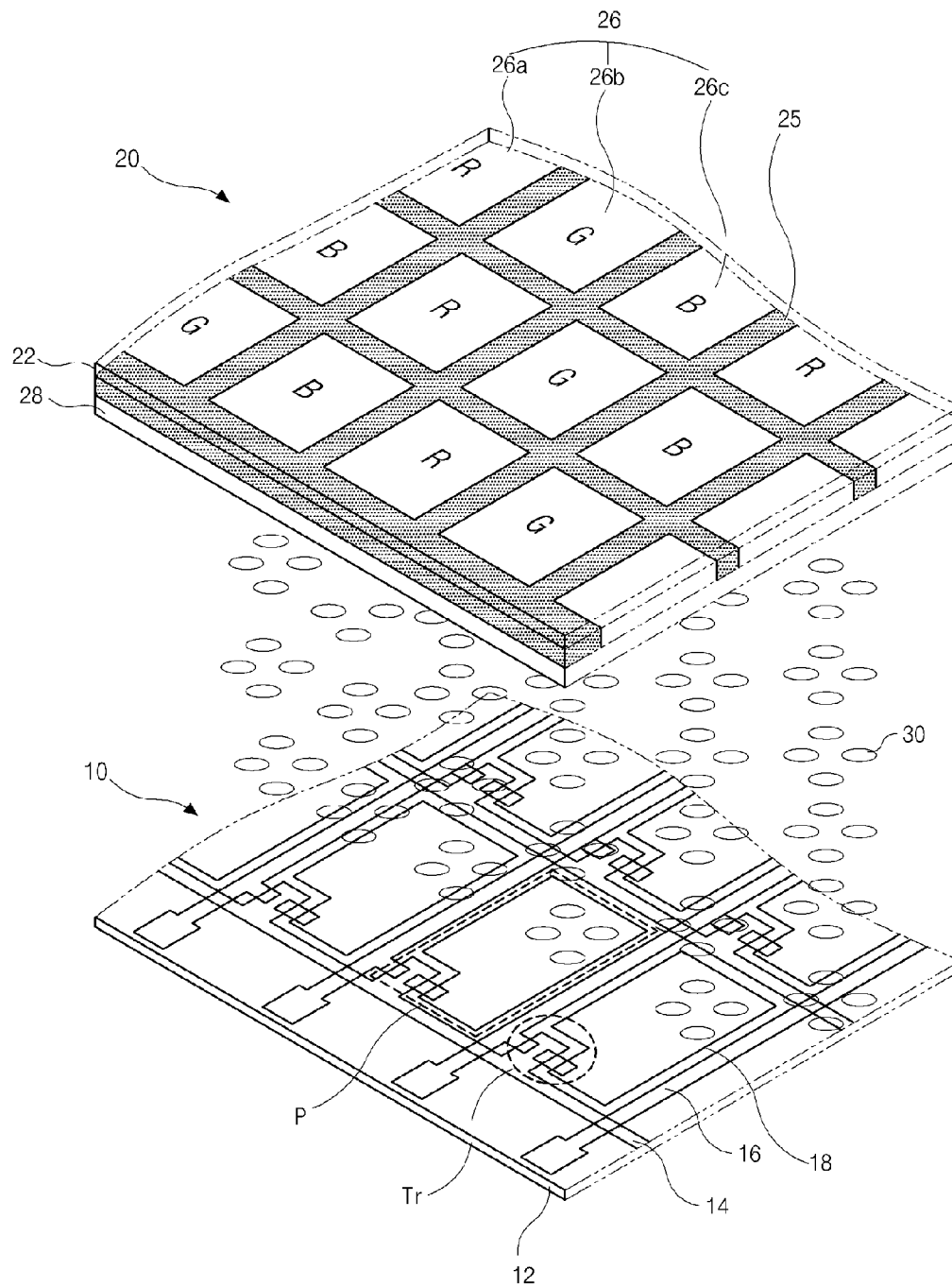


FIG. 2
RELATED ART

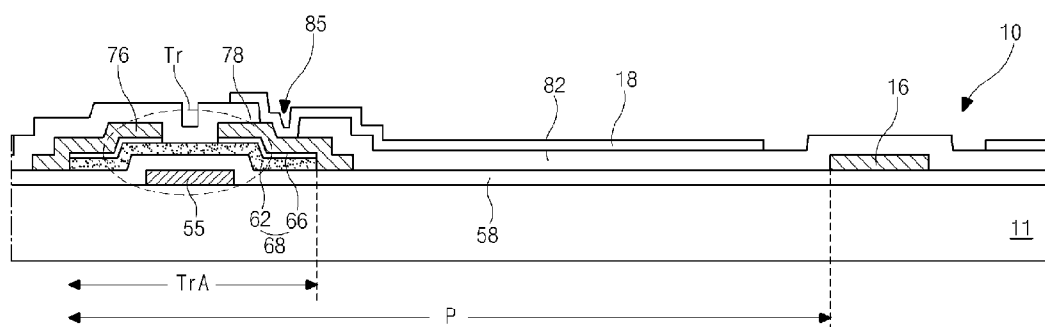


FIG. 3

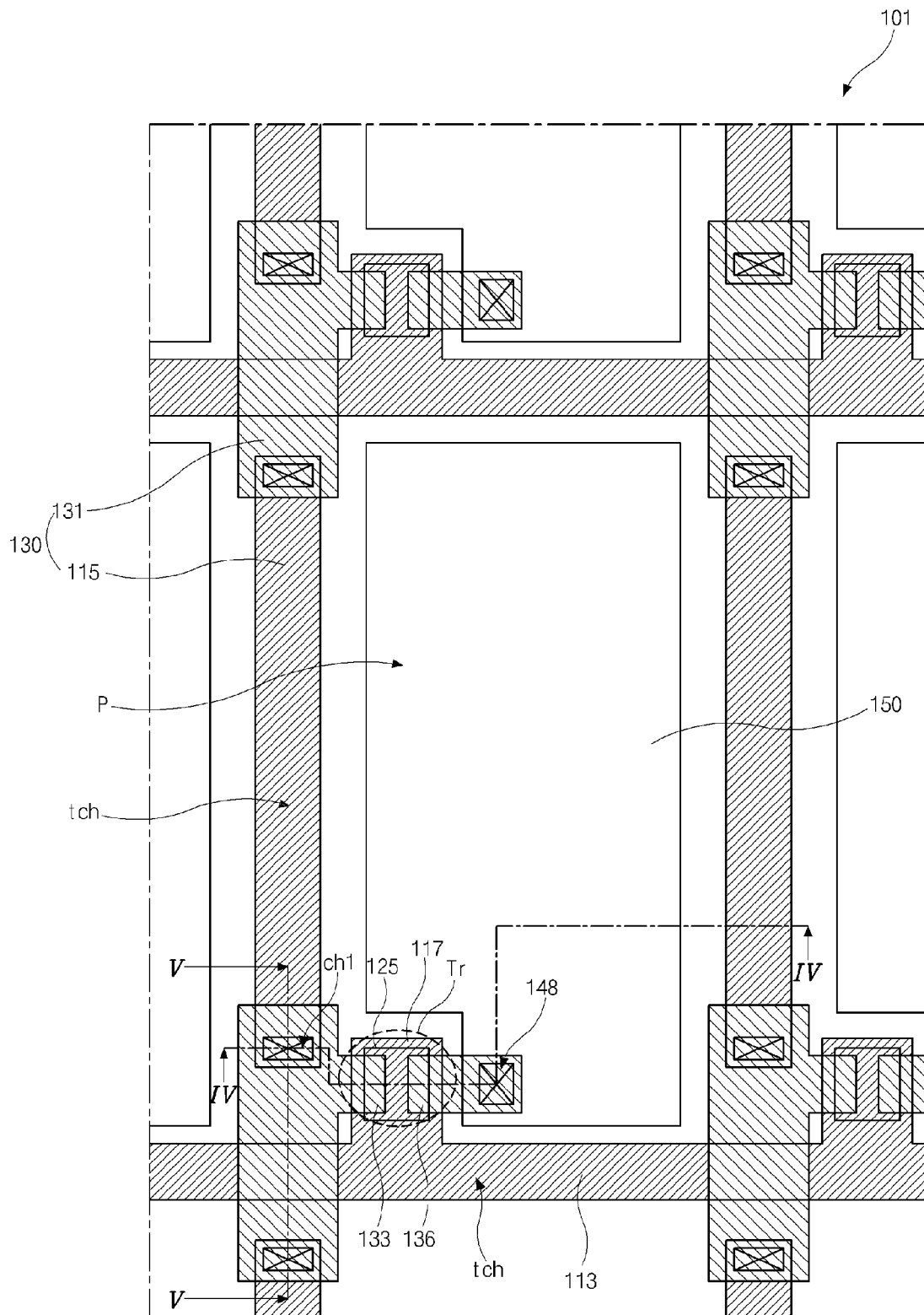


FIG. 4

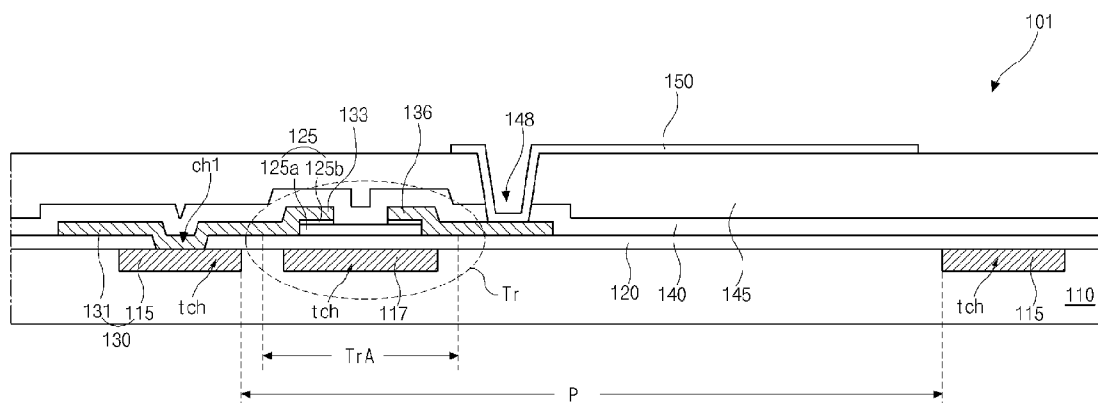


FIG. 5

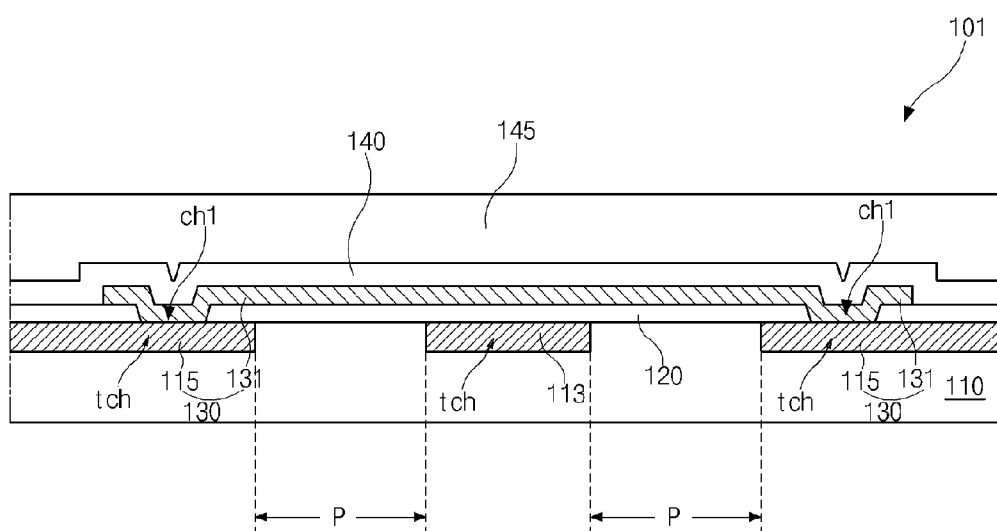


FIG. 6

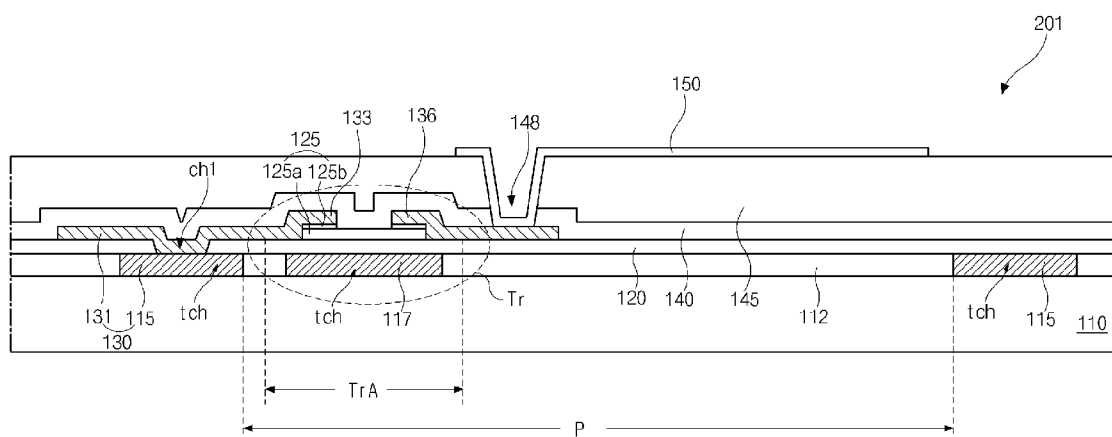


FIG. 7A

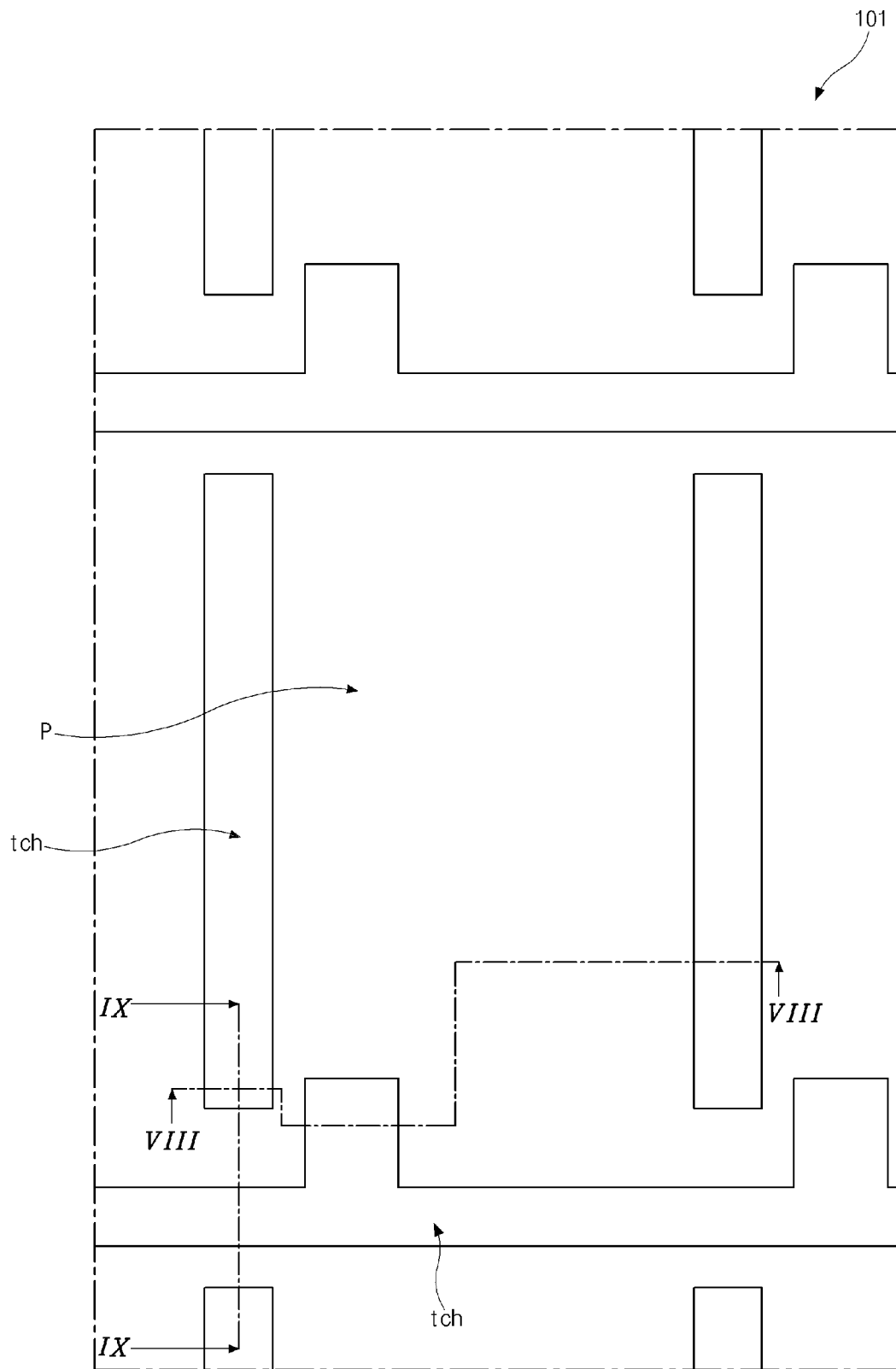


FIG. 7B

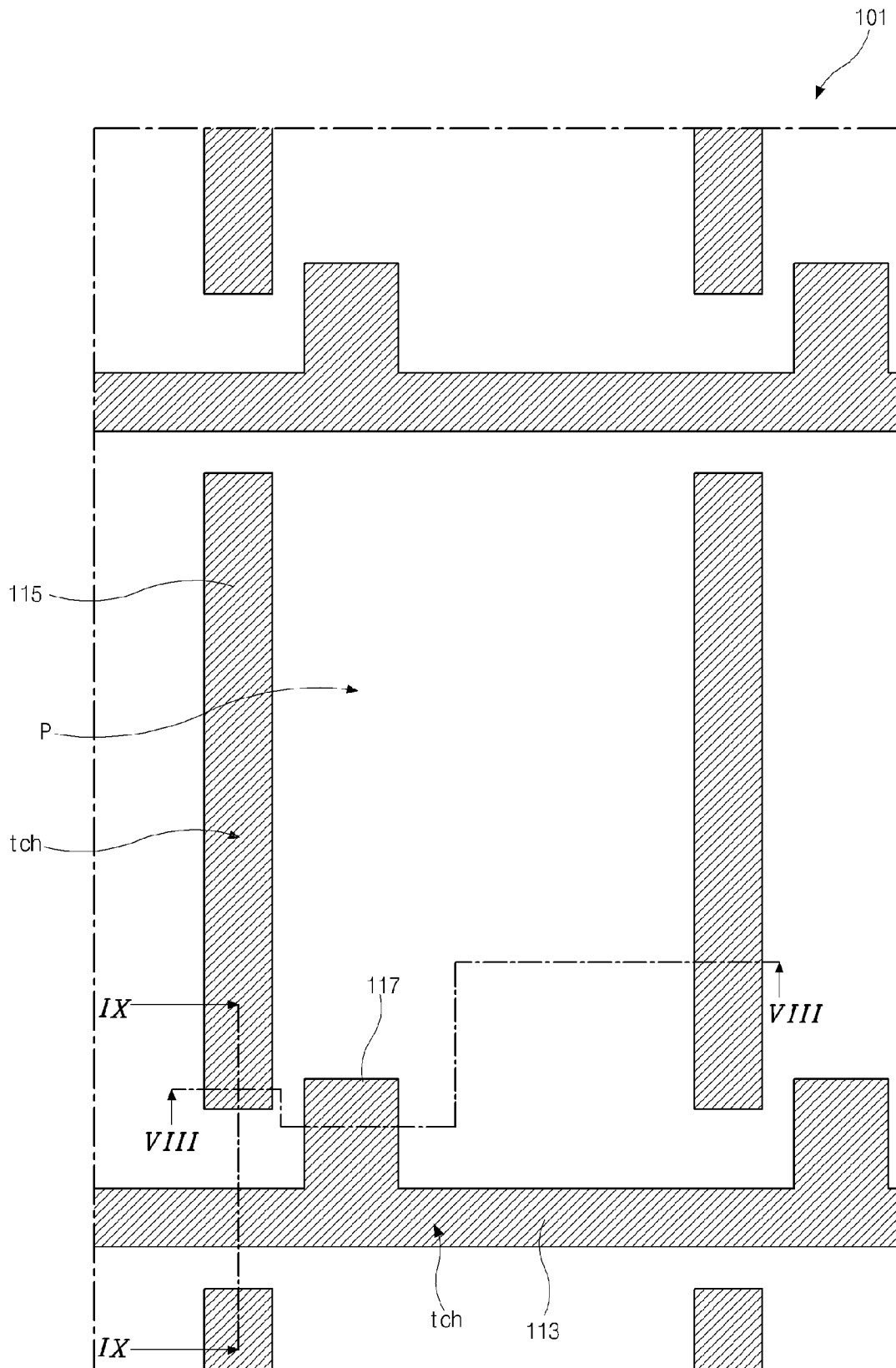


FIG. 7C

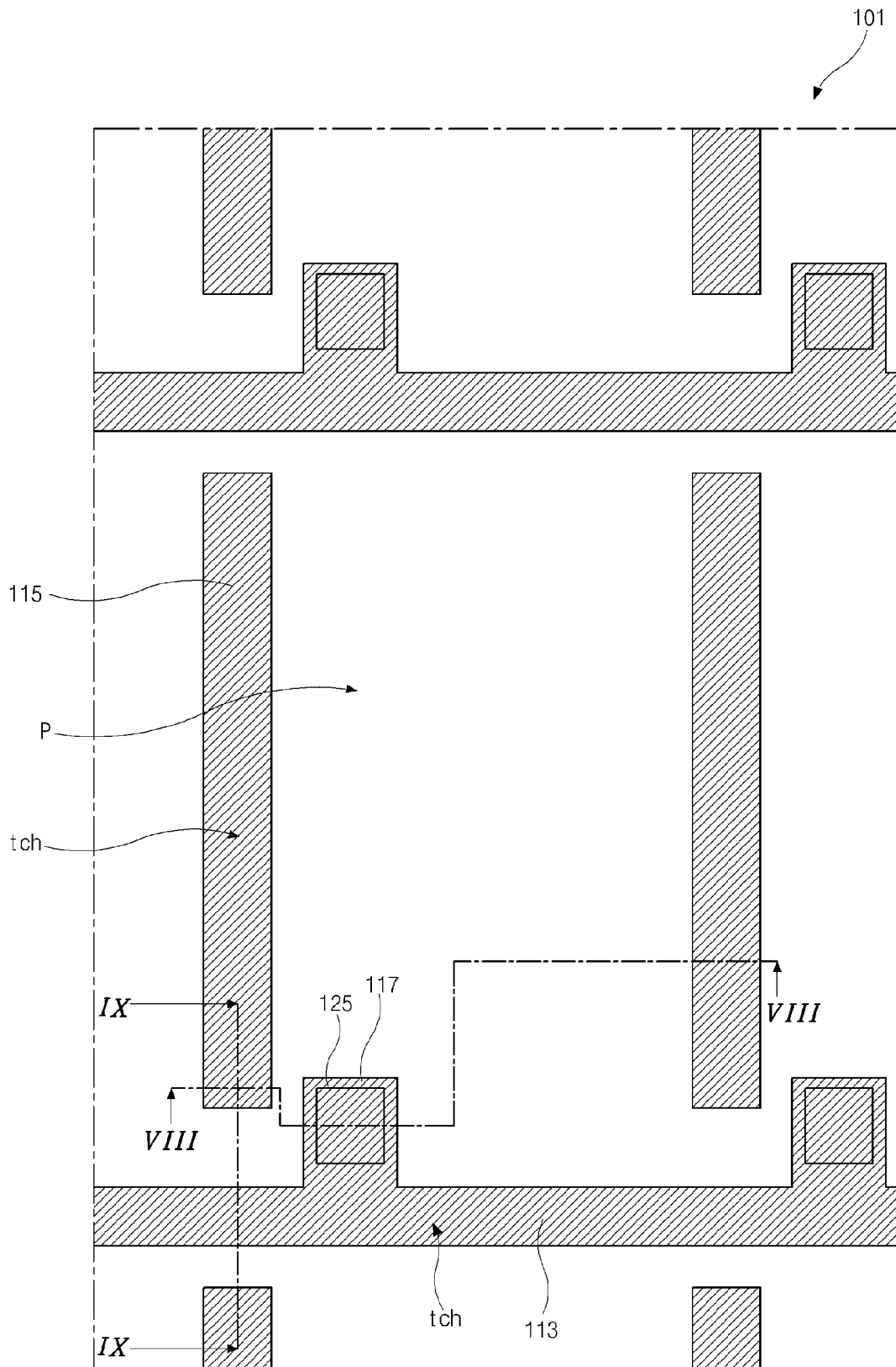


FIG. 7D

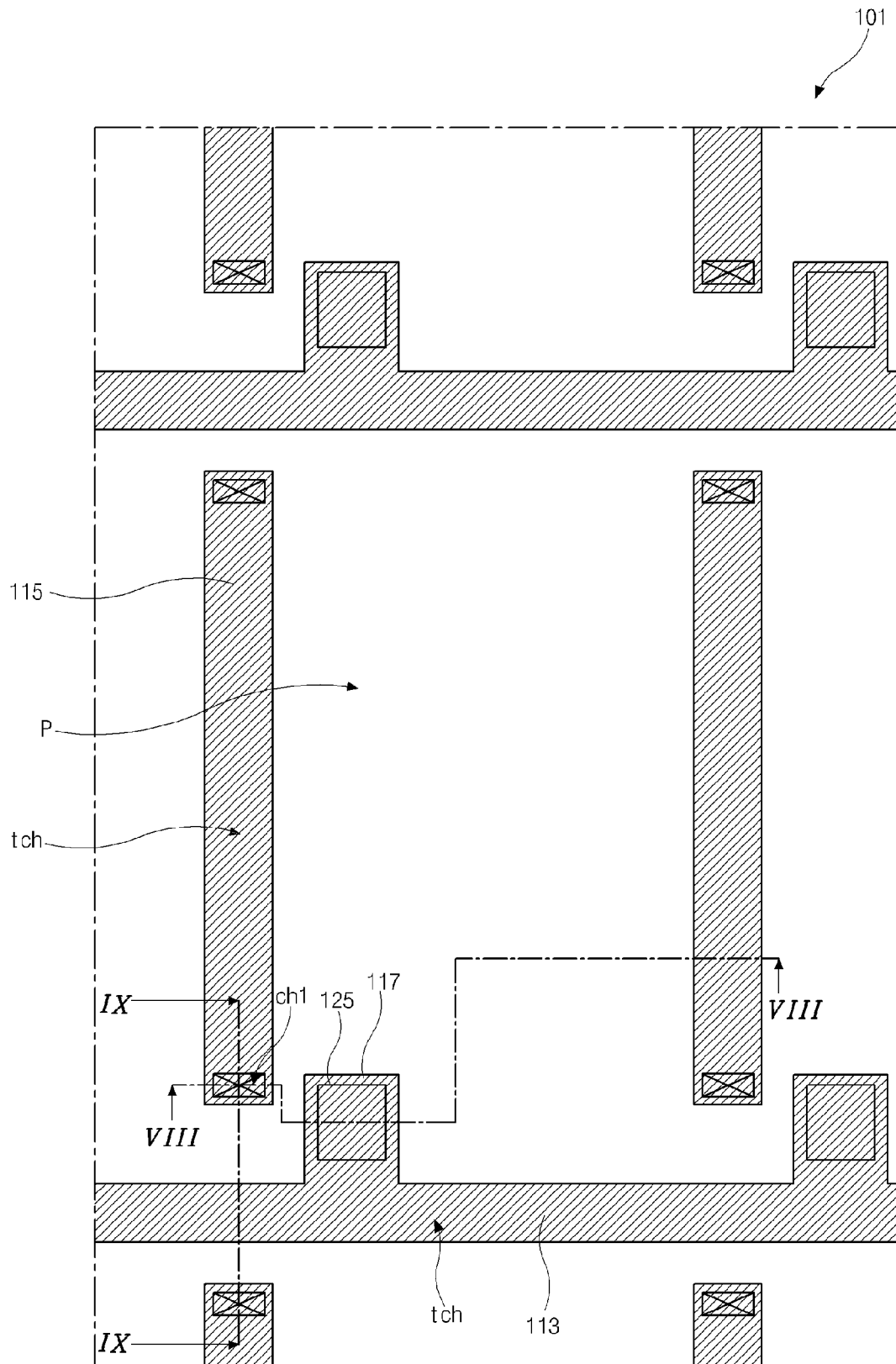


FIG. 7E

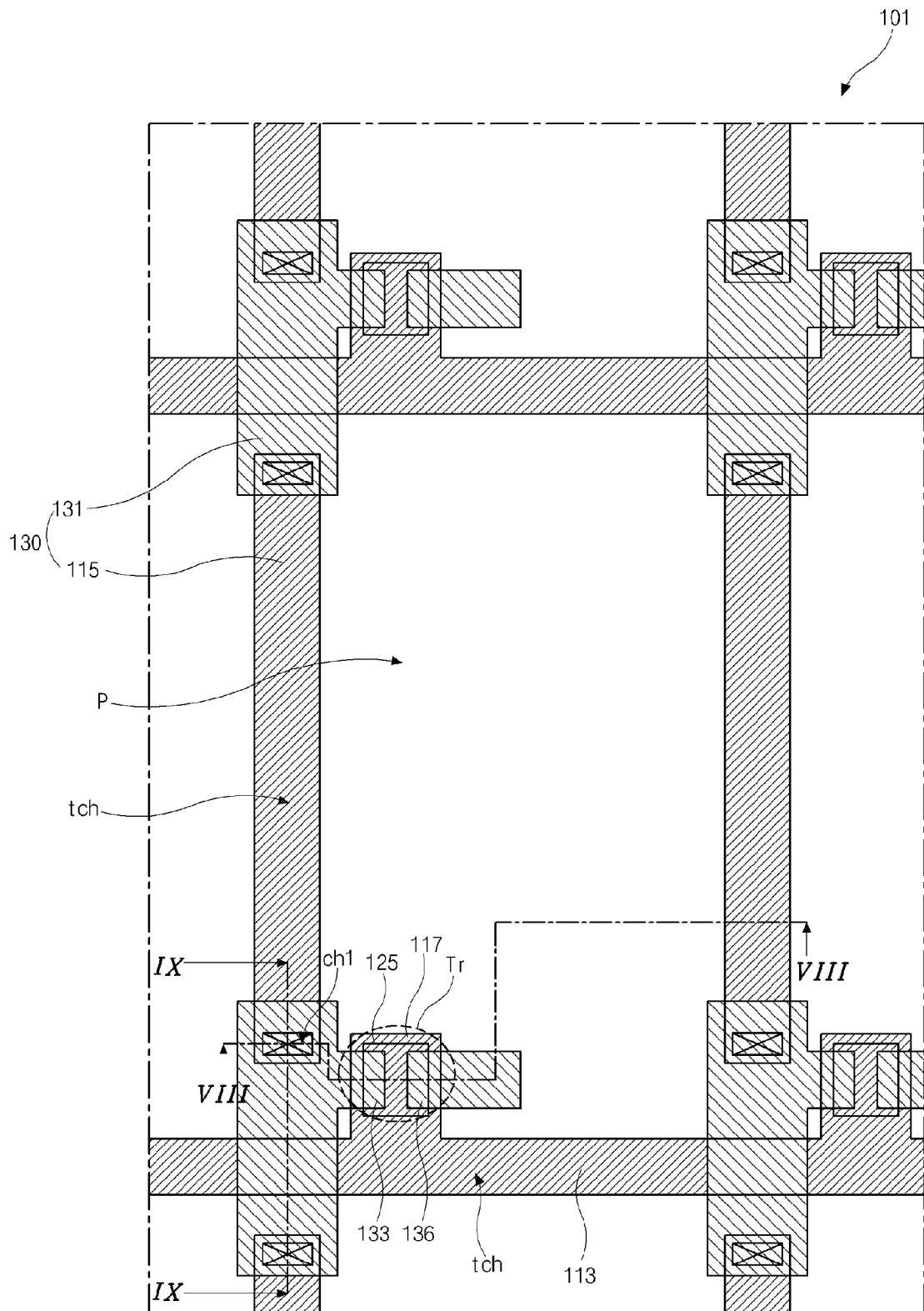


FIG. 7F

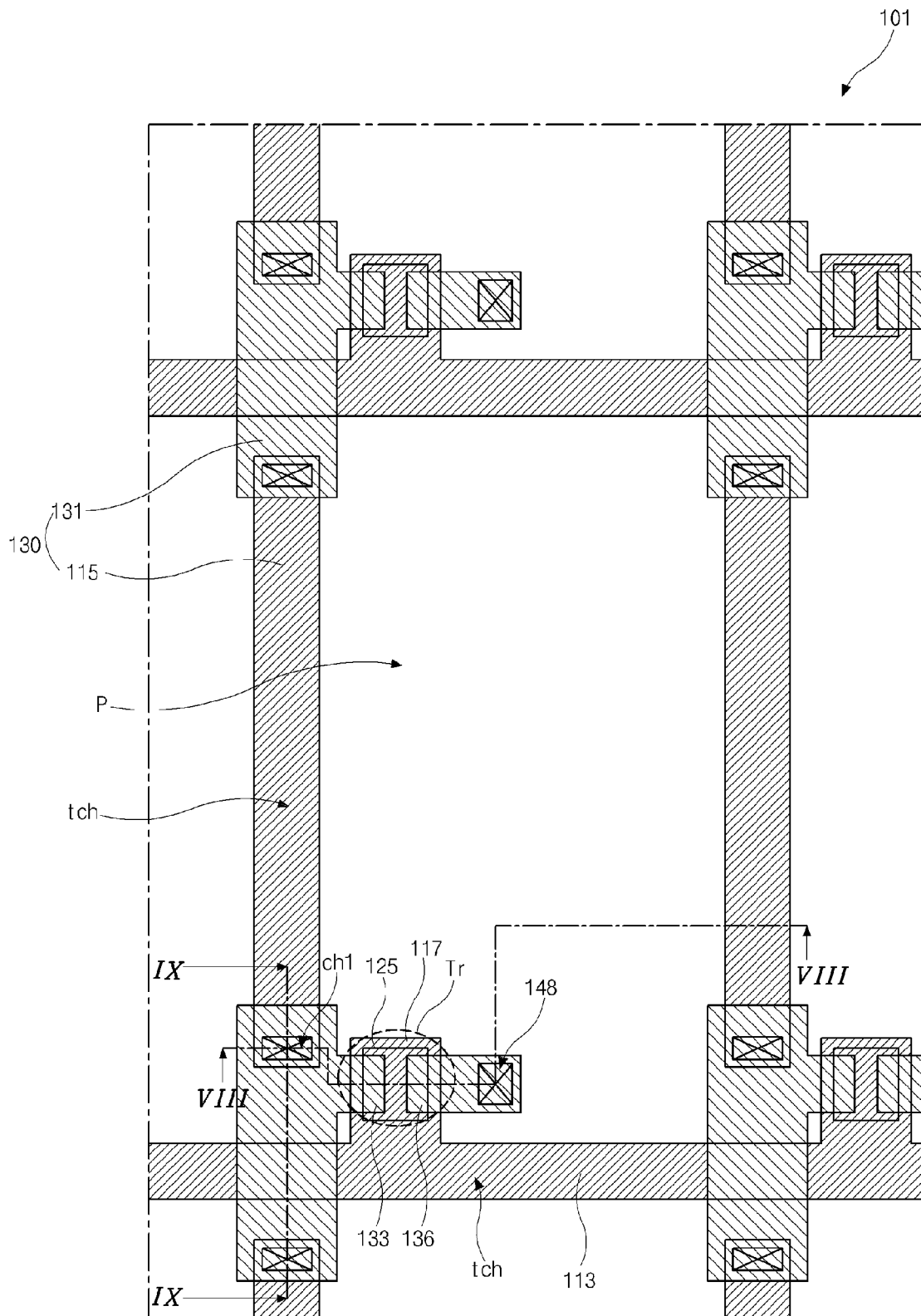


FIG. 7G

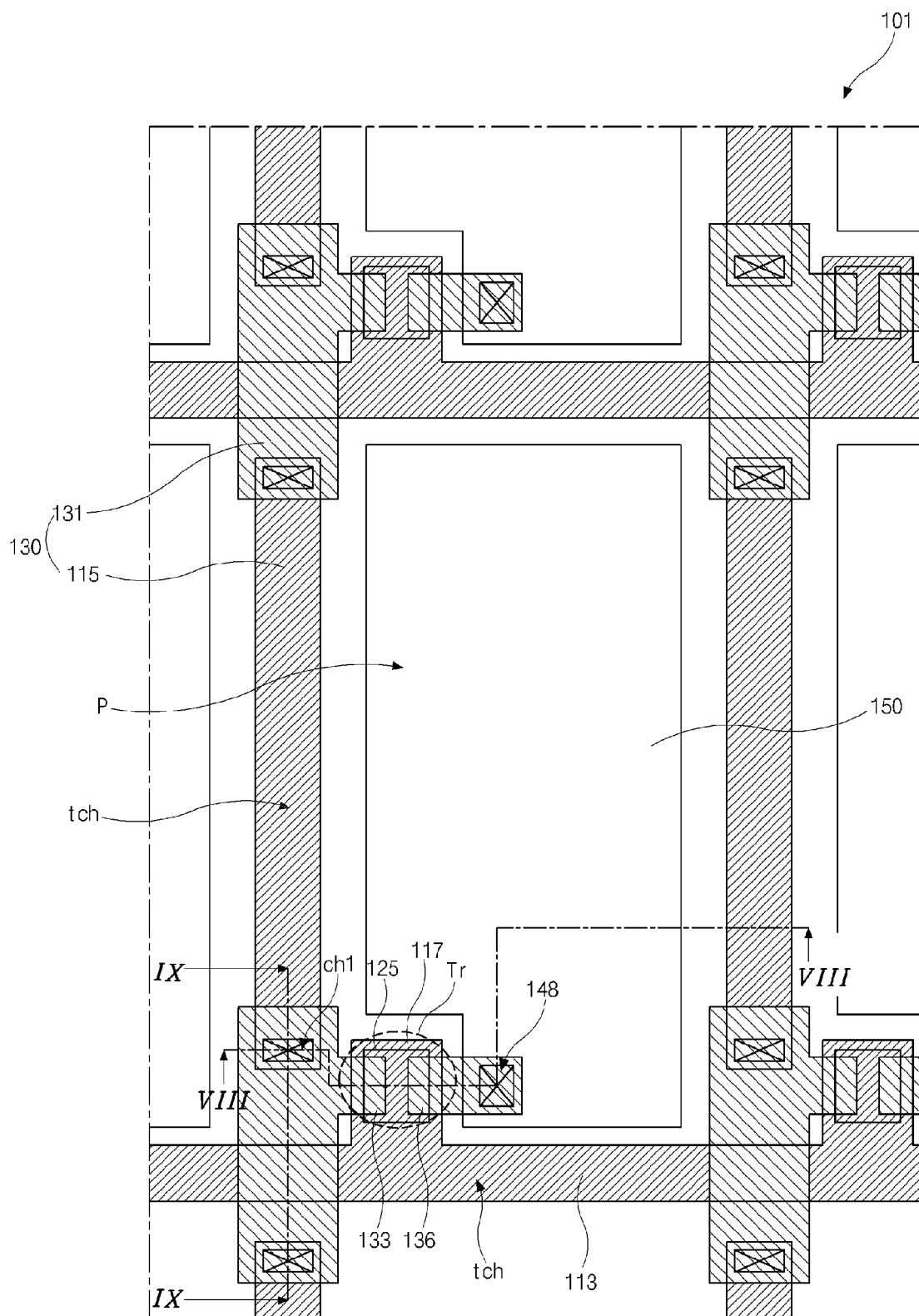


FIG. 8A

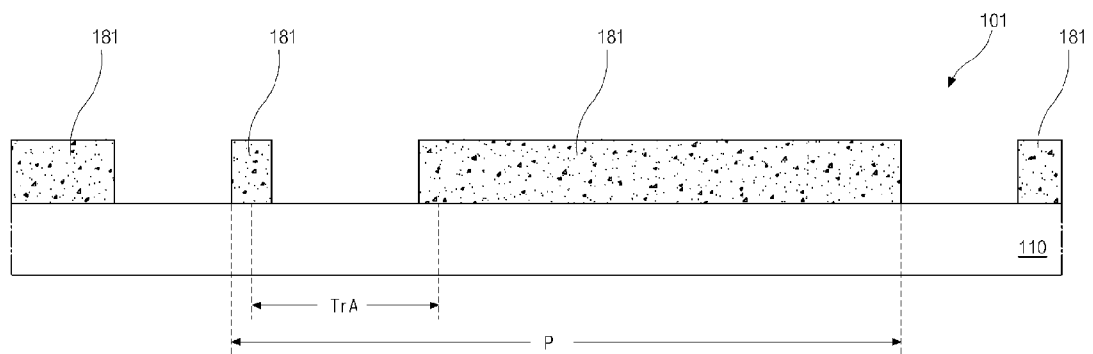


FIG. 8B

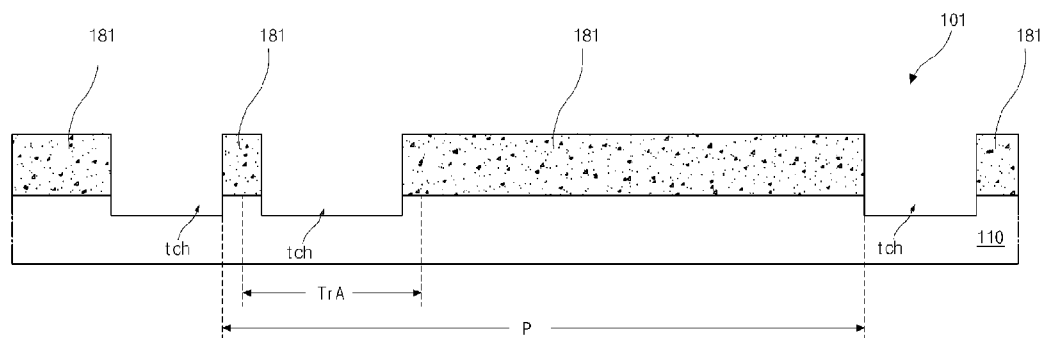


FIG. 8C

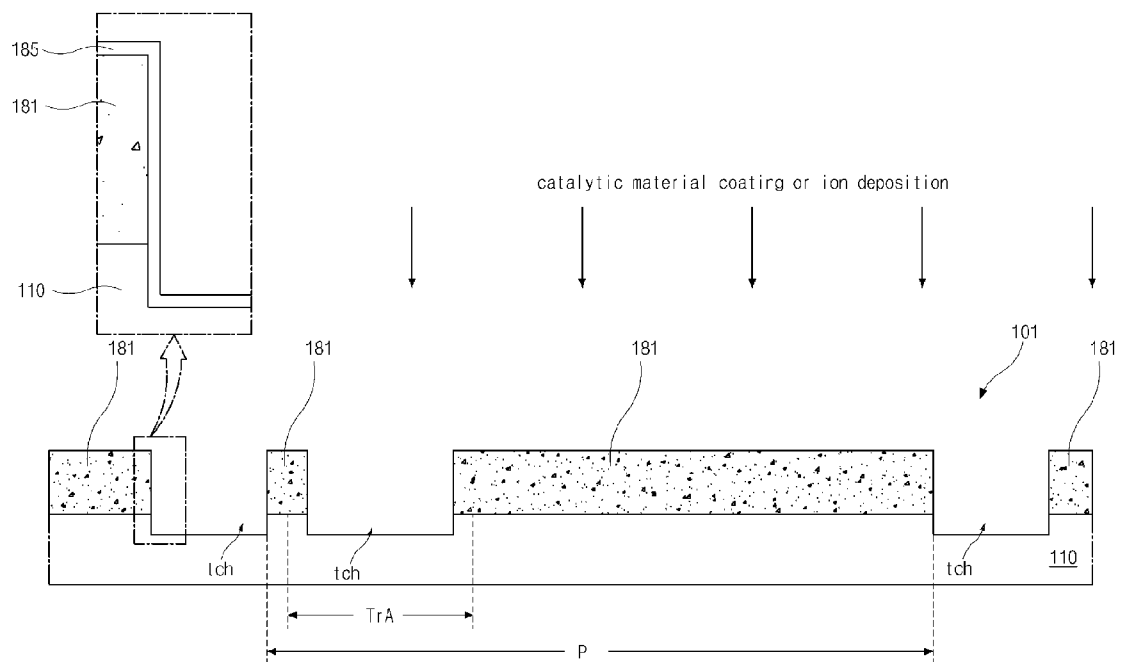


FIG. 8D

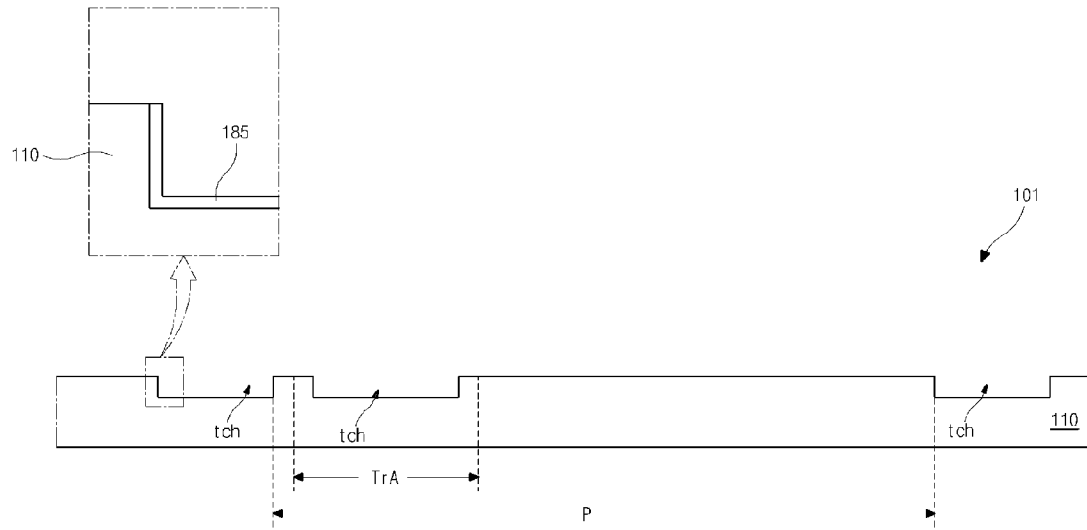


FIG. 8E

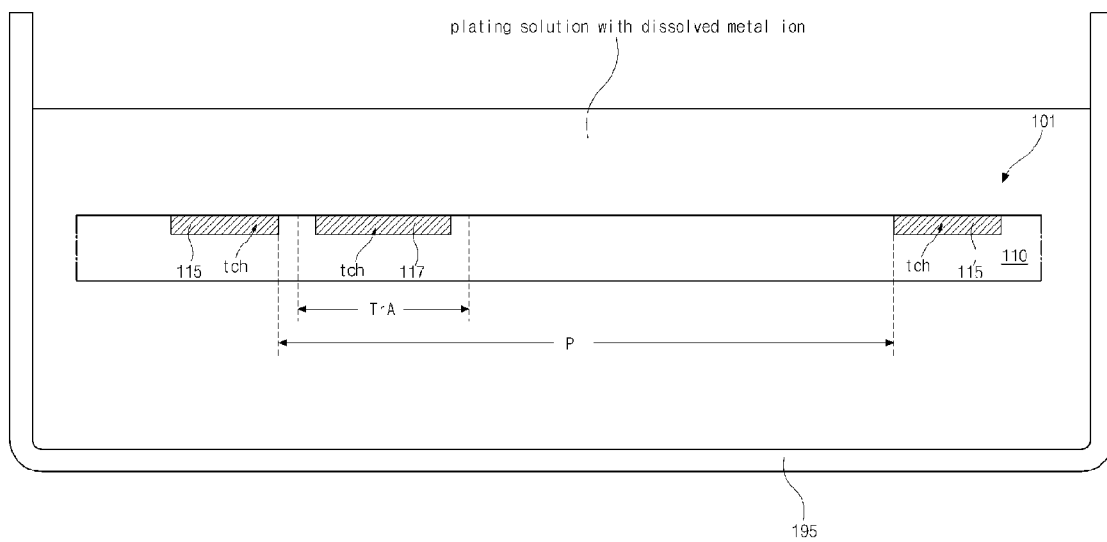


FIG. 8F

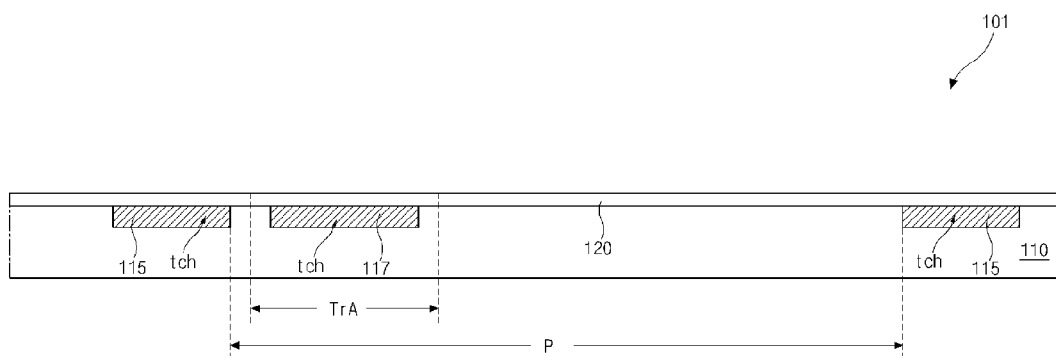


FIG. 8G

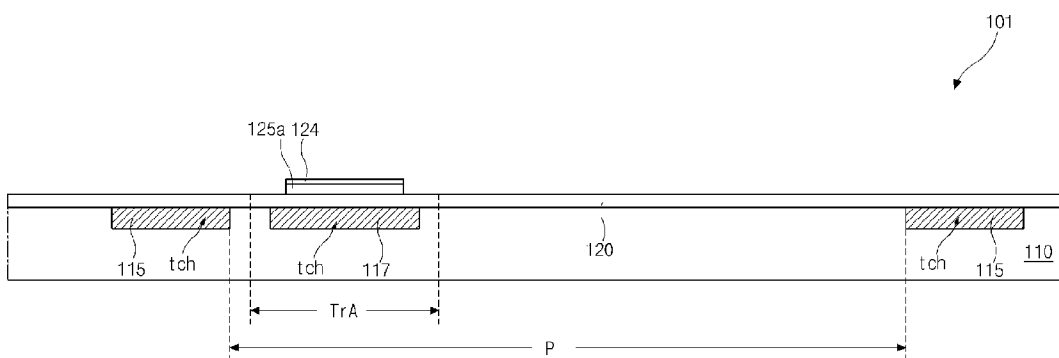


FIG. 8H

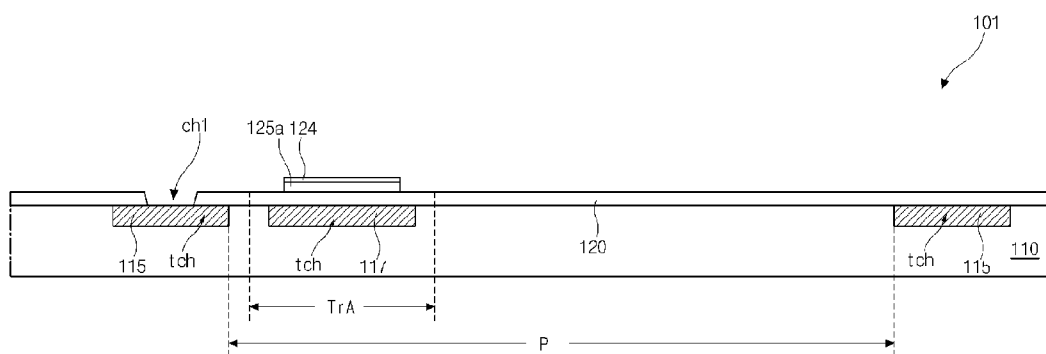


FIG. 8I

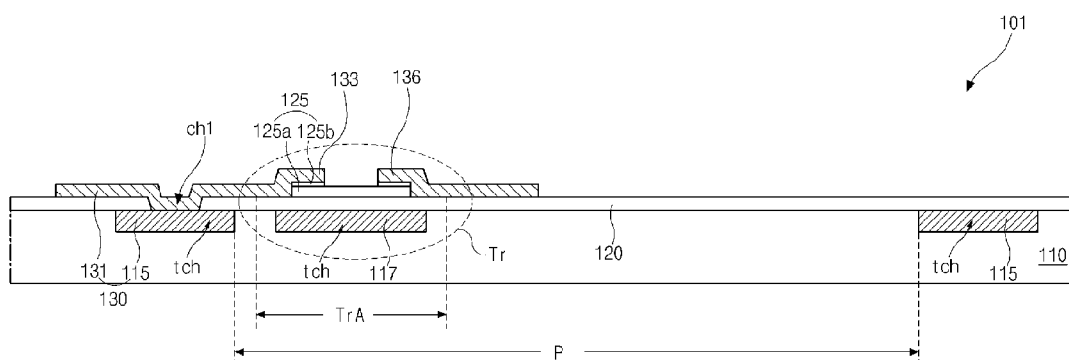


FIG. 8J

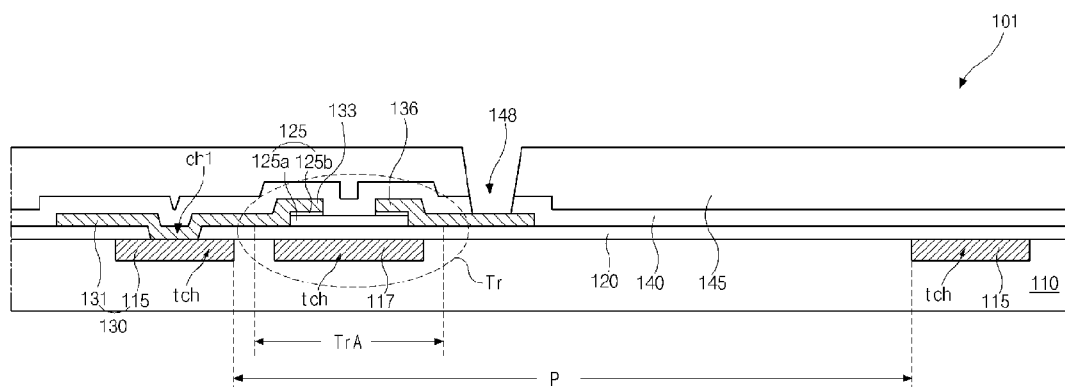


FIG. 8K

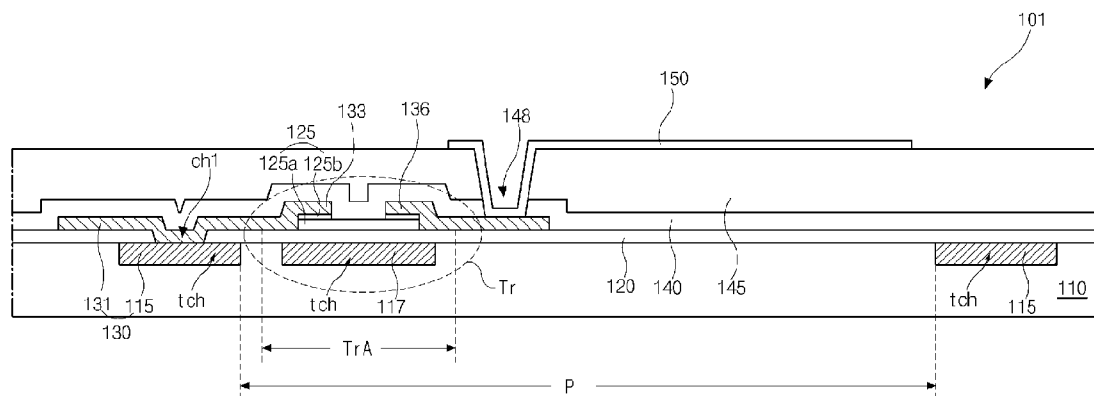


FIG. 9A

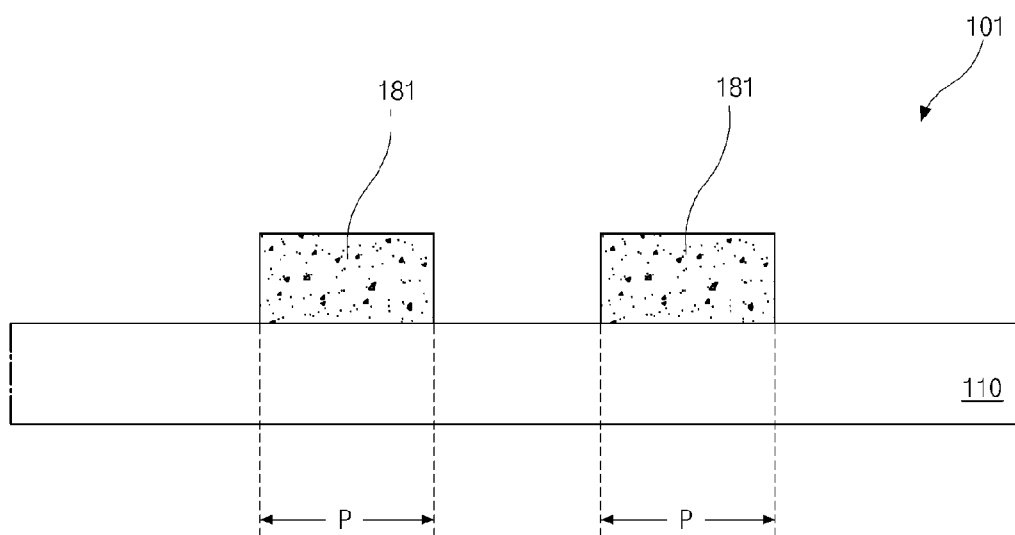


FIG. 9B

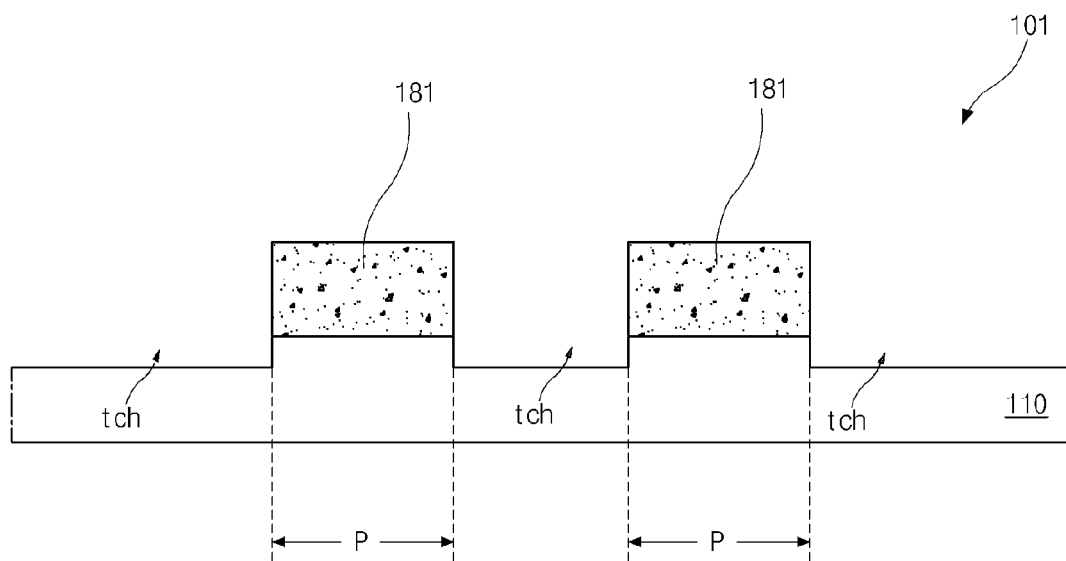


FIG. 9C

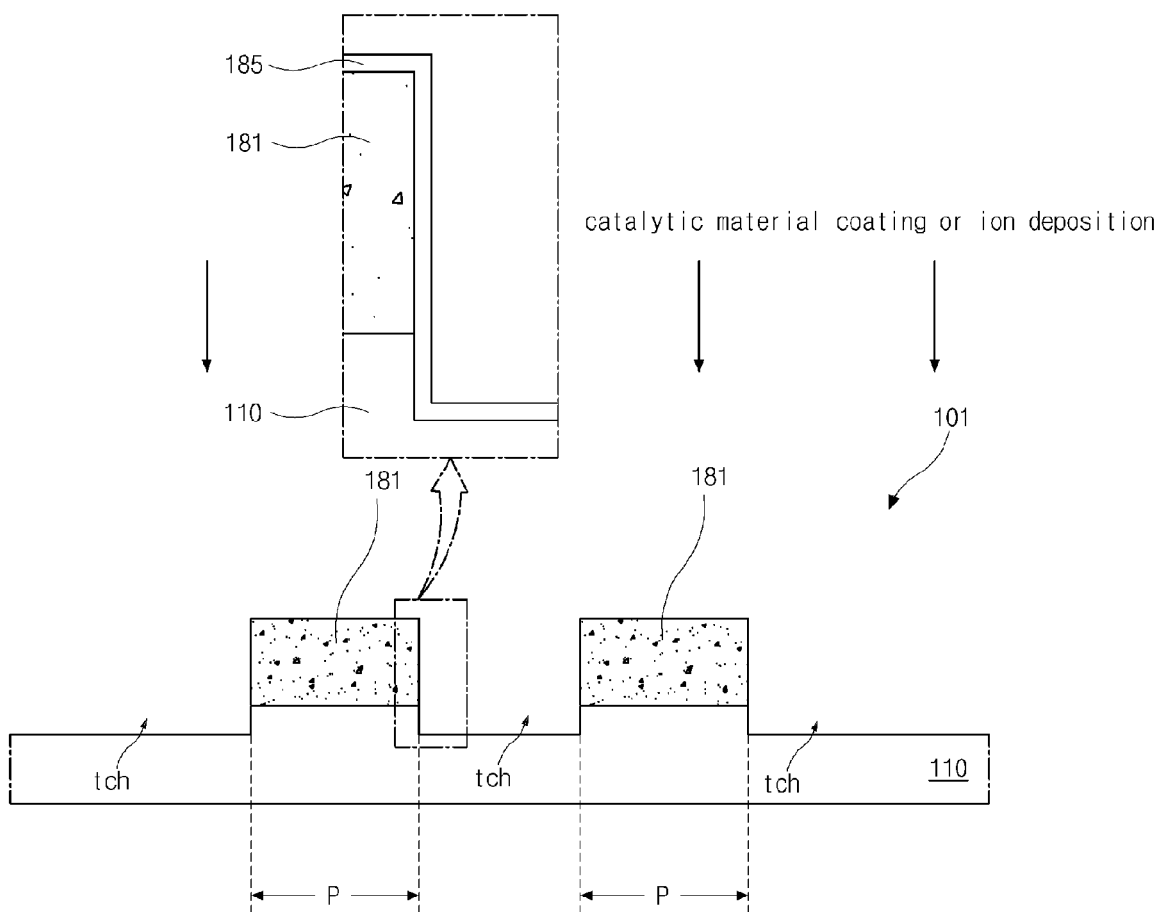


FIG. 9D

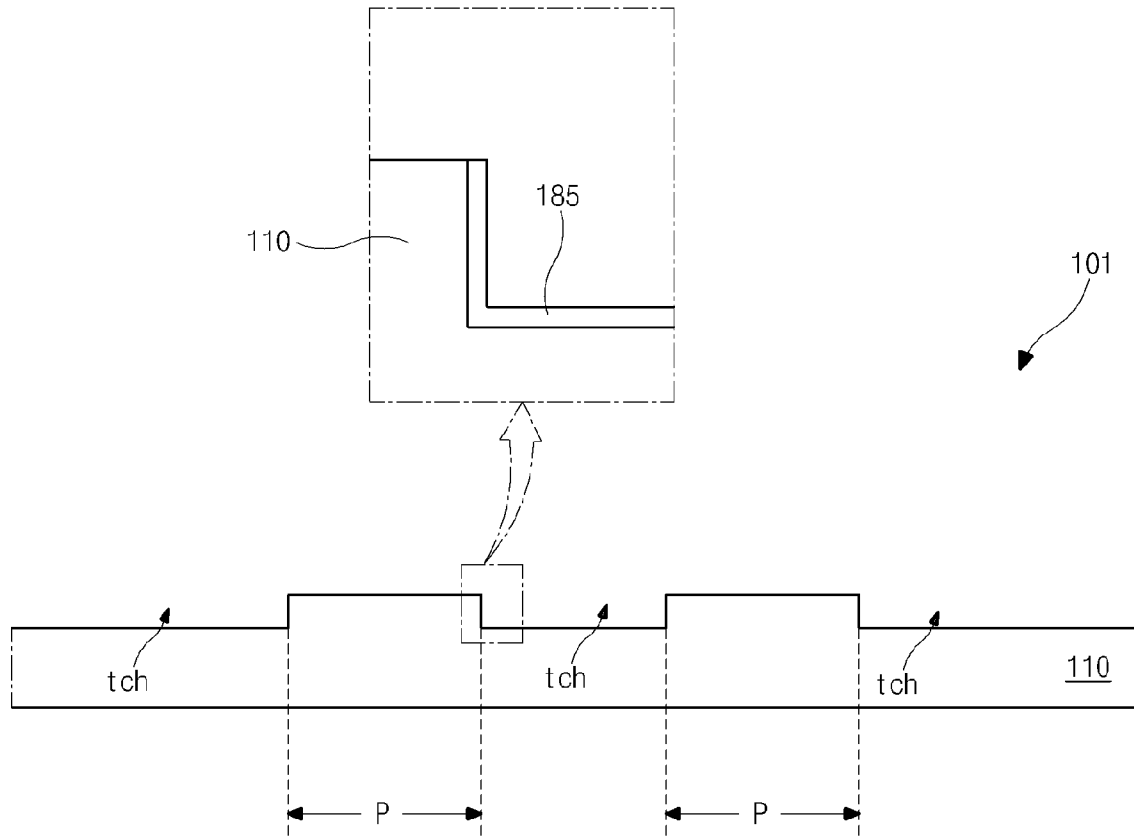


FIG. 9E

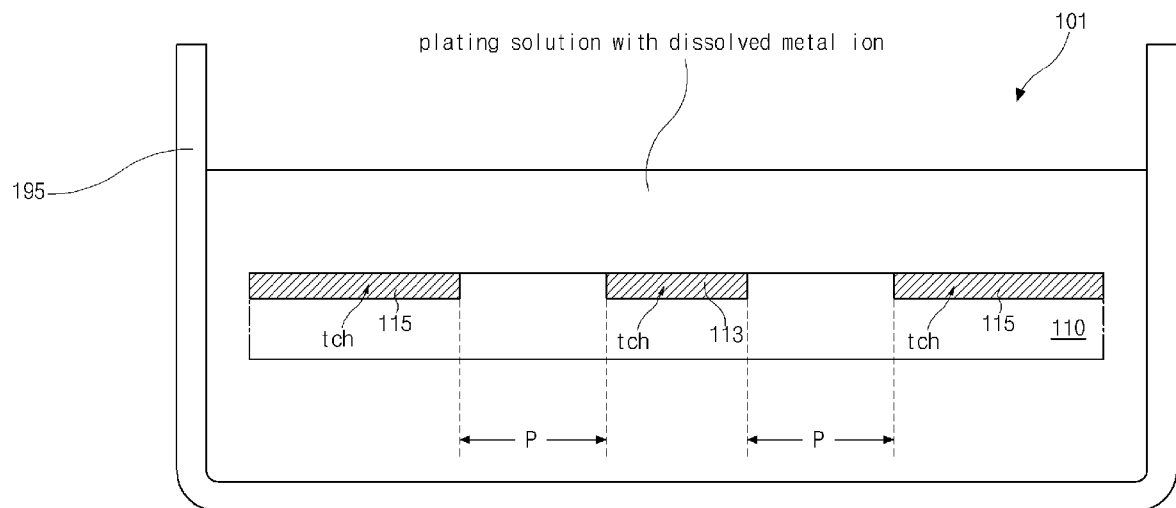


FIG. 9F

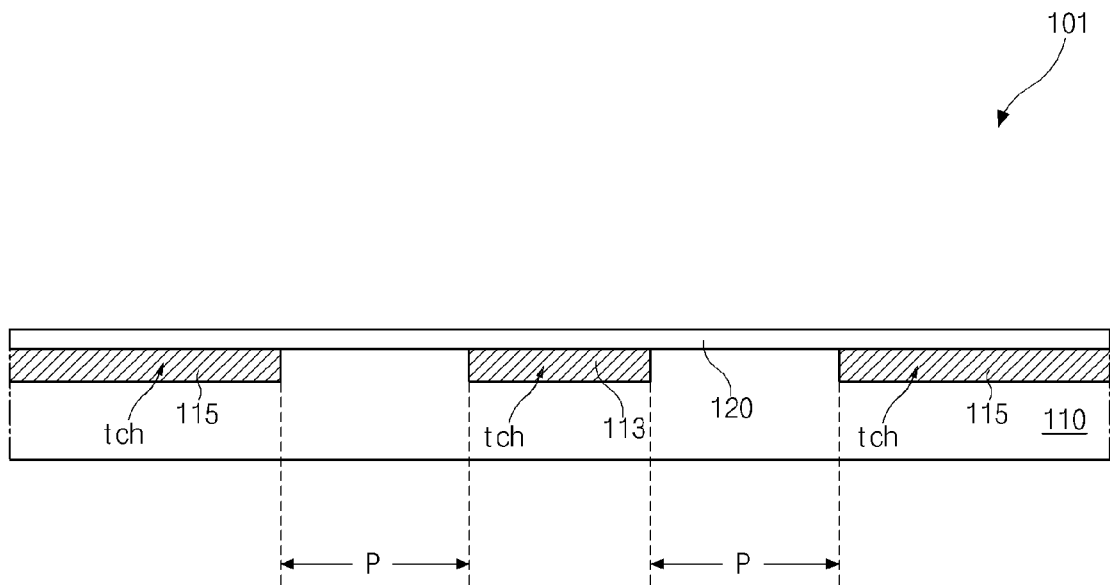


FIG. 9G

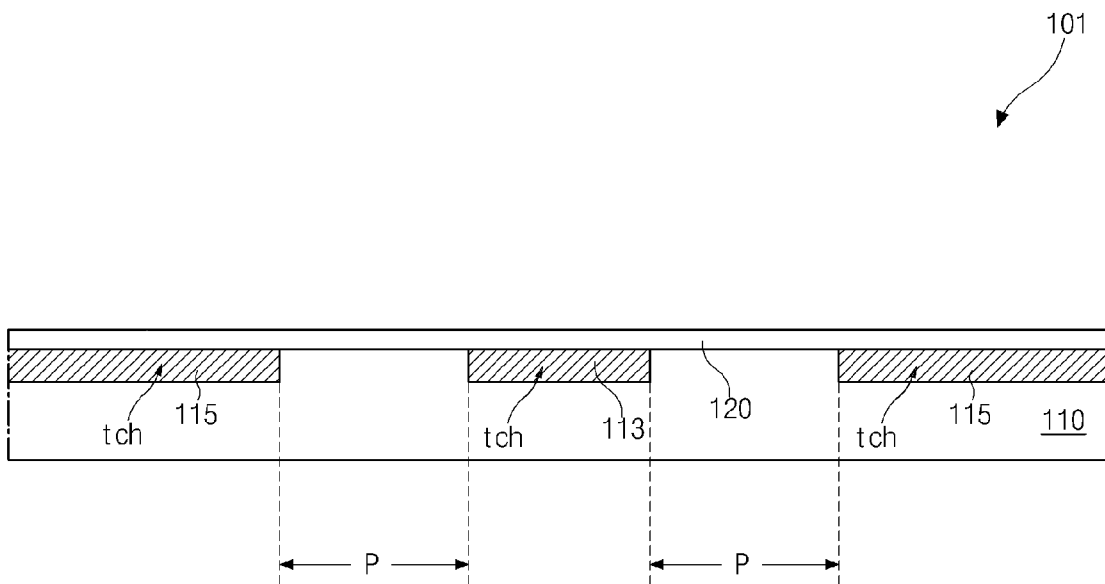


FIG. 9H

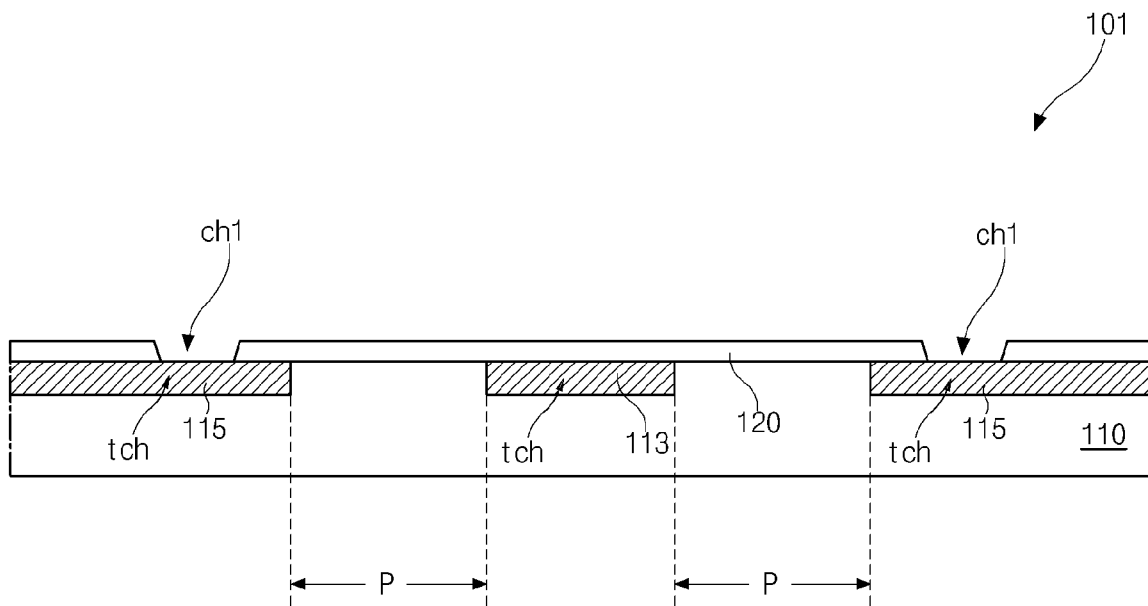


FIG. 9I

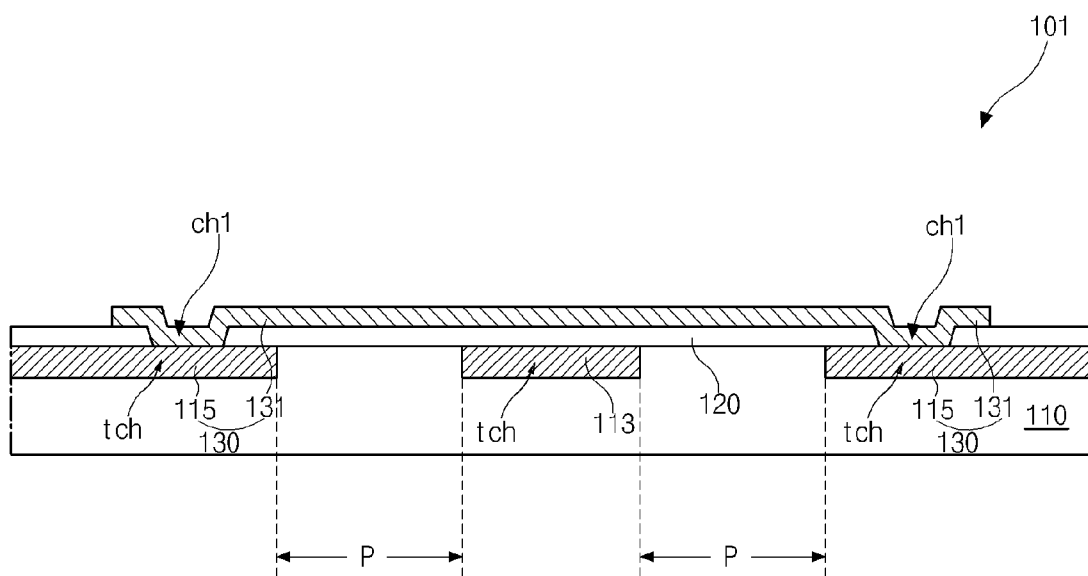


FIG. 9J

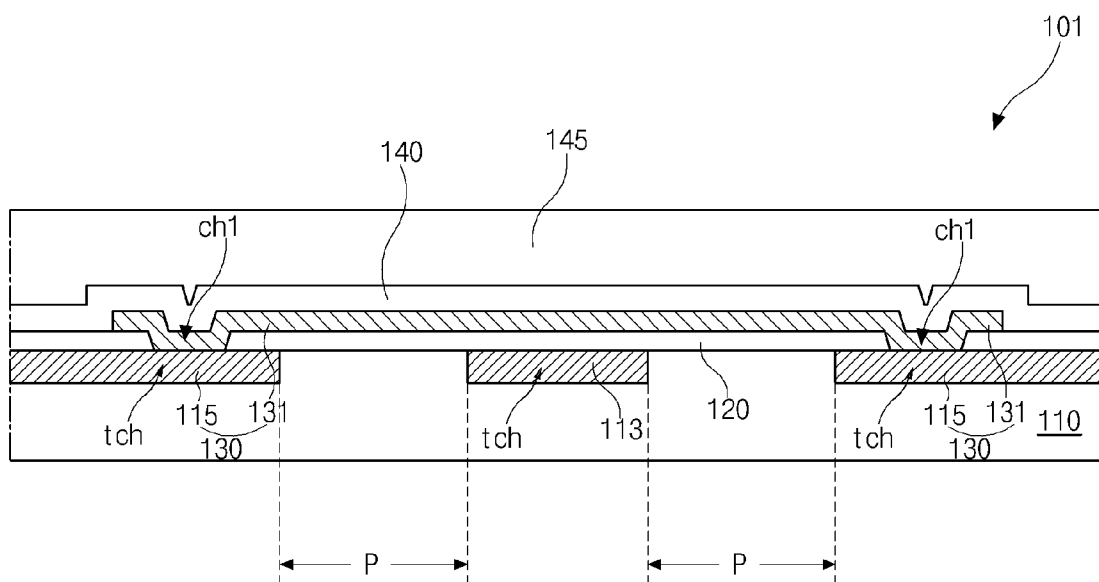


FIG. 9K

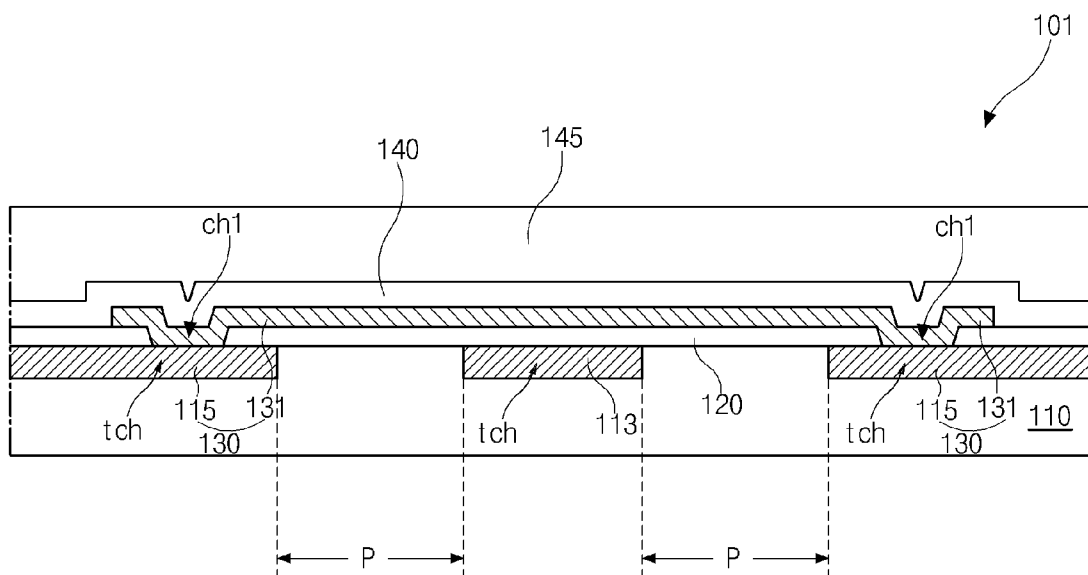


FIG. 10A

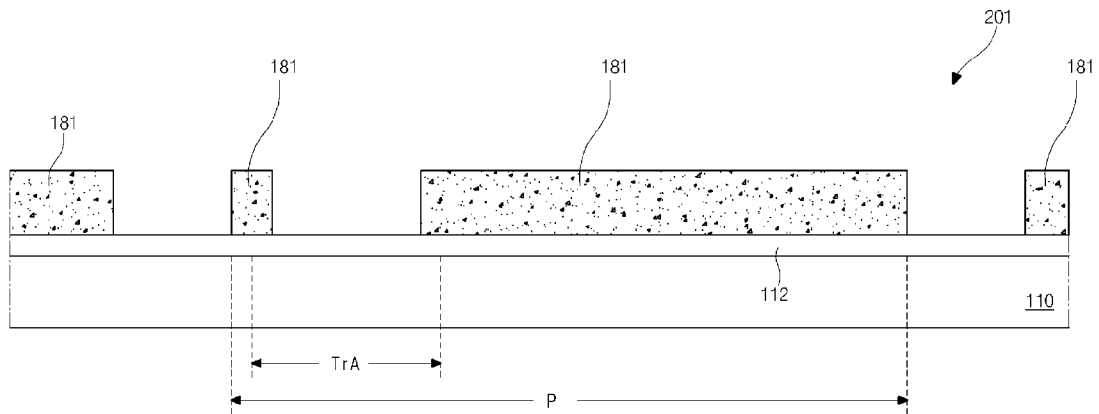


FIG. 10B

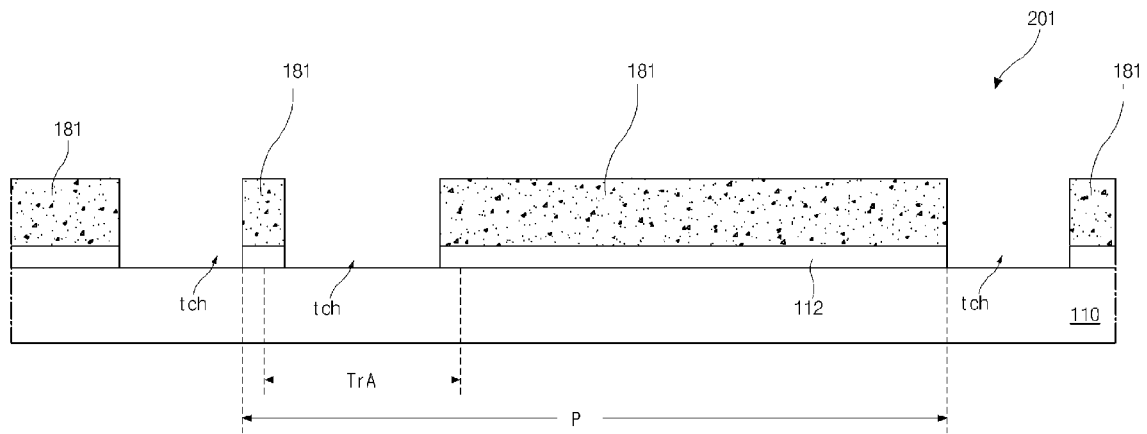


FIG. 10C

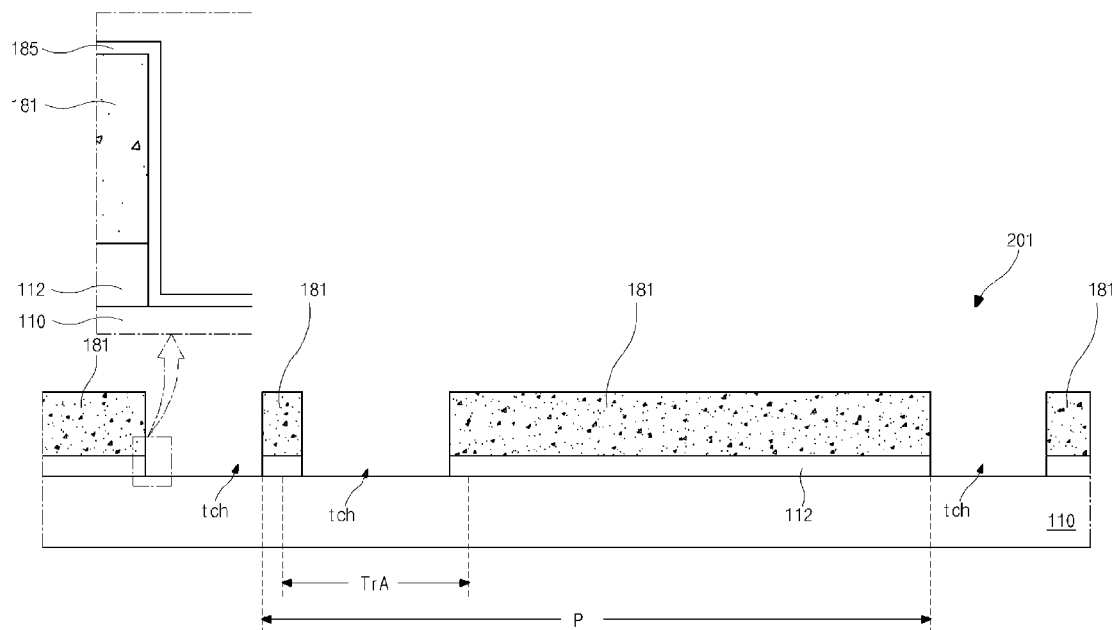


FIG. 10D

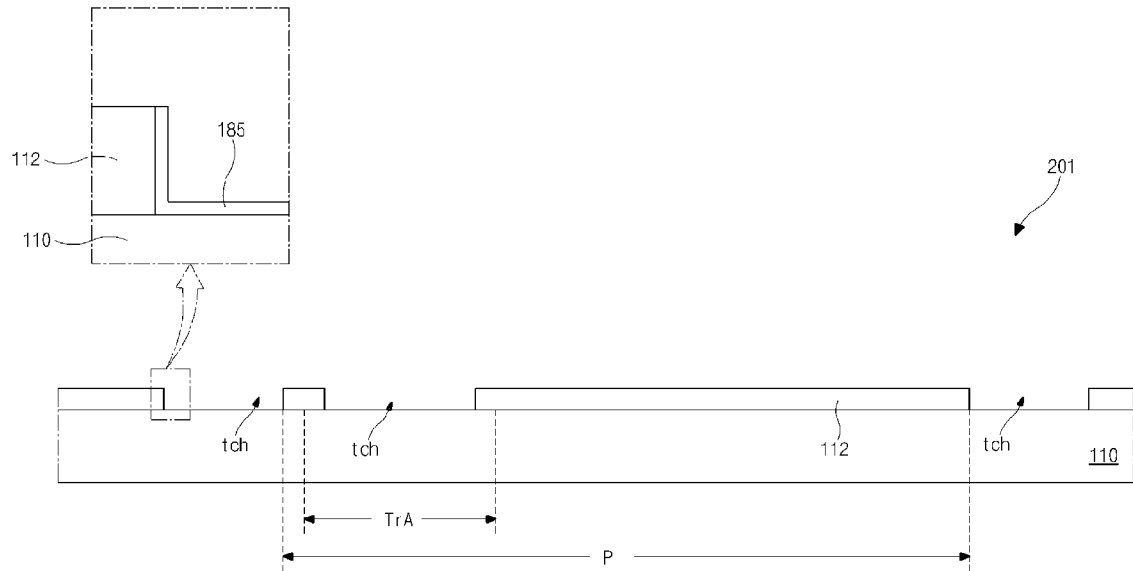
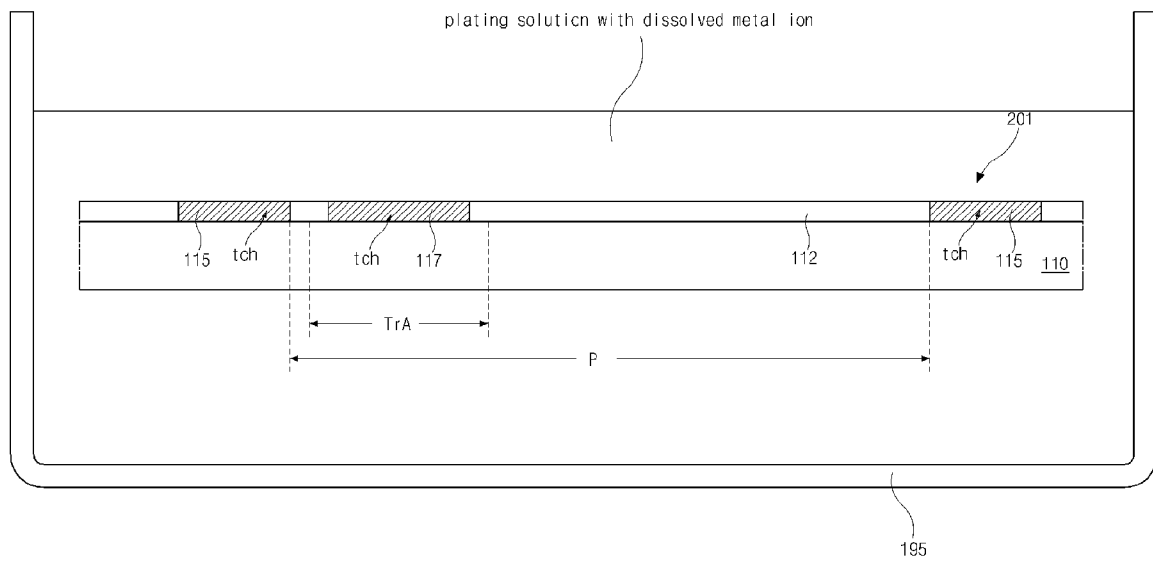


FIG. 10E





EUROPEAN SEARCH REPORT

Application Number
EP 13 19 5263

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	US 2012/007091 A1 (LEE JUNGIL [KR] ET AL) 12 January 2012 (2012-01-12)	1,2,6-8,15	INV. G02F1/1362
Y	* and the corresponding text passages; figures 3, 4A-E *	3-5,9-14	
Y	JP H03 85530 A (SHARP KK) 10 April 1991 (1991-04-10) * abstract; figure 2A *	3,4,10,12	
Y	US 2009/236627 A1 (KIM JANG-SUB [KR] ET AL) 24 September 2009 (2009-09-24) * and the corresponding text passages; figure 7 *	5,14	
Y	US 2008/314628 A1 (SONG KI YONG [KR] ET AL) 25 December 2008 (2008-12-25) * and the corresponding text passages; figure 2 *	9,11,13	
			TECHNICAL FIELDS SEARCHED (IPC)
			G02F
The present search report has been drawn up for all claims			
Place of search Munich		Date of completion of the search 11 November 2014	Examiner Lüssem, Georg
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

EPO FORM 1503 03.82 (P04C01)

**ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.**

EP 13 19 5263

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report.
The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

11-11-2014

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2012007091 A1	12-01-2012	CN 102315166 A	11-01-2012
		DE 102011077647 A1	15-03-2012
		KR 20120004642 A	13-01-2012
		US 2012007091 A1	12-01-2012

JP H0385530 A	10-04-1991	JP H0385530 A	10-04-1991
		JP H0820643 B2	04-03-1996

US 2009236627 A1	24-09-2009	NONE	

US 2008314628 A1	25-12-2008	EP 2012350 A2	07-01-2009
		JP 2009004774 A	08-01-2009
		KR 100847985 B1	22-07-2008
		US 2008314628 A1	25-12-2008

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

REFERENCES CITED IN THE DESCRIPTION

This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

Patent documents cited in the description

- KR 1020130075901 [0001]

专利名称(译)	用于液晶显示器的阵列基板及其制造方法		
公开(公告)号	EP2818917A1	公开(公告)日	2014-12-31
申请号	EP2013195263	申请日	2013-12-02
[标]申请(专利权)人(译)	乐金显示有限公司		
申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
当前申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
[标]发明人	MOON TAE HYOUNG SONG TAE JOON LEE KYU HWANG LEE KYUNG HA		
发明人	MOON, TAE-HYOUNG SONG, TAE-JOON LEE, KYU-HWANG LEE, KYUNG-HA		
IPC分类号	G02F1/1362		
CPC分类号	G02F1/136286 G02F2001/136295 H01L27/1244 H01L27/1259		
审查员(译)	IÜssem , 乔治		
优先权	1020130075901 2013-06-28 KR		
其他公开文献	EP2818917B1		
外部链接	Espacenet		

摘要(译)

阵列基板包括：沟槽，其具有距基板表面的深度；栅极线，栅极电极和填充各个沟槽的数据图案，其中数据图案位于相邻栅极线之间；栅极线上的栅极绝缘层，栅极和数据图案，基本上平坦在基板上，并包括分别暴露数据图案两端的接触孔；栅极绝缘层上的数据连接部分，通过接触孔接触相邻的数据图形；源极，从数据连接部分延伸，漏极与源极隔开；源极和漏极上的钝化层，包括暴露漏极的漏极接触孔；钝化层上的像素电极，通过漏极接触孔与漏电极接触。

