(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 2 765 452 B1

(12) EUROPEAN PATENT SPECIFICATION

(45) Date of publication and mention of the grant of the patent:
11.03.2015 Bulletin 2015/11

(51) Int Cl.:
G02F 1/1343 *(2006.01)*

(21) Application number: **14154271.2**

(22) Date of filing: **07.02.2014**

(54) Liquid crystal display

Flüssigkristallanzeige

Affichage à cristaux liquides

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR

(30) Priority: **12.02.2013 KR 20130014968**

(43) Date of publication of application:
13.08.2014 Bulletin 2014/33

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Printed by Jouve, 75001 PARIS (FR)

Description

BACKGROUND

FIELD

[0001] Exemplary embodiments relate to display technology, and more particularly to, a liquid crystal display including two field generating electrodes disposed on the same substrate.

DISCUSSION

[0002] Conventional liquid crystal displays typically include two display panels on which field generating electrodes, such as pixel electrodes and a common electrode, are formed, and a liquid crystal layer disposed therebetween. To facilitate the display of images, voltage is usually applied to the field generating electrodes to form an electric field in the liquid crystal layer. In this manner, the alignment of liquid crystal molecules of the liquid crystal layer is affected by the electric field, and polarization of incident light is controlled in association therewith. The transmittance of the liquid crystal display may increase when, for instance, the alignment of the liquid crystal molecules is controlled better.

[0003] Typically, each pixel electrode of a conventional liquid crystal display is connected with a switching element that is, in turn, connected with signal lines, such as a gate line and a data line. The switching element usually includes a three (3)-terminal element, such as a thin film transistor, which transfers data voltage to the pixel electrode through an output terminal thereof. It is noted that the pixel electrodes and the common electrode may be disposed on one display panel, such as the display panel including the switching element(s).

[0004] Therefore, there is a need for an approach that provides efficient, cost effective techniques to improve the control of liquid crystal molecules, and, in turn, the transmittance and/or other characteristics of an associated display device.

[0005] The above information disclosed in this Background section is only for enhancement of understanding of the background of the invention, and, therefore, it may contain information that does not form the prior art that is already known in this country to a person of ordinary skill in the art.

[0006] The document EP 2 472 310 A discloses a fringe field switching liquid crystal display device wherein branch portions of the pixel electrodes extend in parallel with the first signal lines, which are formed on the gate insulating layer. In the claimed invention the gate insulating layer is formed on the first signal lines.

SUMMARY

[0007] Exemplary embodiments provide a liquid crystal display including two field generating electrodes disposed on the same substrate.

[0008] Additional aspects will be set forth in the detailed description which follows and, in part, will be apparent from the disclosure, or may be learned by practice of the invention.

[0009] According to exemplary embodiments, a liquid crystal display, includes: a substrate; first signal lines disposed on the substrate, the first signal lines longitudinally extending in substantially a first direction; a gate insulating layer disposed on the first signal lines; a first electrode disposed on the gate insulating layer; a thin film transistor connected to a first signal line of the first signal lines, the thin film transistor including the gate insulating layer and the first electrode; a pixel electrode longitudinally extending in substantially the first direction, the pixel electrode being connected to the thin film transistor and configured to receive a data voltage from the thin film transistor; a common electrode overlapping with at least a portion of the pixel electrode; and a first insulating layer disposed between the pixel electrode and the common electrode. One of the pixel electrode and the common electrode has a planar shape and the other includes a plurality of branch electrodes overlapping with at least a portion of the planar-shaped electrode, the branch electrodes extend substantially parallel to the first signal line, and a portion of the common electrode overlaps with at least a portion of the first signal line.

[0010] According to exemplary embodiments, transmittance of a liquid crystal display including two field generating electrodes disposed on the same substrate may be increased. In addition, the parasitic capacitance may be reduced between a signal line and a field generating electrode, which, thereby, minimizes signal delay and crosstalk between the signal line and the field generating electrode. Furthermore, light leakage caused, at least in part, by electric field distortions may also be reduced.

[0011] According to exemplary embodiments, a number of data driving circuit chips may be reduced, which, thereby, reduces an edge portion (e.g., bezel region) of a corresponding display panel. Moreover, when integrating a gate driving circuit on a substrate, exemplary embodiments permit greater design freedom in the choice of integration regions for the gate driving circuit.

[0012] The foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate exemplary embodiments of the invention, and together with the description serve to explain the principles of the invention.

FIG. 1 is a layout view of a liquid crystal display, according to exemplary embodiments.

FIG. 2 is a cross-sectional view of the liquid crystal display of FIG. 1 taken along sectional line II-II, according to exemplary embodiments.

FIG. 3 is a layout view of a liquid crystal display, according to exemplary embodiments.

FIG. 4 is a cross-sectional view of the liquid crystal display of FIG. 3 taken along sectional line IV-IV, according to exemplary embodiments.

FIG. 5 is a layout view of a liquid crystal display, according to exemplary embodiments.

FIG. 6 is a cross-sectional view of the liquid crystal display of FIG. 5 taken along sectional line VI-VI, according to exemplary embodiments.

FIG. 7 is a layout view of a liquid crystal display, according to exemplary embodiments.

FIG. 8 is a cross-sectional view of the liquid crystal display of FIG. 7 taken along sectional line VIII-VIII, according to exemplary embodiments.

FIG. 9 is a layout view of a liquid crystal display, according to exemplary embodiments.

FIG. 10 is a cross-sectional view of the liquid crystal display of FIG. 9 taken along sectional line X-X, according to exemplary embodiments.

FIG. 11 is a cross-sectional view of the liquid crystal display of FIG. 9 taken along sectional line XI-XI, according to exemplary embodiments.

FIG. 12 is a cross-sectional view of the liquid crystal display of FIG. 9 taken along sectional line XII-XII, according to exemplary embodiments.

FIGS. 13 and 14 are layout views of a polarity of a data voltage in a liquid crystal display, according to exemplary embodiments.

FIGS. 15-18 are layout views of a manufacturing method of the liquid crystal display of FIG. 9, according to exemplary embodiments.

FIG. 19 is a layout view of a liquid crystal display, according to exemplary embodiments.

FIG. 20 is a cross-sectional view of the liquid crystal display of FIG. 19 taken along sectional line XX-XX, according to exemplary embodiments.

FIG. 21 is a layout view of a liquid crystal display, according to exemplary embodiments.

FIG. 22 is a cross-sectional view of the liquid crystal display of FIG. 21 taken along sectional line XXII-XXII, according to exemplary embodiments.

FIG. 23 is a layout view of a liquid crystal display, according to exemplary embodiments.

FIG. 24 is a cross-sectional view of the liquid crystal display of FIG. 23 taken along sectional line XXIV-XXIV, according to exemplary embodiments.

FIG. 25 is a block diagram of a liquid crystal display, according to exemplary embodiments.

FIG. 26 is a layout view of a liquid crystal display, according to exemplary embodiments.

FIG. 27 is a cross-sectional view of the liquid crystal display of FIG. 26 taken along sectional line XXVII-XXVII, according to exemplary embodiments.

FIG. 28 is a cross-sectional view of the liquid crystal display of FIG. 26 taken along sectional line XXVIII-XXVIII, according to exemplary embodiments.

FIG. 29 is a layout view of a liquid crystal display, according to exemplary embodiments.

FIG. 30 is a cross-sectional view of the liquid crystal display of FIG. 29 taken along sectional line XXX-XXX, according to exemplary embodiments.

FIG. 31 is a cross-sectional view of the liquid crystal display of FIG. 29 taken along sectional line XXXI-XXXI, according to exemplary embodiments.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

[0014] In the following description, for the purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of various exemplary embodiments. It is apparent, however, that various exemplary embodiments may be practiced without these specific details or with one or more equivalent arrangements. In other instances, well-known structures and devices are shown in block diagram form in order to avoid unnecessarily obscuring various exemplary embodiments.

[0015] In the accompanying figures, the size and relative sizes of layers, films, panels, regions, etc., may be exaggerated for clarity and descriptive purposes. Also, like reference numerals denote like elements.

[0016] When an element or layer is referred to as being "on," "connected to," or "coupled to" another element or layer, it may be directly on, connected to, or coupled to the other element or layer or intervening elements or layers may be present. When, however, an element or layer is referred to as being "directly on," "directly connected to," or "directly coupled to" another element or layer, there are no intervening elements or layers present. For the purposes of this disclosure, "at least one of X, Y, and Z" and "at least one selected from the group consisting of X, Y, and Z" may be construed as X only, Y only, Z only, or any combination of two or more of X, Y, and Z, such as, for instance, XYZ, XYY, YZ, and ZZ. Like numbers refer to like elements throughout. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

[0017] Although the terms first, second, etc. may be used herein to describe various elements, components, regions, layers and/or sections, these elements, components, regions, layers and/or sections should not be limited by these terms. These terms are used to distinguish one element, component, region, layer or section from another region, layer or section. Thus, a first element, component, region, layer or section discussed below could be termed a second element, component, region, layer or section without departing from the teachings of the present disclosure.

[0018] Spatially relative terms, such as "beneath," "below," "lower," "above," "upper," and/or the like, may be used herein for descriptive purposes, and thereby, to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the drawings. Spatially relative terms are intended to encompass different orientations of an apparatus in use or operation in addition to the orientation depicted in the drawings. For example, if the apparatus in the drawings is turned over, elements described as "below" or "beneath" other elements or features would then be oriented "above" the other elements or features. Thus, the exemplary term "below" can encompass both an orientation of above and below. Furthermore, the apparatus may be otherwise oriented (e.g., rotated 90 degrees or at other orientations), and as such, the spatially relative descriptors used herein interpreted accordingly.

[0019] The terminology used herein is for the purpose of describing particular embodiments and is not intended to be limiting. As used herein, the singular forms "a," "an," and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. Moreover, the terms "comprises" and/or "comprising," when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[0020] Various exemplary embodiments are described herein with reference to sectional illustrations that are schematic illustrations of idealized exemplary embodiments and/or intermediate structures. As such, variations from the shapes of the illustrations as a result, for example, of manufacturing techniques and/or tolerances, are to be expected. Thus, exemplary embodiments disclosed herein should not be construed as limited to the particular illustrated shapes of regions, but are to include deviations in shapes that result from, for instance, manufacturing. For example, an implanted region illustrated as a rectangle will, typically, have rounded or curved features and/or a gradient of implant concentration at its edges rather than a binary change from implanted to non-implanted region. Likewise, a buried region formed by implantation may result in some implantation in the region between the buried region and the surface through which the implantation takes place. Thus, the regions illustrated in the drawings are schematic in nature and their shapes are not intended to illustrate the actual shape of a region of a device and are not intended to be limiting.

[0021] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this disclosure is a part. Terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and will not be interpreted in an idealized or overly formal sense, unless expressly so defined herein.

[0022] FIG. 1 is a layout view of a liquid crystal display, according to exemplary embodiments. FIG. 2 is a cross-sectional view of the liquid crystal display of FIG. 1 taken along sectional line II-II.

[0023] Referring to FIG. 1, a liquid crystal display includes a plurality of pixels PX arranged in, for example, a matrix formation. It is contemplated, however, that any suitable arrangement may be utilized. As shown, a row direction is referred to as a first (or x-direction), and a column direction is referred to as a second (or y-direction). Referring to FIG. 2, the liquid crystal display further includes a lower panel 100 and an upper panel 200 facing each other, and a liquid crystal layer 3 disposed therebetween.

[0024] According to exemplary embodiments, the lower panel 100 includes a plurality of signal lines disposed on an insulation substrate 110. The plurality of signal lines may include a first signal line SL1 and a second signal line SL2 alternately arranged in the x-direction. In this manner, the first signal line SL1 and the second signal line SL2 may substantially extend in the y-direction. To this end, the longitudinal extension of the first signal line SL1 and the second signal line SL2 in the y-direction may also be periodically curved (or otherwise bent) in the x-direction, such as seen in FIG. 1. Alternatively, the first signal line SL1 and the second signal line SL2 may extend in a straight (or substantially straight) line.

[0025] The first signal line SL1 and the second signal line SL2 may transmit signals of the same or different kind. For example, the first signal line SL1 and the second signal line SL2 of the same kind may be data lines configured to transmit a data signal to each pixel PX. As another example, the first signal line SL1 may be a gate line configured to transmit a gate signal of a combination of a gate-on voltage Von and a gate-off voltage Voff to each pixel PX. In this manner, the second signal line SL2 may be a common voltage line configured to transmit a common voltage Vcom, or the second signal line SL2 may be a gate line.

[0026] As shown in FIG. 1, a respective first signal line SL1 and second signal line SL2 may be disposed in association with each pixel array in the x-direction. It is contemplated, however, that the first signal line SL1 and the second signal line SL2 may be alternatively disposed, such as, in association with, two or more pixel arrays.

[0027] A gate insulating layer 140 is disposed on the first signal line SL1 and the second signal line SL2. The gate insulating layer 140 may be made of (or otherwise include) any suitable material, such as, for example, an inorganic insulator, e.g., silicon nitride (SiNx), silicon oxide (SiOx), etc.

[0028] A first passivation layer 180a may be disposed on the gate insulating layer 140. The first passivation layer 180a may be made of (or otherwise include) any suitable material, such as, for instance, an organic insulating material and/or an inorganic insulating material. It is noted, however, that the first passivation layer 180a may be omitted.

[0029] A plurality of pixel electrodes 191 may be disposed on the first passivation layer 180a. A pixel electrode 191 disposed at each pixel PX may exhibit a planar shape, such as a polygonal shape including edges parallel to the first signal line SL1 and/or the second signal line SL2. A length of the pixel electrode 191 in the y-direction may be longer than the length in the x-direction. That is, the length of one pixel PX in the y-direction may be longer than the length in the x-direction.

[0030] According to exemplary embodiments, each pixel electrode 191 may be disposed between a first signal line SL1 and a second signal line SL2; however, any other suitable arrangement may be utilized. The pixel electrode 191 may not overlap with the first signal line SL1 or the second signal line SL2. The pixel electrode 191 may be formed of any suitable material, such as, for example, a transparent conductive material, e.g., aluminum zinc oxide (AZO), gallium zinc oxide (GZO), indium tin oxide (ITO), indium zinc oxide (IZO), etc. It is also contemplated that one or more conductive polymers (ICP) may be utilized, such as, for example, polyaniline, poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate) (PEDOT:PSS), etc.

[0031] The pixel electrode 191 may receive a data signal through a switching element (not shown), such as a thin film transistor. In this manner, the switching element may include terminals connected to the first signal line SL1 or the second signal line SL2. It is noted that the first signal line SL1 or the second signal line SL2 may be disposed at a layer closest to the insulation substrate 110 among the layers in which several terminals of the switching element are disposed. For instance, the first signal line SL1 and/or the second signal line SL2 may be directly disposed on the insulation substrate 110.

[0032] A second passivation layer 180b made of any suitable insulating material may be disposed on the pixel electrode 191.

[0033] According to exemplary embodiments, a common electrode 131 may be disposed on the second passivation layer 180b. The common electrode 131 overlaps with the pixel electrode 191 of each pixel PX. Further, the common electrode 131 may include a plurality of branch electrodes 133 substantially extending parallel to each other and separated from each other, as well as includes a boundary portion 135 overlapping with the first signal line SL1 and the second signal line SL2.

[0034] A plurality of branch electrodes 133 disposed in association with one pixel PX may be connected to each other in a lower end and an upper end thereof. A region between the branch electrodes 133 may be referred to as a slit.

[0035] In exemplary embodiments, the boundary portion 135 may be disposed close to a boundary of the pixel(s) PX neighboring the boundary portion 135 in the x-direction. As shown in FIGS. 1 and 2, the boundary portion 135 may cover the first signal line SL1 and the second signal line SL2. That is, the boundary portion 135 may cover both edge sides of the first signal line SL1 and/or the second signal line SL2. It is noted, however, that the first signal line SL1 and/or the second signal line SL2 may longitudinally extend from the boundary portion 135 in the y-direction. In exemplary embodiments, the branch electrode 133 and the boundary portion 135 may substantially extend parallel to the first signal line SL1 and the second signal line SL2.

[0036] According to exemplary embodiments, the common electrode 131 receives a common voltage, and the common electrode 131 may be disposed in association with a plurality of pixels PX that are connected to each other. When, for instance, the second signal line SL2 is a common voltage line, the common electrode 131 may be electrically connected to the second signal line SL2. The common electrode 131 may be made of (or otherwise include) any suitable material, such as one or more of the aforementioned transparent conductive materials.

[0037] The upper panel 200, according to exemplary embodiments, may include a light blocking member 220 and a color filter 230 respectively disposed on an insulation substrate 210. In this manner, the light blocking member 220 may include a portion covering (e.g., disposed over) the first signal line SL1 and the second signal line SL2, as well as include a portion overlapping with a corresponding portion of the color filter 230. The light blocking member 220 prevents light leakage between neighboring pixels PX, such that openings therein define the pixels PX. The color filter 230 may be configured to facilitate display of one or more primary colors, e.g., red, green, and/or blue. It is contemplated, however, that color filter 230 may facilitate the display of any other suitable color, such as cyan, magenta, yellow, white, etc., colors.

[0038] Unlike as shown in FIG. 2, at least one of the light blocking member 220 and the color filter 230 may be disposed on the lower panel 100.

[0039] The liquid crystal layer 3 includes liquid crystal molecules (not shown). The liquid crystal molecules may be aligned so that long axes thereof are horizontal (or otherwise parallel) to the surfaces of the lower and upper display panels 100 and 200 in a state when an electric field is not applied.

[0040] According to exemplary embodiments, when a data voltage is applied to the pixel electrode 191, an electric field is imposed on the liquid crystal layer 3 together with the common electrode 131, which may be supplied with a common voltage. In this manner, the alignment direction of the liquid crystal molecules of the liquid crystal layer 3 may be correspondingly controlled based on the fringe patterns of the electric field. As previously mentioned, the controlled alignment of the liquid crystal molecules may be utilized to facilitate the display of a corresponding image. Accordingly, the pixel electrode 191 and the common electrode 131 may be respectively referred to as field generating electrodes.

[0041] According to exemplary embodiments, the length of each pixel PX in the y-direction is longer than the length in the x-direction, and the branch electrodes 133 of the common electrode 131 may substantially extend in the y-direction. In this manner, as compared to when the branch electrodes 133 extend in the x-direction, a disclination region that may be generated at or near an end region of a slit between the branch electrodes 133 may be decreased, such that the transmittance of the liquid crystal display may be increased.

[0042] In exemplary embodiments, the first signal line SL1 or the second signal line SL2 overlapping with the boundary portion 135 of the common electrode 131 may be disposed on the layer closest to the insulation substrate 110 among the layers in which the several terminals of the switching element connected to the pixel electrode 191 are disposed. That is, according to exemplary embodiments, the first signal line SL1 or the second signal line SL2 may be disposed under the gate insulating layer 140, and, for instance, may be disposed directly on the insulation substrate 110. As such, a distance between the first signal line SL1 or the second signal line SL2 and the boundary portion 135 of the common electrode 131 or the pixel electrode 191 may be maximized. Accordingly, the parasitic capacitance between the first signal line SL1 or the second signal line SL2 and the boundary portion 135 of the common electrode 131 or the pixel electrode 191 may be reduced, such that a signal delay of the first signal line SL1 or the second signal line SL2 may be minimized. It is also noted that crosstalk between the first signal line SL1 or the second signal line SL2 and the boundary portion 135 of the common electrode 131 or the pixel electrode 191 may be reduced, such that light leakage due to electric field distortion may be reduced.

[0043] According to exemplary embodiments, since the parasitic capacitance between the first signal line SL1 or the second signal line SL2 and the boundary portion 135 of the common electrode 131 or the pixel electrode 191 may be reduced, it is not necessary to form an insulating layer formed of an organic insulating material between the first signal line SL1 or the second signal line SL2 and the common electrode 131 or the pixel electrode 191. In other words, the first passivation layer 180a may not include an organic insulating material. When, for example, the insulating layer of the first passivation layer 180a is formed of an inorganic insulating material, a material cost may be reduced, as compared with instances when an organic insulating material is utilized and a processing step, such as deposition and photo-processing is utilized, processing time to manufacture the corresponding liquid crystal display may be reduced. Furthermore, undesirable absorption of incident light by an organic insulating material may be reduced, such that the transmittance of the liquid crystal display may be further increased. To this end, it is also not necessary to form a contact hole in a comparatively thick organic insulating material, such that an aperture ratio is not undesirably reduced.

[0044] FIG. 3 is a layout view of a liquid crystal display, according to exemplary embodiments. FIG. 4 is a cross-sectional view of the liquid crystal display of FIG. 3 taken along sectional line IV-IV.

[0045] Referring to FIGS. 3 and 4, the liquid crystal display is substantially similar to the liquid crystal display illustrated in FIGS. 1 and 2; however, the liquid crystal display of FIGS. 3 and 4 includes an alternatively configured boundary portion 135 of the common electrode 131. Accordingly, to avoid obscuring exemplary embodiments described herein, duplicative descriptions of similarly configured features are omitted.

[0046] As shown in FIGS. 3 and 4, the boundary portion 135 of the common electrode 131 may include an opening 35 elongated substantially in the y-direction. In FIG. 3, while only the portion of the boundary portion 135 disposed on the first signal line SL1 includes the opening 35, it is contemplated that the portion of the boundary portion 135 disposed on the second signal line SL2 may also include an opening 35. According to exemplary embodiments, the longitudinal extension of the opening 35 may be curved (or otherwise bent) in the x-direction. Alternatively, the opening 35 may be straight or substantially straight.

[0047] A width of the opening 35 in the x-direction may be larger, smaller, or equal to the width of the first signal line SL1 or the second signal line SL2 in the x-direction. In this manner, the opening 35 may expose the edge side(s) of the first signal line SL1 or the second signal line SL2, or may cover at least one edge side thereof.

[0048] FIG. 5 is a layout view of a liquid crystal display, according to exemplary embodiments. FIG. 6 is a cross-sectional view of the liquid crystal display of FIG. 5 taken along sectional line VI-VI.

[0049] Referring to FIGS. 5 and 6, the liquid crystal display is substantially similar to the liquid crystal display illustrated in FIGS. 1 and 2; however, the liquid crystal display of FIGS. 5 and 6 may include alternative depositions and configurations of the common electrode 131 and the pixel electrode 191. Accordingly, to avoid obscuring exemplary embodiments described herein, duplicative descriptions of similarly configured features are omitted.

[0050] As seen in FIGS. 5 and 6, the common electrode 131 may be disposed on the first passivation layer 180a. The second passivation layer 180b and a plurality of pixel electrodes 191 may be sequentially disposed on the common electrode 131. The common electrode 131 may be formed on the entire surface (or a portion thereof) of the insulation substrate 110 and may include at least one opening. In this manner, the common electrode 131 may be disposed in association with each pixel PX, and, thereby, may exhibit a planar shape. Further, the common electrode 131 may overlap with the first signal line SL1 and the second signal line SL2. As shown in FIGS. 5 and 6, the common electrode 131 may cover the first signal line SL1 and the second signal line SL2.

[0051] According to exemplary embodiments, each pixel electrode 191 may overlap with a corresponding portion of the common electrode 131 disposed in association with the pixel PX including the pixel electrode 191. Further, the pixel electrode 191 may include a plurality of branch electrodes 193 substantially parallel to each other and separated from each other. A plurality of branch electrodes 133 of one pixel electrode 191 may be connected to each other at or near a lower end portion and/or an upper end portion thereof. The region between the branch electrodes 193 may be referred to as a slit.

[0052] FIG. 7 is a layout view of a liquid crystal display, according to exemplary embodiments. FIG. 8 is a cross-sectional view of the liquid crystal display of FIG. 7 taken along sectional line VIII-VIII.

[0053] Referring to FIGS. 7 and 8, the liquid crystal display is substantially similar to the liquid crystal display illustrated in FIGS. 5 and 6; however, the liquid crystal display of FIGS. 7 and 8 includes an alternatively configured common electrode 131. Accordingly, to avoid obscuring exemplary embodiments described herein, duplicative descriptions of similarly configured features are omitted.

[0054] As seen in FIGS. 7 and 8, the common electrode 131 may include a plurality of openings 35 elongated substantially in the y-direction. In FIG. 7, while only the portion of the common electrode 131 disposed over the first signal line SL1 includes opening 35, it is contemplated that the portion of the common electrode 131 disposed over the second signal line SL2 may also include an opening 35. According to exemplary embodiments, the longitudinal extension of the opening 35 may be curved (or otherwise bent) in the x-direction. Alternatively, the opening 35 may be straight or substantially straight.

[0055] A width of the opening 35 in the x-direction may be larger, smaller, or equal to the width of the first signal line SL1 or the second signal line SL2 in the x-direction. In this manner, the opening 35 may expose the edge side(s) of the first signal line SL1 or the second signal line SL2, or may cover at least one edge side thereof.

[0056] A more detailed structure of a liquid crystal display will now be described with reference to FIGS. 9-12. To avoid obscuring exemplary embodiments described herein, duplicative descriptions are omitted.

[0057] FIG. 9 is a layout view of a liquid crystal display, according to exemplary embodiments. FIG. 10 is a cross-sectional view of the liquid crystal display of FIG. 9 taken along sectional line X-X. FIG. 11 is a cross-sectional view of the liquid crystal display of FIG. 9 taken along sectional line XI-XI. FIG. 12 is a cross-sectional view of the liquid crystal display of FIG. 9 taken along sectional line XII-XII.

[0058] As seen in FIGS. 9-12, the liquid crystal display includes the lower panel 100 and the upper panel 200 facing each other, and the liquid crystal layer 3 disposed therebetween. The upper panel 200 and the liquid crystal layer 3 are configured as those previously described, and, therefore, a detailed description of these components has been omitted.

[0059] Lower panel 100, according to exemplary embodiments, includes a plurality of gate conductors, including a plurality of gate lines 121 and a plurality of common voltage lines 129 disposed on an insulation substrate 110.

[0060] The gate line 121 transmits the gate signal and longitudinally extends in substantially the y-direction. As seen in, for instance, FIG. 9, the gate line 121 may be curved (or otherwise bent) in the x-direction, or may be straight or substantially straight. Each gate line 121 includes a plurality of gate electrodes 124.

[0061] The common voltage line 129 transmits a common voltage and longitudinally extends in substantially the y-direction. In this manner, the common voltage line 129 may be substantially parallel to the gate line 121. As such, the common voltage line 129 may be curved (or otherwise bent) in the x-direction, or may be straight or substantially straight. Each common voltage line 129 may include a plurality of expansions 128.

[0062] According to exemplary embodiments, the gate line 121 and the common voltage line 129 are alternately arranged in the x-direction and are disposed in each pixel array in the x-direction; however, the gate line 121 and the common voltage line 129 may be alternatively arranged. FIG. 9 illustrates one gate line 121 being disposed in association with two pixel arrays. Further, as shown in FIG. 9, the gate line 121 and the common voltage line 129 may be periodically curved (or otherwise bent) in the y-direction.

[0063] A gate insulating layer 140 is disposed on the gate conductor. A semiconductor 154 is disposed on the gate insulating layer 140. The semiconductor 154 may be made of (or otherwise include) any suitable material, such as, for example, amorphous silicon, crystalline silicon, an oxide, etc.

[0064] A pair of ohmic contacts 163 and 165 may be disposed on each semiconductor 154. The ohmic contacts 163 and 165 may be made of (or otherwise include) any suitable material, such as, for instance, n+ hydrogenated amorphous silicon (a-Si), which may be heavily doped with an N-type impurity, such as, for example, phosphorous. Alternatively, the pair of ohmic contacts 163 and 165 may be made of a silicide. It is also contemplated that the ohmic contacts 163 and 165 may be omitted.

[0065] A data conductor, including a plurality of pairs of first and second data lines 171a and 171b, and a plurality of drain electrodes 175 may be formed on the ohmic contacts 163 and 165. The first and second data lines 171a and 171b transmit the data signal and longitudinally extend in substantially the x-direction, and, thereby, intersect the gate line 121 and the common voltage line 129. The first and second data lines 171a and 171b respectively include a plurality of source electrodes 173 extending toward the gate electrodes 124.

[0066] According to exemplary embodiments, a pair of first and second data lines 171a and 171 b may be disposed in association with one row of pixels PX. The first data line 171 a and the second data line 171b may alternately extend in the y-direction. The pixels PX of one row of pixels PX may be disposed between a pair of first and second data lines 171a and 171b. As seen in FIG. 9, however, the first data line 171 a is disposed at an upper side of one row of pixels PX and the second data line

171b is disposed at a lower side of the row of pixels PX. The first and second data lines 171a and 171b disposed between rows of pixels PX adjacent to each other in the y-direction may be disposed relatively close to each other.

[0067] The drain electrode 175 includes a bar-type end and another end including a wide area, which opposes the source electrode 173 with respect to the gate electrode 124.

[0068] The gate electrode 124, the source electrode 173, and the drain electrode 175 form a thin film transistor Q, such as a switching element, along with the semiconductor 154. A portion of the semiconductor 154 not covered by the source electrode 173 and the drain electrode 175 is exposed to form a channel region of the thin film transistor Q. As shown in FIG. 9, the thin film transistors Q of the pixels PX of a row may be alternately connected to the first and second data lines 171a and 171b disposed at the upper and lower sides, however, any other suitable arrangement may be utilized.

[0069] According to exemplary embodiments, a plurality of pixel electrodes 191 is disposed on the drain electrode 175. In this manner, a pixel electrode 191 is disposed in association with each pixel PX and may exhibit a planar shape, e.g., a polygonal shape, including edges that extend parallel to the gate line 121 and the common voltage line 129. The length of the pixel electrode 191 in the y-direction may be longer than the length in the x-direction. That is, the length of one pixel PX in the y-direction may be longer than the length in the x-direction.

[0070] Each pixel electrode 191 may be disposed between the gate line 121 and the common voltage line 129; however, any other suitable arrangement may be utilized. The pixel electrode 191 may not overlap with the gate line 121 or the common voltage line 129. The pixel electrode 191 may contact the drain electrode 175, and, thereby, may be configured to receive the data voltage from the drain electrode 175. The remaining configuration of the pixel electrode 191 is substantially the same as previously described in association with FIGS. 1 and 2, and, therefore, a corresponding detailed description has been omitted.

[0071] According to exemplary embodiments, the first passivation layer 180a may be further disposed between the pixel electrode 191 and the drain electrode 175. In this manner, the pixel electrode 191 may be electrically connected to the drain electrode 175 through a contact hole in the first passivation layer 180a.

[0072] The second passivation layer 180b may be disposed on the pixel electrode 191. The second passivation layer 180b and the gate insulating layer 140 include a contact hole 183 exposing the expansion 128 of the common voltage line 129.

[0073] A common electrode 131 may be disposed on the second passivation layer 180b. Corresponding portions of the common electrode 131 overlap with the pixel electrode 191 of each pixel PX and includes a plurality of branch electrodes 133 substantially extending parallel to each other and separated from each other. The common electrode 131 may also include a boundary portion 135 overlapping with the gate line 121 or the common voltage line 129. The boundary portion 135 may be disposed near a boundary of adjacently disposed pixels PX neighboring each other in the x-direction. The boundary portion 135 may cover the gate line 121 and the common voltage line 129. The branch electrode 133 and the boundary portion 135 of the common electrode 131 may substantially extend parallel to the gate line 121 and the common voltage line 129.

[0074] According to exemplary embodiments, the common electrode 131 contacts the expansion 128 of the common voltage line 129 via the contact hole 183, and, thereby, is electrically connected thereto. Accordingly, non-uniformity in the common voltage induced by resistance in the common electrode 131 may be reduced. The remainder of the configuration of the common electrode 131 is the same as previously described, and, therefore, a corresponding detailed description has been omitted.

[0075] According to exemplary embodiments, the length in the y-direction of each pixel PX is longer than the length in the x-direction, and the branch electrodes 133 of the common electrode 131 may substantially extend in the y-direction. As compared to branch electrodes 133 extending in the x-direction, a disclination region that may be generated at or near an end portion of the slit between branch electrodes 133 may be decreased, such that the transmittance of the liquid crystal display may be increased.

[0076] In exemplary embodiments, the gate line 121 overlapping with the boundary portion 135 of the common electrode 131 may be disposed in a layer closest to the insulation substrate 110 among the layers in which the several terminals of the thin film transistor Q are disposed. For instance, the gate line 121 may be disposed under the gate insulating layer 140, and may be disposed directly on the insulation substrate 110. As such, a distance between the gate line 121 and the boundary portion 135 of the common electrode 131 or the pixel electrode 191 may be at a maximum. The parasitic capacitance between the gate line 121 and the boundary portion 135 of the common electrode 131 or the pixel electrode 191 may, thereby, be reduced, and, as such, the signal delay of the gate line 121 may be correspondingly minimized (or otherwise reduced). Further, crosstalk between the gate line 121 and the boundary portion 135 of the common electrode 131 or the pixel electrode 191 may be reduced, such that light leakage resulting, at least in part, from electric field distortions may also be reduced.

[0077] According to exemplary embodiments, since the parasitic capacitance between the gate line 121 and the boundary portion 135 of the common electrode 131 or the pixel electrode 191 may be reduced, it is not necessary to form an insulating layer made of an organic insulating material between the gate line 121 and the common electrode 131 or the pixel electrode 191. In other words, the first passivation layer 180a may not include an organic insulating material. When, for example, the insulating layer of the first passivation layer 180a is formed of an inorganic insulating material, a material cost may be reduced, as compared with instances when an organic insulating material is utilized and a processing step, such as a deposition and photo-processing is utilized, processing time to manufacture the corresponding liquid crystal display may be reduced. Furthermore, undesirable absorption of incident light by an organic insulating material may be reduced, such that the transmittance of the liquid crystal display may be further increased. To this end, it is also not necessary to form a contact hole in a comparatively thick organic insulating material, such that an aperture ratio is not undesirably reduced. Moreover, in exemplary embodiments, the first passivation layer 180a is not formed, such that the manufacturing cost and the manufacturing time may be further reduced.

[0078] An operation of the liquid crystal display, according to exemplary embodiments, will be described with reference to FIG. 9.

[0079] According to exemplary embodiments, if the gate signal transmitted by the gate line 121 is the gate-on voltage, the thin film transistor Q connected to the gate line 121 may be turned on. In this manner, the data voltage applied to the first and second data lines 171a and 171b may be applied to the corresponding pixel electrode 191 via the "turned-on" thin film transistor Q. A difference between the data voltage applied to the pixel electrode 191 and the common voltage applied to the common electrode 131 may be considered as representing a pixel voltage. The liquid crystal molecules of liquid crystal layer 3 may be oriented depending on the magnitude of the pixel voltage, and, accordingly, polarization of incident light propagating through the liquid crystal layer 3 may vary. Such variation of the polarization appears as a variation in transmittance of light due to a polarizer (not shown), which may be coupled to the display panel, and, thereby, the pixel PX may display an image.

[0080] In association with a unit of the horizontal period 1H, the gate-on voltage may be sequentially applied to all the gate lines 121, and the data voltage may be applied to all the pixels PX, so as to display an image of one frame. Once presentation of one frame is finished, the next frame may be started, and the polarity of the data voltage applied to each pixel PX for the common voltage (hereinafter referred to as a polarity of the data voltage) may become opposite to the polarity of the previous frame.

[0081] According to exemplary embodiments, during one frame, the polarity of the data voltage respectively transmitted by the first and second data lines 171a and 171b may be uniform. Also, during one frame, at least two of the plurality of first and the second data lines 171a and 171b may transmit data voltages of different polarities. FIG. 9 is illustrates an example in which a pair of the first and second data lines 171a and 171b opposing each other with respect to one row of pixels PX transmit data voltages of different polarities during one frame. In this manner, the first and second data lines 171a and 171b adjacent to each other may transmit data voltages of the same polarity during one frame. As shown in FIG. 9, the thin film transistors Q of a pixel PX of a row of pixels PX may be alternately connected to the first and second data lines 171a and 171 b, and the pixels PX connected to the adjacent first and second data lines 171a and 171b may be adjacent in a diagonal direction, such that one-by-one (1x1) dot inversion occurs, in which the polarities of the data voltages applied to the pixels PX adjacent in the x-direction or the y-direction are opposite to each other. In this manner, display quality degradation may be reduced.

[0082] According to exemplary embodiments, while the polarities of the data voltages transmitted by the first and second data lines 171a and 171 b during one frame are uniform, various polarity inversions may be realized by applying the data voltages of the different polarities according to the positions of the first and second data lines 171a and 171b. As such, the power consumption of the data driving may be reduced.

[0083] Another operation of the liquid crystal display, according to exemplary embodiments, will be described with reference to FIGS. 13 and 14.

[0084] FIGS. 13 and 14 are respective layout views of a polarity of a data voltage in a liquid crystal display, according to exemplary embodiments.

[0085] Referring to FIG. 13, the operation of the liquid crystal display may be substantially similarly as previously described in association with FIG. 9, and therefore, duplicative descriptions have been omitted. In this manner, differences are described below.

[0086] The polarity of the data voltage transmitted by the first and second data lines 171a and 171b during one frame may be constant; however the polarities of the data voltages transmitted by the adjacent first and second data lines 171a and 171b may be opposite to each other. Accordingly, the polarities of the data voltages transmitted to a pair of the first and second data lines 171a and 171b opposing each other with respect to one row of pixels PX may be different, and the polarities of the data voltages transmitted to the first and second data lines 171a and 171b adjacent to each other may be different. As shown in FIG. 13, the thin film transistors Q of the pixels PX of a row may be alternately connected to the first and second data lines 171a and 171b, and the pixels PX connected to the first and second data lines 171a and 171b adjacent to each other are adjacent in the y-direction, such that one-by-one (1x1) dot inversion, in which the polarities of the data voltages applied to the pixels PX adjacent in the x-direction or the y-direction are opposite to each other may be realized. As such, display quality degradation may be reduced.

[0087] Referring to FIG. 14, the operation of the liquid crystal display may be substantially the same as previously described in association with FIG. 9, and, therefore, duplicative descriptions have been omitted. As such, differences are described below.

[0088] According to exemplary embodiments, the polarities of the data voltages transmitted to the first and second data lines 171a and 171b are the same as the exemplary embodiment shown in FIG. 9. The thin film transistors Q of the pixels PX of one pixel row are alternately connected to the first and second data lines 171a and 171b by two units, and the pixels PX connected to the first and second data lines 171a and 171b are adjacent to each other in a diagonal direction, such that one-by-two (1x2) dot inversion may occur, in which the polarities of the data voltages applied to the pixels PX adjacent in the y-direction are opposite to each other and the polarities of the data voltages are changed by the unit of two pixels PX in the x-direction. As such, display quality degradation may be reduced.

[0089] According to exemplary embodiments, various polarity inversions may be realized by controlling the arrangement of the thin film transistor Q and the arrangement of the polarity of the data voltage transmitted to the first and second data lines 171a and 171b.

[0090] A manufacturing method of a lower panel of an exemplary liquid crystal display is described in more detail in association with FIGS. 15-18 along with FIGS. 9-FIG. 12.

[0091] FIGS. 15-18 are respective layout views of a manufacturing method of the liquid crystal display of FIG. 9, according to exemplary embodiments.

[0092] Referring to FIG. 15, a conductive material, such as a metal, is deposited and patterned on an insulation substrate 110 to form a plurality of gate lines 121 including a gate electrode 124, and a plurality of common voltage lines 129 including an expansion 128.

[0093] As seen in FIG. 16, a gate insulating layer 140 made of, for instance, an inorganic insulating material is deposited on the gate line 121 and the common voltage line 129. A semiconductor 154 is formed on the gate insulating layer 140. Ohmic contact islands 163 and 165 may be formed on the semiconductor 154. A conductive material, such as a metal, is deposited and patterned on the semiconductor 154 to form a plurality of pairs of the first and second data lines 171a and 171b respectively including source electrodes 173 and a plurality of drain electrodes 175.

[0094] Adverting to FIG. 17, a transparent conductive material, such as AZO, GZO, ITO, IZO, etc., may be deposited and patterned on the drain electrode 175 to form a plurality of pixel electrodes 191 respectively contacting the drain electrodes 175.

[0095] With reference to FIG. 18, an inorganic insulating material is deposited and patterned on the pixel electrode 191 to form the second passivation layer 180b including a contact hole 183.

[0096] As seen in FIG. 9, a transparent conductive material, such as AZO, GZO, ITO, IZO, etc., is deposited and patterned on the second passivation layer 180b to form a common electrode 131 overlapping with the pixel electrode 191.

[0097] FIG. 19 is a layout view of a liquid crystal display, according to exemplary embodiments. FIG. 20 is a cross-sectional view of the liquid crystal display of FIG. 19 taken along sectional line XX-XX.

[0098] Referring to FIGS. 19 and 20, the liquid crystal display is substantially to the liquid crystal display illustrated in FIGS. 9-12; however, the liquid crystal display of FIGS. 19 and 20 includes an alternatively configured boundary portion 135 of the common electrode 131. Accordingly, to avoid obscuring exemplary embodiments described herein, duplicative descriptions of similarly configured features are omitted.

[0099] The boundary portion 135 of the common electrode 131 may include an opening 35 elongated substantially in the y-direction. In FIG. 19, while only the portion of the boundary portion 135 disposed on the gate line 121 includes the opening 35, it is contemplated that the portion of the boundary portion 135 disposed on the common voltage line 129 may include the opening 35. In exemplary embodiments, the longitudinal extension of the opening 35 may be curved (or otherwise bent) in the x-direction. Alternatively, the opening 35 may be straight or substantially straight.

[0100] The width of the opening 35 in the x-direction may be larger than, smaller than, or equal to the width of the gate line 121 or the common voltage line 129 in the x-direction. The opening 35 may expose the edge side(s) of the gate line 121 or the common voltage line 129, or may cover at least one edge side thereof.

[0101] FIG. 21 is a layout view of a liquid crystal display, according to exemplary embodiments. FIG. 22 is a cross-sectional view of the liquid crystal display of FIG. 21 taken along sectional line XXII-XXII.

[0102] Referring to FIGS. 21 and 22, the liquid crystal display is substantially the same as the liquid crystal display illustrated in FIGS. 9-FIG. 12; however, the liquid crystal display of FIGS. 21 and 22 includes an alternative depositions for the common electrode 131 and the pixel electrode 191. Accordingly, to avoid obscuring exemplary embodiments described herein, duplicative descriptions of similarly configured features are omitted.

[0103] Differently than shown in FIGS. 9-12, the first passivation layer 180a is disposed on the thin film transistor Q and the common electrode 131 is disposed on the first passivation layer 180a. The second passivation layer 180b and a plurality of pixel electrodes 191 may be sequentially disposed on the common electrode 131.

[0104] The common electrode 131 may be formed on the entire surface (or a portion thereof) of the insulation substrate 110, and corresponding portions of the common electrode 131 disposed in each pixel PX may have the planar shape. In exemplary embodiments, the common electrode 131 overlaps with the gate line 121 and may also overlap with the common voltage line 129. As shown in FIGS. 21-22, the common electrode 131 may cover the gate line 121.

[0105] According to exemplary embodiments, each pixel electrode 191 overlaps with the common electrode 131 in association with a corresponding pixel PX. In this manner, each pixel electrode 191 includes a plurality of branch electrodes 193 substantially parallel to each other and separated from each other. The pixel electrode 191 may be connected to the drain electrode 175 via the contact hole 185 formed in the first passivation layer 180a and the second passivation layer 180b.

[0106] FIG. 23 is a layout view of a liquid crystal display, according to exemplary embodiments. FIG. 24 is a cross-sectional view of the liquid crystal display of FIG. 23 taken along sectional line XXIV-XXIV.

[0107] Referring to FIGS. 23 and 24, the liquid crystal display is substantially the same as the liquid crystal display illustrated in FIGS. 21 and 22; however, the liquid crystal display of FIGS. 23 and 24 includes a differently configured common electrode 131. Accordingly, to avoid obscuring exemplary embodiments described herein, duplicative descriptions of similarly configured features are omitted.

[0108] As seen in FIGS. 23 and 24, the common electrode 131 may include a plurality of openings 35 longitudinally elongated in substantially the y-direction. As seen in, for instance, FIG. 23, the opening 35 may be curved (or otherwise bent) in the x-direction; however, it is also contemplated that the opening 35 may be straight or substantially straight. While the opening 35 is only disposed on the gate line 121, it is contemplated that the common electrode 131 disposed on the common voltage line 129 may include an opening 35.

[0109] The width of the opening 35 in the x-direction may be larger than, smaller than, or equal to the width of the gate line 121 or the common voltage line 129 in the x-direction. The opening 35 may expose the edge side(s) of the gate line 121 or the common voltage line 129, or may cover at least one edge side thereof.

[0110] FIG. 25 is a block diagram of a liquid crystal display, according to exemplary embodiments.

[0111] Referring to FIG. 25, a lower panel 100 of a liquid crystal display is connected to gate drivers 400a and 400b, and, thereby, is configured to receive gate signals from one or more of the gate drivers 400a and 400b. In FIG. 25, the gate drivers 400a and 400b are disposed at (or near) the upper side and the lower side of the lower panel 100. It is contemplated, however, that the gate drivers 400a and 400b may be disposed in any other suitable arrangement, such as, for instance, on only one side of the lower panel 100.

[0112] According to exemplary embodiments, the length of the lower panel 100 in the x-direction may be longer than the length in the y-direction, as shown in FIG. 25. In this manner, as compared with the gate line 121 longitudinally extending in the x-direction, the gate line 121 longitudinally extends in substantially the y-direction, such that the length of the gate line 121 is short and a number of thin film transistors Q connected to each gate line 121 may be reduced, which, thereby, reduces the delay of the gate signal. In exemplary embodiments, the longitudinal extension of the gate line 121 may be curved (or otherwise bent) in the x-direction; however, it is also contemplated that the gate line may be straight or substantially straight.

[0113] It is also noted that, when integrating the gate drivers 400a and 400b configured to apply the gate signals to the gate lines 121 on the insulation substrate 110, an area to form the gate drivers 400a and 400b may be increased as compared to instances when the gate line 121 longitudinally extends in the x-direction. As such, there exists greater design freedom in choosing where the gate drivers 400a and 400b are to be disposed. Accordingly, the width of the upper and lower edge regions (e.g., bezel regions) of the lower panel 100 may be reduced. Further, as compared to instances when the data line 171 longitudinally extends in substantially the y-direction, the data line 171 longitudinally extends in substantially the x-direction. As such, the number of data lines 171 and the number of data driving circuit chips configured to apply the data signal to the data lines 171 may be reduced. This also reduces the cost of and manufacturing time for the corresponding liquid crystal display.

[0114] FIG. 26 is a layout view of a liquid crystal display, according to exemplary embodiments. FIG. 27 is a cross-sectional view of the liquid crystal display of FIG. 26 taken along sectional line XXVII-XXVII. FIG. 28 is a cross-sectional view of the liquid crystal display of FIG. 26 taken along sectional line XXVIII-XXVIII. It is noted that the liquid crystal display of FIGS. 26-28 is substantially the same as shown in FIGS. 9-25; however, the liquid crystal display of FIGS. 26-28 includes the gate line 121 longitudinally extending in a different direction.

[0115] According to exemplary embodiments, the lower panel 100 includes a plurality of data lines 171 and a plurality of drain electrodes 175 disposed on the insulation substrate 110. The data lines 171 longitudinally extend in substantially the y-direction. In exemplary embodiments, the longitudinal extension of the data lines 171 may be curved (or otherwise bent) in the x-direction; however, it is also contemplated that the data lines 171 may be straight or substantially straight. Each data line 171 includes a plurality of source electrodes 173. The drain electrode 175 includes a portion opposing the source electrode 173.

[0116] A plurality of semiconductors 154 may be disposed on the data lines 171 and the drain electrodes 175. Each semiconductor 154 overlaps with a corresponding portion of a source electrode 173 and a drain electrode 175. The semiconductor 154 may be formed of any suitable material, such as, for instance, amorphous silicon, crystalline silicon, an oxide, etc. As a metal oxide semiconductor, the oxide semiconductor may be formed of a metal oxide, such as, for instance, zinc (Zn), indium (In), gallium (Ga), tin (Sn), titanium (Ti), etc., or a combination thereof. Ohmic contacts (not shown) may be disposed between the source electrode 173 and drain electrode 175, and the semiconductor 154.

[0117] A gate insulating layer 140 is disposed on the semiconductor 154.

[0118] A plurality of gate lines 121 including a plurality of gate electrodes 124 is disposed on the gate insulating layer 140. The gate lines 121 longitudinally extend in substantially the x-direction. Each gate electrode 124 is disposed on the semiconductor 154. For instance, each gate electrode 124 may be disposed on a portion of the semiconductor 154 corresponding to a space between the source electrode 173 and the drain electrode 175.

[0119] The gate electrode 124, the source electrode 173, and the drain electrode 175 form the thin film transistor Q along with the semiconductor 154.

[0120] According to exemplary embodiments, the first passivation layer 180a is disposed on the thin film transistor Q, and a common electrode 131 is disposed on the first passivation layer 180a. The common electrode 131 may exhibit a planar shape, and, thereby, may be formed as a plate on the entire surface (or a portion thereof) of the insulation substrate 110. To this end, the first passivation layer 180a may include an opening 38 at a region corresponding to the drain electrode 175.

[0121] The second passivation layer 180b is disposed on the common electrode 131. A plurality of pixel electrodes 191, including branch electrodes 193 and a connection 195, are disposed on the second passivation layer 180b. The connection 195 connects upper and lower ends of a plurality of branch electrodes 193.

[0122] The gate insulating layer 140, the first passivation layer 180a, and the second passivation layer 180b may include a contact hole 185 exposing the drain electrode 175. In this manner, the pixel electrode 191 may be electrically connected to the drain electrode 175 via the contact hole 185, and, thereby, configured to receive the data voltage.

[0123] A first alignment layer 11 may be coated on an inner surface of the lower panel 100.

[0124] According to exemplary embodiments, the upper panel 200 may include a light blocking member 220 and a color filter 230 disposed on an insulation substrate 210. It is contemplated, however, that at least one of the light blocking member 220 and the color filter 230 may be disposed on the lower panel 100. A second alignment layer 21 may be coated on the color filter 230 and the light blocking member 220.

[0125] In exemplary embodiments, the first alignment layer 11 and the second alignment layer 21 may be horizontal alignment layers. It is contemplated, however, that any other suitable configuration may be utilized.

[0126] According to exemplary embodiments, the common electrode 131 of FIGS. 26-28 may include a plurality of openings (not shown) formed along the data line 171, such as previously described in association with FIGS. 7 and 8 and in FIGS. 23 and 24.

[0127] FIG. 29 is a layout view of a liquid crystal display, according to exemplary embodiments. FIG. 30 is a cross-sectional view of the liquid crystal display of FIG. 29 taken along sectional line XXX-XXX. FIG. 31 is a cross-sectional view of the liquid crystal display of FIG. 29 taken along sectional line XXXI-XXXI. The liquid crystal display of FIGS. 29-31 is substantially the same as shown in FIGS. 26-28, however, the liquid crystal display of FIGS. 29-31 may include differently disposed pixel electrodes 191 and common electrode 131.

[0128] For instance, differently than as shown in FIGS. 26-28, the first passivation layer 180a, in FIGS. 29-31, is disposed on the thin film transistor Q. A plurality of pixel electrodes 191 is disposed on the first passivation layer 180a. The second passivation layer 180b and the common electrode 131 may be sequentially disposed on the pixel electrode 191.

[0129] According to exemplary embodiments, the pixel electrode 191 may have a planar shape, which may fill most of the region enclosed by the gate line 121 and the data line 171. The shape of the pixel electrode 191 may polygonal with edges substantially extending parallel to the gate lines 121 and the data line 171. The pixel electrode 191 may be electrically connected to the drain electrode 175 via the contact hole 185, which is formed in the gate insulating layer 140 and the first passivation layer 180a. As such, the pixel electrode 191 may be configured to receive the data voltage.

[0130] The common electrode 131 includes a plurality of branch electrodes 133 overlapping with each pixel electrode 191 and a boundary portion 135 overlapping with the data line 171. The boundary portion 135 may be disposed close to a boundary of adjacently disposed pixels PX neighboring each other in the x-direction. The boundary portion 135 covers the data line 171 and may longitudinally extend substantially parallel to the data line 171.

[0131] According to exemplary embodiments, the boundary portion 135 of the common electrode 131 may include a plurality of openings (not shown) formed along the data line 171, such as previously described in association with FIGS. 3 and 4 or FIGS. 19 and 20.

[0132] Accordingly, it is noted that the liquid crystal displays shown in FIGS. 26-28 or FIGS. 29-31 may include the data line 171 being disposed between the pixel array and the branch electrode 193 of the pixel electrode 191. The data line 171 may longitudinally extend in substantially the y-direction. Further, the common electrode 131 may overlap with the data line 171. It is also noted that the data line 171 may be disposed as the layer closest to the insulation substrate 110 among the layers where the several terminals of the thin film transistor Q connected to the pixel electrode 191 are positioned. That is, the data line 171 may be disposed under the gate insulating layer 140, such as, for instance, directly disposed on the insulation substrate 110. As such, the distance between the data line 171 and the common electrode 131 or the pixel electrode 191 may be maximized (or otherwise increased). Further, the parasitic capacitance between the data line 171 and the common electrode 131 or the pixel electrode 191 may be reduced, which, thereby, minimizes (or otherwise reduces) the signal delay of the data line

171. Also, crosstalk between the data line 171 and the common electrode 131 or the pixel electrode 191 may be reduced, which, thereby, reduces light leakage resulting from, for instance, electric field distortion(s).

[0133] According to exemplary embodiments, it is not necessary to form an insulating layer made of an organic insulating material between the data line 171 and the common electrode 131 or the pixel electrode 191. Accordingly, as compared to instances when an insulating layer made of an organic insulating material is disposed between the data line 171 and the common electrode 131 or the pixel electrode 191, the material cost, in exemplary embodiments, may be reduced and the processing steps, such as the deposition and the photo-processing steps, and time may be reduced. Further, absorption of incident light by an organic insulating material may be avoided (or otherwise reduced) such that the transmittance of the corresponding liquid crystal display may be increased. Moreover, it is not necessary to form a contact hole in a thick organic insulating material, such that an aperture ratio of the liquid crystal display is not undesirably reduced.

[0134] While certain exemplary embodiments and implementations have been described herein, other embodiments and modifications will be apparent from this description. Accordingly, the invention is not limited to such embodiments, but rather to the scope of the presented claims.

[0135] The liquid crystal display as per the invention may further comprise the following features, in combination with any one of claims 1 to 15:

- The first signal lines and the common voltage lines are alternately arranged in a second direction different from the first direction;
- Pixel electrodes in a row of pixels arranged in the second direction are alternately connected to a first data line of the data lines and a second data line of the data lines; and the first and second data lines are configured to transmit data voltages of opposite polarities;
- Common voltage lines longitudinally extending substantially parallel to the first signal line, the common voltage lines being disposed on the same layer as the first signal line, wherein the common electrode is connected to a first common voltage line of the common voltage lines;
- The first signal lines and the common voltage lines are alternately arranged in a second direction different from the first direction;
- The first signal line comprises a data line configured to transmit a data signal to the thin film transistor;
- A gate line disposed on the gate insulating layer, the gate line being connected to the first electrode and intersecting the data line, wherein the thin film transistor further comprises: a source electrode connected to the data line, a drain electrode facing the source electrode, and a semiconductor disposed on respective portions of the source electrode and the drain electrode.

Claims

1. A liquid crystal display, comprising:

a substrate (110);
first signal lines (SL1) disposed on the substrate (110), the first signal lines (SL1) longitudinally extending in substantially a first direction;
a gate insulating layer (140) disposed on the first signal lines (SL1);
a first electrode (173) disposed on the gate insulating layer (140);
a thin film transistor (Q) connected to a first signal line (SL1) of the first signal lines (SL1), the thin film transistor (Q) comprising the gate insulating layer (140) and the first electrode (173);
a pixel electrode (191) longitudinally extending in substantially the first direction, the pixel electrode (191) being connected to the thin film transistor (Q) and configured to receive a data voltage from the thin film transistor (Q);
a common electrode (131) overlapping with at least a portion of the pixel electrode (191); and
a first insulating layer (180b) disposed between the pixel electrode (191) and the common electrode (131),
wherein:

one of the pixel electrode (191) and the common electrode (131) has a planar shape and the other comprises branch electrodes (133; 193) overlapping with at least a portion of the planar-shaped electrode,
the branch electrodes (133; 193) extend substantially parallel to the first signal line (SL1), and
at least a portion of the common electrode (131) overlaps with at least a portion of the first signal line (SL1).

2. The liquid crystal display of claim 1, wherein:

at least the portion of the common electrode (131) overlapping with at least the portion of the first signal line (SL1) comprises an opening (35) extending along at least the portion of the first signal line (SL1).

3. The liquid crystal display of claim 2, wherein:

the first signal line (SL1) comprises a gate line (121) configured to transmit a gate signal to the thin film transistor (Q).

4. The liquid crystal display of claim 3, further comprising:

data lines (171 a, 171b) disposed on the gate insulating layer (140), the data lines (171 a, 171 b) intersecting the gate line (121),
wherein the first electrode (173) is connected to a first data line of the data lines (171 a, 171 b), and
wherein the thin film transistor (Q) further comprises:

a second electrode (175) facing the first electrode (173), the second electrode (175) being connected to the pixel electrode (191), and
a semiconductor (154) overlapping with at least a portion of the first electrode (173) and the second electrode (175).

5. The liquid crystal display of claim 4, further comprising:

common voltage lines (129) longitudinally extending substantially parallel to the first signal line (SL1), the common voltage lines (129) being disposed on the same layer as the first signal line (SL1),
wherein the common electrode (131) is connected to a first common voltage line of the common voltage lines (129).

6. The liquid crystal display of claim 5, wherein:

the first signal lines (SL1) and the common voltage lines (129) are alternately arranged in a second direction different from the first direction.

7. The liquid crystal display of claim 6, wherein:

pixel electrodes (191) in a row of pixels arranged in the second direction are alternately connected to a first data line of the data lines (171 a, 171 b) and a second data line of the data lines (171 a, 171 b); and
the first and second data lines (171 a, 171 b) are configured to transmit data voltages of opposite polarities.

8. The liquid crystal display of claim 7, further comprising:

a second insulating layer disposed between the first signal line (SL1) and the common electrode (131),
wherein the second insulating layer does not comprise an organic insulating material.

9. The liquid crystal display of claim 2, wherein:

the first signal line (SL1) comprises a data line (171 a, 171 b) configured to transmit a data signal to the thin film transistor (Q).

10. The liquid crystal display of claim 9, further comprising:

a gate line (121) disposed on the gate insulating layer (140), the gate line (121) being connected to the first electrode (173) and intersecting the data line (171 a, 171 b),
wherein the thin film transistor (Q) further comprises:

a source electrode (173) connected to the data line (171 a, 171 b),
a drain electrode (175) facing the source electrode (173), and
a semiconductor (154) disposed on respective portions of the source electrode (173) and the drain electrode (175).

11. The liquid crystal display of claim 10, further comprising:

a second insulating layer disposed between the first signal line (SL1) and the common electrode (131),
wherein the second insulating layer does not comprise an organic insulating material.

12. The liquid crystal display of claim 10, wherein:

the semiconductor (154) comprises an oxide semiconductor.

13. The liquid crystal display of claim 1, wherein:

the first signal line (SL1) comprises a gate line (121) configured to transmit a gate signal to the thin film transistor (Q).

14. The liquid crystal display of claim 13, further comprising:

data lines (171a, 171b) disposed on the gate insulating layer (140), the data lines (171 a, 171 b) intersecting the gate line (121),
wherein the first electrode (173) is connected to a first data line of the data lines (171 a, 171b), and
wherein the thin film transistor (Q) further comprises:

a second electrode (175) facing the first electrode (173), the second electrode (175)

being connected to the pixel electrode (191), and
a semiconductor (154) disposed on respective portions of the first electrode (173) and the second electrode (175).

15. The liquid crystal display of claim 14, further comprising:

common voltage lines (129) longitudinally extending substantially parallel to the first signal line (SL1), the common voltage lines (129) being disposed on the same layer as the first signal line (SL1),
wherein the common electrode (131) is connected to a first common voltage line of the common voltage lines (129).

Patentansprüche

1. Flüssigkristallanzeige, umfassend:

ein Substrat (110);
erste Signalleitungen (SL1), die auf dem Substrat (110) angeordnet sind, wobei sich die ersten Signalleitungen (SL1) in Längsrichtung im Wesentlichen in einer ersten Richtung erstrecken;
eine Gate-Isolierschicht (140), die auf den ersten Signalleitungen (SL1) angeordnet ist;
eine erste Elektrode (173), die auf der Gate-Isolierschicht (140) angeordnet ist;
einen Dünnschichttransistor (Q), der mit einer ersten Signalleitung (SL1) der ersten Signalleitungen (SL1) verbunden ist, wobei der Dünnschichttransistor (Q) die Gate-Isolierschicht (140) und die erste Elektrode (173) umfasst;
eine Pixelelektrode (191), die sich in Längsrichtung im Wesentlichen in der ersten Richtung erstreckt, wobei die Pixelelektrode (191) mit dem Dünnschichttransistor (Q) verbunden ist und dafür ausgelegt ist, eine Datenspannung vom Dünnschichttransistor (Q) zu empfangen;
eine gemeinsame Elektrode (131), die wenigstens einen Teil der Pixelelektrode (191) überlappt; und
eine erste Isolierschicht (180b), die zwischen der Pixelelektrode (191) und der gemeinsamen Elektrode (131) angeordnet ist,
wobei:

eine aus der Pixelelektrode (191) und der gemeinsamen Elektrode (131) eine ebene Form aufweist und die andere Zweigelektroden (133; 193) aufweist, die wenigstens einen Teil der ebenen Elektrode überlappen, sich die Zweigelektroden (133; 193) im Wesentlichen parallel zur ersten Signalleitung (SL1) erstrecken, und
wenigstens ein Teil der gemeinsamen Elektrode (131) wenigstens einen Teil der ersten Signalleitung (SL1) überlappt.

2. Flüssigkristallanzeige nach Anspruch 1, wobei:

wenigstens der Teil der gemeinsamen Elektrode (131), der wenigstens einen Teil der ersten Signalleitung (SL1) überlappt, eine Öffnung (35) aufweist, die sich entlang von wenigstens dem Teil der ersten Signalleitung (SL1) erstreckt.

3. Flüssigkristallanzeige nach Anspruch 2, wobei:

die erste Signalleitung (SL1) eine Gate-Leitung (121) umfasst, die dafür ausgelegt ist, ein Gate-Signal zum Dünnschichttransistor (Q) zu übertragen.

4. Flüssigkristallanzeige nach Anspruch 3, ferner umfassend:

Datenleitungen (171 a, 171 b), die auf der Gate-Isolierschicht (140) angeordnet sind, wobei die Datenleitungen (171 a, 171 b) die Gate-Leitung (121) kreuzen,
wobei die erste Elektrode (173) mit einer ersten Datenleitung der Datenleitungen (171 a, 171 b) verbunden ist, und
wobei der Dünnschichttransistor (Q) ferner Folgendes umfasst:

eine zweite Elektrode (175), die der ersten Elektrode (173) gegenüberliegt, wobei die zweite Elektrode (175) mit der Pixelelektrode (191) verbunden ist, und
einen Halbleiter (154), der wenigstens einen Teil der ersten Elektrode (173) und der zweiten Elektrode (175) überlappt.

5. Flüssigkristallanzeige nach Anspruch 4, ferner umfassend:

gemeinsame Spannungsleitungen (129), die sich in Längsrichtung im Wesentlichen parallel zur ersten Signalleitung (SL1) erstrecken, wobei die gemeinsamen Spannungsleitungen (129) auf der gleichen Schicht wie die erste Signalleitung (SL1) angeordnet sind,
wobei die gemeinsame Elektrode (131) mit einer ersten gemeinsamen Spannungsleitung der gemeinsamen Spannungsleitungen (129) verbunden ist.

6. Flüssigkristallanzeige nach Anspruch 5, wobei:

die ersten Signalleitungen (SL1) und die gemeinsamen Spannungsleitungen (129) abwechselnd in einer zweiten Richtung angeordnet sind, die sich von der ersten Richtung unterscheidet.

7. Flüssigkristallanzeige nach Anspruch 6, wobei:

Pixelelektroden (191) in einer in der zweiten Richtung angeordneten Pixelreihe abwechselnd mit einer ersten Datenleitung der Datenleitungen (171 a, 171 b) und einer zweiten Datenleitung der Datenleitungen (171 a, 171 b) verbunden sind; und
die ersten und zweiten Datenleitungen (171 a, 171 b) dafür ausgelegt sind, Datenspannungen mit entgegengesetzten Polaritäten zu übertragen.

8. Flüssigkristallanzeige nach Anspruch 7, ferner umfassend:

eine zweite Isolierschicht, die zwischen der ersten Signalleitung (SL1) und der gemeinsamen Elektrode (131) angeordnet ist,
wobei die zweite Isolierschicht kein organisches Isoliermaterial umfasst.

9. Flüssigkristallanzeige nach Anspruch 2, wobei:

die erste Signalleitung (SL1) eine Datenleitung (171 a, 171 b) umfasst, die dafür ausgelegt ist, ein Datensignal zum Dünnschichttransistor (Q) zu übertragen.

10. Flüssigkristallanzeige nach Anspruch 9, ferner umfassend:

eine Gate-Leitung (121), die auf der Gate-Isolierschicht (140) angeordnet ist, wobei die Gate-Leitung (121) mit der ersten Elektrode (173) verbunden ist und die Datenleitung (171 a, 171 b) kreuzt,
wobei der Dünnschichttransistor (Q) ferner Folgendes umfasst:

eine Source-Elektrode (173), die mit der Datenleitung (171a, 171b) verbunden ist,
eine Drain-Elektrode (175), die der Source-Elektrode (173) gegenüberliegt, und
einen Halbleiter (154), der auf jeweiligen Abschnitten der Source-Elektrode (173) und der Drain-Elektrode (175) angeordnet ist.

11. Flüssigkristallanzeige nach Anspruch 10, ferner umfassend:

eine zweite Isolierschicht, die zwischen der ersten Signalleitung (SL1) und der gemeinsamen Elektrode (131) angeordnet ist,
wobei die zweite Isolierschicht kein organisches Isoliermaterial umfasst.

12. Flüssigkristallanzeige nach Anspruch 10, wobei:

der Halbleiter (154) einen Oxid-Halbleiter umfasst.

13. Flüssigkristallanzeige nach Anspruch 1, wobei:

die erste Signalleitung (SL1) eine Gate-Leitung (121) umfasst, die dafür ausgelegt ist, ein Gate-Signal zum Dünnschichttransistor (Q) zu übertragen.

14. Flüssigkristallanzeige nach Anspruch 13, ferner umfassend:

Datenleitungen (171 a, 171 b), die auf der Gate-Isolierschicht (140) angeordnet sind, wobei die Datenleitungen (171 a, 171 b) die Gate-Leitung (121) kreuzen,
wobei die erste Elektrode (173) mit einer ersten Datenleitung der Datenleitungen (171a, 171b) verbunden ist, und
wobei der Dünnschichttransistor (Q) ferner Folgendes umfasst:

eine zweite Elektrode (175), die der ersten Elektrode (173) gegenüberliegt, wobei die zweite Elektrode (175) mit der Pixelelektrode (191) verbunden ist, und
einen Halbleiter (154), der auf jeweiligen Abschnitten der ersten Elektrode (173) und der zweiten Elektrode (175) angeordnet ist.

15. Flüssigkristallanzeige nach Anspruch 14, ferner umfassend:

gemeinsame Spannungsleitungen (129), die sich in Längsrichtung im Wesentlichen parallel zur ersten Signalleitung (SL1) erstrecken, wobei die gemeinsamen Spannungsleitungen (129) auf der gleichen Schicht wie die erste Signalleitung (SL1) angeordnet sind,
wobei die gemeinsame Elektrode (131) mit einer ersten gemeinsamen Spannungsleitung der gemeinsamen Spannungsleitungen (129) verbunden ist.

Revendications

1. Affichage à cristaux liquides comprenant :

un substrat (110) ;

des premières lignes de signal (SL1) disposées sur le substrat (110), lesquelles premières lignes de signal (SL1) s'étendent dans le sens longitudinal sensiblement dans une première direction ;
une couche d'isolation de grille (140) disposée sur les premières lignes de signal (SL1);
une première électrode (173) disposée sur la couche d'isolation de grille (140) ;
un transistor en couche mince (Q) connecté à une première ligne de signal (SL1) parmi les premières lignes de signal (SL1), le transistor en couche mince (Q) comprenant la couche d'isolation de grille (140) et la première électrode (173) ;
une électrode de pixel (191) qui s'étend dans le sens longitudinal dans sensiblement la première direction, laquelle électrode de pixel (191) est connectée au transistor en couche mince (Q) et configurée pour recevoir une tension de données du transistor en couche mince (Q) ;
une électrode commune (131) recouvrant au moins une partie de l'électrode de pixel (191) ; et
une première couche isolante (180b) disposée entre l'électrode de pixel (191) et l'électrode commune (131),
dans lequel :

soit l'électrode de pixel (191), soit l'électrode commune (131) a une forme plane et l'autre comprend des électrodes de ramification (133 ; 193) qui recouvrent au moins une partie de l'électrode de forme plane,
les électrodes de ramification (133 ; 193) s'étendent de façon sensiblement parallèle à la première ligne de signal (SL1), et
au moins une partie de l'électrode commune (131) recouvre au moins une partie de la première ligne de signal (SL1).

2. Affichage à cristaux liquides selon la revendication 1, dans lequel au moins la partie de l'électrode commune (131) qui recouvre au moins la partie de la première ligne de signal (SL1) comprend une ouverture (35) qui s'étend le long d'au moins la partie de la première ligne de signal (SL1).

3. Affichage à cristaux liquides selon la revendication 2, dans lequel la première ligne de signal (SL1) comprend une ligne de grille (121) configurée pour transmettre un signal de grille au transistor en couche mince (Q).

4. Affichage à cristaux liquides selon la revendication 3, comprenant en outre des lignes de données (171a, 171b) disposées sur la couche d'isolation de grille (140), lesquelles lignes de données (171a, 171b) croisent la ligne de grille (121), dans lequel la première électrode (173) est connectée à une première ligne de données parmi les lignes de données (171 a, 171 b), et
dans lequel le transistor en couche mince (Q) comprend en outre :

une deuxième électrode (175) faisant face à la première électrode (173), laquelle deuxième électrode (175) est connectée à l'électrode de pixel (191), et
un semi-conducteur (154) recouvrant au moins une partie de la première électrode (173) et de la deuxième électrode (175).

5. Affichage à cristaux liquides selon la revendication 4, comprenant en outre des lignes de tension commune (129) qui s'étendent longitudinalement de façon sensiblement parallèle à la première ligne de signal (SL1), les lignes de tension commune (129) étant disposées sur la même couche que la première ligne de signal (SL1), l'électrode commune (131) étant connectée à une première ligne de tension commune parmi les lignes de tension commune (129).

6. Affichage à cristaux liquides selon la revendication 5, dans lequel les premières lignes de signal (SL1) et les lignes de tension commune (129) sont disposées alternativement dans une deuxième direction différente de la première direction.

7. Affichage à cristaux liquides selon la revendication 6, dans lequel les électrodes de pixel (191) d'une ligne de pixels disposée dans la deuxième direction sont connectées alternativement à une première ligne de données parmi les lignes de données (171a, 171b) et à une deuxième ligne de données parmi les lignes de données (171a, 171b) ; et
les première et deuxième lignes de données (171 a, 171 b) sont configurées pour transmettre des tensions de données de polarité opposée.

8. Affichage à cristaux liquides selon la revendication 7, comprenant en outre une deuxième couche isolante disposée entre la première ligne de signal (SL1) et l'électrode commune (131), laquelle deuxième couche isolante ne contient pas de matériau isolant organique.

9. Affichage à cristaux liquides selon la revendication 2, dans lequel la première ligne de signal (SL1) comprend une ligne de données (171 a, 171 b) configurée pour transmettre un signal de données au transistor en couche mince (Q).

10. Affichage à cristaux liquides selon la revendication 9, comprenant en outre :

une ligne de grille (121) disposée sur la couche d'isolation de grille (140), laquelle ligne de grille (121) est connectée à la première électrode (173) et croise la ligne de données (171a, 171b), dans lequel le transistor en couche mince (Q) comprend en outre :

une électrode de source (173) connectée à la ligne de données (171a, 171b), une électrode de drain (175) faisant face à l'électrode de source (173), et
un semi-conducteur (154) disposé sur des parties respectives de l'électrode de source (173) et de l'électrode de drain (175).

11. Affichage à cristaux liquides selon la revendication 10, comprenant en outre une deuxième couche isolante disposée entre la première ligne de signal (SL1) et l'électrode commune (131), laquelle deuxième couche isolante ne contient pas de matériau isolant organique.

12. Affichage à cristaux liquides selon la revendication 10, dans lequel le semi-conducteur (154) comprend un semi-conducteur en oxyde.

13. Affichage à cristaux liquides selon la revendication 1, dans lequel la première ligne de signal (SL1) comprend une ligne de grille (121) configurée pour transmettre un signal de grille au transistor en couche mince (Q).

14. Affichage à cristaux liquides selon la revendication 13, comprenant en outre des lignes de données (171 a, 171 b) disposées sur la couche d'isolation de grille (140), lesquelles lignes de données (171 a, 171 b) croisent la ligne de grille (121), dans lequel la première électrode (173) est connectée à une première ligne de données parmi les lignes de données (171 a, 171 b), et
dans lequel le transistor en couche mince (Q) comprend en outre :

une deuxième électrode (175) faisant face à la première électrode (173), laquelle deuxième électrode (175) est connectée à l'électrode de pixel (191), et
un semi-conducteur (154) disposé sur des parties respectives de la première électrode (173) et de la deuxième électrode (175).

15. Affichage à cristaux liquides selon la revendication 14, comprenant en outre des lignes de tension commune (129) qui s'étendent longitudinalement de façon sensiblement parallèle à la première ligne de signal (SL1), lesquelles lignes de tension commune (129) sont disposées sur la même couche que la première ligne de signal (SL1),
dans lequel l'électrode commune (131) est connectée à une première ligne de tension commune parmi les lignes de tension commune (129).

FIG. 1

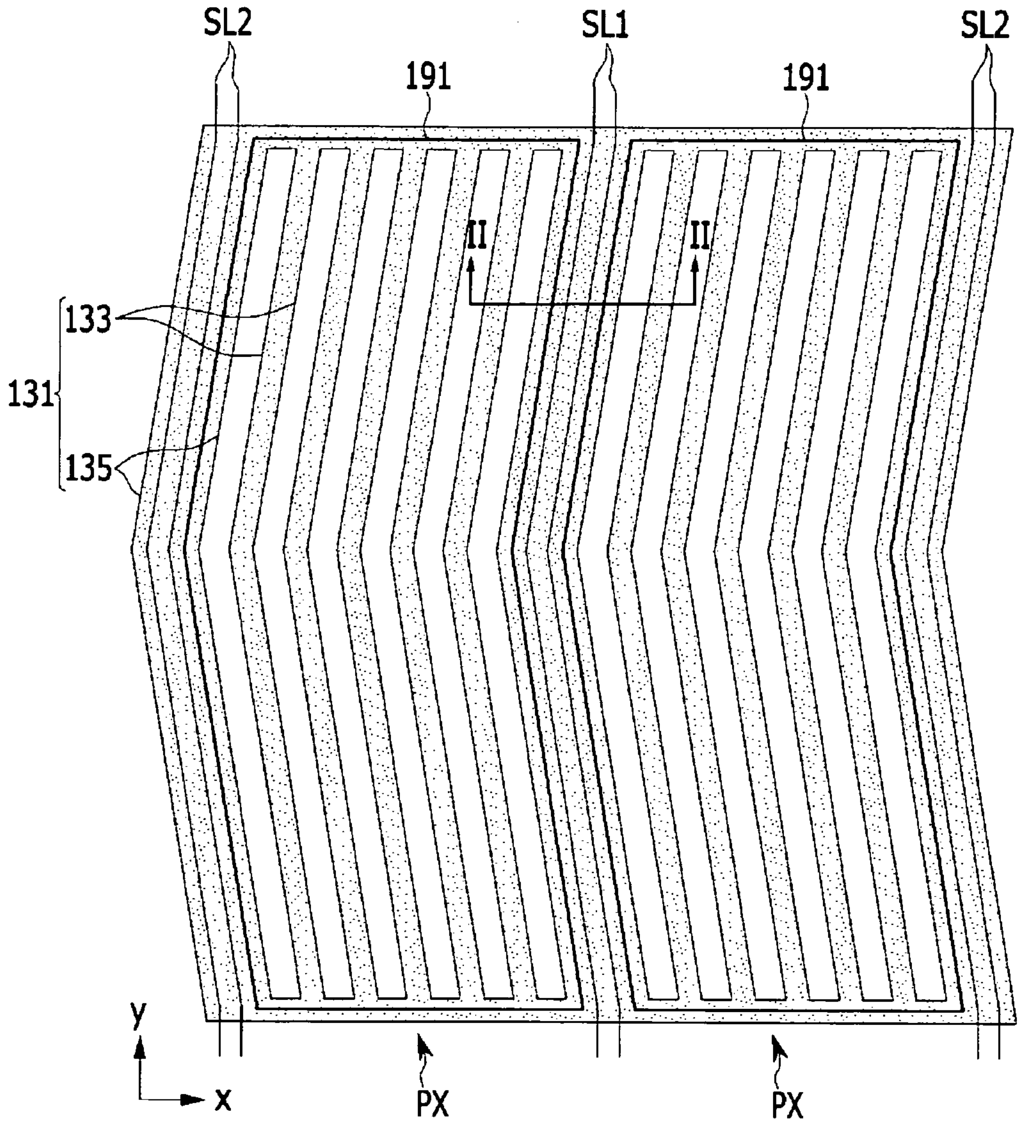


FIG. 2

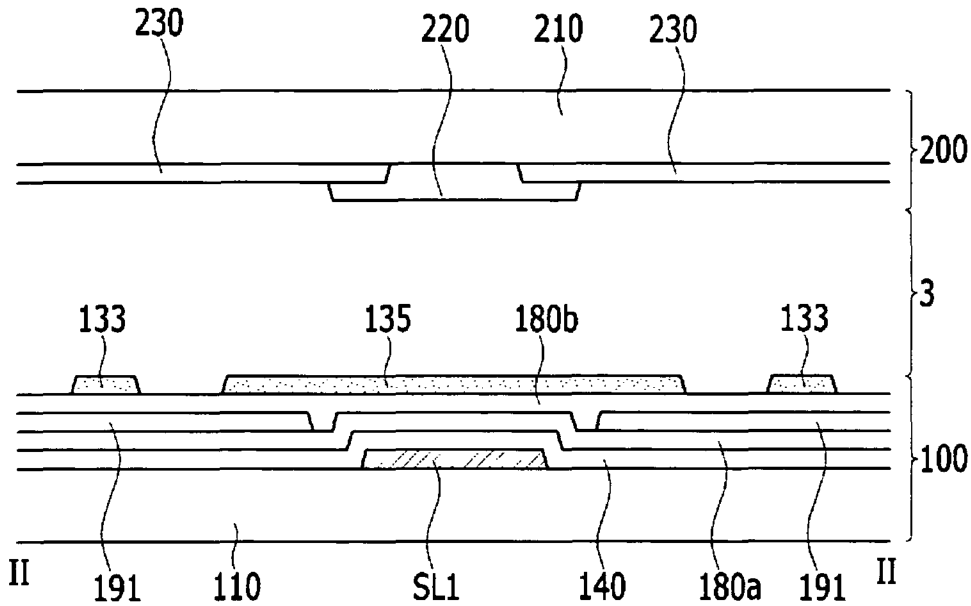

230
220
210
230
200
3
133
135
180b
133
100
II
191
110
SL1
140
180a
191
II

FIG. 3

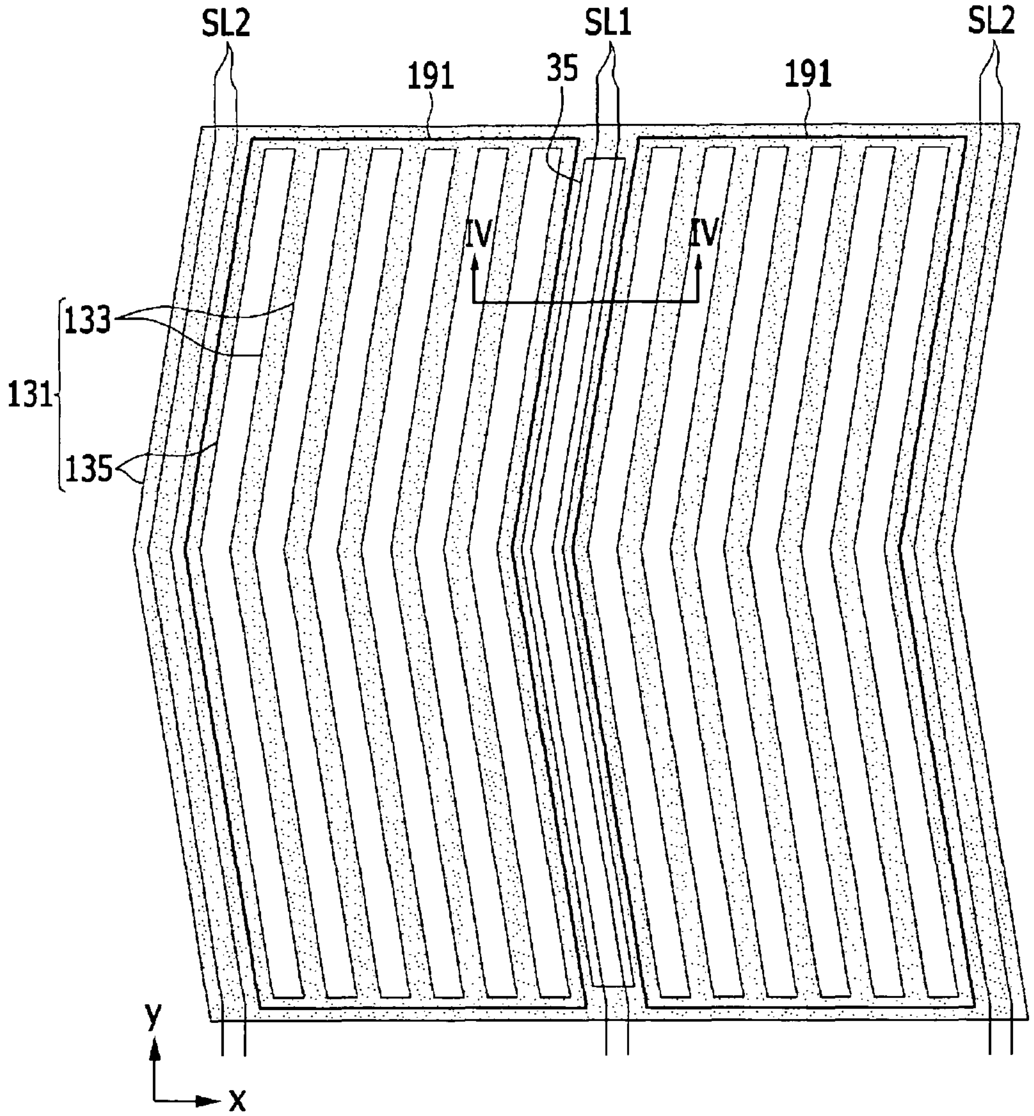


FIG. 4

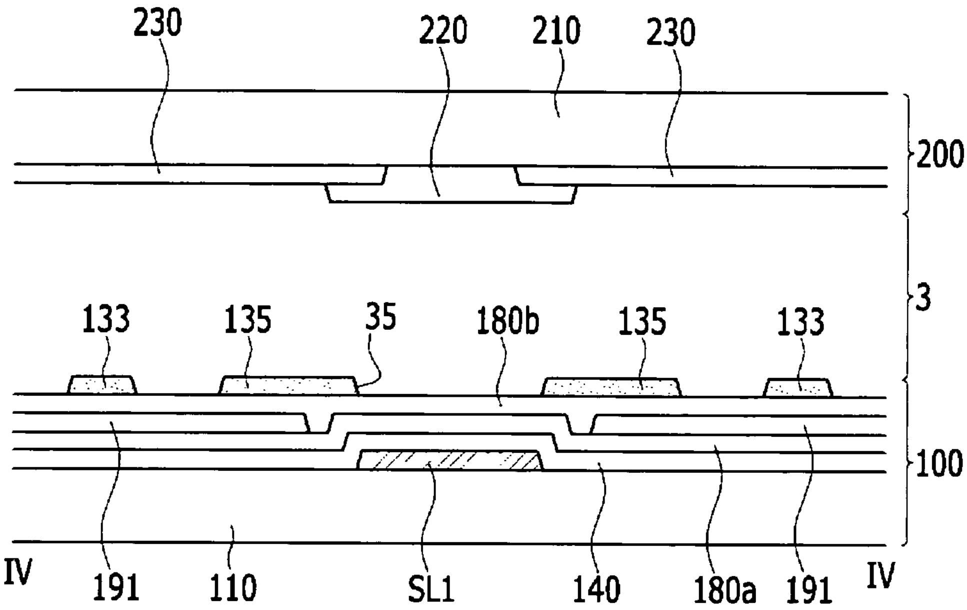

230
220
210
230
200
3
133
135
35
180b
135
133
100
IV
191
110
SL1
140
180a
191
IV

FIG. 5

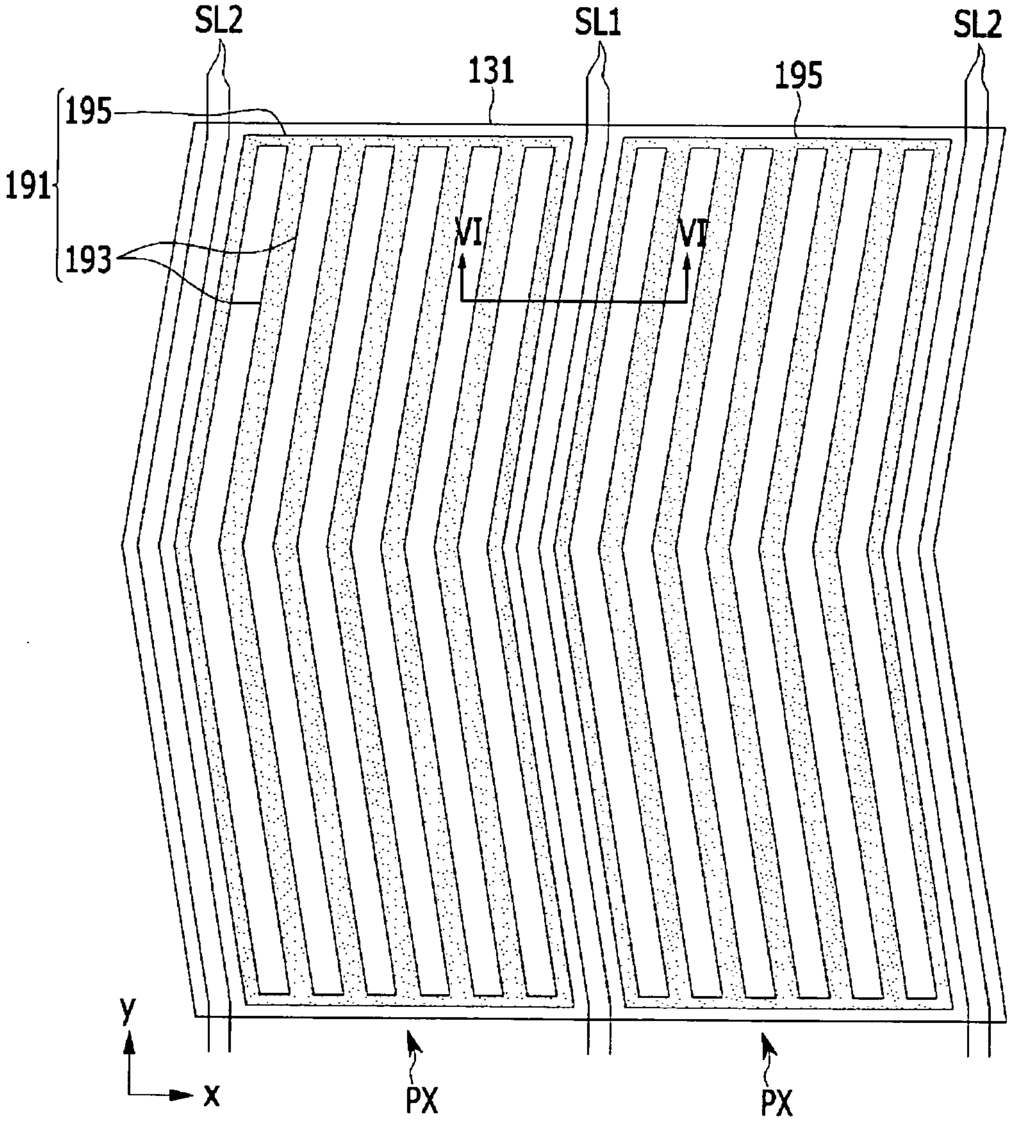


FIG. 6

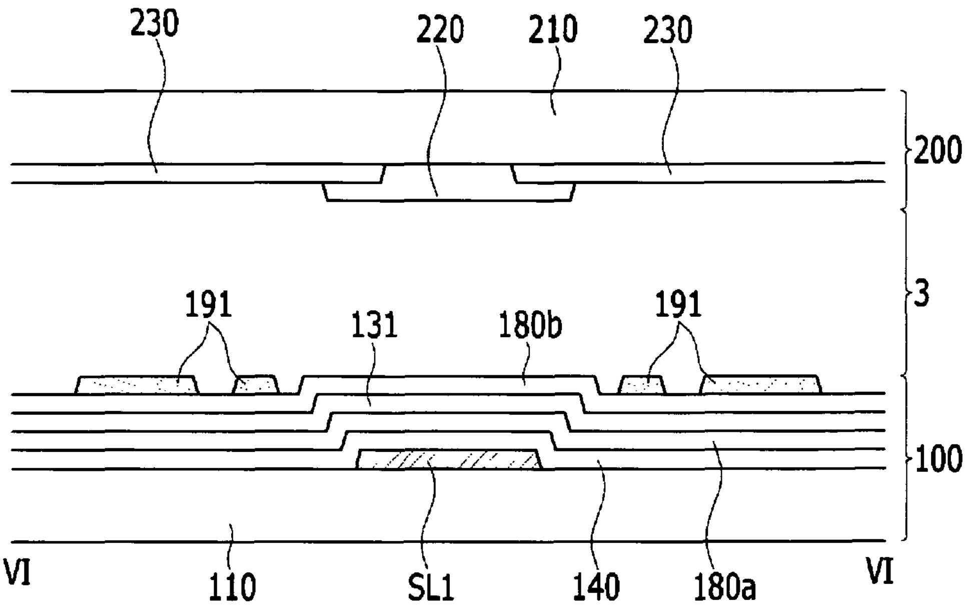


FIG. 7

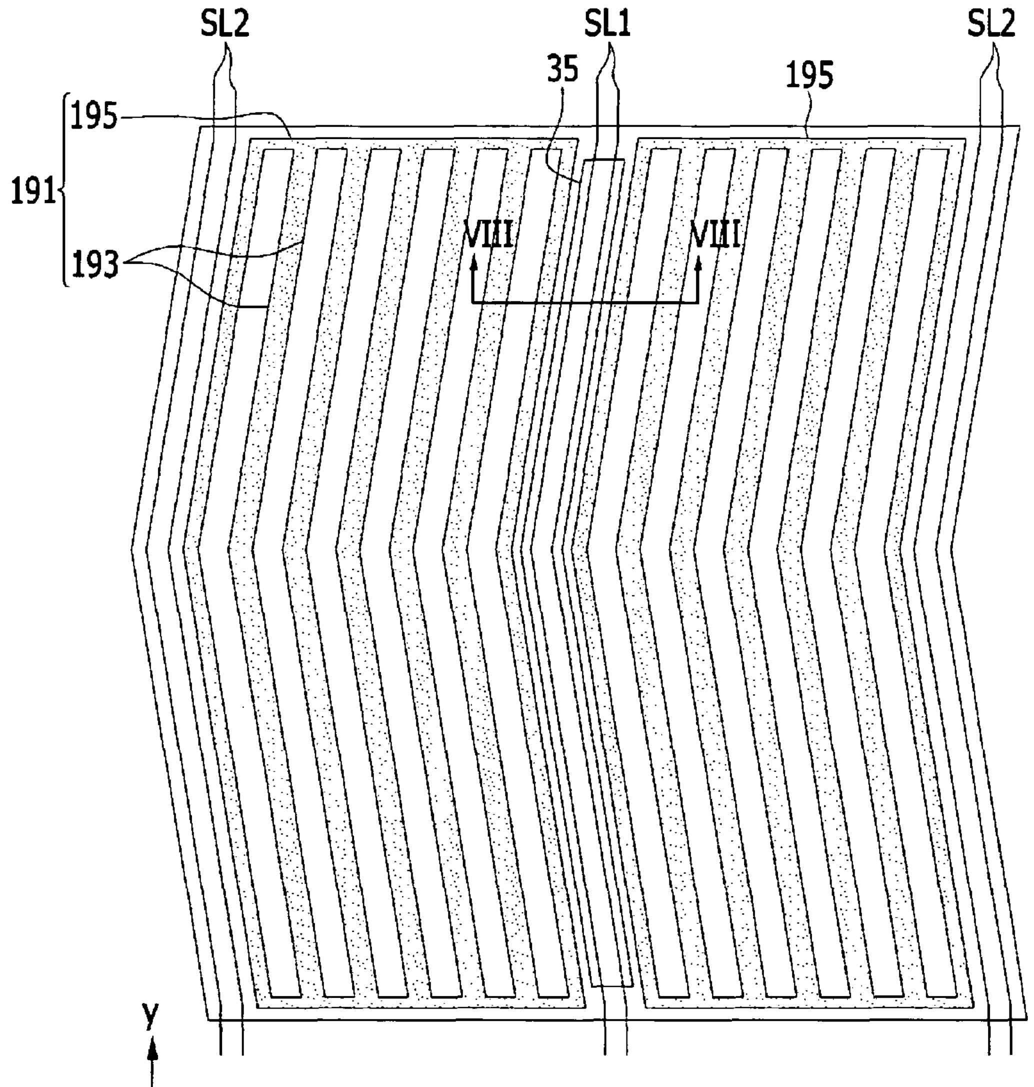


FIG. 8

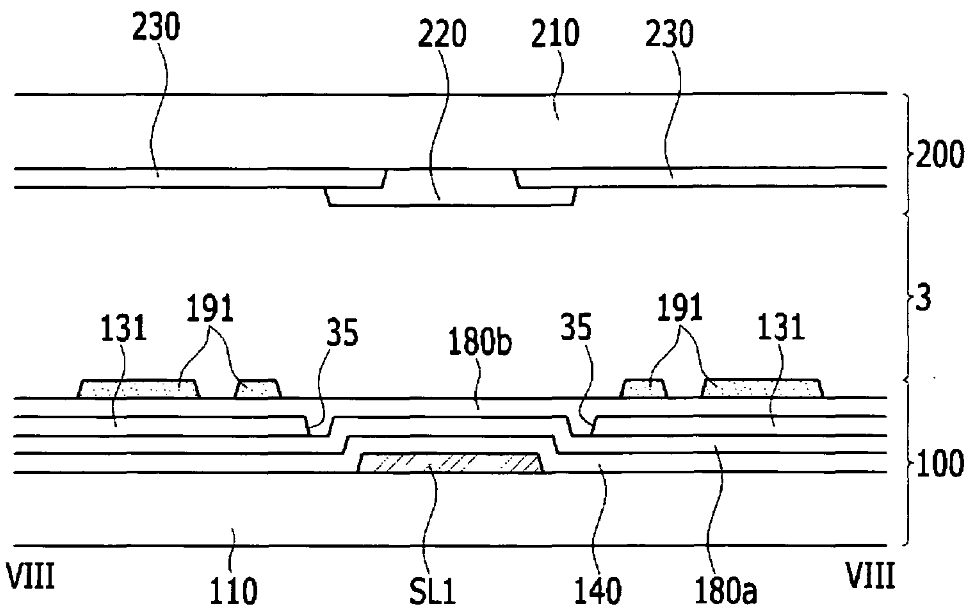
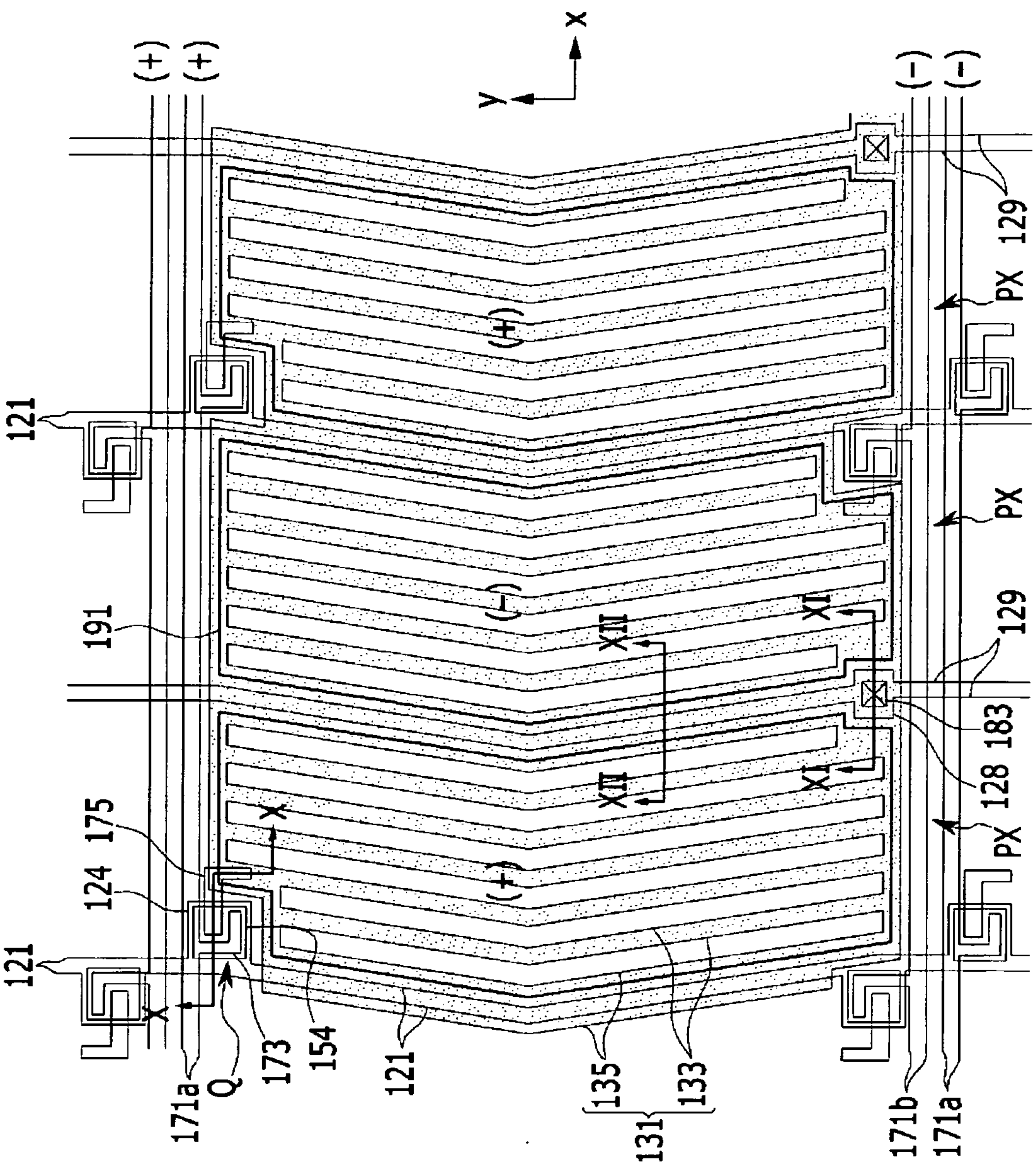

230
220
210
230
200
3
131
191
35
180b
35
191
131
100
VIII
110
SL1
140
180a
VIII

FIG. 9



x
y
(+)
(-)
121
191
124
175
X
Q
173
154
135
133
131
171a
171b
129
PX
128
183
XI
XII

FIG. 10

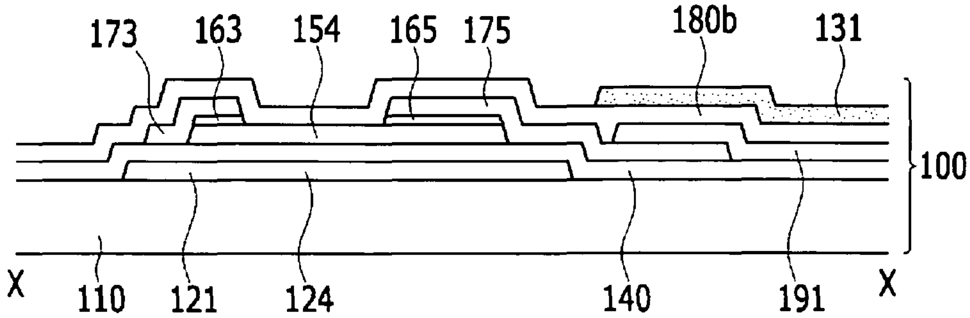


FIG. 11

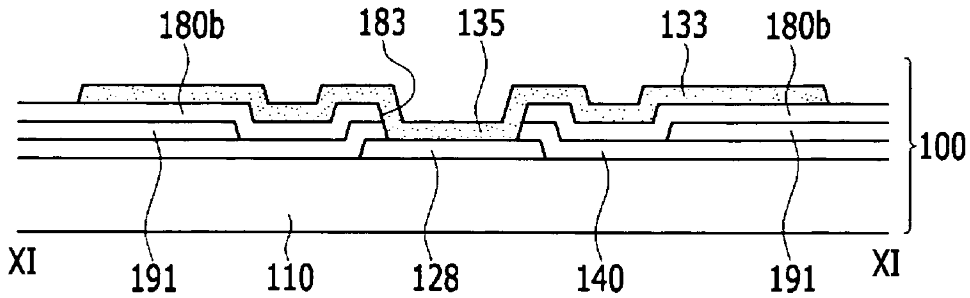
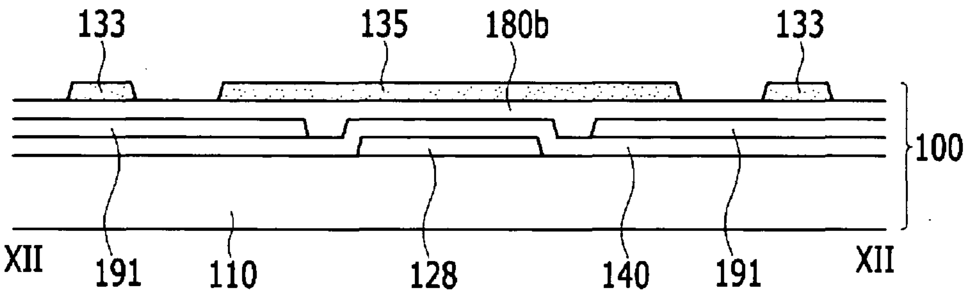


FIG. 12



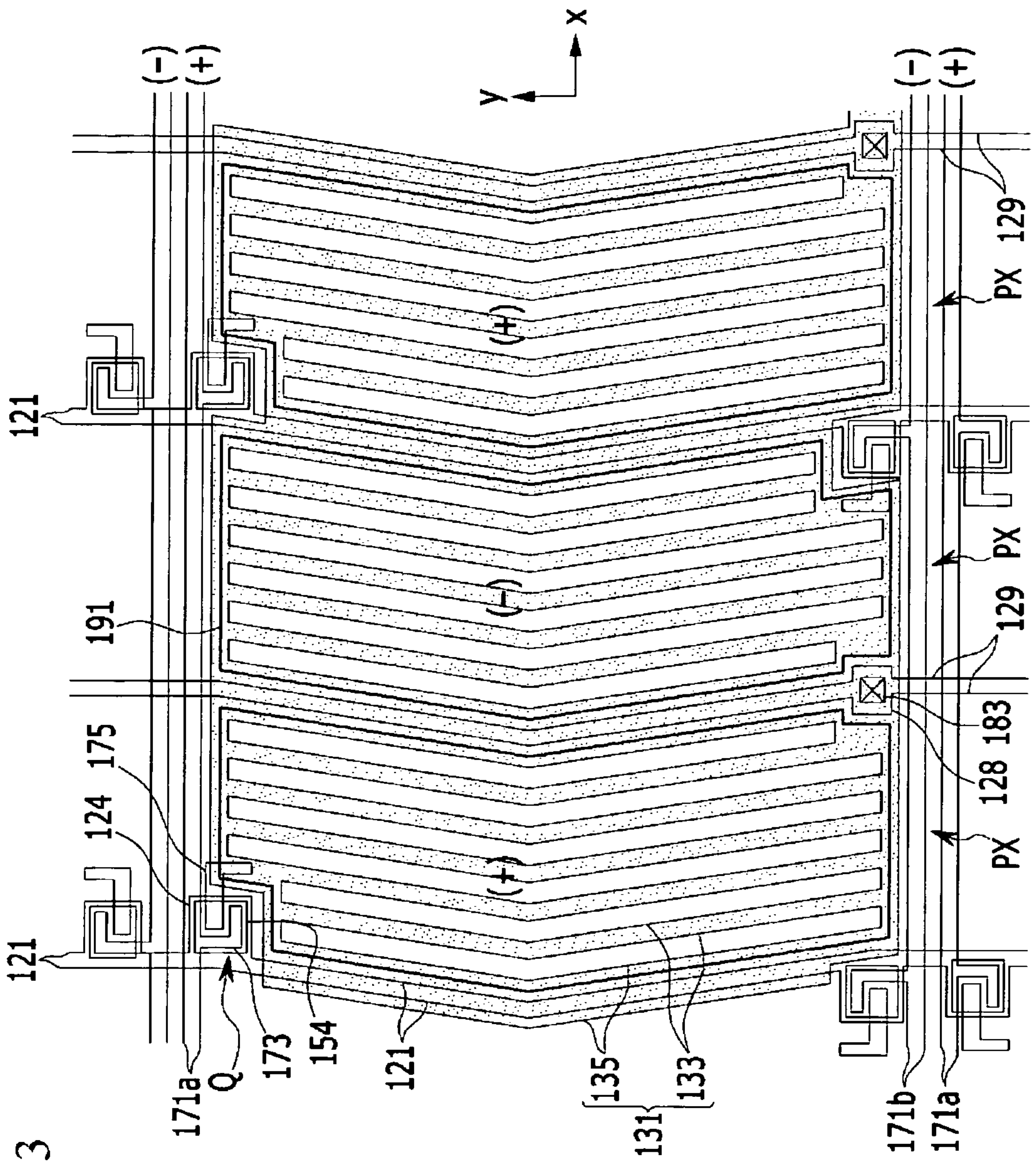
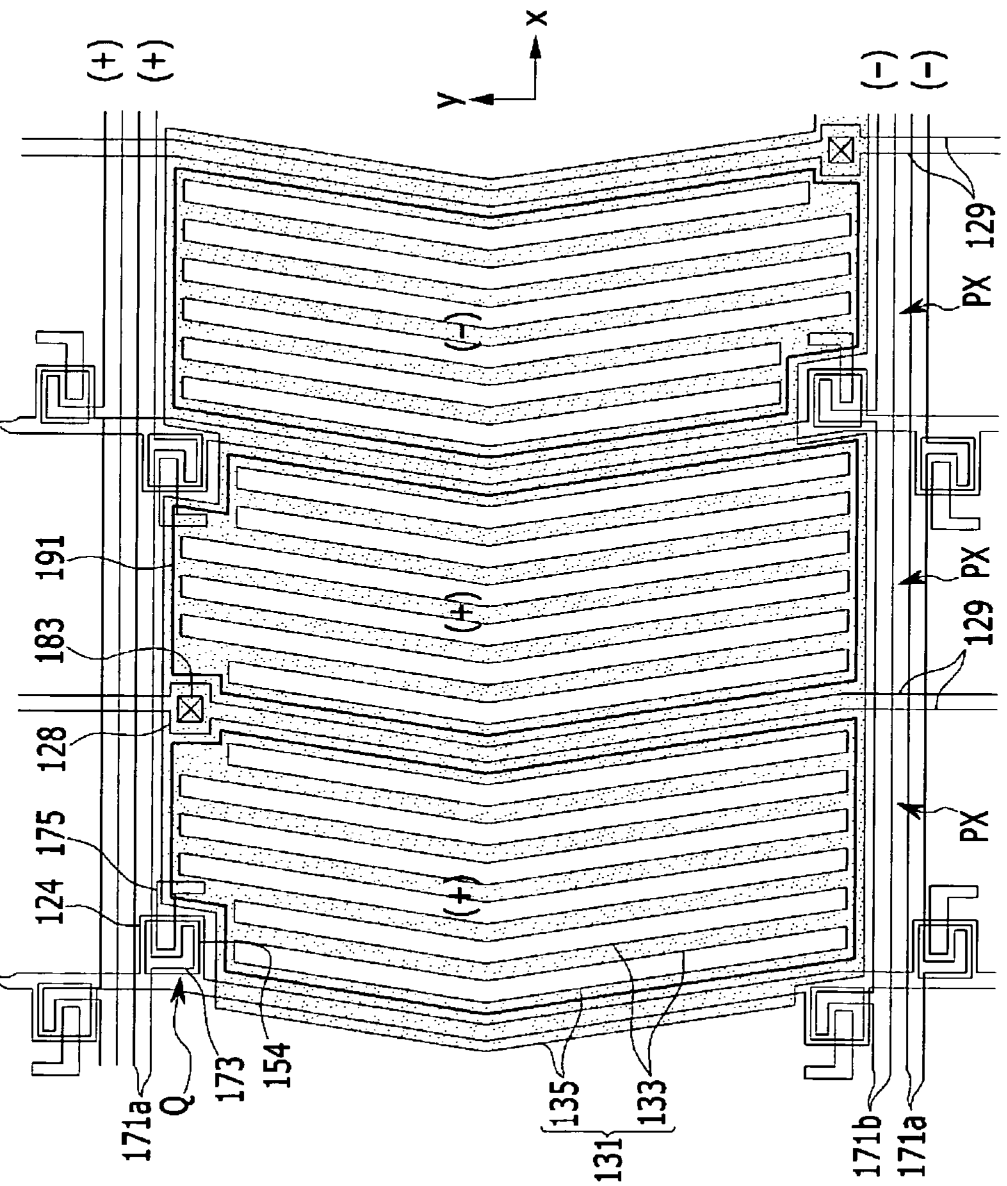


FIG. 13

FIG. 14


(+)
(+)
(-)
(-)
x
y
121
191
183
128
175
124
121
171a
Q
173
154
135
133
131
171b
171a
129
PX
PX
129
PX
(-)
(+)
(+)

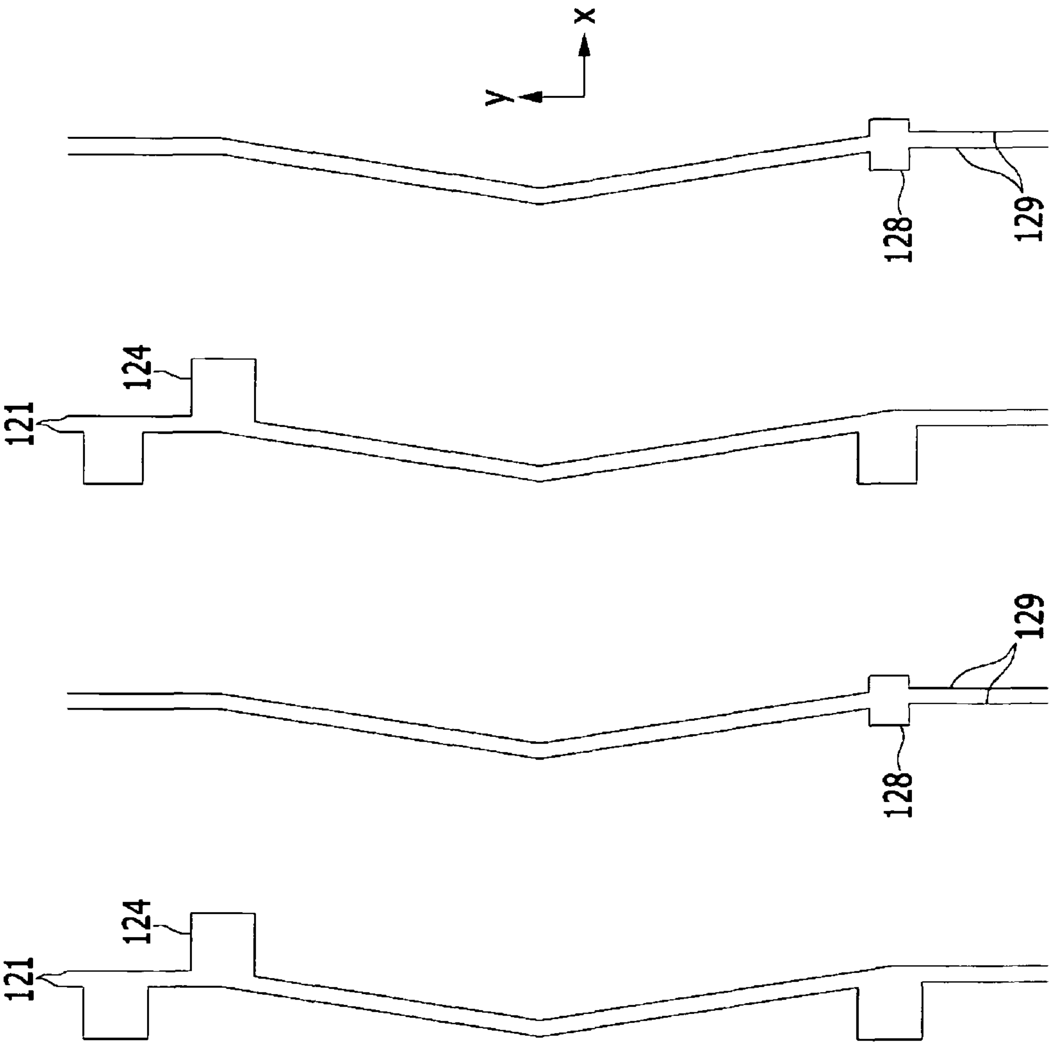


FIG. 15

FIG. 16

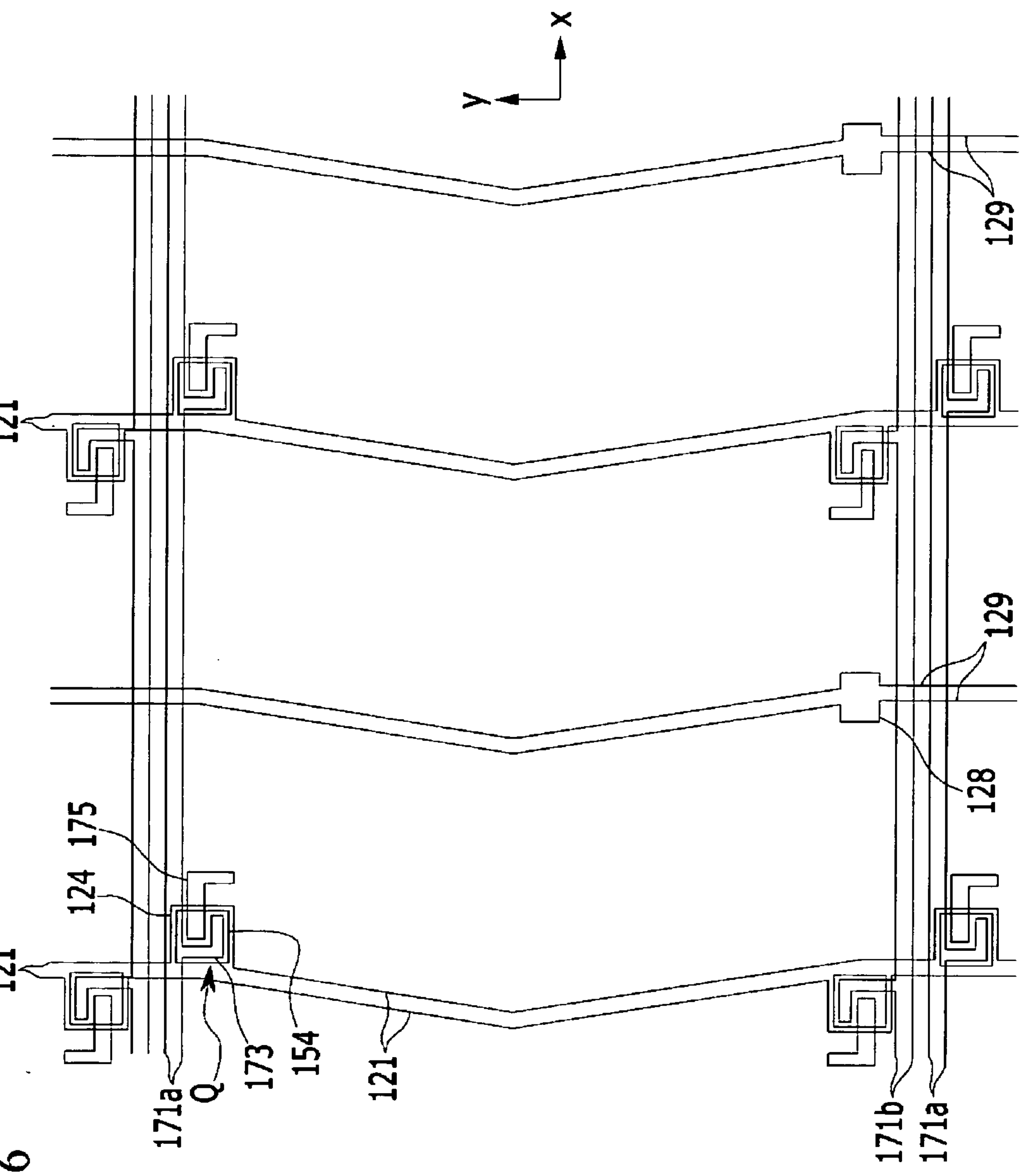


FIG. 17

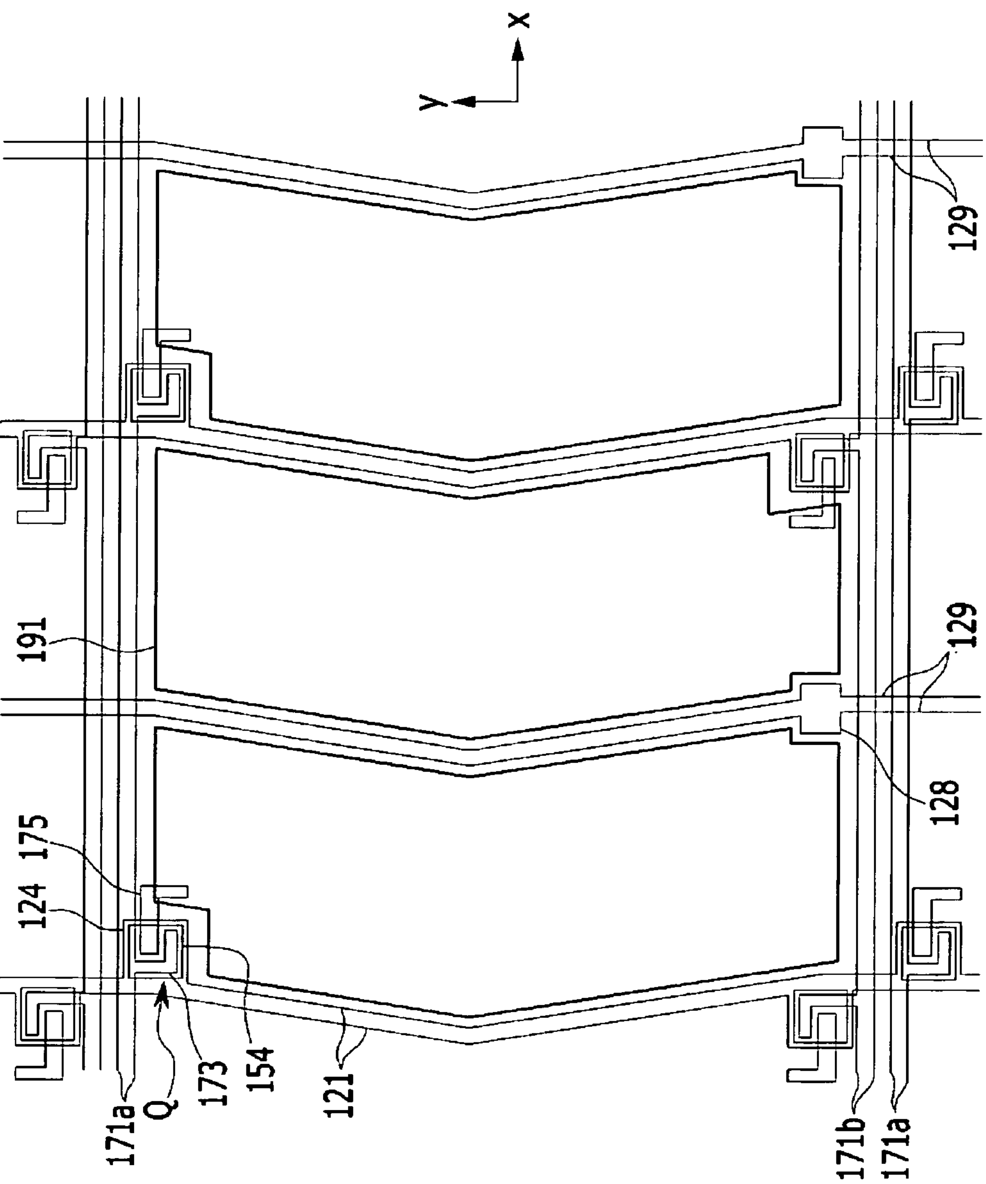
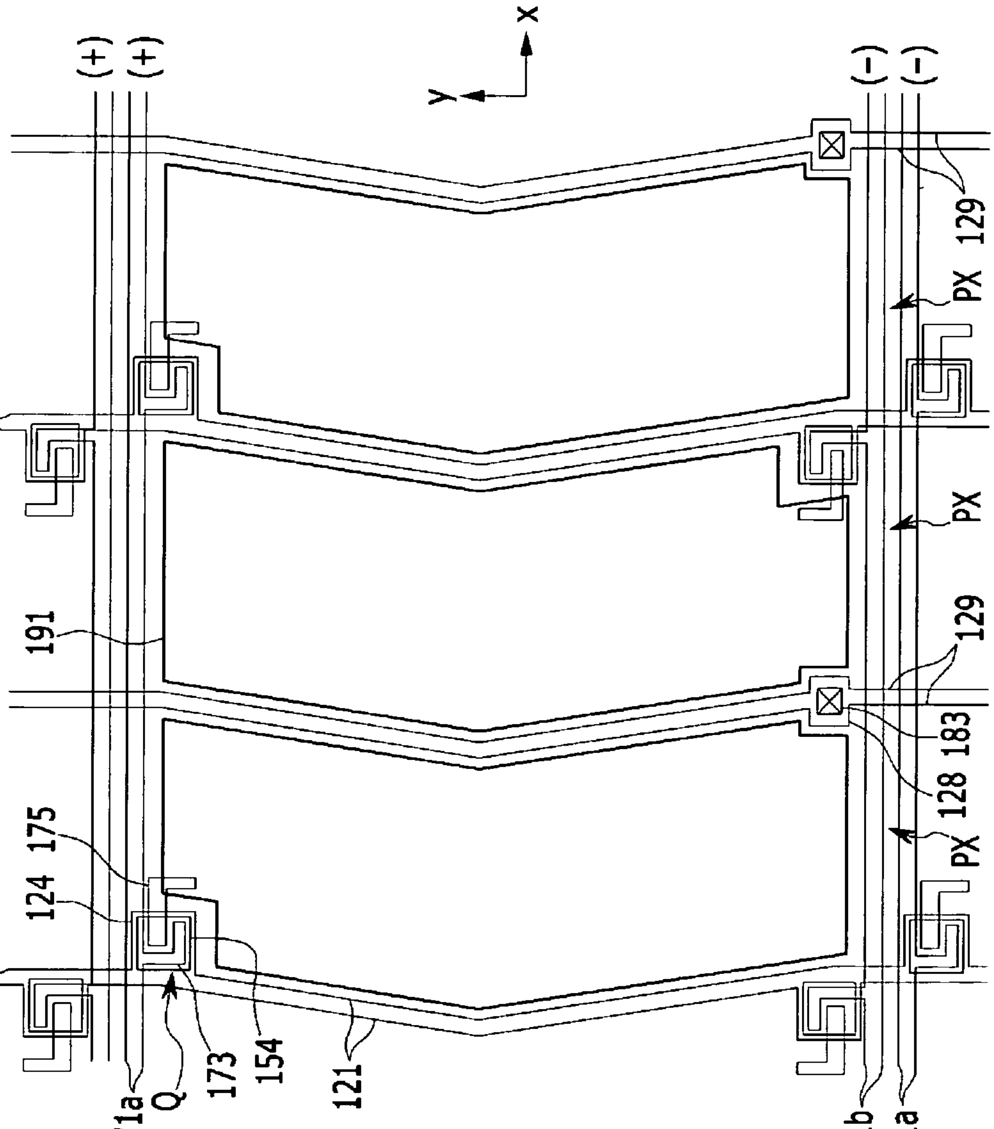


FIG. 18



(+)
(+)
X
Y
(-)
(-)
121
191
124
175
121
171a
Q
173
154
121
129
PX
PX
129
183
128
PX
171b
171a

FIG. 19

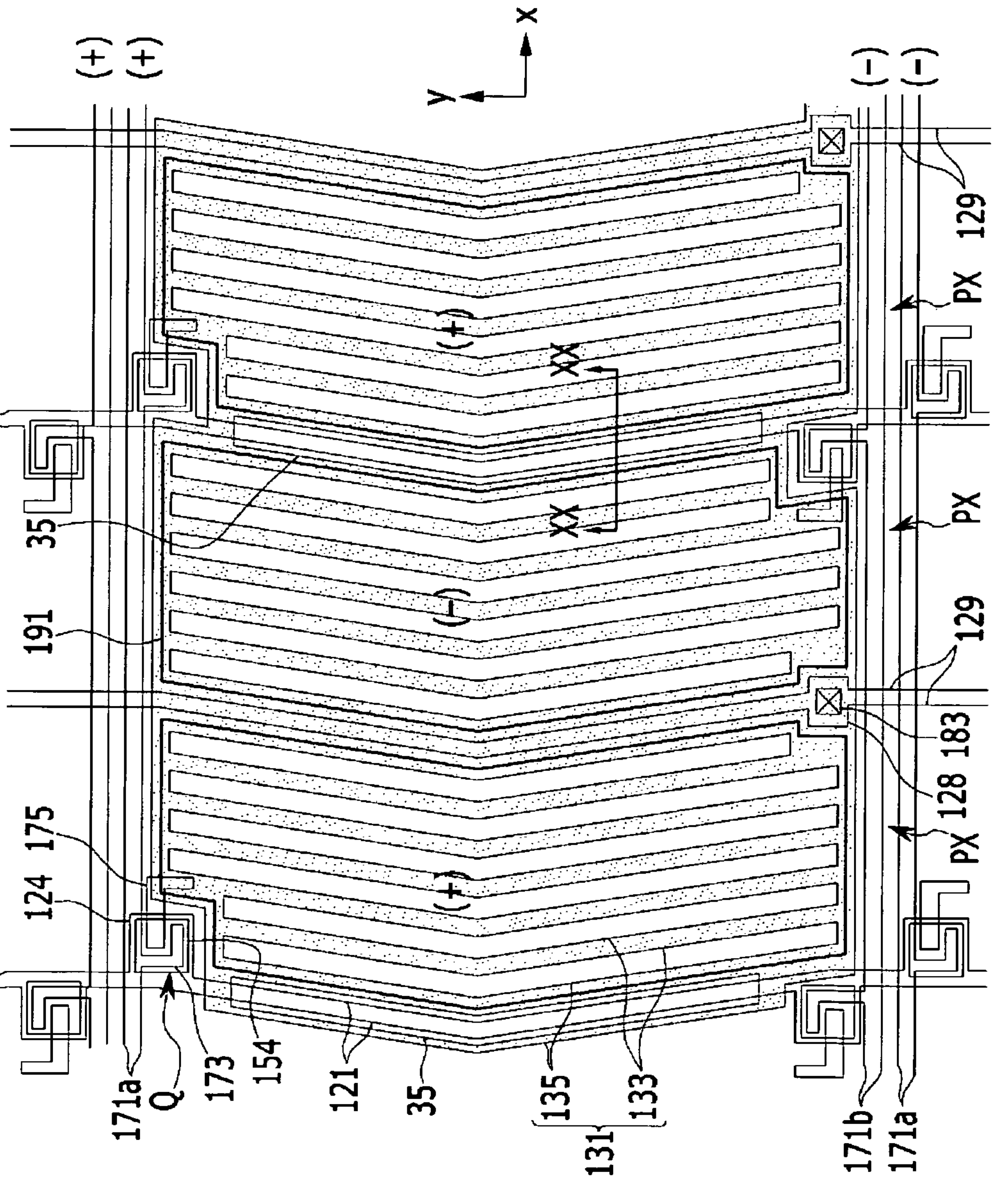
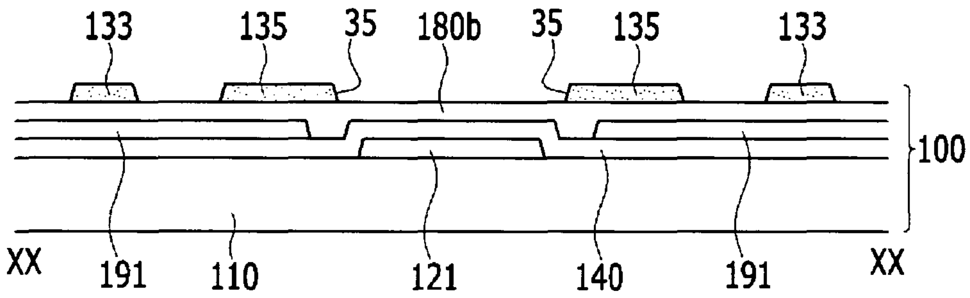

x
y
(+)
(+)
(-)
(-)
121
35
191
124
175
121
171a
Q
173
154
121
35
135
133
131
171b
171a
XX
XX
(+)
(-)
(+)
PX
PX
PX
129
129
183
128

FIG. 20



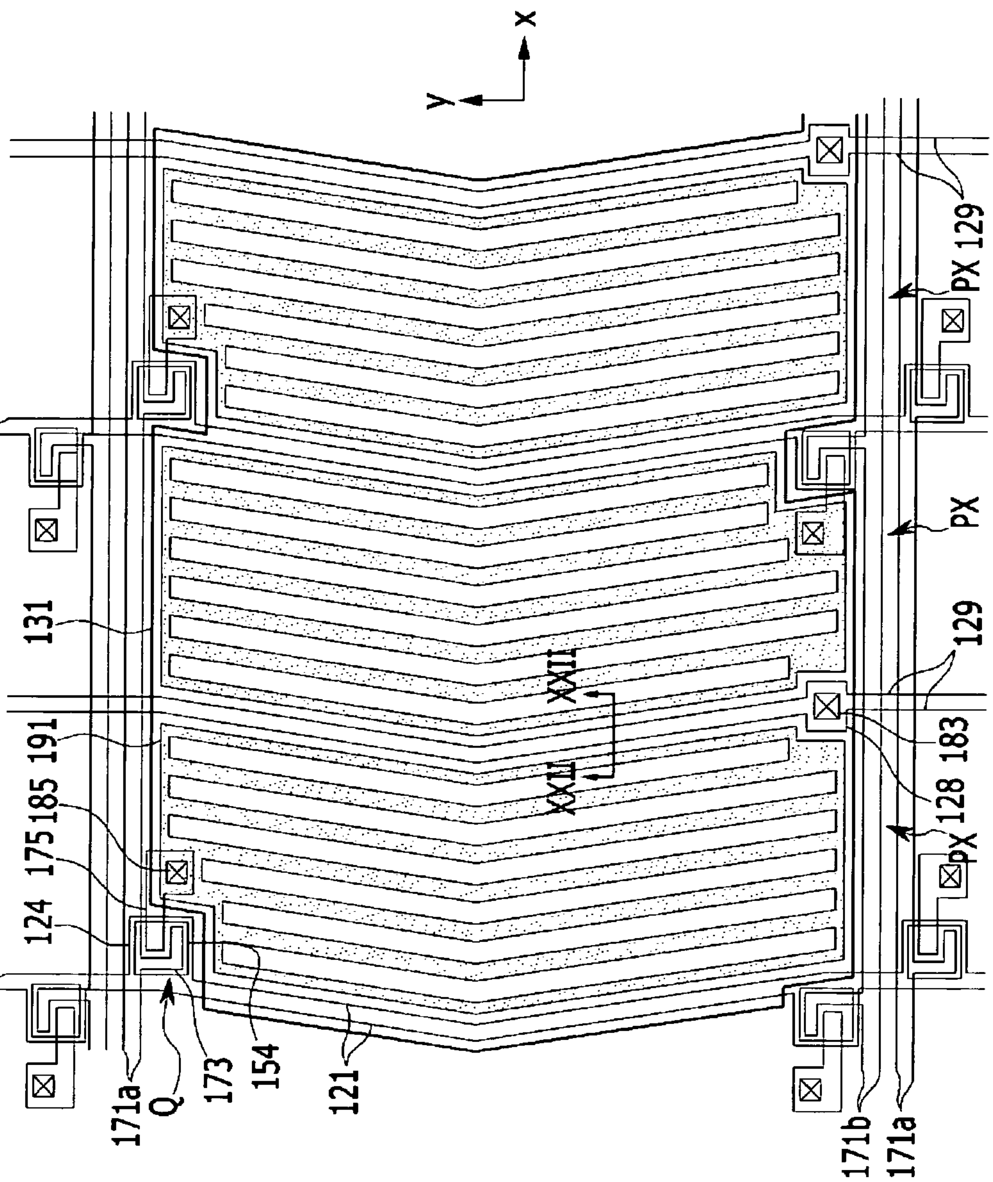
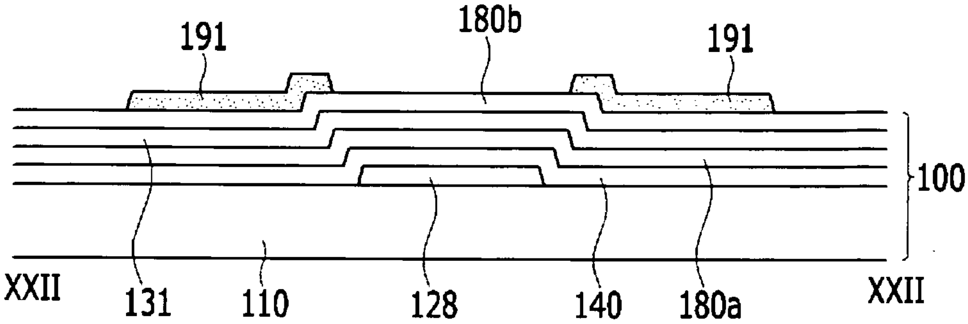

x
y
121
131
191
185
175
124
121
171a
Q
173
154
121
XXII
XXII
PX 129
PX
129
183
128
PX
171b
171a

FIG. 21

FIG. 22



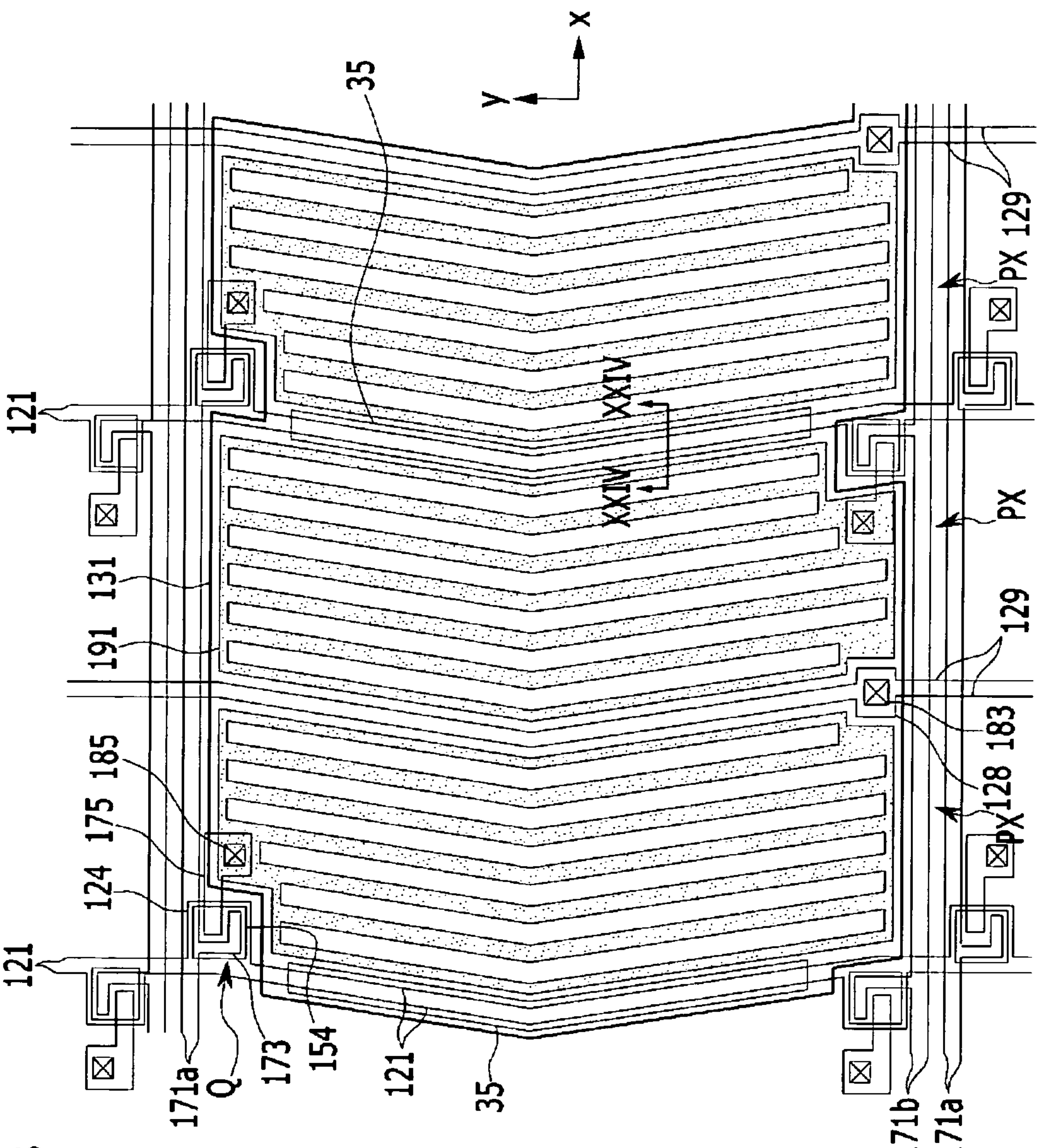

x
y
35
121
XXIV
XXIV
131
191
185
175
124
121
171a
Q
173
154
121
35
129
PX 129
PX
129
183
128
PX
171b
171a

FIG. 23

FIG. 24

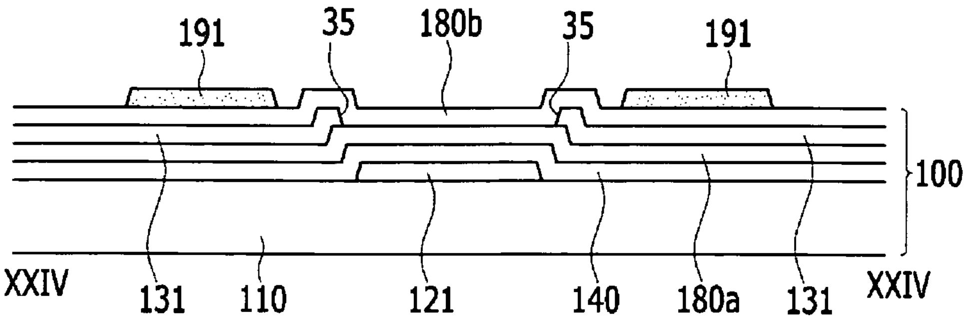


FIG. 25

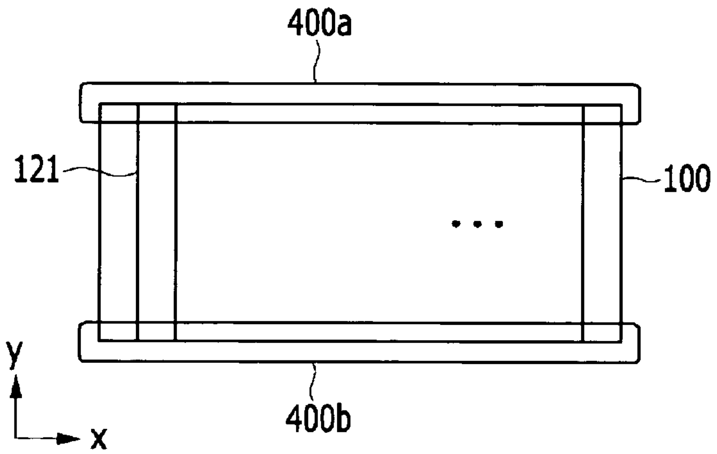


FIG. 26

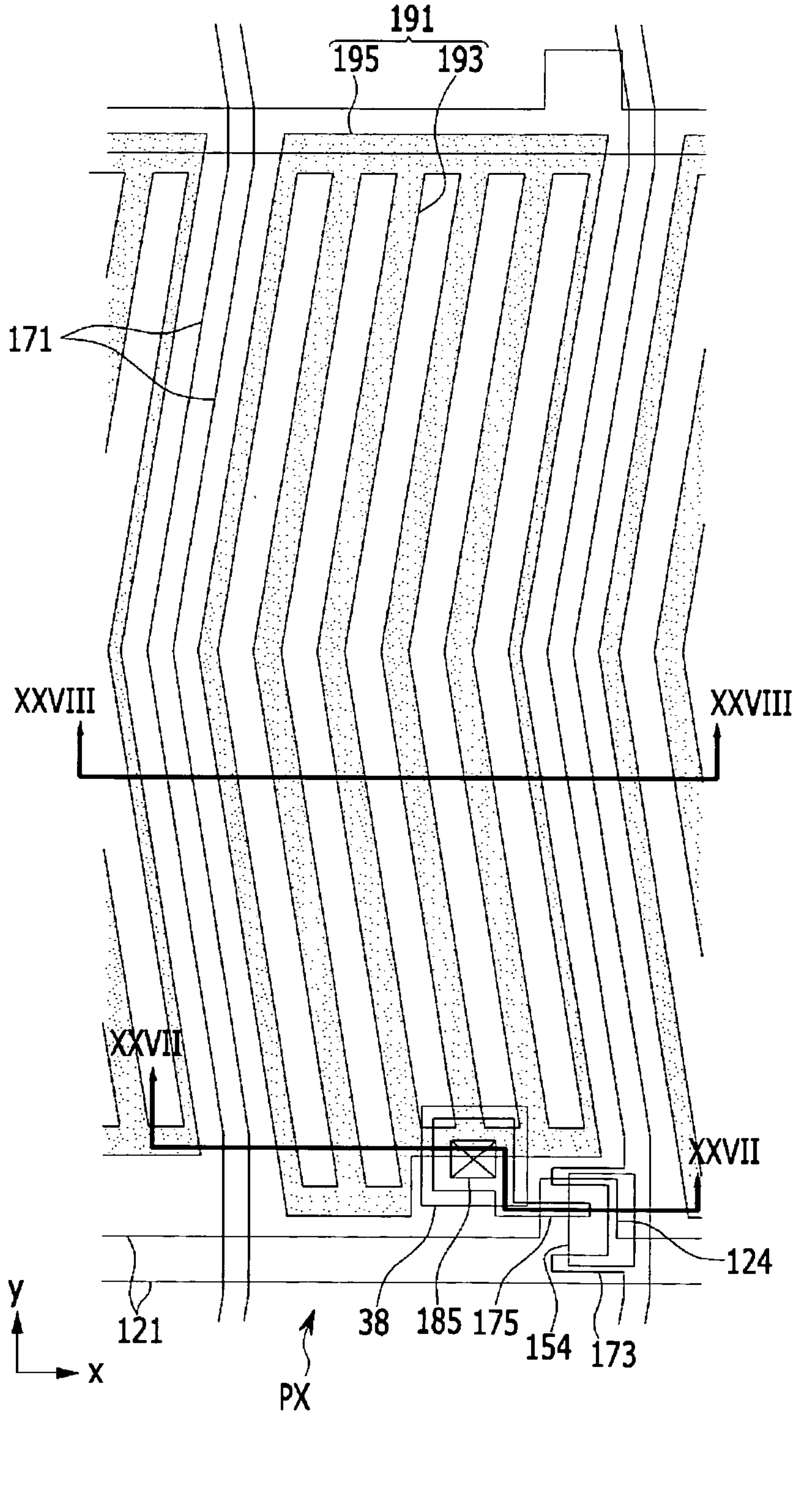

191
195
193
171
XXVIII
XXVIII
XXVII
XXVII
124
y
x
121
PX
38
185
175
154
173

FIG. 27

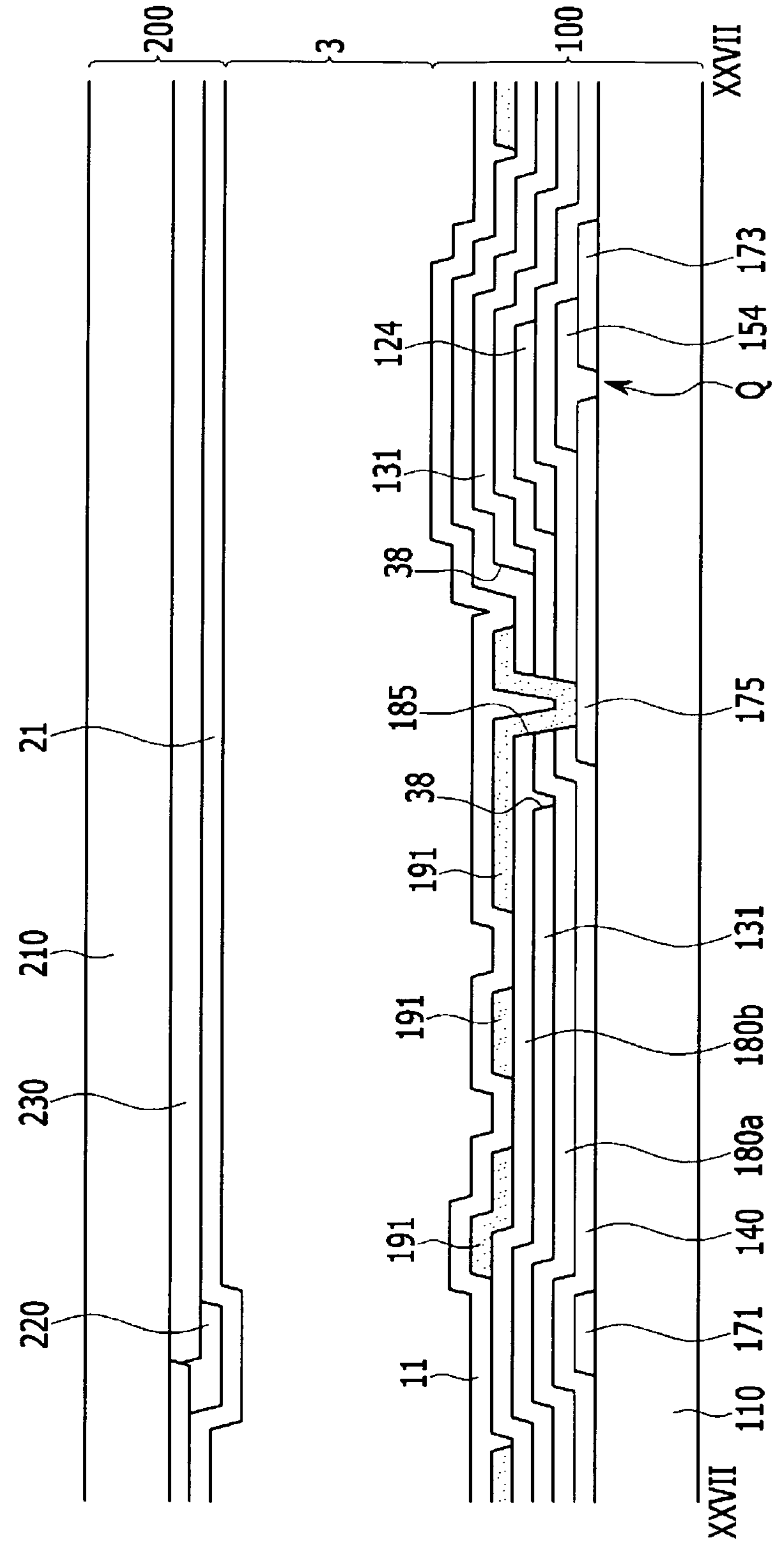

200
3
100
XXVII
21
210
230
220
11
191
185
191
191
38
38
131
124
173
154
Q
175
131
180b
180a
140
171
110
XXVII

FIG. 28

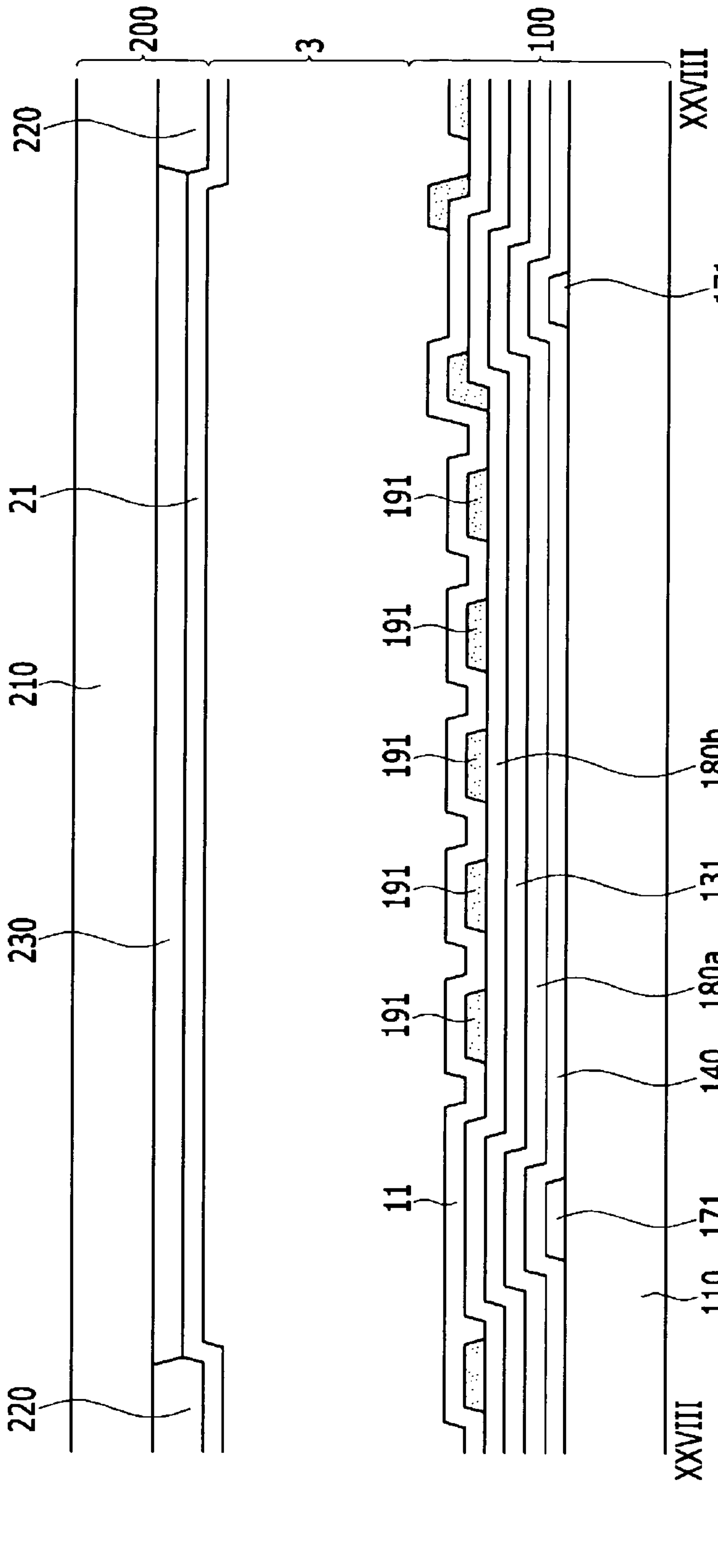

200
3
100
220
21
210
230
220
191
191
191
191
191
11
171
171
180b
131
180a
140
110
XXVIII
XXVIII

FIG. 29

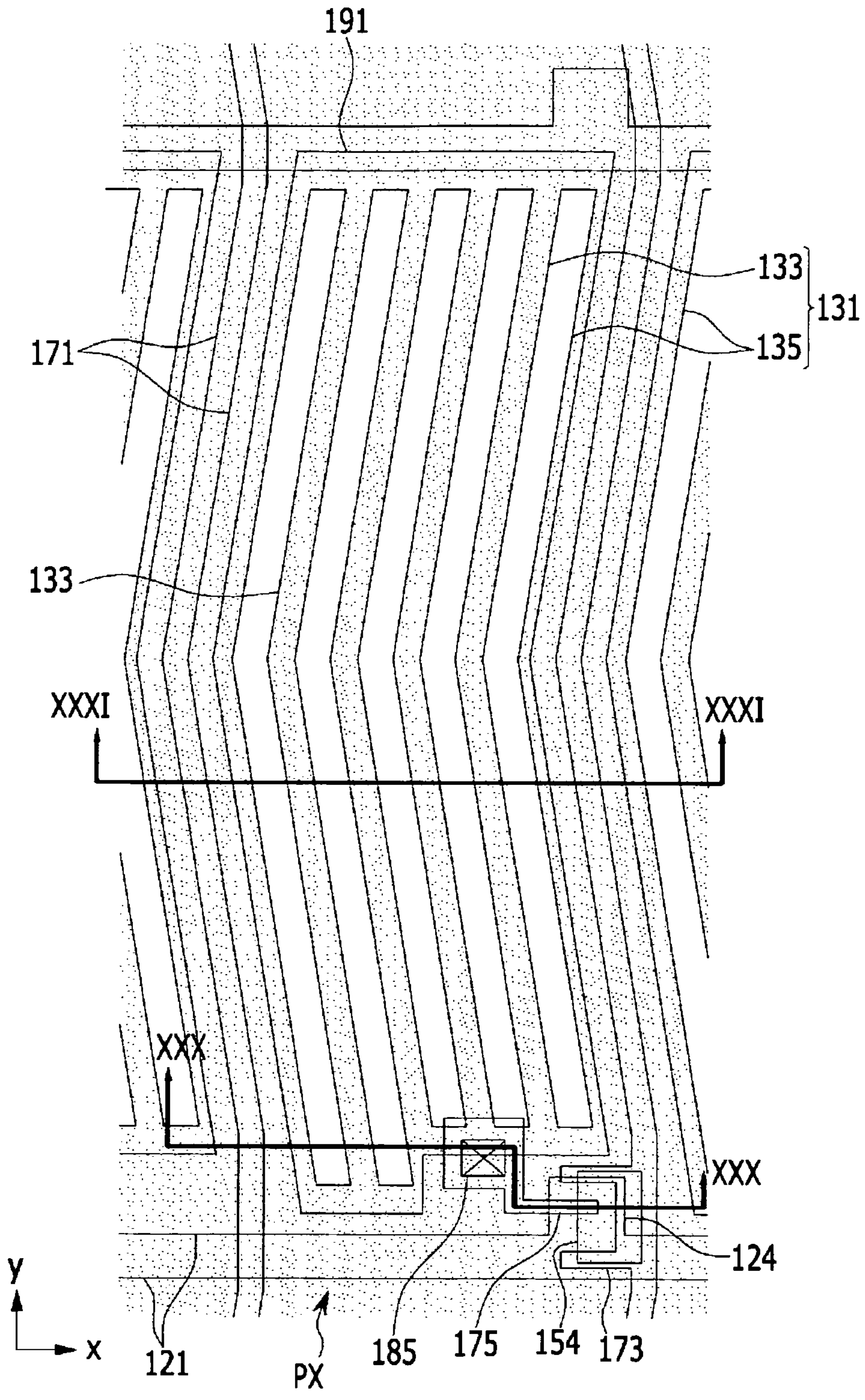

191
133
131
135
171
133
XXXI
XXXI
XXX
XXX
124
y
x
121
PX
185
175
154
173

FIG. 30

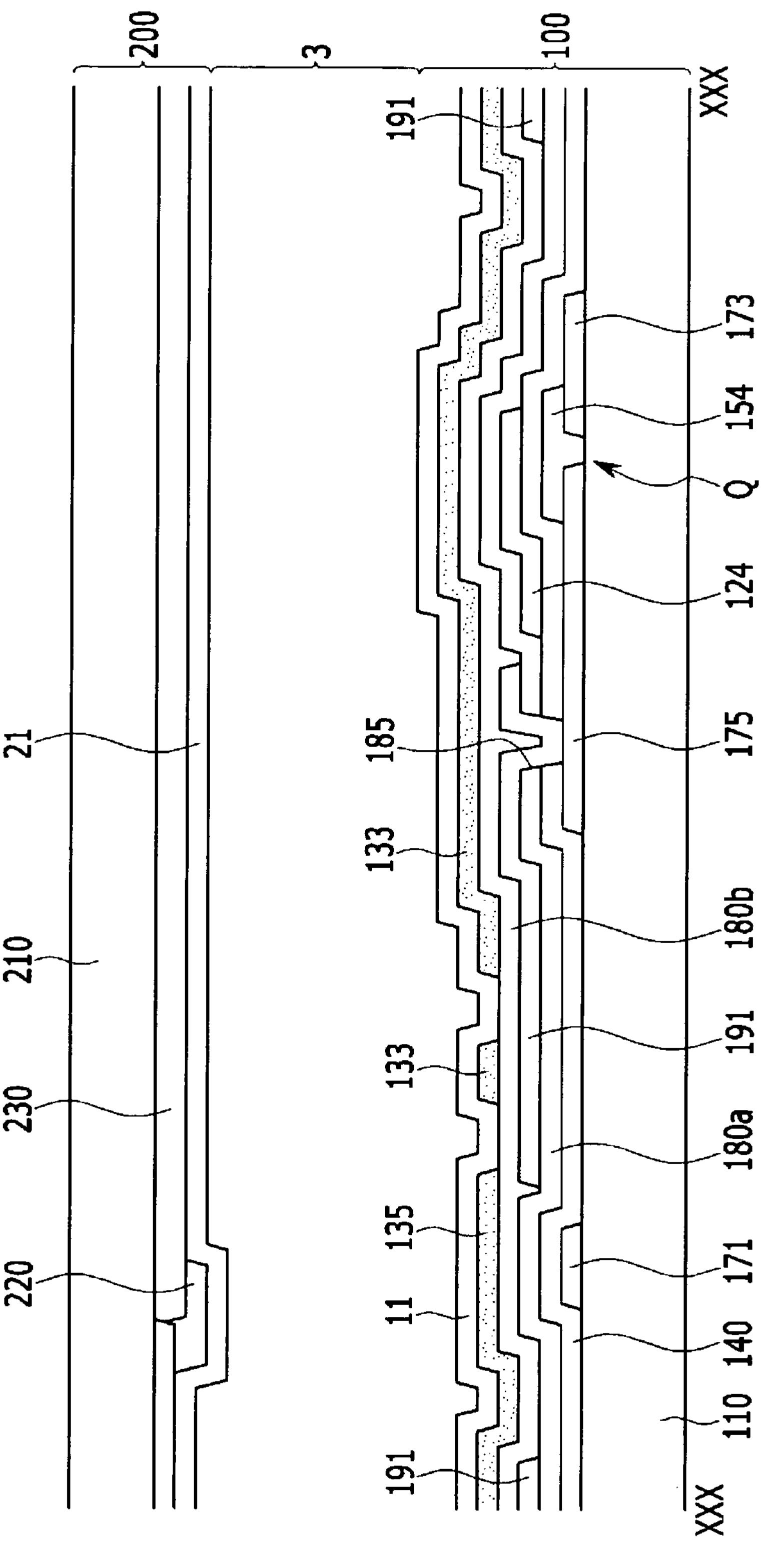
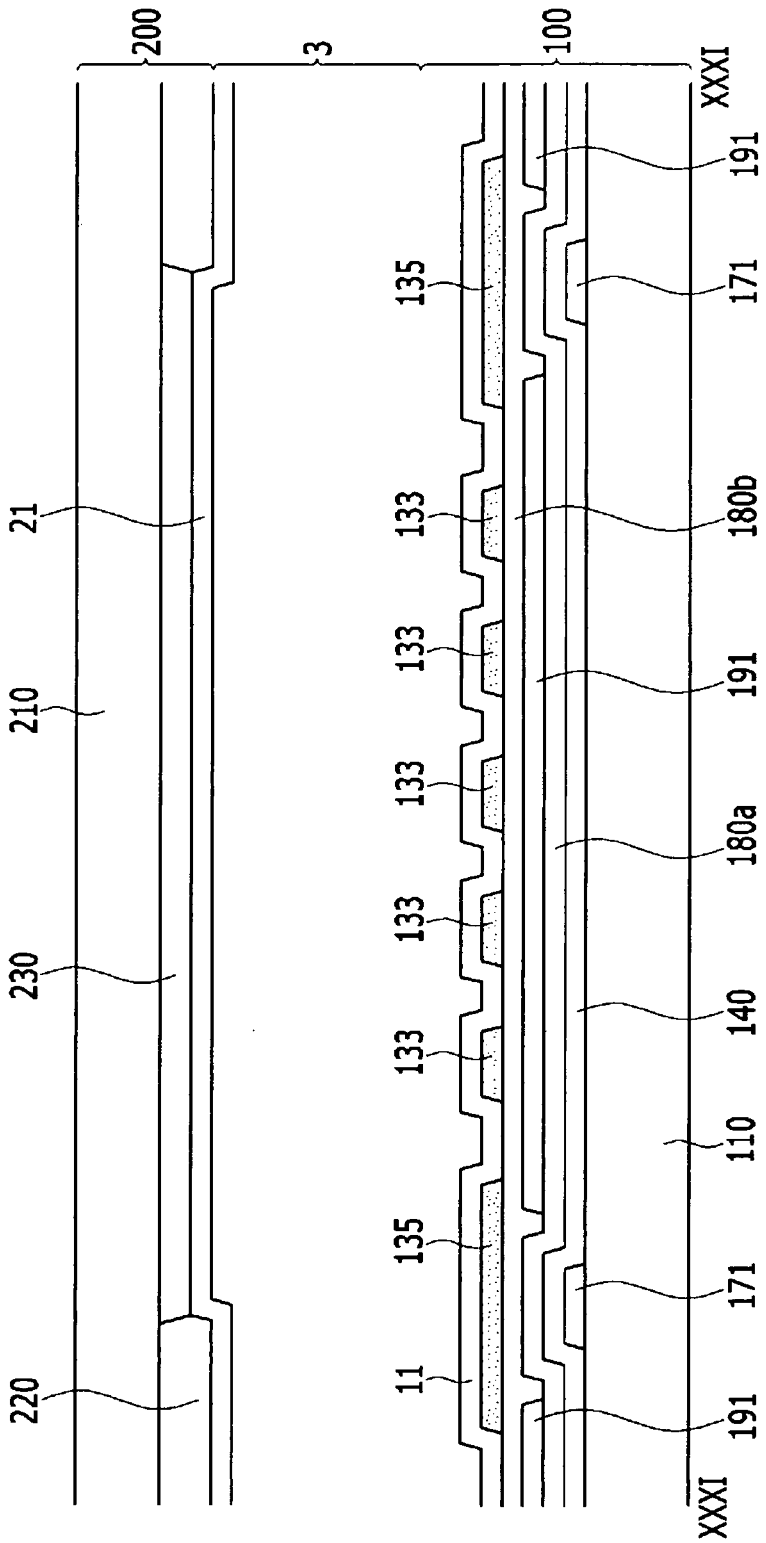

200
3
100
XXX
210
21
230
220
191
185
133
133
135
11
191
173
154
Q
124
175
180b
191
180a
171
140
110
XXX

FIG. 31


200
3
100
XXXI
191
171
135
133
180b
133
191
133
180a
133
140
133
110
135
171
11
191
XXXI
21
210
230
220

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- EP 2472310 A **[0006]**

patsnap

专利名称(译)	液晶显示器		
公开(公告)号	EP2765452B1	公开(公告)日	2015-03-11
申请号	EP2014154271	申请日	2014-02-07
[标]申请(专利权)人(译)	三星显示有限公司		
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IPC分类号	G02F1/1343		
CPC分类号	G02F1/134363 G02F2001/134318 G02F2001/134372 G02F1/13306 G02F1/133345 G02F1/1343 G02F1/134309 G02F1/13439 G02F1/136286 G02F1/1368 G02F2001/136272 G02F2201/121 H01L27/1225 H01L27/124 H01L29/7869		
代理机构(译)	DR.威猛和合作伙伴		
优先权	1020130014968 2013-02-12 KR		
其他公开文献	EP2765452A1		
外部链接	Espacenet		

摘要(译)

一种液晶显示装置，包括基板（110）;第一信号线（SL1）设置在基板（110）上并沿y方向延伸;栅极绝缘层（140）设置在第一信号线（SL1）上;第一电极（173,175）设置在栅极绝缘层（140）上;薄膜晶体管（Q）连接到第一信号线（SL1）之一并包括栅极绝缘层（140）和第一电极（173,175）;像素电极（191），其在y方向上延伸，连接到薄膜晶体管（Q），并被配置为从薄膜晶体管（Q）接收数据电压;公共电极（131,133,135）与至少一个重叠像素电极（191）的一部分;第一绝缘层（180b）设置在像素电极（191）和公共电极（131,133,135）之间。像素电极（191）或公共电极（131,133,135）具有平面形状，另一个包括与平面形状重叠并且基本上平行于第一信号线（SL1）延伸的分支电极。公共电极（131,133,135）的至少一部分与第一信号线（SL1）的至少一部分重叠。由于栅极绝缘层（140）设置在第一信号线（SL1）上，因此第一信号线（SL1）和公共电极之间的寄生电容可以是降低。

FIG. 1