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(54) **DRIVING METHOD FOR COMMON ELECTRODES, CIRCUIT AND LIQUID CRYSTAL DISPLAY THEREOF**

(57) A driving method for common electrodes includes: generating a first common electrode signal applied to the storage electrode line of each line pixel on an array substrate and a second common electrode signal applied to the common electrode, which forms liquid crystal capacitance with the pixel electrode of each line pixel on the array substrate. The jumping sequence of the first common electrode signal is the inverse of the jumping sequence of gate electrode signal applied to the gate electrode of corresponding line pixel. The method also includes inputting the first common electrode signal to each line pixel and inputting the second common electrode signal to the said common electrode.

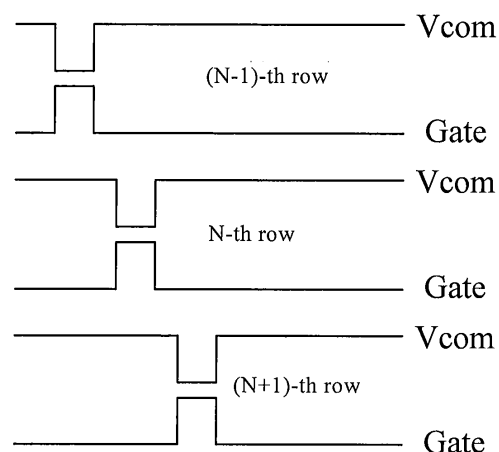


FIG.2

EP 2 560 156 A1

Description

TECHNICAL FIELD

5 **[0001]** The present invention relates to a common electrode driving method, a common electrode driving circuit and a liquid crystal display.

BACKGROUND

10 **[0002]** A liquid crystal display is a display of flat panel type commonly used at present, of which a thin film transistor liquid crystal display (TFT-LCD) has become a mainstream product.

[0003] In related arts, the liquid crystal display includes an array substrate and a color-filter substrate, in which the array substrate comprises a plurality of pixels arranged thereon in a matrix form, and each of the pixels includes a pixel electrode and a thin film transistor (TFT) connected to the pixel electrode as a switching element. With a common electrode located on the array substrate or on the color-filter substrate, the pixel electrode forms a liquid crystal capacitance, which applies electrical field to liquid crystal material. In addition, the pixel electrode may form a storage capacitance with a storage electrode formed on the array substrate so as to supplement the liquid crystal capacitance.

[0004] Fig. 1 is a schematic diagram for equivalent circuit of a unit pixel of the liquid crystal display in related arts. As shown in Fig. 1, when a TFT-LCD is in operation, on the array substrate, the gate ON voltage is firstly applied to a gate electrode g connected to gate line Gn and the TFT is switched on, thus a data voltage on a data line Dm for displaying an image signal is applied to the drain electrode d through the source electrode s. The drain electrode d is connected to a pixel electrode p, and the above data voltage is applied to the pixel electrode p through the drain electrode d so that a pixel electrode voltage is formed, where Cn is a storage electrode line. On the color-filter substrate, there is disposed a common electrode layer, and a voltage difference between the pixel electrode voltage on the pixel electrode p and the common electrode voltage V0 on the common electrode layer gives rise to a liquid crystal capacitance Clc, which is applied to liquid crystal molecules to make liquid crystal molecules orientated. Since a parasitic capacitance Cgd is formed between the gate electrode g and the drain electrode d, a sharp fluctuation in voltage when the gate line Gn is turned on and off is applied to the pixel electrode p with this parasitic capacitance Cgd, so that a kickback voltage ΔV_p is generated on the pixel electrode voltage, thus accuracy of the pixel electrode voltage is influenced and a screen flicker is caused.

SUMMARY

35 **[0005]** In an embodiment of the invention, there is provided a common electrode driving method, comprising: generating a first common electrode signal to be applied to a storage electrode line of each row of pixels on an array substrate, and a second common electrode signal to be applied to a common electrode forming a liquid crystal capacitance with pixel electrodes of each row of pixels on the array substrate, the first common electrode signal being opposite to a gate signal applied to the corresponding row of pixels in terms of transition timing; and inputting the first common electrode signal to each row of pixels, and inputting the second common electrode signal to the common electrode.

40 **[0006]** In another embodiment of the invention, there is provided a common electrode driving circuit, comprising: a driving signal generation circuit for generating a first common electrode signal to be applied to a storage electrode line of each row of pixels on an array substrate, and a second common electrode signal to be applied to a common electrode forming a liquid crystal capacitance with pixel electrodes of each row of pixels on the array substrate, the first common electrode signal being opposite to a gate signal applied to the corresponding row of pixels in terms of transition timing; and a common electrode signal output terminal for inputting the first common electrode signal to each row of pixels, and inputting the second common electrode signal to the common electrode.

45 **[0007]** In a further embodiment of the invention, there is provided a liquid crystal display, comprising: a liquid crystal panel; and a driver for driving the liquid crystal panel, wherein the liquid crystal panel is made by assembling an array substrate and a color-filter substrate with a liquid crystal layer filled therebetween, the driver comprising a gate driver, a data driver and a common electrode driver; wherein the common electrode driver is used for generating a first common electrode signal to be applied to a storage electrode line of each row of pixels on the array substrate, and a second common electrode signal to be applied to a common electrode forming a liquid crystal capacitance with pixel electrodes of each row of pixels on the array substrate, and inputting the generated first common electrode signal to each row of pixels respectively and inputting the generated second common electrode signal to the common electrode; and wherein the first common electrode signal is opposite to a gate signal applied to the corresponding row of pixels in terms of transition timing.

BRIEF DESCRIPTION OF THE DRAWINGS

- [0008]** Fig. 1 is a schematic diagram for equivalent circuit of a unit pixel of the liquid crystal display in related arts;
- [0009]** Fig. 2 is a timing chart for a relationship between the first common electrode signal and the gate signal in a first embodiment of common electrode driving method according to the invention;
- [0010]** Fig. 3 is a structural diagram of the first embodiment of common electrode driving circuit according to the invention;
- [0011]** Fig. 4 is a structural diagram of a fourth embodiment of common electrode driving circuit according to the invention; and
- [0012]** Fig. 5 is a structural diagram of a first embodiment of a liquid crystal display according to the invention.

DETAILED DESCRIPTION

[0013] To make objectives, technical solutions and advantages provided by embodiments of present invention more clearly, a clear and full description will be made to the technical solutions of embodiments of present invention hereinafter in connection with the accompanying drawings of present embodiments. Apparently, rather than all the embodiments, embodiments to be described is only a part of embodiments of present invention. Based on the embodiments of present invention, all the other embodiments acquired by those skilled in the art without making creative work belong to the scope claimed by present invention.

[0014] A first embodiment of common electrode driving method according to the invention comprises steps as follows.

[0015] In step 201, a first common electrode signal for rows of pixels on an array substrate and a second common electrode signal on a color-filter substrate are generated, the first common electrode signal being opposite to a gate signal for a corresponding row of pixels in terms of transition timing, and absolute value of charge change amount in the storage capacitance due to the transition of the first common electrode signal being equal to that of charge change amount in a parasitic capacitance due to the transition of the gate signal but change directions of them being opposite to each other. The first common electrode signal is applied to a storage electrode line on the array substrate forming a storage capacitance with a pixel electrode, and the storage electrode line can be also referred to as storage common electrode line to which a common electrode signal is applied.

[0016] The origination for generation of the kickback voltage ΔV_p on the pixel electrode lies in existence of the parasitic capacitance C_{gd} which is caused from the overlap between the gate electrode of TFT as a switching element of pixel and the drain electrode thereof. When an OFF voltage is inputted to the gate line, the amount of the charges Q_{gd} stored in the parasitic capacitance C_{gd} is changed, and at this moment, since the sum of charges stored in liquid crystal capacitance C_{lc} formed by the pixel electrode and the common electrode therebetween, storage capacitance C_{st} formed in the overlap between the pixel electrode and the storage electrode line, and the parasitic capacitance C_{gd} is in conservation, a change in the charges Q_{gd} stored in the parasitic capacitance C_{gd} causes a change in charge distribution on the overall pixel electrode, and voltage applied to the pixel electrode is changed and a kickback voltage ΔV_p is generated on the pixel electrode. A research shows an expression of kickback voltage $\Delta V_p = C_{gd}(V_{gh} - V_{gl}) / (C_{gd} + C_{lc} + C_{st})$, where V_{gh} is ON voltage of gate electrode, and V_{gl} is OFF voltage of gate electrode. The liquid crystal capacitance is used to drive the orientation of liquid crystal for displaying. Together with the pixel electrode, the common electrode can be formed on array substrate (that is, an LCD of horizontal electric field type, such as IPS or FFS-type LCD) or color-filter substrate which is disposed in opposite to the array substrate (that is, an LCD of vertical electric field type, such as TN-type LCD). In this embodiment, the common electrode is formed on the color-filter substrate, for example. The storage capacitance is used to supplement the liquid crystal capacitance, and enables the liquid crystal capacitance to be stably operated for displaying. The drain of the TFT, which is connected to the pixel electrode, transmits data signal on data line connected to the source of the TFT to the pixel electrode when the TFT is turned on. The TFT can be of a bottom-gate type, a top-gate type, or a combination of both, and the gate electrode and the source and drain electrodes are formed with a gate insulation layer and a semiconductor layer separated therebetween.

[0017] Fig. 2 is a timing chart for a relationship between the first common electrode signal and the gate signal in a first embodiment of common electrode driving method according to the invention. As shown in Fig. 2, the first common electrode signal V_{com} applied to the storage electrode line and the gate signal $Gate$ corresponding to a same row of pixels are opposite to each other in terms of transition timing; that is, when the gate signal is at a high level, the first common electrode signal is at a low level, and when the gate signal is at a low level, the first common electrode signal is at a high level. That is also to say, when the gate line is turned on, the storage electrode line is turned off, and when the gate line is turned off, the storage electrode line is turned on.

[0018] The inventors have conducted a deep analysis and study on mechanism of kickback voltage generated by the pixel electrode, and found that when the OFF voltage is applied to the gate line, the total amount of charges stored in the liquid crystal capacitance C_{lc} , the storage capacitance C_{st} and the parasitic capacitance C_{gd} before the TFT is turned off is same as the total amount thereof after the TFT is turned off.

[0019] Before the TFT is turned off, the charge amount stored in the parasitic capacitance Cgd can be expressed as

$$Q_{gd1} = C_{gd}(V_{p1} - V_{gh}),$$

after the TFT is turned off, the charge amount stored in the parasitic capacitance Cgd is expressed as

$$Q_{gd2} = C_{gd}(V_{p2} - V_{gl}),$$

thus a change of the charges stored in the parasitic capacitance Cgd upon turning off of the TFT, that is ΔQ_{gd} , is expressed as

$$\begin{aligned} \Delta Q_{gd} &= Q_{gd2} - Q_{gd1} \\ &= C_{gd}[(V_{p2} - V_{gl}) - (V_{p1} - V_{gh})] \end{aligned}$$

$$= C_{gd}(\Delta V_p + V_{gh} - V_{gl}),$$

where V_{p1} is the voltage of the pixel electrode immediately before the TFT is turned off, V_2 is the voltage of the pixel electrode immediately after the TFT is turned off, and $\Delta V_p = V_{p2} - V_{p1}$.

[0020] When an ON voltage is applied to the storage electrode line at this row, the amount of the charges stored in the storage capacitance Cst before it is turned on is expressed as

$$Q_{st1} = C_{st}(V_{p1} - V_{cl}),$$

the amount of the charges stored in the storage capacitance Cst after it is turned on is expressed as

$$Q_{st2} = C_{st}(V_{p2} - V_{ch}),$$

thus a change in the charges stored in the storage capacitance Cst upon turning on of the TFT, that is ΔQ_{gd} , is expressed as

$$\begin{aligned} \Delta Q_{st} &= Q_{st2} - Q_{st1} \\ &= C_{st}[(V_{p2} - V_{ch}) - (V_{p1} - V_{cl})] \\ &= C_{st}(\Delta V_p + V_{cl} - V_{ch}), \end{aligned}$$

where V_{ch} is a voltage with which the storage electrode line is turned on, and V_{cl} is a voltage with which the storage electrode line is turned off.

[0021] In this embodiment, since the transition timing for the first common electrode signal is opposite to that of the gate signal for the corresponding row of pixels, and absolute value of the charge change amount due to the transition of first common electrode signal in the storage capacitance is equal to that of charge change amount in a parasitic capacitance due to the transition of the gate signal but the change directions of them are opposite to each other, that is, the first common electrode signal generated in the this embodiment can enable a relation of $\Delta Q_{gd} = -\Delta Q_{st}$, and at the same time, the sum of the charges stored in the liquid crystal capacitance Clc, the storage capacitance Cst, and parasitic capacitance Cgd is in conservation, thus there is a relation of $\Delta Q_{lc} + \Delta Q_{gd} + \Delta Q_{st} = 0$, hence $\Delta Q_{lc} = 0$, where ΔQ_{lc} is the

charge change amount upon turning off of the gate, and $\Delta Q_{lc} = C_{lc}(V_{p2} - V_{p1})$. Since the liquid crystal capacitance C_{lc} is a constant, relations of $V_{p2} = V_{p1}$ and $\Delta V_p = V_{p2} - V_{p1} = 0$ stand. That is, there is no change occurred to the pixel voltage upon turning off of the gate. The reason thereof is that the change amount of the charges stored in the parasitic capacitance C_{gd} upon turning off of the TFT, that is, ΔQ_d , and the change amount of the charges stored in the storage capacitance C_{st} upon turning on of the storage electrode line are the same in magnitude and opposite to in change direction, thus total change of the charges stored in the two capacitance become zero, and changes in the charges stored in the two capacitances are offset with each other. Therefore, the change amount in the charges on the pixel electrode become zero, and hence a kickback voltage ΔV_p on the pixel electrode become zero. However, those skilled in the art can realize that, even if the change amount of the charges stored in the parasitic capacitance C_{gd} , that is ΔQ_d , is not completely the same as that of the charges stored in the storage capacitance C_{st} , that is ΔQ_{st} , this embodiment can also function to reduce kickback voltage ΔV_p on the pixel voltage upon turning off of the gate, thus display quality of the liquid crystal display is improved.

[0022] It should be noted that, in this embodiment, it is possible to superpose a transition timing signal on the basis of a constant common electrode signal to be inputted to the array substrate and the color-filter substrate generated by the related art, so as to generate a first common electrode signal to be inputted to the array substrate, while a second common electrode signal to be inputted to the color-filter substrate is still maintained as the original constant common electrode signal.

[0023] In step 202, the first common electrode signal is inputted to the rows of pixels, and the second common electrode signal is inputted to the color-filter substrate.

[0024] After generation of the first common electrode signal required by rows of pixels on the array substrate and the second common electrode signal on the color-filter substrate respectively, a driving circuit can correspondingly input the first common electrode signal to rows of pixels and input the second common electrode signal to the color-filter substrate. In this embodiment, the first common electrode signal generated in step 201 is inputted to the rows of pixels, so that kickback voltage ΔV_p will not be generated on the pixel electrodes. Thereby, accuracy of pixel electrode voltage is ensured and a screen flicker is avoided.

[0025] For this embodiment, with the transition timing of the first common electrode signal inputted to the rows of pixels being specified to be opposite to that of the gate signal for a corresponding row of pixels, and with the absolute value of the charge change amount in the storage capacitance due to the transition of first common electrode signal being equal to that of the charge change amount in the parasitic capacitance due to the transition of the gate signal but the change directions of them being opposite to each other, changes in the charges stored in the parasitic capacitance and storage capacitance are offset with each other and the charge change amount on the pixel electrode become zero, so that kickback voltage on the pixel electrode become zero. Thereby, accuracy of pixel electrode voltage is ensured and a screen flicker is avoided.

[0026] In a second embodiment of the common electrode driving method according to present invention, the storage capacitance C_{st} can be of a structure in which it is provided on the storage electrode line (C_{st} On Common). That is, the storage capacitance is formed by overlapping the pixel electrode with the storage electrode line. In addition, the common electrode, with which the pixel electrode forms a liquid crystal capacitance, is formed on the color-filter substrate disposed in opposite to the array substrate. The method of this embodiment can include steps as follows.

[0027] In step 401, the first common electrode signal for rows of pixels on an array substrate and the second common electrode signal on the color-filter substrate are generated, the first common electrode signal being opposite to the gate signal for a corresponding row of pixels in terms of transition timing, and a difference between the high level and the low level of the first common electrode signal being equal to $[C_{gd} \cdot (V_{gh} - V_{gl})] / C_{st}$, where C_{gd} is the capacity value of the parasitic capacitance, C_{st} is the capacity value of the storage capacitance, and V_{gh} and V_{gl} are an ON voltage and an OFF voltage of the gate electrode, respectively.

[0028] In this embodiment, in order to make the charge change amount in the storage capacitance due to the transition of the first common electrode signal equal to the charge change amount in the parasitic capacitance due to the transition of gate line, a difference between the high level and the low level of the first common electrode signal is specified to be equal to $[C_{gd} \cdot (V_{gh} - V_{gl})] / C_{st}$.

[0029] Specifically, upon turning off of the gate signal, that is, upon transition of the storage electrode line, a sum of charges stored in the liquid crystal capacitance C_{lc} , the storage capacitance C_{st} and the parasitic capacitance C_{gd} is in conservation, that is $Q_{p1} = Q_{p2}$, where Q_{p1} is a sum of charges stored in these three capacitances before the transition of the gate signal, and Q_{p2} is a sum of charges stored in these three capacitances after the transition of the gate signal.

[0030] Here,

$$\begin{aligned}
 Q_{p1} &= Q_{lc1} + Q_{st1} + Q_{gd1} \\
 &= C_{lc} (V_{p1} - V_0) + C_{st} (V_{p1} - V_{cl}) + C_{gd} (V_{p1} - V_{gh});
 \end{aligned}$$

$$\begin{aligned}
 Q_{p2} &= Q_{lc2} + Q_{st2} + Q_{gd2} \\
 &= C_{lc} (V_{p2} - V_0) + C_{st} (V_{p2} - V_{ch}) + C_{gd} (V_{p2} - V_{gl});
 \end{aligned}$$

therefore,

$$\begin{aligned}
 C_{lc} (V_{p1} - V_0) + C_{st} (V_{p1} - V_{cl}) + C_{gd} (V_{p1} - V_{gh}) \\
 = C_{lc} (V_{p2} - V_0) + C_{st} (V_{p2} - V_{ch}) + C_{gd} (V_{p2} - V_{gl});
 \end{aligned}$$

that is,

$$C_{lc} (V_{p2} - V_{p1}) + C_{st} (V_{p2} - V_{p1} + V_{cl} - V_{ch}) + C_{gd} (V_{p2} - V_{p1} + V_{gh} - V_{gl}) = 0;$$

which also is,

$$(C_{lc} + C_{st} + C_{gd}) (V_{p2} - V_{p1}) + C_{st} (V_{cl} - V_{ch}) + C_{gd} (V_{gh} - V_{gl}) = 0;$$

for

$$(V_{ch} - V_{cl}) = C_{gd} (V_{gh} - V_{gl}) / C_{st};$$

$$(C_{lc} + C_{st} + C_{gd}) (V_{p2} - V_{p1}) = 0;$$

and for

$$(C_{lc} + C_{st} + C_{gd}) \neq 0;$$

$$V_{p2} - V_{p1} = 0, \text{ that is, } \Delta V_p = 0.$$

[0031] In step 402, the first common electrode signal is inputted to the rows of pixels, and the second common electrode signal is inputted to the color-filter substrate.

[0032] In this embodiment, the first common electrode signal generated in step 401 is inputted to the rows of pixels, so that the kickback voltage ΔV_p will not be generated on the pixel electrodes. Thereby, accuracy of pixel electrode voltage is ensured and a screen flicker is avoided.

[0033] In this embodiment, with the transition timing of the first common electrode signal inputted to the rows of pixels being specified to be opposite to that of the gate signal for a corresponding row of pixels, and a difference between the high level and the low level of the first common electrode signal being equal to $[C_{gd} (V_{gh} - V_{gl})] / C_{st}$, changes in the charges stored in parasitic capacitance and storage capacitance are offset with each other and the charge change

amount on the pixel electrode become zero, thus a kickback voltage on the pixel electrode become zero. Thereby, accuracy of pixel electrode voltage is ensured and a screen flicker is avoided.

[0034] In a third embodiment of common electrode driving method according to present invention, the storage capacitance Cst can be of a structure in which it is provided on the storage electrode line and the gate line (Cst On Common + Cst On Gate). That is, the storage capacitance is formed by overlapping the pixel electrode with both the storage electrode line and the gate line. The common electrode, with which the liquid crystal capacitance is formed, is formed on the color-filter substrate disposed in opposite to the array substrate. The method of this embodiment can include steps as follows.

[0035] In step 501, the first common electrode signal for the rows of pixels on an array substrate and the second common electrode signal on the color-filter substrate are generated, the first common electrode signal being opposite to the gate signal for a corresponding row of pixels in terms of transition timing, and a difference between the high level and the low level of the first common electrode signal being equal to $[C_{gd} \cdot (V_{gh} - V_{gl})] / C_{st1}$, where C_{gd} is the capacity value of the parasitic capacitance, C_{st1} is the capacity value of a part of the storage capacitance on the storage electrode line, and V_{gh} and V_{gl} are an ON voltage and an OFF voltage of the gate electrode, respectively.

[0036] For the case in which, between the pixel electrode and the storage electrode line as well as between the pixel electrode and the gate line, there are formed the storage capacitance Cst, the storage capacitance Cst can be divided into two parts of Cst1 and Cst2 in this embodiment, where Cst1 is a part formed by the storage electrode line, and Cst2 is a part formed by the gate line. Therefore, the capacitances which keep charges in conservation become liquid crystal capacitance C_{lc} , parasitic capacitance C_{gd} , and Cst1 and Cst2, of which dynamic signals applied by the storage electrode line only influences the part of Cst1. Therefore, the difference between this embodiment and the second embodiment of common electrode driving method according to present invention is that, it is only required to replace Cst in the second embodiment with Cst1 and deem Cst2 to be a part of the liquid crystal capacitance C_{lc} . The principle for implementation thereof is the same as that of the second embodiment of common electrode driving method according to present invention, and the description thereof will not be repeated herein.

[0037] In step 502, the first common electrode signal is inputted to the rows of pixels, and the second common electrode signal is inputted to the color-filter substrate.

[0038] In this embodiment, the first common electrode signal generated in step 501 is inputted to the rows of pixels, so that the kickback voltage ΔV_p will not be generated on the pixel electrodes. Thereby, accuracy of pixel electrode voltage is ensured and a screen flicker is avoided.

[0039] For this embodiment, with the transition timing of the first common electrode signal inputted to the rows of pixels being specified to be opposite to that of the gate signal for a corresponding row of pixels, and a difference between the high level and the low level of the first common electrode signal being equal to $[C_{gd} \cdot (V_{gh} - V_{gl})] / C_{st1}$, changes in the charges stored in the parasitic capacitance and the storage capacitance are offset with each other and the charge change amount on the pixel electrode become zero, so that kickback voltage on the pixel electrode become zero. Thereby, accuracy of pixel electrode voltage is ensured and a screen flicker is avoided.

[0040] Fig. 3 is a structural diagram of a first embodiment of common electrode driving circuit according to the invention. As shown in Fig. 3, the common electrode driving circuit according to this embodiment comprises a driving signal generation circuit 11 and a common electrode signal output terminal 12. The driving signal generation circuit 11 is used for generating a first common electrode signal for rows of pixels on the array substrate and a second common electrode signal on the color-filter substrate, the first common electrode signal being opposite to the gate signal for a corresponding row of pixels in terms of transition timing, and the charge change amount in the storage capacitance due to the transition of first common electrode signal is equal to the charge change amount in the parasitic capacitance due to the transition of the gate signal; and the common electrode signal output terminal 12 is used for inputting the first common electrode signal to the rows of pixels, and inputting the second common electrode signal to the common electrode on the color-filter substrate.

[0041] The common electrode driving circuit according to this embodiment can be included in an existing common electrode driving circuit. Those skilled in the art can design a specific circuit implementation by themselves in accordance with functions implemented by the common electrode driving circuit according to this embodiment, and a description thereof will not be given herein.

[0042] The common electrode driving circuit according to this embodiment can be used to carry out the first embodiment of common electrode driving method, and principle for implementation thereof is similar, thus a description thereof will not be repeated herein.

[0043] For the common electrode driving circuit according to this embodiment, with the transition timing of the first common electrode signal inputted to the rows of pixels being specified to be opposite to that of the gate signal for a corresponding row of pixels, and the charge change amount in the storage capacitance due to the transition of first common electrode signal being equal to the charge change amount in the parasitic capacitance due to the transition of the gate signal, changes in the charges stored in the parasitic capacitance and in storage capacitance are offset with each other and charge change amount on the pixel electrode become zero, thus a kickback voltage on the pixel electrode

become zero. Thereby, accuracy of pixel electrode voltage is ensured and a screen flicker is avoided.

[0044] In a second embodiment of common electrode driving circuit according to this invention, the structure thereof also can be configured by the circuit structure shown in Fig. 3. Further, in this embodiment, storage capacitance Cst has a structure in which the pixel electrode is overlapped with the storage electrode line, and a difference between the high level and the low level of the first common electrode signal generated by the driving signal generation circuit 11 is equal to $[C_{gd} \cdot (V_{gh} - V_{gl})] / C_{st}$, where Cgd is the capacity value of the parasitic capacitance, Cst is the capacity value of the storage capacitance, and Vgh and Vgl are ON voltage and OFF voltage of the gate electrode, respectively.

[0045] The common electrode driving circuit according to this embodiment can be used to carry out the method of the second embodiment of common electrode driving method, and principle for implementation thereof is similar, thus a description thereof will not be repeated herein.

[0046] For the common electrode driving circuit according to this embodiment, with the transition timing of the first common electrode signal inputted to the rows of pixels being specified to be opposite to that of the gate signal for a corresponding row of pixels, and a difference between the high level and the low level of the first common electrode signal being equal to $[C_{gd} \cdot (V_{gh} - V_{gl})] / C_{st}$, changes in the charges stored in the parasitic capacitance and storage capacitance are offset with each other and the charge change amount on the pixel electrode become zero, thus a kickback voltage on the pixel electrode become zero. Thereby, accuracy of pixel electrode voltage is ensured and a screen flicker is avoided.

[0047] In a third embodiment of common electrode driving circuit according to this invention, the structure thereof also can be configured by the circuit structure shown in Fig. 3. Further, in this embodiment, the storage capacitance has a structure in which the pixel electrode is respectively overlapped with the storage electrode line and the gate line, and a difference between the high level and the low level of the first common electrode signal generated by the driving signal generation circuit 11 is equal to $[C_{gd} \cdot (V_{gh} - V_{gl})] / C_{st1}$, where Cgd is the capacity value of the parasitic capacitance, Cst1 is the capacity value of a part of the storage capacitance on the storage electrode line, and Vgh and Vgl are ON voltage and OFF voltage of the gate electrode, respectively.

[0048] The common electrode driving circuit according to this embodiment can be used to carry out the method of third embodiment of common electrode driving method, and principle for implementation thereof is similar, thus a description thereof will not be repeated herein.

[0049] For the common electrode driving circuit according to this embodiment, with the transition timing of the first common electrode signal inputted to the rows of pixels being specified to be opposite to that of the gate signal for a corresponding row of pixels, and a difference between the high level and the low level of the first common electrode signal being equal to $[C_{gd} \cdot (V_{gh} - V_{gl})] / C_{st1}$, changes in the charges stored in the parasitic capacitance and storage capacitance are offset with each other and charge change amount on the pixel electrode become zero, thus a kickback voltage on the pixel electrode become zero. Thereby, accuracy of pixel electrode voltage is ensured and a screen flicker is avoided.

[0050] Fig. 4 is a structural diagram of a fourth embodiment of common electrode driving circuit according to the invention. As shown in Fig. 4, the common electrode driving circuit according to this embodiment is configured on the basis of the first embodiment of the common electrode driving circuit shown in Fig.3, and further, the driving signal generation circuit 11 includes a first driving signal generation unit 111 and a second driving signal generation unit 112. The first driving signal generation unit 111 is used for generating the second common electrode signal; and the second driving signal generation unit 112 is used for generating the first common electrode signal for the rows of pixels on the array substrate by generating a transition timing signal and superposing the transition timing signal on the second common electrode signal generated by the first driving signal generation unit, the first common electrode signal being opposite to the gate signal for a corresponding row of pixels in terms of transition timing, and the charge change amount in the storage capacitance due to the transition of the first common electrode signal being equal to that of the charge change amount due to the transition of the gate signal.

[0051] In this embodiment, on the basis of the related arts, it is possible to use the second driving signal generation unit 112 to generate the transition timing signal and superpose the transition timing signal on the second common electrode signal generated by the first driving signal generation unit 111 and inputted to the color-filter substrate, and thereby to generate the first common electrode signal to be inputted to the array substrate, so that the first common electrode signal is opposite to the gate signal for a corresponding row of pixels in terms of transition timing, and the charge change amount in the storage capacitance due to the transition of first common electrode signal is equal to that of the charge change amount due to the transition of the gate signal. Therefore, changes in the charges stored in the parasitic capacitance and storage capacitance are offset with each other, and the charge change amount on the pixel electrode become zero, thus a kickback voltage on the pixel electrode become zero. Thereby, accuracy of pixel electrode voltage is ensured and a screen flicker is avoided. Furthermore, the common electrode driving circuit according to this embodiment only needs a small modification to that in the related arts, and implementation thereof is convenient.

[0052] Fig. 5 is a structural diagram of a first embodiment of a liquid crystal display according to the invention. As shown in Fig. 5, the liquid crystal display according to this embodiment includes a liquid crystal panel and a driver for

driving the liquid crystal panel. The liquid crystal panel is made by assembling an array substrate 1 and a color-filter substrate 2 with a liquid crystal layer 3 filled therebetween. The driver comprises a gate driver 4, a data driver 5 and a common electrode driver 6. The common electrode driver 6 is used for generating a first common electrode signal for the rows of pixels on the array substrate 1 and a second common electrode signal on the color-filter substrate 2, and inputting the generated first common electrode signal to the rows of pixels respectively and inputting the generated second common electrode signal to the common electrode on the color-filter substrate. The first common electrode signal is opposite to a gate signal for a corresponding row of pixels in terms of transition timing, and the charge change amount in the storage capacitance due to the transition of the first common electrode signal is equal to that of the charge change amount due to the transition of the gate signal.

[0053] In the liquid crystal display according to this embodiment, the first common electrode signal is opposite to the gate signal for a corresponding row of pixels in terms of transition timing, and the charge change amount in the storage capacitance due to the transition of first common electrode signal is equal to the charge change amount in the parasitic capacitance due to the transition of the gate signal. That is, the first common electrode signal generated in the this embodiment can enable a relation of $\Delta Q_{gd} = -\Delta Q_{st}$, and at the same time, a sum of charges stored in the liquid crystal capacitance C_{lc} , the storage capacitance C_{st} , and parasitic capacitance C_{gd} is in conservation, thus there is relation of $\Delta Q_{lc} + \Delta Q_{gd} + \Delta Q_{st} = 0$, hence $\Delta Q_{lc} = 0$, where ΔQ_{lc} is charge change amount upon turning off of the gate, and $\Delta Q_{lc} = C_{lc}(V_{p2} - V_{p1})$. Since the liquid crystal capacitance C_{lc} is a constant, it comes to relation of $V_{p2} = V_{p1}$, and thus $\Delta V_p = V_{p2} - V_{p1} = 0$. That is, there is no change occurred to the pixel voltage upon turning off of the gate. The reason thereof is that the change amount of the charges stored in the parasitic capacitance C_{gd} upon turning off of the TFT, that is, ΔQ_d , and the change amount of the charges stored in the storage capacitance C_{st} upon turning on of the storage electrode line are the same in magnitude and opposite in change direction, thus total change of the charges stored in the two capacitance become zero, and changes in the charges stored in the two capacitances are offset with each other. Therefore, change amount in charges on the pixel electrode become zero, and hence a kickback voltage ΔV_p on the pixel electrode become zero.

[0054] It should be noted that, the common electrode driving circuit 6 according to this embodiments can be implemented with the common electrode driving circuit shown in Fig. 3 or Fig. 4, and a description thereof will not be repeated herein.

[0055] For the liquid crystal display according to this embodiment, with the transition timing of the first common electrode signal inputted to the rows of pixels being specified to be opposite to that of the gate signal for a corresponding row of pixels, and the charge change amount in the storage capacitance due to the transition of first common electrode signal being equal to the charge change amount in the parasitic capacitance due to the transition of the gate signal, changes in the charges stored in the parasitic capacitance and the storage capacitance are offset with each other, and the charge change amount on the pixel electrode become zero, thus a kickback voltage on the pixel electrode become zero. Thereby, accuracy of pixel electrode voltage is ensured and a screen flicker is avoided.

[0056] In a second embodiment of the liquid crystal display according to this invention, the structure thereof also can be configured by the structure shown in Fig. 5. Further, in this embodiment, the storage capacitance C_{st} has a structure in which the pixel electrode is overlapped with the storage electrode line, and a difference between the high level and the low level of the first common electrode signal generated by the common electrode driving circuit 6 is equal to $[C_{gd} \cdot (V_{gh} - V_{gl})] / C_{st}$, where C_{gd} is the capacity value of the parasitic capacitance, C_{st} is the capacity value of the storage capacitance, and V_{gh} and V_{gl} are an ON voltage and an OFF voltage of the gate electrode, respectively.

[0057] The liquid crystal display according to this embodiment can be used to carry out the method of the second embodiment of common electrode driving method, and the principle for implementation thereof is similar, thus the description thereof will not be repeated herein.

[0058] For the liquid crystal display according to this embodiment, with the transition timing of the first common electrode signal inputted to the rows of pixels being specified to be opposite to that of the gate signal for a corresponding row of pixels, and a difference between the high level and the low level of the first common electrode signal being equal to $[C_{gd} \cdot (V_{gh} - V_{gl})] / C_{st}$, changes in the charges stored in the parasitic capacitance and the storage capacitance are offset with each other and charge change amount on the pixel electrode become zero, thus a kickback voltage on the pixel electrode become zero. Thereby, accuracy of pixel electrode voltage is ensured and a screen flicker is avoided.

[0059] In a third embodiment of the liquid crystal display according to this invention, the structure thereof also can be configured by the structure shown in Fig. 5. Further, in this embodiment, the storage capacitance C_{st} has a structure in which the pixel electrode is respectively overlapped with the storage electrode line and the gate line, and a difference between the high level and the low level of the first common electrode signal generated by the common electrode driving circuit 6 is equal to $[C_{gd} \cdot (V_{gh} - V_{gl})] / C_{st1}$, where C_{gd} is the capacity value of the parasitic capacitance, C_{st1} is the capacity value of a part of the storage capacitance on the storage electrode line, and V_{gh} and V_{gl} are an ON voltage and an OFF voltage of the gate electrode, respectively.

[0060] The liquid crystal display according to this embodiment can be used to carry out the method of the third embodiment of common electrode driving method, and the principle for implementation thereof is similar, thus the description

thereof will not be repeated herein.

[0061] For the liquid crystal display according to this embodiment, with the transition timing of the first common electrode signal inputted to the rows of pixels being specified to be opposite to that of the gate signal for a corresponding row of pixels, and a difference between the high level and the low level of the first common electrode signal being equal to $[C_{gd} \cdot (V_{gh} - V_{gl})] / C_{st1}$, changes in the charges stored in the parasitic capacitance and storage capacitance are offset with each other and the charge change amount on the pixel electrode become zero, thus a kickback voltage on the pixel electrode become zero. Thereby, accuracy of pixel electrode voltage is ensured and a screen flicker is avoided.

[0062] Those skilled in the art can understand that, the steps for implementing the above embodiments can be fully or partly realized by software, hardware, firmware or the like in association with a program. The aforementioned program can be stored in a computer readable storage medium. When executed, the program executes the steps involving the embodiments of above methods, and the aforementioned storage medium include a various of medium that can store program codes, such as ROM, RAM, diskette or optical disc and the like.

[0063] Finally, it should be explained that, the above embodiments are only used for explaining the technical solution of present invention, and not for limitation thereto. Although the present invention has been explained in details with reference to the preferred embodiments, it should be understood by those skilled in the art that modifications and equivalent alternations may be made to the technical solution of present invention, and these modifications and equivalent alternations can not depart the modified technical solution from the spirit and scope of the technical solution of present invention.

Claims

1. A common electrode driving method, comprising:

generating a first common electrode signal to be applied to a storage electrode line of each row of pixels on an array substrate, and a second common electrode signal to be applied to a common electrode forming a liquid crystal capacitance with pixel electrodes of each row of pixels on the array substrate, the first common electrode signal being opposite to a gate signal applied to the corresponding row of pixels in terms of transition timing; and inputting the first common electrode signal to each row of pixels, and inputting the second common electrode signal to the common electrode.

2. The common electrode driving method according to claim 1, wherein the storage capacitance has a structure in which the pixel electrode is overlapped with the storage electrode line, and a difference between a high level and a low level of the first common electrode signal is equal to $[C_{gd} \cdot (V_{gh} - V_{gl})] / C_{st}$, where C_{gd} is a capacity value of a parasitic capacitance connected in series with the storage capacitance, C_{st} is a capacity value of the storage capacitance, and V_{gh} and V_{gl} are an ON voltage and an OFF voltage of a gate electrode, respectively.

3. The common electrode driving method according to claim 1, wherein the storage capacitance has a structure in which the pixel electrode is respectively overlapped with the storage electrode line and the gate line, and a difference between a high level and a low level of the first common electrode signal is equal to $[C_{gd} \cdot (V_{gh} - V_{gl})] / C_{st1}$, where C_{gd} is a capacity value of a parasitic capacitance connected in series with the storage capacitance, C_{st1} is a capacity value of a part of the storage capacitance on the storage electrode line, and V_{gh} and V_{gl} are an ON voltage and an OFF voltage of a gate electrode, respectively.

4. The common electrode driving method according to claim 1, wherein an absolute value of a charge change amount due to the transition of the first common electrode signal in the storage capacitance is equal to that of a charge change amount due to the transition of the gate signal in a parasitic capacitance connected in series with a storage capacitance, and change directions of them are opposite to each other.

5. The common electrode driving method according to claim 1, wherein the common electrode is formed on a color-filter substrate or the array substrate.

6. A common electrode driving circuit, comprising:

a driving signal generation circuit for generating a first common electrode signal to be applied to a storage electrode line of each row of pixels on an array substrate, and a second common electrode signal to be applied to a common electrode forming a liquid crystal capacitance with pixel electrodes of each row of pixels on the array substrate, the first common electrode signal being opposite to a gate signal applied to the corresponding

row of pixels in terms of transition timing; and

a common electrode signal output terminal for inputting the first common electrode signal to each row of pixels, and inputting the second common electrode signal to the common electrode.

7. The common electrode driving circuit according to claim 6, wherein the storage capacitance has a structure in which the pixel electrode is overlapped with the storage electrode line, and a difference between a high level and a low level of the first common electrode signal generated by the driving signal generation circuit is equal to $[C_{gd} \cdot (V_{gh} - V_{gl})] / C_{st}$, where C_{gd} is a capacity value of a parasitic capacitance connected in series with the storage capacitance, C_{st} is a capacity value of the storage capacitance, and V_{gh} and V_{gl} are an ON voltage and an OFF voltage of a gate electrode, respectively.
8. The common electrode driving circuit according to claim 6, wherein the storage capacitance has a structure in which the pixel electrode is respectively overlapped with the storage electrode line and the gate line, and a difference between a high level and a low level of the first common electrode signal generated by the driving signal generation circuit is equal to $[C_{gd} \cdot (V_{gh} - V_{gl})] / C_{st1}$, where C_{gd} is a capacity value of a parasitic capacitance connected in series with the storage capacitance, C_{st1} is a capacity value of a part of the storage capacitance on the storage electrode line, and V_{gh} and V_{gl} are an ON voltage and an OFF voltage of a gate electrode, respectively.
9. The common electrode driving circuit according to claim 6, wherein an absolute value of a charge change amount due to the transition of the first common electrode signal in the storage capacitance is equal to that of a charge change amount due to the transition of the gate signal in a parasitic capacitance connected in series with a storage capacitance, and change directions of them are opposite to each other.
10. The common electrode driving circuit according to claim 6, wherein the driving signal generation circuit comprises:
 - a first driving signal generation unit for generating the second common electrode signal; and
 - a second driving signal generation unit for generating the first common electrode signal by generating a transition timing signal and superposing the transition timing signal on the second common electrode signal generated by the first driving signal generation unit.
11. A liquid crystal display, comprising:
 - a liquid crystal panel; and
 - a driver for driving the liquid crystal panel,wherein the liquid crystal panel is formed by assembling an array substrate and a color-filter substrate with a liquid crystal layer filled therebetween, the driver comprising a gate driver, a data driver and a common electrode driver, wherein the common electrode driver is used for generating a first common electrode signal to be applied to a storage electrode line of each row of pixels on the array substrate, and a second common electrode signal to be applied to a common electrode forming a liquid crystal capacitance with pixel electrodes of each row of pixels on the array substrate, and inputting the generated first common electrode signal to each row of pixels and inputting the generated second common electrode signal to the common electrode, and wherein the first common electrode signal is opposite to a gate signal applied to the corresponding row of pixels in terms of transition timing.
12. The liquid crystal display according to claim 11, wherein the storage capacitance has a structure in which the pixel electrode is overlapped with the storage electrode line, and a difference between a high level and a low level of the first common electrode signal is equal to $[C_{gd} \cdot (V_{gh} - V_{gl})] / C_{st}$, where C_{gd} is a capacity value of a parasitic capacitance connected in series with the storage capacitance, C_{st} is a capacity value of the storage capacitance, and V_{gh} and V_{gl} are an ON voltage and an OFF voltage of a gate electrode, respectively.
13. The liquid crystal display according to claim 11, wherein the storage capacitance has a structure in which the pixel electrode is respectively overlapped with the storage electrode line and the gate line, and a difference between a high level and a low level of the first common electrode signal is equal to $[C_{gd} \cdot (V_{gh} - V_{gl})] / C_{st1}$, where C_{gd} is a capacity value of a parasitic capacitance connected in series with the storage capacitance, C_{st1} is a capacity value of a part of the storage capacitance on the storage electrode line, and V_{gh} and V_{gl} are an ON voltage and an OFF voltage of a gate electrode, respectively.

14. The liquid crystal display according to claim 11, wherein an absolute value of a charge change amount due to the transition of the first common electrode signal in the storage capacitance is equal to that of a charge change amount due to the transition of the gate signal in the parasitic capacitance connected in series with the storage capacitance, and change directions of them are opposite to each other.

5 15. The liquid crystal display according to claim 11, wherein the common electrode is formed on the color-filter substrate or the array substrate.

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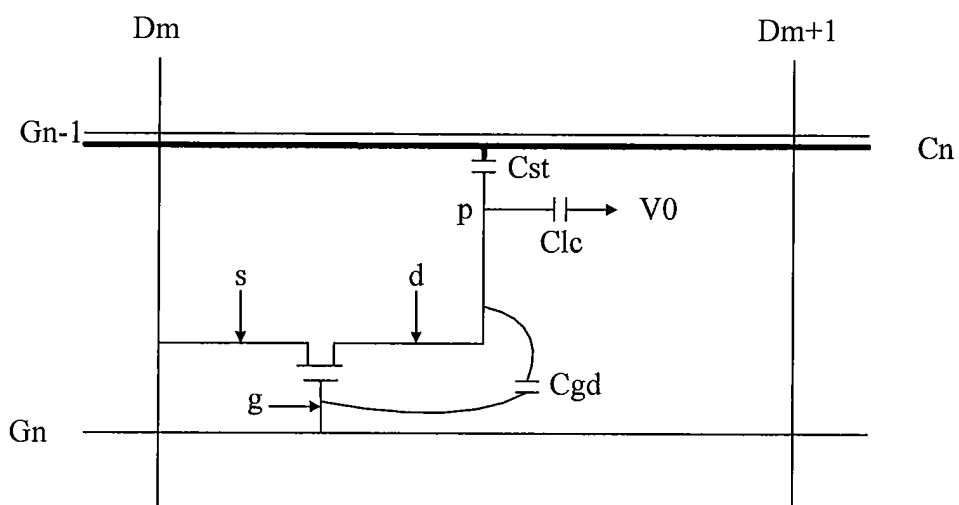


FIG.1

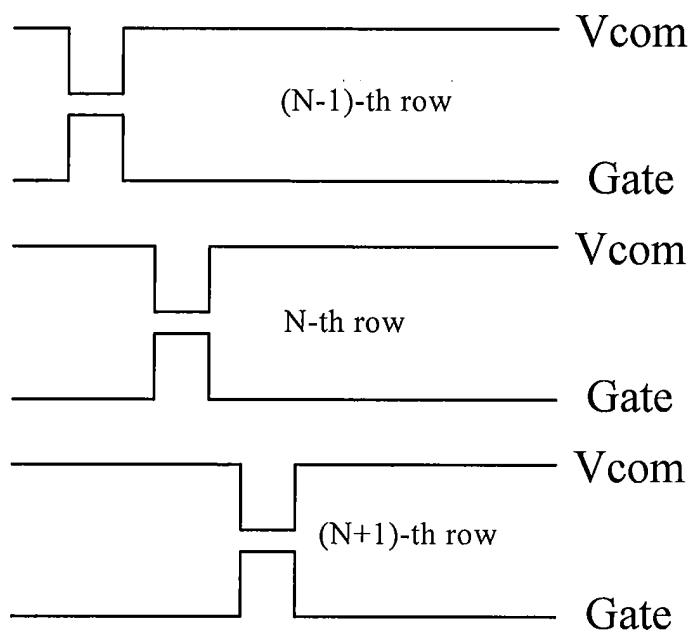


FIG.2

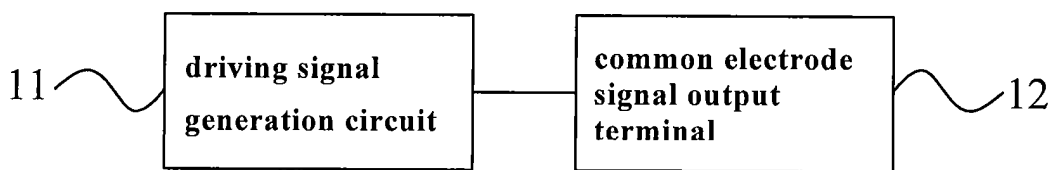


FIG.3

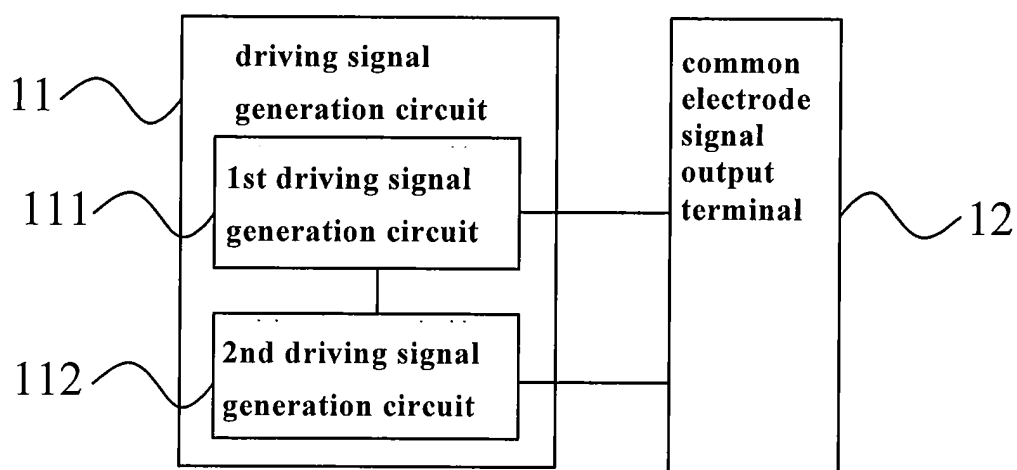


FIG.4

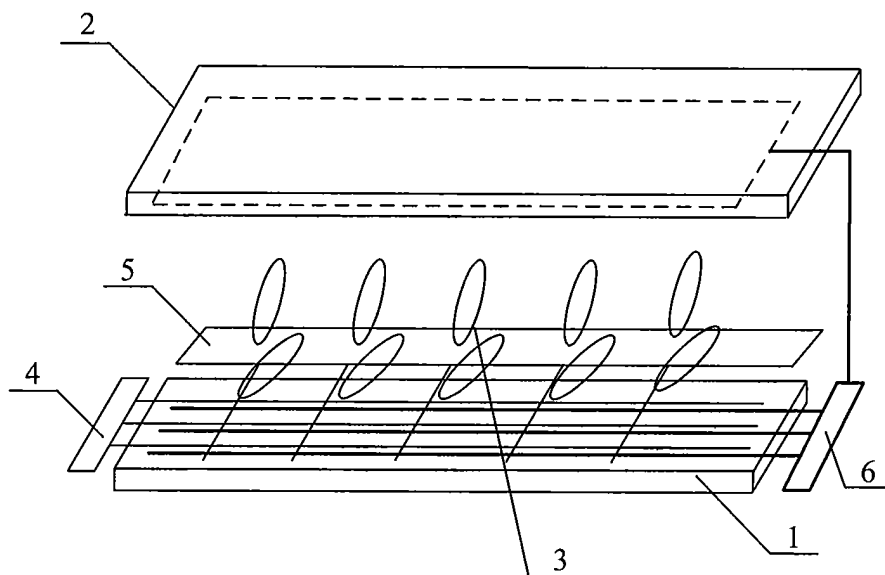


FIG.5

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2011/072939

A. CLASSIFICATION OF SUBJECT MATTER

G09G3/36 (2006.01) i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: G02F1/-; G09G3/-

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT,CNKI,WPI,EPODOC: common electrode, counter electrode, LCD, storage capacitance, capacitor, parasitic, gate, scan line

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US2005/0264509A1(SENDA, Michiru et al.) 01Dec. 2005 (01.12.2005) description paragraphs 【0021】 - 【0042】 , figs.1-2	1-15
A	US2008/0150928A1(KONINKLIJKE PHILIPS ELECTRONIC,N.V.)26 Jun. 2008 (26.06.2008) the whole document	1-15
A	US2006/0119756A1(SAMSUNG ELECTRONICS CO.,LTD.)08 Jun. 2006 (08.06.2006) the whole document	1-15
A	US2007/0164957A1(CHI MEI OPTOELECTRONICS CORP.)19 Jul. 2007 (19.07.2007) the whole document	1-15
A	US2007/0176905A1(HANNSTAR DISPLAY CORP.)02 Aug. 2007 (02.08.2007) the whole document	1-15
A	CN1744184A(SAMSUNG ELECTRONICS CO. ,LTD.)08 Mar. 2006 (08.03.2006) the whole document	1-15

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

* Special categories of cited documents:	“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
“A” document defining the general state of the art which is not considered to be of particular relevance	
“E” earlier application or patent but published on or after the international filing date	“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
“L” document which may throw doubts on priority claim (S) or which is cited to establish the publication date of another citation or other special reason (as specified)	“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
“O” document referring to an oral disclosure, use, exhibition or other means	
“P” document published prior to the international filing date but later than the priority date claimed	“&”document member of the same patent family

Date of the actual completion of the international search
26 May 2011 (26.05.2011)Date of mailing of the international search report
14 Jul. 2011 (14.07.2011)Name and mailing address of the ISA/CN
The State Intellectual Property Office, the P.R.China
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INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2011/072939

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		KR20060003968A	12.01.2006
		TW200615670A	16.05.2006

Form PCT/ISA /210 (patent family annex) (July 2009)

专利名称(译)	公共电极的驱动方法，电路及其液晶显示器		
公开(公告)号	EP2560156A1	公开(公告)日	2013-02-20
申请号	EP2011768452	申请日	2011-04-18
[标]申请(专利权)人(译)	北京京东方光电科技有限公司		
申请(专利权)人(译)	北京京东方光电科技有限公司.LTD.		
当前申请(专利权)人(译)	北京京东方光电科技有限公司.LTD.		
[标]发明人	XUE HAILIN XU YUBO LI CHENG ZHAN HONGMING ZHANG JIDONG		
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IPC分类号	G09G3/36		
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优先权	201010152188.3 2010-04-16 CN		
其他公开文献	EP2560156A4		
外部链接	Espacenet		

摘要(译)

一种公共电极的驱动方法，包括：产生施加到阵列基板上每个线像素的存储电极线的第一公共电极信号和施加到公共电极的第二公共电极信号，其与像素电极形成液晶电容。阵列基板上的每个行像素。第一公共电极信号的跳跃序列是施加到相应行像素的栅电极的栅电极信号的跳跃序列的倒数。该方法还包括将第一公共电极信号输入到每个线像素并将第二公共电极信号输入到所述公共电极。

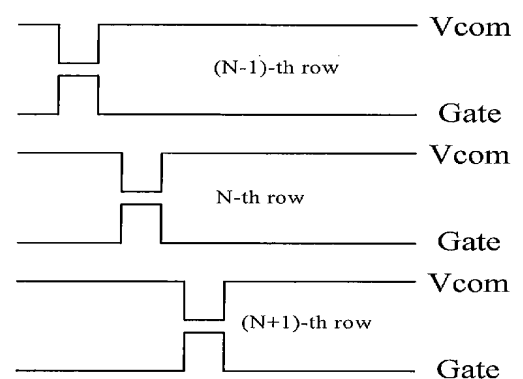


FIG.2