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(54) **Liquid crystal display**

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**Description**

## BACKGROUND OF THE INVENTION

## (a) Field of the Invention

**[0001]** The present invention relates to a liquid crystal display.

## (b) Description of the Related Art

**[0002]** A liquid crystal display ("LCD") is a widely used type of flat panel display ("FPD"), and typically includes two display panels on which field generating electrodes, such as pixel electrodes and a common electrode, are disposed, and a liquid crystal layer interposed between the two display panels. Voltages are applied to the field generating electrodes to generate an electric field in the liquid crystal layer. The electric field determines orientations of liquid crystal molecules in the liquid crystal layer, and controls polarization of incident light to display an image.

**[0003]** The LCD may further include switching elements connected to pixel electrodes, and signal lines such as gate lines and data lines, for example, which control the switching elements and apply voltages to the pixel electrodes.

**[0004]** The LCD typically receives an input image signal from an external source, e.g., a graphics controller, and the input image signal includes luminance information for each pixel, and the luminance information includes grayscale values. Each pixel receives the data voltage corresponding to the luminance information. The data voltage is applied to each pixel, and a difference between the data voltage and the common voltage is a pixel voltage. Each pixel thereby displays a luminance representing a gray level of the image signal based on the pixel voltage. A range of the pixel voltage applied to the liquid crystal display may vary based on a driver.

**[0005]** In a conventional LCD, the driver of the liquid crystal display may be disposed on the display panel as an integrated circuit ("IC") chip, or disposed on a flexible circuit film and attached to the display panel. However, the IC chip increases the manufacturing cost of the liquid crystal display. Particularly, the cost of the driver of the liquid crystal display is substantially increased as the number of data lines applying the data voltage is increased.

**[0006]** The following documents contain background art relevant to the invention.

**[0007]** US2006/0215066 discloses a liquid crystal display having two pixel electrodes per pixel, each electrode being controlled by a thin film transistor. The first pixel electrode is capacitively coupled to the second electrode via a third transistor and a capacitor (cf. fig. 4)

**[0008]** W02004/086129 discloses also a liquid crystal display having two pixel electrodes per pixel, each connected to a TFT (fig. 3, items T1 and T2) and electrically

connected to each other by a holding capacitor (fig. 3, CCcpb).

## BRIEF SUMMARY OF THE INVENTION

**[0009]** The invention discloses a liquid crystal display according to the appended claims.

**[0010]** Exemplary embodiments of the present invention provide a liquid crystal display ("LCD") having advantages that include, but are not limited to, increased contrast ratio and viewing angle, improved response speed of liquid crystal molecules, and reduced cost of the driver of the liquid crystal display by decreasing a required number of data lines.

**[0011]** In an exemplary embodiment, the first pixel electrode may include first branches, the second pixel electrode may include second branches, and the first branches of the first pixel electrode and the second branches of the second pixel electrode may be alternately disposed on the first substrate.

**[0012]** the first substrate, a fourth switching element connected to the fourth gate line and the third data line, a fifth switching element connected to the fifth gate line and the fourth data line, and a third pixel electrode connected to the fourth switching element and a fourth pixel electrode connected to the fifth switching element and separated from the third pixel electrode. The first gate line may be adapted to receive a gate-on signal, the first pixel electrode may be adapted to receive a first data voltage from the first data line and the third pixel electrode may be adapted to receive a second data voltage from the second data line. The second gate line may be adapted to receive the gate-on signal, the second pixel electrode may be adapted to receive a third data voltage from the second data line and the fourth pixel electrode may be adapted to receive a fourth data voltage from the third data line, wherein the first data voltage and the second data voltage may have different polarities, and the second data voltage and the third data voltage may have different polarities. The third gate line may be adapted to receive the gate on signal, wherein the second data voltage may be transmitted through the third switching element.

**[0013]** An exemplary embodiment of the liquid crystal display may further include: a fourth gate line disposed on the first substrate, a fifth gate line disposed on the first substrate, and a sixth gate line disposed on the first substrate; a third data line disposed on the first substrate and a fourth data line disposed on the first substrate; a fourth switching element connected to the fourth gate line and the third data line; a fifth switching element connected to the fifth gate line and the fourth data line; a sixth switching element connected to the sixth gate line and an output terminal of the fifth switching element; and a third pixel electrode connected to the fourth switching element and a fourth pixel electrode connected to the fifth switching element and separated from the third pixel electrode, where the fourth gate line may be connected

to the first gate line and transmit the first gate signal, the fifth gate line may be connected to the second gate line and transmit the second gate signal, the sixth gate line may be connected to the third gate line and transmit the same gate signal, and the third pixel electrode and the fourth pixel electrode may form a second liquid crystal capacitor.

**[0014]** In an exemplary embodiment, the first data line and the third data line may be disposed substantially adjacent to each other, and the second data line and the fourth data line may be disposed substantially adjacent to each other.

**[0015]** In an exemplary embodiment, the third pixel electrode may include third branches, the fourth pixel electrode may include fourth branches, and the third branches of the third pixel electrode and the fourth branches of the fourth pixel electrode may be alternately disposed on the first substrate.

#### BRIEF DESCRIPTION OF THE DRAWINGS

**[0016]** The above and other aspects, advantages and features of the present invention will become more apparent by describing in further detail exemplary embodiments thereof with reference to the accompanying drawings, in which:

FIG. 1 is a block diagram of an exemplary embodiment of a liquid crystal display according to the present invention;

FIG. 2 is a schematic equivalent circuit diagram of an exemplary embodiment of a pixel according to the present invention;

FIG. 3 is a partial cross-sectional view of an exemplary embodiment of a liquid crystal display according to the present invention;

FIG. 4 is a plan view illustrating a layout of an exemplary embodiment of pixel electrodes of a liquid crystal display according to the present invention;

FIG. 5 is a schematic circuit diagram of four pixels of a liquid crystal display not according to the present invention;

FIG. 6 is a signal timing diagram of wave forms of signals applied to one pixel of the liquid crystal display in FIG. 5;

FIG. 7 is a plan view illustrating a layout of four pixels of a liquid crystal display in FIG. 5;

FIG. 8 is a schematic circuit diagram of four pixels of a liquid crystal display not according to the present invention;

FIG. 9 is a schematic circuit diagram of two pixels of a liquid crystal display not according to the present invention;

FIG. 10 is a partial cross-sectional view of a storage capacitor in a liquid crystal display not according to the present invention;

FIG. 11 is a schematic circuit diagram of an exemplary embodiment of two pixels of a liquid crystal

display according to the present invention;

FIG. 12 is a schematic circuit diagram of an alternative exemplary embodiment of one pixel according to the present invention;

FIG. 13 is a schematic circuit diagram of one pixel in a liquid crystal display not according to the present invention;

FIG. 14 is a signal timing diagram of waveforms of signals applied to the one pixel of the liquid crystal display in FIG. 13; and

FIG. 15 is a schematic circuit diagram of one pixel in a liquid crystal display not according to the present invention.

#### 15 DETAILED DESCRIPTION OF THE INVENTION

**[0017]** The invention now will be described more fully hereinafter with reference to the accompanying drawings, in which various embodiments are shown. This invention may, however, be embodied in many different forms, and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. Like reference numerals refer to like elements throughout.

**[0018]** Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this invention belongs. It will be further understood that terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and the present disclosure, and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

**[0019]** Exemplary embodiments are described herein with reference to cross section illustrations that are schematic illustrations of idealized embodiments. As such, variations from the shapes of the illustrations as a result, for example, of manufacturing techniques and/or tolerances, are to be expected. Thus, embodiments described herein should not be construed as limited to the particular shapes of regions as illustrated herein but are to include deviations in shapes that result, for example, from manufacturing. For example, a region illustrated or described as flat may, typically, have rough and/or non-linear features. Moreover, sharp angles that are illustrated may be rounded. Thus, the regions illustrated in the figures are schematic in nature and their shapes are not intended to illustrate the precise shape of a region and are not intended to limit the scope of the present claims.

**[0020]** FIG. 1 is a block diagram of an exemplary embodiment of a liquid crystal display according to the present invention, and FIG. 2 is a schematic equivalent circuit diagram of an exemplary embodiment of a pixel according to an exemplary embodiment of the present invention.

**[0021]** As shown in FIG. 1, the liquid crystal display includes a liquid crystal panel assembly 300, a gate driver 400, a data driver 500, a gray voltage generator 800 and a signal controller 600.

**[0022]** As shown in FIG. 2, the liquid crystal panel assembly 300 includes a lower panel 100 and an upper panel 200 disposed to, e.g., facing, the lower panel 100, and a liquid crystal layer 3 interposed between the lower panel 100 and the upper panel (hereinafter collectively referred to as "display panels 100 and 200").

**[0023]** The liquid crystal capacitor Clc includes a first pixel electrode PEa and a second pixel electrode PEb of the lower panel 100 as two terminals thereof, and the liquid crystal layer 3 between the first pixel electrode PEa and the second pixel electrode PEb is a dielectric. The first pixel electrode PEa is connected to a first switching element (not shown in FIG. 2), and the second pixel electrode PEb is connected to a second switching element (not shown). The first switching element and the second switching element are connected to corresponding gate lines (not shown) and data lines (not shown).

**[0024]** The liquid crystal layer 3 has dielectric anisotropy, and liquid crystal molecules of the liquid crystal layer 3 may be arranged such that their longitudinal axes are aligned substantially vertical to surfaces of the display panels 100 and 200 when an electric field is not applied in the liquid crystal layer 3. The liquid crystal layer 3 may have positive dielectric anisotropy.

**[0025]** The first pixel electrode PEa and the second pixel electrode PEb may be disposed on two different layers or on a same layer, and the liquid crystal panel assembly may further include a common electrode (not shown) disposed on one panel of the lower panel 100 and the upper panel 200. Separate electrodes (not shown) disposed on the lower panel 100 may overlap the first and second pixel electrodes PEa and PEb via an insulator interposed therebetween, and thereby form a first storage capacitor (not shown) and a second storage capacitor (not shown), which assist the liquid crystal capacitor Clc.

**[0026]** In an exemplary embodiment, when a display panel displays colors, each pixel PX may display one of primary colors (spatial division), or each pixel PX may display primary colors in turn (temporal division). In an exemplary embodiment, the primary colors may be spatially or temporally synthesized, and a predetermined color is thereby displayed. The primary colors may be three primary colors, such as red, green and blue, for example. In an exemplary embodiment, as shown in FIG. 2, each pixel PX may include a color filter CF, corresponding to one of the primary colors, disposed on the upper panel 200. In an alternative exemplary embodiment, the color filter CF may be disposed on or below the first and second pixel electrodes PEa and PEb of the lower panel 100.

**[0027]** In an exemplary embodiment, the liquid crystal panel assembly 300 includes at least one polarizer (not shown) which provides light polarization.

**[0028]** An operation of a liquid crystal display according to an exemplary embodiment of the present invention will be described hereafter.

**[0029]** FIG. 3 is a partial cross-sectional view of an exemplary embodiment of a liquid crystal display according to the present invention.

**[0030]** As shown in FIG. 2 and FIG. 3, when a data line connected to a pixel PX receives a data voltage, the data voltage is applied to the pixel PX through the first and second switching elements turned on by the gate signal. When the first and second switching elements turned on by the gate signal, the first pixel electrode PEa receives a first data voltage through the first switching element, and the second pixel electrode PEb receives a second data voltage through the second switching element. In an exemplary embodiment, two data voltages, e.g., the first data voltage and the second data voltage, applied to the first and second pixel electrodes PEa and PEb, respectively, may be data voltages corresponding to a luminance to be displayed by the pixel PX, and may have opposite polarities with respect to a reference voltage Vref.

**[0031]** The difference between the two data voltages applied to the first and second subpixels PXa and PXb may be a charged voltage of the liquid crystal capacitors Clc, e.g., a pixel voltage. When a potential difference is generated between two terminals of the liquid crystal capacitor Clc, as shown in FIG. 3, an electric field parallel to the surfaces of the display panel 100 and 200 is generated in the liquid crystal layer 3 between the first pixel electrode PEa and the second pixel electrode PEb. When liquid crystal molecules 31 have positive dielectric anisotropy, the liquid crystal molecules 31 are arranged such that the longitudinal axes thereof are aligned to be parallel to a direction of the electric field, and inclination degrees of the liquid crystal molecules 31 may vary based on a magnitude of the pixel voltage. When the liquid crystal molecules 31 are aligned as described above, the liquid crystal layer 3 is referred to as an electrically-induced optical compensation ("EOC") mode liquid crystal layer. In an exemplary embodiment, a degree of a change of polarization of light passing through the liquid crystal layer 3 may vary based on the inclination degree of the liquid crystal molecules 31. The change of the polarization may change transmittance of the light by the polarizer, and the pixel PX thereby displays a predetermined luminance.

**[0032]** In an exemplary embodiment, when one pixel PX receives the two data voltages having opposite polarities with respect to the reference voltage Vref, a driving voltage is substantially increased and a response speed and a transmittance of the liquid crystal molecule are thereby substantially increased. In an exemplary embodiment, when the polarities of the two data voltages applied to one pixel PX are opposite to each other, degradation of the display quality due to flicker is substantially prevented under driving types such as a column inversion or a row inversion, for example, as the degradation is

substantially prevented under a dot inversion.

**[0033]** In an exemplary embodiment, when the first and second switching elements are turned off in one pixel PX, the two data voltages applied to the first and second pixel electrodes PEa and PEb are substantially decreased by a kickback voltage such that the charging voltage of the pixel PX is substantially maintained, and display characteristics of the liquid crystal display are thereby effectively improved.

**[0034]** A layout of an exemplary embodiment of the first and second pixel electrodes PEa and PEb of a pixel PX of the liquid crystal panel assembly according to the present invention will be described hereafter. FIG. 4 is a plan view of a layout of an exemplary embodiment of pixel electrodes of a pixel of a liquid crystal display.

**[0035]** As shown in FIG. 4, an overall contour of the pixel electrodes PE including the first pixel electrode PEa and the second pixel electrode PEb has a quadrangle shape. The first pixel electrode PEa and the second pixel electrode PEb are engaged with each other with a gap 91 therebetween. The first and second pixel electrodes PEa and PEb, respectively, are substantially mirror symmetric with respect to an imaginary transverse center line CL. The first pixel electrode PEa includes a first upper region disposed above the imaginary transverse center line CL and a first lower region disposed below the imaginary transverse center line CL, and the second pixel electrode PEb includes a second upper region disposed above the imaginary transverse center line CL and a second lower region disposed below the imaginary transverse center line CL.

**[0036]** The first pixel electrode PEa includes an upper projection, a lower projection, a first left longitudinal stem, a first transverse stem extending to a right direction from a center of the first left longitudinal stem, first upper branches and first lower branches. The first upper branches disposed above the imaginary transverse center line CL extend substantially obliquely in an upper right direction from the first left longitudinal stem and from the first transverse stem. The first lower branches disposed below the imaginary transverse center line CL extend substantially obliquely in a lower right direction from the first left longitudinal stem and the first transverse stem. An angle between the first upper and lower branches and the gate line 121 or an angle between the first upper and lower branches and the transverse center line CL may be about 45 degrees.

**[0037]** The second pixel electrode PEb includes a middle projection, a second right longitudinal stem, a second upper transverse stem, a second lower transverse stem, second upper branches and second lower branches. The second upper transverse stem and the second lower transverse stem extend substantially horizontally to a left direction from a lower end and an upper end of the longitudinal stem, respectively. The second upper branches disposed above the imaginary transverse center line CL extends substantially obliquely in a lower left direction from the second right longitudinal stem or the second

upper transverse stem. The second lower branches disposed below the imaginary transverse center line CL extends substantially obliquely in an upper left direction from the second right longitudinal stem or the second lower transverse stem. An angle between the second upper and lower branches of the second pixel electrode PEb and the gate line 121 or an angle between the second upper and lower branches of the second pixel electrode PEb and the imaginary transverse center line CL may be about 45 degrees. An angle between the second upper branches adjacent to the imaginary transverse center line CL and the second lower branches adjacent to the imaginary transverse center line CL may be about 90 degrees.

**[0038]** The first upper and lower branches of the first subpixel electrode PEa and the second upper and lower branches of the second subpixel electrode PEb are alternately disposed by engaging the upper and lower branches of the first subpixel electrodes PEa with the upper and lower branches of the second subpixel electrodes PEb, respectively, with a predetermined gap 91 therebetween, and thereby formed in a pectinated pattern.

**[0039]** In an alternative exemplary embodiment, the first and second pixel electrodes PEa and PEb of the pixel PX of the liquid crystal display may be in a different shape in which at least a portions the first pixel electrode PEa and at least a portion of the second pixel electrode PEb are alternately disposed in a same layer.

**[0040]** An arrangement and driving method of pixels and signal lines of an example of a liquid crystal display not according to the present invention will be described hereafter with reference to FIG. 5 and FIG. 6. FIG. 5 is a schematic circuit diagram of an example of four pixels of the liquid crystal display not according to the present invention, and FIG. 6 is a signal timing diagram illustrating an example not according to the invention of wave forms of signals applied to one pixel of the liquid crystal display of FIG. 5.

**[0041]** Referring back to FIG. 2 and as shown in FIG. 5, a liquid crystal display may include a first pixel PX(m, n) and a second pixel PX(m, n+1) adjacent to the first pixel PX(m, n) in a pixel row direction, a third pixel PX(m+1, n) and a fourth pixel PX(m+1 and n+1), respectively, adjacent to the first pixel PX(m, n) and the second pixel PX(m, n+1) in a pixel column direction, and signal lines Gi(a), Gi(b), Gi+1(a), Gi+1(b), Dj, Dj+1, and Dj+2 connected thereto. The signal lines Gi(a), Gi(b), Gi+1(a), Gi+1(b), Dj, Dj+1, and Dj+2 include pairs of gate lines which transmit gate signals (alternatively referred to as "scanning signals"), for example, a i-th (where "i" is a natural number less than or equal to "n") pair of gate lines Gi(a) and Gi(b), and a (i+1)-th pair of gate lines Gi+1(a) and Gi+1(b), and data lines which transmit data voltages including a j-th (where "j" is a natural number less than or equal to "m") data line, e.g. a first data line Dj, a (j+1)-th data line, e.g., a second data line Dj+1, and a (j+2)-th data line, e.g., a third data line Dj+2.

**[0042]** The first pixel  $PX(m, n)$  is connected to a first upper gate line  $Gi(a)$ , which is one of the  $i$ -th pair of gate lines  $Gi(a)$  and  $Gi(b)$ , the first data line  $Dj$  and the second data line  $Dj+1$ . The first pixel  $PX(m, n)$  includes a first switching element  $Qa$  connected to the first gate line  $Gi(a)$  and the first data line  $Dj$ , a second switching element  $Qb$  connected to the first upper gate line  $Gi(a)$ , and the second data line  $Dj+1$ , a liquid crystal capacitor  $Clc$  connected to the first and second switching elements  $Qa$  and  $Qb$ , and a first storage capacitor  $Csta$  and a second storage capacitor  $Cstb$  connected to the liquid crystal capacitor  $Clc$ . An alternative exemplary embodiment may not include the first and second storage capacitors  $Csta$  and  $Cstb$ . The first and second switching elements  $Qa$  and  $Qb$ , may be three terminal elements, such as thin film transistors, for example. The first storage capacitor  $Csta$  may include a control terminal connected to the first upper gate line  $Gi(a)$ , an input terminal connected to the first data line  $Dj$ , and an output terminal connected to the liquid crystal capacitor  $Clc$  and the first storage capacitor  $Csta$ , and the second storage capacitor  $Cstb$  may include a control terminal connected to the first gate line  $Gi(a)$ , an input terminal connected to the second data line  $Dj+1$ , and a second output terminal connected to the liquid crystal capacitor  $Clc$  and the second storage capacitor  $Cstb$ . The liquid crystal capacitor  $Clc$  includes the first pixel electrode  $PEa$  and the second pixel electrode  $PEb$  as two terminals thereof, and the liquid crystal layer 3 between the first pixel electrode and the second pixel electrode may be a dielectric. The first pixel electrode  $PEa$  is connected to the first switching element  $Qa$ , and the second pixel electrode  $PEb$  is connected to the second switching element  $Qb$ .

**[0043]** The second pixel  $PX(m, n+1)$  adjacent to the first pixel  $PX(m, n)$  in the pixel row direction is connected to a first lower gate line  $Gi(b)$ , which is the other of the  $i$ -th pair of gate lines  $Gi(a)$  and  $Gi(b)$ , the second data line and the third data line  $Dj+2$ . The second pixel  $PX(m, n+1)$  includes a first switching element  $Qa$  connected to the second gate line  $Gi(b)$  and the second data line  $Dj+1$ , a second switching element  $Qb$  connected to the first lower gate line  $Gi(b)$  and the third data line  $Dj+2$ , a liquid crystal capacitor  $Clc$  connected to the first and second switching elements  $Qa$  and  $Qb$ , and a first storage capacitor  $Csta$  and a second storage capacitor  $Cstb$  connected to the liquid crystal capacitor  $Clc$ .

**[0044]** The third pixel  $PX(m+1, n)$  adjacent to the first pixel  $PX(m, n)$  in the pixel column direction is connected to the second upper gate line  $Gi+1(a)$ , which is one of the  $(i+1)$ -th pair of gate lines  $Gi+1(a)$  and  $Gi+1(b)$ , the third data line  $Dj$  and the second data line  $Dj+1$ , and includes a first switching elements  $Qa$  connected to the second upper  $Gi+1(a)$  and the first data line  $Dj$ , a second switching element  $Qb$  connected to the second upper gate line  $Gi+1(a)$  and the second data line  $Dj+1$ , a liquid crystal capacitor  $Clc$  connected to the first and second switching elements  $Qa$  and  $Qb$ , and a first storage capacitor  $Csta$  and a second storage capacitor  $Cstb$  con-

nected to the liquid crystal capacitor  $Clc$ .

**[0045]** The fourth pixel  $PX(m+1, n+1)$  adjacent to the second pixel  $PX(m, n+1)$  in the pixel column direction is connected to the second lower gate line  $Gi+1(b)$  which is the other of the  $(i+1)$ -th pair of gate lines  $Gi+1(a)$  and  $Gi+1(b)$ , the second data line  $Dj+1$ , and the third data line  $Dj+2$ , and includes a first switching elements  $Qa$  connected to the second lower gate line  $Gi+1(b)$  and the second data line  $Dj+1$  and a second switching element  $Qb$  connected to the second lower gate line  $Gi+1(b)$  and the third data line  $Dj+2$ , a liquid crystal capacitor  $Clc$  connected to the first and second switching elements  $Qa$  and  $Qb$ , and a first storage capacitor  $Csta$  and a second storage capacitor  $Cstb$  connected to the liquid crystal capacitor  $Clc$ .

**[0046]** The first pixel  $PX(m, n)$  and the second pixel  $PX(m, n+1)$  adjacent to each other in the pixel row direction are both connected to the second data line  $Dj+1$ , and the third pixel  $PX(m+1, n)$  and the fourth pixel  $PX(m+1, n+1)$  are both connected to the second data line  $Dj+1$ .

**[0047]** As shown in FIG. 5 and FIG. 6, when the first upper gate line  $Gi(a)$  of the  $i$ -th pair of gate lines  $Gi(a)$  and  $Gi(b)$  receives a gate-on voltage, a first data voltage is applied to the first pixel  $PX(m, n)$  through the first and second switching elements  $Qa$  and  $Qb$  of the first pixel  $PX(m, n)$  that are turned on. In an example not according to the invention, the first pixel electrode  $PEa$  of the first pixel  $PX(m, n)$  receives the first data voltage from the first data line  $Dj$  through the first switching element  $Qa$  of the first pixel  $PX(m, n)$ , and the second pixel electrode  $PEb$  of the first pixel  $PX(m, n)$  receives a second data voltage from the second data line  $Dj+1$  through the second switching element  $Qb$  of the first pixel  $PX(m, n)$ . When the first lower gate line  $Gi(b)$  of the  $i$ -th pair of gate lines  $Gi(a)$  and  $Gi(b)$  receives the gate-on voltage, the second data voltage is applied to the second pixel  $PX(m, n+1)$  through the first and second switching elements of the second pixel  $PX(m, n+1)$  that are turned on. The first pixel electrode  $PEa$  of the second pixel  $PX(m, n+1)$  receives the second data voltage from the second data line  $Dj+1$  through the first switching element  $Qa$  of the second pixel  $PX(m, n+1)$ , and the second pixel electrode  $PEb$  of the second pixel  $PX(m, n+1)$  receives a third data voltage from the third data line  $Dj+2$  through the second switching element  $Qb$  of the second pixel  $PX(m, n+1)$ . Accordingly, a data voltage to be transmitted to the second pixel electrode  $PEb$  of the first pixel  $PX(m, n)$  is applied to the second data line  $Dj+1$  during a time that the first upper gate line  $Gi(a)$  receives the gate-on signal, and a data voltage to be transmitted to the first pixel electrode  $PEa$  of the second pixel  $PX(m, n+1)$  is applied to the second data line  $Dj+1$  during a time that the first lower gate line  $Gi(b)$  receives the gate-on signal.

**[0048]** Voltages applied to the first and second pixel electrodes  $PEa$  and  $PEb$  of the first pixel  $PX(m, n)$  and the third pixel  $PX(m, n+1)$  are data voltages corresponding to a luminance for the first pixel  $PX(m, n)$  and the third pixel  $PX(m, n+1)$  to be respectively displayed, and have

opposite polarities with respect to the reference voltage  $V_{ref}$ , for example, a common voltage  $V_{com}$  of a common electrode (not shown). In an exemplary embodiment, when a polarity of the first data voltage applied to the first data line  $D_j$  is positive, a polarity of the second data voltage applied to the second data line  $D_{j+1}$  is negative and a polarity of the third data voltage applied to the third data line  $D_{j+2}$  is positive. When the polarity of the first data voltage applied to the first data line  $D_j$  is negative, the polarity of the second data voltage applied to the second data line  $D_{j+1}$  is positive and the polarity of the third data voltage applied to the third data line  $D_{j+2}$  is negative. As described above, the data lines of an example of a liquid crystal display not according to the present invention may be driven with a column inversion.

**[0049]** In a conventional liquid crystal display, two pixels adjacent to each other in the pixel row direction are connected to one gate line and four different data lines. That is, the first and second switching elements connected to the first and second pixel electrodes of each of the two pixels are connected to a same gate line, but they are connected to different data lines such that they receive the data voltages through the different data lines.

**[0050]** In an example of a liquid crystal display not according to the present invention, two pixels of the liquid crystal display adjacent to each other in the pixel row direction are respectively connected to one gate line of a pair of gate lines and the other gate line of the pair of gate lines, and connected to three data lines by sharing a middle data line of the three data lines disposed in a middle portion of the two pixels adjacent to the two pixels. Accordingly, a number of data lines is reduced, and the cost of the driver of the liquid crystal display is thereby substantially reduced. In an example not according to the invention, gate lines are disposed in pairs, and a number of gate lines is thereby substantially increased, however gate signals are gate on/off signals, and an operation of a gate driver is thereby simplified, while the manufacturing cost is reduced.

**[0051]** An example not according to the invention of the pixel of the liquid crystal display shown in FIG. 5 will be described hereafter with reference to FIG. 7. FIG. 7 is a plan view illustrating a layout of an example not according to the invention of four pixels of the liquid crystal display shown in FIG. 5.

**[0052]** Referring back to FIG. 5 and as shown in FIG. 7, the liquid crystal display includes the first pixel  $PX(m, n)$  and the second pixel  $PX(m, n+1)$ , the third pixel  $PX(m+1, n)$  and the fourth pixel  $PX(m+1, n+1)$  respectively adjacent to the first pixel  $PX(m, n)$  and the second pixel  $PX(m, n+1)$  in the pixel column direction, pairs of gate lines, for example, a pair of gate lines including a first upper gate line 121a1 and a first lower gate line 121b1, and a pair of gate lines including a second upper gate line 121a2 and a second lower gate line 121b2, and data lines, for example, a first data line 171 a, a second data line 171b and a third data line 171 c connected thereto. Each of the first pixel  $PX(m, n)$ , the second pixel  $PX(m,$

$n+1)$ , the third pixel  $PX(m+1, n)$ , and the fourth pixel  $PX(m+1, n+1)$  includes a first pixel electrode 191a and a second pixel electrode 191b connected to a first switching element and a second switching element, respectively. The first switching element and the second switching element may be three terminal elements such as thin film transistors, for example. The first switching element and the second switching element, respectively, include control electrodes, e.g., a first gate electrode 124a and a second gate electrode 124b, input electrodes, e.g., a first source electrode 173a and a second source electrode 173b, and output electrodes, e.g., a drain electrode 175a and a second drain electrode 175b. The control electrodes of the first and second switching elements are respectively connected to one line and the other line of the pair of gate lines 121a and 121b, the input electrodes of the first and second switching elements are respectively connected to one line and another line of the data lines 171 a, 171b and 171 c, and the output electrodes of the first and second switching elements are respectively connected to the first pixel electrode 191a and the second pixel electrode 191b through a first contact hole 185a and a second contact hole 185b. The first pixel electrode 191a and the second pixel electrode 191b may be substantially alternately disposed on a same layer.

**[0053]** The liquid crystal display includes a storage electrode line 131 and storage electrodes 135a and 135b, and the storage electrodes 135a and 135b overlap the first pixel electrode 191 a and the second pixel electrode 191b thereby forming storage capacitors.

**[0054]** An alternative arrangement and driving method of pixels and signal lines a liquid crystal display not according to the present invention will be described hereafter with reference to FIG. 2 and FIG. 8. FIG. 8 is a schematic circuit diagram of four pixels of a liquid crystal display not according to the present invention.

**[0055]** As shown in FIG. 8, the liquid crystal display includes a first pixel  $PX(m, n)$  and a second pixel  $PX(m, n+1)$  adjacent to the first pixel  $PX(m, n)$  in the pixel row direction a third pixel  $PX(m+1, n)$  and a fourth pixel  $PX(m+1, n+1)$  respectively adjacent to the first pixel  $PX(m, n)$  and the second pixel  $PX(m, n+1)$  in the pixel column direction, gate lines connected thereto, for example, a first gate line  $G_i$  and a second gate line  $G_{i+1}$ , and pairs of data lines connected thereto, for example, a first pair of data lines  $D_j$  and  $D_j'$ , a second pair of data lines  $D_{j+1}$  and  $D_{j+1}'$ , and a third pairs of data lines  $D_{j+2}$  and  $D_{j+2}'$ .

**[0056]** The first gate line  $G_i$  including a first upper line and a first lower line and the second gate line  $G_{i+1}$  including a second upper line and second lower line are disposed along the pixel column direction. The first pair of data lines  $D_j$  and  $D_j'$  including a first data line  $D_j$  and a second data line  $D_j'$ , the second pair of data lines  $D_{j+1}$  and  $D_{j+1}'$  including a first data line  $D_{j+1}$  and a second data line  $D_{j+1}'$ , and the third pair of data lines  $D_{j+2}$  and  $D_{j+2}'$  including a first data line  $D_{j+2}$  and a second data line  $D_{j+2}'$  are disposed along the pixel row direction.

**[0057]** A control terminal of the first switching element

Qa of the first pixel and a control terminal of the second switching element Qb of the first pixel respectively connected to the first pixel electrode PEa and the second pixel electrode PEb of the first pixel PX(m, n) are connected the first upper line of the i-th gate line, e.g., the first gate line Gi, and an input terminal of the first switching element Qa and an input terminal of the second switching element Qb are respectively connected to one data line of the j-th pair of data lines, e.g., the second data line Dj' of the first pair of data lines Dj and Dj', and one data line of the (j+1)-th pair of data lines, e.g., the second data line Dj+1' of the second pair of data lines Dj+1 and Dj+1'.

**[0058]** A control terminal of the first switching element Qa of the second pixel and a control terminal of the second switching element Qb of the second pixel, respectively connected to the first pixel electrode PEa and the second pixel electrode PEb of the second pixel PX(m, n+1) adjacent to the first pixel PX(m, n) in the pixel row direction, are connected to an upper line of the (i+1)-th gate line, e.g., the second upper line of the second gate line Gi+1, and an input terminal of the first switching element Qa of the first pixel and an input terminal of the second switching element Qb of the first pixel are respectively connected to one data line of the (j+1)-th pair of data lines, e.g., the second data line Dj+1' of the second pair of data lines Dj+1 and Dj+1', and one data line of the (j+2)-th pair of data lines, e.g., the second data line Dj+2' of the third pair of data lines Dj+2 and Dj+2'.

**[0059]** A control terminal of the first switching elements Qa of the third pixel and a control terminal of the second switching element Qb of the third pixel, respectively connected to the first pixel electrode PEa and the second pixel electrode PEb of the third pixel PX(m+1, n) adjacent to the first pixel PX(m, n) in the pixel column direction, are connected to a lower line of the i-th gate line, e.g., the first lower line of the first gate line Gi, and an input terminal of the first switching element of the third pixel and an input terminal of the second switching element of the third pixel are respectively connected to one data line of the j-th pair of data lines, e.g., the first data line Dj of the first pair of data lines Dj and Dj' and one data line of the (j+1)-th pair of data lines, e.g., the second data line Dj+1' of the second pair of data lines Dj+1 and Dj+1'.

**[0060]** A control terminal of the first switching element of the fourth pixel and a control terminal of the second switching element Qb of the fourth pixel, respectively connected to the first pixel electrode PEa and the second pixel electrode PEb of the fourth pixel PX(m+1, n+1) adjacent to the second pixel PX(m, n+1) in the pixel column direction and the third pixel PX(m+1, n) in the pixel row direction, are connected to the second branch of the (i+1)-th gate line, e.g., the second lower line of the second gate line Gi+1, and an input terminal of the first switching element of the fourth pixel and an input terminal of the second switching element Qb of the fourth pixel are respectively connected to one data line of the (j+1)-th pair of data lines, e.g., the first data line Dj+1 of the second pair of data lines Dj+1 and Dj+1' and one data line of the

(j+2)-th pair of data lines, e.g., the first data line Dj+2 of the third pair of data lines Dj+2 and Dj+2'. As described above, the first pixel PX(m, n) and the second pixel PX(m, n+1) adjacent to each other in the pixel row direction are connected to one data line, e.g., the second data line Dj+1' of the second pair of data lines Dj+1 and Dj+1', and the third pixel PX(m+1, n) and the fourth pixel PX(m+1, n+1) adjacent to each other in the pixel row direction are connected to one data line, e.g., the first data line Dj+1 of the second pair of data lines Dj+1 and Dj+1'. The first pixel PX(m, n) and the third pixel PX(m+1, n) adjacent to each other in the pixel column direction are respectively connected to an upper line and a lower line of one gate line, e.g., the first upper line and the first lower line of the first gate line Gi and thereby receives gate on/off voltages through the one gate line, e.g., the first gate line Gi, and the second pixel PX(m, n+1) and the fourth pixel PX(m+1, n+1) adjacent to each other in the pixel column direction are respectively connected to an upper line and a lower line of one gate line, e.g., the second upper line and the second lower line of the second gate line Gi+1 and thereby receives the gate on/off voltages through the one gate line, e.g., the second gate line Gi+1. Accordingly, the number of data lines and the number of gate lines are reduced, and the cost of the driver of the liquid crystal display is thereby substantially reduced and the driving speed is thereby increased.

**[0061]** An alternative arrangement of pixels and signal lines of a liquid crystal display not according to the present invention will be described hereafter with reference to FIG. 9. FIG. 9 is a schematic circuit diagram of two neighboring pixels of a liquid crystal display not according to the present invention.

**[0062]** An arrangement of pixels and signal lines of the liquid crystal display shown in FIG. 9 is substantially similar to the arrangement of pixels and signal lines of FIG. 5. As an alternative, the first pixel PX(m, n) is connected to the first upper gate line Gi(a) of the i-th pair of gate lines Gi(a) and Gi(b), the first data line Dj and the second data line Dj+1, and the second pixel PX(m, n+1) adjacent to the first pixel PX(m, n) in the pixel row direction is connected to the first lower gate line Gi(b) of the i-th pair of gate lines Gi(a) and Gi(b), the second data line Dj+1 and the third data line Dj+2. The first pixel PX(m, n) and the second pixel PX(m, n+1) adjacent to each other in the pixel row direction are connected to the middle data line of the three data line, e.g., the second data line Dj+1.

**[0063]** As an alternative, two terminals of a storage capacitor Cst of a pixel are connected to an output terminal of a first switching element Qa of the pixel and a second switching element Qb of the pixel.

**[0064]** FIG. 10 is a partial cross-sectional view of a storage capacitor Cst in a liquid crystal display not according to the present invention.

**[0065]** As shown in FIG. 10, a first pixel electrode PEa of a pixel is connected to a storage capacitance electrode 178 through a contact hole 186, and a voltage that the first pixel electrode PEa receives is thereby transmitted

to the storage capacitance electrode 178. The storage capacitance electrode 178 overlaps the second pixel electrode PEb via an insulating layer 180, and the storage capacitance electrode 178 and the second pixel electrode PEb thereby form the storage capacitor Cst.

**[0066]** An exemplary embodiment of an arrangement of pixels and signal lines, and a driving method of a liquid crystal display will be described hereafter with reference to FIG. 11 and FIG. 2. FIG. 11 is a schematic circuit diagram of an exemplary embodiment of two pixels of a liquid crystal display according to the present invention.

**[0067]** Referring back to FIG. 2 and as shown in FIG. 11, an exemplary embodiment of the liquid crystal display includes the first pixel PX(m, n) and the second pixel PX(m, n+1) adjacent to each other in the pixel row direction, and gate lines connected thereto, e.g., a first gate line Gi, a second gate line Gi+1, and a third gate line Gi+2, and data lines connected thereto, e.g., a first data line Dj, a second data line Dj+1, and a third data line Dj+2.

**[0068]** The first pixel PX(m, n) includes a first switching element Qa connected to the i-th gate line, e.g., the first gate line Gi, and the j-th data line, e.g., the first data line Dj, a second switching element Qb connected to the (i+1)-th gate line, e.g., the second gate line Gi+1, and the (j+1)-th data line, e.g., the second data line Dj+1, a first storage capacitor Csta connected to the first switching element Qa of the first pixel and a second storage capacitor Cstb connected to the second switching element Qb of the first pixel. The first pixel PX(m, n) further includes a third switching element Qc connected to the (i+2)-th gate line, e.g., the third gate line Gi+2, and an output terminal of the second switching element Qb of the first pixel.

**[0069]** The first pixel electrode PEa of the first pixel is connected to the first switching element Qa of the first pixel, and the second pixel electrode PEb of the first pixel is connected to the second switching element Qb of the first pixel through the third switching element Qc of the first pixel.

**[0070]** The second pixel PX(m, n+1) adjacent to the first pixel PX(m, n) in the pixel row direction includes a first switching element Qa connected to the i-th gate line, e.g., the first gate line Gi, and the (j+1)-th data line, e.g., the second data line Dj+1, a second switching element Qb connected to the (i+1)-th gate line, e.g., the second gate line Gi+1, and the (j+2)-th data line, e.g., the third data line Dj+2, and a first storage capacitor Csta connected to the first switching element Qa of the second pixel and a second storage capacitor Cstb connected to a second switching element Qb of the second pixel. In an exemplary embodiment, the second pixel PX(m, n+1) further includes a third switching element Qc connected to the (i+2)-th gate line, e.g., the third gate line Gi+2, and to an output terminal of the second switching element Qb of the second pixel.

**[0071]** The first pixel PX(m, n) and the second pixel PX(m, n+1) adjacent to each other in the pixel row direction are connected to the (j+1)-th data line, e.g., the second

data line Dj+1.

**[0072]** When the first gate line Gi receives a gate-on voltage, a first data voltage and a second data voltage are respectively applied to the first pixel PX(m, n) through the first switching element Qa of the first pixel that is thereby turned on and to the second pixel PX(m, n+1) through the first switching element Qa of the second pixel that is thereby turned on. That is, the first pixel electrode PEa of the first pixel PX(m, n) receives the first data voltage from the first data line Dj through the first switching element Qa of the first pixel and a point A of the first pixel thereby receives the first data voltage, and the first pixel electrode PEa of the second pixel PX(m, n+1) receives the second data voltage from the second data line Dj+1 through the first switching element Qa of the second pixel and a point A of the second pixel thereby receives the second data voltage.

**[0073]** When the first gate line Gi receives a gate-off voltage and the second gate line Gi+1 receives the gate-on voltage, the point A of the first pixel and the point A of the second pixel are floated, and a second data voltage is applied to the first pixel PX(m, n) through the second switching element of the first pixel that is thereby turned on, and a third data voltage is applied to the second pixel PX(m, n+1) through the second switching element of the second pixel that is thereby turned on. That is, the second pixel electrode PEb of the first pixel PX(m, n) and the second pixel electrode PEb of the second pixel PX(m, n+1) respectively receive second data voltages from the second data line Dj+1 through second switching element Qb of the first pixel and third data voltages from the third data line Dj+2 through the second switching element Qb of the second pixel.

**[0074]** When the second gate line Gi+1 receives the gate-off voltage and the third gate line Gi+2 receives the gate-on voltage, the output terminal of the second switching element Qb of the first pixel and the output terminal of the second switching element Qb of the second pixel are floated, and the third switching element Qc of the first pixel and the third switching element Qc of the second pixel are turned-on, and the first second data voltage and second third data voltage respectively charged and applied to the second pixel electrode PEb of the first pixel and to the second pixel electrode PEb of the second pixel are respectively transmitted to a point B of the first pixel through the third switching element Qc of the first pixel and to a point B of the second pixel through the third switching element Qc of the second pixel. Accordingly, voltages of predetermined magnitudes are charged between the point A and the point B of the first pixel forming two terminals of the liquid crystal capacitor Clc of the first pixel and between the point A and the point B of the second pixels forming two terminals of the liquid crystal capacitor Clc of the second pixels, respectively. In an exemplary embodiment, data voltages respectively applied to the two terminals of the liquid crystal capacitor Clc of the first and second pixel may correspond to luminances of the first pixel PX(m, n) and the second pixel PX(m,

n+1) to be displayed, and have opposite polarities with respect to the common voltage  $V_{com}$ . In an exemplary embodiment, data voltages applied to the first and second pixel electrodes PEa and PE of the first pixel and the first and second pixel electrodes PEa and PE of the second pixel may correspond to luminances of the pixel PX(m, n) and the second pixel PX(m, n+1) to be displayed and have opposite polarities with respect to the reference electrode  $V_{ref}$ . When the first data voltage applied to the first data line Dj is positive, the second data voltage applied to the second data line Dj+1 is negative and the third data voltage applied to the third data line Dj+2 is positive, and when the first data voltage applied to the first data line Dj is negative, the second data voltage applied to the second data line Dj+1 is positive and the third data voltage applied to the third data line Dj+2 is negative. As described above, the data lines of an exemplary embodiment of the liquid crystal display according to the present invention may be driven with a column inversion.

**[0075]** In a conventional liquid crystal display, when one terminal of a liquid crystal capacitor of the conventional liquid crystal display has been charged and thereby floated with one voltage, and the other terminal of the liquid crystal capacitor is being charged with another voltage having polarity opposite to a polarity of the one voltage, it is difficult for the liquid crystal capacitor of the conventional liquid crystal display to be charged with a predetermined magnitude. However, in an exemplary embodiment of the liquid crystal display according to the present invention, for example, the first and second data voltages respectively applied to the first and second pixel electrodes PEa and PEb of the first pixel through the first and second switching elements Qa and Qb of the first pixel during respective gate-on times is charged to the liquid crystal capacitor Clc of the first pixel through the output terminal of the first and second switching elements Qa and Qb of the first pixel that have been floated during a gate-off time. Accordingly, the liquid crystal capacitor Clc of the first pixel may be charged when the two terminals of the liquid crystal capacitor Clc are floated, and the first and second data voltages having opposite polarities may be charged with a predetermined magnitude.

**[0076]** An arrangement and driving method of signal lines and pixels of an exemplary embodiment of a liquid crystal display will be described hereafter with reference to FIG. 2 and FIG. 12. FIG. 12 is a schematic circuit diagram of an exemplary embodiment of a pixel of a liquid crystal display according to the present invention.

**[0077]** As shown in FIG. 12, an exemplary embodiment of the liquid crystal display includes a first pixel PX(m) and a second pixel PX(m+1) adjacent to each other in the pixel column direction, and gate lines, e.g., a first gate line Gi, a second gate line Gi+1, and a third gate line Gi+2, and pairs of data lines, e.g., a first pair of data lines Dj and Dj' and a second pair of data lines Dj+1, and Dj+1' connected thereto.

**[0078]** The first gate line Gi including a first upper line and a first lower line, the second gate line Gi+1 including

a second upper line and a second lower line, and the third gate line Gi+2 including a third upper line and a third lower line are disposed along the pixel column direction. The first pair of data lines Dj and Dj' including a first data line Dj and a second data line Dj', and the second pair of data lines Dj+1 and Dj+1' including a first data Dj+1 and a second data line Dj+1', are disposed along the pixel row.

**[0079]** The control terminal of the first switching element Qa of the first pixel PX(m) connected to the first pixel electrode PEa of the first pixel PX(m) is connected to the first upper line of the first gate line Gi, and the input terminal thereof is connected to one data line of the j-th pair of data lines, e.g., the second data line Dj' of the first pair of data lines Dj and Dj'. The control terminal of the second switching element Qb of the first pixel PX(m) connected to the second pixel electrode PEb of the first pixel PX(m) is connected to the second upper line of the second gate line Gi+1, and the input terminal thereof is connected to one data line of the (j+1)-th pair of data lines, e.g., the second data line Dj+1' of the second pair of data lines Dj+1 and Dj+1'. The input terminal of the third switching element Qc of the first pixel PX(m) connected to the output terminal of the second switching element Qb of the first pixel PX(m) is connected to the third upper line of the third gate line Gi+2.

**[0080]** The control terminal of the first switching element Qa of the second pixel PX(m+1) connected to the first pixel electrode PEa of the second pixel PX(m+1) is connected to the first lower line of the first gate line Gi, and the input terminal thereof is connected to one data line of the j-th pair of data lines, e.g. the first data line Dj of the first pair of data lines Dj and Dj'. The control terminal of the second switching element Qb of the second pixel PX(m+1) connected to the second pixel electrode PEb of the second pixel PX(m+1) is connected to the second lower line of the second gate line Gi+1, and the input terminal thereof is connected to one data line of the (j+1)-th pair of data lines, e.g., the first data line Dj+1 of the second pair of data lines Dj+1 and Dj+1'. The input terminal of the third switching element Qc of the second pixel PX(m+1) connected to the output terminal of the second switching element Qb of the second pixel PX(m+1) is connected to the third lower line of the third gate line Gi+2.

**[0081]** As described above, in an exemplary embodiment of a liquid crystal display, the control terminal of the first switching elements Qa of the first pixel PX(m) connected to the first pixel electrode PEa of the first pixel PX(m) and the control terminal of the first switching element Qa of the second pixel PX(m+1) connected to the first pixel electrode PEa of the second pixel PX(m+1) adjacent to the first pixel PX(m) in the pixel column direction are respectively connected to the first upper line and the first lower line of the first gate line Gi, and thereby receive the gate on/off voltages from one gate line, e.g., the first gate line Gi. The control terminal of the second switching element Qb of the first pixel PX(m) and the control terminal

of the second switching element Qb of the second pixel PX(m+1) are respectively connected to the second upper line and the second lower line of the same gate line Gi+1, and thereby receive the gate on/off voltages from one gate line, e.g., the second gate line Gi+1. The input terminal of the third switching element Qc of the first pixel (PX(m)) connected to the output terminal of the second switching element Qb of the first pixel PX(m) and the input terminal of the third switching element Qc of the second pixel PX(m+1) connected to the output terminal of the second switching element Qb of the second pixel PX(m+1) are respectively connected to the third upper line and the third lower line of the third gate line Gi+2, and thereby receive the gate on/off voltages from one gate line, e.g., the third gate line Gi+2. Accordingly, the driving speed is substantially increased.

**[0082]** An arrangement and a driving method of pixels and signal lines of a liquid crystal display will be described hereafter with reference to FIG. 2, FIG. 13 and FIG. 14.

**[0083]** FIG. 13 is a schematic circuit diagram of one pixel in a liquid crystal display not according to the present invention, and FIG. 14 is a signal timing diagram illustrating waveforms of a signal applied to the one pixel of the liquid crystal display in FIG. 13.

**[0084]** Referring back to FIG. 2 and as shown in FIG. 13, a liquid crystal display includes the first switching element Qa connected to the first pixel electrode PEa of the pixel PX, the second switching element Qb connected to the second pixel electrode PEb of the pixel PX, gate lines including a first gate line Gi and a second gate line Gi+1, and a data line Dj. The liquid crystal display includes the liquid crystal capacitor Clc and a step-up capacitor Cb connected to the first and second switching elements Qa and Qb. The control terminal of the first switching element Qa is connected to the first gate line Gi, and the input terminal thereof is connected to the data line Dj. The control terminal of the second switching element Qb is connected to the second gate line Gi+1, and the input terminal thereof is connected to the data line Dj. The output terminal of the first switching element Qa and the output terminals of second switching element Qb are connected to the liquid crystal capacitor Clc and the step-up capacitor Cb. Two terminals of the step-up capacitor Cb are connected to the first switching element Qa and the second switching element Qb.

**[0085]** A driving method of a liquid crystal display in FIG. 13 will be described hereafter with reference to FIG. 14.

**[0086]** Referring back to FIG. 13 and as shown in FIG. 14, when the first gate line Gi receives the gate-on signal and the first switching element Qa is thereby turned on, the first pixel electrode PEa receives one data voltage from the data line Dj and a point A is charged with the one data voltage.

**[0087]** When the first gate line Gi receives a gate-off signal, the second gate line Gi+1 receives a gate-on signal, and the second switching element Qb is thereby turned on, the second pixel electrode PEb receives other

data voltage through the data line Dj, and a point B is charged with the other data voltage. When a voltage of the point A Va is increased, a voltage of the point B Vb is thereby increased, and a voltage charged between the two terminals of the liquid crystal capacitor Clc connected to the point A and the point B is thereby changed and a magnitude of the charging voltage is thereby varied based on a capacity of the step-up capacitor Cb. Accordingly, by changing a capacity of the step-up capacitor Cb, the voltage charged to the liquid crystal capacitor Clc when the pixel receives two gate-on signals, is changed to have a predetermined magnitude.

**[0088]** In the liquid crystal display, the magnitude of the voltage charged to the liquid crystal capacitor may be changed by using two gate lines, one data line, and a step-up capacitor. Accordingly, compared to a liquid crystal display driven with one gate line and two data lines, a number of data lines is reduced, and the cost of the driver of the liquid crystal display is thereby substantially reduced.

**[0089]** Next, signal lines and a pixel arrangement of a liquid crystal display not according to the present invention will be described with reference to FIG. 15. FIG. 15 is a schematic circuit diagram of one pixel of a liquid crystal display not according to the present invention.

**[0090]** As shown in FIG. 15, an arrangement of a pixel and signal lines of the liquid crystal display is substantially similar to the liquid crystal display in FIG. 13 except for a fourth switching element Qd connected to the first gate line Gi and the point B of the step-up capacitor Cb. The control terminal of the fourth switching element Qd is connected to the first gate line Gi, and the input terminal thereof is connected to a common voltage point Vcom. Accordingly, when the first gate line Gi receives the gate-on signal such that the first pixel electrode PEa of the pixel PX receives a data voltage, the point B of the step-up capacitor Cb and one terminal of the liquid crystal capacitor Clc are changed with the common voltage Vcom. The point B of the step-up capacitor Cb and the one terminal of the liquid crystal capacitor Clc is refreshed by being charged with the common voltage Vcom which is the reference voltage to the point B of the step-up capacitor Cb and the one terminal of the liquid crystal capacitor Clc, and thereby minimize an influence of the voltages charged during a previous frame to the point B of the step-up capacitor Cb and the one terminal of the liquid crystal capacitor Clc.

**[0091]** According to exemplary embodiments of the present invention as described herein provide advantages which include, but are not limited to, a high contrast ratio and a wide viewing angle, fast response speed of the liquid crystal, and a low manufacturing cost by substantially reducing number of signal lines in a liquid crystal display.

**[0092]** The present invention should not be construed as being limited to the exemplary embodiments set forth herein. Rather, these exemplary embodiments are provided so that this disclosure will be thorough and com-

plete and will fully convey the concept of the present invention to those skilled in the art.

**[0093]** While the present invention has been particularly shown and described with reference to exemplary embodiments thereof, it will be understood by those of ordinary skill in the art that various changes in form and details may be made therein without departing from the scope of the present invention which is defined by the following claims.

## Claims

### 1. A liquid crystal display comprising:

a first substrate (100);  
 a second substrate (200) disposed opposite to the first substrate (100);  
 a liquid crystal layer (3) interposed between the first and second substrates (100; 200) and including liquid crystal molecules (31);  
 a first gate line (Gi) disposed on the first substrate (100) and which is adapted to transmit a first gate signal;  
 a second gate line (Gi+1) disposed on the first substrate (100) and which is adapted to transmit a second gate signal;  
 a third gate line (Gi+2) disposed on the first substrate (100) and which is adapted to transmit a third gate signal;  
 a first data line (Dj) disposed on the first substrate (100);  
 a second data line (Dj+1) disposed on the first substrate (100);  
 and a pixel (Px), the pixel (Px) comprising:

a first switching element (Qa) connected to the first gate line (Gi) and the first data line (Dj);  
 a second switching element (Qb) connected to the second gate line (Gi+1) and the second data line (Dj+1);

a third switching element (Qc) connected to the third gate line (Gi+2) and an output terminal of the second switching element (Qb);  
 a storage capacitor (Cstb) connected to the output terminal of second switching element (Qb);  
 and

a first pixel electrode (PEa) connected to the first switching element (Qa) and a second pixel electrode (PEb) connected to the second switching element (Qb) through the third switching element (Qc) and separated from the first pixel electrode (PEa),

wherein an input terminal of the third switching element (Qc) is connected to the output terminal of the second switching element (Qb), an output

terminal of the third switching element (Qc) is connected to the second pixel electrode (PEb), and

the first pixel electrode (PEa) and the second pixel electrode (PEb) and the liquid crystal layer (3) between the first pixel electrode (PEa) and the second pixel electrode (PEb) form a first liquid crystal capacitor (Clc).

2. The liquid crystal display of claim 1, wherein the first pixel electrode (PEa) includes first branches, the second pixel electrode (PEb) includes second branches, and the first branches of the first pixel electrode (PEa) and the second branches of the second pixel electrode (PEb) are alternately disposed on the first substrate (100).

3. The liquid crystal display of claim 1 or 2, wherein the first gate line (Gi) is adapted to receive a gate-on signal, and the first pixel electrode (PEa) is adapted to receive a first data voltage from the first data line (Dj) through the first switching element (Qa), and the second gate line (Gi+1) is adapted to receive the gate-on signal, and the second pixel electrode (PEb) is adapted to receive a second data voltage from the second data line (Dj+1) through the second switching element (Qb) and the third switching element (Qc), wherein the first data voltage and the second data voltage have different polarities, and the third gate line (Gi+2) is adapted to receive the gate on signal, wherein the second data voltage is transmitted through the third switching element (Qc).

4. The liquid crystal display of claim 1 or 2, further comprising:

a fourth gate line disposed on the first substrate (100);  
 a fifth gate line disposed on the first substrate (100);  
 a sixth gate line disposed on the first substrate (100);  
 a third data line (D'<sub>j</sub>) disposed on the first substrate (100);  
 a fourth (D'<sub>j+1</sub>) data line disposed on the first substrate (100);  
 and a second pixel (Px) adjacent to the first pixel in a same column, the second pixel (Px) comprising:

a fourth switching element (Q<sub>A</sub>) connected to the fourth gate line and the third data line (D'<sub>j</sub>);  
 a fifth switching element (Q<sub>B</sub>) connected to the fifth gate line and the fourth data line (D'<sub>j+1</sub>);

- a sixth switching element ( $Q_C$ ) connected to the sixth gate line and an output terminal of the fifth switching element ( $Q_B$ ), and a third pixel electrode connected to the fourth switching element ( $Q_A$ ) and a fourth pixel electrode connected to the fifth switching element ( $Q_B$ ) through the sixth switching element ( $Q_C$ ) and separated from the third pixel electrode, wherein the fourth gate line is parallel connected to the first gate line ( $G_i$ ) and transmits the first gate signal, the fifth gate line is parallel connected to the second gate line ( $G_{i+1}$ ) and transmits the second gate signal, the sixth gate line is parallel connected to the third gate line ( $G_{i+2}$ ) and transmits the third gate signal, and the third pixel electrode and the fourth pixel electrode and the liquid crystal layer (3) between the third pixel electrode and the fourth pixel electrode form a second liquid crystal capacitor ( $Clc$ ).
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5. The liquid crystal display of claim 4, wherein the first data line ( $D_j$ ) and the third data line ( $D'_j$ ) are disposed adjacent to each other, and the second data line ( $D_{j+1}$ ) and the fourth data ( $D'_{j+1}$ ) line are disposed adjacent to each other.
6. The liquid crystal display of claim 5, wherein the third pixel electrode includes third branches, the fourth pixel electrode includes fourth branches, and the third branches of the third pixel electrode and the fourth branches of the fourth pixel electrode are alternately disposed on the first substrate (100).

#### Patentansprüche

1. Flüssigkristall-Display, das Folgendes umfasst:

ein erstes Substrat (100);  
 ein zweites Substrat (200), das gegenüber dem ersten Substrat (100) angeordnet ist;  
 eine Flüssigkristallschicht (3), die zwischen dem ersten und dem zweiten Substrat (100; 200) eingefügt ist und Flüssigkristallmoleküle (31) umfasst;  
 eine erste Gate-Leitung ( $G_i$ ), die am ersten Substrat (100) angeordnet und dazu geeignet ist, ein erstes Gate-Signal zu übertragen;  
 eine zweite Gate-Leitung ( $G_{i+1}$ ), die am ersten Substrat (100) angeordnet und dazu geeignet ist, ein zweites Gate-Signal zu übertragen;  
 eine dritte Gate-Leitung ( $G_{i+2}$ ), die am ersten Substrat (100) angeordnet und dazu geeignet

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ist, ein drittes Gate-Signal zu übertragen;  
 eine erste Datenleitung ( $D_j$ ), die am ersten Substrat (100) angeordnet ist;  
 eine zweite Datenleitung ( $D_{j+1}$ ), die am ersten Substrat (100) angeordnet ist;  
 und ein Pixel ( $P_x$ ), wobei das Pixel ( $P_x$ ) Folgendes umfasst:

ein erstes Schaltelement ( $Q_a$ ), das mit der ersten Gate-Leitung ( $G_i$ ) und der ersten Datenleitung ( $D_j$ ) verbunden ist;  
 ein zweites Schaltelement ( $Q_b$ ), das mit der zweiten Gate-Leitung ( $G_{i+1}$ ) und der zweiten Datenleitung ( $D_{j+1}$ ) verbunden ist;  
 ein drittes Schaltelement ( $Q_c$ ), das mit der dritten Gate-Leitung ( $G_{i+2}$ ) und einem Ausgangsanschluss des zweiten Schaltelements ( $Q_b$ ) verbunden ist;  
 einen Speicherkondensator ( $C_{stb}$ ), der mit dem Ausgangsanschluss des zweiten Schaltelements ( $Q_b$ ) verbunden ist; und  
 eine erste Pixelelektrode ( $PE_a$ ), die mit dem ersten Schaltelement ( $Q_a$ ) verbunden ist, und eine zweite Pixelelektrode ( $PE_b$ ), die mit dem zweiten Schaltelement ( $Q_b$ ) durch das dritte Schaltelement ( $Q_c$ ) verbunden und von der ersten Pixelelektrode ( $PE_a$ ) getrennt ist, wobei ein Eingangsanschluss des dritten Schaltelements ( $Q_c$ ) mit dem Ausgangsanschluss des zweiten Schaltelements ( $Q_b$ ) verbunden ist, ein Ausgangsanschluss des dritten Schaltelements ( $Q_c$ ) mit der zweiten Pixelelektrode ( $PE_b$ ) verbunden ist, und die erste Pixelelektrode ( $PE_a$ ) und die zweite Pixelelektrode ( $PE_b$ ) und die Flüssigkristallschicht (3) zwischen der ersten Pixelelektrode ( $PE_a$ ) und der zweiten Pixelelektrode ( $PE_b$ ) einen ersten Flüssigkristallkondensator ( $Clc$ ) bilden.

2. Flüssigkristall-Display gemäß Anspruch 1, wobei die erste Pixelelektrode ( $PE_a$ ) erste Verzweigungen umfasst, die zweite Pixelelektrode ( $PE_b$ ) zweite Verzweigungen umfasst, und die ersten Verzweigungen der ersten Pixelelektrode ( $PE_a$ ) und die zweiten Verzweigungen der zweiten Pixelelektrode ( $PE_b$ ) abwechselnd am ersten Substrat (100) angeordnet sind.
3. Flüssigkristall-Display gemäß Anspruch 1 oder 2, wobei die erste Gate-Leitung ( $G_i$ ) dazu geeignet ist, ein Gate-on-Signal zu empfangen, und die erste Pixelelektrode ( $PE_a$ ) dazu geeignet ist, eine erste Datenspannung von der ersten Datenleitung ( $D_j$ ) über das erste Schaltelement ( $Q_a$ ) zu empfangen, und die zweite Gate-Leitung ( $G_{i+1}$ ) dazu geeignet ist,

das Gate-on-Signal zu empfangen, und die zweite Pixelelektrode (PEb) dazu geeignet ist, eine zweite Datenspannung von der zweiten Datenleitung (Dj+1) über das zweite Schaltelement (Qb) und das dritte Schaltelement (Qc) zu empfangen, wobei die erste Datenspannung und die zweite Datenspannung unterschiedliche Polaritäten aufweisen, und die dritte Gate-Leitung (Gi+2) dazu geeignet ist, das Gate-on-Signal zu empfangen, wobei die zweite Datenspannung durch das dritte Schaltelement (Qc) übertragen wird.

4. Flüssigkristall-Display gemäß Anspruch 1 oder 2, ferner umfassend:

eine vierte Gate-Leitung, die am ersten Substrat (100) angeordnet ist;  
 eine fünfte Gate-Leitung, die am ersten Substrat (100) angeordnet ist;  
 eine sechste Gate Leitung, die am ersten Substrat (100) angeordnet ist;  
 eine dritte Datenleitung (D'j), die am ersten Substrat (100) angeordnet ist;  
 eine vierte Datenleitung (D'j +1), die am ersten Substrat (100) angeordnet ist; und  
 ein zweites Pixel (Px) angrenzend an das erste Pixel in einer gleichen Spalte, wobei das zweite Pixel (Px) Folgendes umfasst:

ein viertes Schaltelement (QA), das mit der vierten Gate-Leitung und der dritten Datenleitung (D'j) verbunden ist;  
 ein fünftes Schaltelement (QB), das mit der fünften Gate-Leitung und der vierten Datenleitung (D'j+1) verbunden ist;  
 ein sechstes Schaltelement (QC), das mit der sechsten Gate-Leitung und einem Ausgangsanschluss des fünften Schaltelements (QB) verbunden ist; und  
 eine dritte Pixelelektrode, die mit dem vierten Schaltelement (QA) verbunden ist, und eine vierte Pixelelektrode, die mit dem fünften Schaltelement (QB) durch das sechste Schaltelement (QC) verbunden und von der dritten Pixelelektrode getrennt ist, wobei die vierte Gate-Leitung parallel mit der ersten Gate-Leitung (Gi) verbunden ist und das erste Gate-Signal überträgt.  
 die fünfte Gate-Leitung parallel mit der zweiten Gate-Leitung (Gi+1) verbunden ist und das zweite Gate-Signal überträgt,  
 die sechste Gate-Leitung parallel mit der dritten Gate-Leitung (Gi+2) verbunden ist und das dritte Gate-Signal überträgt, und die dritte Pixelelektrode und die vierte Pixelelektrode und die Flüssigkristallschicht (3) zwischen der dritten Pixelelektrode und

der vierten Pixelelektrode einen zweiten Flüssigkristallkondensator (Clc) bilden.

5. Flüssigkristall-Display gemäß Anspruch 4, wobei die erste Datenleitung (Dj) und die dritte Datenleitung (D'j) angrenzend aneinander angeordnet sind, und die zweite Datenleitung (Dj+1) und die vierte Datenleitung (D'j+1) angrenzend aneinander angeordnet sind.
6. Flüssigkristall-Display gemäß Anspruch 5, wobei die dritte Pixelelektrode dritte Verzweigungen umfasst, die vierte Pixelelektrode vierte Verzweigungen umfasst, und die dritten Verzweigungen der dritten Pixelelektrode und die vierten Verzweigungen der vierten Pixelelektrode abwechselnd am ersten Substrat (100) angeordnet sind.

#### Revendications

1. Affichage à cristaux liquides comprenant :

un premier substrat (100) ;  
 un deuxième substrat (200) disposé en face du premier substrat (100) ;  
 une couche de cristaux liquides (3) interposée entre le premier substrat et le deuxième (100 ; 200) et contenant des molécules de cristaux liquides (31) ;  
 une première ligne de grille (Gi) disposée sur le premier substrat (100) et adaptée pour transmettre un premier signal de grille ;  
 une deuxième ligne de grille (Gi+1) disposée sur le premier substrat (100) et adaptée pour transmettre un deuxième signal de grille ;  
 une troisième ligne de grille (Gi+2) disposée sur le premier substrat (100) et adaptée pour transmettre un troisième signal de grille ;  
 une première ligne de données (Dj) disposée sur le premier substrat (100) ;  
 une deuxième ligne de données (Dj+1) disposée sur le premier substrat (100) ;  
 et un pixel (Px), le pixel (Px) comprenant :

un premier élément de commutation (Qa) connecté à la première ligne de grille (Gi) et à la première ligne de données (Dj) ;  
 un deuxième élément de commutation (Qb) connecté à la deuxième ligne de grille (Gi+1) et à la deuxième ligne de données (Dj+1) ;  
 un troisième élément de commutation (Qc) connecté à la troisième ligne de grille (Gi+2) et à une borne de sortie du deuxième élé-

- ment de commutation ( $Q_b$ ) ;  
 une capacité de stockage ( $C_{stb}$ ) connectée à la borne de sortie du deuxième élément de commutation ( $Q_b$ ) ; et  
 une première électrode de pixel (PEa) connectée au premier élément de commutation ( $Q_a$ ) et une deuxième électrode de pixel (PEb) connectée au deuxième élément de commutation ( $Q_b$ ) via le troisième élément de commutation ( $Q_c$ ) et séparée de la première électrode de pixel (PEa),  
 une borne d'entrée du troisième élément de commutation ( $Q_c$ ) étant connectée à la borne de sortie du deuxième élément de commutation ( $Q_b$ ), une borne de sortie du troisième élément de commutation ( $Q_c$ ) étant connectée à la deuxième électrode de pixel (PEb), et  
 la première électrode de pixel (PEa) et la deuxième électrode de pixel (PEb) et la couche de cristaux liquides (3) entre la première électrode de pixel (PEa) et la deuxième électrode de pixel (PEb) forment une première capacité à cristaux liquides (Clc).
2. Affichage à cristaux liquides selon la revendication 1, dans lequel  
 la première électrode de pixel (PEa) comprend des premières branches ; la deuxième électrode de pixel (PEb) comprend des deuxième branches, et les premières branches de la première électrode de pixel (PEa) et les deuxième branches de la deuxième électrode de pixel (PEb) sont disposées alternativement sur le premier substrat (100).
3. Affichage à cristaux liquides selon la revendication 1 ou 2, dans lequel  
 la première ligne de grille ( $G_i$ ) est adaptée pour recevoir un signal de grille active et la première électrode de pixel (PEa) est adaptée pour recevoir une première tension de données de la première ligne de données ( $D_j$ ) via le premier élément de commutation ( $Q_a$ ), et  
 la deuxième ligne de grille ( $G_{i+1}$ ) est adaptée pour recevoir le signal d'activation de grille et la deuxième électrode de pixel (PEb) est adaptée pour recevoir une deuxième tension de données de la deuxième ligne de données ( $D_{j+1}$ ) via le deuxième élément de commutation ( $Q_b$ ) et le troisième élément de commutation ( $Q_c$ ),  
 la première tension de données et la deuxième tension de données ayant des polarités différentes, et la troisième ligne de grille ( $G_{i+2}$ ) est adaptée pour recevoir le signal d'activation de grille, la deuxième tension de données étant transmise via le troisième élément de commutation ( $Q_c$ ).
4. Affichage à cristaux liquides selon la revendication

1 ou 2, comprenant en outre :

une quatrième ligne de grille disposée sur le premier substrat (100) ;  
 une cinquième ligne de grille disposée sur le premier substrat (100) ;  
 une sixième ligne de grille disposée sur le premier substrat (100) ;  
 une troisième ligne de données ( $D_{j'}$ ) disposée sur le premier substrat (100) ;  
 une quatrième ligne de données ( $D_{j'+1}$ ) disposée sur le premier substrat (100) ;  
 et un deuxième pixel ( $P_x$ ) adjacent au premier pixel dans une même colonne, lequel deuxième pixel ( $P_x$ ) comprend :

un quatrième élément de commutation ( $Q_A$ ) connecté à la quatrième ligne de grille et à la troisième ligne de données ( $D_{j'}$ ) ;  
 un cinquième élément de commutation ( $Q_B$ ) connecté à la cinquième ligne de grille et à la quatrième ligne de données ( $D_{j'+1}$ ) ;  
 un sixième élément de commutation ( $Q_C$ ) connecté à la sixième ligne de grille et à une borne de sortie du cinquième élément de commutation ( $Q_B$ ) ; et  
 une troisième électrode de pixel connectée au quatrième élément de commutation ( $Q_A$ ) et une quatrième électrode de pixel connectée au cinquième élément de commutation ( $Q_B$ ) via le sixième élément de commutation ( $Q_C$ ) et séparée de la troisième électrode de pixel,  
 la quatrième ligne de grille étant montée en parallèle avec la première ligne de grille ( $G_i$ ) et transmettant le premier signal de grille, la cinquième ligne de grille étant montée en parallèle avec la deuxième ligne de grille ( $G_{i+1}$ ) et transmettant le deuxième signal de grille,  
 la sixième ligne de grille étant montée en parallèle avec la troisième ligne de grille ( $G_{i+2}$ ) et transmettant le troisième signal de grille, et  
 la troisième électrode de pixel et la quatrième électrode de pixel et la couche de cristaux liquides (3) entre la troisième électrode de pixel et la quatrième électrode de pixel formant une capacité à cristaux liquides (Clc).

5. Affichage à cristaux liquides selon la revendication 4, dans lequel  
 la première ligne de données ( $D_j$ ) et la troisième ligne de données ( $D_{j'}$ ) sont adjacentes l'une à l'autre, et la deuxième ligne de données ( $D_{j+1}$ ) et la quatrième ligne de données ( $D_{j'+1}$ ) sont adjacentes l'une à l'autre.

6. Affichage à cristaux liquides selon la revendication 5, dans lequel la troisième électrode de pixel comprend des troisièmes branches, la quatrième électrode de pixel comprend des quatrièmes branches, et les troisièmes branches de la troisième électrode de pixel et les quatrièmes branches de la quatrième électrode de pixel sont disposées alternativement sur le premier substrat (100).

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FIG. 1

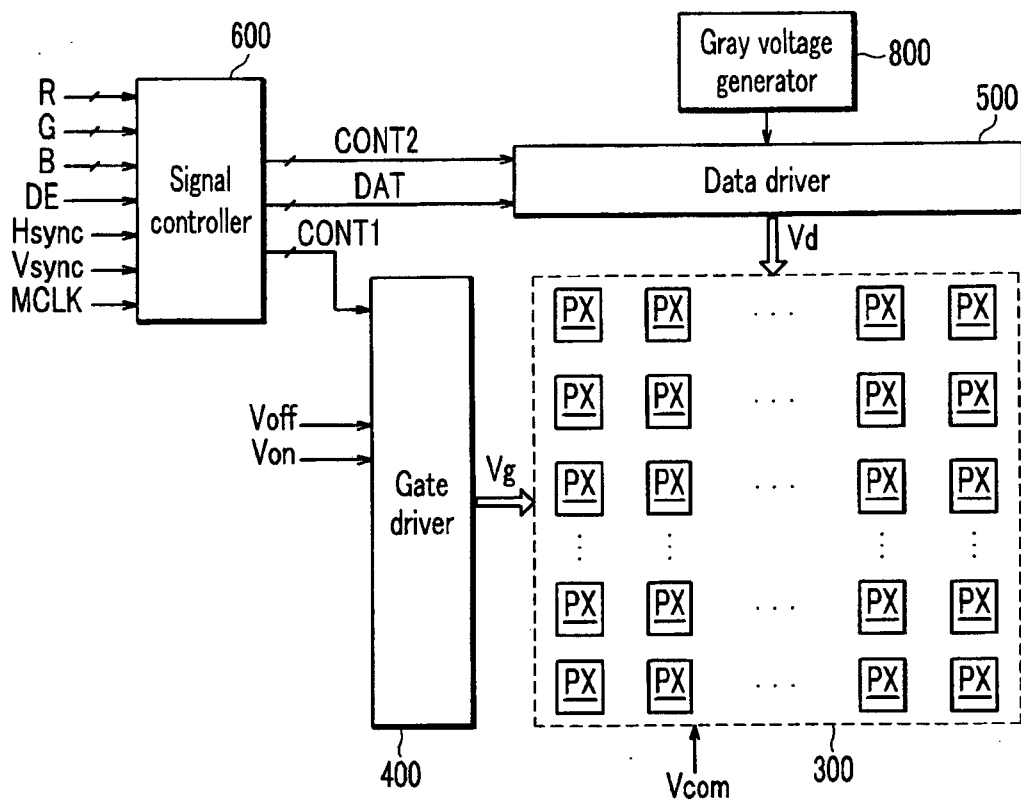


FIG. 2

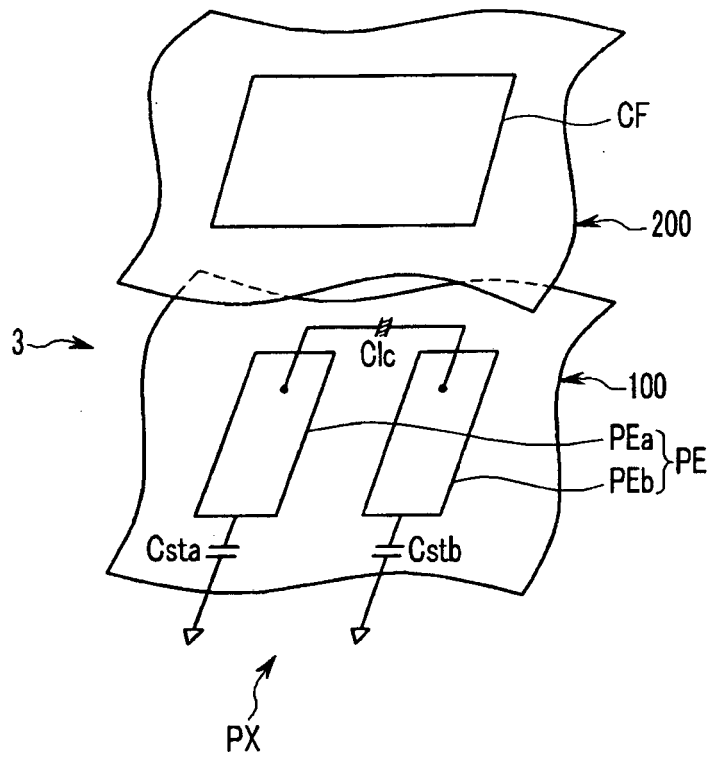


FIG. 3

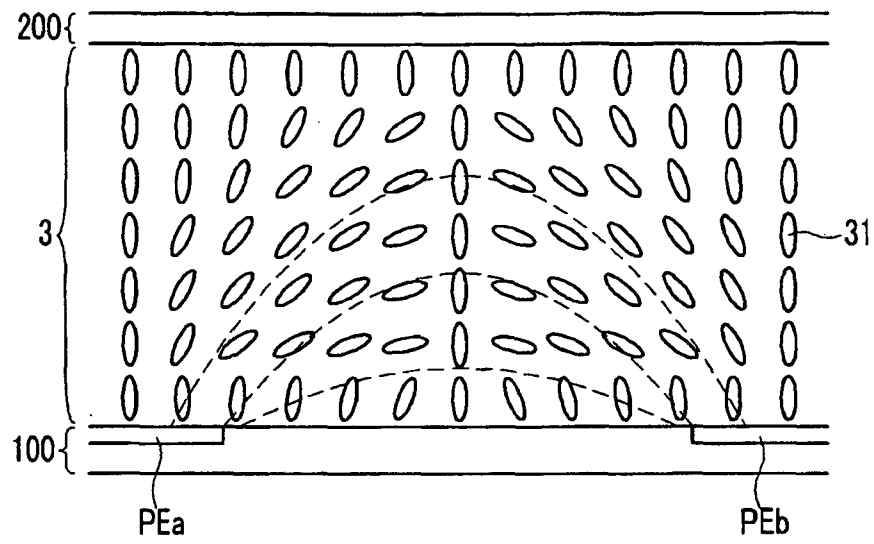


FIG. 4

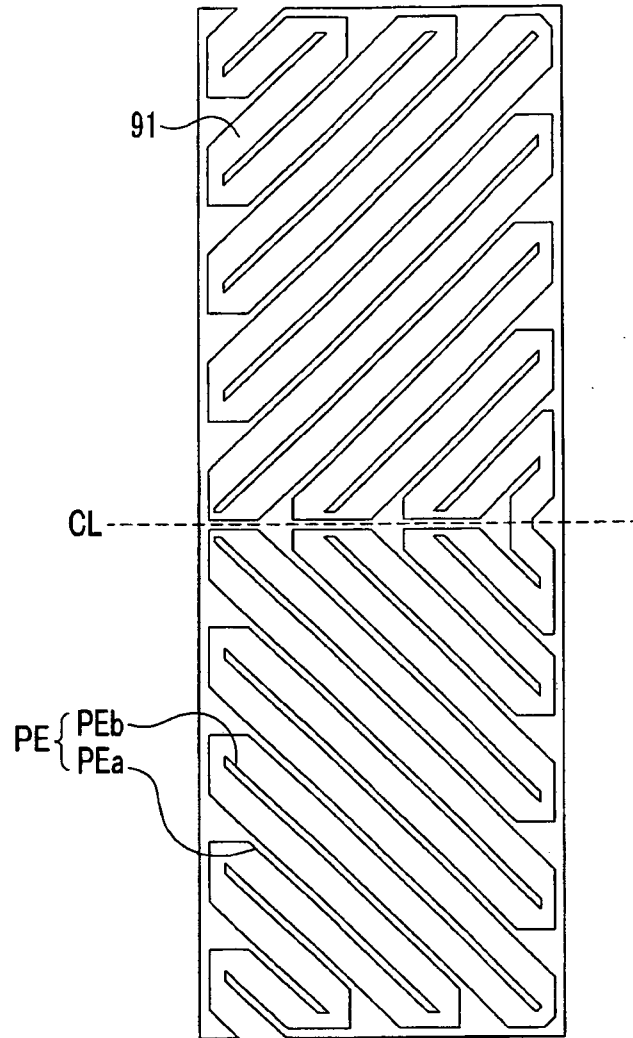


FIG. 5

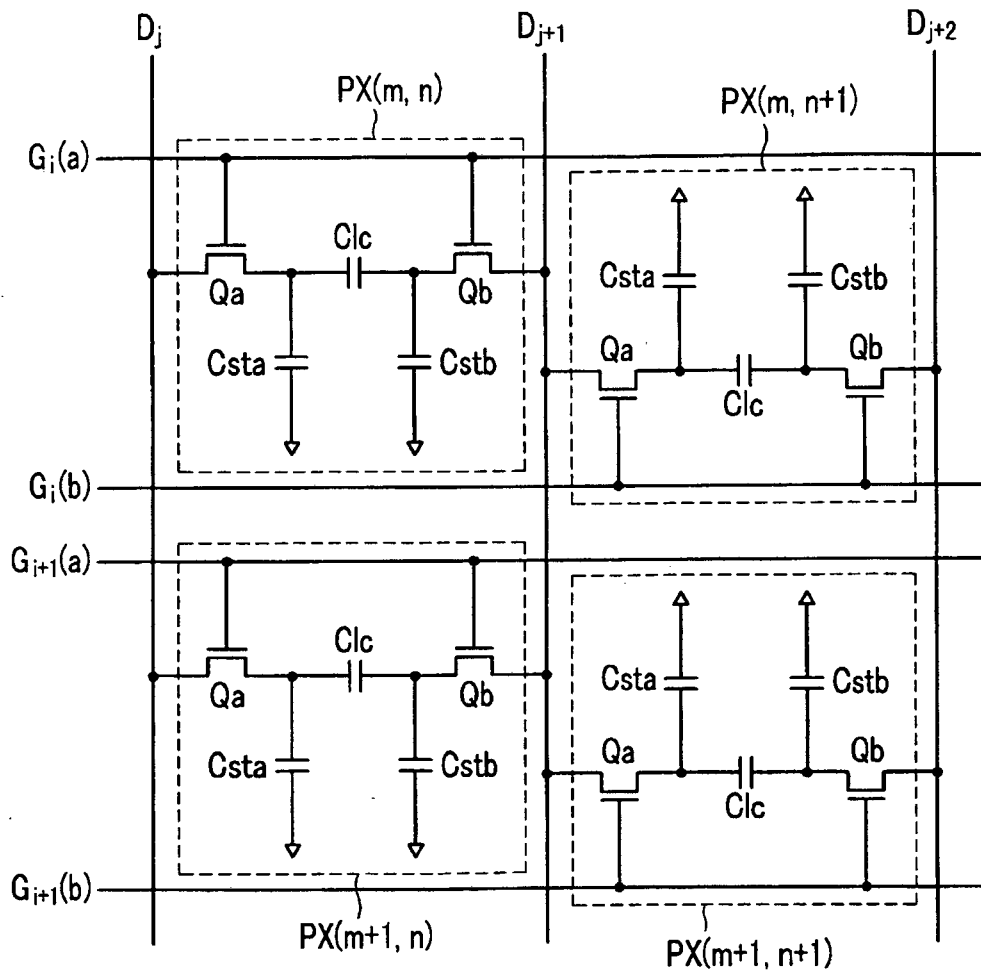


FIG. 6

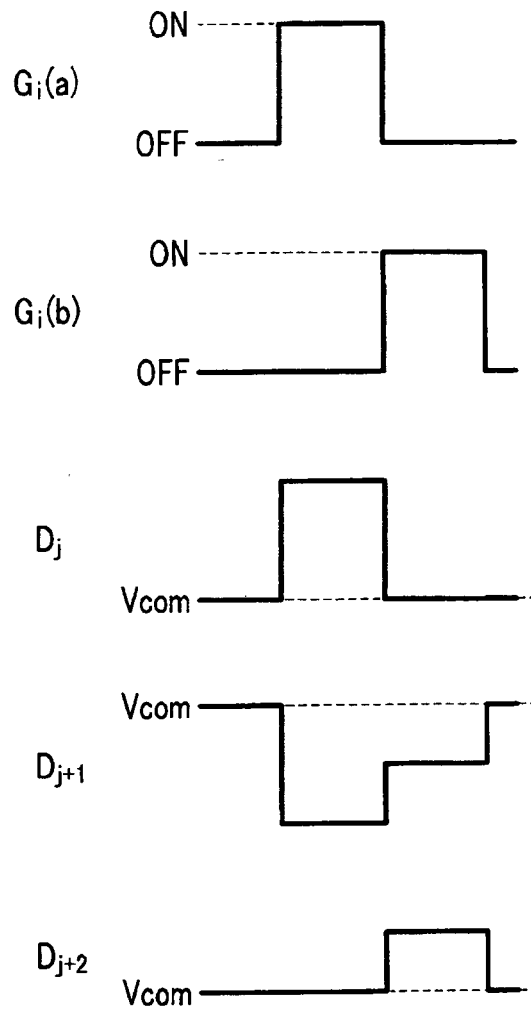


FIG. 7

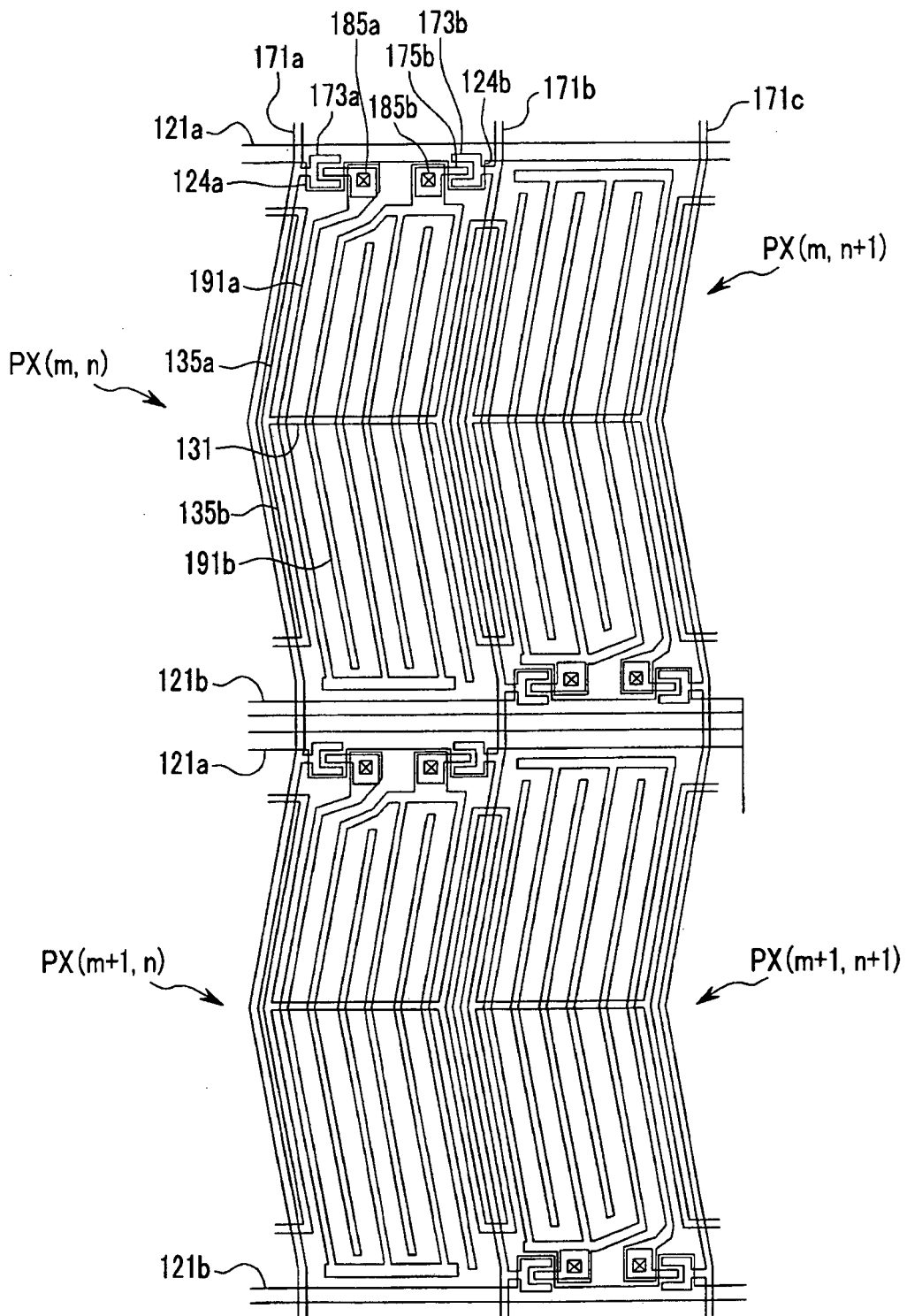


FIG. 8

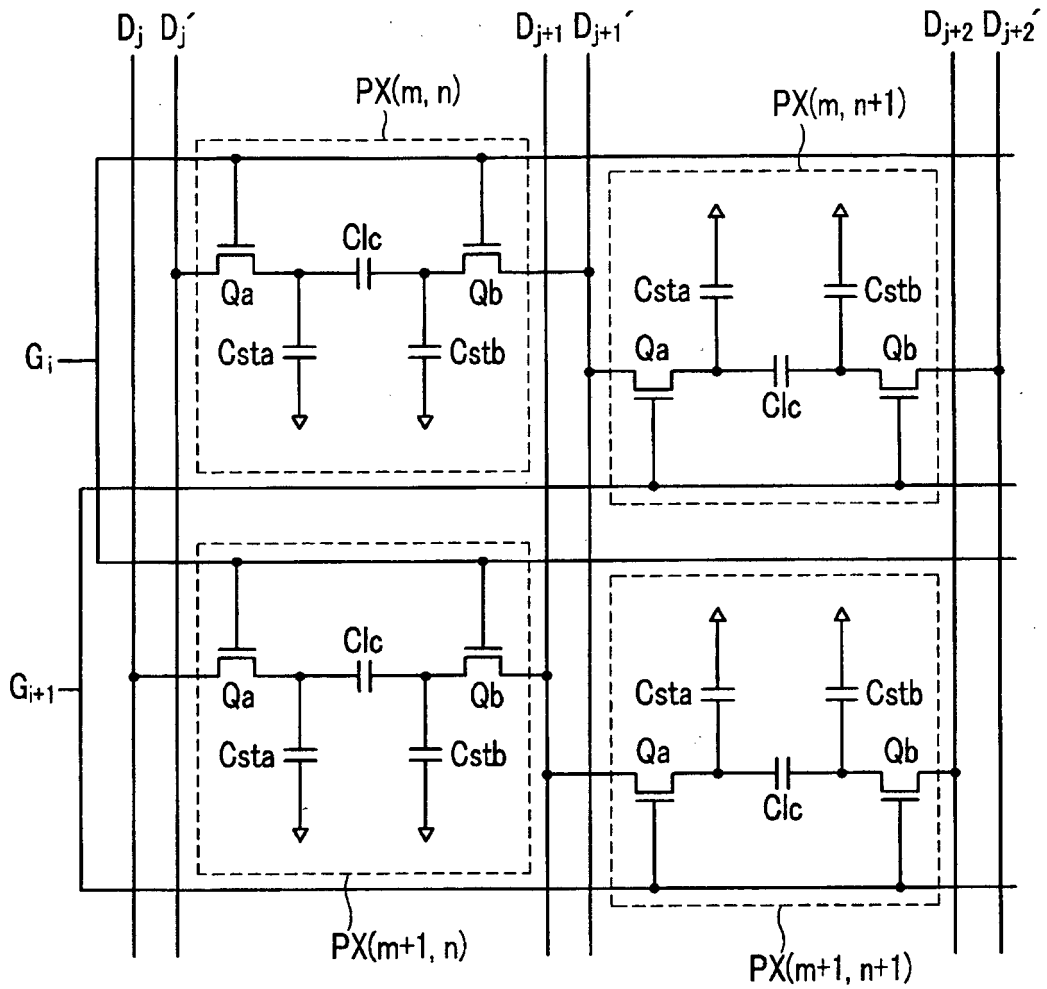


FIG. 9

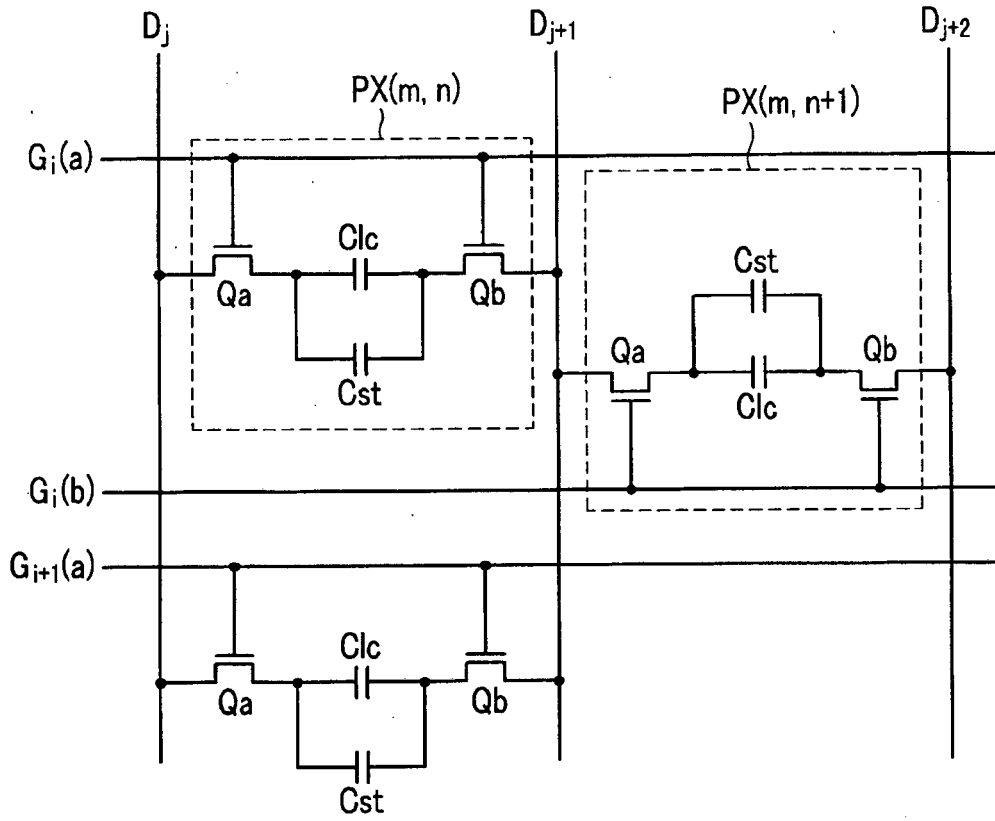


FIG. 10

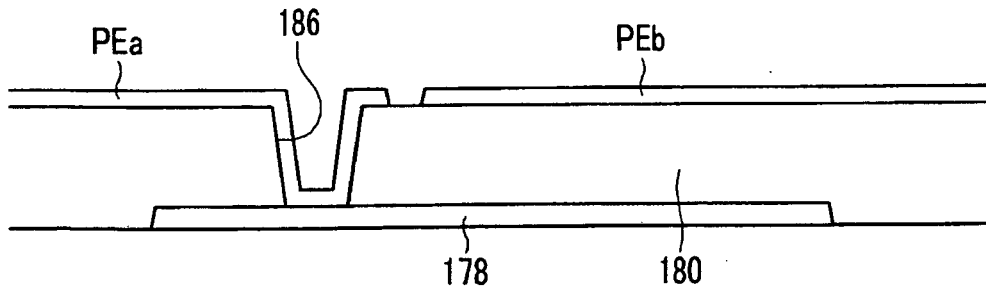


FIG. 11

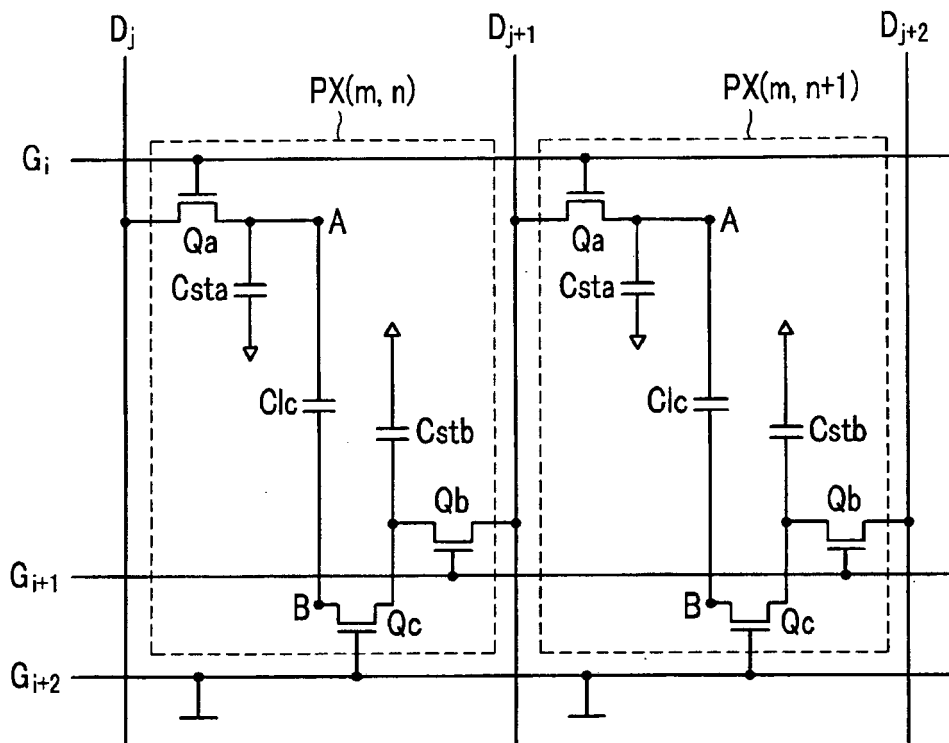


FIG. 12

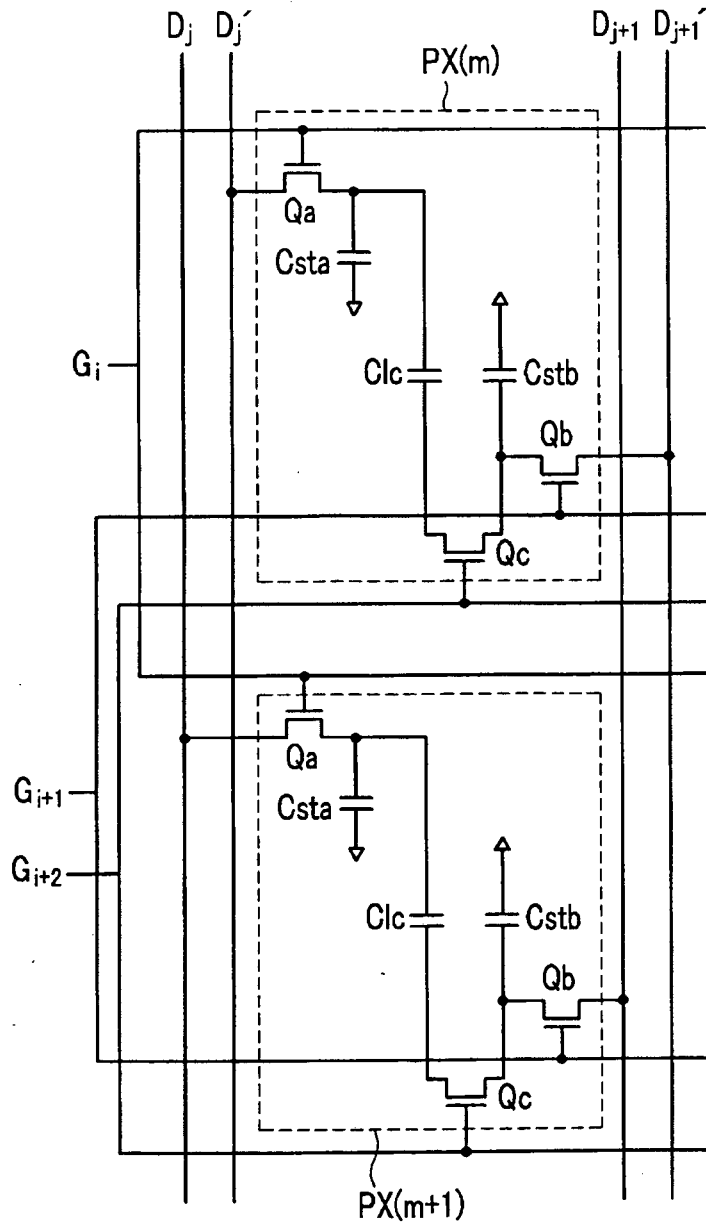


FIG. 13

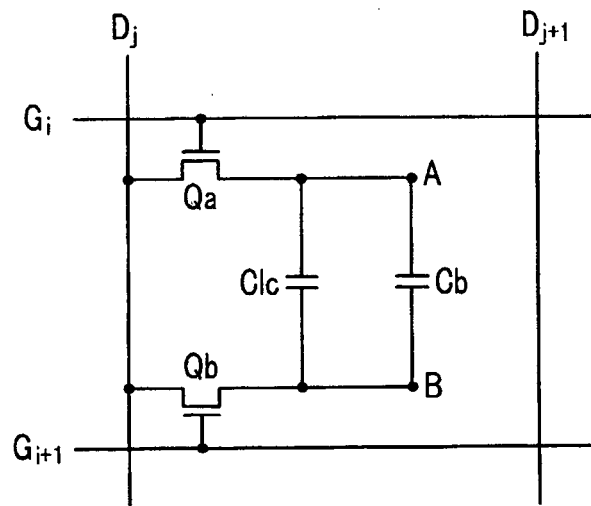


FIG. 14

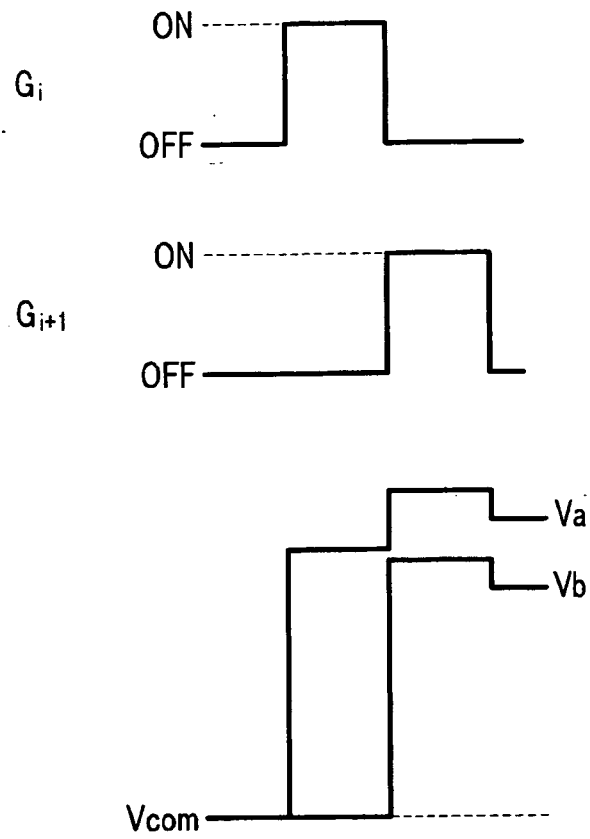
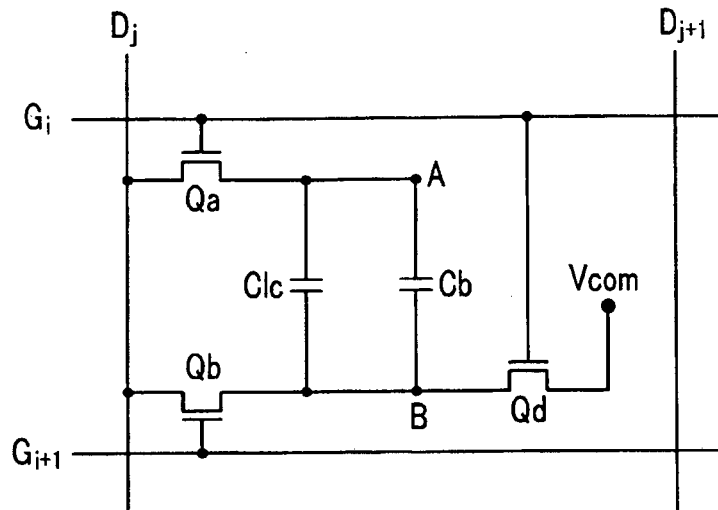


FIG. 15



**REFERENCES CITED IN THE DESCRIPTION**

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- US 20060215066 A [0007]
- WO 2004086129 A [0008]

专利名称(译)	液晶显示器		
公开(公告)号	<a href="#">EP2365387B1</a>	公开(公告)日	2014-03-12
申请号	EP2011002347	申请日	2010-01-27
[标]申请(专利权)人(译)	三星电子株式会社		
申请(专利权)人(译)	SAMSUNG ELECTRONICS CO. , LTD.		
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外部链接	<a href="#">Espacenet</a>		

摘要(译)

一种液晶显示器, 包括: 第一基板和与第一基板相对设置的第二基板;液晶层夹在第一和第二基板之间并包括液晶分子;第一栅极线, 设置在第一基板上并传输第一栅极信号;第二栅极线, 设置在第一基板上并传输第二栅极信号;第三栅极线, 设置在第一基板上并传输第三栅极信号;第一数据线设置在第一基板上, 第二数据线设置在第一基板上, 像素包括: 第一开关元件, 连接到第一栅极线和第一数据线;连接的第二开关元件到第二栅极线和第二数据线;第三开关元件, 连接到第三栅极线, 第二开关元件的输出端子;连接到第二开关元件的存储电容器和连接到第一开关元件的第一像素电极和通过第三开关元件连接到第二开关元件并与第一像素电极分开的第二像素电极, 其中输入端子第三开关元件连接第二开关元件的输出端, 第三开关元件的输出端连接第二像素电极, 第一像素电极和第二像素电极形成第一液晶电容。

FIG. 1

