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## (54) Liquid crystal display panel with charge sharing scheme

(57) A LCD panel in which a pixel has a first sub-pixel area and a second sub-pixel area, each area having a storage capacitor. Each pixel has a first gate line for providing a first gate-line signal for charging the first and second storage capacitors, and a second gate line for providing a second gate-line signal for removing part of the charges in the second storage capacitor to a third capacitor after the first gate-line signal has passed. The width of the first and second gate-line signals and their timing can be varied so that the first gate-line signal provided to a row can be used as the second gate-line signal to one of the preceding rows. In some embodiments, a pixel in each row has a duplicate pixel arranged to similarly receive the first and second gate-line signals, but data signals are received from different data lines.

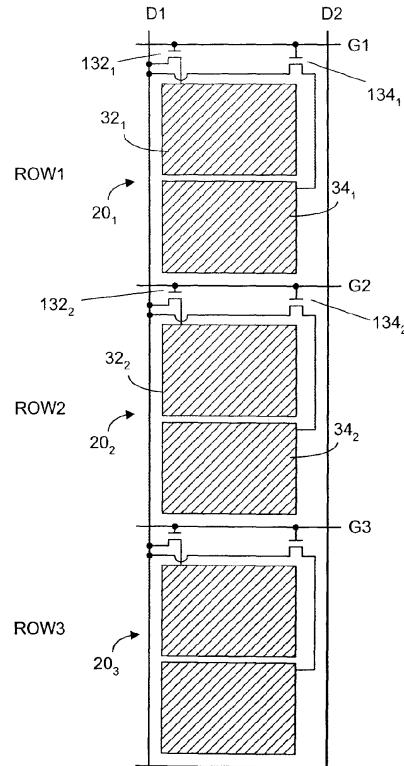


FIG.4

**Description**Field of the Invention

**[0001]** The present invention relates generally to a liquid crystal display (LCD) panel and, more particularly, to a method for driving rows of pixels in an LCD panel.

Background of the Invention

**[0002]** A typical liquid crystal display (LCD) panel has a plurality of pixels arranged in a two-dimensional array, driven by a data driver and a gate driver. As shown in Figure 1, the LCD pixels **10** in a LCD panel **1** are arranged in rows and columns in a display area **100**. A data driver **200** is used to provide a signal indicative of data to each of the columns and a gate driver is used to provide a gate line signal to each of the rows. In a color LCD panel, an image is generally presented in three colors: red (**R**), green (**G**) and blue (**B**). Each of the pixels **10** is typically divided into three color sub-pixels: red sub-pixel **20R**, green sub-pixel **20G** and blue sub-pixel **20B**, as shown in Figure 2. A data line **221** is used to provide the data signal to the **R** sub-pixel in a column, a data line **222** is used to provide the data signal to the **G** sub-pixel in the same pixel column, and a data line **223** is used to provide the data signal to the **B** sub-pixel in the same pixel column. The data line **224** is used to provide the data signal to the **R** sub-pixel in the next pixel column. A gate line **231** is used to provide the gate line signal to all sub-pixels in a row and a gate line **232** is used to provide the gate line signal to all sub-pixels in the next row. In a transflective LCD panel, each of the color sub-pixels may be further divided into a transmissive area and a reflective area.

**[0003]** A typical LCD panel is fabricated with two substrates. As shown in Figure 3, the LCD panel has an upper substrate **12** and a lower substrate **18** and a liquid crystal layer disposed between the substrates. On the upper substrate **12**, a transparent, electrically conducting layer **14** is provided as a common electrode. In each of the color sub-pixels **20**, an electrically conducting layer is disposed on the lower substrate **18** as a pixel electrode. The LCD panel also comprises an electronic component layer **17** for controlling the voltage between the common electrode and the pixel electrode. The common electrode is usually connected to a common ground or a common voltage source **COM**.

Summary of the Invention

**[0004]** The present invention provides a liquid crystal display comprising a plurality of pixels arranged in a plurality of rows and columns, wherein each of some or all of pixels comprises a first sub-pixel area and a second sub-pixel area, each of the first and second sub-pixel areas having a storage capacitor. Each pixel has a first gate line for providing a first gate line signal for charging the first and second storage capacitors, and a second

gate line for providing a second gate line signal for removing part of the charges in the second storage capacitor to a third capacitor. The first and second gate line signals have the same width, but the width and the timing between the gate line signals can be varied so that the first gate line signal provided to a row can be used as the second gate line signal to one of the preceding rows. In some embodiments of the present invention, a pixel in each row have a duplicate pixel which is arranged to similarly receive the first and second gate line signals, but the pixel and its duplicate pixel receive data signals from different data lines.

**[0005]** Thus, the first aspect of the present invention is a liquid crystal display panel comprising:

15 a plurality of pixels arranged in a plurality of rows and columns; and  
20 a plurality of data lines, each for providing data signals to the pixels in a column, wherein each of some or all of the pixels comprises:  
25 a first gate line for providing a first gate-line signal; a second gate line for providing a second gate-line signal after the first gate-line signal has passed; a first sub-pixel area; and  
30 a second sub-pixel area, wherein

35 the first sub-pixel area comprises a first sub-pixel electrode electrically connected to a first charge-storage capacitor, the first sub-pixel electrode arranged to receive the data signals from one of the data lines via a first switching element, the first switching element comprising a control end arranged to receive the first gate-line signal for switching; and

40 the second sub-pixel area comprises a second sub-pixel electrode electrically connected to a second charge-storage capacitor, the second sub-pixel electrode arranged to receive said data signals from said one of the data lines via a second switching element, the second switching element comprising a control end arranged to receive the first gate-line signal for switching, wherein the second sub-pixel electrode is further connected to a third capacitor via a third switching element, the third switching element comprising a control end arranged to receive the second gate-line signal for switching.

**[0006]** The first charge-storage capacitor can be connected to the third capacitor via a fourth capacitor.

**[0007]** In various embodiments of the present invention, the first gate-line signal provided to the pixels in the second row and the first gate-line signal provided to the pixels in the first row have an overlapped period.

**[0008]** In some embodiments of the present invention, the second gate-line signal provided to the pixels in the first row and the first gate-line signal provided to the pixels in the second row have an overlapped period. The first

gate-line signal provided to the pixels in the third row and the second gate-line signal provided to the pixels in the first row are substantially the same. The first gate-line signal provided to the pixels in the fourth row and the second gate-line signal provided to the pixels in the first row are substantially the same.

**[0009]** In some embodiments of the present invention, each pixel further comprises:

a third sub-pixel area and a fourth sub-pixel area, 10  
wherein

the third sub-pixel area comprises a third sub-pixel electrode electrically connected to a fourth charge-storage capacitor, the third sub-pixel electrode arranged to receive data signals from a different one of the data lines via a fourth switching element, the fourth switching element comprising a control end arranged to receive the first gate-line signal for switching; and 15  
the fourth sub-pixel area comprises a fourth sub-pixel electrode electrically connected to a fifth charge-storage capacitor, the fourth sub-pixel electrode arranged to receive the data signals from said different one of the data lines via a fifth switching element, the fifth switching element comprising a control end arranged to receive the first gate-line signal for switching, and wherein 20  
the fourth sub-pixel electrode is further connected to a sixth capacitor via a sixth switching element, the sixth switching element comprising a control end arranged to receive the second gate-line signal for switching. 25

**[0010]** The control end of the fifth switching element is arranged to receive the first gate-line signal from a third gate line, and the control end of the sixth switching element is arranged to receive the second gate-line signal from a fourth gate line. The first gate-line signal is provided to the pixels in the second row after the first gate-line signal provided to the pixels in the first row has passed. 35

**[0011]** A second aspect of the present invention is a method for used in a liquid crystal display panel, the display panel comprising:

a plurality of pixels arranged in a plurality of rows and columns; and  
a plurality of data lines, each for providing data signals to the pixels in a column, wherein each of some or all of the pixels comprises:

a first gate line;  
a first sub-pixel area comprising a first sub-pixel electrode electrically connected to a first charge-storage capacitor; and  
a second sub-pixel area comprising a second sub-pixel electrode electrically connected to a 50  
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second charge-storage capacitor, said method comprising:

arranging a second gate line in said each pixel;  
providing a first gate-line signal via the first gate line for charging the first charge-storage capacitor and the second charge-storage capacitor; and  
providing a second gate-line signal via the second gate line for removing part of electrical charge in the second charge-storage capacitor, wherein the second gate-line signal is provided after the first gate-line signal has passed.

The first sub-pixel electrode is arranged to receive the data signals from one of the data lines via a first switching element, the first switching element comprising a control end arranged to receive the first gate-line signal for said charging the first charge-storage capacitor, and

the second sub-pixel electrode is arranged to receive said data signals from said one of the data lines via a second switching element, the second switching element comprising a control end arranged to receive the first gate-line signal for said charging the second charge-storage capacitor, said method further comprising:

connecting the second sub-pixel electrode to the third capacitor via a third switching element, the third switching element comprising a control end arranged to receive the second gate-line signal for said removing part of the electrical charge in the second charge-storage capacitor to the third capacitor.

**[0012]** In some embodiments of the present invention, each pixel further comprises:

a third sub-pixel area and a fourth sub-pixel area, 45  
wherein

the third sub-pixel area comprises a third sub-pixel electrode electrically connected to a fourth charge-storage capacitor, the third sub-pixel electrode arranged to receive data signals from a different one of the data lines via a fourth switching element, the fourth switching element comprising a control end; and  
the fourth sub-pixel area comprises a fourth sub-pixel electrode electrically connected to a fifth charge-storage capacitor, the fourth sub-pixel electrode arranged to receive the data signals from said different one of the data lines via a fifth

switching element, the fifth switching element comprising a control end;

said method further comprising:

connecting the fifth charge-storage capacitor to a sixth capacitor via a sixth switching element, the sixth switching element comprising a control end;

providing the first gate-line signal to the control end of the fourth switching element and to the control end of the fifth switching element for charging the fourth charge-storage capacitor and fifth charge-storage capacitor;

providing the second gate-line signal to the control end of the sixth switching element for moving part of the electrical charge in the fifth charge-storage capacitor to the sixth capacitor.

[0013] In some embodiments of the present invention, each pixel further comprises:

a third gate line arranged to provide the first gate-line signal to the control end of the fourth switching element and to the control end of the fifth switching element; and

a fourth gate line arranged to provide the second gate-line signal to the control end of the sixth capacitor. The method further comprises:

directing the first gate-line signal provided to the pixels in the second row or the third row to the second gate line in the pixels in the first row.

[0014] The present invention will become apparent upon reading the description taken in conjunction with Figures 4-18.

#### Brief Description of the Drawings

[0015]

Figure 1 shows a typical LCD panel.

Figure 2 shows three color sub-pixels in a pixel in a typical LCD panel.

Figure 3 shows a cross sectional view of a pixel or color sub-pixel in a typical LCD panel.

Figure 4 shows the sub-pixel electrodes in a pixel or color sub-pixel in a LCD panel, according to the present invention.

Figure 5 shows an equivalent circuit of the pixel or color sub-pixel, according to one embodiment of the present invention.

Figure 6 shows the gate line pulse width, according to another embodiment of the present invention.

Figure 7 shows an equivalent circuit of the pixel or color sub-pixel, according to a different embodiment of the present invention.

Figure 8a shows the connection between the sub-pixel electrodes during the charging stage.

Figure 8b shows the relationship between the sub-pixel electrodes during the charge-sharing stage.

Figure 9 is a schematic representation showing the component layout in a pixel or color sub-pixel, according to one embodiment of the present invention. Figure 10 is a cross sectional view of a pixel or color sub-pixel, according to one embodiment of the present invention.

Figure 11 is a timing diagram showing a pre-charge procedure, according to one embodiment of the present invention.

Figure 12 is a schematic representation of a charging and charge-sharing scheme as illustrated in Figure 5.

Figure 13 is a schematic representation of another charging and charge-sharing scheme, according to the present invention.

Figure 14 is a schematic representation of yet another charging and charge-sharing scheme, according to the present invention.

Figure 15a is a schematic representation of a different charging and charge-sharing scheme, according to the present invention.

Figure 15b is a schematic representation of another different charging and charge-sharing scheme, according to the present invention.

Figure 16 is a schematic representation of yet another charging and charge-sharing scheme, according to the present invention.

Figure 17 shows an equivalent circuit of color sub-pixels, according to one embodiment of the present invention.

Figure 18 shows repeating rows in an hG-2D LCD display.

#### Detailed Description of the Invention

[0016] In various embodiments of the present invention, a pixel or color sub-pixel of a liquid crystal display (LCD) panel comprises two areas, each area comprising an area electrode, together with a common electrode, for controlling the alignment of the liquid crystal layer in the respective area. For simplicity, the term sub-pixel will be used to represent a pixel or a color sub-pixel. As shown in Figure 4, the sub-pixel 20<sub>1</sub> includes a first sub-pixel electrode 32<sub>1</sub> to define a first sub-pixel area and a second sub-pixel electrode 34<sub>1</sub> to define a second sub-pixel area. The sub-pixel 20<sub>2</sub> includes a first sub-pixel electrode 32<sub>2</sub> to define a first sub-pixel area and a second sub-pixel electrode 34<sub>2</sub> to define a second sub-pixel area. The sub-pixel 20<sub>3</sub> and other sub-pixels may have similar first and second sub-pixel electrodes. The sub-pixels in a column share a data line, and the sub-pixels in a row share a gate line. As shown in Figure 4, the sub-pixels 20<sub>1</sub>, 20<sub>2</sub>, 20<sub>3</sub>, ... share a data line D1, and the sub-pixels in the next column (not shown) share a different data line D2.

The sub-pixel **20<sub>1</sub>** and other sub-pixels on the same row share a gate line **G1**; the sub-pixel **20<sub>2</sub>** and other sub-pixels on the same row share a gate line **G2**; and the sub-pixel **20<sub>3</sub>** and other sub-pixels on the same row share a gate line **G3**.

**[0017]** The first sub-pixel electrode **32<sub>1</sub>** of the sub-pixel **20<sub>1</sub>** is connected to the data line **D1** through a first switching element **132<sub>1</sub>** and the second sub-pixel electrode **34<sub>1</sub>** is connected to the data line **D1** through a second switching element **134<sub>1</sub>**. The control end of the first and second switching elements **132<sub>1</sub>** and **134<sub>1</sub>** is connected to the gate line **G1**. The first sub-pixel electrode **32<sub>2</sub>** of the sub-pixel **20<sub>2</sub>** is connected to the data line **D1** through a first switching element **132<sub>2</sub>** and the second sub-pixel electrode **34<sub>2</sub>** is connected to the data line **D1** through a second switching element **134<sub>2</sub>**. The control end of the first and second switching elements **132<sub>2</sub>** and **134<sub>2</sub>** is connected to the gate line **G2**.

**[0018]** The first sub-pixel electrode **32<sub>1</sub>** and the common electrode (**COM**, see Figure 3) form a capacitor **ClcA** and the second sub-pixel electrode **34<sub>1</sub>** and the common electrode form a capacitor **ClcB**, as shown in Figure 5. Furthermore, the first sub-pixel electrode **32<sub>1</sub>** is connected to a storage capacitor **CstA** and the second sub-pixel electrode **34<sub>1</sub>** is connected to a storage capacitor **CstB**. Likewise, the first sub-pixel electrode **32<sub>2</sub>** and the common electrode form a capacitor **ClcA**, and the second sub-pixel electrode **34<sub>2</sub>** and the common electrode form a capacitor **ClcB**. The first sub-pixel electrode **32<sub>2</sub>** is connected to a storage capacitor **CstA** and the second sub-pixel electrode **34<sub>2</sub>** is connected to a storage capacitor **CstB**.

**[0019]** As shown in Figure 5, the second sub-pixel electrode **34<sub>1</sub>** is further connected to another capacitor **Cx** through a switching element **136<sub>1</sub>**. The second sub-pixel electrode **34<sub>2</sub>** is further connected to another capacitor **Cx** through a switching element **136<sub>2</sub>**. Likewise, the second sub-pixel electrode in each sub-pixel is also connected to a capacitor **Cx** through a switching element. The control end of the switching element **136<sub>1</sub>** is connected to an additional gate line **G1x**, the control end of the switching element **136<sub>2</sub>** is connected to an additional gate line **G2x**, and so forth.

**[0020]** It is understood that a display panel, such as an LCD panel, is arranged to present an image on a frame-by-frame basis. For each frame, a series of gate line signals is provided to the LCD panel to activate the sub-pixels on one row at a time, for example. As shown in Figure 5, the gate line signal on gate line **G1** is provided between **t0** and **t2**, the gate line signal on gate line **G2** is provided between **t1** and **t3**, and the gate line signal on gate line **G3** is provided between **t2** and **t4**, for example. As such, the gate line signals provided on adjacent rows or gate lines are partially overlapped.

**[0021]** According to one embodiment of the present invention, in each of the sub-pixels, the capacitors **ClcA**, **CstA**, **ClcB** and **CstB** are charged at the same time by the data signal on a data line **D** when the switching ele-

ments **132<sub>i</sub>** and **134<sub>i</sub>** are turned on during a gate-line signal on a gate line **Gi**. Thus, the capacitors **ClcA**, **CstA**, **ClcB** and **CstB** in the sub-pixel **20<sub>1</sub>** are charged during **t0** and **t2**, for example. After the charging of the capacitors **ClcA**, **CstA**, **ClcB** and **CstB** is completed, part of the charge on the capacitors **ClcB** and **CstB** will be shared to the connected capacitor **Cx** during a signal on the additional gate line. As a result, the voltage potential on the second sub-pixel electrode **34<sub>i</sub>** is lower than that on the first sub-pixel electrode **32<sub>i</sub>**. Since the sub-pixel intensity is mainly determined by the voltage between the pixel electrode and the common electrode, the sub-pixel intensity in the second sub-pixel area will change as a result of charge-sharing.

**[0022]** As shown in Figure 5, charging on sub-pixel **20<sub>1</sub>** on the first row is performed between **t0** and **t2** by gate-line signal on **G1**; charging on sub-pixel **20<sub>2</sub>** on the second row is performed between **t1** and **t3** by gate-line signal on **G2**; and charging on sub-pixel **20<sub>3</sub>** is performed between **t2** and **t4** by gate-line signal on **G3**. Charge-sharing on sub-pixel **20<sub>1</sub>** on the first row is performed between **t2** and **t4** by a signal on **G1x**; charge-sharing on sub-pixel **20<sub>2</sub>** on the second row is performed between **t3** and **t5** by a signal on **G2x**; and charge-sharing on sub-pixel **20<sub>3</sub>** is performed between **t4** and **t6** (not shown) by a signal on **G3x**. Thus, the gate-line signal on **G3** can be provided to **G1x** for charge-sharing on sub-pixel **20<sub>1</sub>**, the gate-line signal on **G4** can be provided to **G2x** for charge-sharing on sub-pixel **20<sub>2</sub>**, and the gate-line signal on **Gi+2** can be provided to **Gix** for charge-sharing on sub-pixel **20<sub>i</sub>**, with **i=1, 2, 3...**

**[0023]** In a different embodiment, charging on sub-pixel **20<sub>1</sub>** on the first row is performed between **t0** and **t3** by gate-line signal on **G1**; charging on sub-pixel **20<sub>2</sub>** on the second row is performed between **t1** and **t4** by gate-line signal on **G2**; charging on sub-pixel **20<sub>3</sub>** is performed between **t2** and **t5** by gate-line signal on **G3**, and charging on sub-pixel **20<sub>4</sub>** (not shown) is performed between **t3** and **t6** by gate-line signal on **G4**, as shown in Figure 6. Charge-sharing on sub-pixel **20<sub>1</sub>** on the first row is performed between **t3** and **t6** by a signal on **G1x**; and charge-sharing on sub-pixel **20<sub>2</sub>** on the second row is performed between **t4** and **t7** (not shown) by a signal on **G2x**. Thus, the gate-line signal on **G4** can be provided to **G1x** for charge-sharing on sub-pixel **20<sub>1</sub>**, and the gate-line signal on **Gi+3** can be provided to **Gix** for charge-sharing on sub-pixel **20<sub>i</sub>**.

**[0024]** In a different capacitor arrangement, according to the present invention, charge-sharing is achieved by two capacitors **Cxa** and **Cxb** connected in series. As shown in Figure 7, the first sub-pixel electrode **32<sub>1</sub>** is connected to capacitor **Cxb** through a switching element **136<sub>1</sub>**. The second sub-pixel electrode **34<sub>2</sub>** is connected to capacitor **Cxb** through capacitor **Cxa**. As with the embodiment as shown in Figures 5 and 6, the control end of the switching element **136<sub>1</sub>** is connected to an additional gate line **G1x**, and so forth.

**[0025]** According to one embodiment of the present

invention, in each of the sub-pixels, the capacitors **C1cA**, **CstA**, **ClcB**, **CstB**, **Cxa** and **Cxb** are charged at the same time by the data signal on a data line **D** when the switching elements **132<sub>i</sub>** and **134<sub>i</sub>** are turned on during a gate line signal on a gate line **Gi**. Thus, the first sub-pixel electrode **32<sub>i</sub>** and the second sub-pixel electrode **34<sub>i</sub>** are charged substantially to the same voltage potential relative to **COM**, as shown in Figure 8a. In the charge-sharing period, the signal on **G1x** causes part of the charge on the capacitors **C1cA** and **CstA** to be shared to capacitor **Cxb**, as shown in Figure 8b. As a result, the voltage potential on the first sub-pixel electrode **32<sub>i</sub>** is lower than the second sub-pixel electrode **34<sub>i</sub>**.

**[0026]** During a frame time, the voltage potential on both the first sub-pixel electrode **32<sub>i</sub>** and second sub-pixel electrode **34<sub>i</sub>** in a sub-pixel are substantially the same only in a charging period. After the charge-sharing period, the voltage potential on one of the sub-pixel electrodes **32<sub>i</sub>** and **34<sub>i</sub>** is lower than the other. As a result, the tilt direction of the liquid-crystal molecules under one of the sub-pixel electrodes is slightly different from that under the other sub-pixel electrode in the same sub-pixel. The slight spread in the tilt direction of the liquid-crystal molecules within a sub-pixel may broaden the viewing angles of a liquid-crystal display panel.

**[0027]** The present invention can be applied to a polymer stabilized alignment (PSA) LCD panel, for example. In general, a sub-pixel in a PSA LCD panel comprises two sub-pixel electrodes separately located in two substantially rectangular sub-pixel areas (see U.S. Patent Application No. 2008/0036931, which is incorporated here by reference). Each of the sub-pixel electrodes is generally divided into four segments, each having a fin-like pattern branched out from the center of the sub-pixel electrode. As such, the liquid-crystal molecules under each sub-pixel electrode form four domains. The storage capacitor associated with each of the sub-pixel electrodes can be located near the center of the sub-pixel electrode, for example. An exemplary component layout of a pixel or color-sub-pixel, according to one embodiment of the present invention, is shown in Figure 9. As shown in Figure 9, the sub-pixel electrode **32<sub>i</sub>** and the sub-pixel electrode **34<sub>i</sub>** are separated by a control section. The control section comprises two gate lines **G1** and **G1x**, separately connected to TFTs **132<sub>i</sub>**, **134<sub>i</sub>** and **136<sub>i</sub>**. The charge-sharing capacitors **Cxa/Cxb** are fabricated at the proximity of TFT **136<sub>i</sub>** and sub-pixel **34<sub>i</sub>**. The control section also comprises metal lines to serve as gate lines and common lines.

**[0028]** A cross sectional view of a sub-pixel, according to one embodiment of the present invention, is schematically shown in Figure 10. As shown in Figure 10, the cross section comprises a number of metal lines (**Metal 1**) or sections **290**, **292** to serve as gate lines and common lines. For example, the metal line **290** is used as a gate terminal of a TFT (**132<sub>i</sub>** or **134<sub>i</sub>** of Figure 6), whereas the metal line **292** is used as a common line. An insulator layer **280** is used as a gate insulator between the metal

line **290** and a gate terminal layer **270** (made of a-Si, for example). On top of the a-Si layer **270** are a source terminal **250** and a drain terminal **252** (Metal 2) of the TFT, separated from the gate terminal layer **270** by two n<sup>+</sup> Si sections **260**, **262**. A data insulator **240** is disposed on top of the TFT and part of the insulator layer **280**. A segment **254** of the **Metal 2** layer is used to form a storage capacitor with the metal section **292**. An ITO layer **230** is disposed on part of the data insulator **240**, in electrical contact with the drain terminal **254** and the **Metal 2** segment **254**.

**[0029]** In a high frame-rate or high-resolution LCD display, in order to increase the charging time, a pre-charge scheme is used. In a LCD display wherein the gate line signal on a gate line does not start until the gate line signal on the immediately preceding gate line has passed, the pre-charge signal is usually separated from and preceding a "select" pulse for selecting a sub-pixel. If a sub-pixel is activated by charging the sub-pixel electrode and its associated storage capacitor from a minimum level to a maximum level, the pre-charge signal is used to charge a sub-pixel from the minimum level to an intermediate level. The "select" pulse is then used to charge the sub-pixel to its maximum level. In the present invention, the gate line signal on **G1** is partially overlapped with the gate line signal on **G2** as shown in Figure 5. The non-overlapping part of the gate line signal on **G1** can be used in a pre-charge procedure in a LCD display with column inversion where the data line polarity on each column is the same within a frame. The pre-charging scheme on a LCD display with column inversion is shown in Figure 11.

**[0030]** The charging and charge-sharing scheme, as depicted in Figure 5, uses a charging gate line **Gi** for charging and a separate charge-sharing gate line **Gix** for charge-sharing in a pixel **20**; on the **i**th row. In general, a pixel comprises three color pixels **R**, **G** and **B**. A schematic representation of that charging and charge-sharing scheme is shown in Figure 12. As shown in Figures 5 and 12, the gate-line signal width is twice as broad as the gate pulse width (GPW) of a conventional LCD display so that the gate-line signals provided on adjacent rows are partially overlapped while the gate-signals provided on the charging gate line and the charge-sharing gate line for the pixels on the same row are separated. The charging and charge-sharing scheme can be used in an LCD driven at a 120Hz frequency, or a frame rate of 120 frames per second.

**[0031]** As shown in Figure 12, each row of pixels has two gate lines. The gate line **Gi** is for charging and the gate line **Gix** is for charge-sharing. The gate-line signals for charging provided on adjacent rows are partially overlapped, whereas the gate-signals provided on the charging gate line and on the charge-sharing gate line for the pixels on the same row are separated. As can be seen from Figure 12, the charging gate line signal provided on **G3** is the same as the charge-sharing gate line signal provided on **G1x**. Thus, it is possible to direct the gate-

line signal provided on **G3** to gate line **G1x**. Similarly, it is possible to direct the gate-line signal provided on **G(n+2)** to gate line **Gnx**.

**[0032]** An advantage of having two gate lines for each row of pixels is that the capacitor **Cx** for sharing the charge from the capacitors **ClcB** and **CstB** can be located in the same sub-pixel as shown in Figures 5 and 6. The charge-sharing conductor - the conductor between **CstB** and the switching element **136** - can be entirely located in the same sub-pixel. Likewise, the capacitor **Cxb** for sharing the charge from **ClcA** and **CstA** can be located in the same sub-pixel as shown in Figure 7. The charge-sharing conductor - the conductor between **CstA** and the switching element **136** - can be entirely located in the same sub-pixel. In the embodiment as shown in Figure 5, the gate line signal width is substantially twice as broad as the gate pulse width (GPW) of a conventional LCD display. In the embodiment as shown in Figure 6, the gate line signal width is substantially three times as broad as the GPW of a conventional LCD display.

**[0033]** If each row of pixels has only one gate line and gate pulse width is greater than the GPW of a conventional LCD display, the charge-sharing conductor must cross the sub-pixels in adjacent rows. This cross charge-sharing scheme would make the pixel layout more complicated and cause an undesirable effect of pixel-to-pixel coupling.

**[0034]** Furthermore, as discussed in conjunction with Figure 11, the timing requirement for pre-charge is that the gate-line signals on adjacent rows of pixels are partially overlapping. However, the timing requirement for charging and charge-sharing is that the charge-sharing is carried only after the charging in the same row is completed. Thus, there would be a trade-off between pre-charge and charge-sharing when only one gate-line is used for providing signals on each row of pixels.

**[0035]** With two gate lines for each row of pixels, both the timing requirement for pre-charge and the timing requirement for charge-sharing can be fulfilled.

**[0036]** A similar charging and charge-sharing scheme can also be used in a 240Hz LCD panel based on a half-gate two-data (hG-2D) technology. As shown in Figure 13, each row of pixels is effectively split into an upper row and a lower row. For example, the pixel row **20<sub>1</sub>** driven by charging gate line **G1** and charge-sharing gate line **G1x** now has a duplicate pixel row **20'<sub>1</sub>** driven by charging gate line **G1'** and charge-sharing gate line **G1x'**. In the hG-2D driving scheme, the gate line signals on charging gate lines **G1** and **G1'** are simultaneously provided to the pixel rows **20<sub>1</sub>** and **20'<sub>1</sub>**, but the data signal to the pixel row **20<sub>1</sub>** associated with **G1** and the data signal to the pixel row **20'<sub>1</sub>** associated with **G1'** are separately provided on two data lines (not shown). Likewise, the gate line signals on charge-sharing gate lines **G1x** and **G1x'** are simultaneously provided. The gate line signal for charging in the pixels on both pixel row **20<sub>i</sub>** and pixel row **20'<sub>i</sub>** is denoted by **gci**. The gate line signal for charge sharing in the pixels on both pixel row **20<sub>i</sub>** and

pixel row **20'<sub>i</sub>** is denoted by **gsi**.

**[0037]** In the embodiment as shown in Figure 13, each pair of related pixel rows **20<sub>i</sub>** and **20'<sub>i</sub>** has its own charging gate-signal **gci** and charge-sharing gate signal **gsi**. Accordingly, in a frame time, there will be n charging gate-signals and n charge-sharing gate signals for n pairs of related pixel rows. It is possible to eliminate the n charge-sharing gate-signals by using the charging gate signals for charge-sharing. An equivalent circuit of the pixel rows in an hG-2D LCD display is shown in Figure 18.

**[0038]** As shown in Figure 14, a charging gate-signal **gc3**, for example, can be simultaneously used for charging in the pixels on pixel row **20<sub>3</sub>** and **20'<sub>3</sub>** and for charge-sharing in the pixels on pixel row **20<sub>1</sub>** and **20'<sub>1</sub>**. Likewise, a charging gate-signal **gc4** can be simultaneously used for charging in the pixels on pixel row **20<sub>4</sub>** and **20'<sub>4</sub>** and for charge-sharing in the pixels on pixel row **20<sub>2</sub>** and **20'<sub>2</sub>**. In this embodiment, the gate-line signal width is twice the gate pulse width (GPW) and the charging gate-signals "jump" over two pairs of rows to do the charge-sharing.

**[0039]** If the gate-line signals are further broadened as shown in Figure 6, the charging gate-signals "jump" over three or more pairs to carry out the charge sharing. As shown in Figure 15a, a charging gate-signal **gc4**, for example, can be simultaneously used for charging in the pixels on pixel row **20<sub>4</sub>** and for charge-sharing in the pixels on pixel row **20<sub>1</sub>**. Likewise, a charging gate-signal **gc5** can be simultaneously used for charging in the pixels on pixel row **20<sub>5</sub>** and for charge-sharing in the pixels on pixel row **20<sub>2</sub>**. In this embodiment, the gate-line signal width is three times the gate pulse width (GPW) and the charging gate-signals "jump" over three pairs of rows to do the charge-sharing.

**[0040]** A similar charging and charge-sharing scheme can also be used in a 240Hz LCD panel based on the hG-2D technology. As shown in Figure 15b, a charging gate-signal **gc4**, for example, can be simultaneously used for charging in the pixels on pixel row **20<sub>4</sub>** and **20'<sub>4</sub>** and for charge-sharing in the pixels on pixel row **20<sub>1</sub>** and **20'<sub>1</sub>**. Likewise, a charging gate-signal **gc5** can be simultaneously used for charging in the pixels on pixel row **20<sub>5</sub>** and **20'<sub>5</sub>** and for charge-sharing in the pixels on pixel row **20<sub>2</sub>** and **20'<sub>2</sub>**. In this embodiment, the gate-line signal width is three times the gate pulse width (GPW) and the charging gate-signals "jump" over three pairs of rows to do the charge-sharing.

**[0041]** If the gate-line signal width is equal to the gate-pulse width (GPW), the charging gate-signals can only jump to the preceding pair of rows to do the charge-sharing. As shown in Figure 16, a charging gate-signal **gc4**, for example, can be simultaneously used for charging in the pixels on pixel row **20<sub>4</sub>** and **20'<sub>4</sub>** and for charge-sharing in the pixels on pixel row **20<sub>3</sub>** and **20'<sub>3</sub>**. Likewise, a charging gate-signal **gc5** can be simultaneously used for charging in the pixels on pixel row **20<sub>5</sub>** and **20'<sub>5</sub>** and for charge-sharing in the pixels on pixel row **20<sub>4</sub>** and **20'<sub>4</sub>**.

**[0042]** In summary, the present invention uses a regular gate-pulse width or a wider gate-pulse width to

achieve various embodiments. With a regular gate-pulse width (GPW), a gate-signal can be used to simultaneously carry out charging in the pixels on a pair **n** of duplicate pixel rows and charge-sharing in the pixels on a preceding pair **n-1** of duplicate pixel rows in a 240Hz display using hG-2D technology, wherein the data signals to the duplicate pixel rows are separately provided by two data lines.

**[0043]** With a double gate-pulse width (2xGPW), a gate signal can be used to simultaneously carry out charging in the pixels on a pixel row **n** and charge-sharing in the pixels on a different pixel row **n-2** a 120Hz display. Furthermore, such a gate signal can be used to simultaneously carry out charging in the pixels on a pair **n** of duplicate pixel row and charge-sharing in the pixels on a different pair **n-2** of duplicate pixel rows in a 240Hz display using hG-2D technology wherein the data signals to the duplicate pixel rows are separately provided by two data lines.

**[0044]** With a triple gate-pulse width (3xGPW), a gate signal can be used to simultaneously carry out charging in the pixels on a pixel row **n** and charge-sharing in the pixels on a different pixel row **n-3** a 120Hz display. Furthermore, such a gate signal can be used to simultaneously carry out charging in the pixels on a pair **n** of duplicate pixel row and charge-sharing in the pixels on a different pair **n-3** of duplicate pixel rows in a 240Hz display using hG-2D technology wherein the data signals to the duplicate pixel rows are separately provided by two data lines.

**[0045]** It is also possible to use a gate-line signal having a pulse width broader than three times the regular GPW and the timing between charging and charge-sharing in the pixels on the same row will be adjusted accordingly.

**[0046]** The pixels **20<sup>1</sup>** in the repeated rows as shown in Figures 13-16 can be identical to the pixels **20<sub>j</sub>**. Thus, the pixel **20<sub>1</sub>** and the pixel **20<sup>1</sup>** as shown in Figure 17 can have substantially the same components except that the switching elements **132<sub>1</sub>, 134<sub>1</sub>** in pixel **20<sub>1</sub>** are arranged to receive the data signals from data line **D1**, whereas the switching elements **132<sup>1</sup>, 134<sup>1</sup>** in pixel **20<sup>1</sup>** are arranged to receive the data signals from a different data line **D1'**.

**[0047]** In a conventional LCD display, the color sub-pixels **R, G, B** in each pixel are arranged in a row as shown in Figure 2. As shown in Figure 2, each color sub-pixel has its own data line. In a Tri-gate LCD display, the color sub-pixels **R, G, B** for each pixel are arranged in a column, and each color sub-pixel has its own gate line. There will be three gate lines per pixel row. In a half-source driver (HSD) type LCD display, the color sub-pixels **R, G, B** in each pixel are arranged in a row, similar to the conventional LCD display, but the **R, G, B** data lines for the sub-pixels are grouped into pairs such that one of the data lines in each pixel is moved to the other side of the sub-pixel. As the data line is moved to the other side of the sub-pixel, it leaves a space or empty

area between two adjacent color sub-pixels. That area can be used for the layout of the charge-sharing conductors. As such, it would not be necessary to reduce the width of the sub-pixel electrodes in order to implement the charge-sharing conductors. For the above reasons, the present invention can be used in a HSD type LCD display without sacrificing the aperture ratio (AR) of a pixel.

**[0048]** In a Polymer Stabilized Alignment (PSA) type LCD display, the charging gate lines **Gi** and charge-sharing gate lines **Gix** can be implemented in a non-overlapping and non-crossing design (see Figure 9, for example). In Figure 9, the gate line **Gi** is substantially parallel to the gate line **Gix** and they are arranged in a space between the first sub-pixel area and the second sub-pixel area.

**[0049]** The various embodiments of the present invention can also be used in a FHD type LCD display with a 1920x1080 resolution, a 4k2k type display with a 3840x2160 resolution.

**[0050]** It should be noted that, the various embodiments of the present invention can be used in a color sub-pixel in a color LCD display, but they can also be used in a pixel of a monochromic LCD display. The LCD display can be a transmissive display, for example. The invention can also be used in a transflective display or a reflective display.

**[0051]** Thus, although the present invention has been described with respect to one or more embodiments thereof, it will be understood by those skilled in the art that the foregoing and various other changes, omissions and deviations in the form and detail thereof may be made without departing from the scope of this invention.

## 35 Claims

1. A liquid crystal display panel comprising:

40 a plurality of pixels arranged in a plurality of rows and columns; and  
a plurality of data lines, each for providing data signals to the pixels in a column,  
wherein each of some or all of the pixels comprises:  
45 a first gate line for providing a first gate-line signal;  
a second gate line for providing a second gate-line signal after the first gate-line signal has passed;  
50 a first sub-pixel area; and  
a second sub-pixel area, wherein  
55 the first sub-pixel area comprises a first sub-pixel electrode electrically connected to a first charge-storage capacitor, the first sub-pixel electrode ar-

ranged to receive the data signals from one of the data lines via a first switching element, the first switching element comprising a control end arranged to receive the first gate-line signal for switching; and 5

the second sub-pixel area comprises a second sub-pixel electrode electrically connected to a second charge-storage capacitor, the second sub-pixel electrode arranged to receive said data signals from said one of the data lines via a second switching element, the second switching element comprising a control end arranged to receive the first 10 gate-line signal for switching, wherein the second sub-pixel electrode is further connected to a third capacitor via a third switching element, the third switching element comprising a control end arranged to receive the second 15 gate-line signal for switching.

2. The liquid crystal display panel according to claim 1, wherein the first charge-storage capacitor is further 20 connected to the third capacitor via a fourth capacitor. 25

3. The liquid crystal display panel according to claim 1, wherein the plurality of rows comprise a first row and a second row and wherein the first gate-line signal provided to the pixels in the second row and the first 30 gate-line signal provided to the pixels in the first row have an overlapped period. 35

4. The liquid crystal display panel according to claim 3, wherein the plurality of rows comprise a third row following the second row, and wherein the first gate-line signal provided to the pixels in the third row and the second gate-line signal provided to the pixels in the first row are substantially the same. 40

5. The liquid crystal display panel according to claim 3, wherein the plurality of rows comprise a third row following the second row and a fourth following the 45 third row, and wherein the first gate-line signal provided to the pixels in the fourth row and the second gate-line signal provided to the pixels in the first row are substantially the same. 50

6. The liquid crystal display panel according to claim 1, wherein the first gate line is substantially parallel to the second gate line. 55

7. The liquid crystal display panel according to claim 1, wherein said each pixel further comprises:

a third sub-pixel area and a fourth sub-pixel ar-

ea, wherein

the third sub-pixel area comprises a third sub-pixel electrode electrically connected to a fourth charge-storage capacitor, the third sub-pixel electrode arranged to receive data signals from a different one of the data lines via a fourth switching element, the fourth switching element comprising a control end arranged to receive the first gate-line signal for switching; and

the fourth sub-pixel area comprises a fourth sub-pixel electrode electrically connected to a fifth charge-storage capacitor, the fourth sub-pixel electrode arranged to receive the data signals from said different one of the data lines via a fifth switching element, the fifth switching element comprising a control end arranged to receive the first gate-line signal for switching, and wherein the fourth sub-pixel electrode is further connected to a sixth capacitor via a sixth switching element, the sixth switching element comprising a control end arranged to receive the second gate-line signal for switching.

8. A method for used in a liquid crystal display panel, the display panel comprising:

a plurality of pixels arranged in a plurality of rows and columns; and

a plurality of data lines, each for providing data signals to the pixels in a column, wherein each of some or all of the pixels comprises:

a first gate line;

a first sub-pixel area comprising a first sub-pixel electrode electrically connected to a first charge-storage capacitor; and

a second sub-pixel area comprising a second sub-pixel electrode electrically connected to a second charge-storage capacitor, said method comprising:

arranging a second gate line in said each pixel;

providing a first gate-line signal via the first gate line for charging the first charge-storage capacitor and the second charge-storage capacitor; and

providing a second gate-line signal via the second gate line for removing part of electrical charge in the second charge-storage capacitor, wherein the second gate-line signal is provided after the first gate-line signal has passed.

9. The method according to claim 8, wherein

the first sub-pixel electrode is arranged to receive the data signals from one of the data lines via a first switching element, the first switching element comprising a control end arranged to receive the first gate-line signal for said charging the first charge-storage capacitor, and the second sub-pixel electrode is arranged to receive said data signals from said one of the data lines via a second switching element, the second switching element comprising a control end arranged to receive the first gate-line signal for said charging the second charge-storage capacitor, said method further comprising:

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connecting the second sub-pixel electrode to the third capacitor via a third switching element, the third switching element comprising a control end arranged to receive the second gate-line signal for said removing part of the electrical charge in the second charge-storage capacitor to the third capacitor.

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10. The method according to claim 9, wherein the plurality of rows comprise a first row and a second row and wherein the first gate-line signal provided to the pixels in the second row and the first gate-line signal provided to the pixels in the first row have an overlapped period.

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11. The method according to claim 10, wherein the plurality of rows comprise a third row following the second row, and wherein the first gate-line signal provided to the pixels in the third row and the second gate-line signal provided to the pixels in the first row are substantially the same.

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12. The method according to claim 10, wherein the plurality of rows comprise a third row following the second row and a fourth following the third row, and wherein the first gate-line signal provided to the pixels in the fourth row and the second gate-line signal provided to the pixels in the first row are substantially the same.

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13. The method according to claim 9, wherein said each pixel further comprises:

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a third sub-pixel area and a fourth sub-pixel area, wherein

the third sub-pixel area comprises a third sub-pixel electrode electrically connected to a fourth charge-storage capacitor, the third sub-pixel electrode arranged to receive data signals from a different one of

the data lines via a fourth switching element, the fourth switching element comprising a control end; and the fourth sub-pixel area comprises a fourth sub-pixel electrode electrically connected to a fifth charge-storage capacitor, the fourth sub-pixel electrode arranged to receive the data signals from said different one of the data lines via a fifth switching element, the fifth switching element comprising a control end,

said method further comprising:

connecting the fifth charge-storage capacitor to a sixth capacitor via a sixth switching element, the sixth switching element comprising a control end; providing the first gate-line signal to the control end of the fourth switching element and to the control end of the fifth switching element for charging the fourth charge-storage capacitor and fifth charge-storage capacitor;

providing the second gate-line signal to the control end of the sixth switching element for moving part of the electrical charge in the fifth charge-storage capacitor to the sixth capacitor.

14. The method according to claim 13, wherein the plurality of rows comprising a first row and a second row following the first row, said method further comprising:

directing the first gate-line signal provided to the pixels in the second row to the second gate line in the pixels in the first row.

15. The method according to claim 13, wherein the plurality of rows comprising a first row, a second row following the first row, and a third row following the second row, said method further comprising:

directing the first gate-line signal provided to the pixels in the third row to the second gate line in the pixels in the first row.

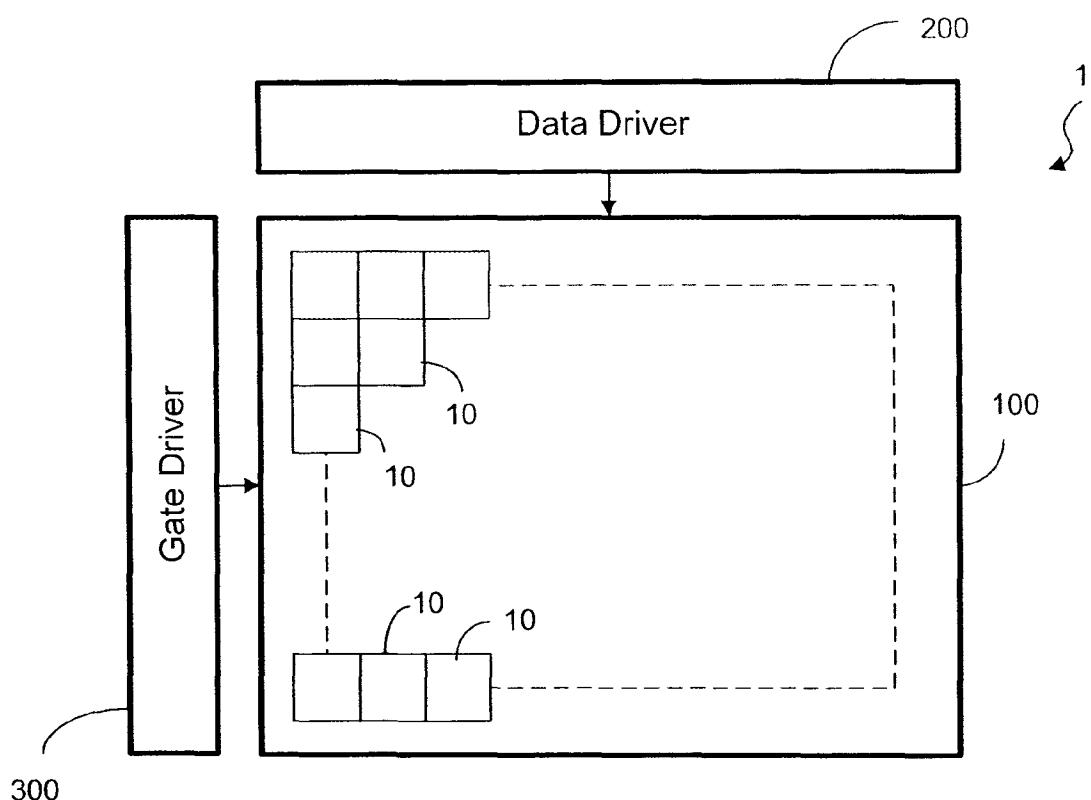


FIG. 1  
(prior art)

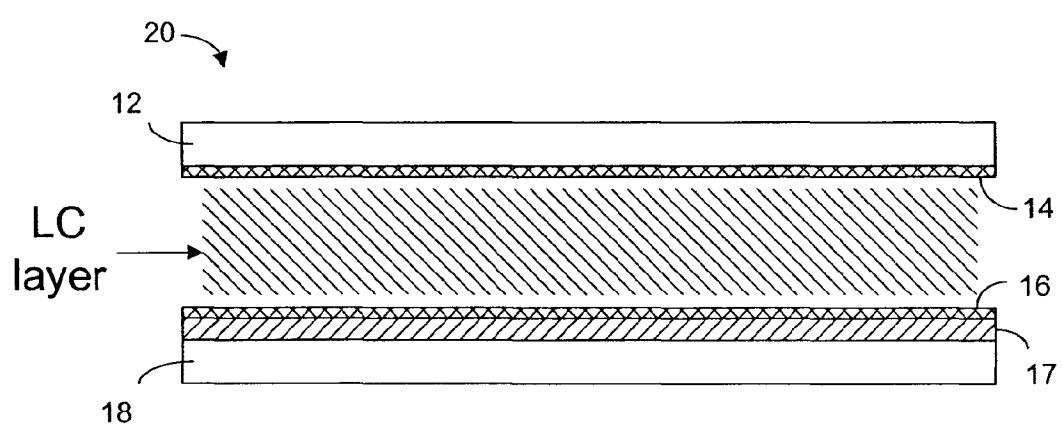
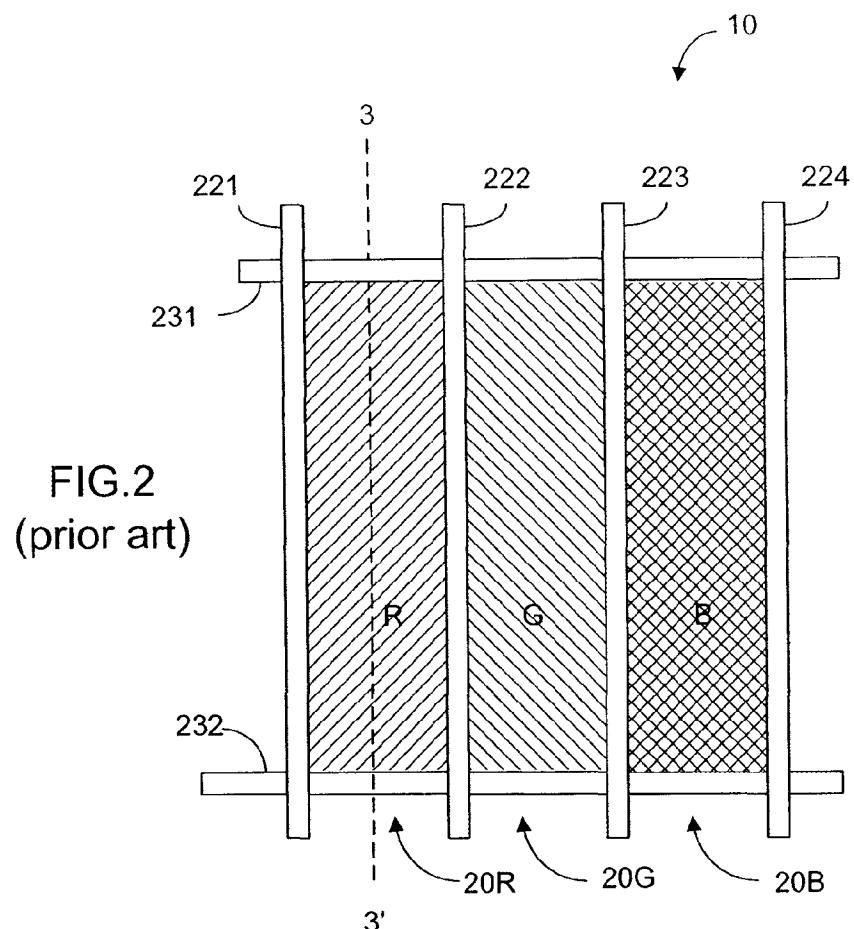


FIG. 3  
(prior art)

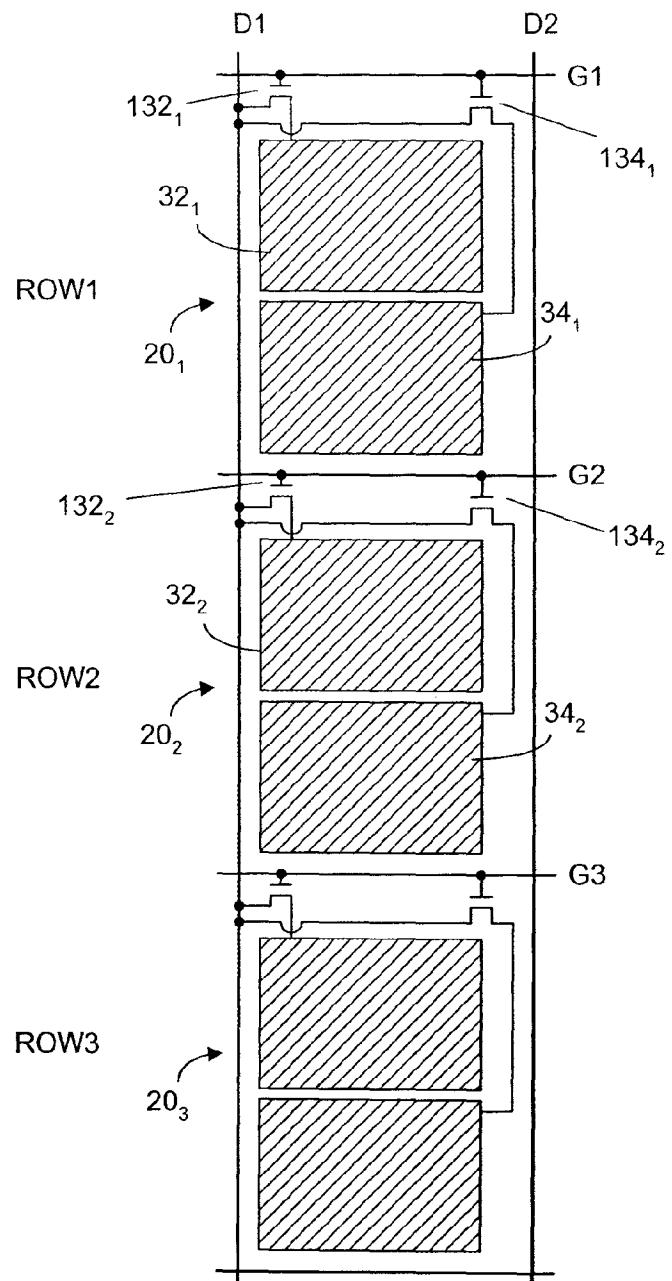


FIG.4

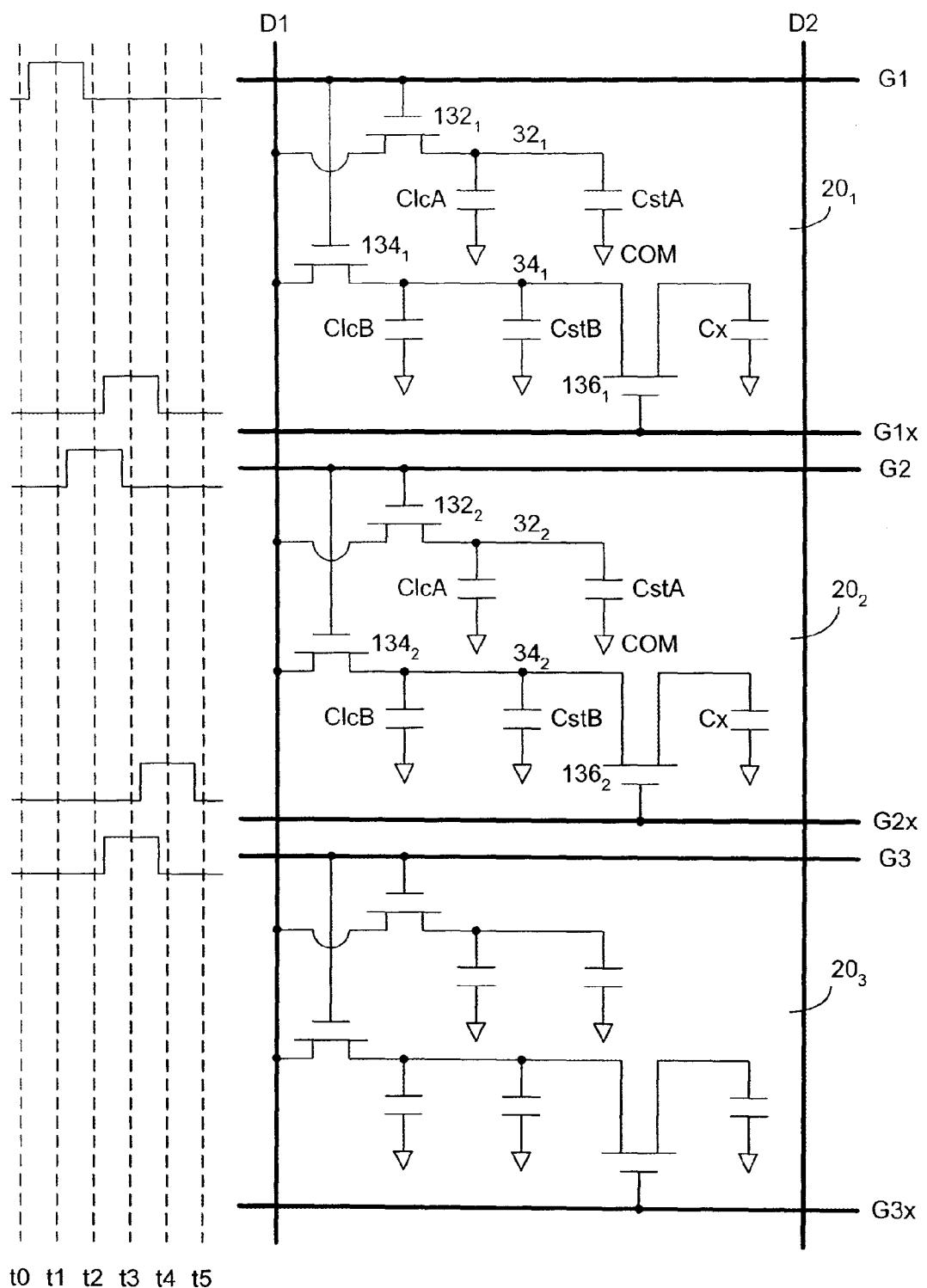


FIG. 5

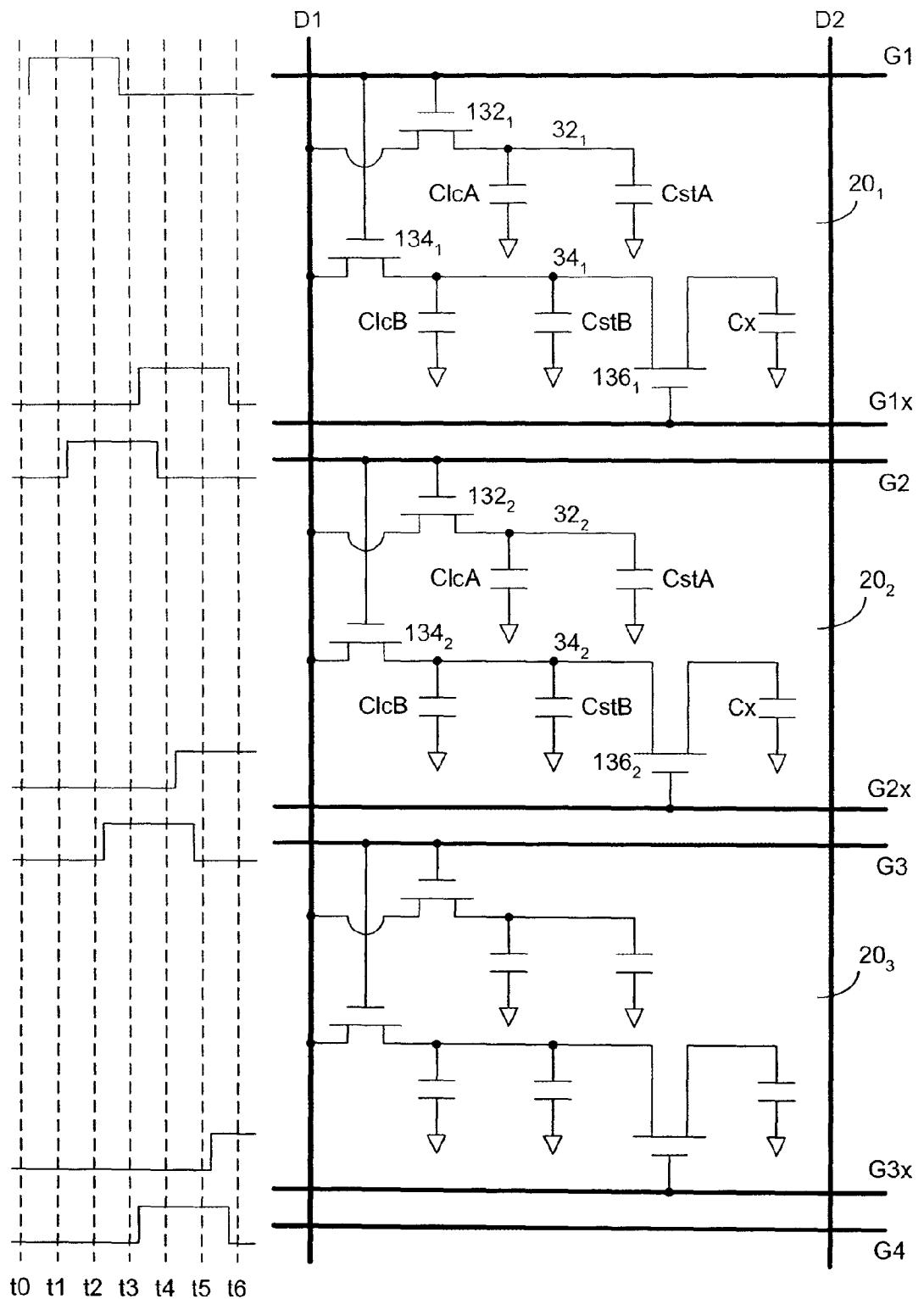


FIG. 6

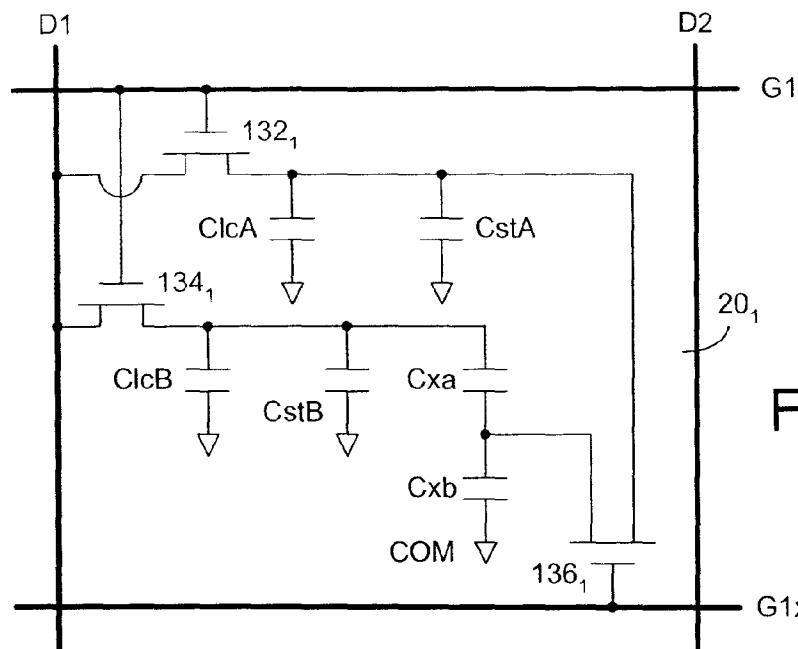


FIG. 7

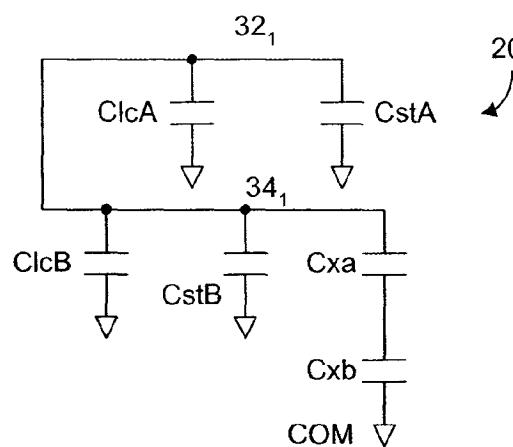


FIG. 8a

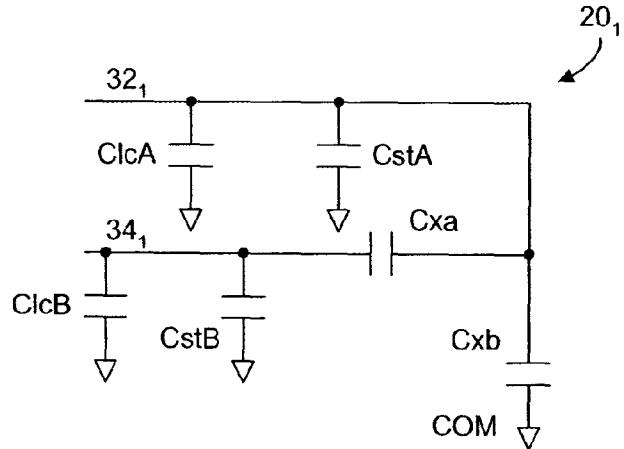


FIG. 8b

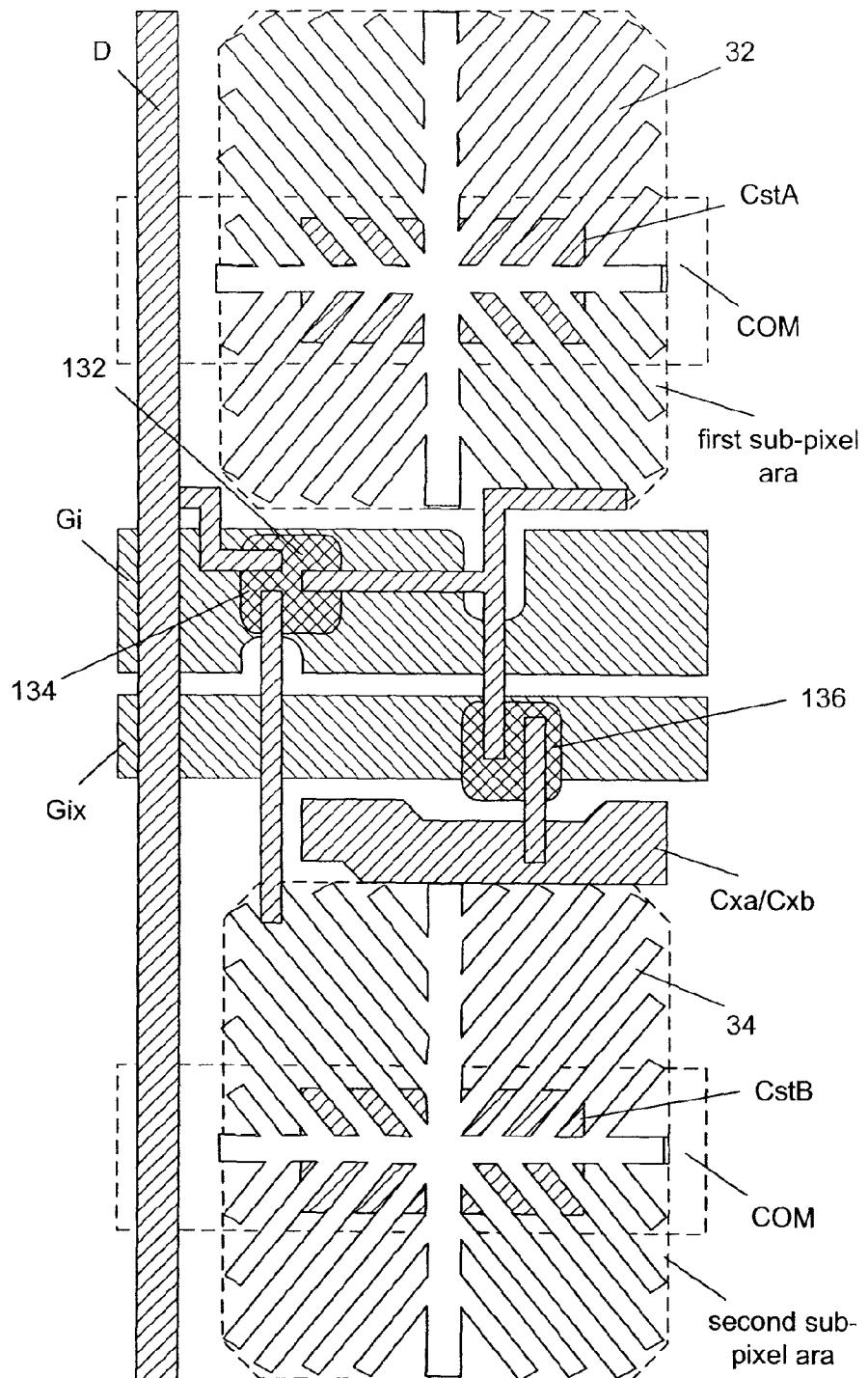


FIG. 9

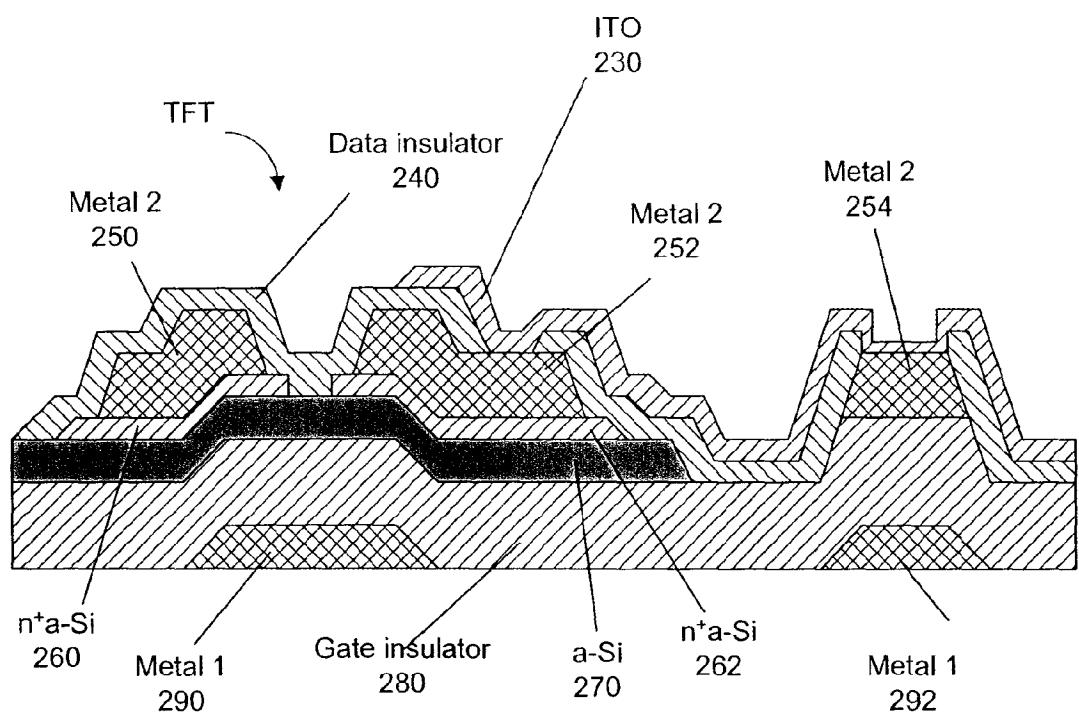


FIG. 10

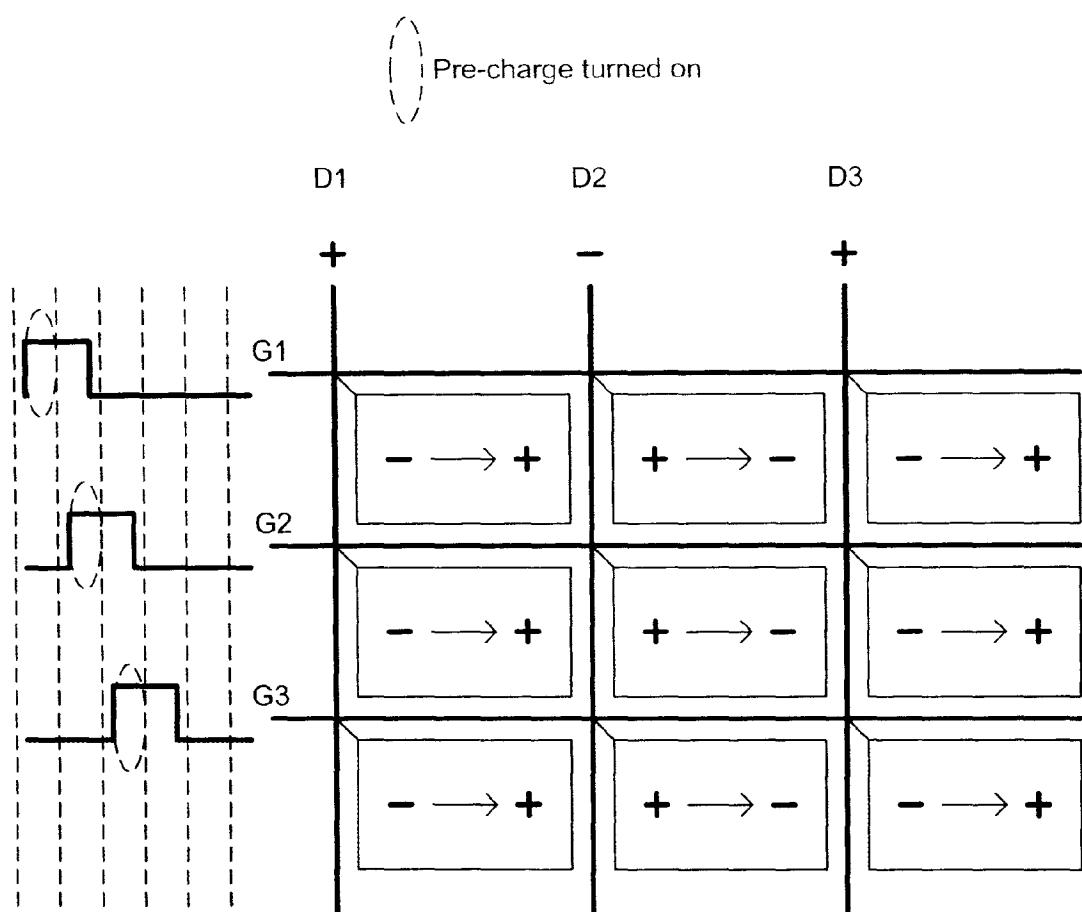


FIG. 11

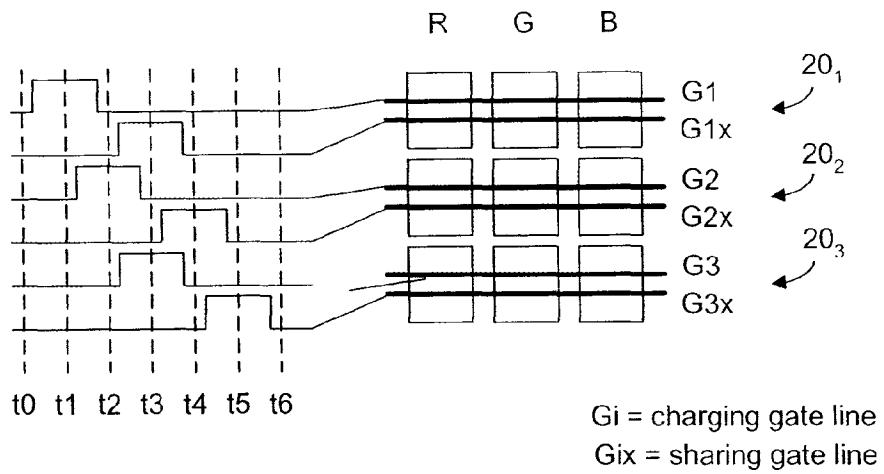
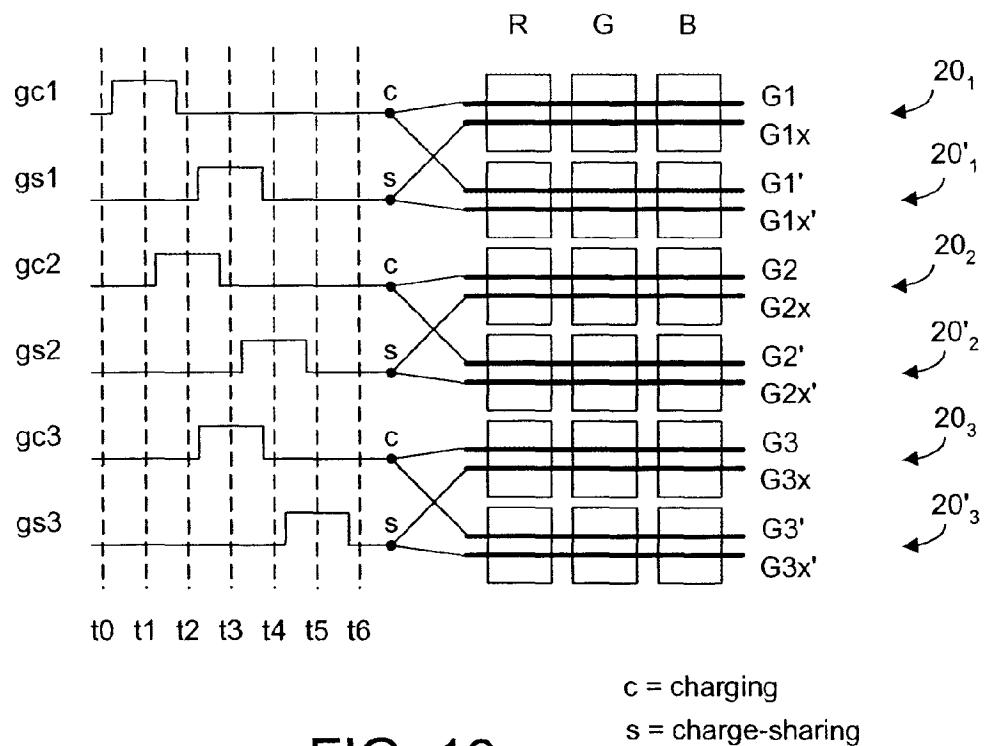


FIG. 12



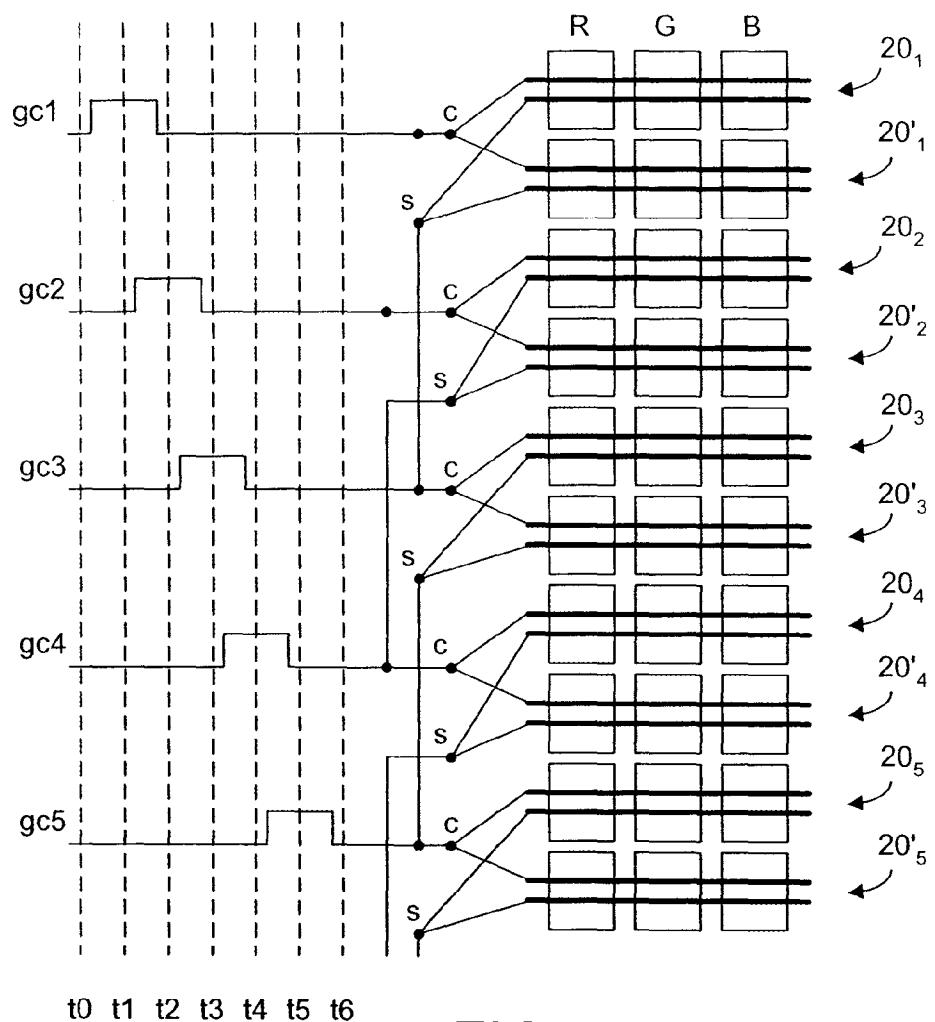


FIG. 14

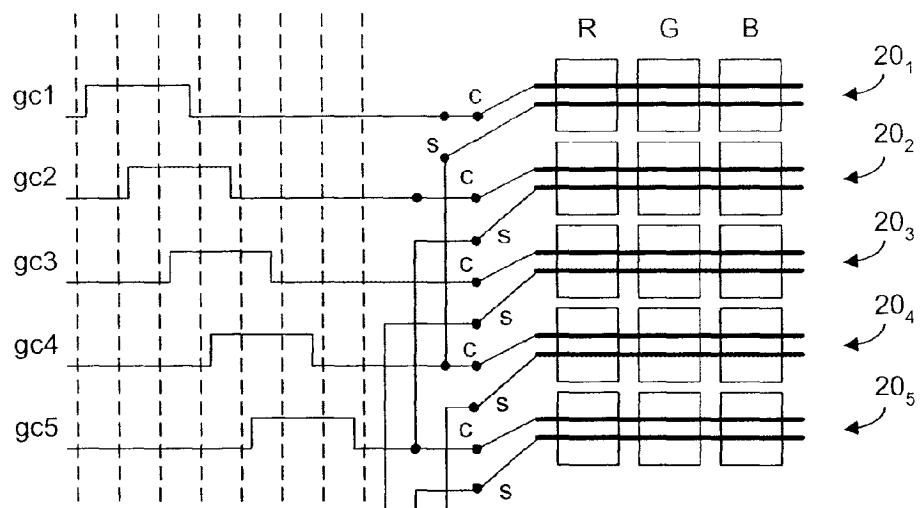


FIG. 15a

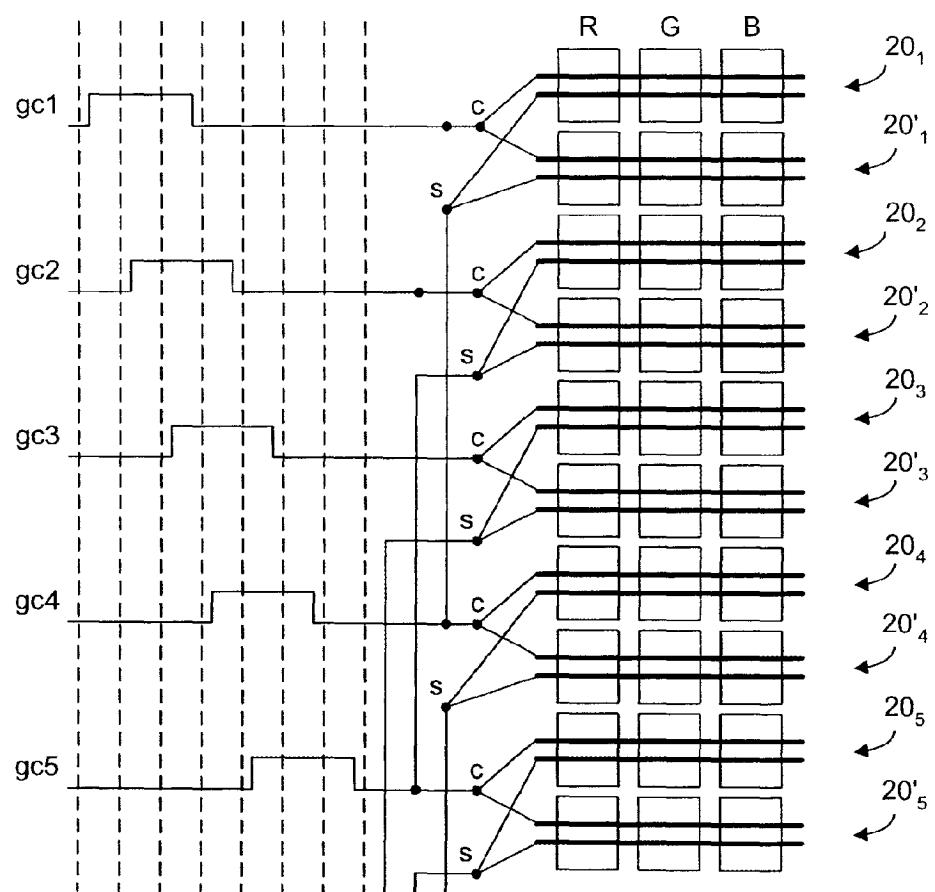


FIG. 15b

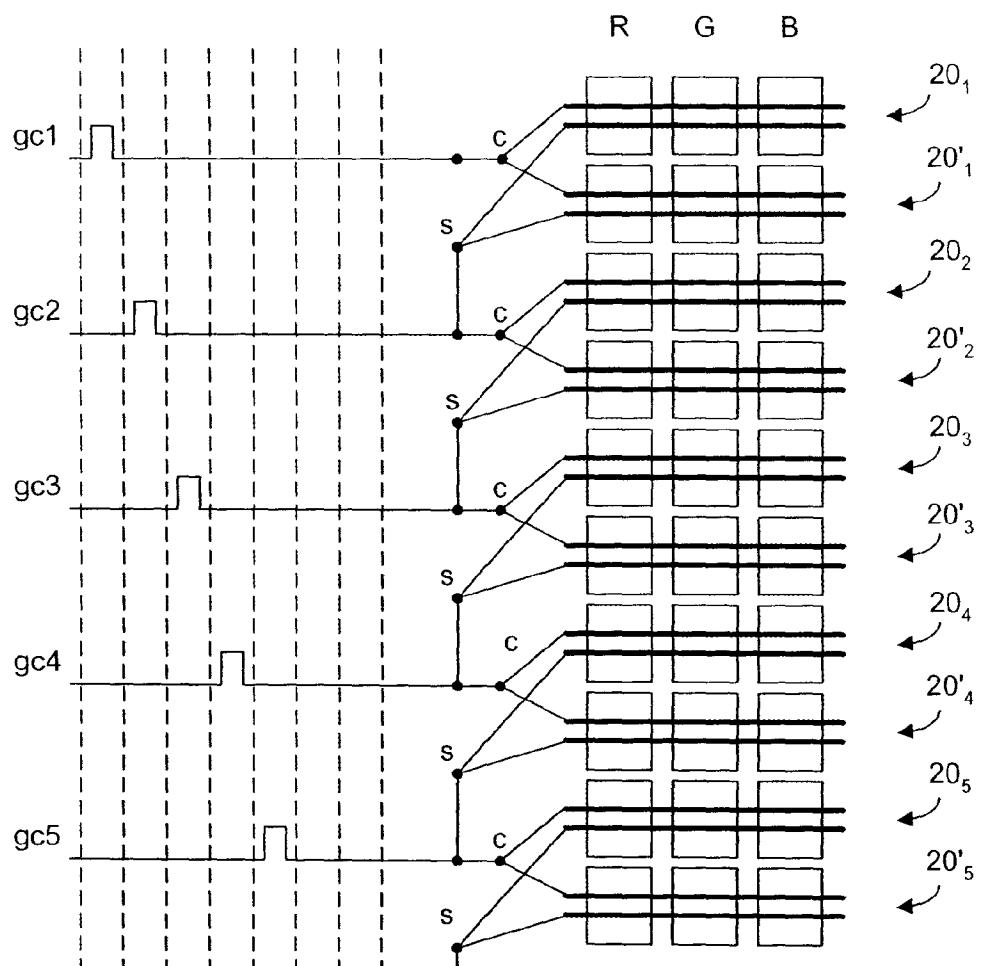


FIG. 16

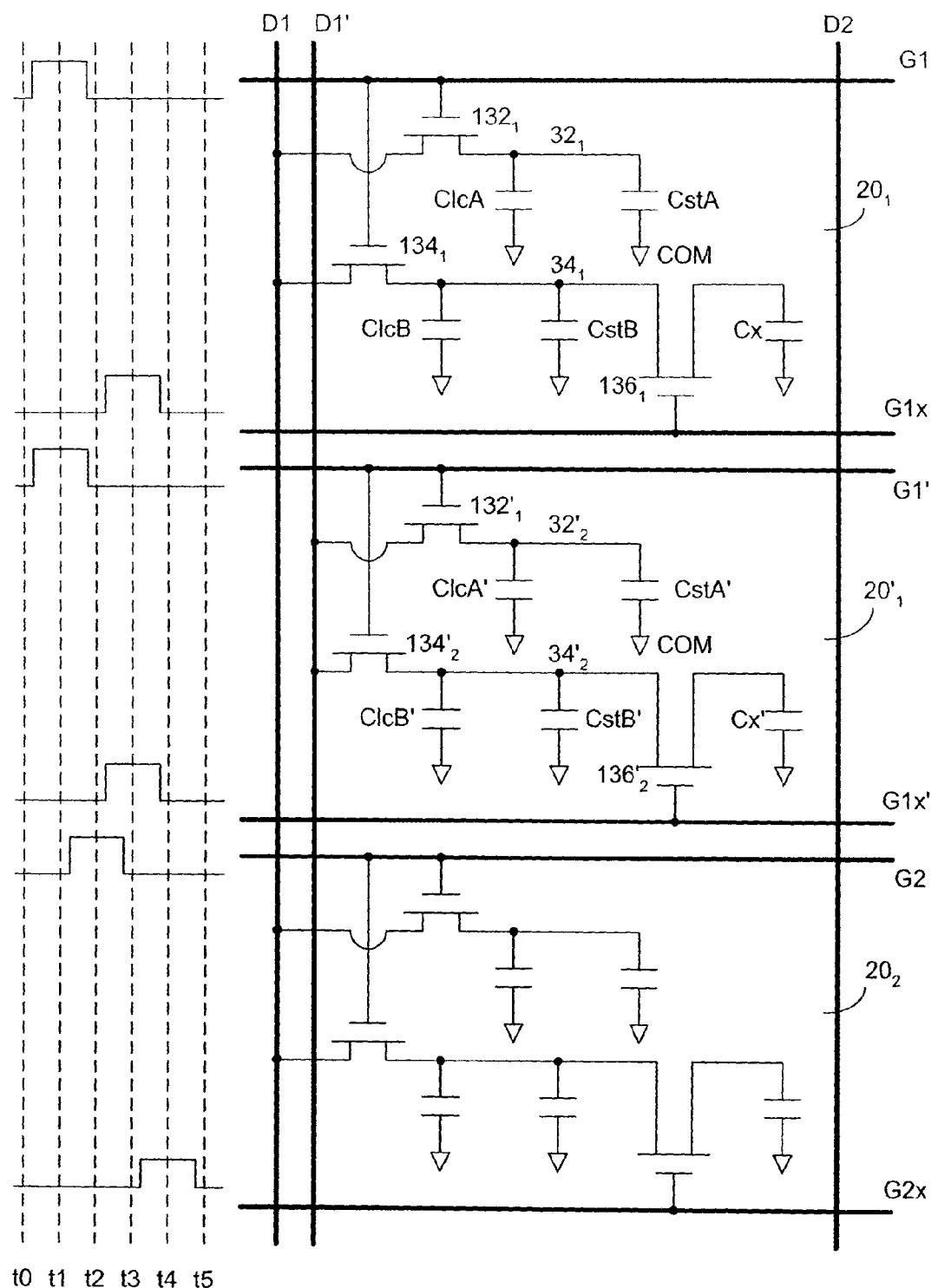


FIG. 17

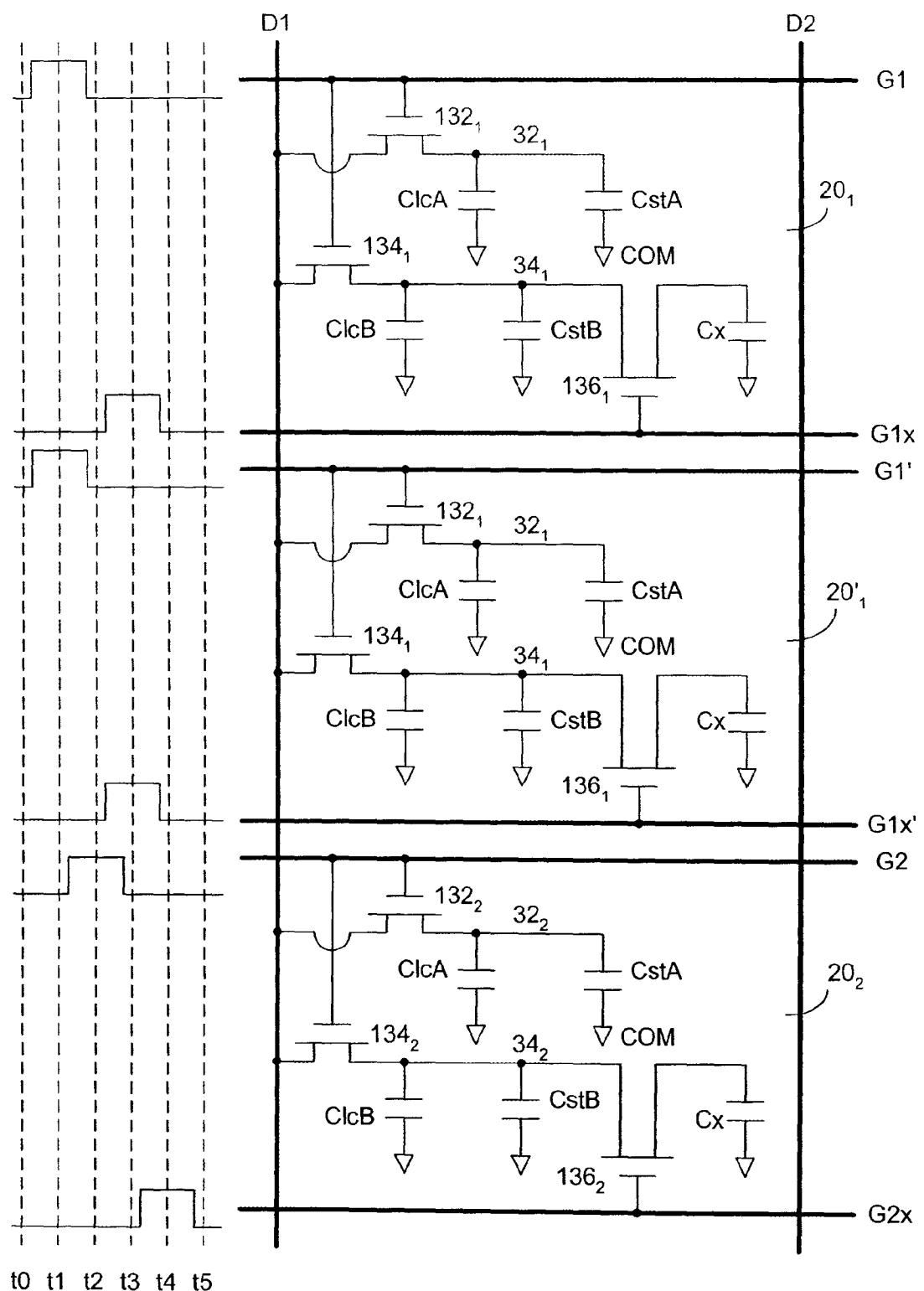


FIG. 18



## EUROPEAN SEARCH REPORT

Application Number  
EP 10 15 1469

DOCUMENTS CONSIDERED TO BE RELEVANT			CLASSIFICATION OF THE APPLICATION (IPC)
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	
X	US 2008/303768 A1 (DO HEE-WOOK [KR] ET AL) 11 December 2008 (2008-12-11)	1,2,6,8,9	INV. G09G3/36
Y	* paragraph [0040] - paragraph [0055] * * paragraph [0107] * * figures 1,2A,2B *	3-5, 10-12	
X	US 2008/246038 A1 (UM YOON-SUNG [KR] ET AL) 9 October 2008 (2008-10-09) * paragraph [0030] - paragraph [0032] * * paragraph [0053] - paragraph [0062] * * paragraph [0084] - paragraph [0085] * * figures 2,5,11B *	1-3,6	
X	US 2009/027325 A1 (KIM DONG-GYU [KR] ET AL) 29 January 2009 (2009-01-29)	1,2,6-9, 13-15	
Y	* paragraph [0002] * * paragraph [0055] - paragraph [0075] * * figures 1,2 *	3-5, 10-12	
Y	US 2007/183218 A1 (LEE BONG-JUN [KR] ET AL) 9 August 2007 (2007-08-09) * paragraph [0003] * * paragraph [0009] * * paragraph [0045] - paragraph [0050] * * figure 3 *	3-5, 10-12	TECHNICAL FIELDS SEARCHED (IPC)
			G09G G02F
The present search report has been drawn up for all claims			
1	Place of search The Hague	Date of completion of the search 24 September 2010	Examiner Lochhead, Steven
CATEGORY OF CITED DOCUMENTS		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons ..... & : member of the same patent family, corresponding document	
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document			

**ANNEX TO THE EUROPEAN SEARCH REPORT  
ON EUROPEAN PATENT APPLICATION NO.**

EP 10 15 1469

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24-09-2010

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专利名称(译)	具有电荷共享方案的液晶显示面板		
公开(公告)号	<a href="#">EP2323124A1</a>	公开(公告)日	2011-05-18
申请号	EP2010151469	申请日	2010-01-22
[标]申请(专利权)人(译)	友达光电股份有限公司		
申请(专利权)人(译)	友达光电股份有限公司		
当前申请(专利权)人(译)	友达光电股份有限公司		
[标]发明人	LIAO PEI CHUN TING TIEN LUN HSU WEN HAO HOU HUNG LUNG		
发明人	LIAO, PEI-CHUN TING, TIEN-LUN HSU, WEN-HAO HOU, HUNG-LUNG		
IPC分类号	G09G3/36		
CPC分类号	G09G3/3648 G02F1/133707 G02F1/136213 G02F1/13624 G09G3/3659 G09G2300/0443 G09G2300/0447 G09G2300/0852 G09G2310/0205 G09G2310/0251 G09G2320/028		
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外部链接	<a href="#">Espacenet</a>		

#### 摘要(译)

一种LCD面板，其中像素具有第一子像素区域和第二子像素区域，每个区域具有存储电容器。每个像素具有：第一栅极线，用于提供用于对第一和第二存储电容器充电的第一栅极线信号；以及第二栅极线，用于提供第二栅极线信号，用于将第二存储电容器中的部分电荷移除到第一个栅极线信号通过后的第三个电容。可以改变第一和第二栅极线信号的宽度及其时序，使得提供给行的第一栅极线信号可以用作前面行之一的第二栅极线信号。在一些实施例中，每行中的像素具有复制像素，其被布置为类似地接收第一和第二栅极线信号，但是从不同数据线接收数据信号。

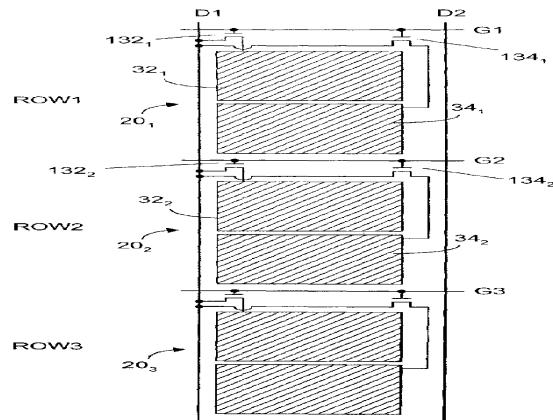


FIG.4