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(54) Method and device for driving a liquid crystal display

Verfahren und Vorrichtung zur Ansteuerung einer Flüssigkristallanzeige

Procédé et dispositif pour commander un dispositif d'affichage à cristaux liquides

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Description

FIELD OF THE INVENTION

[0001] The present invention relates generally to a liquid crystal display (LCD), and more particularly, to a source driver of a display panel for displaying an image data in an adaptive column inversion and methods of driving same.

BACKGROUND OF THE INVENTION

[0002] Liquid crystal display (LCD) is commonly used as a display device because of its capability of displaying images with good quality while using little power. An LCD apparatus includes an LCD panel formed with liquid crystal cells and pixel elements with each associating with a corresponding liquid crystal cell and having a liquid crystal capacitor and a storage capacitor, a thin film transistor (TFT) electrically coupled with the liquid crystal capacitor and the storage capacitor. These pixel elements are substantially arranged in the form of a matrix having a number of pixel rows and a number of pixel columns. Typically, scanning signals, generated from a gate driver, are sequentially applied to the number of pixel rows, through a plurality of scanning lines along the row direction, for sequentially turning on the pixel elements row-by-row. When a scanning signal is applied to a pixel row to turn on corresponding TFTs of the pixel elements of a pixel row, source signals of an image to be displayed, generated from a source driver, for the pixel row are simultaneously applied to the number of pixel columns, through a plurality of data lines arranged crossing over the plurality of scanning lines along the column direction, so as to charge the corresponding liquid crystal capacitor and storage capacitor of the pixel row for aligning orientations of the corresponding liquid crystal cells associated with the pixel row to control light transmittance there-through. By repeating the procedure for all pixel rows, all pixel elements are supplied with corresponding source signals of the image signal, thereby displaying the image signal thereon.

[0003] Liquid crystal molecules have a definite orientational alignment as a result of their long, thin shapes. The orientations of liquid crystal molecules in liquid crystal cells of an LCD panel play a crucial role in the transmittance of light therethrough. It is known if a substantially high voltage is applied between the liquid crystal layer for a long period of time, the optical transmission characteristics of the liquid crystal molecules may change. This change may be permanent, causing an irreversible degradation in the display quality of the LCD panel. To prevent the LC molecules from being deteriorated, the polarity of the voltage signals applied on the LC cell has to be changed continuously. Usually, a source driver is configured to generate such voltage signals having their polarity alternated according to an inversion scheme such as frame inversion, row inversion, column inversion,

dot inversion, or 2-line inversion.

[0004] Typically, the display quality of an image in a dot inversion or a 2-line inversion is better than that in other inversion schemes; however, the power consumption is higher comparing to that in the other inversion schemes. The column inversion may result in a low consumption of power, but there are issues such as crosstalks and vertical flickers. For a zig-zag arrangement of pixels, the display quality of an image is similar to that of the dot inversion, while its power consumption is similar to that of the column inversion. However, crosstalks and horizontal bright and dark lines may occur in the zig-zag scheme.

[0005] Therefore, a heretofore unaddressed need exists in the art to address the aforementioned deficiencies and inadequacies.

[0006] US 2006/0092120 A1 and US 2006/0022929 A1 both describe a liquid crystal display device having a control unit, a gate driving unit, a data driving unit and a liquid crystal panel. EP 2 075 788 A2 and US 2003/227428 A1 describe alternative signal-line driving circuits for a liquid crystal display. US 2006/0092120 A1 in particular includes a LCD controlling unit which is configured to control a liquid crystal panel. The controlling unit includes an image judging unit and a method determining unit. The image judging unit is configured to compare a gradation of each pixel of image data with a reference gradation. The method determining unit is configured to determine an inversion driving method for displaying the image data on the liquid crystal panel every plurality of pixels of less than one frame in the image data as a selection inversion driving method based on the comparison result.

[0007] Starting from the state of the art it is the object of the present application to provide a source driver and a method for using the same which allows a reduction of power consumption and a improvement of imaging properties.

SUMMARY OF THE INVENTION

[0008] The above-mentioned objects are solved by the method for driving a display panel according to claim 2 and the source driver for driving a display panel according to claim 1.

[0009] In one aspect, the present invention relates to a source driver for driving a display panel to display an image data in an adaptive column inversion, where the display panel comprises a plurality of pixels spatially arranged in a matrix form and a plurality of data lines, each data line being associated with pixels of a corresponding pixel column, where the image data is decomposed into a number of frames, and each frame of the image data is mapped onto the pixel matrix with grey levels such that a grey level associated with a pixel is corresponding to the shade of grey of the frame to be displayed at the pixel.

[0010] In one embodiment, the source driver includes a data processing unit adapted for determining the grey

levels of the image data mapped onto the pixel matrix, a MUX coupled to the data processing unit and adapted for receiving a frame polarity control signal, FramePOL, and a pixel polarity control signal, XPOL, and outputting a polarity control signal, POL, that is corresponding one of FramePOL and XPOL according to the determined grey levels of the image data, and a switch module coupled to the MUX and controlled by the polarity control signal POL, a first digital-to-analog converter with a positive polarity (PDAC) adapted for receiving a first digital signal associated with the image data and converting the first digital signal into a first analog signal, a second digital-to-analog converter with a negative polarity (NDAC) adapted for receiving a second digital signal associated with the image data and converting the second digital signal into a second analog signal, a first operational amplifier coupled to the PDAC and the NDAC through the switch module and adapted for receiving one of the first analog signal from the PDAC and the second analog signal from the NDAC and outputting a first data signal to an odd data line of the plurality of data line, and a second operational amplifier coupled to the PDAC and the NDAC through the switch module and adapted for receiving the other of the first analog signal from the PDAC and the second analog signal from the NDAC and outputting a second data signal to an even data line of the plurality of data line.

[0011] In one embodiment, the data processing unit comprises a logic circuit adapted for determining N most-significant bits (MSBs) of the image data mapped onto two neighboring data lines, such that when all of the N MSBs is equal to 1 or 0, the output of the logic circuit is 1, otherwise, the output of the logic circuit is 0, N being a positive integer, where when the output of the logic circuit is 1, the MUX selects the frame polarity control signal FramePOL, and when the output of the logic circuit is 0, the MUX selects the pixel polarity control signal POL. In one embodiment, N = 4.

[0012] In one embodiment, the first and second analog signals have positive and negative polarities, respectively. The first and second data signals have positive and negative polarities, respectively.

[0013] In one embodiment, the polarity control signal POL has a low state and a high state, where when the polarity control signal POL is in the high state, each odd data line of the plurality of data line receives the first data signal, while each even data line of the plurality of data line receives the second data signal, and where when the polarity control signal POL is in the low state, each odd data line of the plurality of data line receives the second data signal, while each even data line of the plurality of data line receives the first data signal.

[0014] In another aspect, the present invention relates to a source driver for driving a display panel to display an image data in an adaptive column inversion, where the display panel comprises a plurality of pixels spatially arranged in a matrix form and a plurality of data lines, each data line being associated with pixels of a corre-

sponding pixel column, where the image data is decomposed into a number of frames, and each frame of the image data is mapped onto the pixel matrix with grey levels such that a grey level associated with a pixel is corresponding to the shade of grey of the frame to be displayed at the pixel. In one embodiment, the source driver includes a data processing unit having a logic circuit adapted for determining N MSBs of image data signals mapped onto two neighboring data lines, such that when all of the N MSBs is equal to 1 or 0, the output of the logic circuit is 1, otherwise, the output of the logic circuit is 0, where N is a positive integer, and a MUX coupled to the data processing unit and adapted for receiving a frame polarity control signal, FramePOL, and a pixel polarity control signal, XPOL, and selectively outputting the frame polarity control signal FramePOL when the output of the logic circuit is 1, or the pixel polarity control signal POL when the output of the logic circuit is 0, as a polarity control signal, POL. When the MUX selects the frame polarity control signal FramePOL, pixels of the pixel matrix associated with the neighboring data lines are driven with a column inversion, while the other pixels of the pixel matrix are driven with one of a dot inversion and a 2-line inversion.

[0015] In one embodiment, the source driver further includes a switch module coupled to the MUX and controlled by the polarity control signal POL, a PDAC adapted for receiving a first digital signal associated with the image data and converting the first digital signal into a first analog signal, a NDAC adapted for receiving a second digital signal associated with the image data and converting the second digital signal into a second analog signal, a first operational amplifier coupled to the PDAC and the NDAC through the switch module and adapted for receiving one of the first analog signal from the PDAC and the second analog signal from the NDAC and outputting a first data signal to an odd data line of the plurality of data line, and a second operational amplifier coupled to the PDAC and the NDAC through the switch module and adapted for receiving the other of the first analog signal from the PDAC and the second analog signal from the NDAC and outputting a second data signal to an even data line of the plurality of data line.

[0016] In one embodiment, the first and second analog signals have positive and negative polarities, respectively. The first and second data signals have positive and negative polarities, respectively.

[0017] In one embodiment, the polarity control signal POL has a low state and a high state, where when the polarity control signal POL is in the high state, each odd data line of the plurality of data line receives the first data signal, while each even data line of the plurality of data line receives the second data signal, and where when the polarity control signal POL is in the low state, each odd data line of the plurality of data line receives the second data signal, while each even data line of the plurality of data line receives the first data signal.

[0018] In yet another aspect, the present invention re-

lates to a method for driving a display panel to display an image data in an adaptive column inversion, where the display panel comprises a plurality of pixels spatially arranged in a matrix form and a plurality of data lines, each data line being associated with pixels of a corresponding pixel column. In one embodiment, the method comprises the steps of inputting an image data to be displayed, where the image data is decomposed into a number of frames, and each frame of the image data is mapped onto the pixel matrix with grey levels such that a grey level associated with a pixel is corresponding to the shade of grey of the frame to be displayed at the pixel, determining N MSBs of image data signals mapped onto two neighboring data lines, N being a positive integer, selecting a frame polarity control signal, FramePOL, when all of the N MSBs of the image data signals mapped onto the two neighboring data lines is equal to 1 or 0, or a pixel polarity control signal, XPOL, when the N MSBs comprise 1 and 0, as a polarity control signal, POL, and displaying the image data in a column inversion in pixels of the pixel matrix when the frame polarity control signal FramePOL is selected and in one of a dot inversion and a 2-line inversion in the other pixels of the pixel matrix when the pixel polarity control signal XPOL is selected. In one embodiment, $N = 4$.

[0019] In one embodiment, the determining step is performed with a data processing unit having a logic circuit adapted such that when all of the N MSBs is equal to 1 or 0, the output of the logic circuit is 1, otherwise, the output of the logic circuit is 0, where N is a positive integer.

[0020] In one embodiment, the selecting step is performed with a MUX adapted such that when the output of the logic circuit is 1, the MUX selects the frame polarity control signal FramePOL, and when the output of the logic circuit is 0, the MUX selects the pixel polarity control signal POL.

[0021] In a further aspect, the present invention relates to a source driver for driving a display panel to display an image data in an adaptive column inversion, wherein the display panel comprises a plurality of pixels spatially arranged in a matrix form and a plurality of data lines, each data line being associated with pixels of a corresponding pixel column, wherein the image data is decomposed into a number of frames, and wherein each frame of the image data is mapped onto the pixel matrix with grey levels such that a grey level associated with a pixel is corresponding to the shade of grey of the frame to be displayed at the pixel.

[0022] In one embodiment, the source driver comprises a data processing unit having a logic circuit adapted for determining the grey levels of image data signals mapped onto each $2n$ neighboring data lines of the plurality of data lines, such that when the determined grey levels are greater than L_m or less than L_n , the output of the logic circuit is 1, otherwise, the output of the logic circuit is 0, wherein n is a positive integer, and wherein $0 < L_n < L_m < L_{\max}$, and $L_{\max} = (2^k - 1)$ being the maximal grey level of k bits.

[0023] Further, the source driver comprises a MUX coupled to the data processing unit and adapted for receiving a frame polarity control signal, FramePOL, and a pixel polarity control signal, XPOL, and selectively outputting the frame polarity control signal FramePOL when the output of the logic circuit is 1, or the pixel polarity control signal POL when the output of the logic circuit is 0, as a polarity control signal, POL, and a plurality of driver modules coupled to the MUX, each driver module adapted for receiving two corresponding image data signals and selectively outputting them to a corresponding odd data line and a corresponding even data line of the $2n$ neighboring data lines according to the control signal POL.

[0024] In one embodiment, the logic circuit comprises a plurality of EX-NOR gates and an AND gate coupled to the plurality of EX-NOR gates, adapted for determining N most-significant bits (MSBs) of the image data signals mapped onto each $2n$ neighboring data lines, such that when all of the N MSBs are equal to 1 or 0, the output of the logic circuit is 1, otherwise, the output of the logic circuit is 0, wherein N is a positive integer.

[0025] In one embodiment, the driver module has a switch module coupled to the MUX and controlled by the polarity control signal POL, a first digital-to-analog converter with a positive polarity (PDAC) adapted for receiving a first digital signal associated with the image data and converting the first digital signal into a first analog signal, a second digital-to-analog converter with a negative polarity (NDAC) adapted for receiving a second digital signal associated with the image data and converting the second digital signal into a second analog signal, a first operational amplifier coupled to the PDAC and the NDAC through the switch module and adapted for receiving one of the first analog signal from the PDAC and the second analog signal from the NDAC and outputting a first data signal to an odd data line of the plurality of data line, and a second operational amplifier coupled to the PDAC and the NDAC through the switch module and adapted for receiving the other of the first analog signal from the PDAC and the second analog signal from the NDAC and outputting a second data signal to an even data line of the plurality of data line. In one embodiment, the first and second analog signals have positive and negative polarities, respectively. The first and second data signals have positive and negative polarities, respectively.

[0026] In one embodiment, when the MUX selects the frame polarity control signal FramePOL, pixels of the pixel matrix associated with the $2n$ neighboring data lines are driven with a column inversion, while the other pixels of the pixel matrix are driven with one of a dot inversion and a 2-line inversion.

[0027] When the determined grey levels are greater than L_m or less than L_n , the control signal POL is the frame polarity control signal FramePOL, and otherwise the polarity control signal POL is the pixel polarity control signal XPOL.

[0028] These and other aspects of the present invention will become apparent from the following description of the preferred embodiment taken in conjunction with the following drawings, although variations and modifications therein may be affected without departing from the scope of the novel concepts of the disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0029] The accompanying drawings illustrate one or more embodiments of the invention and, together with the written description, serve to explain the principles of the invention. Wherever possible, the same reference numbers are used throughout the drawings to refer to the same or like elements of an embodiment, and wherein:

Fig. 1 shows schematically a block diagram of a source driver according to one embodiment of the present invention;

Fig. 2 shows schematically (a) a logic circuit of the source driver, and (b) and (c) most-significant bits of grey levels of an image signal to be displayed;

Fig. 3 shows schematically an image displayed with (a) a 2-dot inversion and (b) an adaptive column inversion according to one embodiment of the present invention;

Fig. 4 shows schematically time charts of driving signals according to one embodiment of the present invention;

Fig. 5 shows schematically one frame of an image displayed with an adaptive column inversion according to one embodiment of the present invention;

Fig. 6 shows schematically another frame of the image displayed with the adaptive column inversion; and

Fig. 7 shows schematically a block diagram of a source driver according to another embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0030] The present invention is more particularly described in the following examples that are intended as illustrative only since numerous modifications and variations therein will be apparent to those skilled in the art. Various embodiments of the invention are now described in detail. Referring to the drawings, like numbers indicate like components throughout the views. As used in the description herein and throughout the claims that follow, the meaning of "a", "an", and "the" includes plural reference unless the context clearly dictates otherwise. Also, as used in the description herein and throughout the claims that follow, the meaning of "in" includes "in" and "on" unless the context clearly dictates otherwise.

[0031] The terms used in this specification generally have their ordinary meanings in the art, within the context of the invention, and in the specific context where each

term is used. Certain terms that are used to describe the invention are discussed below, or elsewhere in the specification, to provide additional guidance to the practitioner regarding the description of the invention. The use of examples anywhere in this specification, including examples of any terms discussed herein, is illustrative only, and in no way limits the scope and meaning of the invention or of any exemplified term. Likewise, the invention is not limited to various embodiments given in this specification.

[0032] As used herein, the term "grey level" refers to one of (discrete) shades of grey for an image, or an amount of light perceived by a human for the image. If the brightness of the image is expressed in the form of shades of grey in n bits, n being an integer greater than zero, the grey level takes values from zero representing black, up to $(2^n - 1)$ representing white, with intermediate values representing increasingly light shades of grey. In an LCD device, the amount of light that transmits through liquid crystals is adjusted to represent the grey level.

[0033] As used herein, the terms "comprising," "including," "having," "containing," "involving," and the like are to be understood to be open-ended, i.e., to mean including but not limited to.

[0034] The description will be made as to the embodiments of the present invention in conjunction with the accompanying drawings of Figs. 1-7. In accordance with the purposes of this invention, as embodied and broadly described herein, this invention, in one aspect, relates to a source driver for driving a display panel to display an image data in an adaptive column inversion. The display panel has a plurality of pixels spatially arranged in a matrix form and a plurality of data lines, each data line being associated with pixels of a corresponding pixel column. The image data is decomposed into a number of frames, where each frame of the image data is mapped onto the pixel matrix with grey levels such that a grey level associated with a pixel is corresponding to the shade of grey of the frame to be displayed at the pixel. In other words, the image data is processed by for example, a video device (not shown), into a plurality of image data signals expressed in the form of grey levels in k bits, and each image data signal is input to a corresponding data line for display in a pixel column associated with the corresponding data line. For example, for a 4-bit, an image data signal in a pixel can be expressed in one of $2^4 = 64$ grey levels depending the shades of grey of the image in the pixel.

[0035] Referring to Fig. 1, a source driver 100 is shown according to one embodiment of the present invention. The source driver 100 includes, among other components, a data processing unit 110, a MUX 120 coupled to the data processing unit 110, a switch module 130 coupled to the MUX 120, a first digital-to-analog converter with a positive polarity (PDAC) 141, a second digital-to-analog converter with a negative polarity (NDAC) 142, and a first operational amplifier 151 and a second operational amplifier 152 coupled to the PDAC 141 and the

NDAC 142 through the switch module 130.

[0036] The data processing unit 110 is adapted for determining the grey levels of the image data 190 mapped onto the pixel matrix, so as to select one or more inversion driving methods to drive the display panel to display the image. In one embodiment, the data processing unit 110 determines the grey levels of image data signals 190 associated with (or input to) two neighboring data lines 171 and 172. Alternatively, as shown below, the data processing unit 110 determines N most-significant bits (MSBs) of the image data signals 190.

[0037] The MUX 120 is adapted for receiving a frame polarity control signal, FramePOL, and a pixel polarity control signal, XPOL, and outputting a polarity control signal, POL, that is corresponding one of FramePOL and XPOL according to the determined grey levels of the image data. For example, when the determined grey levels are greater than L_m or less than L_n , the polarity control signal POL is the frame polarity control signal FramePOL, and otherwise the polarity control signal POL is the pixel polarity control signal XPOL, where $0 < L_n < L_m < L_{max}$, and $L_{max} = (2^k - 1)$ being the maximal grey level of k bits. L_n and L_m are two predetermined grey levels. Alternatively, when the determined grey levels are greater than L_m or less than L_n , pixels of the pixel matrix associated with the determined grey levels are driven with a column inversion, and the other pixels of the pixel matrix are driven with one of a dot inversion and a 2-line inversion. The pixel polarity control signal XPOL is generated from a timing controller (T-con, not shown) and used to determine a data inversion scheme.

[0038] The switch module 130 may include a pair of switches SW1 and SW2 that are coupled to the PDAC 141, the NDAC 142, the first operational amplifier 151 and the second operational amplifier 152 and controlled by the polarity control signal POL. For example, when the polarity control signal POL is in a high state (H), the output signals of the PDAC 141, the NDAC 142 are respectively delivered to the first operational amplifier 151 and the second operational amplifier 152. Otherwise, when the polarity control signal POL is in a low state (L), the output signals of the PDAC 141, the NDAC 142 are respectively delivered to the second operational amplifier 152 and the first operational amplifier 151.

[0039] The PDAC 141 is adapted for receiving a first digital signal 191 of the image data and converting the first digital signal 191 into a first analog signal. The NDAC 142 is adapted for receiving a second digital signal 192 of the image data and converting the second digital signal 192 into a second analog signal. The image data 190 and the first digital signal 191 and the second digital signal 192 are processed of the image to be displayed. In one embodiment, the image data 190 includes at least the first digital signal 191 and the second digital signal 192. The first and second analog signals have positive and negative polarities, respectively. The first operational amplifier 151 and the second operational amplifier 152 are coupled to the PDAC 141 and the NDAC 142 through

the switch module 130. The first operational amplifier 151 is adapted for receiving one of the first analog signal from the PDAC 141 and the second analog signal from the NDAC 142, and outputting a first data signal to an odd data line 161, while the second operational amplifier 152 is adapted for receiving the other of the first analog signal from the PDAC 141 and the second analog signal from the NDAC 142 and outputting a second data signal to an even data line 162. The first and second data signals have positive and negative polarities, respectively.

[0040] In operation, when the polarity control signal POL is in the high state (H), the odd data line 161 receives the first data signal, while the even data line 162 receives the second data signal, and when the polarity control signal POL is in the low state (L), the odd data line 161 receives the second data signal, while the even data line 162 receives the first data signal.

[0041] In one embodiment, the data processing unit 110 includes a logic circuit for determining N MSBs of the image data mapped onto two neighboring data lines. As shown in Fig. 2(a), the logic circuit includes a first EX-NOR gate 111, a second EX-NOR gate 112 and an AND gate 113 coupled to each other. In the exemplary embodiment, $N = 4$. The output of the first EX-NOR gate 111 (or the second EX-NOR gate 112) is true, indicated by 1, only when all of four inputs are the same, i.e., all of the four inputs are 0 or all of the four inputs are 1 in the binary. Otherwise, it is false. Additionally, the output of the AND gate 113 is true, indicated by 1, only when all of the outputs of the first EX-NOR gate 111 and the second EX-NOR gate 112 are true (1). The first EX-NOR gate 111 and the second EX-NOR gate 112 are utilized to determine four (4) MSBs of data signals of two neighboring data lines, respectively.

[0042] When all of the four MSBs, indicated by A, B, C and D, respectively, of the data signals are equal to 1, as shown in Fig. 2(b) or 0, as shown in Fig. 2(c), the output of the logic circuit is true, indicated by 1. Otherwise, the output of the logic circuit is false, indicated by 0. When the output of the logic circuit is true, 1, the MUX selects the frame polarity control signal FramePOL as the polarity control signal POL, i.e., a column inversion. When the output of the logic circuit is false, the MUX selects the pixel polarity control signal XPOL as the polarity control signal POL, i.e., a dot inversion or a 2-dot inversion.

[0043] Fig. 3(a) shows schematically an image displayed with a 2-dot inversion. Fig. 3(b) shows schematically the image displayed with an adaptive column inversion, that is, S1 and S2 columns are in the column inversion, and S3 and S4 column are in the 2-dot inversion.

[0044] Referring to Fig. 4, time charts of driving/control signals are shown according to one embodiment of the present invention. In the charts, YDIO is corresponding to a start pulse of image frames. Each frame has a polarity, FramePOL, which is opposite to that of its immediately prior and/or next frame. In other words, Frame-

POL changes every frame. XSTB rising edge latch XPOL determines the polarity of each horizontal line.

[0045] Figs. 5 and 6 are two consecutive frames of an image displayed with an adaptive column inversion. The grey levels of the image in area 520 are near or close to the maximal grey level, i.e., greater than a predetermined value, for example, $L_m = L_{59}$, FramePOL is adapted to control the PDAC, the NDAC, the first and second operational amplifiers, accordingly, the image is displayed in a column inversion. Further, the grey levels of the image in area 530 are near or close to the minimal grey level, i.e., less than a predetermined value, for example, $L_n = L_4$, FramePOL is adapted to control the PDAC, the NDAC, the first and second operational amplifiers, accordingly, the image is displayed in a column inversion. However, when the grey levels of the image are between $L_n = L_4$ and $L_m = L_{59}$, XPOL is adapted to control the PDAC, the NDAC, the first and second operational amplifiers, accordingly, the image is displayed in a 2-dot column inversion, as indicated in area 510.

[0046] In another aspect, the present invention relates to a method for driving a display panel to display an image data in an adaptive column inversion. In one embodiment, the method includes the following steps: at first, an image data to be displayed is provided. The image data is decomposed into a number of frames, where each frame of the image data is mapped onto the pixel matrix with grey levels such that a grey level associated with a pixel is corresponding to the shade of grey of the frame to be displayed at the pixel.

[0047] Then, N MSBs of image data signals mapped onto two neighboring data lines are determined.

[0048] Next, when all of the N MSBs of the image data signals mapped onto the two neighboring data lines is equal to 1 or 0, a frame polarity control signal FramePOL is selected as a polarity control signal POL, or when the N MSBs comprise 1 and 0, a pixel polarity control signal XPOL is selected as the polarity control signal, POL.

[0049] The image data is displayed in a column inversion in pixels of the pixel matrix when the frame polarity control signal FramePOL is selected and in one of a dot inversion and a 2-line inversion in the other pixels of the pixel matrix when the pixel polarity control signal XPOL is selected.

[0050] In one embodiment, the determining step is performed with a data processing unit having a logic circuit adapted such that when all of the N MSBs is equal to 1 or 0, the output of the logic circuit is 1, otherwise, the output of the logic circuit is 0, wherein N is a positive integer. The selecting step is performed with a MUX adapted such that when the output of the logic circuit is 1, the MUX selects the frame polarity control signal FramePOL, and when the output of the logic circuit is 0, the MUX selects the pixel polarity control signal POL.

[0051] Fig. 7 shows schematically a block diagram of a source driver 700 according to another embodiment of the present invention. In this embodiment, the source driver 700 comprises a data processing unit 710, a MUX

720 coupled to the data processing unit 710, and a plurality of driver modules, DM1, DM2, ..., DMn, 780 coupled to the MUX 720.

[0052] The data processing unit 710 included a logic circuit adapted for determining the grey levels of image data signals mapped onto each 2n neighboring data lines, S1, S2, ..., S2n, of the plurality of data lines, such that when the determined grey levels are greater than L_m or less than L_n , the output of the logic circuit is 1, otherwise, the output of the logic circuit is 0, where n is a positive integer, and $0 < L_n < L_m < L_{max}$, and $L_{max} = (2^k - 1)$ being the maximal grey level of k bits.

[0053] As shown in Fig. 7, the logic circuit includes 2n EX-NOR gates, D1, D2, ..., D2n, and an AND gate coupled to the 2n EX-NOR gates, D1, D2, ..., D2n. Each EX-NOR gate is configured to receive a corresponding image data signal and output 0 or 1 based on the input image data signal. Specifically, if all of N most-significant bits (MSBs) of the input image data signal are equal to 1, or 0, the EX-NOR gate outputs 1, otherwise, it outputs 0. When all of N most-significant bits (MSBs) of the input image data signal are equal to 1, the grey levels of the input image data signal are greater than L_m . When all of N most-significant bits (MSBs) of the input image data signal are equal to 0, the grey levels of the input image data signal are less than L_n .

[0054] For such a logic circuit, when each and every EX-NOR gate outputs 1 or 0, the output of the logic circuit is 1, otherwise, the output of the logic circuit is 0.

[0055] The MUX 720 is coupled to the logic circuit and adapted for receiving a frame polarity control signal, FramePOL, and a pixel polarity control signal, XPOL. When the output of the logic circuit is 1, the MUX 720 selects the frame polarity control signal FramePOL as the polarity control signal POL, i.e., a column inversion. When the output of the logic circuit is 0, the MUX 720 selects the pixel polarity control signal XPOL as the polarity control signal POL, i.e., a dot inversion or a 2-dot inversion.

[0056] Each driver module 780 is adapted for receiving two corresponding image data signals 791 and 792 and selectively outputting them to a corresponding odd data line 761 and a corresponding even data line 762 of the 2n neighboring data lines, S1, S2, ..., S2n, according to the control signal POL. The corresponding odd data line 761 is one of S1, S3, ..., S2n-1, while the corresponding even data line 762 is one of S2, S4, ..., S2n.

[0057] The driver module 780 has a switch module 730 coupled to the MUX 720, a first digital-to-analog converter with a positive polarity (PDAC) 741, a second digital-to-analog converter with a negative polarity (NDAC) 742, and a first operational amplifier 751 and a second operational amplifier 752 coupled to the PDAC 741 and the NDAC 742 through the switch module 730.

[0058] The switch module 730 may include a pair of switches SW1 and SW2 that are coupled to the PDAC 741, the NDAC 742, the first operational amplifier 751 and the second operational amplifier 752 and controlled

by the polarity control signal POL. For example, when the polarity control signal POL is in a high state (H), the output signals of the PDAC 741, the NDAC 742 are respectively delivered to the first operational amplifier 751 and the second operational amplifier 752. Otherwise, when the polarity control signal POL is in a low state (L), the output signals of the PDAC 741, the NDAC 742 are respectively delivered to the second operational amplifier 752 and the first operational amplifier 751.

[0059] The PDAC 741 is adapted for receiving a first digital signal 791 of the image data and converting the first digital signal 791 into a first analog signal. The NDAC 742 is adapted for receiving a second digital signal 792 of the image data and converting the second digital signal 792 into a second analog signal. The image data 790 and the first digital signal 791 and the second digital signal 792 are processed of the image to be displayed. In one embodiment, the image data 790 includes at least the first digital signal 791 and the second digital signal 792. The first and second analog signals have positive and negative polarities, respectively. The first operational amplifier 751 and the second operational amplifier 752 are coupled to the PDAC 741 and the NDAC 742 through the switch module 730. The first operational amplifier 751 is adapted for receiving one of the first analog signal from the PDAC 741 and the second analog signal from the NDAC 742, and outputting a first data signal to an odd data line 761, while the second operational amplifier 752 is adapted for receiving the other of the first analog signal from the PDAC 741 and the second analog signal from the NDAC 742 and outputting a second data signal to an even data line 762. The first and second data signals have positive and negative polarities, respectively.

[0060] In operation, when the MUX selects the frame polarity control signal FramePOL, pixels of the pixel matrix associated with the 2n neighboring data lines S1, S2, ..., S2n, are driven with a column inversion, while the other pixels of the pixel matrix are driven with one of a dot inversion and a 2-line inversion.

[0061] According to the present invention, the display quality of an image in a display device can be substantially improved, while the power consumption can be reduced significantly.

[0062] The foregoing description of the exemplary embodiments of the invention has been presented only for the purposes of illustration and description and is not intended to be exhaustive or to limit the invention to the precise forms disclosed. Many modifications and variations are possible in light of the above teaching.

[0063] The embodiments were chosen and described in order to explain the principles of the invention and their practical application so as to activate others skilled in the art to utilize the invention and various embodiments and with various modifications as are suited to the particular use contemplated. Alternative embodiments will become apparent to those skilled in the art to which the present invention pertains without departing from its scope. Accordingly, the scope of the present invention is defined

by the appended claims rather than the foregoing description and the exemplary embodiments described therein.

Claims

1. A source driver (100) for driving a display panel to display an image data (190) in an adaptive column inversion, wherein the display panel comprises a plurality of pixels spatially arranged in a matrix form and a plurality of data lines, each data line being associated with pixels of a corresponding pixel column, wherein the image data (190) is decomposed into a number of frames, and wherein each frame of the image data (190) is mapped onto the pixel matrix with grey levels such that a grey level associated with a pixel is corresponding to the shade of grey of the frame to be displayed at the pixel, comprising:

(a) a data processing unit (110, 710) adapted for determining the grey levels of image data signals mapped onto the pixel matrix, wherein the data processing unit (110, 710) comprises a logic circuit, and the logic circuit comprises a first gate (111), a second gate (112) and an AND gate (113) coupled to the first gate (111) and the second gate (112), wherein the logic circuit is adapted for determining N most-significant bits (MSBs) of the image data mapped onto two neighboring data lines and to provide N MSBs to the first gate and the second gate respectively, wherein when all of the N MSBs inputted to the first gate (111) are equal to 1 or when all of the N MSBs inputted to the first gate (111) are equal to 0, the output of the first gate (111) is 1, otherwise, the output of the first gate (111) is 0, wherein when all of the N MSBs inputted to the second gate (112) are equal to 1 or when all of the N MSBs inputted to the second gate (112) are equal to 0, the output of the second gate (112) is 1, otherwise, the output of the second gate (112) is 0, wherein when the outputs of the first gate (111) and the second gate (112) are 1, the output of the AND gate (113) is 1, otherwise, the output of the AND gate (113) is 0;

(b) a MUX (120, 720) coupled to the data processing unit (110, 710) and adapted for receiving a frame polarity control signal, FramePOL, and a pixel polarity control signal, XPOL, and outputting a polarity control signal, POL, that is corresponding to one of FramePOL and XPOL according to the determined grey levels of the image data (190), wherein, when the output of the logic circuit is 1, the MUX (120, 720) selects the frame polarity control signal FramePOL, and, when the output of the logic circuit is 0, the MUX (120, 720) selects the pixel polarity control

signal XPOL, wherein, when the MUX (120, 720) selects the frame polarity control signal FramePOL, pixels of the pixel matrix associated with the neighboring data lines are driven with a column inversion by one driver module (780), while when the MUX (120, 720) selects the pixel polarity control signal XPOL, pixels of the pixel matrix associated with the neighboring data lines are driven with one of a dot inversion and a 2-line inversion by the driver module (780); and (c) a plurality of driver modules (780) coupled to the MUX (120, 720), each driver module (780) comprising:

- (a) a switch module (130, 730) coupled to the MUX (120, 720) and controlled by the polarity control signal POL;
- (b) a first digital-to-analog converter (141, 741) with a positive polarity (PDAC) adapted for receiving a first digital signal (191, 791) associated with the image data and converting the first digital signal (191, 791) into a first analog signal;
- (c) a second digital-to-analog converter (142, 742) with a negative polarity (NDAC) adapted for receiving a second digital signal (192, 792) associated with the image data and converting the second digital signal (192, 792) into a second analog signal;
- (d) a first operational amplifier (151, 751) coupled to the PDAC and the NDAC through the switch module (130, 730) and adapted for receiving one of the first analog signal from the PDAC and the second analog signal from the NDAC and outputting a first data signal to an odd data line (161, 761) of the plurality of data lines; and
- (e) a second operational amplifier (152, 752) coupled to the PDAC and the NDAC through the switch module (130, 730) and adapted for receiving the other of the first analog signal from the PDAC and the second analog signal from the NDAC and outputting a second data signal to an even data line (162, 762) of the plurality of data lines,

the switch module (130, 730) being adapted such that the first operational amplifier (151, 751) is coupled to the PDAC through the switch module (130, 730), when the polarity control signal POL is in a high state (H), and that the first operational amplifier (151, 751) is coupled to the NDAC through the switch module (130, 730) when the polarity control signal POL is in a low state (L), that the second operational amplifier (152, 752) is coupled to the PDAC through the switch module (130, 730) when the polarity control signal POL is in the low state (L), and that

the second operational amplifier (152, 752) is coupled to the NDAC through the switch module (130, 730) when the polarity control signal POL is in the high state (H), wherein the first and second analog signals have positive and negative polarities, respectively.

2. A method for driving a display panel to display an image data in an adaptive column inversion, wherein the display panel comprises a plurality of pixels spatially arranged in a matrix form and a plurality of data lines, each data line being associated with pixels of a corresponding pixel column, the display panel further comprising a source driver according to claim 1, the method further comprising the steps of:

- (a) inputting an image data (190) to be displayed, wherein the image data (190) is decomposed into a number of frames, and wherein each frame of the image data (190) is mapped onto the pixel matrix with grey levels such that a grey level associated with a pixel is corresponding to the shade of grey of the frame to be displayed at the pixel;
- (b) determining N most-significant bits (MSBs) of image data signals (191, 192, 791, 792) mapped onto two neighboring data lines (161, 162), N being a positive integer ;
- (c) selecting on of a frame polarity control signal, FramePOL, and a pixel polarity control signal, XPOL, using the logic circuit of the source driver;
- (d) displaying the image data (190) in a column inversion in a part of the pixels of the pixel matrix associated with the neighboring data lines when the frame polarity control signal FramePOL is selected and in one of a dot inversion and a 2-line inversion in the part of the pixels of the pixel matrix associated with the neighboring data lines when the pixel polarity control signal XPOL is selected.

Patentansprüche

1. Quelltreiber (100) zur Ansteuerung eines Anzeigepanels zur Anzeige von Bilddaten (190) mit einer adaptiven Spalteninversion, wobei das Anzeigepanel eine Vielzahl von Pixeln, die räumlich in einer Matrixform angeordnet sind, und eine Vielzahl von Datenleitungen umfasst, wobei jede Datenleitung den Pixeln einer korrespondierenden Pixelspalte zugeordnet ist, wobei die Bilddaten (190) in eine Mehrzahl von Datenübertragungsblöcken (Frames) zerlegt werden, und wobei jeder Datenübertragungsblock der Bilddaten (190) mit Grauwerten auf die Pixelmatrix abgebildet wird, sodass ein mit einem Pixel assoziierter Grauwert der Grauschattierung des Datenübertragungsblocks, der an dem Pixel angezeigt

werden soll, entspricht, umfassend:

(a) eine Datenverarbeitungseinheit (110, 710),
die ausgebildet ist, die Grauwerte der auf die
Pixelmatrix abgebildeten Bilddatensignale zu
bestimmen, wobei die Datenverarbeitungsein- 5
heit (110, 710) eine Logikschaltung umfasst,
und wobei die Logikschaltung ein erstes Gatter
(111), ein zweites Gatter (112) und ein UND-
Gatter (AND gate) (113) umfasst, das mit dem 10
ersten Gatter (111) und dem zweiten Gatter
(112) gekoppelt ist, wobei die Logikschaltung
zur Bestimmung der N höchstsignifikantesten
Bits (MSBs) der auf zwei benachbarte Datenlei- 15
tungen abgebildeten Bilddaten und zur jeweili-
gen Bereitstellung der N MSBs an das erste Gat-
ter und das zweite Gatter ausgebildet ist, wobei,
wenn alle der N MSBs, die in das erste Gatter
(111) eingespeist werden, gleich 1 sind oder 20
wenn alle der in das erste Gatter (111) einge-
speisten N MSBs gleich 0 sind, die Ausgabe des
ersten Gatters (111) 1 ist, wobei ansonsten die
Ausgabe des ersten Gatters (111) 0 ist, wobei,
wenn alle der N MSBs, die in das zweite Gatter
(112) eingespeist werden, gleich 1 sind oder 25
wenn alle der in das zweite Gatter (112) einge-
speisten N MSBs gleich 0 sind, die Ausgabe des
zweiten Gatters (112) 1 ist, wobei ansonsten die
Ausgabe des zweiten Gatters (112) 0 ist, wobei 30
die Ausgabe des UND-Gatters (113) 1 ist, wenn
die Ausgaben des ersten Gatters (111) und des
zweiten Gatters (112) 1 sind, wobei ansonsten
die Ausgabe des UND-Gatters (113) 0 ist,
(b) einen Multiplexer (MUX) (120, 720), der mit 35
der Datenverarbeitungseinheit (110, 710) ge-
koppelt ist und konfiguriert ist, ein Polaritätskon-
trollsignal für den Datenübertragungsblock (Fra-
me), FramePOL, und ein Pixelpolaritätskontroll-
signal, XPOL, zu empfangen und ein Polaritäts- 40
kontrollsignal, POL, auszugeben, das gemäß
den ermittelten Grauwerten der Bilddaten (190)
entweder dem FramePOL oder dem XPOL ent-
spricht, wobei, wenn die Ausgabe der Logik-
schaltung 1 ist, der MUX (120, 720) das Polari- 45
tätskontrollsignal für den Datenübertragungs-
block, FramePOL, auswählt, und wobei, wenn
die Ausgabe der Logikschaltung 0 ist, der MUX
(120, 720) das Pixelpolaritätskontrollsignal,
XPOL, auswählt, wobei, wenn der MUX (120, 50
720) das Polaritätskontrollsignal für den Daten-
übertragungsblock, FramePOL, auswählt, die
Pixel der Pixelmatrix, die den benachbarten Da-
tenleitungen zugeordnet sind, durch ein Treiber-
modul (780) mit einer Spalteninversion ange- 55
steuert werden, wohingegen, wenn der MUX
(120, 720) das Pixelpolaritätskontrollsignal,
XPOL, auswählt, die Pixel der Pixelmatrix, die
den benachbarten Datenleitungen zugeordnet

sind, durch das Treibermodul (780) entweder
mit einer Punktinversion oder einer 2-Zeilenin-
version angesteuert werden, und
(c) eine Mehrzahl an Treibermodulen (780), die
mit dem MUX (120, 720) gekoppelt sind, wobei
jedes Treibermodul (780) umfasst:

(a) ein Schaltmodul (130, 730), das mit dem
MUX (120, 720) gekoppelt ist und durch das
Polaritätskontrollsignal POL gesteuert wird,
(b) einen ersten Digital-zu-Analog-Konver-
ter (141, 741) mit einer positiven Polarität
(PDAC), der ausgebildet ist, ein erstes di-
gitales Signal (191, 791), das den Bilddaten
zugeordnet ist, zu empfangen und das erste
digitale Signal (191, 791) in ein erstes Ana-
logsignal umzuwandeln,
(c) einen zweiten Digital-zu-Analog-Kon-
verter (142, 742) mit einer negativen Polarität
(NDAC), der ausgebildet ist, ein zweites di-
gitales Signal (192, 792), das den Bilddaten
zugeordnet ist, zu empfangen und das
zweite digitale Signal (192, 792) in ein zwei-
tes Analogsignal umzuwandeln,
(d) einen ersten Operationsverstärker (151,
751), der mit dem PDAC und dem NDAC
durch das Schaltmodul (130, 730) verbun-
den ist und ausgebildet ist, entweder das
erste Analogsignal von dem PDAC oder das
zweite Analogsignal von dem NDAC zu
empfangen und ein erstes Datensignal an
eine ungerade Datenleitung (161, 761) der
Vielzahl von Datenleitungen auszugeben,
und
(e) einen zweiten Operationsverstärker
(152, 752), der mit dem PDAC und dem
NDAC durch das Schaltmodul (130, 730)
verbunden ist und ausgebildet ist, das üb-
rigbleibende erste Analogsignal von dem
PDAC oder zweite Analogsignal von dem
NDAC zu empfangen kann und ein zweites
Datensignal an eine gerade Datenleitung
(162, 762) der Vielzahl von Datenleitungen
auszugeben,

wobei das Schaltmodul (130, 730) derart konfi-
guriert ist,
dass der erste Operationsverstärker (151, 751)
durch das Schaltmodul (130, 730) mit dem
PDAC verbunden ist, wenn das Polaritätskon-
trollsignal POL in einem hohen Zustand (H) ist,
und
dass der erste Operationsverstärker (151, 751)
durch das Schaltmodul (130, 730) mit dem
NDAC verbunden ist, wenn das Polaritätskon-
trollsignal POL in einem niedrigen Zustand (L) ist,
dass der zweite Operationsverstärker (152,
752) durch das Schaltmodul (130, 730) mit dem

PDAC verbunden ist, wenn das Polaritätskontrollsignal POL in dem niedrigen Zustand (L) ist, und

dass der zweite Operationsverstärker (152, 752) durch das Schaltmodul (130, 730) mit dem NDAC verbunden ist, wenn das Polaritätskontrollsignal POL in dem hohen Zustand (H) ist, wobei das erste und das zweite Analogsignal jeweils positive und negative Polaritäten haben.

2. Verfahren zur Ansteuerung eines Anzeigepanels zur Anzeige von Bilddaten mit einer adaptiven Spalteninversion, wobei das Anzeigepanel eine Vielzahl von Pixeln, die räumlich in einer Matrixform angeordnet sind, und eine Vielzahl von Datenleitungen umfasst, wobei jede Datenleitung den Pixeln einer korrespondierenden Pixelspalte zugeordnet ist, wobei das Anzeigepanel ferner einen Quelltreiber nach Anspruch 1 umfasst, wobei das Verfahren außerdem die folgende Schritte umfasst:

(a) Eingabe von Bilddaten (190), welche angezeigt werden sollen, wobei die Bilddaten (190) in eine Mehrzahl von Datenübertragungsblöcken (Frames) zerlegt werden, und wobei jeder Datenübertragungsblock der Bilddaten (190) mit Grauwerten auf die Pixelmatrix derart abgebildet wird, dass ein einem Pixel zugeordneter Grauwert der Grauschattierung des Datenübertragungsblocks entspricht, der an dem Pixel angezeigt werden soll,

(b) Ermittlung der N höchstsignifikantesten Bits (MSBs) der Bilddatensignale (191, 192, 791, 792), die auf zwei benachbarte Datenleitungen (161, 162) abgebildet werden, wobei N eine positive ganze Zahl ist,

(c) Auswahl von entweder dem Polaritätskontrollsignal für den Datenübertragungsblock, FramePOL, oder dem Pixelpolaritätskontrollsignal, XPOL, unter Verwendung der Logikschaltung des Quelltreibers,

(d) Anzeige der Bilddaten (190) in einer Spalteninversion in einem den benachbarten Datenleitungen zugeordneten Teil der Pixel der Pixelmatrix, wenn das Polaritätskontrollsignal für den Datenübertragungsblock, FramePOL, ausgewählt wird, oder in entweder einer Punktinversion oder einer 2-Zeileninversion in dem den benachbarten Datenleitungen zugeordneten Teil der Pixel der Pixelmatrix, wenn das Pixelpolaritätskontrollsignal, XPOL, ausgewählt wird.

Revendications

1. Pilote source (100) pour commander un panneau d'affichage pour afficher des données d'image (190) dans une inversion de colonne adaptative, le pan-

neau d'affichage comprenant une pluralité de pixels arrangés spatialement dans une forme matricielle et une pluralité de lignes de données, chaque ligne de données étant associée à des pixels d'une colonne de pixels correspondante, les données d'image (190) étant décomposées dans un certain nombre de cadres et chaque cadre des données d'image (190) étant mappé sur la matrice de pixels avec des niveaux de gris de telle manière qu'un niveau de gris associé à un pixel correspond à la teinte de gris du cadre devant être affichée sur le pixel comprenant :

(a) une unité de traitement de données (110, 710) adaptée pour déterminer les niveaux de gris des signaux de données d'image mappés sur la matrice de pixels, l'unité de traitement de données (110, 710) comprenant un circuit logique et le circuit logique comprenant une première porte (111), une seconde porte (112) et une porte ET (113) couplée à la première porte (111) et à la seconde porte (112), le circuit logique étant adapté pour déterminer N bits les plus significatifs (MSB) des données d'image mappées sur deux lignes de données voisines et pour fournir N MSB respectivement à la première porte et à la seconde porte, dans laquelle, lorsque tous les N MSB entrés à la première porte (111) sont égaux à 1 ou quand tous les N MSB entrés à la première porte (111) sont égaux à 0, la sortie de la première porte (111) est 1, sinon la sortie de la première porte (111) est 0, dans laquelle, lorsque tous les N MSB entrés à la seconde porte (112) sont égaux à 1 ou lorsque tous les N MSB entrés à la seconde porte (112) sont égaux à 0, la sortie de la seconde porte (112) est 1, sinon la sortie de la seconde porte (112) est 0, dans laquelle, quand les sorties de la première porte (111) et de la seconde porte (112) sont 1, la sortie de la porte ET (113) est 1, sinon la sortie de la porte ET (113) est 0 ;

(b) un MUX (120, 720) couplé à l'unité de traitement de données (110, 710) et adapté pour recevoir un signal de commande de polarité du cadre, FramePOL, et un signal de commande de polarité de pixel, XPOL, et pour sortir un signal de commande de polarité, POL, qui correspond à l'un des signaux FramePOL et XPOL selon les niveaux de gris déterminés des données d'image (190), dans lequel, lorsque la sortie du circuit logique est 1, le MUX (120, 720) sélectionne le signal de commande de polarité du cadre FramePOL et, lorsque la sortie du circuit logique est 0, le MUX (120, 720) sélectionne le signal de commande de polarité de pixels XPOL, dans lequel, lorsque le MUX (120, 720) sélectionne le signal de commande de polarité de cadre FramePOL, des pixels de la matrice de pixels associés aux lignes de données voisi-

nes sont commandées avec une inversion de colonne par un module de pilote (780) tandis que, lorsque le MUX (120, 720) sélectionne le signal de commande de polarité de pixel XPOL, des pixels de la matrice de pixels associés aux lignes de données voisines sont commandées avec l'une des inversions, une inversion de points et une inversion de 2 lignes par le module de pilote (780) et

(c) une pluralité de modules de pilote (780) couplés au MUX (120, 720), chaque module de pilote (780) comprenant :

(a) un module de commutation (130, 730) couplé au MUX (120, 720) et commandé par le signal de commande de polarité POL ;

(b) un premier convertisseur numérique-analogique (141, 741) avec une polarité positive (PDAC) adaptée pour recevoir un premier signal numérique (191, 791) associé aux données d'image et pour convertir le premier signal numérique (191, 891) en un premier signal analogique ;

(c) un second convertisseur numérique-analogique (142, 742) avec une polarité négative (NDAC) adaptée pour recevoir un second signal numérique (192, 792) associé aux données d'image et pour convertir le second signal numérique (192, 792) en un second signal analogique ;

(d) un premier amplificateur opérationnel (151, 751) couplé au PDAC et au NDAC par le module de commutation (130, 730) et adapté pour recevoir l'un des signaux, le premier signal analogique du PDAC et le second signal analogique du NDAC et pour sortir un premier signal de données à une ligne de données impaire (161, 761) de la pluralité des lignes de données et

(e) un second amplificateur opérationnel (152, 752) couplé au PDAC et au NDAC par le module de commutation (130, 730) et adapté pour recevoir l'autre signal, le premier signal analogique du PDAC et le second signal analogique du NDAC et pour sortir un second signal de données à une ligne de données paire (162, 762) de la pluralité de lignes de données,

le module de commutation (130, 730) étant adapté de telle manière que le premier amplificateur opérationnel (151, 751) est couplé au PDAC par le module de commutation (130, 730) lorsque le signal de commande de polarité POL est à l'état haut (H) et que le premier amplificateur opérationnel (151, 171) est couplé au NDAC par le module de commutation (130, 730)

lorsque le signal de commande de polarité POL est dans un état bas (L), que le second amplificateur opérationnel (152, 752) est couplé au PDAC par le module de commutation (130, 730) lorsque le signal de commande de polarité POL est à l'état bas (L) et que le second amplificateur opérationnel (152, 752) est couplé au NDAC par le module de commutation (130, 730) lorsque le signal de commande de polarité POL est à l'état haut (H), le premier et le second signal analogique ayant respectivement des polarités positives et négatives.

2. Procédé pour commander un panneau d'affichage pour afficher des données d'image dans une inversion de colonne adaptative, le panneau d'affichage comprenant une pluralité de pixels arrangés spatialement dans une forme matricielle et une pluralité de lignes de données, chaque ligne de données étant associée à des pixels d'une colonne de pixels correspondante, le panneau d'affichage comprenant de plus un pilote source selon la revendication 1, le procédé comprenant de plus les étapes :

(a) d'entrée de données d'image (190) à afficher, les données d'image (190) étant décomposées en un certain nombre de cadres et chaque cadre de données d'image (190) étant mappé sur la matrice de pixels avec des niveaux de gris de telle manière qu'un niveau de gris associé à un pixel correspond à la teinte de gris du cadre devant être affichée sur le pixel ;

(b) de détermination de N bits les plus significatifs (MSB) des signaux de données d'image (191, 192, 791, 792) mappés sur deux lignes de données voisines (161, 162), N étant un nombre entier positif ;

(c) de sélection d'un des signaux de commande, le signal de polarité de cadre, FramePOL, et un des signaux de commande de polarité de pixels, XPOL, utilisant le circuit logique du pilote source ;

(d) d'affichage des données d'image (190) dans une inversion de colonne dans une partie des pixels de la matrice de pixels associée aux lignes de données voisines lorsque le signal de commande de polarité de cadre FramePOL est sélectionné et dans l'une des inversions, l'inversion de points et l'inversion de 2 lignes dans la partie des pixels de la matrice de pixels qui est associée aux lignes de données voisines lorsque le signal de commande de polarité de pixels XPOL est sélectionné.

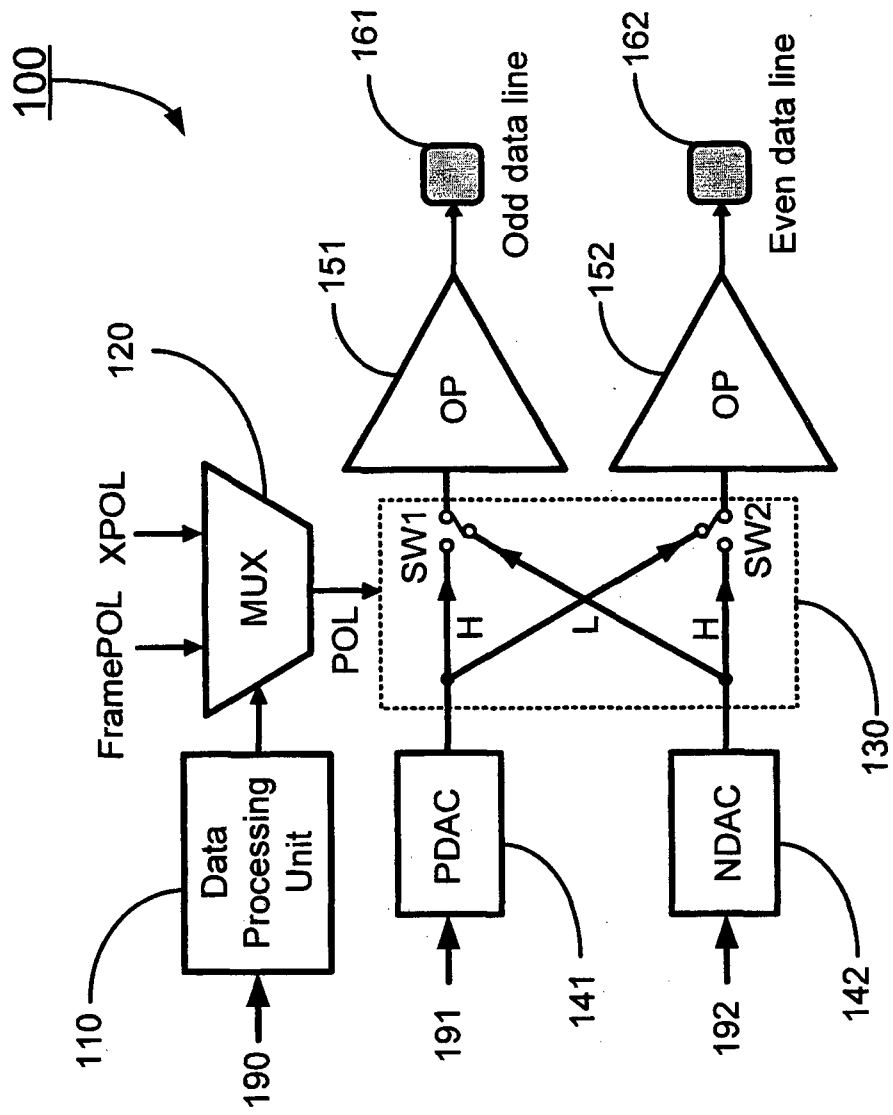
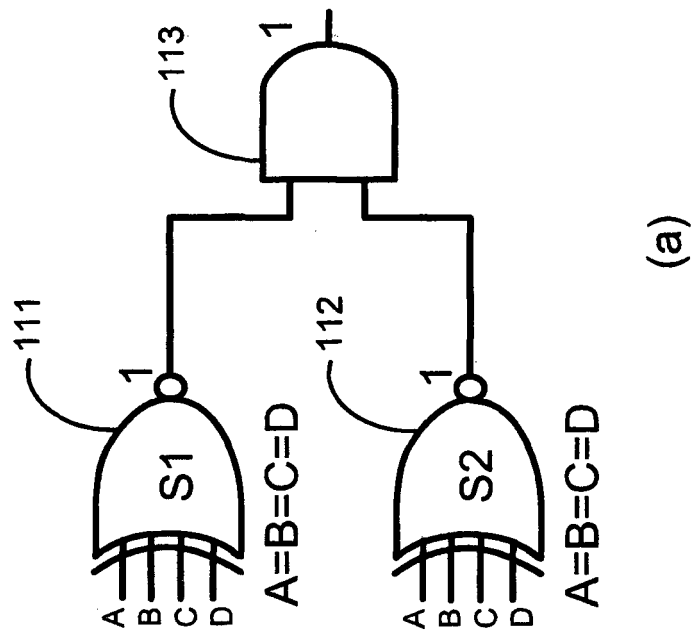


Fig. 1



(b)

Grey Levels	ABCD
L60	111100
L61	111101
L62	111110
L63	111111

Grey Levels in binary

(c)

Grey Levels	ABCD
L00	000000
L01	000001
L02	000010
L03	000011

Grey Levels in binary

Fig. 2

S1	S2	S3	S4
+	-	+	-
+	+	-	-
+	-	-	+
+	+	-	+

(b)

S1	S2	S3	S4
+	-	+	-
+	+	-	-
-	-	+	+
-	+	-	+

(a)

Fig. 3

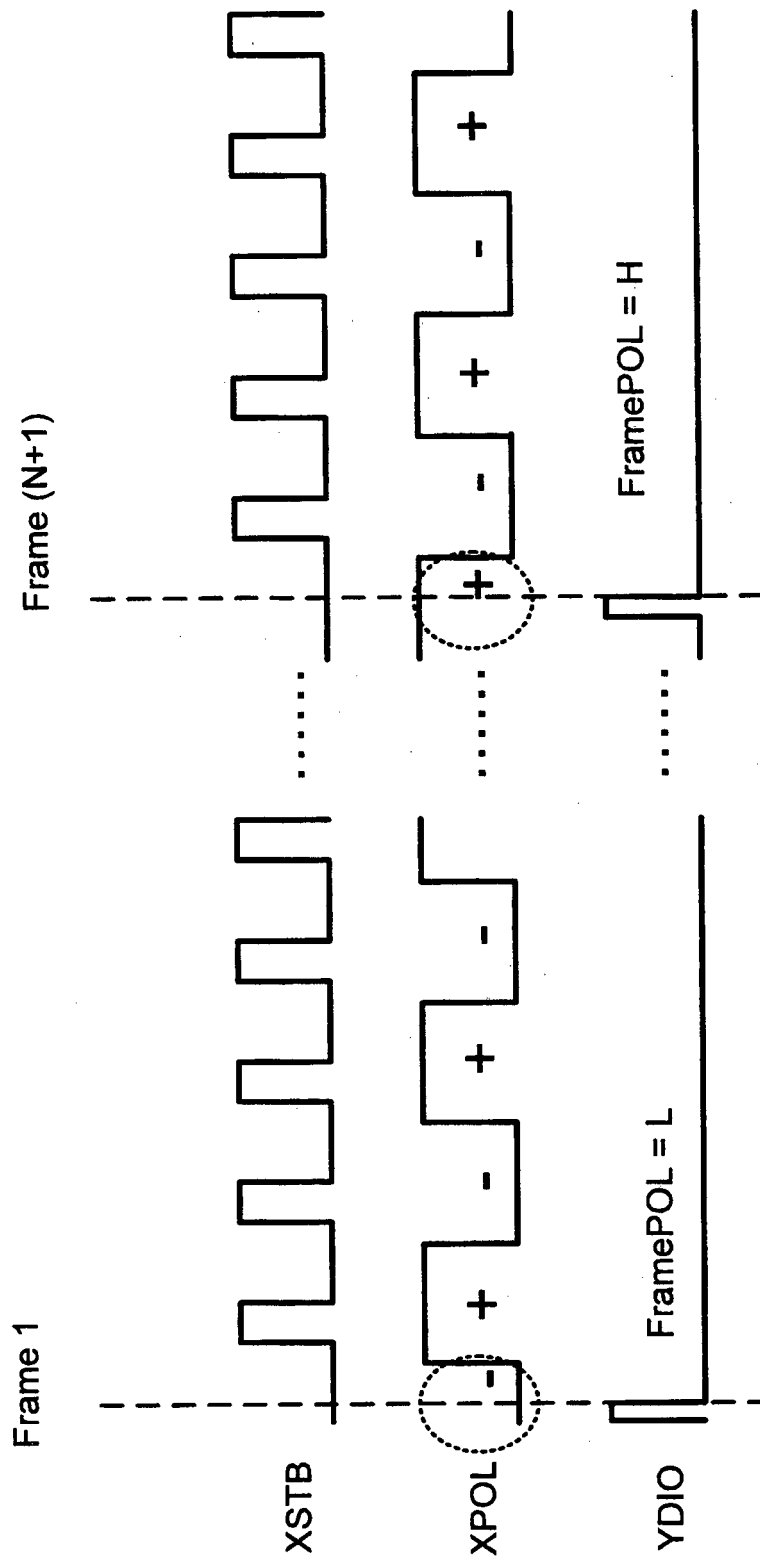


Fig. 4

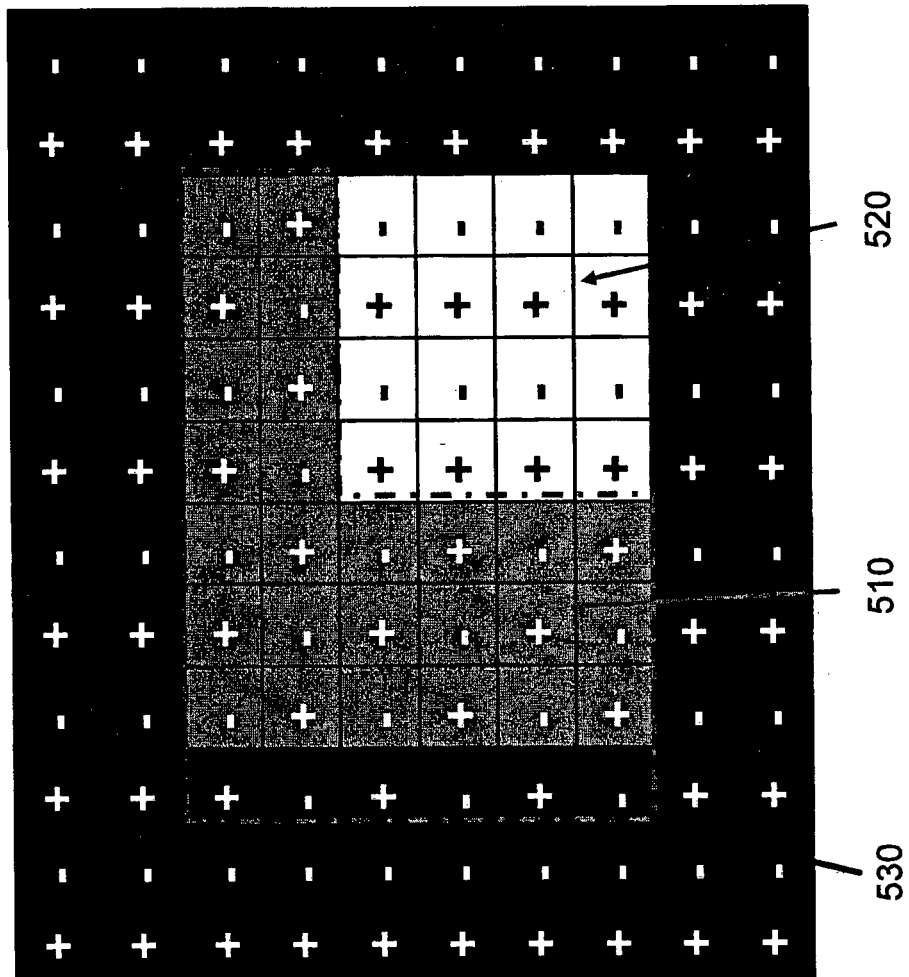


Fig. 5

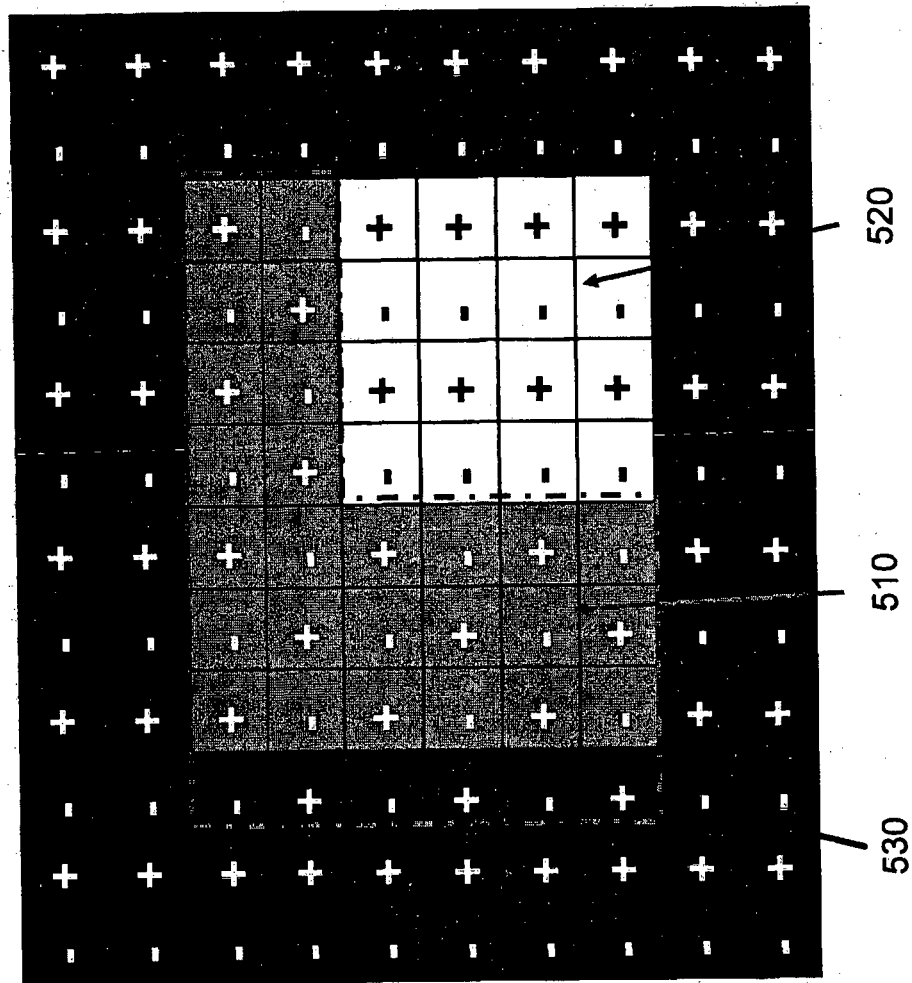


Fig. 6

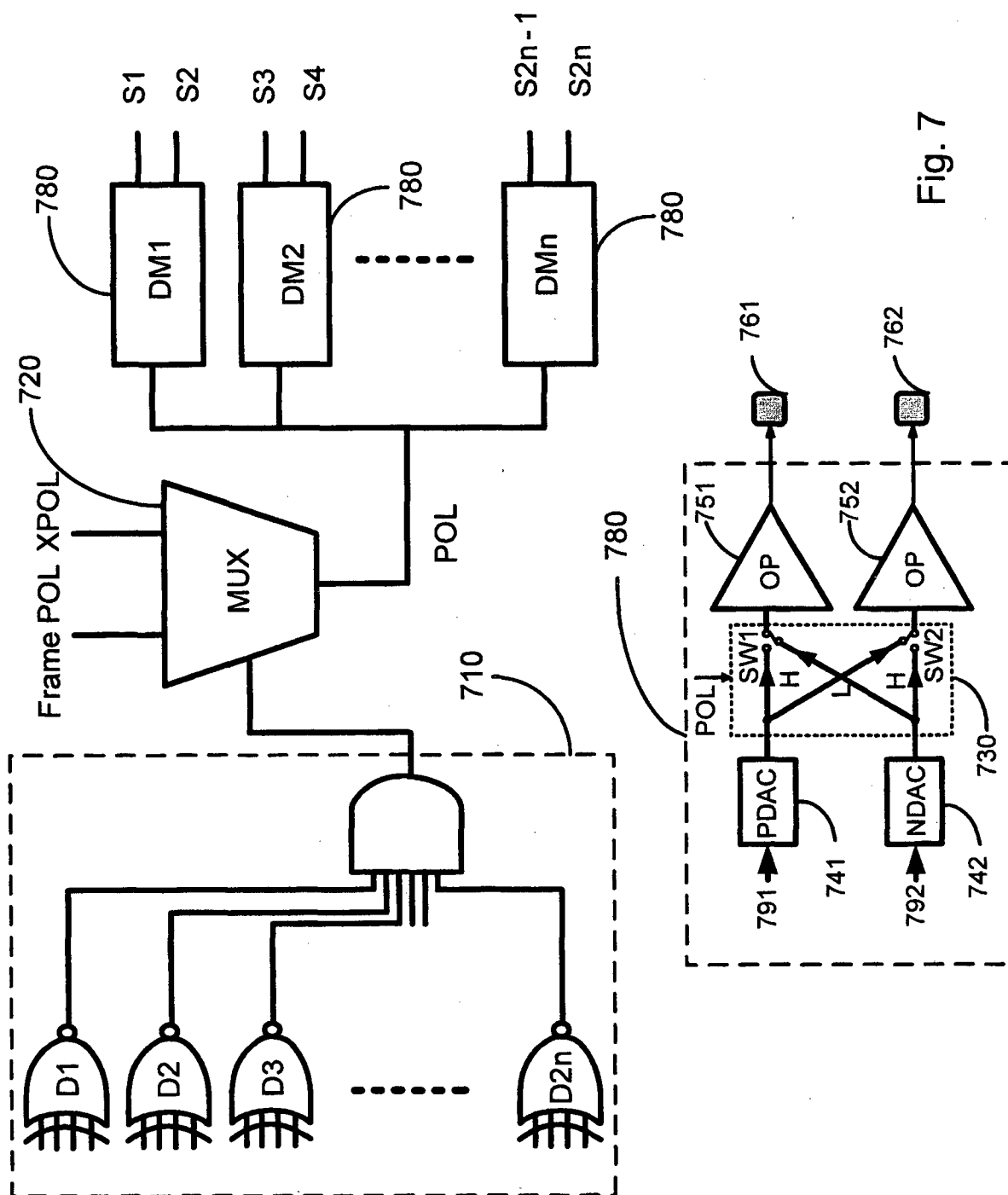


Fig. 7

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

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专利名称(译)	用于驱动液晶显示器的方法和装置		
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摘要(译)

液晶显示器 (LCD) 包括用于驱动显示面板以在自适应列反转中显示图像数据的源极驱动器。在一个实施例中，源极驱动器包括数据处理单元，该数据处理单元具有适于确定两个相邻数据线的图像数据信号的N个最高有效位 (MSB) 的逻辑电路，使得当所有N个MSB等于1或在图0中，逻辑电路的输出为1，否则，逻辑电路的输出为0，并且MUX耦合到数据处理单元并适于接收帧极性控制信号，FramePOL和像素极性控制信号，XPOL，并且当逻辑电路的输出为1时选择性地输出帧极性控制信号FramePOL，或者当逻辑电路的输出为0时选择性地输出像素极性控制信号POL，作为极性控制信号POL。

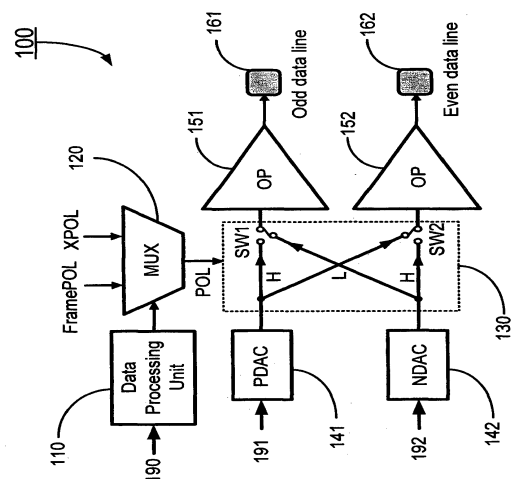


Fig. 1