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(54) DISPLAY PANEL DRIVING CIRCUIT, LIQUID CRYSTAL DISPLAY DEVICE, SHIFT REGISTER, LIQUID CRYSTAL PANEL, AND DISPLAY DEVICE DRIVING METHOD

(57) A display panel drive circuit includes a shift register (10a) constructed of unit circuits (SC1 to SCm) connected in stages. The unit circuits generate signal line selection signals (G1 to Gm), respectively, which signal line selection signals are made active for a respective certain period of time to form a respective pulse, and the pulses are outputted successively from respective unit circuits in order of ordinal number starting from a first stage until an end stage. Each of the unit circuits receive (i) clock signals (CK1 and CK2) generated based on a sync signal received from outside of the display panel drive circuit, (ii) a start pulse signal (GSP) generated based on the sync signal, or a signal line selection signal generated in a stage different from its own stage, and (iii) a clear signal (CLR). The clear signal (CLR) is made active in a case where anomalousness is included in the sync signal, and no pulse is outputted from the shift register (10a) until a subsequent vertical scanning period starts. This configuration achieves a display panel drive circuit which prevents display disorder or holds down increase in load given to a power source, each of which occurs in a case where anomalousness is included in the sync signal (VSYNC, HSYNC, or DE).

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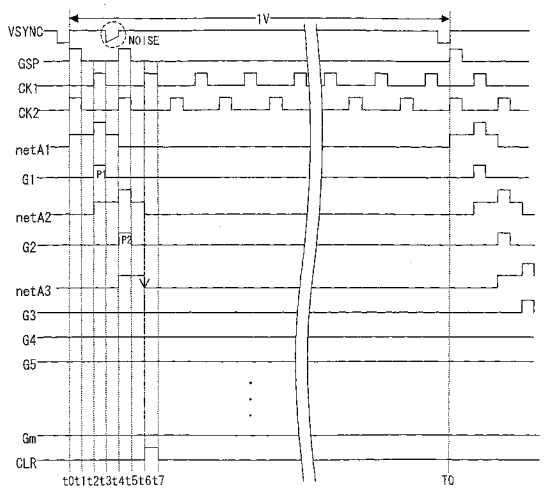

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Description

Technical Field

[0001] The present invention relates to a display panel driving circuit and a shift register for use in such a display panel driving circuit.

Background Art

[0002] Fig. 40 is a circuit diagram illustrating a conventional shift register for use in a gate driver that is included in a liquid crystal display device. As shown in Fig. 40, a conventional shift register 100 is made up of a plurality of shift circuits (unit circuits) sc1, sc2, ... scm, and scd, which are connected in stages. Each of the shift circuits sci (i = 1, 2, 3, ... or m) includes input nodes qfi, qbi, and CKAi, and an output node qoi. The shift circuit scd, which is a dummy shift circuit, includes input nodes qfd and CKAd and an output node qod.

[0003] The shift circuit sc1 has its node qf1 be connected to an output terminal via which a gate start pulse signal GSP is outputted, has its node qb1 be connected to the node qo2 of the shift circuit sc2, and has its node CKA1 be connected to a first clock line CKL1 to which a first clock signal is supplied; and from its node qo1, a gate on-pulse signal (signal line selection signal) g1 is outputted. Further, each of the shift circuits sci (i = 2, 3, ... or m-1) has its node qfi be connected to the node qo(i-1) of the shift circuit sc(i-1), has its node qbi be connected to the node qo(i+1) of the shift circuit sc(i+1), and has its node CKAi be connected to the first clock line CKL1 or a second clock line CKL2 to which a second clock signal is supplied; and from its node qoi, a gate on-pulse signal (signal line selection signal) gi is outputted. In a case where i is an odd number, the node CKAi is connected to the first clock line CKL1, and in a case where i is an even number, the node CKAi is connected to the second clock line CKL2.

[0004] The shift circuit scm has its node qfm be connected to the node qo(m-1) of the shift circuit sc(m-1), has its node qbm be connected to the node qod of the dummy shift circuit scd, and has its node CKAm be connected to the first clock line CKL1 or the second clock line CKL2; and from its node qom, the gate on-pulse signal (signal line selection signal) gm is outputted. In a case where m is an odd number, the shift circuit scm has its node CKAi be connected to the first clock line CKL1, and in a case where m is an even number, the shift circuit scm has its node CKAi be connected to the second clock line CKL2. The dummy shift circuit scd has its node qfd be connected to the node qom of the shift circuit scm, and its node CKAd be connected to the first clock line CKL1 or the second clock line CKL2. In the case where m is an odd number, the dummy shift circuit scd has its node CKAd be connected to the second clock line CKL2, and in the case where m is an even number, the dummy shift circuit scd has its node CKAd be connected to the first clock line CKL1.

[0005] Fig. 41 is a timing chart illustrating waveforms of a vertical sync signal VSYNC, the gate start pulse signal GSP, the first clock signal CK1, the second clock signal CK2, gate on-pulse signals gi (i = 1 to m), and an output via the node qod. Note that each of the first clock signal CK1 and the second clock signal CK2 includes, in one cycle, one "H (high)" (active) clock period and one "L (low)" (non-active) clock period; synchronously with activation (rise) of one of the clock signals CK1 and CK2, the other one of the clock signals CK1 and CK2 is inactivated (falls).

[0006] In the shift circuit sc1 in a first stage, an electric potential of the node qf1 rises upon activation of the gate start pulse signal GSP. As a result, the first clock signal CK1 is outputted via the node qo1, and accordingly the gate on-pulse signal g1 is activated. Moreover, in the shift circuit sc2 in a subsequent stage, an electric potential of the node qf2 rises upon activation of the gate on-pulse signal g1. As a result, the second clock signal CK2 is outputted via the node qo2, and accordingly the gate on-pulse signal g2 is activated. This activation of the gate on-pulse signal g2 makes the first clock signal CK1 no longer be outputted via the node qo1 in the shift circuit sc1 but a lower-potential side power supply potential be outputted via the node qo1. Consequently, the gate on-pulse signal g1 is inactivated after being active for a certain period of time, which as a result generates a pulse P1.

[0007] That is, in the shift circuit sci (i = 2, 3, ... or m-1), an electric potential of the node qfi rises upon activation of the gate on-pulse signal g(i-1). As a result, the clock signal (CK1 or CK2) is outputted via the node qoi, and accordingly the gate on-pulse signal gi is activated. Moreover, in the shift circuit sc(i+1) in a subsequent stage, an electric potential of the node qf(i+1) rises upon activation of the gate on-pulse signal gi. As a result, the clock signal (CK2 or CK1) is outputted via the node qo (i+1), and accordingly the gate on-pulse signal g(i+1) is activated. This activation of the gate on-pulse signal g (i+1) makes the clock signal no longer be outputted via the node qoi in the shift circuit sci but a lower-potential side power supply potential be outputted via the node qoi. Consequently, the gate on-pulse signal gi is inactivated after being active for a certain period of time, which as a result generates a pulse Pi.

[0008] Moreover, in the shift circuit scm, an electric potential of the node qfm rises upon activation of the gate on-pulse signal g(m-1). As a result, the clock signal (CK1 or CK2) is outputted via the node qom, and accordingly the gate on-pulse signal gm is activated. Further, in the dummy shift circuit scd in a subsequent stage, an electric potential of the node qfd rises upon activation of the gate on-pulse signal gm. As a result, the clock signal (CK2 or CK1) is outputted via the node qod (i.e., an electric potential at the node qod rises). The rise of the potential of the node qod makes the clock signal no longer be outputted via the node qom in the shift circuit scm, but a lower-potential side power supply potential be outputted

via the node qom. Therefore, the gate on-pulse signal gm is inactivated after being active for a certain period of time, which as a result generates a pulse Pm.

[0009] As discussed above, in the shift register 100, the gate on pulse signals outputted from respective shift circuits are successively activated for a certain period of time, and a pulse is outputted successively from respective shift circuits in order of ordinal number starting from the shift circuit sc1 in the first stage until the shift circuit scm in an end stage. Note that the following Patent Literatures 1 through 3 are known documents relevant to the technique described above.

Patent Literature 1

[0010] Japanese Patent Application Publication, Tokukai, No. 2001-273785 A (Publication Date: October 5, 2001)

Patent Literature 2

[0011] Japanese Patent Application Publication, Tokukai, No. 2006-24350 A (Publication Date: January 26, 2006)

Patent Literature 3

[0012] Japanese Patent Application Publication, Tokukai, No. 2007-114771 A (Publication Date: May 10, 2007)

Summary of Invention

[0013] In the conventional shift register, the gate start pulse signal GSP is activated in connection with an output of a pulse of the vertical sync signal VSYNC. In this case, as illustrated in Fig. 42, for example if a noise generates in the vertical sync signal VSYNC, the gate start pulse signal GSP becomes activated in connection with the noise, thereby causing two pulses be outputted from two shift circuits, simultaneously. This anomalousness that two pulses are simultaneously outputted may continue until the end stage of the shift register. Moreover, for example if a noise generates in the horizontal sync signal HSYNC, the clock signal becomes disordered, and anomalousness that a pulse width of the gate on-pulse signal becomes small may continue until the end stage of the shift register.

[0014] As described above, with the conventional shift register, anomalousness in the gate on-pulse signal continues until the end stage in the case where a sync signal such as the vertical sync signal VSYNC, the horizontal sync signal HSYNC, a data enable signal DE or the like includes an anomalousness such as a noise. This causes disorder in display on the panel, and gives a great load to a power source, in driving the panel.

[0015] The present invention proposes a display panel driving circuit which allows holding down (i) disorder of display and (ii) increase in load to the power source, in a case where anomalousness occurs in a sync signal (VSYNC or HSYNC, or DE). The present invention further proposes a shift register for use in such a display panel driving circuit.

[0016] Further, the conventional shift register requires providing a shift circuit scd (dummy stage) for resetting the shift circuit scm (end stage). This causes the circuit area in the shift register to increase in size.

[0017] The present invention proposes a display panel driving circuit which allows holding down the size of the circuit area in a shift register. The present invention further proposes a shift register for use in such a display panel driving circuit.

[0018] A display panel drive circuit of the present invention is a display panel drive circuit receiving a sync signal from outside, the display panel drive circuit including a shift register constructed of unit circuits connected in stages, the unit circuits outputting signal line selection signals, respectively, each of the signal line selection signals being made active for a respective certain period of time to form a respective pulse, the pulses being outputted successively from respective unit circuits in order of ordinal number starting from a first stage until an end stage, each of the unit circuits receiving (i) a clock signal, (ii) a start pulse signal or a signal line selection signal generated in a stage different from its own stage, and (iii) a clear signal, the clear signal being made active in a case where anomalousness is included in at least the sync signal, and no pulse is outputted from the shift register after the clear signal is made active, until a subsequent vertical scanning period starts.

[0019] Moreover, a display panel drive circuit of the present invention is a display panel drive circuit receiving a sync signal from outside, the display panel drive circuit including a shift register constructed of unit circuits connected in stages, each of the unit circuits receiving a clock signal and outputting a respective pulse by use of the received clock signal, the pulses being outputted successively from each of the stages, each of the unit circuits having an output transistor provided between an input terminal of the clock signal and an output terminal of the respective unit circuit, a clear signal being generated and inputted into each of the unit circuits, the clear signal being made active in a case where anomalousness is included in at least the sync signal, and once the clear signal is made active, the output transistor provided in each of the unit circuits being turned OFF until a subsequent vertical scanning period starts.

[0020] According to the display panel drive circuit of the present invention, once a clear signal is made active due to anomalousness in a sync signal, pulse output from the shift register stops thereafter. Therefore, it is possible to prevent disorder of display and hold down an increase in load given to the power source.

[0021] The display panel drive circuit may be configured in such a manner that the clock signal, the start pulse signal, and the clear signal are generated based

on the sync signal.

[0022] The display panel drive circuit may be configured in such a manner that the sync signal includes at least one of a vertical sync signal, a horizontal sync signal, and a data enable signal.

[0023] The display panel drive circuit may be configured in such a manner that, regardless of whether or not anomalousness is included in the sync signal, the clear signal is made active after the end stage outputs its respective pulse, so that the signal line selection signal outputted from the end stage remains inactive.

[0024] The display panel drive circuit may be configured in such a manner that regardless of whether or not anomalousness is included in the sync signal, the clear signal is made active after the pulse is outputted from a unit circuit in the end stage, so that the output transistor in each of the unit circuits is turned OFF until the subsequent vertical scanning period starts.

[0025] The display panel drive circuit may be configured in such a manner that the clear signal is made active at a timing in which no pulse is outputted or at a timing in which the pulse is made inactive.

[0026] The display panel drive circuit of the present invention may be configured in such a manner that each of the unit circuits except for that in the end stage includes a set transistor, an output transistor, a reset transistor, a clear transistor, and a capacitor, the set transistor, output transistor, reset transistor, and clear transistor each having a control terminal, a first conductive terminal, and a second conductive terminal, and the capacitor having a first electrode and a second electrode, the clear transistor receiving the clear signal via its control terminal, the reset transistor receiving, via its control terminal, a signal line selection signal outputted from a stage subsequent to its own stage, the set transistor receiving, via its control terminal, the start pulse signal or a signal line selection signal outputted from a stage previous to its own stage, the output transistor receiving the clock signal via its first conductive terminal, the second conductive terminal of the output transistor being connected to the first electrode of the capacitor, the control terminal of the set transistor and the first conductive terminal of the set transistor being connected to each other, and the second conductive terminal of the set transistor being connected to (i) the control terminal of the output transistor and (ii) the second electrode of the capacitor, the first conductive terminal of the clear transistor being connected to the control terminal of the output transistor, and the second conductive terminal of the clear transistor being connected to the constant potential source, the first conductive terminal of the reset transistor being connected to the control terminal of the output transistor, and the second conductive terminal of the reset transistor being connected to a constant potential source, and the second conductive terminal of the output transistor serving as an output terminal of the respective unit circuit. Note that, in the present application, one of the source terminal and drain terminal of a transistor is defined as the first conductive terminal, and the other one of the source terminal and drain terminal of the transistor is defined as the second conductive terminal. Depending on the design of the transistor, the first conductor of all the transistors may be the source terminal, or the first transistor of a certain transistor may be the drain terminal and the first transistors of the remaining transistors may be the source terminal.

[0027] The display panel drive circuit of the present invention may be configured in such a manner that each of the unit circuits except for that in the end stage further includes a potential supplying transistor, the potential supplying transistor having a control terminal, a first conductive terminal, and a second conductive terminal, the first conductive terminal of the potential supplying transistor being connected to the second conductive terminal of the output transistor, and the second conductive terminal of the potential supplying transistor being connected to the constant potential source, the potential supplying transistor receiving, via its control terminal, a signal line selection signal outputted from a stage subsequent to its own stage.

[0028] The display panel drive circuit of the present invention may be configured in such a manner that each of the unit circuits except for that in the end stage further includes a potential supplying transistor, the potential supplying transistor having a control terminal, a first conductive terminal, and a second conductive terminal, the first conductive terminal of the potential supplying transistor being connected to the second conductive terminal of the output transistor, and the second conductive terminal of the potential supplying transistor being connected to the constant potential source, the potential supplying transistor receiving, via its control terminal, a clock signal different from the clock signal received via the first conductive terminal of the output transistor.

[0029] The display panel drive circuit of the present invention may be configured in such a manner that the unit circuit in the end stage includes a set transistor, an output transistor, a clear transistor, and a capacitor, the set transistor, output transistor, and clear transistor each having a control terminal, a first conductive terminal, and a second conductive terminal, and the capacitor having a first electrode and a second electrode, the clear transistor receiving the clear signal via its control terminal, the set transistor receiving, via its control terminal, a signal line selection signal outputted from a stage previous to its own stage, and the output transistor receiving the clock signal via its first conductive terminal, the second conductive terminal of the output transistor being connected to the first electrode of the capacitor, the control terminal of the set transistor and the first conductive terminal of the set transistor being connected to each other, and the second conductive terminal of the set transistor being connected to (i) the control terminal of the output transistor and (ii) the second electrode of the capacitor, the first conductive terminal of the clear transistor being connected to the control terminal of the output transistor, and the second conductive terminal of the clear transistor

being connected to the constant potential source, and the second conductive terminal of the output transistor serving as an output terminal of the unit circuit in the end stage.

[0030] The display panel drive circuit of the present invention may be configured in such a manner that the unit circuit in the end stage further includes a potential supplying transistor, the potential supplying transistor having a control terminal, a first conductive terminal, and a second conductive terminal, the potential supplying transistor receiving the clear signal via its control terminal, the first conductive terminal of the potential supplying transistor being connected to the second conductive terminal of the output transistor, and the second conductive terminal of the potential supplying transistor being connected to the constant potential source.

[0031] The display panel drive circuit of the present invention may be configured in such a manner that the clear signal is made active at a timing in which the signal line selection signal received from a respective stage is made inactive, or is made active while the signal line selection signal received from the respective stage is inactive.

[0032] The display panel drive circuit of the present invention may be configured in such a manner that a plurality of clock signals each having phases different from each other are inputted into the shift register, the plurality of clock signals being received by the output transistors of different unit circuits, respectively.

[0033] The display panel drive circuit of the present invention may be configured in such a manner that each of the plurality of clock signals have an inactive period that partially coincides with an inactive period of another of the plurality of clock signals.

[0034] The display panel drive circuit of the present invention may be configured in such a manner that the plurality of clock signals include two clock signals which are shifted in phase by half a cycle.

[0035] The display panel drive circuit of the present invention may be configured in such a manner that at least one of the plurality of clock signals is made inactive while the clear signal is made active.

[0036] The display panel drive circuit of the present invention may be configured in such a manner that each of the set transistor, the output transistor, the reset transistor, and the clear transistor is an N-channel transistor.

[0037] The display panel drive circuit of the present invention may be configured in such a manner that each of the set transistor, the output transistor, the reset transistor, the clear transistor, and the potential supplying transistor is an N-channel transistor.

[0038] The display panel drive circuit of the present invention may be configured in such a manner that the first conductive terminal of each of the transistors is a drain terminal, and the second conductive terminal of each of the transistors is a source terminal.

[0039] The display panel drive circuit of the present invention may be configured in such a manner that the first conductive terminal of each of the transistors is a source terminal, and the second conductive terminal of each of the transistors is a drain terminal.

[0040] The display panel drive circuit of the present invention may be configured further including a timing controller into which the sync signal is inputted, for generating the clock signal, the start pulse signal, and the clear signal with use of the sync signal thus inputted.

[0041] The display panel drive circuit of the present invention may be configured further including an anomalousness detection circuit for detecting anomalousness of the sync signal, the clear signal being generated based on a result of the detection.

[0042] A liquid crystal display device of the present invention includes the display panel drive circuit; and a liquid crystal panel.

[0043] The liquid crystal display device of the present invention may be configured in such a manner that the shift register is provided monolithically in the liquid crystal panel.

[0044] In the liquid crystal display device of the present invention, the liquid crystal panel may be formed by use of amorphous silicone. Moreover, the liquid crystal panel may be formed by use of polysilicon.

[0045] A shift register of the present invention is provided in a display panel drive circuit that receives a sync signal, the shift register constructed of unit circuits connected in stages, the unit circuits generating signal line selection signals, respectively, each of the signal line selection signals being made active for a respective certain period of time to form a respective pulse, the pulses being outputted successively from respective unit circuits, in order of ordinal number starting from a first stage until an end stage, each of the unit circuits receiving (i) a clock signal, (ii) a start pulse signal or a signal line selection signal generated by a stage different from its own stage, and (iii) a clear signal, the clear signal being made active in a case where anomalousness is included in at least the sync signal, and no pulse is outputted after the clear signal is made active until a subsequent vertical scanning period starts. In this case, the shift register may be monolithically provided.

[0046] A method of the present invention for driving a display device, the display device receiving a sync signal from outside and including a shift register constructed of unit circuits connected in stages, the unit circuits generating signal line selection signals, respectively, each of the signal line selection signals being made active for a respective certain period of time to form a respective pulse, the shift register outputting the pulses successively from respective unit circuits in order of ordinal number starting from a first stage until an end stage, is a method including: inputting, to each of the unit circuits, (i) a clock signal, (ii) a start pulse signal or a signal line selection signal generated in a stage different from its own stage, and (iii) a clear signal; and activating the clear signal in a case where anomalousness is included in at least the sync signal, so that no pulse is outputted from the shift

register after the clear signal is made active, until a subsequent vertical scanning period starts.

[0047] A display panel drive circuit of the present invention includes: a shift register constructed of unit circuits connected in stages, the unit circuits outputting signal line selection signals, respectively, each of the signal line selection signals being made active for a respective certain period of time to form a respective pulse, the shift register outputting the pulses successively from respective unit circuits in order of ordinal number starting from a first stage until an end stage, a unit circuit in the end stage receiving (i) a signal line selection signal generated in a stage different from its own stage, (ii) a clock signal, and (iii) a clear signal, and the clear signal being made active after the end stage outputs its respective pulse, so that the signal line selection signal outputted from the end stage remains inactive.

[0048] According to the display panel drive circuit of the present invention, resetting can be carried out by use of a clear signal at an end stage (unit circuit). Hence, no dummy stage (dummy shift circuit) is required as in the conventional technique, and thus it is possible to reduce circuit area of the shift register.

[0049] The display panel drive circuit of the present invention may be configured in such a manner that each of the unit circuits except for the unit circuit in the end stage includes a set transistor, an output transistor, a reset transistor, and a capacitor, the set transistor, output transistor, and reset transistor each having a control terminal, a first conductive terminal, and a second conductive terminal, and the capacitor having a first electrode and a second electrode, the set transistor receiving, via its control terminal, a start pulse signal or a signal line selection signal outputted from a stage previous to its own stage, the reset transistor receiving, via its control terminal, a signal line selection signal outputted from a stage subsequent to its own stage, and the output transistor receiving the clock signal via its first conductive terminal, the second conductive terminal of the output transistor being connected to a first electrode of the capacitor, the control terminal of the set transistor and the first conductive terminal of the set transistor being connected to each other, and the second conductive terminal of the set transistor being connected to (i) the control terminal of the output transistor and (ii) a second electrode of the capacitor, the first conductive terminal of the reset transistor being connected to the control terminal of the output transistor, and the second conductive terminal of the reset transistor being connected to a constant potential source, and the second conductive terminal of the output transistor serving as an output terminal of the respective unit circuit.

[0050] The display panel drive circuit of the present invention may be configured in such a manner that a unit circuit in the end stage includes a set transistor, an output transistor, a clear transistor provided for resetting the end stage, and a capacitor; the set transistor, output transistor, and clear transistor each having a control terminal, a first conductive terminal, and a second conductive terminal, and the capacitor having a first electrode and a second electrode, the set transistor receiving, via its control terminal, a signal line selection signal outputted from a stage previous to its own stage, the clear transistor receiving the clear signal via its control terminal, and the output transistor receiving the clock signal via its first conductive terminal, the second conductive terminal of the output transistor being connected to the first electrode of the capacitor, the control terminal of the set transistor and the first conductive terminal of the set transistor being connected to each other, and the second conductive terminal of the set transistor being connected to (i) the control terminal of the output transistor and (ii) the second electrode of the capacitor, the first conductive terminal of the clear transistor being connected to the control terminal of the output transistor, and the second conductive terminal of the clear transistor being connected to a constant potential source, and the second conductive terminal of the output transistor serving as an output terminal of the unit circuit in the end stage.

[0051] The display panel drive circuit of the present invention may be configured in such a manner that the unit circuit of the end stage further includes a potential supplying transistor, the potential supplying transistor having a control terminal, a first conductive terminal, and a second conductive terminal, the potential supplying transistor receiving the clear signal via its control terminal, the first conductive terminal of the potential supplying transistor being connected to the second conductive terminal of the output transistor, and the second conductive terminal of the potential supplying transistor being connected to the constant potential source.

[0052] A shift register of the present invention is a shift register provided in a display panel drive circuit, the shift register being constructed of unit circuits connected in stages, the unit circuits generating signal line selection signals, respectively, each of the signal line selection signals being made active for a respective certain period of time to form a respective pulse, the pulses being outputted successively from respective unit circuits in order of ordinal number starting from a first stage until an end stage, a unit circuit in the end stage receiving (i) a signal line selection signal generated in a stage different from its own stage, (ii) a clock signal, and (iii) a clear signal, and the clear signal being made active after a pulse is outputted from the end stage, so that the signal line selection signal outputted from the end stage remains inactive.

[0053] A method of the present invention for driving a display device including a shift register constructed of unit circuits connected in stages, the unit circuits generating signal line selection signals, respectively, each of the signal line selection signals being made active for a respective certain period of time to form a respective pulse, the shift register outputting the pulses successively from respective unit circuits in order of ordinal number starting from a first stage until an end stage, is a method

including: inputting, to a unit circuit in the end stage, (i) a signal line selection signal generated in a stage different from its own stage, (ii) a clock signal, and (iii) a clear signal; and activating the clear signal after a pulse is outputted from the end stage, so that the signal line selection signal outputted from the end stage remains inactive.

[0054] According to the display panel driving circuit of the present invention, once a clear signal is made active due to anomalousness in a sync signal, pulse output from the shift register stops thereafter. Therefore, it is possible to prevent disorder of display and hold down an increase in load given to the power source.

[0055] Moreover, according to the display panel driving circuit of the present invention, it is possible to reset the shift register by use of the clear signal at an end stage (unit circuit). Consequently, a dummy stage (dummy shift circuit) is not required as in a conventional display panel driving circuit, thereby allowing reduction of circuit area in the shift register.

Brief Description of Drawings

[0056]

Fig. 1
Fig. 1 is a block diagram illustrating a configuration of a present shift register.
Fig. 2
Parts (a) and (b) of Fig. 2 are circuit diagrams illustrating a configuration of a unit circuit of a shift register.
Fig. 3
Fig. 3 is a circuit diagram illustrating a configuration of a present shift register.
Fig. 4
Fig. 4 is a timing chart illustrating an operation (in a case where a sync signal includes no anomalousness) of the shift register shown in Fig. 3.
Fig. 5
Fig. 5 is a timing chart illustrating an operation (in a case where a sync signal includes anomalousness) of the shift register shown in Fig. 3.
Fig. 6
Fig. 6 is a circuit diagram illustrating another configuration of a present shift register.
Fig. 7
Fig. 7 is a timing chart illustrating an operation (in a case where a sync signal includes no anomalousness) of the shift register shown in Fig. 6.
Fig. 8
Fig. 8 is a circuit diagram illustrating another configuration of a present shift register.
Fig. 9
Fig. 9 is a timing chart illustrating an operation (in a case where a sync signal includes no anomalousness) of the shift register shown in Fig. 8.
Fig. 10
Fig. 10 is a timing chart illustrating an operation (in a case where a sync signal includes anomalousness) of the shift register shown in Fig. 8.
Fig. 11
Fig. 11 is a circuit diagram illustrating another configuration of a present shift register.
Fig. 12
Fig. 12 is a timing chart illustrating an operation (in a case where a sync signal includes no anomalousness) of the shift register shown in Fig. 11.
Fig. 13
Fig. 13 is a circuit diagram illustrating another configuration of a present shift register.
Fig. 14
Fig. 14 is a timing chart illustrating an operation (in a case where a sync signal includes no anomalousness) of the shift register shown in Fig. 13.
Fig. 15
Fig. 15 is a timing chart illustrating an operation (in a case where a sync signal includes anomalousness) of the shift register shown in Fig. 13.
Fig. 16
Fig. 16 is a timing chart illustrating an operation (in a case where a sync signal includes anomalousness) of the shift register shown in Fig. 13.
Fig. 17
Fig. 17 is a circuit diagram illustrating a through current.
Fig. 18
Fig. 18 is a timing chart illustrating an operation (in a case where a sync signal includes anomalousness) of the shift register shown in Fig. 13.
Fig. 19
Fig. 19 is a block diagram illustrating another configuration of a present shift register.
Fig. 20
Parts (a) and (b) of Fig. 20 are circuit diagrams illustrating a configuration of a unit circuit of a present shift register.
Fig. 21
Fig. 21 is a timing chart illustrating an operation (in a case where a sync signal includes no anomalousness) of the shift register shown in Fig. 19.
Fig. 22
Fig. 22 is a timing chart illustrating an operation (in a case where a sync signal includes anomalousness) of the shift register shown in Fig. 19.
Fig. 23
Fig. 23 is a block diagram illustrating a configuration of a liquid crystal display device of Embodiments 1 and 2.
Fig. 24
Fig. 24 is a block diagram illustrating a configuration of a liquid crystal display device of Embodiments 3 and 4.
Fig. 25
Fig. 25 is a block diagram illustrating a configuration of a shift register of Embodiment 3.
Fig. 26

Parts (a) and (b) of Fig. 26 are circuit diagrams illustrating a configuration of a unit circuit of the shift register of Embodiment 3.

Fig. 27

Fig. 27 is a circuit diagram illustrating a configuration of the shift register of Embodiment 3.

Fig. 28

Fig. 28 is a timing chart illustrating an operation of the shift register shown in Fig. 27.

Fig. 29

Fig. 29 is a circuit diagram illustrating another configuration of a present shift register.

Fig. 30

Fig. 30 is a timing chart illustrating an operation of the shift register shown in Fig. 29.

Fig. 31

Fig. 31 is a circuit diagram illustrating another configuration of the shift register of Embodiment 3.

Fig. 32

Fig. 32 is a timing chart illustrating an operation of the shift register shown in Fig. 31.

Fig. 33

Fig. 33 is a circuit diagram illustrating another configuration of the shift register of Embodiment 3.

Fig. 34

Fig. 34 is a timing chart illustrating an operation (in a case where a sync signal includes no anomalousness) of the shift register shown in Fig. 33.

Fig. 35

Fig. 35 is a circuit diagram illustrating another configuration of the shift register of Embodiment 3.

Fig. 36

Fig. 36 is a timing chart illustrating an operation (in a case where a sync signal includes no anomalousness) of the shift register shown in Fig. 35.

Fig. 37

Fig. 37 is a block diagram illustrating a configuration of a shift register of Embodiment 4.

Fig. 38

Parts (a) and (b) of Fig. 38 are circuit diagrams illustrating a configuration of a unit circuit of the shift register of Embodiment 4.

Fig. 39

Fig. 39 is a timing chart illustrating an operation of the shift register shown in Fig. 37.

Fig. 40

Fig. 40 is a block diagram illustrating a configuration of a conventional shift register.

Fig. 41

Fig. 41 is a timing chart illustrating an operation of the shift register shown in Fig. 40.

Fig. 42

Fig. 42 is a timing chart illustrating an operation of the shift register shown in Fig. 40.

Reference Signs List

[0057]

1:	Liquid crystal display device (display device)
10, 10a to 10g:	Shift register
G1 to Gm:	Gate on-pulse (signal line selection signal)
SC1 to SCm:	Shift circuit (unit circuit)
GSP:	Gate start pulse
CK1:	First clock signal
CK2:	Second clock signal
CLR:	Clear signal
Tra:	Set transistor
Trb:	Output transistor
Trc:	Clear transistor
Trd:	Reset transistor
Tre:	Low-potential supplying transistor

Description of Embodiments

[0058] The following describes one embodiment of the present invention, with reference to Figs 1 through 39.

[0059] Fig. 23 is a block diagram illustrating a configuration of a liquid crystal display device of the present invention. As shown in Fig. 23, a liquid crystal display device 1 of the present invention includes a liquid crystal panel 3, a gate driver 5, a source driver 6, a timing controller 7, a data processing circuit 8, and an anomalousness detection circuit 9. The gate driver 5 includes a shift register 10 and a level shifter 4. The gate driver 5, the timing controller 7, and the anomalousness detection circuit 9 make up a liquid crystal panel driving circuit 11. Note that, in the present embodiment, the level shifter 4 is included in the gate driver 5. However, the level shifter 4 can be provided outside of the gate driver 5.

[0060] The liquid crystal panel 3 includes scanning signal lines 16 driven by the gate driver 5, data signal lines 15 driven by the source driver 6, pixels P, storage capacitor wires (not illustrated), and the like. Further, the shift register 10 is monolithically provided in the liquid crystal panel 3. Each of the pixels P is provided with (i) a transistor (TFT) which is connected to one of the scanning signal lines 16 and one of the data signal lines 15 and (ii) a pixel electrode connected to the transistor. Note that the transistors provided in the pixels and a transistor of the shift register can be formed by use of amorphous silicon, polycrystalline silicon, CG silicon, or the like.

[0061] The timing controller 7 receives, from outside of the liquid crystal display device 1, a vertical sync signal VSYNC, a horizontal sync signal HSYNC, and a data-enable signal DE, each of which is a sync signal. Note that these sync signals (VSYNC, HSYNC, and DE) are supplied also to the anomalousness detection circuit 9. Moreover, the data processing circuit 8 receives video data (RGB digital data) from outside of the liquid crystal display device 1. The anomalousness detection circuit 9 detects anomalousness in the sync signals and sends an error signal to the timing controller 7 in a case where the anomalousness detection circuit 9 detects anomalousness in a sync signal. Note that the anomalousness

detection circuit 9 can detect anomalousness in sync signals with use of, for example, a method disclosed in "Japanese Patent Application Publication No. 2003-167545". The timing controller 7 generates a plurality of source clock signals (ck1, ck2 etc.), a source clear signal (clr), and a source gate start pulse signal (gsp) with use of the sync signals and the error signal sent from the anomalousness detection circuit 9. Note that the source clock signals (e.g., ck1 and ck2), the source clear signal (clr), and the source gate start pulse signal (gsp) are shifted in level by the level shifter 6 so as to become clock signals (CK1, CK2 etc.), a clear signal (CLR), and a gate start pulse signal (GSP), respectively. The timing controller 7 outputs a control signal to the data processing circuit 8, and also outputs a source timing signal to the source driver 6 based on the received sync signals (VSYNC, HSYNC, and DE).

[0062] The clock signals (CKA, CKB etc.), the clear signal (CLR), and the gate start pulse signal (GSP) are supplied to the shift register 10. The clear signal (CLR) becomes "L" (inactive) in a case where the sync signals (VSYNC, HSYNC, and DE) includes no anomalousness, becomes "H" (active) in a case where at least one of the sync signals (VSYNC, HSYNC, and DE) include anomalousness, and becomes "H" (active) after a pulse is outputted from the end stage regardless of whether or not anomalousness is included in the sync signals. The shift register 10 generates gate on-pulse signals with use of these signals (CKA, CKB etc.; CLR; and GSP), and outputs the gate on-pulse signals to the scanning signal lines provided in the liquid crystal panel 3. The shift register 10 includes shift circuits connected in stages, which each of the shift circuits generates a gate on-pulse signal. The gate on-pulse signals generated in the stages (shift circuits) are successively activated for a respective given period. This causes pulses (on-pulses) to be outputted successively in order of ordinary number from the first stage until the end stage. Thereafter, in the liquid crystal panel 3, the scanning signal lines are successively selected, in accordance with the pulses.

[0063] The data processing circuit 8 carries out a predetermined process to video data, and outputs a data signal to the source driver 6 in accordance with the control signal outputted from the timing controller 7. The source driver 6 generates signal potential with use of (i) the data signal outputted from the data processing circuit 8 and (ii) the source timing signal outputted from the timing controller 7, and outputs the generated signal potential to the data signal lines provided in the liquid crystal panel 3. The signal potentials are written in pixel electrodes of the pixels via the transistors of the pixels.

Embodiment 1

[0064] Fig. 1 illustrates a configuration of a shift register 10a in accordance with the present Embodiment 1. As shown in Fig. 1, the shift register 10a is made up of a plurality of shift circuits (unit circuits) SC1, SC2, ... and SCm connected in stages. Each of the shift circuits SCi (i = 1, 2, 3, ... and m-1) includes input nodes Qfi, Qbi, CKAi, and CLi, and an output node Qoi. The shift circuit SCm includes input nodes Qfm, CKAm, and CLm, and an output node Qom.

[0065] The shift circuit SC1 has its node Qf1 be connected to a GSP output terminal RO of the level shifter (see Fig. 23). Further, the shift circuit has its node Qb1 be connected to the node Qo2 of a shift circuit SC2, has its node CKA1 be connected to a first clock line CKL1 to which a first clock signal is supplied, and has its node CL1 be connected to a clear line CLRL to which a clear signal (CLR) is supplied. Further, the shift circuit SC1 outputs a gate on-pulse signal (signal line selection signal) G1 via its node Qo1.

[0066] Each of the shift circuits SCi (i = 2 to m-1) has its node Qfi be connected to the node Qo(i-1) of the shift circuit SC(i-1) and has its node Qbi be connected to the node Qo(i+1) of the shift circuit SC(i+1). In a case where i is an odd number, the node CKAi is connected to the first clock line CKL1, and in a case where i is an even number, the node CKAi is connected to the second clock line CKL2. Further, the node CLi of each of the shift circuits SCi is connected to the clear line CLRL. Moreover, each of the shift circuits SCi outputs a gate on-pulse signal (signal line selection signal) Gi via its node Qoi.

[0067] The shift circuit SCm has its node Qfm be connected to the node Qo(m-1) of the shift circuit SC(m-1), has its node CKAm be connected to the second clock line CKL2, and has its node CLm be connected to the clear line CLRL. Further, the shift circuit SCm outputs a gate on-pulse signal (signal line selection signal) Gm via its node Qom.

[0068] Specifically illustrated in (a) of Fig. 2 is a circuit diagram of a configuration employed by each of the shift circuits SCi (i = 1 to m-1). As illustrated in (a) of Fig. 2, each of the shift circuits SCi (i = 1 to m-1) includes a set transistor Tra, an output transistor Trb, a clear transistor Trc, a reset transistor Trd, and a capacitor C. Note that each of the transistors Tra to Trd is an N-channel transistor.

[0069] The transistor Trb has its source terminal be connected to a first electrode of the capacitor C. The transistor Tra has its gate terminal (control terminal) and its drain terminal be connected to each other, and has its source terminal be connected to (i) a gate terminal of the transistor Trb and (ii) a second electrode of the capacitor C. The transistor Trc has its drain terminal be connected to the gate terminal of the transistor Trb and its source terminal be connected to a lower-potential-side power supply Vss. The transistor Trd has its drain terminal be connected to the gate terminal of the transistor Trb and its source terminal be connected to the lower-potential-side power supply Vss. The gate terminal of the transistor Tra is connected to the node Qfi, the transistor Trb has its drain terminal be connected to the node CKAi, the transistor Trc has its gate terminal be connected to the node CLi; the transistor Trd has its gate terminal be

connected to the node Qbi; and the source terminal of the transistor Trb is connected to the node Qoi. Note that a connection point of the source terminal of the transistor Tra, the second electrode of the capacitor C, and the gate terminal of the transistor Trb is defined as a node netAi.

[0070] Specifically illustrated in (b) of Fig. 2 is a circuit diagram of a configuration of the shift circuit SCm. As illustrated in (b) of Fig. 2, the shift circuit SCm includes a set transistor Tra, an output transistor Trb, a clear transistor Trc, and a capacitor C. Note that each of the transistors Tra to Trc is an N-channel transistor, and the capacitor C can also be parasitic capacitor. The transistor Trb has its source terminal be connected to a first electrode of the capacitor C. The transistor Tra has its gate terminal (control terminal) and its drain terminal be connected to each other, and the transistor Tra has its source terminal be connected to (i) a gate terminal of the transistor Trb and (ii) a second electrode of the capacitor C. The transistor Trc has its drain terminal be connected to the gate terminal of the transistor Trb and has its source terminal be connected to a lower-potential-side power supply Vss. The gate terminal of the transistor Tra is connected to the node Qfm, the transistor Trb has its drain terminal be connected to the node CKAm, the transistor Trc has its gate terminal be connected to the node CLm, and the source terminal of the transistor Trb is connected to the node Qom. Note that a connection point of the source terminal of the transistor Tra, the second electrode of the capacitor C, and the gate terminal of the transistor Trb is defined as a node netAm.

[0071] The nodes (Qfi, Qbi, CKAi, CLi, and Qoi) in each of the shift circuits SCi (i = 1 to m-1) and the nodes (Qfm, CKAm, CLm, and Qom) in the shift circuit SCm are connected to respective destinations as illustrated in Fig. 1. The configuration of an entire shift register 10a is as specifically illustrated in Fig. 3.

[0072] The following describes operations of the shift register 10a illustrated in Fig. 3. Fig. 4 is a timing chart illustrating waveforms of a vertical sync signal VSYNC, a gate start pulse signal GSP, a first clock signal CK1, a second clock signal CK2, gate on-pulse signals Gi (i = 1 to m), and a clear signal (CLR), in a case where the sync signals include no anomalousness. Note that each of the first clock signal CK1 and the second clock signal CK2 includes, in one cycle, one clock period of a "H" (active) period and three clock periods of a "L" (inactive) period. After one of the clock signals CK1 and CK2 is inactivated (falls), the other one of the clock signals CK1 and CK2 is activated (rises) with a delay of one clock period. This is merely an example of the first and second clock signals CK1 and CK2; the "H" period and "L" period may be arbitrarily set as long as there is a period in which both clock signals coincide as "L".

[0073] At t0 in Fig. 4, activation of the gate start pulse signal GSP causes a rise in electric potential of Qf1. This rise in the electric potential turns Tra of SC1 ON, thereby causing electric potential at netA1 to change from "L" to "H". As a result, Trb of SC1 is also turned ON, and accordingly CK1 is outputted via Qo1. According to the configuration, G1 remains at "L". At t1, which is a timing one clock period elapsed after t0, GSP falls (is inactivated) and becomes "L". However, the electric potential at the node netA1 is maintained at "H" by the capacitor C of SC1, and accordingly Trb of SC1 also remains turned ON.

[0074] At t2, which is a timing one clock period elapsed after t1, CK1 rises (is activated), thereby causing G1 to be activated and become "H". At this point, the electric potential at netA1 rises to an electric potential higher than "H" by the capacitor C. Moreover, the activation of G1 causes electric potential at Qf2 to rise. As a result, Tra of SC2 is turned ON, thereby causing electric potential at netA2 to change from "L" to "H". This also causes Trb of SC2 to be turned ON, and accordingly CK2 is outputted via Qo2. According to the configuration, G2 remains at "L".

[0075] At t3, which is a timing one clock period elapsed after t2, CK1 falls and becomes "L", and the electric potential at netA1 also returns back to "H". However, since Trb of SC1 remains turned ON, CK1 is continuously outputted via Qo1. According to the configuration, G1 is inactivated from "H" to "L", and this state "L" is maintained. Note that, even if G1 is inactivated and becomes "L", the electric potential at netA2 is maintained at "H" by the capacitor C of SC2, and Trb of SC2 remains turned ON.

[0076] At t4, which is a timing one clock period elapsed after t3, CK2 rises, thereby causing G2 to be activated and become "H". At this point, the electric potential at netA2 rises to an electric potential higher than "H" by the capacitor C. Moreover, the activation of G2 causes electric potential at Qb1 to rise; consequently, Trd of SC1 turns ON, which connects netA1 to Vss, thereby causing the electric potential at netA1 to change from "H" to "L". As a result, Trb of SC1 is turned OFF, and CK1 is no longer outputted via Qo1.

[0077] At t5, which is a timing one clock period elapsed after t4, CK2 falls and becomes "L" and the electric potential at netA2 also is returned back to "H". However, since Trb of SC2 remains turned ON, CK2 is continuously outputted via Qo2. According to the configuration, G2 is inactivated from "H" to "L", and this state "L" is maintained.

[0078] Further, at tx, CK2 rises, and accordingly Gm is also activated and becomes "H". At this point, the electric potential at netAm rises to an electric potential higher than "H" by the capacitor C.

[0079] At ty, which is a timing one clock period elapsed after tx, CK2 falls and becomes "L", and the electric potential at netAm is also returned back to "H". However, since Trb of SCm remains turned ON, CK2 is continuously outputted via Qom. According to the configuration, Gm is inactivated from "H" to "L", and this state "L" is maintained.

[0080] At tz, which is a timing one clock period elapsed after ty, CK2 remains at "L". However, since the clear

signal CLR is activated and becomes "H", Trc of SCm turns ON, which connects netAm to Vss, thereby causing the electric potential at netAm to change from "H" to "L". As a result, Trb of SCm is turned OFF, and CK2 is no longer outputted via Qom.

[0081] Note that, in Fig. 4, the clear signal CLR is activated at tz (which is one clock period elapsed after the fall of Gm). However, the present invention is not limited to this. For example, the clear signal CLR can be activated between ty and tz (ty exclusive). However, the clear signal CLR should not be activated at ty. This is because, if the clear signal CLR is activated at ty, Gm maintains its "H" (active) state.

[0082] As described above, in a case where the sync signal includes no anomalousness, the gate-on pulse signals Gi outputted from the respective shift circuits SCi (i = 1 to m) are successively made active each for a respective certain period of time in the shift register 10a, and accordingly the pulses P1 to Pm are outputted successively from respective shift circuits in an order of ordinary number, from the shift circuit SC1 in the first stage to the shift circuit SCm in the end stage.

[0083] Fig. 5 is a timing chart illustrating waveforms of a vertical sync signal VSYNC, a gate start pulse signal GSP, a first clock signal CK1, a second clock signal CK2, gate on-pulse signals Gi (i = 1 to m), and a clear signal (CLR), in a case where the sync signal includes anomalousness.

[0084] Operations of the shift resister 10a from. t0 to t5 in Fig. 5 are identical to those illustrated in Fig. 4. At t5, CK2 falls and becomes "L", and the electric potential at netA2 also returns to "H"; however, since Trb of SC2 remains turned ON, CK2 is continuously outputted via Qo2. According to the configuration, G2 is inactivated from "H" to "L", and this state "L" is maintained. At t5, G2 is inactivated and becomes "L", but the electric potential at netA3 is maintained at "H" by the capacitor C of the shift circuit SC3, and accordingly the transistor Trb of the shift circuit SC3 remains turned ON.

[0085] In a case where, as illustrated in Fig. 5, noise generates in the vertical sync signal VSYNC between t3 and t4, and accordingly GSP is activated at an unexpected timing (t4), the clear signal CLR is activated and becomes "H" at t6. This causes Trc of SC3 to be turned ON, which connects netA3 to Vss, thereby causing the electric potential at netA3 to change from "H" to "L". As a result, Trb of SC3 turns OFF, and CK1 is no longer outputted via Qo3. Accordingly, G3 remains at "L" (inactive). According to the configuration, no pulse is outputted from SC3; this avoids Trb of SC4, SC5, ... and SCm to be turned ON, which shift circuits are the shift circuits in the subsequent stages, and as a result no pulse is outputted from these shift circuits. Hence, during a current vertical scanning period, no pulse is outputted from the shift circuits subsequent to the shift circuit SC2 (pulse P2), and accordingly the gate on-pulse signals outputted from the respective stages remain at "L" (inactive) until a subsequent vertical scanning period (T0) starts.

[0086] Note that, in Fig. 5, the clear signal CLR is activated at t6, however the present invention is not limited to this. The clear signal CLR can be activated between t5 and t6.

[0087] According to the embodiment, the clear signal CLR becomes "H" (active) in a case where the sync signal (VSYNC, HSYNC, or DE) includes anomalousness, and no pulse is outputted from the shift register thereafter until the subsequent vertical scanning period starts. This makes it possible to prevent occurrence of display disorder and to hold down increase of load given on the power source.

[0088] Note that the shift register 10a illustrated in Fig. 3 can be configured as like a shift register 10b illustrated in Fig. 6. The shift register 10b, in addition to the configuration of the shift register 10a, includes a N-channel low-potential supplying transistor Tre in the shift circuit SCm in the end stage. The transistor Tre has its source terminal be connected to the lower-potential-side power supply, its drain terminal be connected to the node Qom, and its gate terminal be connected to the node CLm.

[0089] According to the configuration of the shift register 10b, it is possible to cause Gm to fall by activating the clear signal CLR. Accordingly, as shown in Fig. 7, the clear signal CLR is activated synchronously with the fall (inactivation) of Gm, at ty.

[0090] Alternatively, the shift register 10a illustrated in Fig. 3 can be configured as like a shift register 10c illustrated in Fig. 8. The shift register 10c, in addition to the configuration of the shift register 10a, includes an N-channel low-potential supplying transistor Tre in each of the shift circuits SCi (i = 1 to m-1). The transistor Tre has its source terminal connected to the lower-potential-side power supply, its drain terminal connected to the node Qoi, and its gate terminal connected to the node Qbi.

[0091] The following describes operations of the shift register 10c illustrated in Fig. 8. Fig. 9 is a timing chart illustrating waveforms of a vertical sync signal VSYNC, a gate start pulse signal GSP, a first clock signal CK1, a second clock signal CK2, gate on-pulse signals Gi (i = 1 to m), and a clear signal (CLR), each in a case where the sync signal includes no anomalousness. Note that each of the first clock signal CK1 and the second clock signal CK2 includes, in one cycle, one clock period of a "H" (active) period and one clock period of a "L" (inactive) period. Upon fall of one of the clock signals CK1 and CK2, the other one of the clock signals CK1 and CK2 synchronously rises.

[0092] At t0 in Fig. 9, activation of GSP causes a rise in electric potential of Qf1. This rise in the electric potential turns Tra of SC1 ON, thereby causing electric potential at netA1 to change from "L" to "H". As a result, Trb of SC1 turns ON, and accordingly CK1 is outputted via Qo1. According to the configuration, the gate on-pulse signal G1 remains at "L".

[0093] At t1, which is a timing one clock period elapsed after t0, GSP falls (is inactivated) and becomes "L". However, no fall occurs to the electric potential at netA1 by

the capacitor C of SC1, and accordingly Trb of SC1 remains turned ON. According to the configuration, the rise of CK1 causes G1 to activate, and makes G1 be "H". At this point, the electric potential at netA1 rises to an electric potential higher than "H" by the capacitor C. Moreover, the activation of G1 causes electric potential at Qf2 to rise. As a result, Tra of SC2 is turned ON, thereby causing electric potential at netA2 to change from "L" to "H". This also causes Trb of SC2 to be turned ON, and accordingly CK2 is outputted via Qo2. According to the configuration, G2 remains at "L".

[0094] At t2, which is a timing one clock period elapsed after t1, CK2 rises, thereby causing G2 to activate and become "H". At this point, the electric potential at netA2 rises to an electric potential higher than "H" by the capacitor C. Moreover, the activation of G2 causes electric potential at Qb1 to rise; consequently, Trd of SC1 is turned ON, which connects netA1 to Vss, thereby causing the electric potential at netA1 to change from "H" to "L". As a result, Trb of SC1 is turned OFF, and CK1 is no longer outputted via Qo1. Moreover, the activation of G2 causes electric potential of Qb1 to rise; consequently, Tre of SC1 is turned ON, which connects Qo1 to Vss, thereby causing electric potential at Qo1 to change from "H" to "L". According to the configuration, G1 is inactivated from "H" to "L", and this state "L" is maintained. Note that, even if G1 is inactivated and becomes "L", the electric potential at netA2 is maintained by the capacitor C of SC2, and accordingly Trb of SC2 remains turned ON. Moreover, when the gate on-pulse signal G2 is activated and electric potential of Qf3 rises, Tra of SC3 turns ON, and accordingly electric potential at netA3 is changed from "L" to "H". As a result, Trb of SC3 is turned on, which causes CK1 be outputted via Qo3. According to the configuration, G3 remains at "L".

[0095] At t3, which is a timing one clock period elapsed after t2, CK1 rises, thereby causing G3 to be activated and become "H". Moreover, the activation of G3 causes electric potential of Qb2 to rise. As a result, Trd of the shift circuit SC2 turns ON, which connects netA2 to Vss, thereby causing electric potential at netA2 to change from "H" to "L". Accordingly, Trb of SC2 is turned OFF and CK2 is no longer outputted via Qo2. Moreover, the activation of G3 causes electric potential of Qb2 to rise. As a result, Tre of SC2 is turned ON, which connects Qo2 to Vss, and thus the electric potential at Qo2 is changed from "H" to "L". According to the configuration, G2 is inactivated from "H" to "L", and this state "L" is maintained.

[0096] Further, at tx, CK2 rises, and accordingly Gm is also activated and becomes "H". At this point, the electric potential at netAm rises to an electric potential higher than "H" by the capacitor C.

[0097] At ty, which is a timing one clock period elapsed after tx, CK2 falls and becomes "L", and the electric potential at netAm also is returned back to "H". However, since Trb of SCm is remained turned ON, CK2 is continuously outputted via Qom. According to the configuration, Gm is inactivated from "H" to "L", and this state "L" is maintained.

[0098] At tz, which is a timing one clock period elapsed after ty, the clear signal CLR is activated and becomes "H". Accordingly, Trc of SCm is turned ON, which connects netAm to Vss, thereby causing the electric potential at netAm to change from "H" to "L". As a result, Trb of SCm is turned OFF, and CK2 is no longer outputted via Qom.

[0099] Note that, in Fig. 9, the clear signal CLR is activated at tz (which is one clock period elapsed after the fall of Gm). However, the present invention is not limited to this. For example, the clear signal CLR can be activated between ty and tz (ty exclusive). However, the clear signal CLR should not be activated at ty. This is because, if the clear signal CLR is activated at ty, Gm maintains its "H" (active) state.

[0100] As described above, in a case where the sync signal includes no anomalousness, the gate on-pulse signals Gi outputted from the respective shift circuits SCi (i = 1 to m) are successively activated each for a respective certain period of time in the shift register 10b, and accordingly the pulses are outputted successively from respective shift circuits in the order of ordinary number, from the shift circuit SC1 in the first stage until the shift circuit SCm in the end stage.

[0101] Fig. 10 is a timing chart illustrating waveforms of a vertical sync signal VSYNC, a gate start pulse signal GSP, a first clock signal CK1, a second clock signal CK2, gate on-pulse signals Gi (i = 1 to m), and a clear signal (CLR), in a case where the sync signal includes anomalousness.

[0102] Operations of the shift resister 10c from t0 to t3 in Fig. 10 are identical to those shown in Fig. 9. In a case where noise generates in the vertical sync signal VSYNC between t2 and t3 and accordingly GSP is activated at an unexpected timing (t3) (see Fig. 10), the clear signal CLR is activated and becomes "H" at t4. This causes Trc of SC3 to be turned ON, which connects netA3 to Vss, thereby causing the electric potential at netA3 to change from "H" to "L". As a result, Trb of SC3 turns OFF, and CK1 is no longer outputted via Qo3. Accordingly, the gate on-pulse signal G3 remains at "L" (inactive). According to the configuration, no pulse is outputted from SC3; this avoids Trb of SC4, SC5, ... and SCm to be turned ON, which shift circuits are the shift circuits in the subsequent stages, and as a result no pulse is outputted from these shift circuits. Accordingly, during a current vertical scanning period, no pulse is outputted from the shift circuits subsequent to the shift circuit SC2, and accordingly the gate on-pulse signals outputted from the respective stages remain at "L" (inactive) until a subsequent vertical scanning period (T0) starts.

[0103] Note that, in Fig. 10, the clear signal CLR is activated at t4, however the present invention is not limited to this. The clear signal CLR can also be activated at t5.

[0104] Note that the shift register 10c illustrated in Fig. 8 can be configured as like a shift register 10d illustrated

in Fig. 11. The shift register 10d, in addition to the configuration of the shift register 10c, includes an N-channel low-potential supplying transistor Tre in the shift circuit SCm in the end stage. The transistor Tre has its source terminal be connected to the lower-potential-side power supply, its drain terminal be connected to the node Qom, and its gate terminal be connected to the node CLm.

[0105] According to the configuration of the shift register 10d, it is possible to cause Gm to fall by activating the clear signal CLR. Accordingly, as shown in Fig. 12, the clear signal CLR is activated synchronously with the fall (inactivation) of Gm, at ty.

[0106] Alternatively, the shift register 10a illustrated in Fig. 3 can be configured as like a shift register 10e illustrated in Fig. 13. The shift register 10e, in addition to the configuration of the shift register 10a, includes an N-channel low-potential supplying transistor Tre in each of the shift circuits SCi (i = 1 to m). The transistor Tre has its source terminal be connected to the lower-potential-side power supply, its drain terminal be connected to the node Qoi, and its gate terminal be connected to the first clock line CKL1 or the second clock line CKL2. Note that, in a case where i is an odd number, the gate terminal of the transistor Tre of the shift circuit SCi is connected to the second clock line CKL2, and in a case where i is an even number, the gate terminal of the transistor Tre is connected to the first clock line CKL1.

[0107] The following describes operations of the shift register 10e illustrated in Fig. 13. Fig. 14 is a timing chart illustrating waveforms of a vertical sync signal VSYNC, a gate start pulse signal GSP, a first clock signal CK1, a second clock signal CK2, gate on-pulse signals Gi (i = 1 to m), and a clear signal (CLR), in a case where the sync signal includes no anomalousness. Note that each of the first clock signal CK1 and the second clock signal CK2 includes, in one cycle, one clock period of a "H" (active) period and one clock period of a "L" (inactive) period. Upon fall of one of the clock signals CK1 and CK2, the other one of the clock signals CK1 and CK2 synchronously rises.

[0108] At t0 in Fig. 14, activation of GSP causes a rise in electric potential of Qf1. The rise in the electric potential turns Tra of SC1 ON, thereby causing electric potential at netA1 to change from "L" to "H". As a result, Trb of SC1 is turned ON, and accordingly CK1 is outputted via Qo1.

[0109] At t1, which is a timing one clock period elapsed after t0, GSP falls (is inactivated) and becomes "L". However, no fall occurs to the electric potential at netA1 by the capacitor C of SCi1, and accordingly Trb of SC1 remains turned ON. According to the configuration, the rise of CK1 causes G1 to activate, and makes G1 be "H". At this point, the electric potential at netA1 rises to an electric potential higher than "H" by the capacitor C. Moreover, the activation of G1 causes electric potential at Qf2 to rise. As a result, Tra of SC2 is turned ON, thereby causing electric potential at netA2 to change from "L" to "H". This also causes Trb of SC2 to be turned ON, and accordingly CK2 is outputted via Qo2. According to the configuration, G2 remains at "L".

[0110] At t2, which is a timing one clock period elapsed after t1, CK2 rises, thereby causing G2 to be activated and become "H". At this point, the electric potential at netA2 rises to an electric potential higher than "H" by the capacitor C. Moreover, the activation of G2 causes electric potential at Qb1 to rise; consequently, Trd of SC1 is turned ON, which connects netA1 to Vss, thereby causing the electric potential at netA1 to change from "H" to "L". As a result, Trb of SC1 is turned OFF, and CK1 is no longer outputted via Qo1. Moreover, since CK2 rises at t2, Tre of SC1 is turned ON, which connects Qo1 to Vss, thereby causing the electric potential at Qo1 to change from "H" to "L". According to the configuration, the gate on-pulse signal G1 is inactivated from "H" to "L", and this state "L" is maintained. Note that, even if G1 is inactivated and becomes "L", the electric potential at netA2 is maintained by the capacitor C of SC2, and accordingly Trb of SC2 remains turned ON. Moreover, when the gate on-pulse signal G2 is activated and electric potential of Qf3 rises, Tra of SC3 turns ON, and accordingly electric potential at netA3 is changed from "L" to "H". As a result, Trb of SC3 is turned on, which causes CK1 be outputted via Qo3. According to the configuration, G3 remains at "L".

[0111] At t3, which is a timing one clock period elapsed after t2, CK1 rises, thereby causing G3 to be activated and become "H". Moreover, the activation of G3 causes electric potential of Qb2 to rise. As a result, Trd of SC2 is turned ON, which connects netA2 to Vss, thereby causing electric potential at netA2 to change from "H" to "L". Accordingly, Trb of SC2 is turned OFF and CK2 is no longer outputted via Qo2. Moreover, at t3, CK1 rises. This causes Tre of SC2 to be turned ON, which connects Qo2 to Vss, thereby causing the electric potential at node Qo2 to change from "H" to "L". According to the configuration, G2 is inactivated from "H" to "L", and this state "L" is maintained.

[0112] Note that, in the shift register 10e, CK2 is at "H" during t4 to t5 and during t6 to t7. Accordingly, Tre of SC1 is turned ON, which connects Qo1 to Vss. This makes it possible to have G1 fall to "L" again (i.e., be drawn to "L"). Similarly, CK1 is at "H" during t5 to t6. Accordingly, Tre of SC2 is turned ON, which connects Qo2 to Vss. This makes it possible to have G2 fall to "L" again (be drawn to "L").

[0113] Further, at tx, CK2 rises; accordingly, Gm is activated and becomes "H". At this point, the electric potential at netAm rises to an electric potential higher than "H" by the capacitor C.

[0114] At ty, which is a timing one clock period elapsed after tx, the clear signal CLR is activated and becomes "H". Accordingly, the transistor Trc of the shift circuit SCm is turned ON, which connects netAm to Vss. This causes the electric potential at netAm to fall to "L". As a result, Trb of SCm is turned OFF, and CK2 is no longer outputted via Qom. Further, at ty, CK1 rises. Accordingly, Tre of

SCm is turned ON, which connects Qom to Vss. As a result, Gm is inactivated and becomes "L".

[0115] Note that, in Fig. 14, the clear signal CLR is activated at ty, however the present invention is not limited to this. For example, the clear signal CLR can be activated between ty and tz (ty and tz inclusive).

[0116] As described above, in a case where the sync signal includes no anomalousness, the gate on-pulse signals Gi outputted from the respective shift circuits SCi (i = 1 to m) are successively activated each for a respective certain period of time in the shift register 10e, and accordingly the pulses are outputted successively from respective shift circuits in the order of ordinal number, from the shift circuit SC1 in the first stage until the shift circuit SCm in the end stage.

[0117] Fig. 15 is a timing chart illustrating waveforms of a vertical sync signal VSYNC, a gate start pulse signal GSP, a first clock signal CK1, a second clock signal CK2, gate on-pulse signals Gi (i = 1 to m), and a clear signal (CLR), in a case where the sync signal includes anomalousness.

[0118] Operations of the shift register 10b from t0 to t3 in Fig. 15 are identical to those illustrated in Fig. 14. In a case where noise generates in the vertical sync signal VSYNC between t1 and t2, and accordingly the gate start pulse signal GSP is activated at an unexpected timing (t2) (see Fig. 15), the clear signal CLR is activated and becomes "H" at t3. This causes Trc of SC3 to be turned ON, which connects netA3 to Vss, thereby causing the electric potential at netA3 to change from "H" to "L". As a result, Trb of SC3 is turned OFF, and CK1 is no longer outputted via Qo3. Accordingly, G3 remains at "L" (inactive). According to the configuration, no pulse is outputted from SC3; this avoids Trb of SC4, SC5, ... and SCm to be turned ON, which shift circuits are the shift circuits in the subsequent stages, and as a result no pulse is outputted from these shift circuits. Accordingly, during the current vertical scanning period, no pulse is outputted from the shift circuits subsequent to the shift circuit SC2, and accordingly the gate on-pulse signals outputted from the respective stages remain at "L" (inactive) until a subsequent vertical scanning period (T0) starts.

[0119] In this case also, CK2 is at "H" during t4 to t5 and during t6 to t7. Accordingly, Tre of SC1 is turned ON, which connects Qo1 to Vss. This makes it possible to have G1 fall to "L" again (i.e., drawn to "L"). Similarly, CK1 is at "H" during t5 to t6. Accordingly, the transistor Tre of the shift circuit SC2 is turned ON, which connects Qo2 to Vss. This makes it possible to have G2 fall to "L" again (drawn to "L").

[0120] Note that, in Fig. 15, the clear signal CLR is activated at t3, however the present invention is not limited to this. The clear signal CLR can be activated between t3 and t4 (t4 and t5 inclusive). For example, Fig. 16 illustrates a case where the clear signal CLR is activated between t3 and t4. That is, at ta, Trc of SC3 is turned ON, which connects netA3 to Vss, thereby causing the electric potential at netA3 to change from "H" to "L". As a result, Trb of SC3 is turned OFF, and CK1 is no longer outputted via Qo3. This causes G3 to remain at "H" (active). Moreover, at ta, Trc of SC4 is turned ON, which connects netA4 to Vss, thereby causing the electric potential at netA4 to change from "H" to "L". As a result, Trb of SC4 is turned OFF; CK2 is no longer outputted via Qo4 and G4 remains at "L" (inactive). Note that, at t4, CK2 rises. This causes Tre of SC3 to be turned ON, which connects Qo3 to Vss. As a result, G3 is inactivated and becomes "L" (inactive).

[0121] In the case of Fig. 16, a through current flows from CKL1 to Vss, during the period between ta and t4, via a path indicated by the arrow illustrated in Fig. 17. This may exert load on a power supply voltage. In view of this, in cases where the clear signal CLR is activated at ta, such a through current in Fig. 17 is prevented by causing CK1 to fall to "L" during a period in which the clear signal CLR is at "H" (active), as illustrated in Fig. 18.

Embodiment 2

[0122] Fig. 19 illustrates a configuration of a liquid crystal panel of the present Embodiment 2. According to the liquid crystal panel illustrated in Fig. 19, a shift register 10f is provided on a left end of the liquid crystal panel, and a shift register 10g is provided on a right end of the liquid crystal panel. The shift register 10f is made up of a plurality of shift circuits SCi (i = 1, 3, 5, ... and 2n+1) connected in stages, and a plurality of shift circuits SCi (i = 2, 4, 6, ... and 2n) connected in stages. Each of the shift circuits SCi (i = 1, 2, 3, ... and 2n-2) includes input nodes Qfi, Qbi, CKAi, CKBi, and CLi, and an output node Qoi. A shift circuit SC(2n-1) includes input nodes Qf(2n-1), CKA(2n-1), CKB(2n-1), and CL(2n-1), and an output node Qo(2n-1). Moreover, a shift circuit SC(2n) includes input nodes Qf(2n), CKA(2n), CKB(2n), and CL(2n), and an output node Qo(2n).

[0123] The shift circuit SC1 has its node Qf1 be connected to a GASP1 output terminal RO1 of a level shifter (see Fig. 23). Further, the shift circuit SC1 has its node Qb1 be connected to the node Qo3 of the shift circuit SC3, has its node CKA1 be connected to a first clock line CKL1 to which a first clock signal is supplied, has its node CKB1 be connected to a third clock line CKL3 to which a third clock signal is supplied, and has its node CL1 be connected to a first clear line CLRL1 to which a first clear signal (CLR1) is supplied. Further, the shift circuit SC1 outputs a gate on-pulse signal (signal line selection signal) G1 via its node Qo1.

[0124] The shift circuit SC2 has its node Qf2 be connected to a GSP2 output terminal RO2 of the level shifter. Further, the shift circuit SC2 has its node Qb2 be connected to a node Qo4 of a shift circuit SC4, has its node CKA2 be connected to a second clock line CKL2 to which a second clock signal is supplied, has its node CKB2 be connected to a fourth clock line CKL4 to which a fourth clock signal is supplied, and has its node CL2 be connected to a second clear line CLRL2 to which a second

clear signal (CLR2) is supplied. Further, the shift circuit SC2 outputs a gate on-pulse signal (signal line selection signal) G2 via its node Qo2.

[0125] Each of the shift circuits SCi (i = 3 to 2n-2) has its node Qfi be connected to the node Qo(i-2) of the shift circuit SC(i-2), and has its node Qbi be connected to the node Qo(i+2) of the shift circuit SC(i+2). In a case where i is an odd number, the node CLi is connected to the first clear line CLRL1, and in a case where i is an even number, the node CLi is connected to the second clear line CLRL2. Moreover, in a case where i is a multiple of 4 + 1, the node CKAi is connected to the first clock line CKL1 and the node CKBi is connected to the third clock line CKL3; in a case where i is a multiple of 4 + 2, the node CKAi is connected to the second clock line CKL2 and the node CKBi is connected to the fourth clock line CKL4; in a case where i is a multiple of 4 + 3, the node CKAi is connected to the third clock line CKL1 and the node CKBi is connected to the first clock line CKL3; and in a case where i is a multiple of 4, the node CKAi is connected to the fourth clock line CKL4 and the node CKBi is connected to the second clock line CKL2. Further, each of the shift circuits SCi (i = 3 to 2n-2) output a gate on-pulse signal (signal line selection signal) Gi via the node Qoi.

[0126] The shift circuit SC(2n-1) has its node Qf(2n-1) be connected to the node Qo(2n-3) of the shift circuit SC (2n-3), has its node CKA(2n-1) be connected to the third clock line CKL3, has its node CKB(2n-1) be connected to the first clock line CKL1, and has its node CL(2n-1) be connected to the first clear line CLRL1. Further, the shift circuit SC(2n-1) outputs a gate on-pulse signal (signal line selection signal) G(2n-1) via its node Qo(2n-1).

[0127] The shift circuit SC(2n) has its node Qf(2n) be connected to the node Qo(2n-2) of the shift circuit SC (2n-2), has its node CKA(2n) be connected to the fourth clock line CKL4, has its node CKB(2n) be connected to the second clock line CKL2, and has its node CL(2n) be connected to the second clear line CLRL2. Further, the shift circuit SC(2n) outputs a gate on-pulse signal (signal line selection signal) G(2n) via its node Qo(2n).

[0128] Specifically illustrated in (a) of Fig. 20 is a circuit diagram of a configuration employed in each of the shift circuits SCi (i = 1 to 2n-2). As illustrated in (a) of Fig. 20, each of the shift circuits SCi (i = 1 to 2n-2) includes a set transistor Tra, an output transistor Trb, a clear transistor Trc, a reset transistor Trd, a low-potential supplying transistor Tre, and a capacitor C. Note that each of the transistors Tra to Tre is an N-channel transistor.

[0129] Trb has its source terminal be connected to a first electrode of the capacitor C. Tra has its gate terminal (control terminal) and its drain terminal be connected to each other, and Tra has its source terminal be connected to (i) a gate terminal of Trb and (ii) a second electrode of the capacitor C. Trc has its drain terminal be connected to the gate terminal of Trb, and Trc has its source terminal connected to a lower-potential-side power supply Vss. Moreover, Trd has its drain terminal be connected to the gate terminal of Trb, and Trd has its source terminal be connected to the lower-potential-side power supply Vss. Tre has its drain terminal be connected to the source terminal of Trb, and Tre has its source terminal be connected to the lower-potential-side power supply Vss. The gate terminal of Tra is connected to the node Qfi, and the drain terminal of Trb is connected to the node CKAi. Tre has its gate terminal be connected to the node CKBi, Trc has its gate terminal be connected to the node CLi, Trd has its gate terminal be connected to the node Qbi, and the source terminal of Trb is connected to the node Qoi. Note that a connection point of the source terminal of Tra, the second electrode of the capacitor C, and the gate terminal of Trb is defined as a node netAi.

[0130] Specifically illustrated in (b) of Fig. 20 is a circuit diagram of a configuration of the shift circuit SCj (j = (2n-1) or 2n). As illustrated in (b) of Fig. 20, the shift circuit SCj includes a set transistor Tra, an output transistor Trb, a clear transistor Trc, a potential supplying transistor Tre, and a capacitor C. Note that each of the transistors Tra to Trc and Tre is an N-channel transistor.

[0131] In the embodiment, Trb has its source terminal be connected to a first electrode of the capacitor C. Tra has its gate terminal (control terminal) and its drain terminal be connected to each other, and Tra has its source terminal be connected to (i) a gate terminal of Trb and (ii) a second electrode of the capacitor C. Trc has its drain terminal be connected to the gate terminal of Trb and has its source terminal be connected to a lower-potential-side power supply Vss. Tre has its drain terminal be connected to the source terminal of Trb and has its source terminal be connected to the lower-potential-side power supply Vss. The gate terminal of Tra is connected to the node Qfj. Trb has its drain terminal be connected to the node CKAj. Tre has its gate terminal be connected to the node CKBj. Trc has its gate terminal be connected to the node CLj. Further, the source terminal of the transistor Trb is connected to the node Qoj. A connection point of the source terminal of Tra, the second electrode of the capacitor C, and the gate terminal of Trb is defined as a node netAj.

[0132] The nodes (Qfi, Qbi, CKAi, CKBi, CLi, and Qoi) in each of the shift circuits SCi (i = 1 to 2n-2) and the nodes (Qfj, CKAj, CKBj, CLj, and Qoj) in the shift circuit SCj (j = (2n-1) or 2n) are connected to respective destinations as illustrated in Fig. 19.

[0133] The following describes operations of the shift registers 10f and 10g illustrated in Fig. 19. Fig. 21 is a timing chart illustrating waveforms of a vertical sync signal VSYNC, gate start pulse signals GSP1 and GSP2, a first clock signal CK1, a second clock signal CK2, a third clock signal CK3, a fourth clock signal CK4, gate on-pulse signals Gi (i = 1 to 2n), a first clear signal CLR1, and a second clear signal CLR2, in a case where the sync signal includes no anomalousness. Note that each of CK1 to CK4 has, in one cycle, one clock period of a "H" (active) period and three clock periods of a "L" (inactive) period. Upon fall of CK1, CK2 synchronously rises, upon fall of

CK2, CK3 synchronously rises, upon fall of CK3, CK4 synchronously rises, and upon fall of CK4, CK1 synchronously rises. Further, GSP2 rises one clock period elapsed after the rise of GSP1.

[0134] At t0 in Fig. 21, activation of GSP1 causes a rise in electric potential of Qf1. This rise in the electric potential turns Tra of SC1 ON, thereby causing electric potential at netA1 to change from "L" to "H". As a result, Trb of SC1 is also turned ON, and accordingly CK1 is outputted via Qo1. According to the configuration, G1 remains at "L".

[0135] At t1, which is a timing one clock period elapsed after t0, GSP1 falls to "L". However, the electric potential at netA1 is maintained at "H" by the capacitor C of SC1, and accordingly Trb of SC1 remains turned ON. Moreover, at t1, the activation of GSP2 causes electric potential of Qf2 to rise. As a result, Tra of SC2 is turned ON, which causes electric potential at netA2 to change from "L" to "H". This also causes Trb of SC2 to be turned ON, and accordingly CK2 is outputted via Qo2. According to the configuration, G2 remains at "L".

[0136] At t2, which is a timing one clock period elapsed after t1, CK1 rises, thereby causing G1 to be activated and become "H". At this point, the electric potential at netA1 rises to an electric potential higher than "H" by the capacitor C. Moreover, the activation of G1 causes electric potential of Qf3 to rise. As a result, Tra of SC3 is turned ON, and accordingly the electric potential at netA3 changes from "L" to "H". This also causes Trb of c SC3 to be turned ON, and accordingly CK3 is outputted via Qo3. According to the configuration, G3 remains at "L". Moreover, at t2, GSP2 falls to "L", however the electric potential at netA2 is maintained at "H" by the capacitor C of SC2, and Trb of SC2 remains turned ON.

[0137] At t3, which is a timing one clock period elapsed after t2, CK1 falls and becomes "L", and the electric potential at netA1 is also returned back to "H". However, since Trb of SC1 remains turned ON, CK1 is continuously outputted via Qo1. As a result, the gate on-pulse signal G1 is inactivated from "H" to "L", and this state "L" is maintained. Note that, even if G1 is inactivated and becomes "L", the electric potential at netA3 is maintained at "H" by the capacitor C of SC3, and the transistor Trb of SC3 remains turned ON. Moreover, at t3, CK2 rises; consequently, G2 also is activated and becomes "H". At this point, the electric potential at netA2 rises to an electric potential higher than "H" by the capacitor C. Moreover, at t3, the activation of G2 causes electric potential of Qf4 to rise; consequently, Tra of SC4 turns ON, which causes the electric potential at netA4 to change from "L" to "H". As a result, Trb of SC4 also turns ON, and CK4 is outputted via Qo4. According to the configuration, G4 remains at "L".

[0138] At t4, which is a timing one clock period elapsed after t3, CK3 rises, thereby causing G3 to be activated and become "H". At this point, the electric potential at netA3 rises to an electric potential higher than "H" by the capacitor C. Moreover, the activation of G3 causes electric potential at Qb1 to rise; consequently, Trd of SC1 turns ON, which connects netA1 to Vss, thereby causing the electric potential at netA1 to change from "H" to "L". As a result, Trb of SC1 is turned OFF, and CK1 is no longer outputted via Qo1. Moreover, at t4, CK3 rises; consequently, Tre of SC1 is turned ON, which connects Qo1 to Vss, thereby causing the electric potential at Qo1 to fall to "L" (i.e., G1 is drawn to "L"). Moreover, at t4, CK2 falls to "L" and the electric potential at netA2 also returns to "H". However, since Trb of SC2 remains turned ON, CK2 is continuously outputted via Qo2. According to the configuration, G2 is inactivated from "H" to "L", and this state "L" is maintained.

[0139] At t5, which is a timing one clock period elapsed after t4, CK4 rises, thereby causing G4 to be activated and become "H". At this point, the electric potential at netA4 rises to an electric potential higher than "H" by the capacitor C. Moreover, the activation of G4 causes an electric potential of Qb2 to rise. As a result, Trd of SC2 is turned ON, which connects netA2 to Vss, thereby causing the electric potential at netA2 to change from "H" to "L". This causes Trb of SC2 to be turned OFF, and CK2 is no longer outputted via Qo2. Moreover, at t5, CK4 rises; consequently, Tre of SC2 also is turned ON, which connects Qo2 to Vss, and accordingly the electric potential at Qo2 falls and becomes "L" (i.e., G2 is drawn to "L"). Moreover, at t5, CK3 falls and becomes "L" and the electric potential at netA3 also returns back to "H". However, since Trb of SC3 remains turned ON, CK3 is continuously outputted via Qo3. As a result, G3 is inactivated from "H" to "L", and this state "L" is maintained.

[0140] At t6, which is a timing one clock period elapsed after t5, CK1 rises, thereby causing G5 to be activated and become "H". At this point, the electric potential at netA5 rises to an electric potential higher than "H" by the capacitor C. Moreover, the activation of G5 causes an electric potential of Qb3 to rise; consequently, Trd of SC3 is turned ON, which connects netA3 to Vss, thereby causing the electric potential at netA3 to change from "H" to "L". Accordingly, Trb of SC3 is turned OFF, and CK3 is no longer outputted via Qo3. Moreover, at t6, CK1 rises; consequently, Tre of SC3 is turned ON, which connects Qo3 to Vss, and accordingly the electric potential at Qo3 falls and becomes "L" (i.e., G3 is drawn to "L"). Moreover, at t6, CK4 falls and becomes "L", and the electric potential at netA4 also returns back to "H". However, since Trb of SC4 remains turned ON, CK4 is continuously outputted via Qo4. As a result, G4 is inactivated from "H" to "L", and this state "L" is maintained.

[0141] At t7, which is a timing one clock period elapsed after t6, CK2 rises, thereby causing G6 to be activated and become "H". At this point, the electric potential at netA6 rises to an electric potential higher than "H" by the capacitor C. Moreover, the activation of G6 causes electric potential of Qb4 to rise. As a result, Trd of SC4 is turned ON, which connects netA4 to Vss, thereby causing the electric potential at netA4 to change from "H" to "L". This causes Trb of SC4 to be turned OFF, and CK4

is no longer outputted via Qo4. Moreover, at t7, CK2 rises; consequently, Tre of SC4 is turned ON, which connects Qo4 to Vss, and accordingly the electric potential at Qo4 falls to "L" (i.e., G4 is drawn to "L").

[0142] At tx, CK3 rises, thereby causing the G(2n-1) to be activated and become "H". At this point, the electric potential at netA(2n-1) rises to an electric potential higher than "H" by the capacitor C.

[0143] At ty, which is a timing one clock period elapsed after tx, CK4 rises, whereby G(2n) activates and becomes "H" (active). At this point, the electric potential at netA(2n) rises to an electric potential higher than "H" by the capacitor C. Moreover, at ty, CK3 falls and becomes "L" and the electric potential at netA(2n-1) is also returned back to "H". However, since the transistor Trb of the shift circuit SC(2n-1) remains turned on, CK3 is continuously outputted via Qo(2n-1). As a result, G(2n-1) is inactivated from "H" to "L", and this state "L" is maintained.

[0144] At tz, which is a timing one clock period elapsed after ty, the first clear signal CLR1 is activated and becomes "H"; consequently, Trc of SC(2n-1) is turned ON, which connects netA(2n-1) to Vss, thereby causing the electric potential at netA(2n-1) to change from "H" to "L". As a result, Trb of SC(2n-1) is turned OFF, and CK3 is no longer outputted via Qo(2n-1). Further, CK1 rises; consequently, Tre of SC(2n-1) is turned ON, which connects Qo(2n-1) to Vss, and accordingly the electric potential at Qo(2n-1) falls to "L" (i.e., G(2n-1) is drawn to "L"). Moreover, at tz, CK4 falls and becomes "L", and the electric potential at netA(2n) is also returned back to "H". However, since Trb of SC(2n) remains turned ON, CK4 is continuously outputted via Qo(2n). As a result, G(2n) is inactivated from "H" to "L", and this state "L" is maintained.

[0145] At tw, which is a timing one clock period elapsed after ty, the second clear signal CLR2 is activated and becomes "H"; consequently, Trc of SC(2n) is turned ON, which connects netA(2n) to Vss, thereby causing the electric potential at netA(2n) to change from "H" to "L". As a result, Trb of SC(2n) is turned OFF, and CK4 is no longer outputted via Qo(2n). Further, CK2 rises; consequently, Tre of SC(2n) is turned ON, which connects Qo (2n) to Vss, and accordingly the electric potential at Qo (2n) falls to "L" (i.e., G(2n) is drawn to "L").

[0146] As described above, in a case where the sync signal includes no anomalousness, the gate-on pulse signals Gi outputted from the respective shift circuits SCi (i = 1, 3, 5, ... and 2n-1) are successively activated each for a respective certain period of time in the shift register 10f, and accordingly the pulses P1, P3, ... and P(2n-1) are outputted successively from respective shift circuits in the order of odd ordinal numbers, from the shift circuit SC1 in the first stage until the shift circuit SC(2n-1) in the end stage. Moreover, the gate-on pulse signals Gi outputted from the respective shift circuits SCi (i = 2, 4, 6, ... and 2n) are successively made active each for a respective certain period of time in the shift register 10g, and accordingly the pulses P1, P2, ... and P(2n) are outputted successively from the respective shift circuits in the order of even ordinal number, from the shift circuit SC2 in the first stage until the shift circuit SC(2n) in the end stage.

[0147] Fig. 22 is a timing chart illustrating waveforms of a vertical sync signal VSYNC, gate start pulse signals GSP1 and GSP2, a first clock signal CK1, a second clock signal CK2, a third clock signal CK3, a fourth clock signal CK4, gate on-pulse signals Gi (i = 1 to 2n), a first clear signal CLR1, and a second clear signal CLR2, in a case where the sync signal includes anomalousness.

[0148] Operations of the shift resisters 10f and 10g from t0 to t3 in Fig. 22 are identical to those illustrated in Fig. 21. In a case where, as illustrated in Fig. 22, noise generates in the vertical sync signal VSYNC between t2 and t3, and accordingly GSP1 is activated at an unexpected timing (t3) and GSP2 is activated at an unexpected timing (t4), the first clear signal CLR1 is activated and becomes "H" at t4 and the second clear signal CLR2 is activated and becomes "H" at t5. As a result, at t4, Trc of SC3 is turned ON, which connects netA3 to Vss, thereby causing electric potential at netA3 to change from "H" to "L". Accordingly, Trb of SC3 is turned OFF, and CK3 is no longer outputted via Qo3, and further G3 remains at "L" (inactive). According to the configuration, no pulse is outputted from SC3; this avoids Trb of SC5, SC7, ... and SC(2n-1) to be turned ON, which shift registers are the shift registers provided in the subsequent stages, and as a result no pulse is outputted from these shift circuits. At t4, CK3 rises; consequently, Tre of SC1 is turned ON, which connects Qo1 to Vss, and accordingly the electric potential at Qo1 falls to "L" (i.e., G1 is drawn to "L").

[0149] At t5, Trc of SC4 is turned ON, which connects netA4 to Vss, thereby causing the electric potential at netA4 to change from "H" to "L". As a result, Trb of SC4 is turned OFF, and CK4 is no longer outputted via Qo4. Accordingly, G4 remains at "L" (inactive). According to the configuration, no pulse is outputted from SC4; this avoids Trb of SC6, SC8, ... and SC(2n) to be turned ON, which shift circuits are the shift circuits provided in the subsequent stages, and as a result no pulse is outputted from these shift circuits. At t5, CK4 rises; consequently, Tre of SC2 is turned ON, which connects Qo2 to Vss, and accordingly the electric potential at Qo2 falls to "L" (i.e., G2 is drawn to "L").

[0150] According to the configuration of the shift register 10f, no pulse is outputted from the shift circuits subsequent to the shift circuit SC1 during a current vertical scanning period, and accordingly the gate on-pulse signals outputted from the respective stages (SC1, SC3, ... and SC(2n-1)) remain at "L" (inactive) until a subsequent vertical scanning period (T0) starts. Moreover, in the shift register 10g, no pulse is outputted from the shift circuits subsequent to the shift circuit SC2 during the current vertical scanning period, and accordingly the gate on-pulse signals outputted from the respective stages (SC2, SC4, ... and SC(2n)) remain at "L" (inactive) until the subsequent vertical scanning period (T0) starts.

[0151] According to Embodiment 2 described above,

the first and second clear signals CLR1 and CLR2 become "H" (active) in a case where the sync signal (VSYNC, HSYNC, or DE) includes anomalousness, and no pulse is outputted from the shift registers (10f, 10g) thereafter until the subsequent vertical scanning period starts. This makes it possible to prevent occurrence of display disorder and to hold down increase of load given on the power source.

[0152] Note that, with the shift registers 10f and 10g illustrated in Fig. 19, GSP1 and GSP2 can be a common gate start pulse signal. In this case, for example in Fig. 21, both the gate start pulse signals GSP1 and GSP2 are made "H" (active) at t0. Moreover, CLR1 and CLR2 can be a common clear signal. In this case, for example in Fig. 21, both CLR1 and CLR2 are made "H" (active) at tw, and in Fig. 22, both CLR1 and CLR2 are made "H" (active) at t5.

[0153] The above description deals with a case where a clear signal is activated caused by anomalousness included in VSYNC. However, it is a matter of course that the clear signal is activated in cases where HSYNC or DE includes anomalousness.

Embodiment 3

[0154] Embodiment 3 is as described below, with reference to Figs. 24 to 36.

[0155] Fig. 24 is a block diagram illustrating a configuration of the present liquid crystal display device. As illustrated in Fig. 24, the present liquid crystal display device 101 includes a liquid crystal panel 103, a gate driver 105, a source driver 106, a timing controller 107, and a data processing circuit 108. The gate driver 105 includes a shift register 110 and a level shifter 104, and the gate driver 105 and the timing controller 107 construct a liquid crystal panel driving circuit 111. In the present embodiment, the level shifter 104 is included in the gate driver 105; however, the level shifter 104 may be provided outside of the gate driver 105.

[0156] The present liquid crystal panel 103 includes scanning signal lines 16 that are driven by the gate driver 105, data signal lines 15 that are driven by the source driver 106, pixels P, retention capacitor wires (not illustrated) and the like, and the shift register 110 is provided monolithically to the liquid crystal panel 103. Each of the pixels P includes (i) a transistor (TFT) connected to one of the scanning signal lines 16 and one of the data signal lines 15 and (ii) a pixel electrode connected to the transistor. Note that the transistor provided in the pixels and the transistor of the shift register can be formed by use of material such as amorphous silicone or polysilicon (e.g., CG silicon).

[0157] The timing controller 107 receives a vertical sync signal VSYNC, a horizontal sync signal HSYNC, and a data enable signal DE, each of which is a sync signal. These signals are received from outside of the liquid crystal display device 101. Moreover, the data processing circuit 108 receives video data (RGB digital data) from outside of the liquid crystal display device 101. The timing controller 107 generates, with use of the sync signals, a plurality of source clock signals (e.g., ck1, ck2), a source clear signal (clr), and a source gate start pulse signal (gsp). The source clock signals (e.g., ck1, ck2), source clear signal (clr), and source gate start pulse signal (gsp) are shifted in level by the level shifter 106, to generate clock signals (e.g., CK1, CK2), a clear signal (CLR), and a gate start pulse signal (GSP), respectively. Moreover, the timing controller 107 outputs a control signal to the data processing circuit 108 in accordance with the received sync signals (VSYNC, HSYNC, and DE), and outputs a source timing signal to the source driver 106.

[0158] The clock signals (CKA, CKB, etc.), clear signal (CLR), and gate start pulse signal (GSP) are supplied to the shift register 110. The clear signal (CLR) is a signal used for resetting the end stage, and becomes "H" (active) after a pulse is outputted from the end stage. The shift register 110 generates a gate on-pulse signal with use of the foregoing signals (CKA, CKB etc.; CLR; and GSP) and this gate on-pulse signal is outputted to the scanning signal lines in the liquid crystal panel 103. The shift register 110 includes shift circuits connected in stages, which each of the shift circuits generates a gate on-pulse signal. The gate on-pulse signals generated in the stages (shift circuits) are successively activated for a respective certain period of time. This causes pulses (on-pulses) to be outputted successively from respective shift circuits in order of ordinal number, from a first stage until an end stage. Thereafter, in the liquid crystal panel 103, the scanning signal lines are successively selected, in accordance with the pulses.

[0159] The data processing circuit 108 carries out a predetermined process to video data, and outputs a data signal to the source driver 106 in accordance with the control signal outputted from the timing controller 107. The source driver 106 generates a signal electric potential by use of the data signal outputted from the data processing circuit 108 and the source timing signal outputted from the timing controller 107, and outputs this electric potential to the data signal lines in the liquid crystal panel 103. Via the transistors provided in each of the pixels, this signal electric potential is written into pixel electrodes of respective pixels.

[0160] Fig. 25 illustrates a configuration of a shift register 110a according to the present embodiment. As illustrated in Fig. 25, the shift register 110a includes a plurality of shift circuits (unit circuits) SC1, SC2, ... SCm that are connected in stages. Each of shift circuits SCi (i = 1, 2, 3, ... m-1) includes input nodes Qfi, Qbi, and CKAi and an output node Qoi, and the shift circuit SCm includes input nodes Qfm, CKAm, and CLm and an output node Qom.

[0161] The shift circuit SC1 has its node Qf1 be connected to a GSP output terminal RO of the level shifter (see Fig. 24). Further, the shift circuit SC1 has its node Qb1 be connected to the node Qo2 of the shift circuit

SC2, and has its node CKA1 be connected to a first clock line CKL1 to which a first clock signal is supplied. Further, the shift circuit SC1 outputs a gate on-pulse signal (signal line selection signal) G1 via its node Qo1.

[0162] Each of the shift circuits SCi (i = 2 to m-1) has its node Qfi be connected to the node Qo(i-1) of the shift circuit SC(i-1), and each of the shift circuits SCi (i = 2 to m-1) has its node Qbi be connected to the node Qo(i+1) of the shift circuit SC(i+1). In a case where i is an odd number, each of the shift circuits SCi has its node CKAi be connected to the first clock line CKL1, and in a case where i is an even number, the node CKAi is connected to the second clock line CKL2. Further, each of the shift circuits SCi outputs a gate on-pulse signal (signal line selection signal) Gi via its node Qoi.

[0163] The shift circuit SCm has its node Qfm be connected to the node Qo(m-1) of the shift circuit SC(m-1), has its node CKAm be connected to the second clock line CKL2, and has its node CLm be connected to the clear line CLRL. Further, the shift circuit SCm outputs a gate on-pulse signal (signal line selection signal) Gm via its node Qom.

[0164] Specifically illustrated in (a) of Fig. 26 is a circuit diagram of a configuration employed by each of SCi (i = 1 to m-1). As illustrated in (a) of Fig. 26, each of SCi (i = 1 to m-1) includes the set transistor Tra, the output transistor Trb, the reset transistor Trd, and the capacitor C. Note that each of the transistors is an N-channel transistor.

[0165] In the embodiment, Trb has its source terminal be connected to a first electrode of the capacitor C. Tra has its gate terminal (control terminal) and its drain terminal be connected to each other, and has its source terminal be connected to (i) a gate terminal of Trb and (ii) a second electrode of the capacitor C. Moreover, Trd has its drain terminal be connected to the gate terminal of Trb, and Trd has its source terminal be connected to a lower-potential-side power supply Vss. Further, the gate terminal of Tra is connected to the node Qfi, Trb has its drain terminal be connected to the node CKAi, Trc has its gate terminal be connected to a node CLi, Trd has its gate terminal be connected to the node Qbi, and the source terminal of Trb is connected to the node Qoi. Note that a connection point of the source terminal of Tra, the second electrode of the capacitor C, and the gate terminal of Trb is defined as a node netBi.

[0166] Moreover, (b) of Fig. 26 is a circuit diagram specifically illustrating a configuration of SCm. As illustrated in (b) of Fig. 26, SCm includes a set transistor Tra, an output transistor Trb, a clear transistor Trc provided for resetting the end stage, and a capacitor C. Note that each of the transistors is an N-channel transistor, and the capacitor C can also be parasitic capacitor. In the embodiment, Trb has its source terminal be connected to a first electrode of the capacitor C. Tra has its gate terminal (control terminal) and its drain terminal be connected to each other, and has its source terminal be connected to (i) a gate terminal of Trb and (ii) a second electrode of the capacitor C. Moreover, Trc has its drain terminal be connected to the gate terminal of Trb, and has its source terminal be connected to a lower-potential-side power supply Vss. Furthermore, the gate terminal of Tra is connected to the node Qfm, Trb has its drain terminal be connected to the node CKAm, Trc has its gate terminal be connected to the node CLm, and the source terminal of Trb is connected to the node Qom. Note that a connection point of the source terminal of Tra, the second electrode of the capacitor C and the gate terminal of Trb is defined as a node netBm.

[0167] The nodes (Qfi, Qbi, CKAi, Qoi) in each of the shift circuits Sci (i = 1 to m-1) and the nodes (Qfm, CKAm, CLm, Qom) in the shift circuit SCm are connected to respective destinations as illustrated in Fig. 25. The configuration of an entire shift register 110a is as specifically illustrated in Fig. 27.

[0168] The following describes operations of the shift register 110a illustrated in Fig. 27. Fig. 28 is a timing chart illustrating waveforms of the vertical sync signal VSYNC, gate start pulse signal GSP, first clock signal CK1, second clock signal CK2, gate on-pulse signals Gi (i = 1 to m), and a clear signal (CLR). Note that each of the first clock signal CK1 and second clock signal CK2 includes, in one cycle, one clock period of a "H" (active) period, and three clock periods of a "L" (inactive) period. After one of CK1 and CK2 is inactivated (falls), the other one of CK1 and CK2 is activated (rises) with a delay of one clock period. Of course, this is merely an example of the first and second clock signals CK1 and CK2; the "H" period and "L" period may be arbitrarily set as long as there is a period in which both clock signals coincide as "L".

[0169] First, at t0 in Fig. 28, activation of GSP causes a rise in electric potential of Qf1. This rise in the electric potential turns Tra of SC1 ON, thereby causing electric potential at netB1 to change from "L" to "H". As a result, Trb of SC1 turns ON, and accordingly CK1 is outputted via Qo1. According to the configuration, G1 remains at "L". At t1, which is a timing one clock period elapsed after t0, GSP falls (is inactivated) and becomes "L". However, the electric potential of netB1 is maintained at "H" by the capacitor C in SC1, and Trb of SC1 also remains turned ON.

[0170] At t2, which is a timing one clock period elapsed after t1, CK1 rises (is activated), thereby causing G1 to be activated and become "H". At this point, the electric potential at netB1 rises to an electric potential higher than "H" by the capacitor C. Moreover, the activation of G1 causes electric potential of Qf2 to rise; consequently, Tra of SC2 turns ON, thereby causing electric potential at netB2 to change from "L" to "H". As a result, Trb of SC2 also turns ON, and accordingly CK2 is outputted via Qo2. According to the configuration, G2 remains at "L".

[0171] At t3, which is a timing one clock period elapsed after t2, CK1 falls and becomes "L", and the electric potential at netB1 also returns back to "H". However, since Trb of SC1 remains turned ON, CK1 is continuously outputted via Qo1. According to the configuration, G1 is in-

activated from "H" to "L", and this state "L" is maintained. Note that, even if G1 is inactivated and becomes "L", the electric potential at netB2 is maintained at "H" by the capacitor C of SC2, and accordingly Trb of SC2 remains turned ON.

[0172] At t4, which a timing one clock period elapsed after t3, CK2 rises, thereby causing G2 to be activated and become "H". At this point, the electric potential at netB2 rises to an electric potential higher than "H" by the capacitor C. Moreover, the activation of G2 causes electric potential at Qb1 to rise; consequently, Trd of SC1 turns ON, which connects netB1 to Vss, thereby causing electric potential at netB1 to change from "H" to "L". As a result, Trb of SC1 is turned OFF, and CK1 is no longer outputted via Qo1.

[0173] At t5, which is a timing one clock period elapsed after t4, CK2 falls and becomes "L" and the electric potential at netB2 also returns back to "H". However, since Trb of SC2 remains turned ON, CK2 is continuously outputted via Qo2. According to the configuration, G2 is inactivated from "H" to "L", and this state "L" is maintained.

[0174] Furthermore, at tx, CK2 rises, and accordingly Gm is also activated and becomes "H". At this point, the electric potential at netBm rises to an electric potential higher than "H" by the capacitor C.

[0175] At ty, which is a timing one clock period elapsed after tx, CK2 falls and becomes "L", and the electric potential at netBm also is returned back to "H". However, since Trb of SCm remains turned ON, CK2 is continuously outputted via Qom. According to the configuration, Gm is inactivated from "H" to "L", and this state "L" is maintained.

[0176] At tz, which is a timing one clock period elapsed after ty, CK2 remains at "L". However, since the clear signal CLR is activated and becomes "H", Trc of SCm turns ON, which connects netBm to Vss. This causes the electric potential of netBm to change from "H" to "L". As a result, Trb of SCm is turned OFF, and CK2 is no longer outputted via Qom.

[0177] In Fig. 28, the clear signal CLR is activated at tz (one clock period elapsed after the fall of Gm). However, the present invention is not limited to this example. For instance, the clear signal CLR can be activated during ty to tz (ty exclusive). Note that the clear signal CLR is to be not activated at ty, since that would cause Gm to maintain the "H" (active) state.

[0178] As described above, in the shift register 110a, gate on-pulse signals Gi outputted from respective shift circuits Sci (i = 1 to m) are made successively active each for a respective certain period of time, and pulses P1 to Pm are successively outputted from respective shift circuits in order of ordinal number, from a first stage shift circuit SC1 until an end stage shift circuit SCm. The end stage (unit circuit SCm) is reset by use of the clear signal; this makes it possible to omit a dummy stage (dummy shift circuit) that is provided in the conventional technique, thereby allowing reduction of circuit area.

[0179] The shift register 110a illustrated in Fig. 27 may also be configured as like a shift register 110b illustrated in Fig. 29. In addition to the configuration of the shift register 110a, the shift register 110b includes an N-channel low-potential supplying transistor Tre in the end stage shift circuit SCm. The transistor Tre has its source terminal be connected to the lower-potential-side power supply, its drain terminal be connected to the node Qom, and its gate terminal be connected to the node CLm.

[0180] According to the configuration of the shift register 110b, activation of the clear signal CLR causes Gm to fall. Therefore, at ty, the clear signal CLR is activated by synchronizing with the fall (inactivation) of Gm, as illustrated in Fig. 30.

[0181] Moreover, it is also possible to configure the shift register 110a in Fig. 27 as like a shift register 110c illustrated in Fig. 31. In addition to the configuration of the shift register 110a, the shift register 110c includes, in each of the shift circuits Sci (i = 1 to m-1), an N-channel low-potential supplying transistor Tre. The transistor Tre has its source terminal be connected to the lower-potential-side power supply, its drain terminal be connected to the node Qoi, and its gate terminal be connected to the node Qbi.

[0182] The following description explains an operation of the shift register 110c illustrated in Fig. 31. Fig. 32 is a timing chart illustrating waveforms of the vertical sync signal VSYNC, gate start pulse signal GSP, first clock signal CK1, second clock signal CK2, gate on-pulse signals Gi (i = 1 to m), and clear signal (CLR). Note that the first clock signal CK1 and the second clock signal CK2 both include, in one cycle, one clock period of a "H" (active) period and one clock period of a "L" (inactive) period; upon fall of one of the CK1 and CK2, the other one of the CK1 and CK2 synchronously rises.

[0183] First, at t0 of Fig. 32, electric potential of Qf1 rises due to activation of GSP. This turns Tra of SC1 ON, thereby causing electric potential of netB1 to change from "L" to "H". As a result, Trb of SIC1 also turns ON, thereby allowing CK1 to be outputted via Qo1. Namely, the G1 remains as "L".

[0184] At t1, which is a timing one clock period elapsed after t0, GSP falls (is inactivated) and becomes "L". However, the electric potential of netB1 does not fall by the capacitor C of SC1, and Trb of SC1 also remains turned ON. Namely, G1 is also activated by the rise of CK1, and G1 becomes "H". At this time, the electric potential of netB1 rises to an electric potential higher than "H", by the capacitor C. Moreover, the activation of G1 causes the electric potential of Qf2 to rise; consequently, Tra of SC2 turns ON, thereby causing the electric potential of netB2 to change from "L" to "H". As a result, Trb of SC2 also turns ON, thereby allowing CK2 to be outputted via Qo2, and G2 is maintained as "L".

[0185] At t2, which is a timing one clock period elapsed after t1, CK2 rises, thereby causing G2 to be activated and become "H". At this time, the electric potential of netB2 rises to an electric potential higher than "H", by the capacitor C. On the other hand, the activation of G2

causes electric potential of Qb1 to rise; consequently, Trd of SC1 turns ON, which connects netB1 to Vss, thereby causing the electric potential at netB1 to change from "H" to "L". As a result, Trb of SC1 turns OFF, and CK1 is no longer outputted via Qo1. Moreover, the activation of the G2 causes electric potential of Qb1 to rise; consequently, Tre of SC1 turns ON, which connects Qo1 to Vss, thereby causing the electric potential at Qo1 to change from "H" to "L". Namely, G1 is inactivated from "H" to "L", and this state "L" is maintained. Note that, even if G1 is inactivated and becomes "L", the electric potential of netB2 is maintained by the capacitor C of SC2, and Trb of SC2 remains turned ON. Moreover, upon rise of the electric potential of Qf3 due to the activation of G2, Tra of SC3 turns ON, and the electric potential of netB3 changes from "L" to "H". This also turns Trb of SC3 ON, thereby allowing CK1 to be outputted via Qo3. Namely, G3 remains as "L".

[0186] At t3, which is a timing one clock period elapsed after t2, CK1 rises, and thus G3 is also activated and becomes "H". On the other hand, the activation of G3 causes the electric potential of Qb2 to rise; consequently, Trd of SC2 turns ON, which connects netB2 to Vss, thereby causing the electric potential of netB2 to change from "H" to "L". As a result, Trb of SC2 turns OFF and CK2 is no longer outputted via Qo2. Moreover, upon rise of the electric potential of Qb2 due to the activation of G3, Tre of SC2 turns ON, which connects Qo2 to Vss, thereby causing the electric potential of Qo2 to change from "H" to "L". Namely, G2 is inactivated from "H" to "L", and this state "L" is maintained.

[0187] Furthermore, at tx, CK2 rises, and thus Gm is also activated and becomes "H". At this time, the electric potential of netBm rises to an electric potential higher than "H" by the capacitor C.

[0188] At ty, which is a timing one clock period elapsed after tx, CK2 falls and becomes "L", and the electric potential of netBm also returns back to "H". However, since Trb of SCm remains turned ON, CK2 is continuously outputted via Qom. Namely, Gm is inactivated from "H" to "L", and this state "L" is maintained.

[0189] At tz, which is a timing one clock period elapsed after ty, the clear signal CLR is activated and becomes "H". This causes Trc of SCm to be turned ON, which connects netBm to Vss; and the electric potential of the netBm is changed from "H" to "L". As a result, Trb of SCm turns OFF, and CK2 is no longer outputted via Qom.

[0190] Note that in Fig. 32, the clear signal CLR is activated at tz (one clock period elapsed after the fall of Gm). However, the present invention is not limited to this. For example, the clear signal CLR can be activated during ty to tz (ty exclusive). Note that the clear signal CLR is to be not activated at ty, since that would cause Gm to maintain the "H" (active) state.

[0191] As described, in the shift register 110b, gate on-pulse signals Gi outputted from respective shift circuits Sci (i = 1 to m) are made successively active each for a respective certain period of time, and pulses are successively outputted from respective shift circuits in the order of ordinal number, from the shift circuit SC1 in the first stage until the shift circuit SCm of the end stage.

[0192] The shift register 110c illustrated in Fig. 31 may be configured as like a shift register 110d illustrated in Fig. 33. The shift register 110d, in addition to the configuration of the shift register 110c, includes an N-channel transistor Tre in the shift circuit SCm, which shift circuit is a shift circuit provided in the end stage. The transistor Tre has its source terminal be connected to the lower-potential-side power supply, its drain terminal be connected to the node Qom, and its gate terminal be connected to the node CLm.

[0193] According to the configuration of the shift register 110d, it is possible to cause a fall in Gm by activating the clear signal CLR. Hence, as illustrated in Fig. 34, at ty, it is possible to activate the clear signal CLR by synchronizing with a fall (inactivation) of Gm.

[0194] The shift register 110a illustrated in Fig. 27 may also be configured as like a shift register 110e illustrated in Fig. 35. The shift register 110e, in addition to the configuration of the shift register 110a, includes an N-channel transistor Tre in each of the shift circuits SCi (i = 1 to m). The transistor Tre has its source terminal be connected to the lower-potential-side power supply, its drain terminal be connected to the node Qoi, and its gate terminal be connected to the first clock line CKL1 or the second clock line CKL2. If the i is an odd number, the gate terminal of the transistor Tre in the shift circuit SCi is connected to the second clock line CKL2, and if the i is an even number, the gate terminal of the transistor Tre in the shift circuit SCi is connected to the first clock line CKL1.

[0195] The following description explains operations of the shift register 110e illustrated in Fig. 35. Fig. 36 is a timing chart illustrating waveforms of the vertical sync signal VSYNC, the gate start pulse signal GSP, the first clock signal CK1, the second clock signal CK2, the gate on-pulse signals Gi (i = 1 to m), and the clear signal (CLR). Each of the first clock signal CK1 and second clock signal CK2 includes, in one cycle, one clock period of a "H" (active) period and one clock period of a "L" (inactive) period; upon fall of one of CK1 and CK2, the other one of CK1 and CK2 synchronously rises.

[0196] First, at t0 in Fig. 36, activation of GSP causes a rise in electric potential of Qf1. This rise in the electric potential turns Tra of SC1 ON, thereby causing electric potential of netB1 to change from "L" to "H". As a result, Trb of SC1 turns ON, and accordingly CK1 is outputted via Qo1.

[0197] At t1, which is a timing one clock period elapsed after t0, GSP falls (is inactivated) and becomes "L". However, the electric potential of netB1 remains high by the capacitor C of SC1, and Trb of SC1 also remains turned ON. As a result, rise of CK1 also causes G1 to activate, and thus G1 becomes "H". At this point, the electric potential of netB1 rises to an electric potential higher than "H" by the capacitor C. Moreover, the activation of G1

causes rise of the electric potential of Qf2. This turns Tra of SC2 ON, which causes the electric potential of netB2 to change from "L" to "H". As a result, Trb of SC2 also is turned ON, and CK2 is outputted via Qo2. According to the configuration, G2 remains at "L".

[0198] At t2, which is a timing one clock period elapsed after t1, CK2 rises, thereby causing G2 to also be activated and become "H". At this point, the electric potential of netB2 rises to an electric potential higher than "H", by the capacitor C. Moreover, the activation of G2 causes the electric potential of Qb1 to rise; consequently, Trd of SC1 turns ON, which connects netB1 to Vss, thereby causing the electric potential of netB1 to change from "H" to "L". As a result, Trb of SC1 turns OFF, and CK1 is no longer outputted via Qo1. Moreover, at t2, CK2 rises; consequently, Tre of SC1 is turned ON, which connects Qo1 to Vss, thereby causing electric potential of the Qo1 to change from "H" to "L". As a result, G1 is inactivated from "H" to "L", and this state "L" is maintained. Note that even if the G1 is inactivated and becomes "L", the electric potential of netB2 is maintained by the capacitor C of SC2, and Trb of SC2 remains turned ON. Moreover, the activation of G2 causes the electric potential of Qf3 to rise; consequently, Tra of SC3 turns ON, thereby causing the electric potential of netB3 to change from "L" to "H". As a result, Trb of SC3 also is turned ON, and CK1 is outputted via Qo3. According to the configuration, G3 remains at "L".

[0199] At t3, which is a timing one clock period elapsed after t2, CK1 rises, thereby causing G3 to be activated and become "H". Moreover, the activation of G3 causes electric potential of Qb2 to rise; consequently, Trd of SC2 is turned ON, which connects netB2 to Vss, thereby causing electric potential of netB2 to change from "H" to "L". As a result, Trb of SC2 turns OFF, and CK2 is no longer outputted to Qo2. Moreover, at t3, CK1 rises; consequently, Tre of SC2 is turned ON, which connects Qo2 to Vss, thereby causing electric potential of Qo2 to change from "H" to "L". As a result, G2 is inactivated from "H" to "L", and this state "L" is maintained.

[0200] Note that, in the shift register 110e, CK2 is "H" during a period between t4 to t5 and a period between t6 to t7. As a result, Tre of SC1 is turned ON, which connects Qo1 to Vss, thereby causing G1 to again fall to "L" (i.e., be drawn to "L"). Similarly, during a period between t5 to t6, CK1 is' "H"; as a result, Tre of SC2 is turned ON, which connects Qo2 to Vss, thereby causing G2 to again fall to "L" (be drawn to "L").

[0201] Furthermore, at tx, CK2 rises; as a result, Gm also is activated and becomes "H". At this point, the electric potential of netBm rises to an electric potential higher than "H", by the capacitor C.

[0202] At ty, which is a timing one clock period elapsed after tx, the clear signal CLR is activated and becomes "H". As a result, Trc of SCm is turned ON, which connects netBm to Vss, thereby causing the electric potential of netBm to fall to "L". Consequently, Trb of SCm is turned OFF, and CK2 is no longer outputted via Qom. Further, CK1 rises at ty, therefore Tre of SCm is turned ON, which connects Qom to Vss. As a result, Gm is inactivated and becomes "L".

[0203] In Fig. 36, the clear signal CLR is activated at ty; however, it is not limited to this. For example, the clear signal CLR may be activated during a period between ty and tz (ty and tz inclusive).

[0204] As described above, in the shift register 110e, the gate on-pulse signals Gi outputted from the shift circuits SCi (i = 1 to m), respectively, are made successively active each for a respectively certain period of time, and pulses thus generated are outputted from the respective shift circuits in order of ordinal number, from the shift circuit SC1 in the first stage until the shift circuit SCm in the end stage. The end stage (unit circuit SCm) is reset with use of the clear signal; this makes it possible to omit the dummy stage (dummy shift circuit) provided in the conventional technique, thereby allowing reduction in circuit area.

Embodiment 4

[0205] Embodiment 4 is as described below, with reference to Figs. 37 to 39. Fig. 37 illustrates a configuration of a liquid crystal panel in accordance with the present embodiment. As illustrated in Fig. 37, the present liquid crystal panel provides a shift register 110f on a left end of the panel and a shift register 110g on a right end of the panel. The shift register 110f includes a plurality of shift circuits SCi (i = 1, 3, 5, ... 2n+1) connected in stages, and shift circuits SCi (i = 2, 4, 6, ... 2n) connected in stages. Each of the shift circuits SCi (i = 1, 2, 3, ... 2n-2) includes input nodes Qfi, Qbi, CKAi, and CKBi, and an output node Qoi. The shift circuit SC(2n-1) includes input nodes Qf(2n-1), CKA(2n-1), CKB(2n-1), and CL(2n-1), and an output node Qo (2n-1). Moreover, the shift circuit SC(2n) includes input nodes Qf(2n), CKA(2n), CKB(2n), and CL(2n), and an output node Qo(2n).

[0206] In the embodiment, the shift circuit SC1 has its node Qf1 be connected to a GSP1 outputting terminal RO1 of a level shifter; has its node Qb1 be connected to the node Qo3 of the shift circuit SC3, has its node CKA1 be connected to a first clock line CKL1 to which a first clock signal is supplied, and has its node CKB1 be connected to a third clock line CKL3 to which a third clock signal is supplied. Further, a gate on-pulse signal (signal line selection signal) G1 is outputted via its node Qo1.

[0207] The shift circuit SC2 has its node Qf2 be connected to a GSP2 outputting terminal RO2 of the level shifter, has its node Qb2 be connected to the node Qo4 of the shift circuit SC4, has its node CKA2 be connected to a second clock line CKL2 to which a second clock signal is supplied, and has its node CKB2 be connected to a fourth clock line CKL4 to which the fourth clock signal is supplied. Further, a gate on-pulse signal (signal line selection signal) G2 is outputted via its node Qo2.

[0208] Moreover, each of the shift circuits SCi (i = 3 to 2n-2) has its node Qfi be connected to the node Qo (i-2)

of the shift circuit SC (i-2), and its node Qbi be connected to the node Qo (i+2) of the shift circuit SC (i+2). Moreover, in a case where i is a multiple of 4 + 1, its node CKAi is connected to the first clock line CKL1 and its node CKBi is connected to the third clock line CKL3; in a case where i is a multiple of 4 + 2, its node CKAi is connected to the second clock line CKL2 and its node CKBi is connected to the fourth clock line CKL4; in a case where i is a multiple of 4 + 3, its node CKAi is co-nnected to the third clock line CKL1 and its node CKBi is connected to the first clock line CKL3; and in a case where i is a multiple of 4, its node CKAi is connected to the fourth clock line CKL4 and its node CKBi is connected to the second clock line CKL2. Further, a gate on-pulse signal (signal line selection signal) Gi is outputted from the node Qoi.

[0209] The shift circuit SC(2n-1) has its node Qf(2n-1) be connected to the node Qo(2n-3) of the shift circuit SC (2n-3), has its node CKA(2n-1) be connected to the third clock line CKL3, has its node CKB(2n-1) connected to the first clock line CKL1, and has its node CL(2n-1) connected to the first clear line CLRL1. Further, a gate on-pulse signal (signal line selection signal) G(2n-1) is outputted from its node Qo(2n-1).

[0210] Moreover, the shift circuit SC(2n) has its node Qf(2n) be connected to the node Qo(2n-2) of the shift circuit SC(2n-2), has its node CKA(2n) be connected to the fourth clock line CKL4, has its node CKB(2n) be connected to the second clock line CKL2, and has its node CL(2n) be connected to the second clear line CLRL2. Further, a gate on-pulse signal (signal line selection signal) G(2n) is outputted from its node Qo(2n).

[0211] Specifically illustrated in (a) of Fig. 38 is a circuit diagram of a configuration employed into each of SCi (i = 1 to 2n-2). As illustrated in (a) of Fig. 38, each of SCi (i = 1 to 2n-2) includes a set transistor Tra, an output transistor Trb, a reset transistor Trd, a low-potential supplying transistor Tre, and a capacitor C. Note that each of the transistors is an N-channel transistor.

[0212] In the embodiment, Trb has its source terminal be connected to a first electrode of the capacitor C. Tra has its gate terminal (control terminal) and its drain terminal be connected to each other, and further has its source terminal be connected to (i) a gate terminal of the Trb and (ii) a second electrode of the capacitor C. Moreover, Trd has its drain terminal be connected to the gate terminal of the Trb, and further has its source terminal be connected to a lower-potential-side power supply Vss. Moreover, Tre has its drain terminal be connected to the source terminal of the Trb, and further has its source terminal be connected to the lower-potential-side power supply Vss. Moreover, the gate terminal of Tra is connected to the node Qfi, Trb has its drain terminal be connected to the node CKAi, Tre has its gate terminal be connected to the node CKBi, Trc has its gate terminal be connected to the node CLi, Trd has its gate terminal be connected to the node Qbi, and the source terminal of the Trb is connected to the node Qoi. Note that a connection point of the source terminal of the Tra, the second electrode of the capacitor C, and the gate terminal of the Trb is defined as a node netBi.

[0213] Moreover, specifically illustrated in (b) of Fig. 38 is a circuit diagram of a configuration of SCj (j = (2n-1) or 2n). As illustrated in (b) of Fig. 38, SCj includes a set transistor Tra, an output transistor Trb, a clear transistor Trc provided for resetting the end stage, a low-potential supplying transistor Tre, and a capacitor C. Note that each of the transistors is an N-channel transistor.

[0214] In the embodiment, Trb has its source terminal be connected to a first electrode of the capacitor C. Tra has its gate terminal (control terminal) and its drain terminal be connected to each other, and further has its source terminal be connected to (i) a gate terminal of Trb and (ii) a second electrode of the capacitor C. Moreover, Trc has its drain terminal be connected to the gate terminal of Trb, and further has its source terminal be connected to a lower-potential-side power supply Vss. Moreover, Tre has its drain terminal connected to the source terminal of the Trb, and further has its source terminal be connected to the lower-potential-side power supply Vss. Furthermore, the gate terminal of the Tra is connected to the node Qfj, Trb has its drain terminal be connected to the node CKAj, Tre has its gate terminal connected to the node CKBj, Trc has its gate terminal be connected to the node CLj, and the source terminal of the Trb is connected to the node Qoj. Moreover, a connection point of the source terminal of the Tra, the second electrode of the capacitor C and the gate terminal of the Trb is defined as a node netBj.

[0215] The nodes (Qfi, Qbi, CKAi, CKBi, Qoi) of each of the shift circuits SCi (i = 1 to 2n-2) and the nodes (Qfj, CKAj, CKBj, CLj, Qoj) of the shift circuit SCj (j = (2n-1) or 2n) are connected to respective destinations as illustrated in Fig. 37.

[0216] The following describes operations of the shift registers 110f and 110g illustrated in Fig. 37. Fig. 39 is a timing chart showing waveforms of the vertical sync signal VSYNC, the gate start pulse signals GSP1 and GSP2, the first clock signal CK1, the second clock signal CK2, the third clock signal CK3, the fourth clock signal CK4, the gate on-pulse signals Gi (i = 1 to 2n), the first clear signal CLR1, and the second clear signal CLR2. Note that each of CK1 to CK4 includes, in one cycle, one clock period of a "H" period and three clock periods of a "L" period; synchronizing with a fall of CK1, CK2 rises; synchronizing with a fall of CK2, CK3 rises; synchronizing with a fall of CK3, CK4 rises; and synchronizing with a fall of CK4, CK1 rises. Moreover, GSP2 rises one clock period elapsed after the rise of GSP1.

[0217] First, at t0 in Fig. 39, GSP1 is activated, which causes electric potential of Qf1 to rise. As a result, Tra of SC1 is turned ON, thereby causing electric potential of netB1 to change from "L" to "H". Consequently, Trb of SC1 also is turned on, and CK1 is outputted via Qo1. According to the configuration, G1 remains at "L".

[0218] At t1, which is a timing one clock period elapsed after t0, GSP1 falls and becomes "L", however the electric

potential of netB1 is maintained as "H" by the capacitor C of SC1, and thus Trb of SC1 remains turned ON. Moreover, at t1, GSP2 is activated, which causes electric potential of Qf2 to rise. As a result, Tra of SC2 is turned ON, thereby causing electric potential of netB2 to change from "L" to "H". Consequently, Trb of SC2 also is turned ON, and CK2 is outputted via Qo2. According to the configuration, G2 remains at "L".

[0219] At t2, which is a timing one clock period elapsed after t1, CK1 rises, thereby causing G1 to be activated and become "H". At this point, electric potential of netB1 rises to an electric potential higher than "H" by the capacitor C. Moreover, the activation of G1 causes electric potential of Qf3 to rise; consequently, Tra of SC3 is turned ON, thereby causing the electric potential of netB3 to change from "L" to "H". As a result, Trb of SC3 also is turned ON, and CK3 is outputted via Qo3. According to the configuration, G3 remains at "L". Moreover, at t2, GSP2 falls and becomes "L", however the electric potential of netB2 is maintained at "H" by the capacitor C of SC2, and Trb of SC2 also remains turned ON.

[0220] At t3, which is a timing one clock period elapsed after t2, CK1 falls and becomes "L", and the electric potential of netB1 also is returned back to "H". However, since Trb of SC1 remains turned ON, CK1 is continuously outputted via Qo1. As a result, G1 is inactivated and changes from "H" to "L", and this state "L" is maintained. Note that even if G1 is inactivated and becomes "L", the electric potential of netB3 is maintained at "H" by the capacitor C of SC3, and thus Trb of SC3 remains turned ON. Moreover, at t3, CK2 rises; consequently, G2 is also activated and becomes "H". At this point, the electric potential of netB2 rises to an electric potential higher than "H", by the capacitor C. Moreover, at t3, the activation of G2 causes electric potential of Qf4 to rise; consequently, Tra of SC4 is turned ON, thereby causing the electric potential of netB4 to change from "L" to "H". As a result, the Trb of SC4 also is turned ON, and accordingly CK4 is outputted via Qo4. According to the configuration, G4 remains at "L".

[0221] At t4, which is a timing one clock period elapsed after t3, CK3 rises, thereby causing G3 to be activated and become "H". At this point, the electric potential of netB3 rises to an electric potential higher than "H" by the capacitor C. Moreover, the activation of G3 causes electric potential at Qb1 to rise; consequently, Trd of SC1 is turned ON, which connects netB1 to Vss, thereby causing the electric potential of netB1 to change from "H" to "L". As a result, Trb of SC1 is turned OFF, and CK1 is no longer outputted via Qo1. Moreover, at t4, CK3 rises; consequently, Tre of SC1 is turned ON, which connects Qo1 to Vss, thereby causing the electric potential of the Qo1 to fall to "L" (G1 is drawn to "L"). Moreover, at t4, CK2 falls and becomes "L", and the electric potential of netB2 is returned back to "H". However, since Trb of SC2 remains turned ON, CK2 is continuously outputted via Qo2. Therefore, G2 is inactivated from "H" to "L", and this state "L" is maintained.

[0222] At t5, which is a timing one clock period elapsed after t4, CK4 rises, thereby causing G4 to be activated and become "H". At this point, electric potential of netB4 rises to an electric potential higher than "H", by the capacitor C. On the other hand, the activation of G4 causes electric potential of Qb2 to rise; consequently, Trd of SC2 is turned ON, which connects netB2 to Vss, thereby causing the electric potential of netB2 to change from "H" to "L". As a result, Trb of SC2 is turned OFF, and CK2 is no longer outputted via Qo2. Moreover, at t5, CK4 rises. This causes Tre of SC2 to turn ON, which connects Qo2 to Vss, thereby causing the electric potential at Qo2 to fall to "L" (G2 is drawn to "L"). At t5, CK3 falls and becomes "L", and the electric potential of netB3 also is returned to "H". However, since Trb of SC3 remains turned ON, CK3 is continuously outputted via Qo3. As a result, G3 is inactivated from "H" to "L", and this state "L" is maintained.

[0223] At t6, which is a timing one clock period elapsed after t5, CK1 rises, thereby causing G5 to be activated and become "H". At this point, the electric potential of netB5 rises to an electric potential higher than "H" by the capacitor C. Moreover, the activation of G5 causes electric potential of Qb3 to rise; consequently, Trd of SC3 is turned ON, which connects netB3 to Vss, thereby causing the electric potential of netB3 to change from "H" to "L". As a result, Trb of SC3 turns OFF and CK3 is no longer outputted via Qo3. Moreover, at t6, CK1 rises; as a result, Tre of SC3 is turned ON, which connects Qo3 to Vss, thereby causing the electric potential of Qo3 to fall to "L" (G3 is drawn to "L"). Moreover, at t6, CK4 falls and becomes "L", and electric potential of netB4 is also returned back to "H". However, since Trb of SC4 remains turned ON, CK4 is continuously outputted via Qo4. As a result, G4 is inactivated from "H" to "L", and this state "L" is maintained.

[0224] At t7, which is a timing one clock period elapsed after t6, CK2 rises, thereby causing G6 to also be activated and become "H". At this point, electric potential of netB6 rises to an electric potential higher than "H" by the capacitor C. Moreover, the activation of G6 causes electric potential of Qb4 to rise; consequently, Trd of SC4 is turned ON, which connects netB4 to Vss, thereby causing the electric potential of netB4 to change from "H" to "L". As a result, Trb of SC4 is turned OFF, and CK4 is no longer outputted via Qo4. Moreover, at t7, CK2 rises, thereby causing Tre of SC4 to be turned ON, which connects Qo4 to Vss. As a result, the electric potential of Qo4 falls to "L" (G4 is drawn to "L").

[0225] Furthermore, at tx, CK3 rises, thereby causing G(2n-1) to also be activated and become "H". At this point, the electric potential of the netB(2n-1) rises to an electric potential higher than "H", by the capacitor C.

[0226] Moreover, at ty, which is a timing one clock period elapsed after tx, CK4 rises, thereby causing G(2n) to also be activated and become "H". At this point, the electric potential of netB(2n) rises to an electric potential higher than "H" by the capacitor C. Moreover, at ty, CK3

falls and becomes "L", and the electric potential of netB (2n-1) is also returned back to "H". However, since Trb of SC(2n-1) remains turned ON, CK3 is continuously outputted via Qo(2n-1). As a result, G(2n-1) is inactivated from "H" to "L", and this state "L" is maintained.

[0227] At tz, which is a timing one clock period elapsed after ty, a first clear signal CLR1 is activated and becomes "H"; consequently, Trc of SC(2n-1) is turned ON, which connects netB(2n-1) to Vss, thereby causing the electric potential of netB(2n-1) to change from "H" to "L". As a result, Trb of SC(2n-1) is turned OFF, and CK3 is no longer outputted via Qo(2n-1). Furthermore, CK1 rises; consequently, Tre of SC(2n-1) is turned ON, which connects Qo(2n-1) to Vss, thereby causing the electric potential of Qo(2n-1) to fall to "L" (G(2n-1) is drawn to "L"). Moreover, at tz, CK4 falls and becomes "L", and the electric potential of netB(2n) is also returned back to "H". However, since Trb of SC(2n) remains turned ON, CK4 is continuously outputted via Qo(2n). As a result, G(2n) is inactivated from "H" to "L", and this state "L" is maintained.

[0228] At tw, which is a timing one clock period elapsed after ty, the second clear signal CLR2 is activated and becomes "H"; consequently, Trc of SC(2n) is turned ON, which connects netB(2n) to Vss, thereby causing electric potential to change from "H" to "L". As a result, Trb of SC (2n) is turned OFF, and CK4 is no longer outputted via Qo(2n). Furthermore, CK2 rises, therefore Tre of SC(2n) is turned ON, which connects Qo(2n) to Vss, thereby causing electric potential of Qo(2n) to fall to "L" (G(2n) is drawn to "L").

[0229] As described above, in a case where the sync signal includes no anomalousness, the gate on-pulse signals Gi outputted from the respective shift circuits SCi (i = 1, 3, 5, ... and 2n-1) are successively made active each for a respective certain period of time in the shift register 110f, and accordingly the pulses P1, P3, ... P(2n-1) are outputted successively from respective shift circuits in the order of odd ordinal number, from the shift circuit SC1 in the first stage until the shift circuit SC(2n-1) in the end stage. Moreover, the gate on-pulse signals Gi outputted from the respective shift circuits SCi (i = 2, 4, 6, ... 2n) are successively made active each for a respective certain period of time in the shift register 110g, and pulses P1, P2, ... P(2n) are outputted successively from the respective shift circuits in the order of even shift circuits, from the shift circuit SC2 in the first stage until the shift circuit SC(2n) in the end stage. Thereafter, in the end stage (unit circuit SC(2n-1) and (2n)), the shift registers 110f and 110g are reset with use of the clear signal. This makes it possible to omit a dummy stage (dummy shift circuit) which is provided in a conventional technique, thereby allowing reduction in the circuit area.

[0230] As illustrated in Fig. 37, with the shift registers 110f and 110g, GSP1 and GSP2 can be a common gate start pulse signal. In this case, for example in Fig. 39, GSP1 and GSP2 are made "H" (active) at t0. Moreover, CLR1 and CLR2 can be a common clear signal. In this case, for example in Fig. 39, CLR1 and CLR2 are made "H" (active) at tw.

[0231] The invention being thus described, it will be obvious that the same way may be varied in many ways. Such variations are not to be regarded as a departure from the spirit and scope of the invention, and all such modifications as would be obvious to one skilled in the art are intended to be included within the scope of the following claims.

Industrial Applicability

[0232] The present display panel driving circuit and shift register are suitably used in a liquid crystal display device.

Claims

1. A display panel drive circuit receiving a sync signal from outside, the display panel drive circuit including a shift register constructed of unit circuits connected in stages, the unit circuits outputting signal line selection signals, respectively, each of the signal line selection signals being made active for a respective certain period of time to form a respective pulse, the pulses being outputted successively from respective unit circuits in order of ordinal number starting from a first stage until an end stage,
each of the unit circuits receiving (i) a clock signal, (ii) a start pulse signal or a signal line selection signal generated in a stage different from its own stage, and (iii) a clear signal,
the clear signal being made active in a case where anomalousness is included in at least the sync signal, and no pulse is outputted from the shift register after the clear signal is made active, until a subsequent vertical scanning period starts.

2. The display panel drive circuit according to claim 1, wherein:

   the clock signal, the start pulse signal, and the clear signal are generated based on the sync signal.

3. The display panel drive circuit according to claim 1 or 2, wherein:

   the sync signal includes at least one of a vertical sync signal, a horizontal sync signal, and a data enable signal.

4. The display panel drive circuit according to any one of claims 1 to 3, wherein:

   regardless of whether or not anomalousness is included in the sync signal, the clear signal is

made active after the end stage outputs its respective pulse, so that the signal line selection signal outputted from the end stage remains inactive.

5. The display panel drive circuit according to any one of claims 1 to 4, wherein:

each of the unit circuits except for that in the end stage includes a set transistor, an output transistor, a reset transistor, a clear transistor, and a capacitor,
the set transistor, output transistor, reset transistor, and clear transistor each having a control terminal, a first conductive terminal, and a second conductive terminal, and the capacitor having a first electrode and a second electrode,
the set transistor receiving, via its control terminal, the start pulse signal or a signal line selection signal outputted from a stage previous to its own stage,
the reset transistor receiving, via its control terminal, a signal line selection signal outputted from a stage subsequent to its own stage,
the clear transistor receiving the clear signal via its control terminal,
the output transistor receiving the clock signal via its first conductive terminal,
the second conductive terminal of the output transistor being connected to the first electrode of the capacitor, the control terminal of the set transistor and the first conductive terminal of the set transistor being connected to each other, and the second conductive terminal of the set transistor being connected to (i) the control terminal of the output transistor and (ii) the second electrode of the capacitor,
the first conductive terminal of the reset transistor being connected to the control terminal of the output transistor, and the second conductive terminal of the reset transistor being connected to a constant potential source,
the first conductive terminal of the clear transistor being connected to the control terminal of the output transistor, and the second conductive terminal of the clear transistor being connected to the constant potential source, and
the second conductive terminal of the output transistor serving as an output terminal of the respective unit circuit.

6. The display panel drive circuit according to claim 5, wherein:

each of the unit circuits except for that in the end stage further includes a potential supplying transistor, the potential supplying transistor having a control terminal, a first conductive terminal, and a second conductive terminal,
the first conductive terminal of the potential supplying transistor being connected to the second conductive terminal of the output transistor, and
the second conductive terminal of the potential supplying transistor being connected to the constant potential source,
the potential supplying transistor receiving, via its control terminal, a signal line selection signal outputted from a stage subsequent to its own stage.

7. The display panel drive circuit according to claim 5, wherein:

each of the unit circuits except for that in the end stage further includes a potential supplying transistor, the potential supplying transistor having a control terminal, a first conductive terminal, and a second conductive terminal,
the first conductive terminal of the potential supplying transistor being connected to the second conductive terminal of the output transistor, and
the second conductive terminal of the potential supplying transistor being connected to the constant potential source,
the potential supplying transistor receiving, via its control terminal, a clock signal different from the clock signal received via the first conductive terminal of the output transistor.

8. The display panel drive circuit according to claim 5, wherein:

the unit circuit in the end stage includes a set transistor, an output transistor, a clear transistor, and a capacitor,
the set transistor, output transistor, and clear transistor each having a control terminal, a first conductive terminal, and a second conductive terminal, and the capacitor having a first electrode and a second electrode,
the set transistor receiving, via its control terminal, a signal line selection signal outputted from a stage previous to its own stage,
the clear transistor receiving the clear signal via its control terminal, and
the output transistor receiving the clock signal via its first conductive terminal,
the second conductive terminal of the output transistor being connected to the first electrode of the capacitor, the control terminal of the set transistor and the first conductive terminal of the set transistor being connected to each other, and the second conductive terminal of the set transistor being connected to (i) the control terminal of the output transistor and (ii) the second electrode of the capacitor,

the first conductive terminal of the clear transistor being connected to the control terminal of the output transistor, and the second conductive terminal of the clear transistor being connected to the constant potential source, and
the second conductive terminal of the output transistor serving as an output terminal of the unit circuit in the end stage.

9. The display panel drive circuit according to claim 8, wherein:

the unit circuit in the end stage further includes a potential supplying transistor, the potential supplying transistor having a control terminal, a first conductive terminal, and a second conductive terminal,
the potential supplying transistor receiving the clear signal via its control terminal,
the first conductive terminal of the potential supplying transistor being connected to the second conductive terminal of the output transistor, and
the second conductive terminal of the potential supplying transistor being connected to the constant potential source.

10. The display panel drive circuit according to claim 5, wherein:

the clear signal is made active at a timing in which the signal line selection signal received from a respective stage is made inactive, or is made active while the signal line selection signal received from the respective stage is inactive.

11. The display panel drive circuit according to claim 5, wherein:

a plurality of clock signals each having phases different from each other are inputted into the shift register, the plurality of clock signals being received by the output transistors of different unit circuits, respectively.

12. The display panel drive circuit according to claim 11, wherein:

each of the plurality of clock signals have an inactive period that partially coincides with an inactive period of another of the plurality of clock signals.

13. The display panel drive circuit according to claim 11, wherein:

the plurality of clock signals include two clock signals which are shifted in phase by half a cycle.

14. The display panel drive circuit according to claim 11, wherein:

at least one of the plurality of clock signals is made inactive while the clear signal is made active.

15. The display panel drive circuit according to claim 5, wherein:

each of the set transistor, the output transistor, the reset transistor, and the clear transistor is an N-channel transistor.

16. The display panel drive circuit according to claim 6 or 7, wherein:

each of the set transistor, the output transistor, the reset transistor, the clear transistor, and the potential supplying transistor is an N-channel transistor.

17. The display panel drive circuit according to claim 15, wherein:

the first conductive terminal of each of the transistors is a drain terminal, and the second conductive terminal of each of the transistors is a source terminal.

18. The display panel drive circuit according to claim 5, wherein:

the first conductive terminal of each of the transistors is a source terminal, and the second conductive terminal of each of the transistors is a drain terminal.

19. The display panel drive circuit according to claim 1, further comprising:

a timing controller for generating the clock signal, the start pulse signal, and the clear signal, with use of the sync signal.

20. The display panel drive circuit according to claim 1, further comprising:

an anomalousness detection circuit for detecting anomalousness of the sync signal,
the clear signal being generated based on a result of the detection.

21. A liquid crystal display device comprising:

a display panel drive circuit recited in claim 1; and
a liquid crystal panel.

22. The liquid crystal display device according to claim 21, wherein:

the shift register is provided monolithically in the liquid crystal panel.

23. The liquid crystal display device according to claim 22, wherein:

the liquid crystal panel is formed by use of amorphous silicone.

24. The liquid crystal display device according to claim 22, wherein:

the liquid crystal panel is formed by use of polysilicon.

25. A shift register, provided in a display panel drive circuit that receives a sync signal, the shift register constructed of unit circuits connected in stages, the unit circuits generating signal line selection signals, respectively, each of the signal line selection signals being made active for a respective certain period of time to form a respective pulse, the pulses being outputted successively from respective unit circuits in order of ordinal number starting from a first stage until an end stage,
each of the unit circuits receiving (i) a clock signal, (ii) a start pulse signal or a signal line selection signal generated by a stage different from its own stage, and (iii) a clear signal,
the clear signal being made active in a case where anomalousness is included in at least the sync signal, and no pulse is outputted after the clear signal is made active, until a subsequent vertical scanning period starts.

26. A liquid crystal panel, wherein a shift register recited in claim 25 is monolithically provided.

27. A method for driving a display device, the display device receiving a sync signal from outside and including a shift register constructed of unit circuits connected in stages, the unit circuits generating signal line selection signals, respectively, each of the signal line selection signals being made active for a respective certain period of time to form a respective pulse, the shift register outputting the pulses successively from respective unit circuits in order of ordinal number starting from a first stage until an end stage, the method comprising:

inputting, to each of the unit circuits, (i) a clock signal, (ii) a start pulse signal or a signal line selection signal generated in a stage different from its own stage, and (iii) a clear signal; and
activating the clear signal in a case where anomalousness is included in at least the sync signal, so that no pulse is outputted from the shift register after the clear signal is made active, until a subsequent vertical scanning period starts.

28. A display panel drive circuit including a shift register constructed of unit circuits connected in stages, the unit circuits outputting signal line selection signals, respectively, each of the signal line selection signals being made active for a respective certain period of time to form a respective pulse, the shift register outputting the pulses successively from respective unit circuits in order of ordinal number starting from a first stage until an end stage,
a unit circuit in the end stage receiving (i) a signal line selection signal generated in a stage different from its own stage, (ii) a clock signal, and (iii) a clear signal, and
the clear signal being made active after the end stage outputs its respective pulse, so that the signal line selection signal outputted from the end stage remains inactive.

29. The display panel drive circuit according to claim 28, wherein:

each of the unit circuits except for the unit circuit in the end stage includes a set transistor, an output transistor, a reset transistor, and a capacitor,
the set transistor, output transistor, and reset transistor each having a control terminal, a first conductive terminal, and a second conductive terminal, and the capacitor having a first electrode and a second electrode,
the set transistor receiving, via its control terminal, a start pulse signal or a signal line selection signal outputted from a stage previous to its own stage,
the reset transistor receiving, via its control terminal, a signal line selection signal outputted from a stage subsequent to its own stage, and
the output transistor receiving the clock signal via its first conductive terminal,
the second conductive terminal of the output transistor being connected to a first electrode of the capacitor, the control terminal of the set transistor and the first conductive terminal of the set transistor being connected to each other, and
the second conductive terminal of the set transistor being connected to (i) the control terminal of the output transistor and (ii) a second electrode of the capacitor,
the first conductive terminal of the reset transistor being connected to the control terminal of the output transistor, and the second conductive terminal of the reset transistor being connected to a constant potential source, and

the second conductive terminal of the output transistor serving as an output terminal of the respective unit circuit.

30. The display panel drive circuit according to claim 28, wherein:

the unit circuit in the end stage includes a set transistor, an output transistor, a clear transistor, and a capacitor,
the set transistor, output transistor, and clear transistor each having a control terminal, a first conductive terminal, and a second conductive terminal, and the capacitor having a first electrode and a second electrode,
the set transistor receiving, via its control terminal, a signal line selection signal outputted from a stage previous to its own stage,
the clear transistor receiving the clear signal via its control terminal, and
the output transistor receiving the clock signal via its first conductive terminal,
the second conductive terminal of the output transistor being connected to the first electrode of the capacitor, the control terminal of the set transistor and the first conductive terminal of the set transistor being connected to each other, and the second conductive terminal of the set transistor being connected to (i) the control terminal of the output transistor and (ii) the second electrode of the capacitor,
the first conductive terminal of the clear transistor being connected to the control terminal of the output transistor, and the second conductive terminal of the clear transistor being connected to a constant potential source, and
the second conductive terminal of the output transistor serving as an output terminal of the unit circuit in the end stage.

31. The display panel drive circuit according to claim 30, wherein:

the unit circuit in the end stage further includes a potential supplying transistor, the potential supplying transistor having a control terminal, a first conductive terminal, and a second conductive terminal,
the potential supplying transistor receiving the clear signal via its control terminal,
the first conductive terminal of the potential supplying transistor being connected to the second conductive terminal of the output transistor, and
the second conductive terminal of the potential supplying transistor being connected to the constant potential source.

32. A display panel drive circuit receiving a sync signal from outside, the display panel drive circuit including a shift register constructed of unit circuits connected in stages, each of the unit circuits receiving a clock signal and outputting a respective pulse by use of the received clock signal, the pulses being outputted successively from each of the stages, each of the unit circuits having an output transistor provided between an input terminal of the clock signal and an output terminal of the respective unit circuit,
a clear signal being generated and inputted into each of the unit circuits, the clear signal being made active in a case where anomalousness is included in at least the sync signal, and
once the clear signal is made active, the output transistor provided in each of the unit circuits being turned OFF until a subsequent vertical scanning period starts.

33. The display panel drive circuit according to claim 32, wherein:

regardless of whether or not anomalousness is included in the sync signal, the clear signal is made active after the pulse is outputted from a unit circuit in the end stage, so that the output transistor in each of the unit circuits is turned OFF until the subsequent vertical scanning period starts.

34. The display panel drive circuit according to claim 32, wherein:

the clear signal is made active at a timing in which no pulse is outputted or at a timing in which the pulse is made inactive.

35. A shift register, provided in a display panel drive circuit, the shift register being constructed of unit circuits connected in stages, the unit circuits generating signal line selection signals, respectively, each of the signal line selection signals being made active for a respective certain period of time to form a respective pulse, the pulses being outputted successively from respective unit circuits in order of ordinal number starting from a first stage until an end stage,
a unit circuit in the end stage receiving (i) a signal line selection signal generated in a stage different from its own stage, (ii) a clock signal, and (iii) a clear signal, and
the clear signal being made active after a pulse is outputted from the end stage, so that the signal line selection signal outputted from the end stage remains inactive.

36. A method for driving a display device including a shift register constructed of unit circuits connected in stages, the unit circuits generating signal line selection signals, respectively, each of the signal line se-

lection signals being made active for a respective certain period of time to form a respective pulse, the shift register outputting the pulses successively from respective unit circuits in order of ordinal number starting from a first stage until an end stage,
the method comprising:

inputting, to a unit circuit in the end stage, (i) a signal line selection signal generated in a stage different from its own stage, (ii) a clock signal, and (iii) a clear signal; and
activating the clear signal after a pulse is outputted from the end stage, so that the signal line selection signal outputted from the end stage remains inactive.

F I G. 1

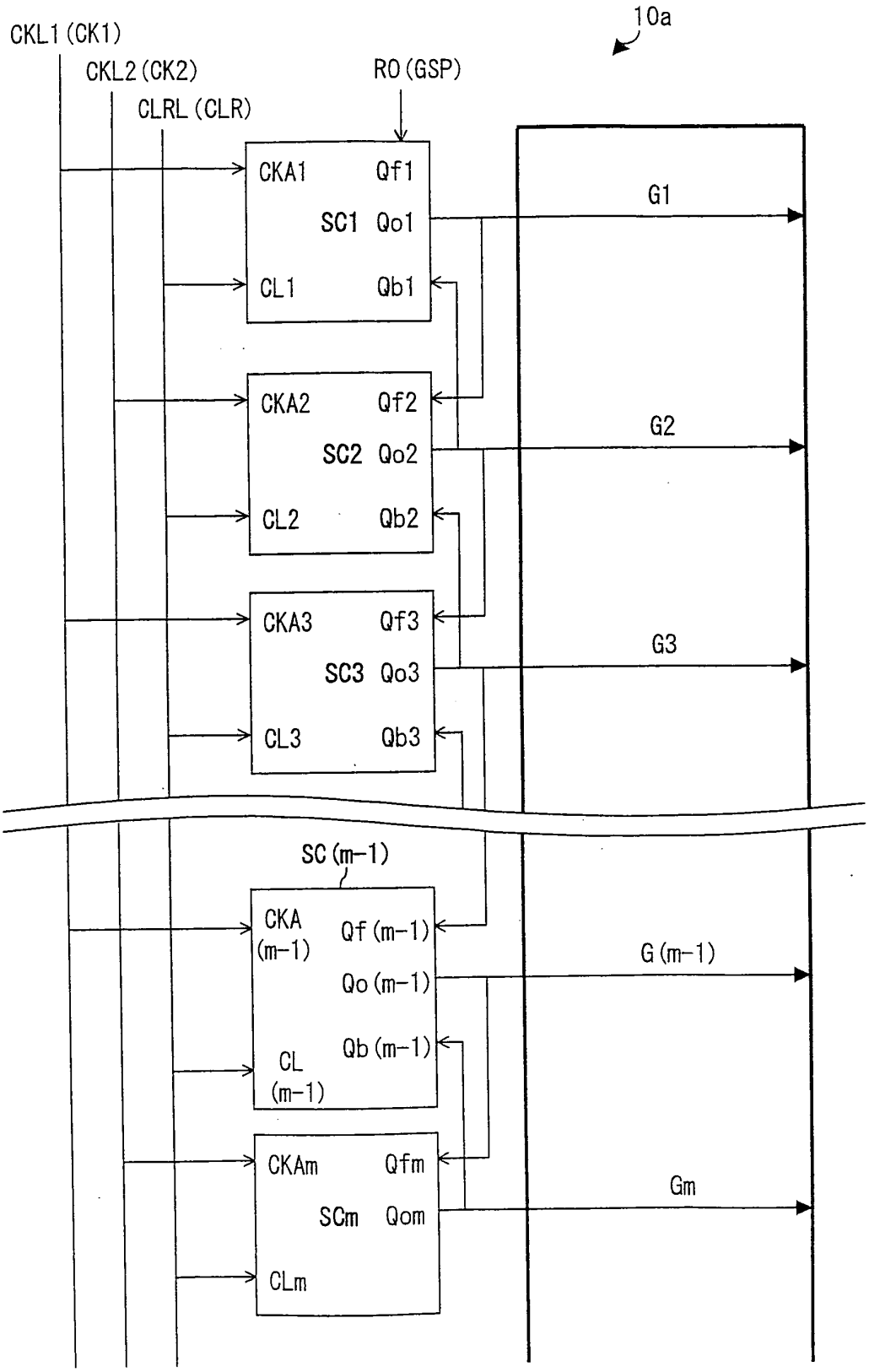
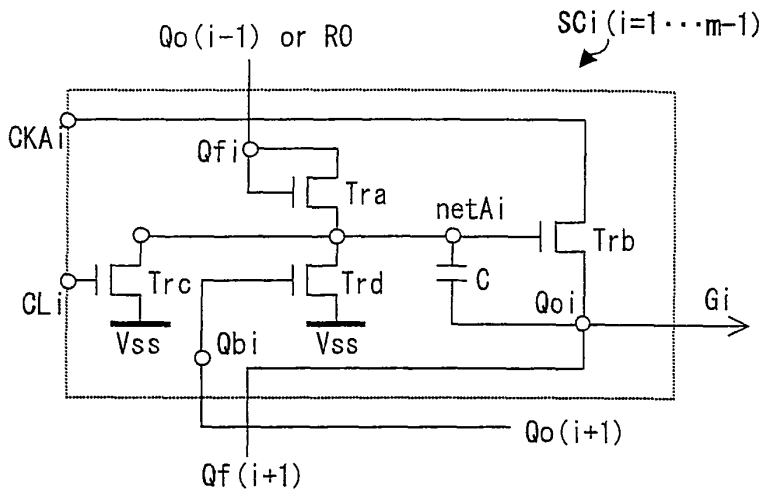

10a
CKL1 (CK1)
CKL2 (CK2)
CLRL (CLR)
RO (GSP)
CKA1
Qf1
SC1
Qo1
CL1
Qb1
G1
CKA2
Qf2
SC2
Qo2
CL2
Qb2
G2
CKA3
Qf3
SC3
Qo3
CL3
Qb3
G3
SC (m-1)
CKA (m-1)
Qf (m-1)
Qo (m-1)
Qb (m-1)
CL (m-1)
G (m-1)
CKAm
Qfm
SCm
Qom
CLm
Gm

FIG. 2

(a)


Qo(i-1) or RO
SCi(i=1···m-1)
CKAi
Qfi
Tra
netAi
Trb
CLi
Trc
Trd
C
Qoi
Gi
Vss
Qbi
Vss
Qo(i+1)
Qf(i+1)

(b)

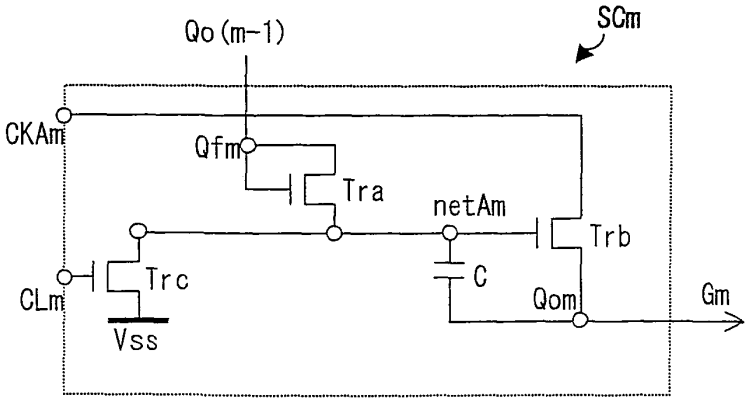
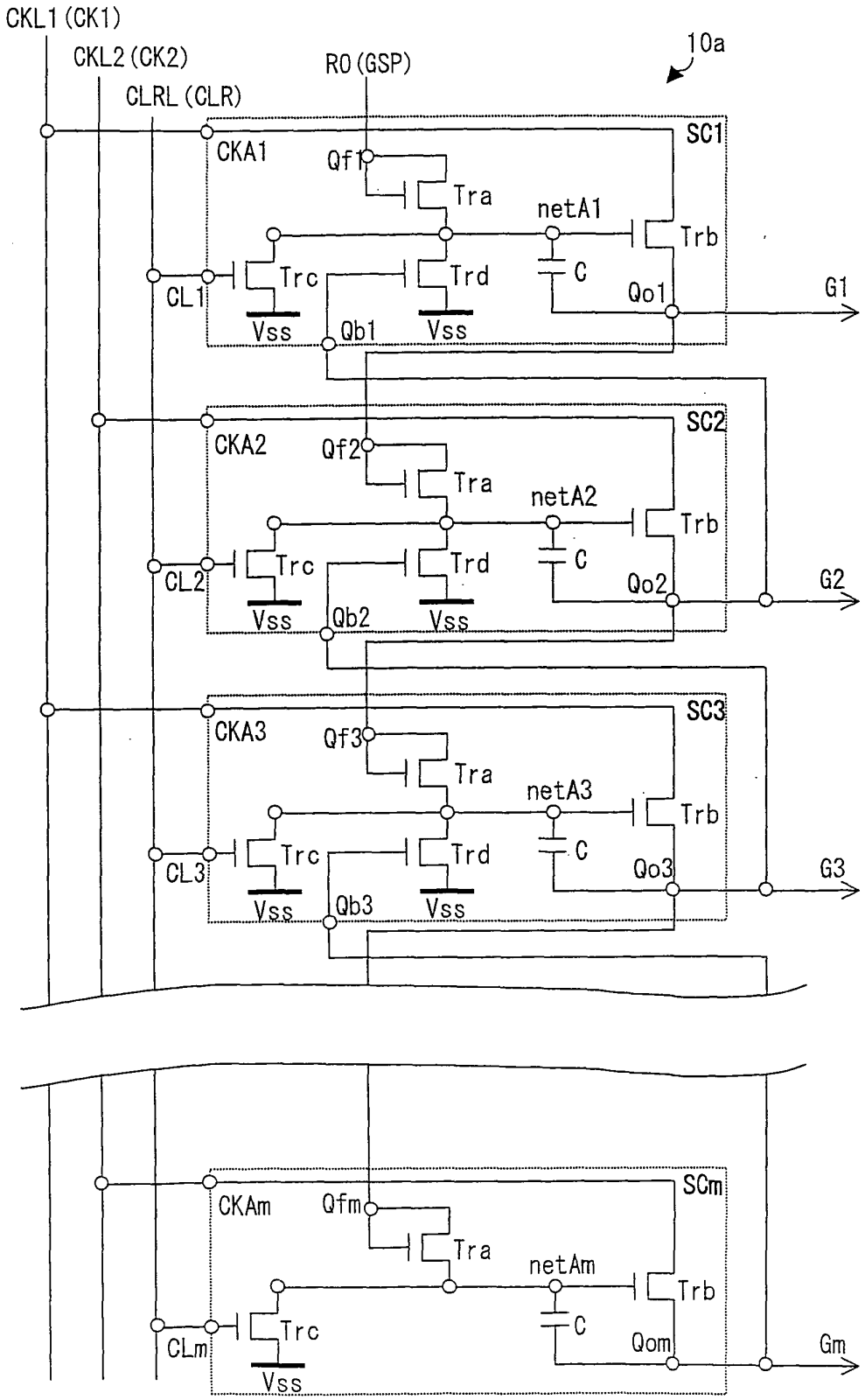

Qo(m-1)
SCm
CKAm
Qfm
Tra
netAm
Trb
CLm
Trc
C
Qom
Gm
Vss

FIG. 3


CKL1 (CK1)
CKL2 (CK2)
CLRL (CLR)
R0 (GSP)
10a
SC1
CKA1
Qf1
Tra
netA1
Trb
Trc
Trd
C
CL1
Qo1
G1
Vss
Qb1
Vss
SC2
CKA2
Qf2
Tra
netA2
Trb
Trc
Trd
C
CL2
Qo2
G2
Vss
Qb2
Vss
SC3
CKA3
Qf3
Tra
netA3
Trb
Trc
Trd
C
CL3
Qo3
G3
Vss
Qb3
Vss
SCm
CKAm
Qfm
Tra
netAm
Trb
Trc
C
CLm
Qom
Gm
Vss

F I G. 4

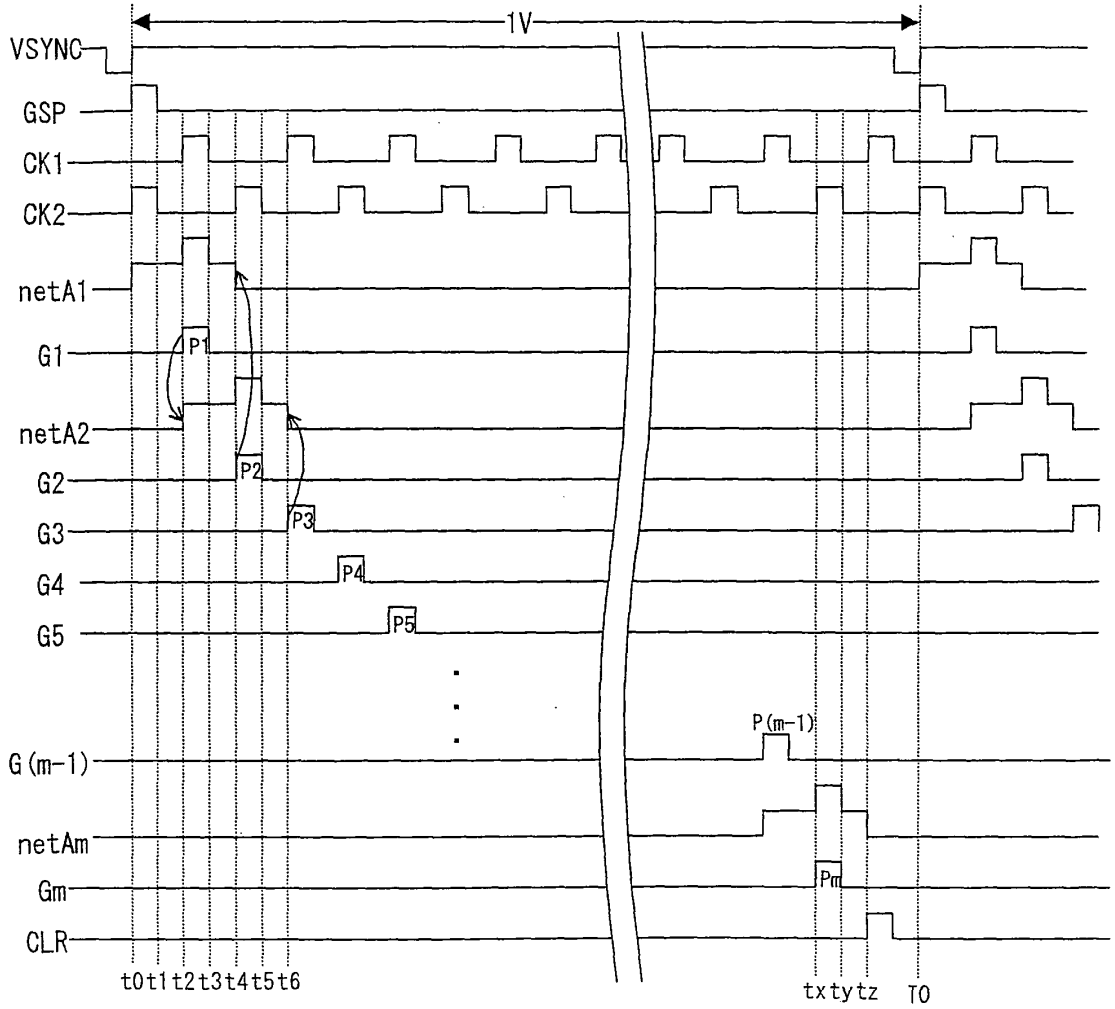

1V
VSYNC
GSP
CK1
CK2
netA1
G1
netA2
G2
G3
G4
G5
G(m-1)
netAm
Gm
CLR
P1
P2
P3
P4
P5
P(m-1)
Pm
t0 t1 t2 t3 t4 t5 t6
tx ty tz T0

FIG. 5

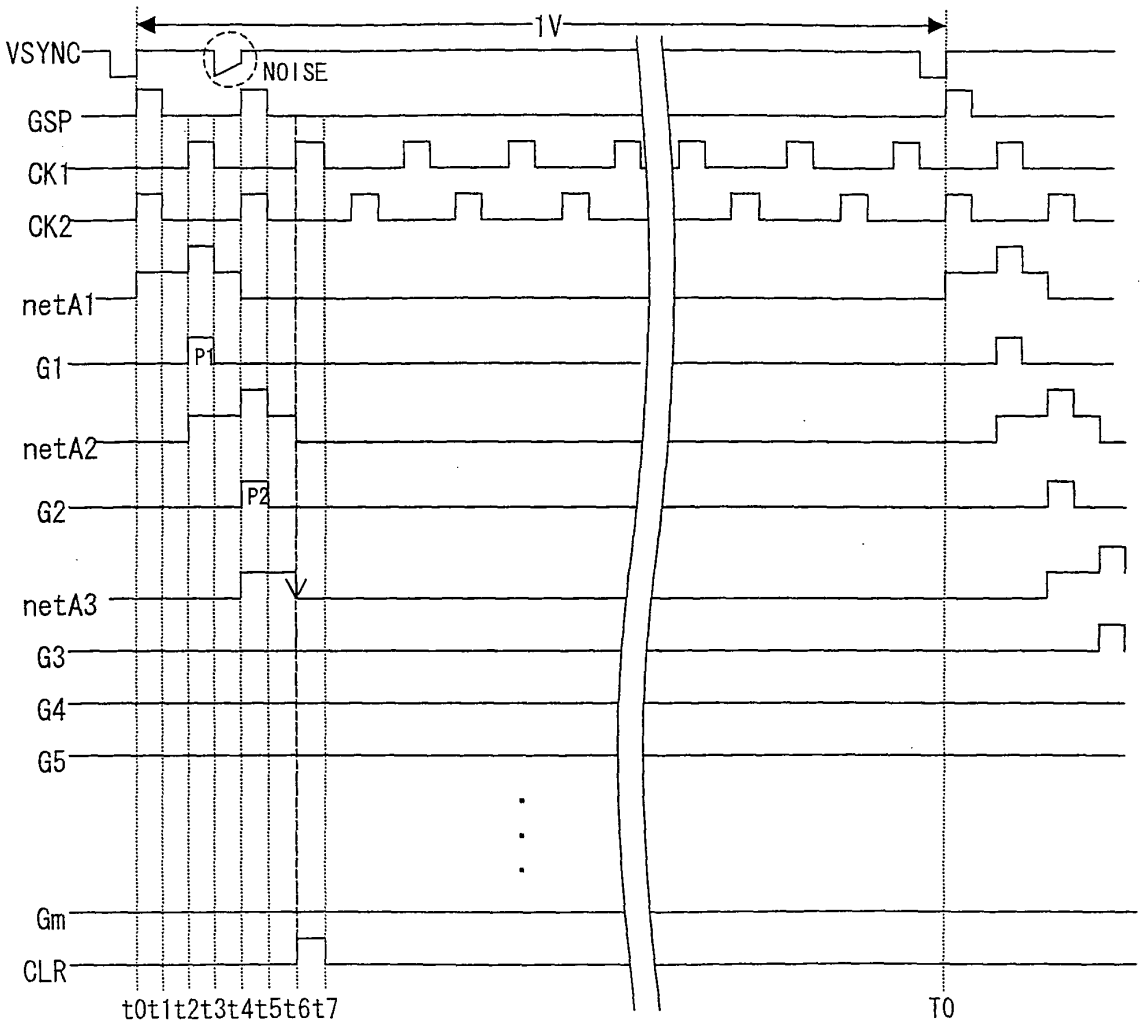
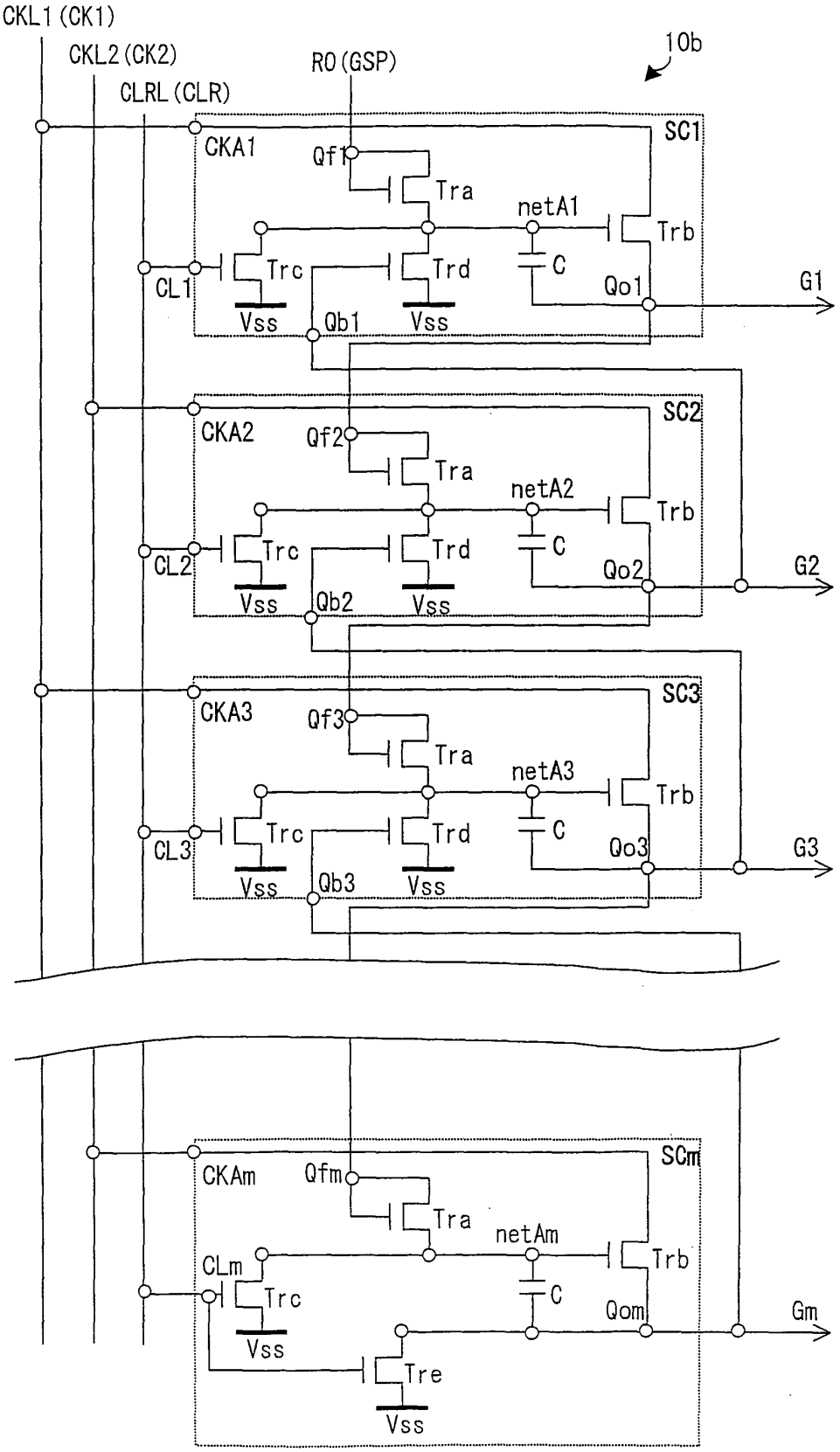
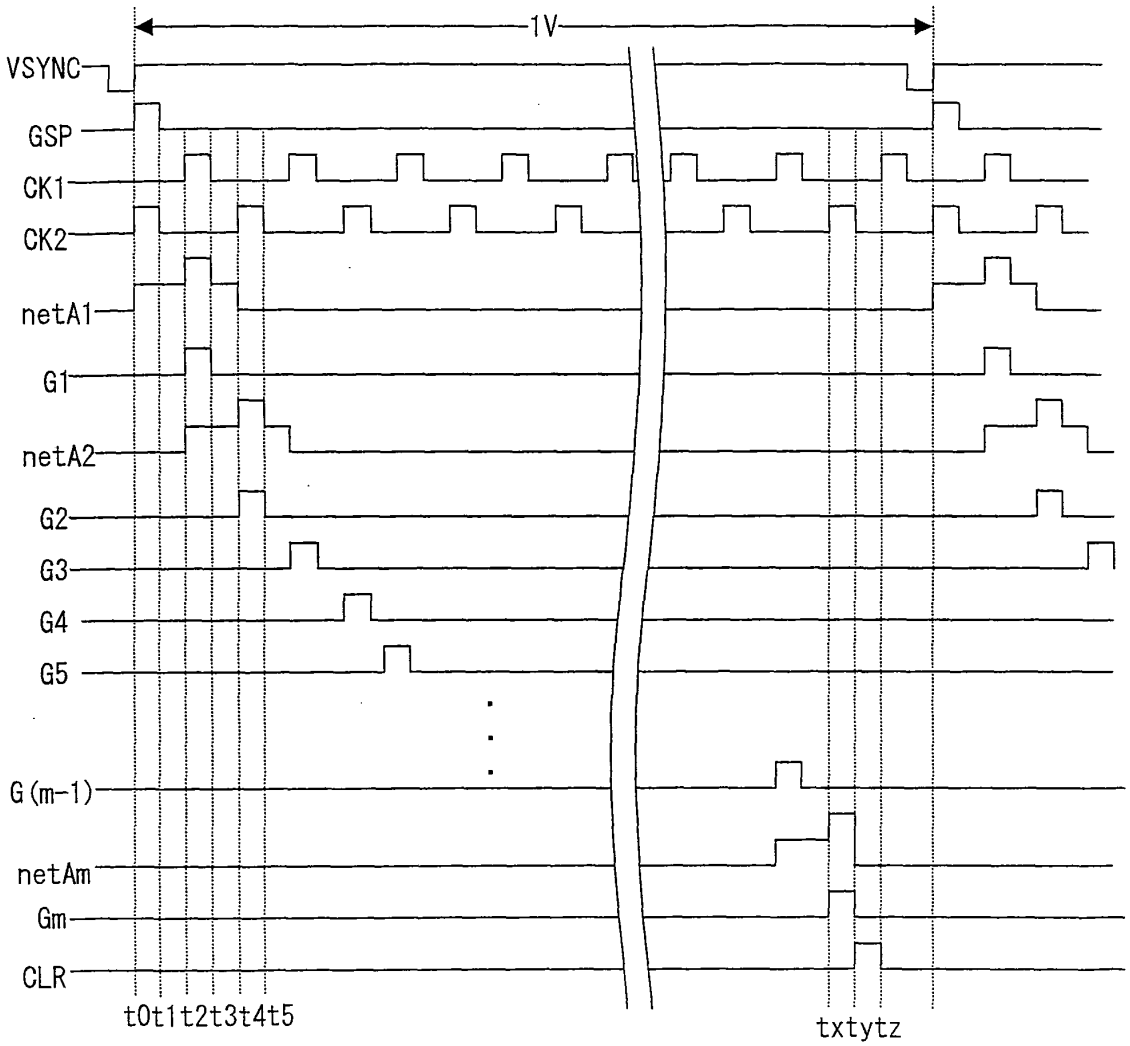

1V
VSYNC
NOISE
GSP
CK1
CK2
netA1
G1
P1
netA2
G2
P2
netA3
G3
G4
G5
Gm
CLR
t0t1t2t3t4t5t6t7
T0

FIG. 6


CKL1 (CK1)
CKL2 (CK2)
CLRL (CLR)
RO (GSP)
10b
SC1
CKA1
Qf1
Tra
netA1
Trb
Trc
Trd
C
CL1
Qo1
G1
Vss
Qb1
Vss
SC2
CKA2
Qf2
Tra
netA2
Trb
Trc
Trd
C
CL2
Qo2
G2
Vss
Qb2
Vss
SC3
CKA3
Qf3
Tra
netA3
Trb
Trc
Trd
C
CL3
Qo3
G3
Vss
Qb3
Vss
SCm
CKAm
Qfm
Tra
netAm
Trb
CLm
Trc
C
Qom
Gm
Vss
Tre
Vss

F I G. 7


1V
VSYNC
GSP
CK1
CK2
netA1
G1
netA2
G2
G3
G4
G5
G(m-1)
netAm
Gm
CLR
t0t1t2t3t4t5
txtytz

F I G. 8

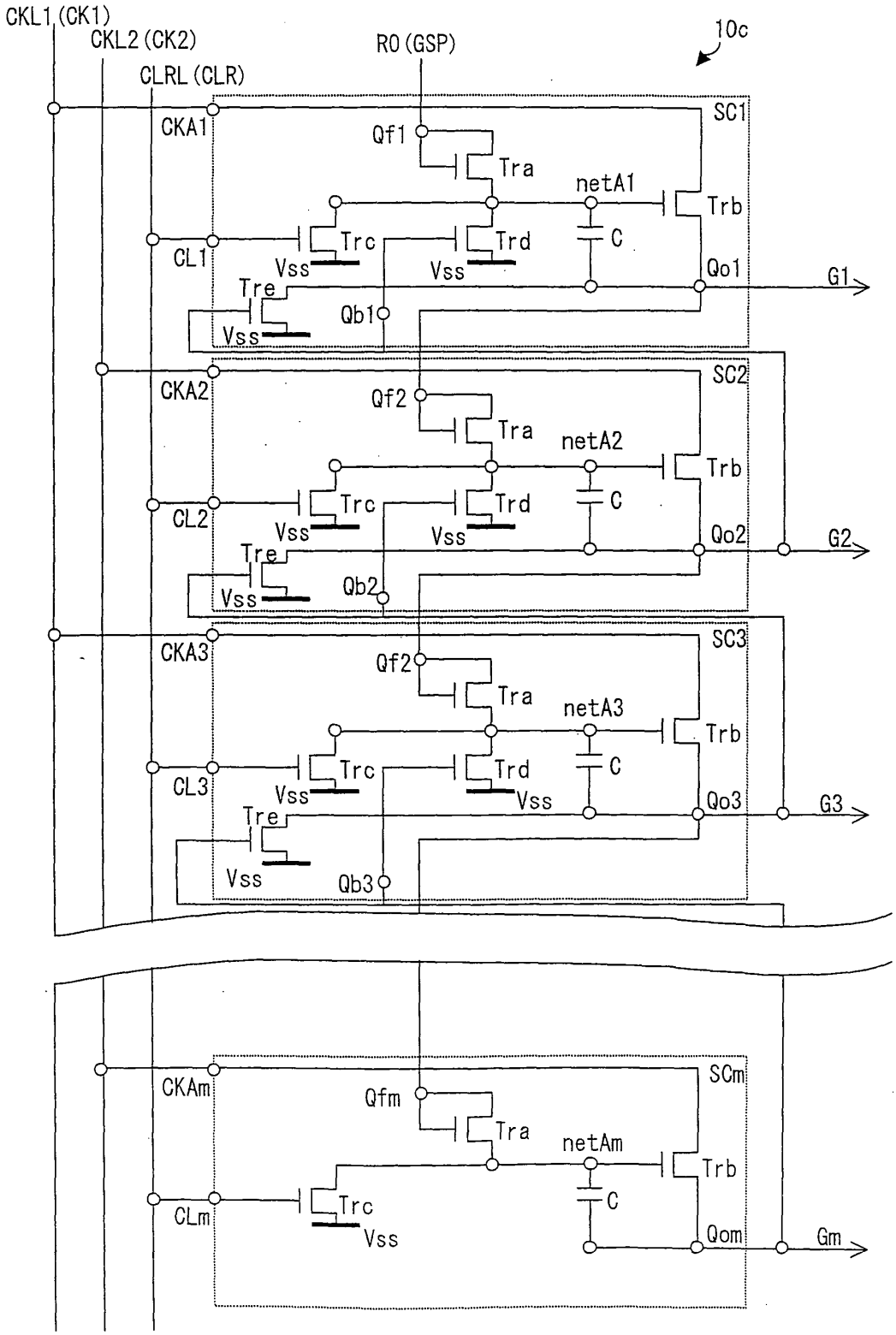

CKL1 (CK1)
CKL2 (CK2)
CLRL (CLR)
RO (GSP)
10c
SC1
CKA1
Qf1
Tra
netA1
Trb
Trc
Trd
C
CL1
Vss
Vss
Qo1
G1
Tre
Qb1
Vss
SC2
CKA2
Qf2
Tra
netA2
Trb
Trc
Trd
C
CL2
Vss
Vss
Qo2
G2
Tre
Qb2
Vss
SC3
CKA3
Qf2
Tra
netA3
Trb
Trc
Trd
C
CL3
Vss
Vss
Qo3
G3
Tre
Vss
Qb3
SCm
CKAm
Qfm
Tra
netAm
Trb
Trc
C
CLm
Vss
Qom
Gm

FIG. 9

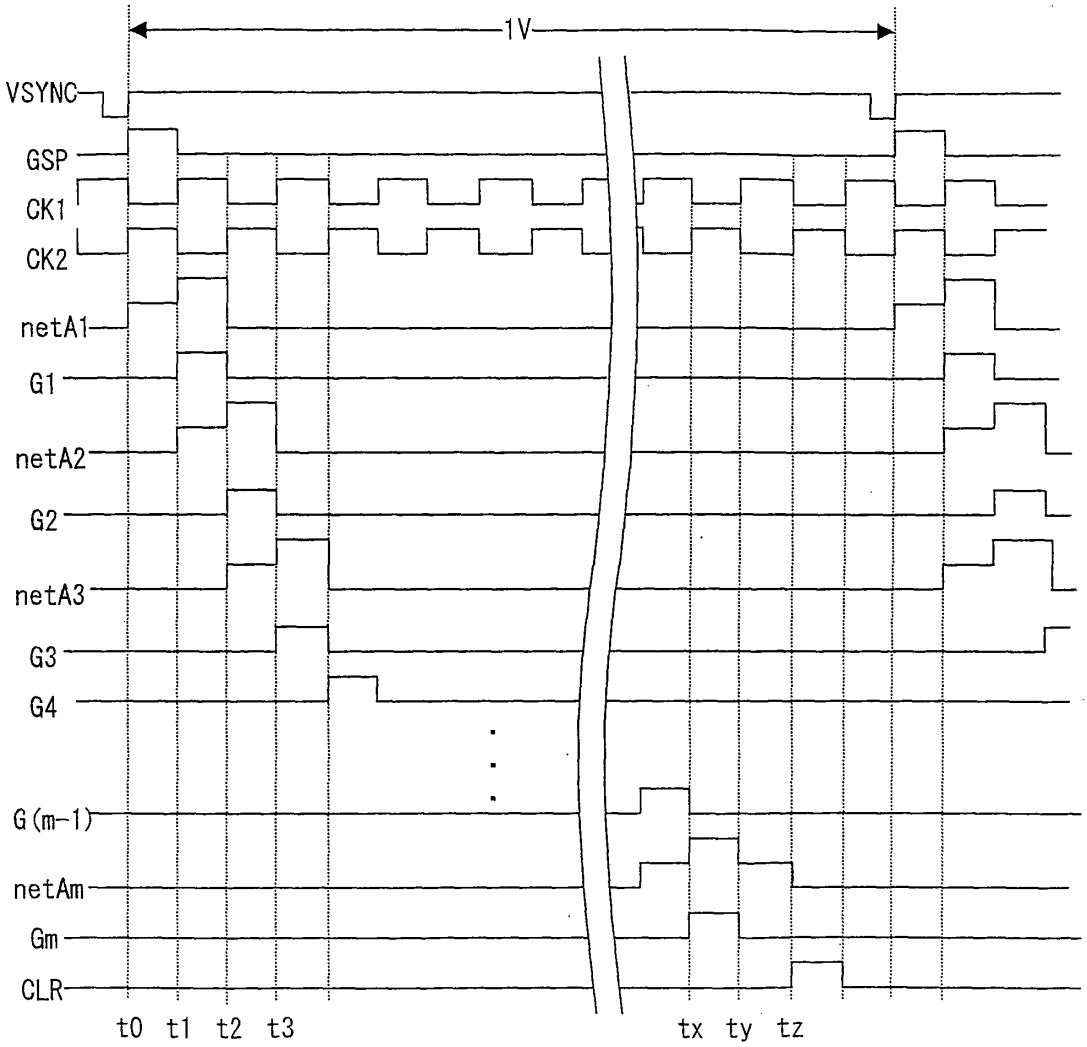

1V
VSYNC
GSP
CK1
CK2
netA1
G1
netA2
G2
netA3
G3
G4
G(m-1)
netAm
Gm
CLR
t0 t1 t2 t3
tx ty tz

FIG. 10

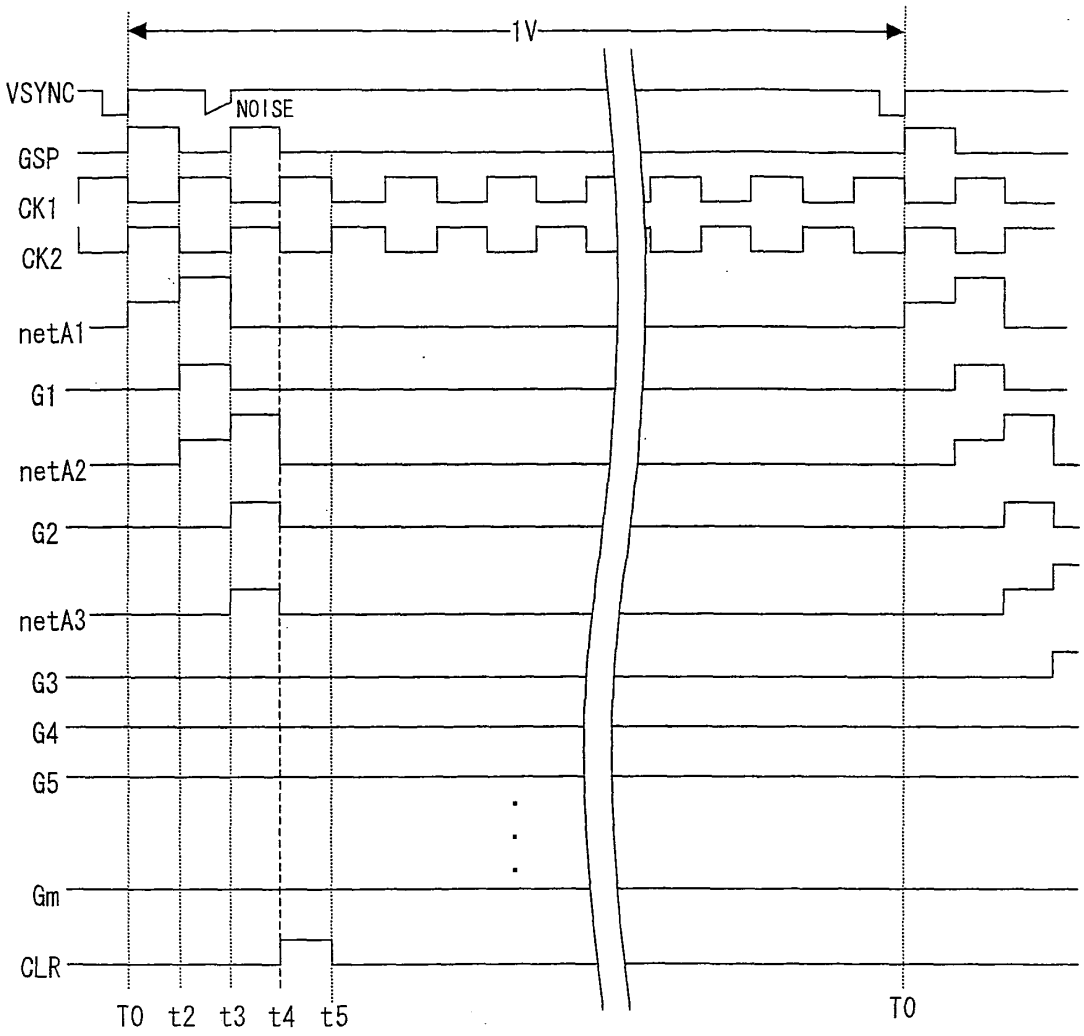

1V
VSYNC
NOISE
GSP
CK1
CK2
netA1
G1
netA2
G2
netA3
G3
G4
G5
Gm
CLR
T0
t2
t3
t4
t5
T0

FIG. 11

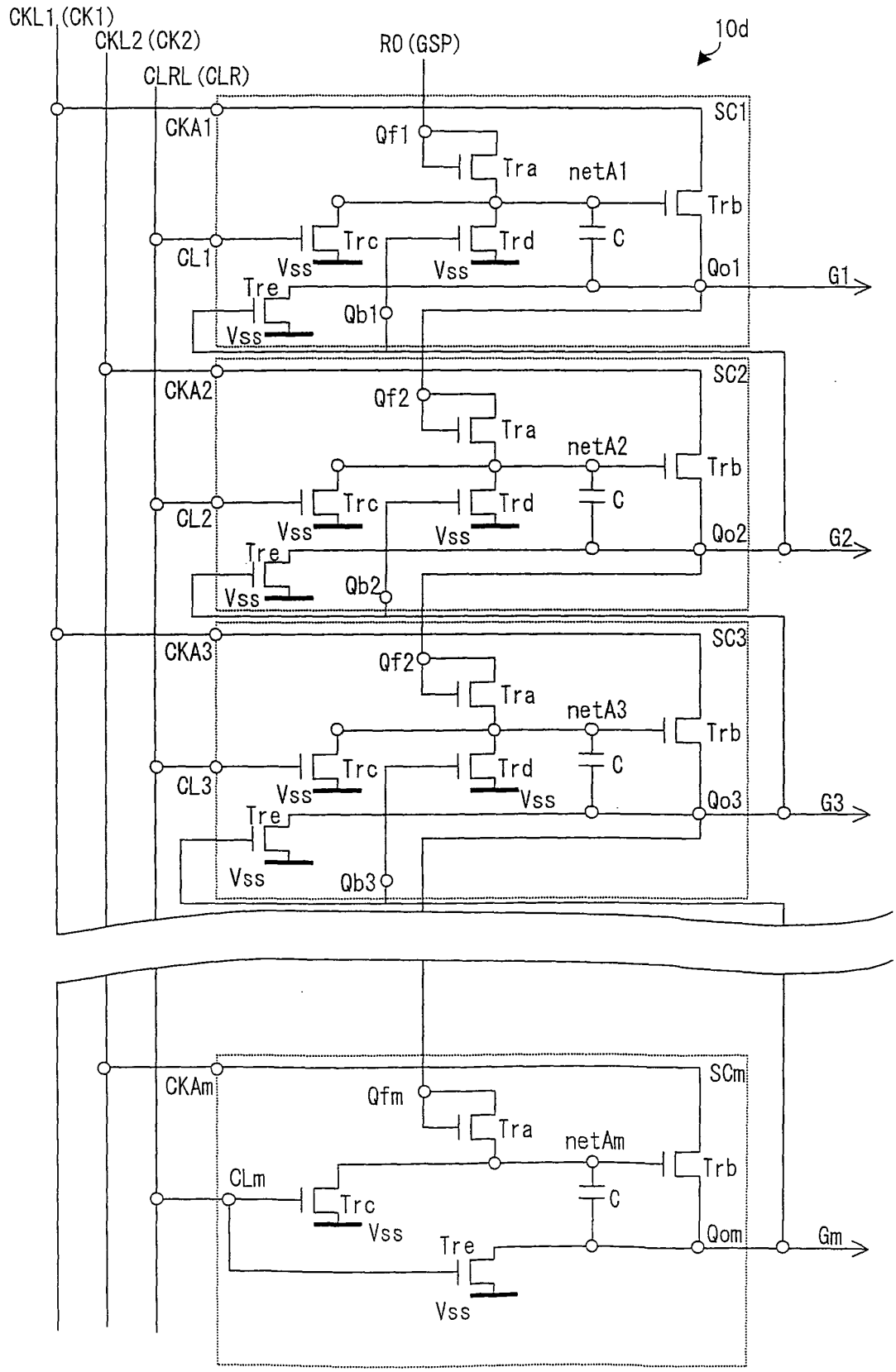
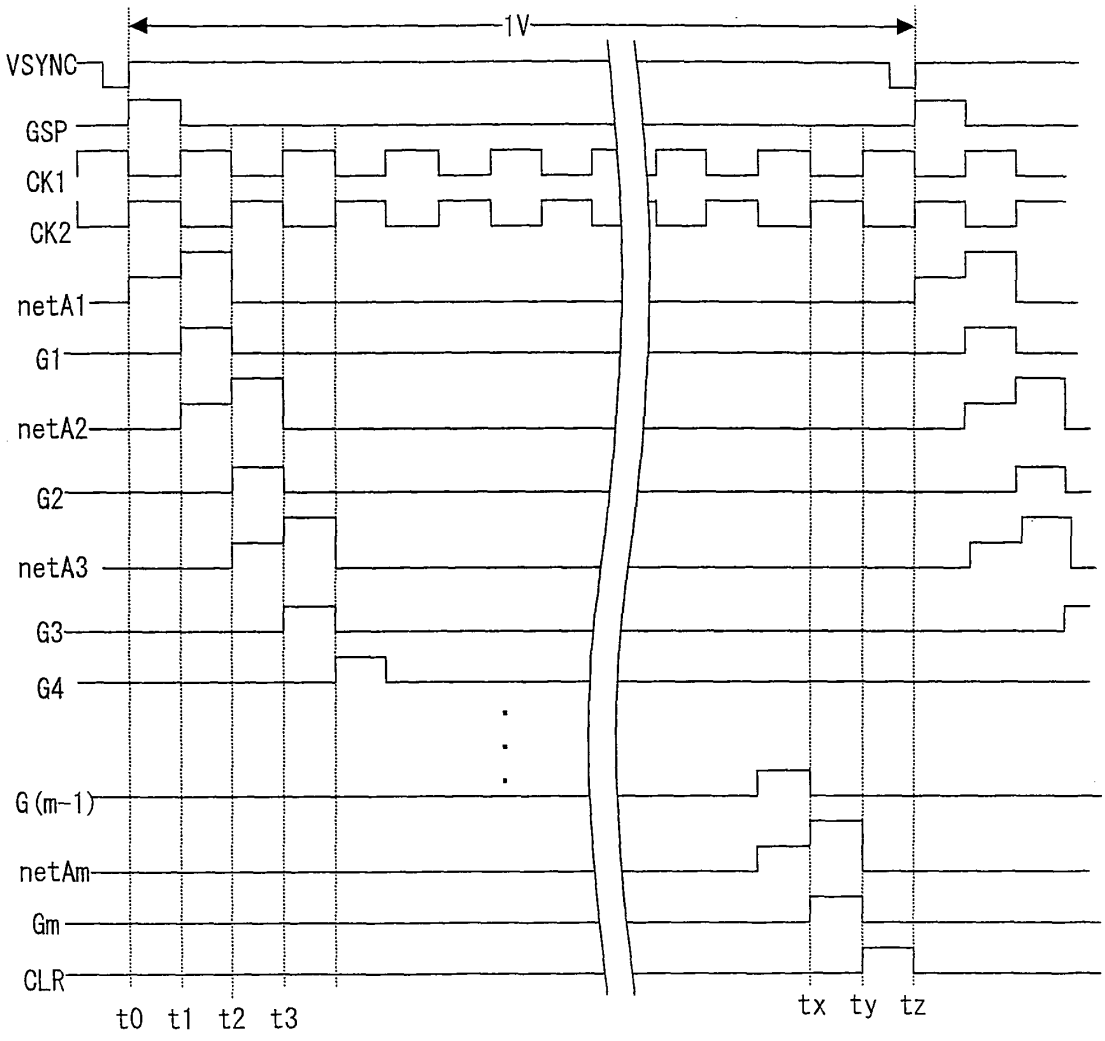

CKL1 (CK1)
CKL2 (CK2)
CLRL (CLR)
RO (GSP)
10d
SC1
CKA1
Qf1
Tra
netA1
Trb
Trc
Trd
C
CL1
Vss
Vss
Qo1
G1
Tre
Qb1
Vss
SC2
CKA2
Qf2
Tra
netA2
Trb
Trc
Trd
C
CL2
Vss
Vss
Qo2
G2
Tre
Qb2
Vss
SC3
CKA3
Qf2
Tra
netA3
Trb
Trc
Trd
C
CL3
Vss
Vss
Qo3
G3
Tre
Vss
Qb3
SCm
CKAm
Qfm
Tra
netAm
Trb
CLm
Trc
C
Vss
Qom
Gm
Tre
Vss

FIG. 12


1V
VSYNC
GSP
CK1
CK2
netA1
G1
netA2
G2
netA3
G3
G4
G(m-1)
netAm
Gm
CLR
t0
t1
t2
t3
tx
ty
tz

F I G. 1 3

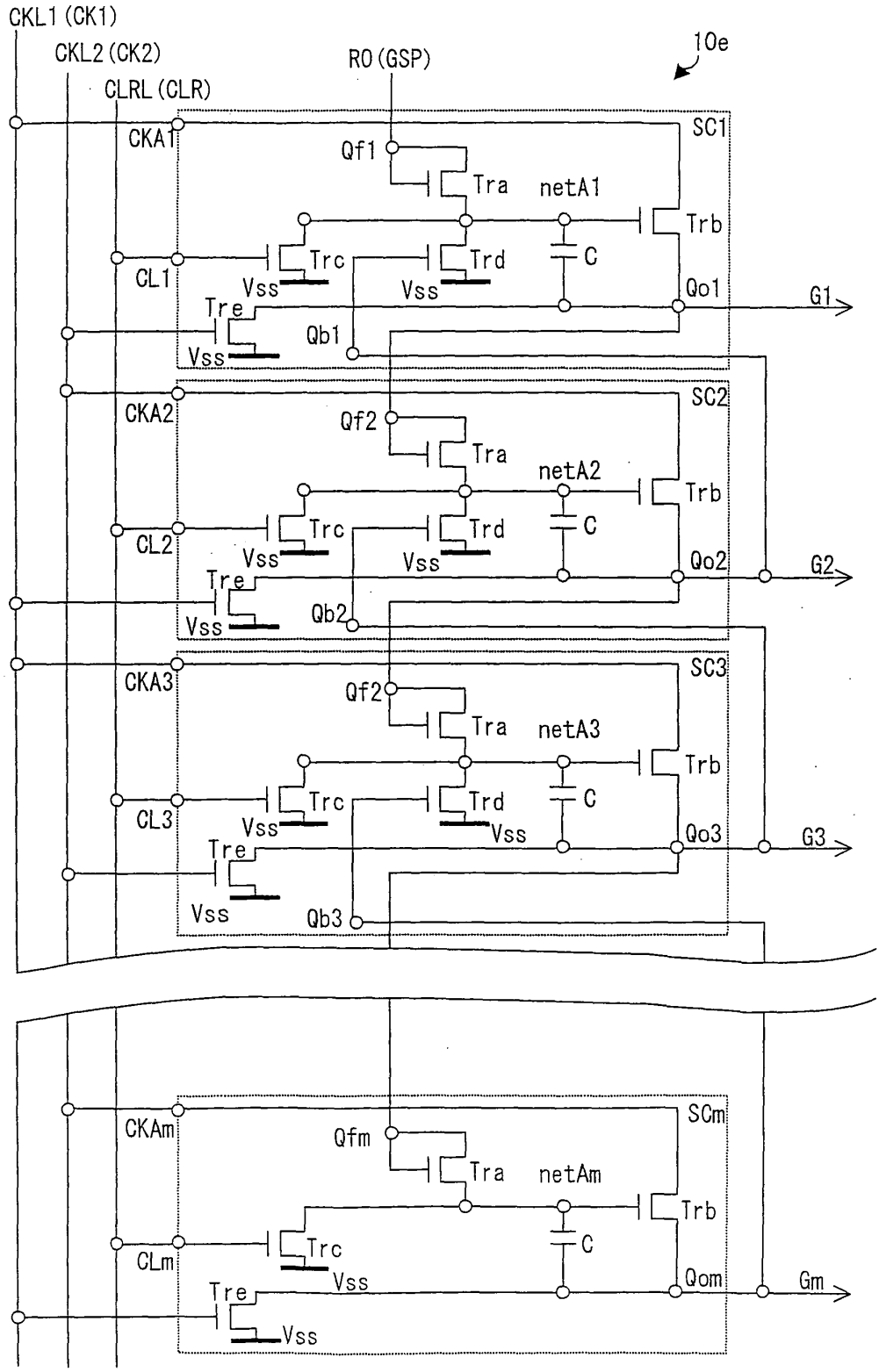

CKL1 (CK1)
CKL2 (CK2)
CLRL (CLR)
RO (GSP)
10e
SC1
CKA1
Qf1
Tra
netA1
Trb
Trc
Trd
C
CL1
Vss
Qo1
G1
Tre
Qb1
SC2
CKA2
Qf2
netA2
CL2
Qo2
G2
Qb2
SC3
CKA3
netA3
CL3
Qo3
G3
Qb3
SCm
CKAm
Qfm
netAm
CLm
Qom
Gm

FIG. 14

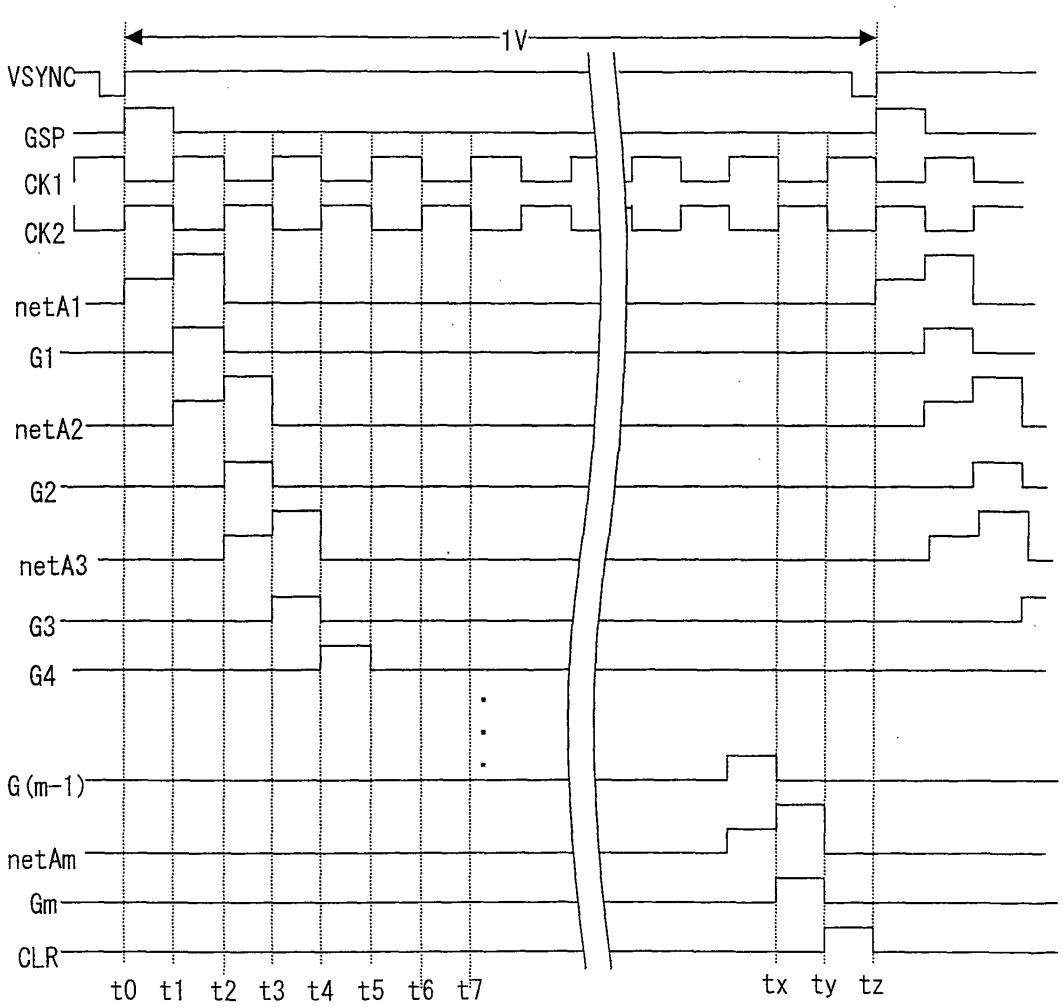

1V
VSYNC
GSP
CK1
CK2
netA1
G1
netA2
G2
netA3
G3
G4
G(m-1)
netAm
Gm
CLR
t0 t1 t2 t3 t4 t5 t6 t7
tx ty tz

FIG. 15

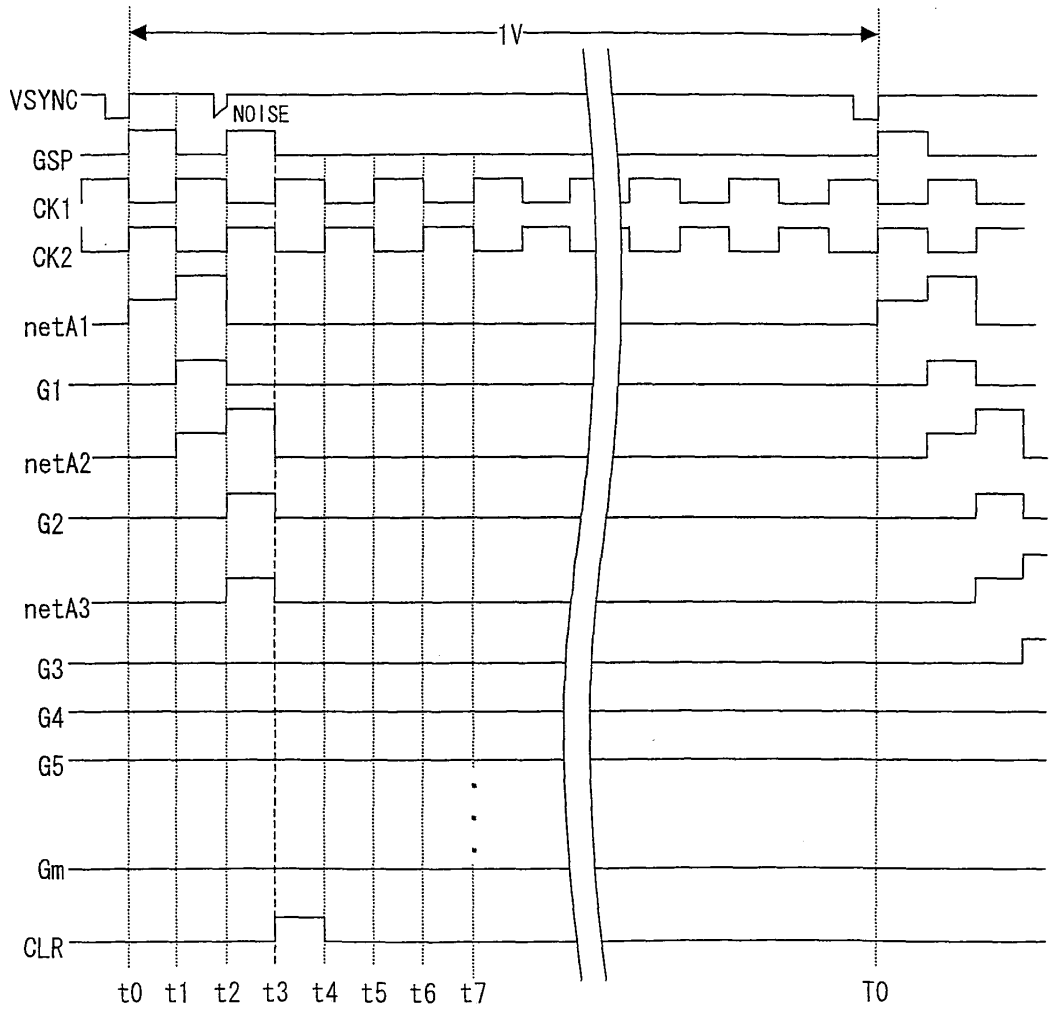
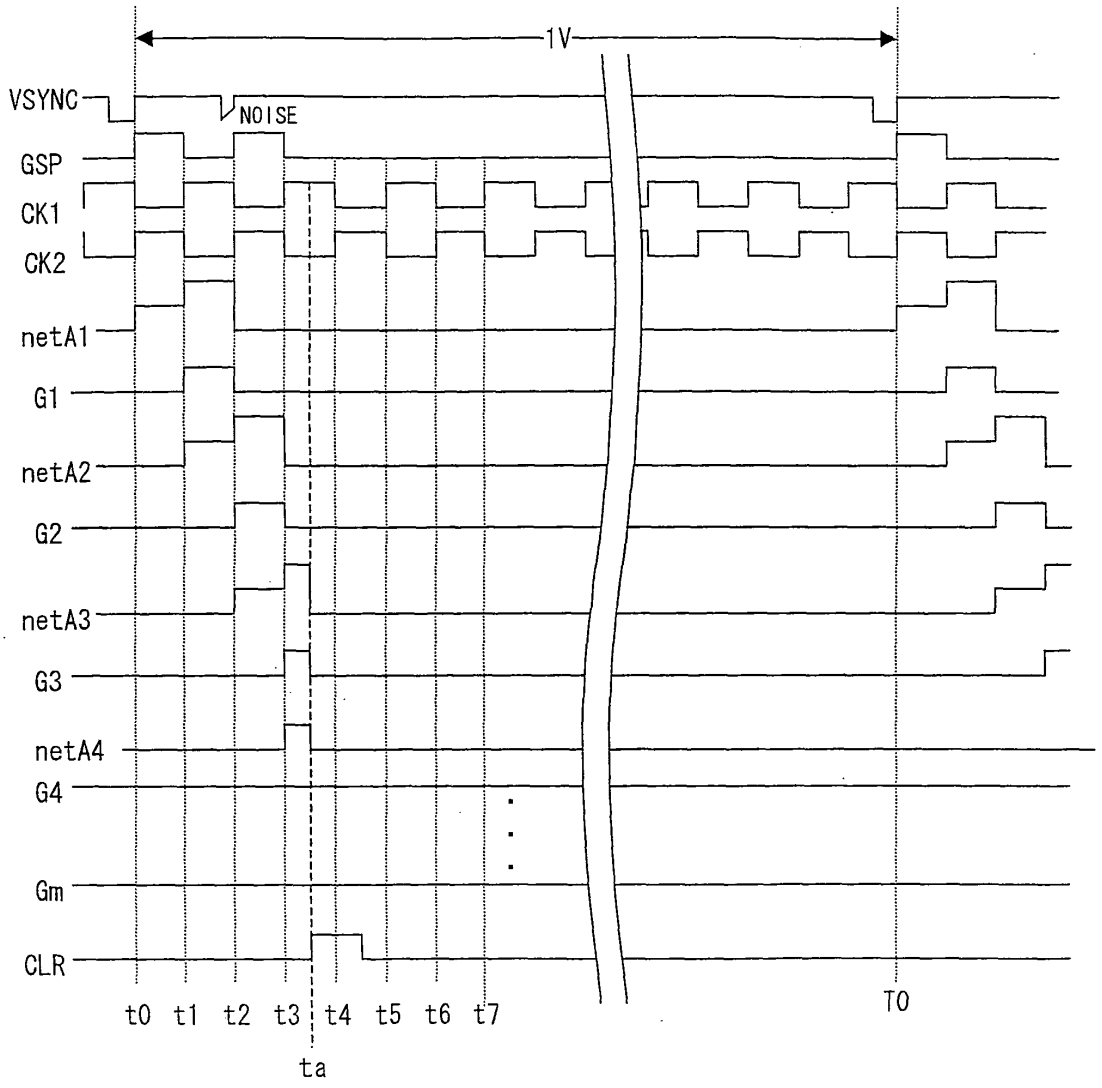

1V
VSYNC
NOISE
GSP
CK1
CK2
netA1
G1
netA2
G2
netA3
G3
G4
G5
Gm
CLR
t0
t1
t2
t3
t4
t5
t6
t7
T0

FIG. 16


1V
VSYNC
NOISE
GSP
CK1
CK2
netA1
G1
netA2
G2
netA3
G3
netA4
G4
Gm
CLR
t0 t1 t2 t3 t4 t5 t6 t7
ta
T0

F I G. 1 7

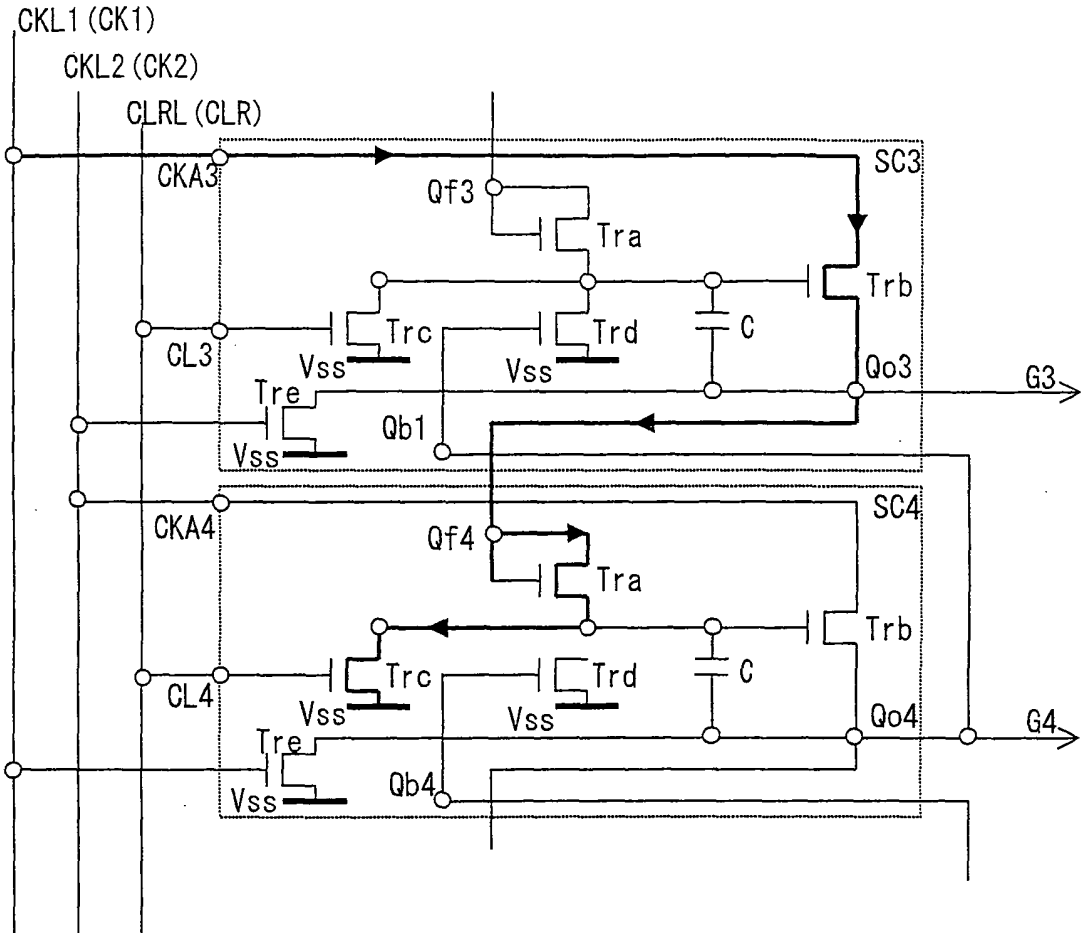

CKL1 (CK1)
CKL2 (CK2)
CLRL (CLR)
CKA3
SC3
Qf3
Tra
Trb
Trc
Trd
C
CL3
Vss
Vss
Qo3
G3
Tre
Qb1
Vss
CKA4
SC4
Qf4
Tra
Trb
Trc
Trd
C
CL4
Vss
Vss
Qo4
G4
Tre
Qb4
Vss

FIG. 18

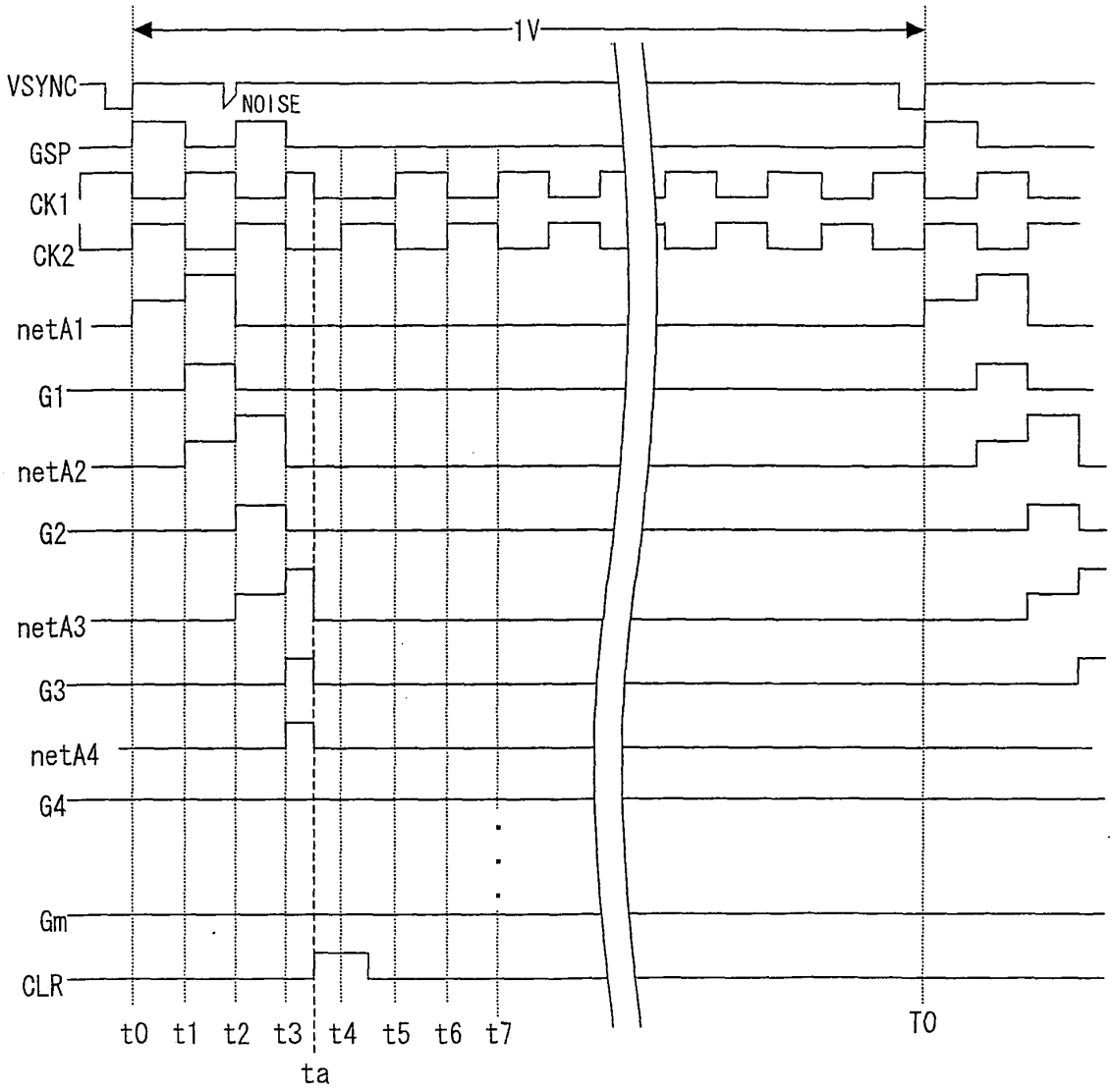

1V
VSYNC
NOISE
GSP
CK1
CK2
netA1
G1
netA2
G2
netA3
G3
netA4
G4
Gm
CLR
t0
t1
t2
t3
t4
t5
t6
t7
ta
T0

FIG. 19

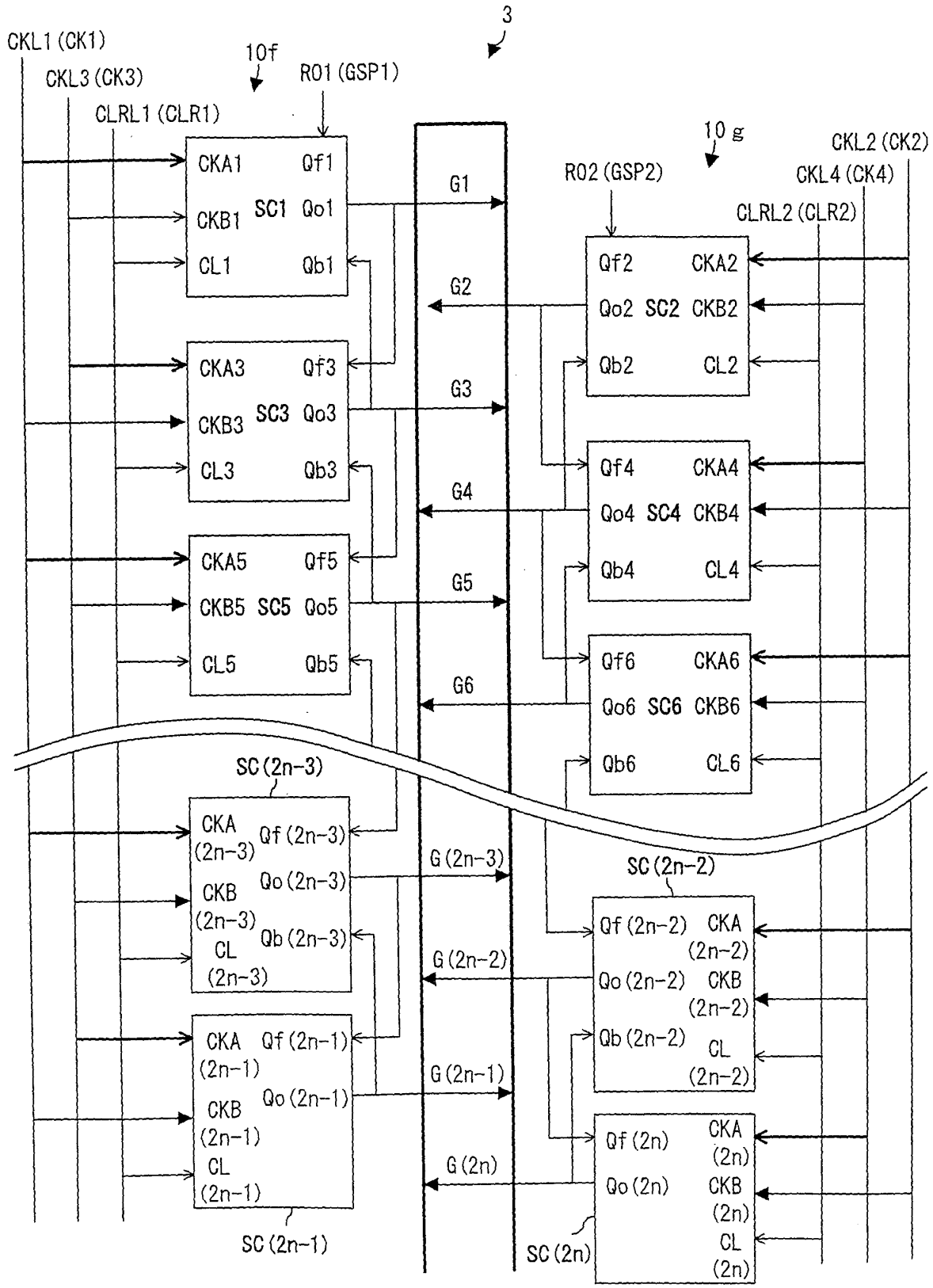
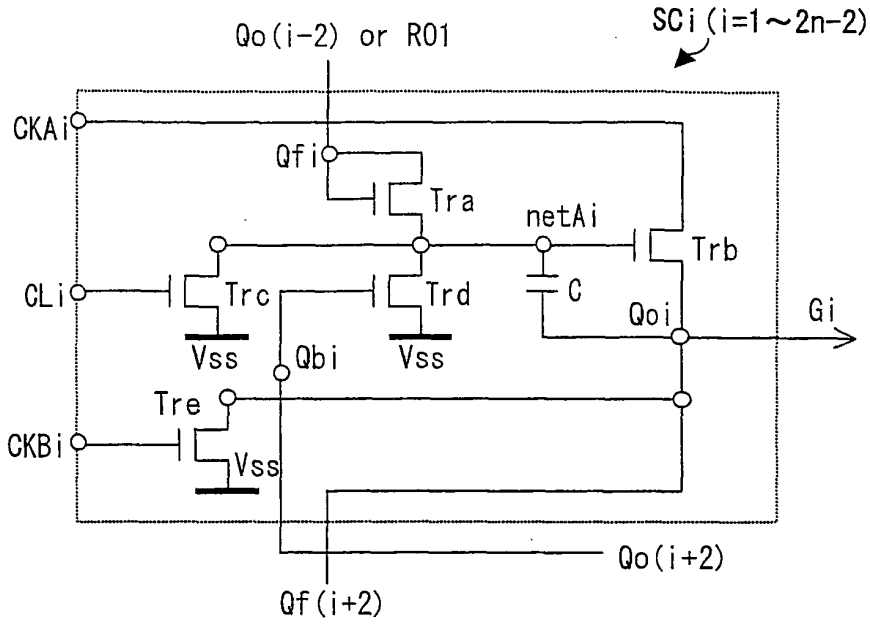

3
CKL1 (CK1)
CKL3 (CK3)
CLRL1 (CLR1)
10f
RO1 (GSP1)
10g
RO2 (GSP2)
CKL2 (CK2)
CKL4 (CK4)
CLRL2 (CLR2)
CKA1
Qf1
CKB1
SC1
Qo1
CL1
Qb1
CKA3
Qf3
CKB3
SC3
Qo3
CL3
Qb3
CKA5
Qf5
CKB5
SC5
Qo5
CL5
Qb5
Qf2
CKA2
Qo2
SC2
CKB2
Qb2
CL2
Qf4
CKA4
Qo4
SC4
CKB4
Qb4
CL4
Qf6
CKA6
Qo6
SC6
CKB6
Qb6
CL6
G1
G2
G3
G4
G5
G6
SC (2n-3)
CKA (2n-3)
Qf (2n-3)
CKB (2n-3)
Qo (2n-3)
CL (2n-3)
Qb (2n-3)
CKA (2n-1)
Qf (2n-1)
CKB (2n-1)
Qo (2n-1)
CL (2n-1)
SC (2n-1)
G (2n-3)
G (2n-2)
G (2n-1)
G (2n)
SC (2n-2)
Qf (2n-2)
CKA (2n-2)
Qo (2n-2)
CKB (2n-2)
Qb (2n-2)
CL (2n-2)
Qf (2n)
CKA (2n)
Qo (2n)
CKB (2n)
CL (2n)
SC (2n)

FIG. 20

(a)


Qo(i-2) or RO1
SCi(i=1～2n-2)
CKAi
Qfi
Tra
netAi
Trb
CLi
Trc
Trd
C
Qoi
Gi
Vss
Qbi
Vss
Tre
CKBi
Vss
Qo(i+2)
Qf(i+2)

(b)

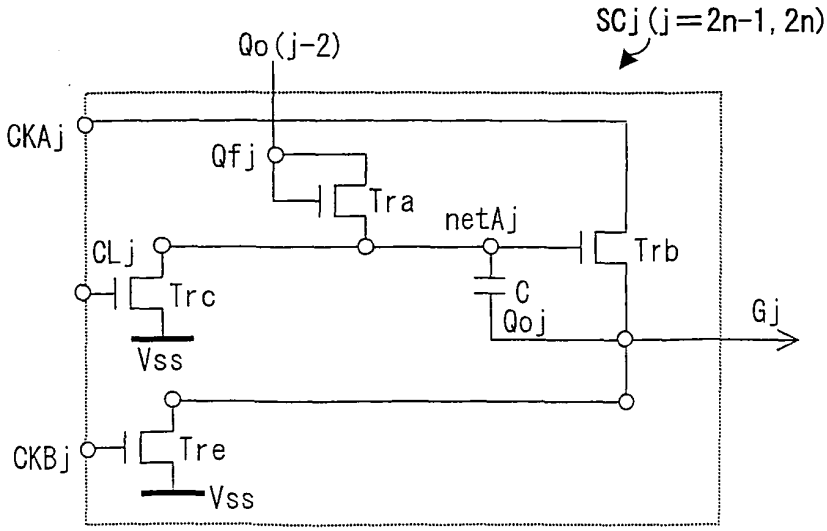

SCj(j=2n-1, 2n)
Qo(j-2)
CKAj
Qfj
Tra
netAj
CLj
Trb
Trc
C
Qoj
Gj
Vss
CKBj
Tre
Vss

FIG. 21

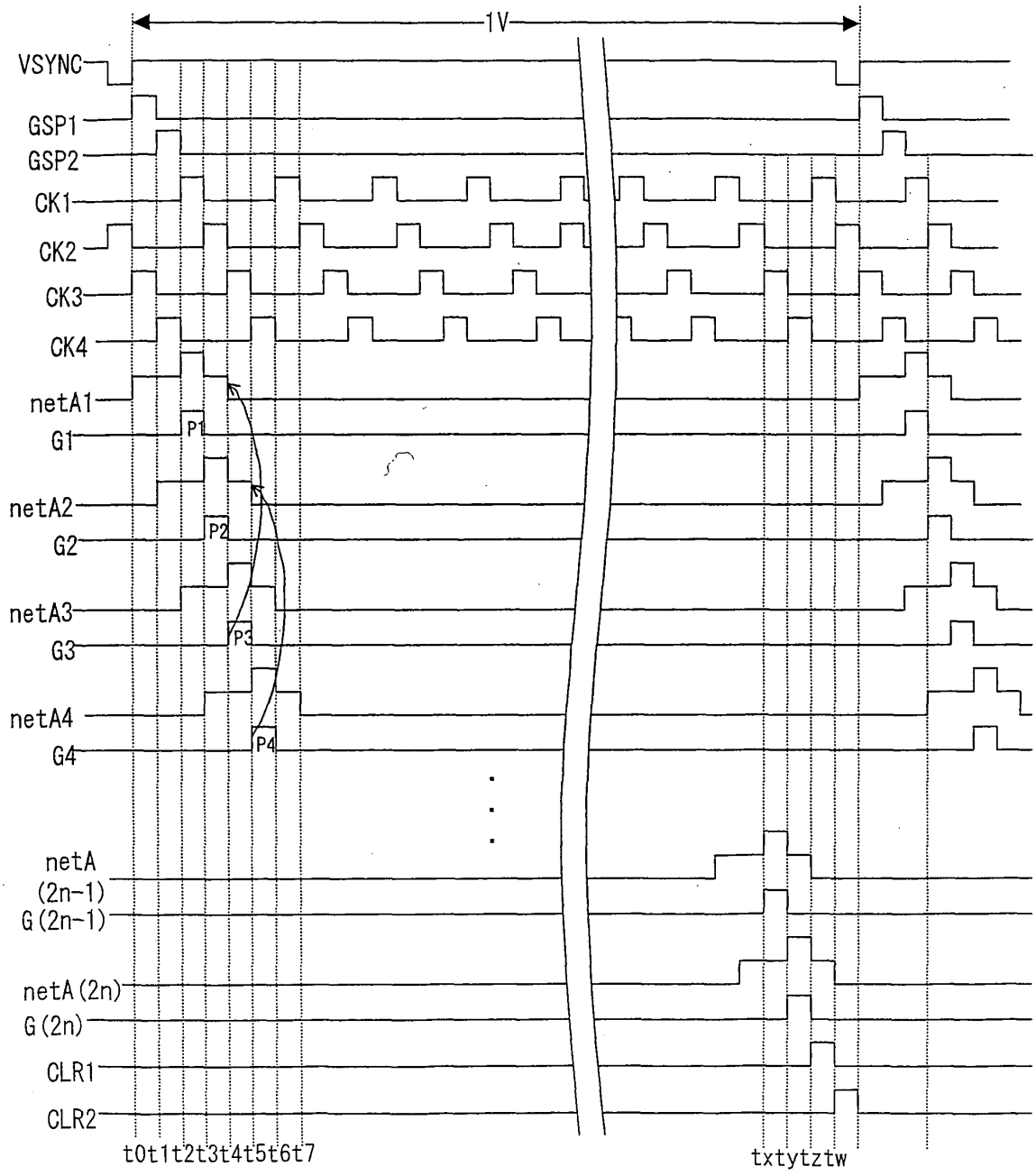

1V
VSYNC
GSP1
GSP2
CK1
CK2
CK3
CK4
netA1
G1
netA2
G2
netA3
G3
netA4
G4
P1
P2
P3
P4
netA
(2n-1)
G(2n-1)
netA(2n)
G(2n)
CLR1
CLR2
t0t1t2t3t4t5t6t7
txtytztw

FIG. 22

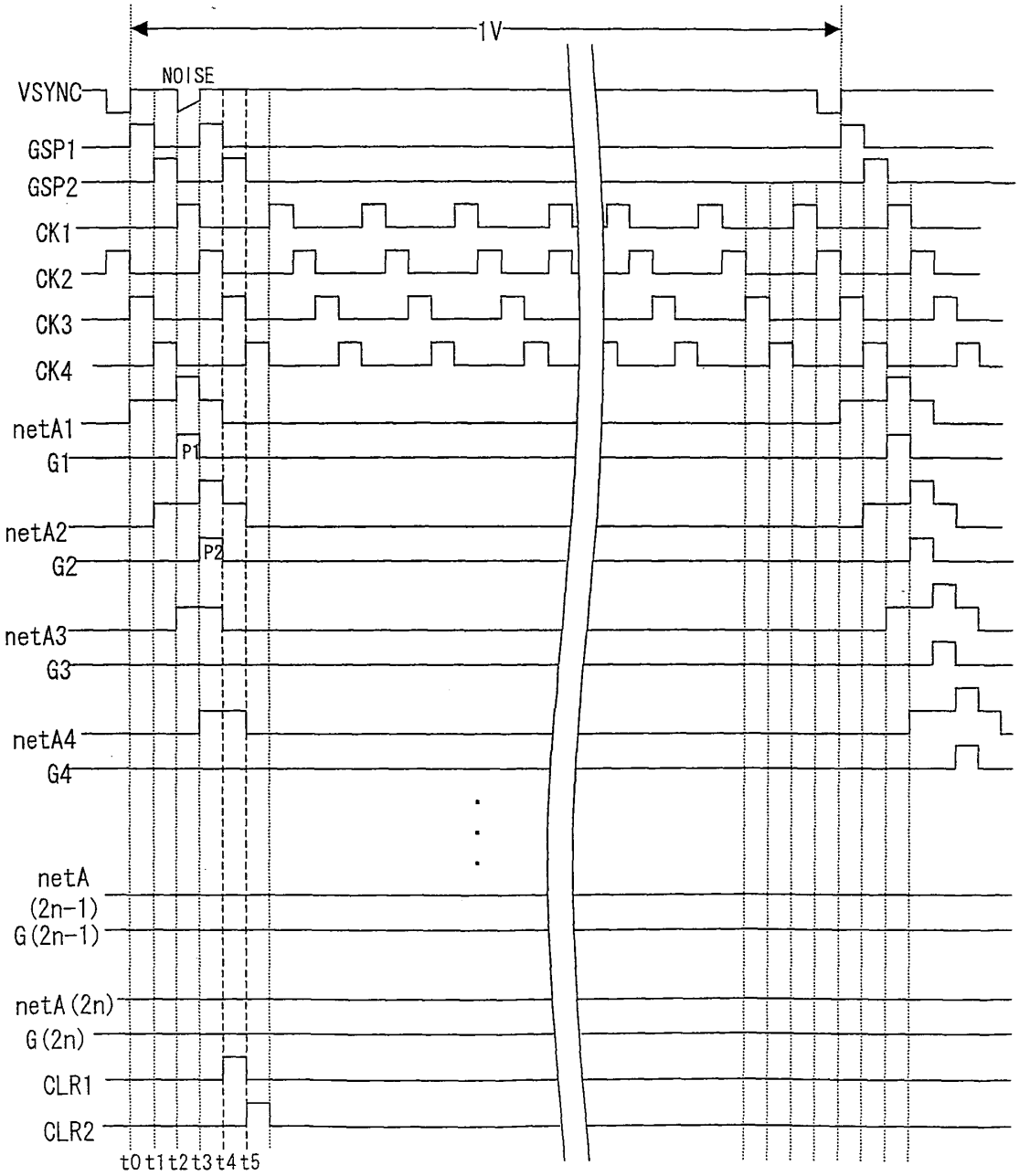

1V
NOISE
VSYNC
GSP1
GSP2
CK1
CK2
CK3
CK4
netA1
P1
G1
netA2
P2
G2
netA3
G3
netA4
G4
netA
(2n-1)
G(2n-1)
netA(2n)
G(2n)
CLR1
CLR2
t0 t1 t2 t3 t4 t5

FIG. 23

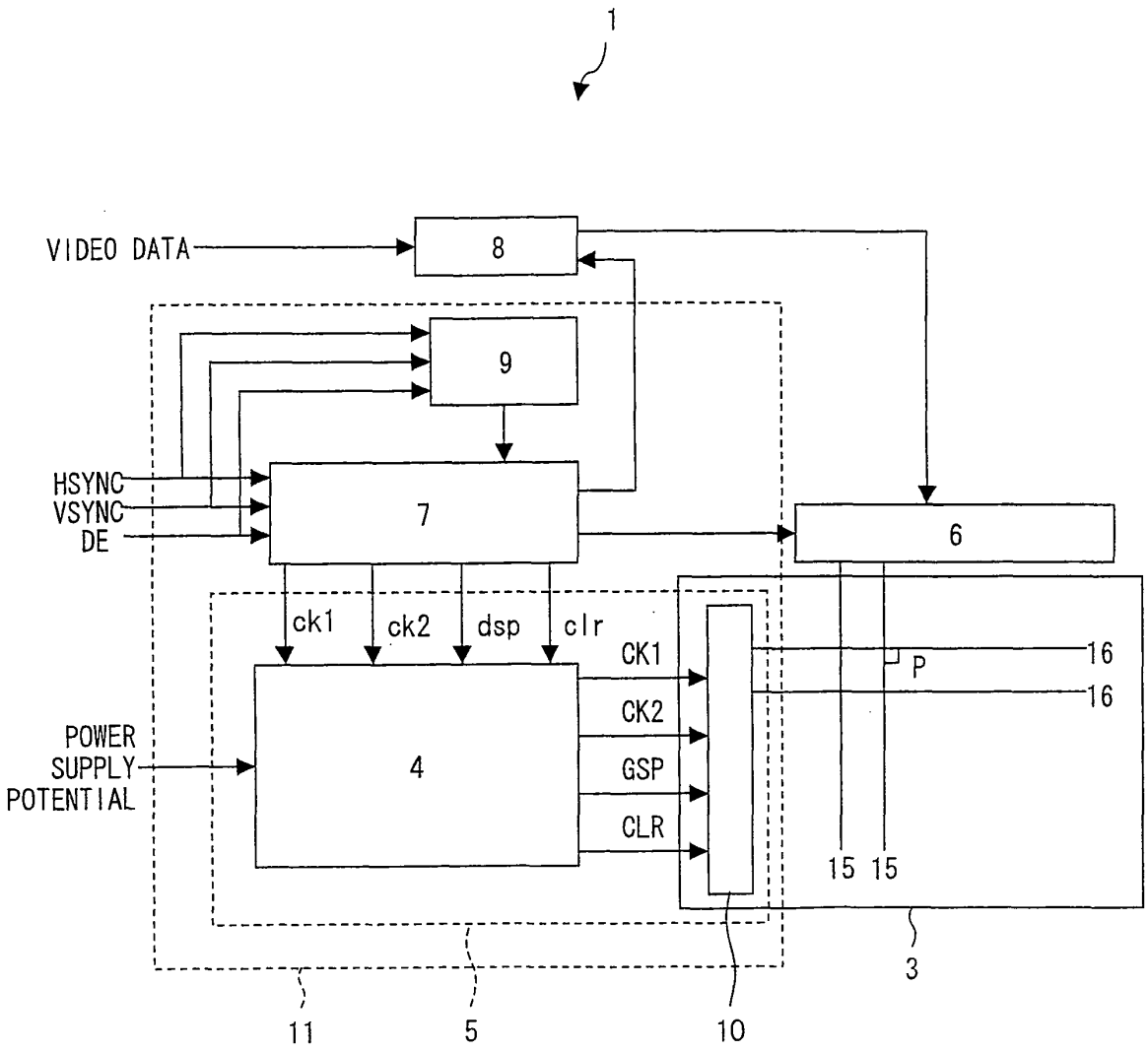

1
VIDEO DATA
8
9
HSYNC
VSYNC
DE
7
6
ck1
ck2
dsp
clr
CK1
CK2
GSP
CLR
P
16
16
POWER
SUPPLY
POTENTIAL
4
15 15
3
11
5
10

FIG. 24

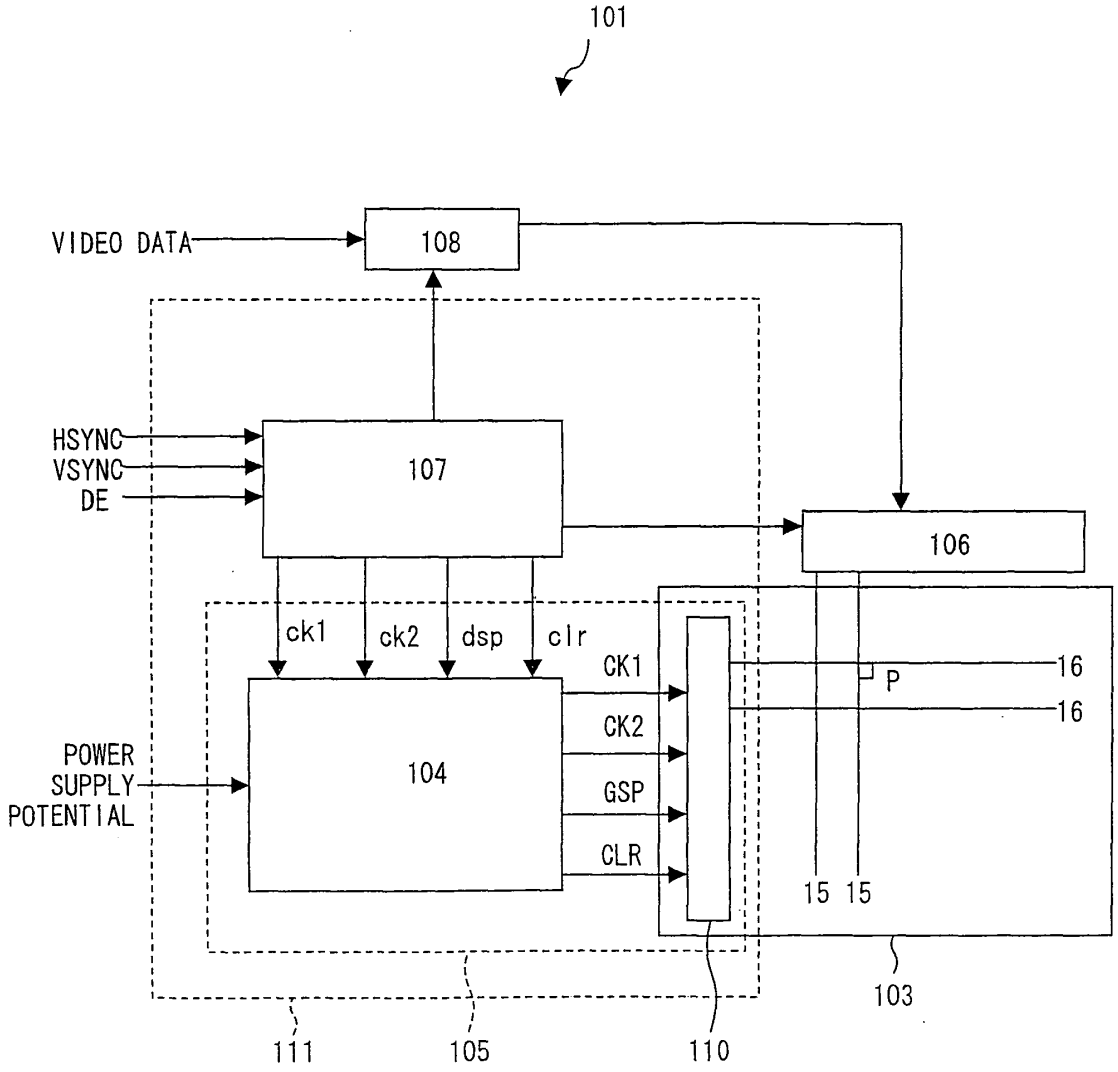

101
VIDEO DATA
108
HSYNC
VSYNC
DE
107
106
ck1
ck2
dsp
clr
CK1
CK2
GSP
CLR
16
16
P
POWER
SUPPLY
POTENTIAL
104
15 15
103
111
105
110

FIG. 25

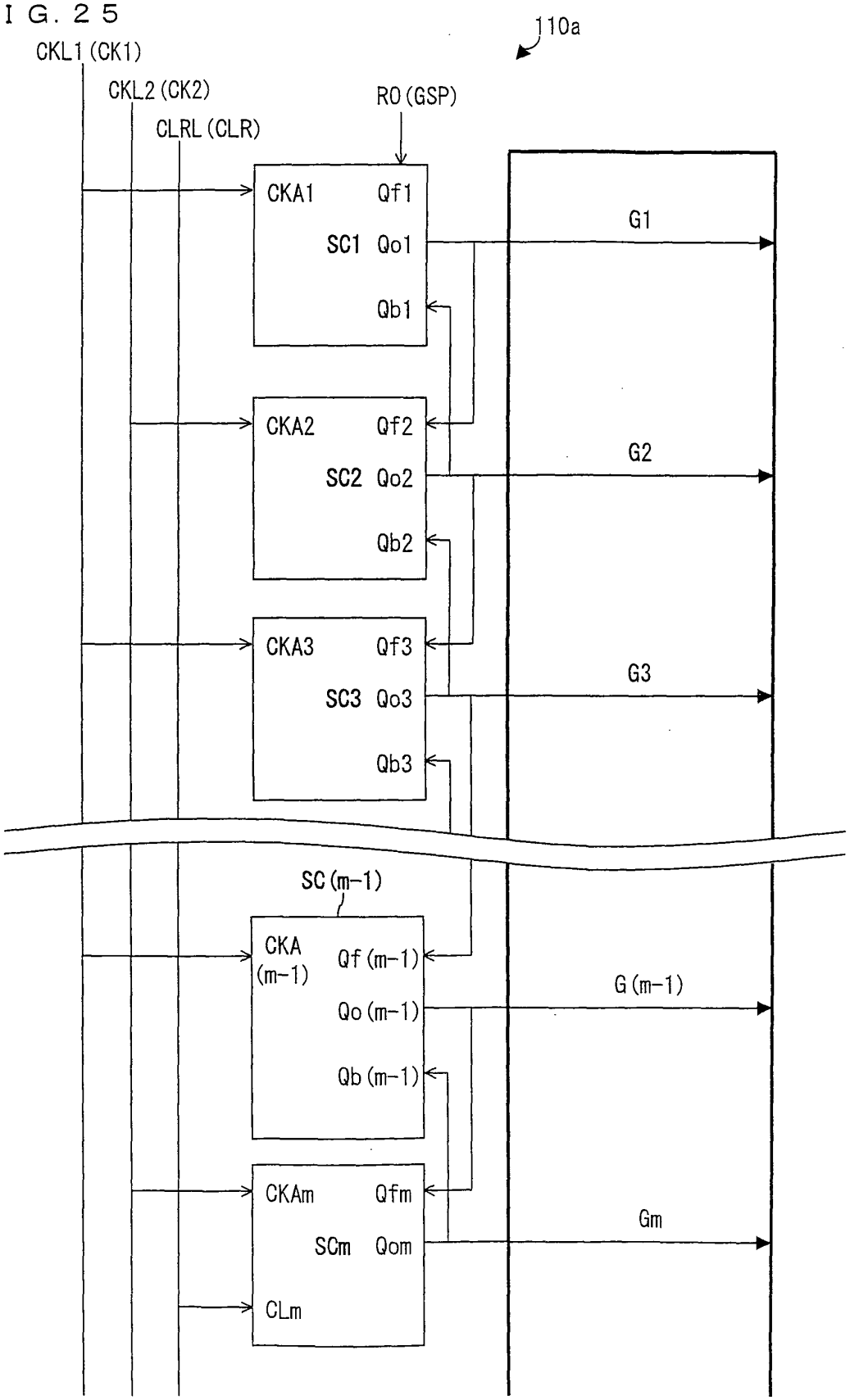

110a
CKL1 (CK1)
CKL2 (CK2)
CLRL (CLR)
RO (GSP)
CKA1
Qf1
SC1
Qo1
Qb1
G1
CKA2
Qf2
SC2
Qo2
Qb2
G2
CKA3
Qf3
SC3
Qo3
Qb3
G3
SC (m-1)
CKA (m-1)
Qf (m-1)
Qo (m-1)
Qb (m-1)
G (m-1)
CKAm
Qfm
SCm
Qom
CLm
Gm

FIG. 26

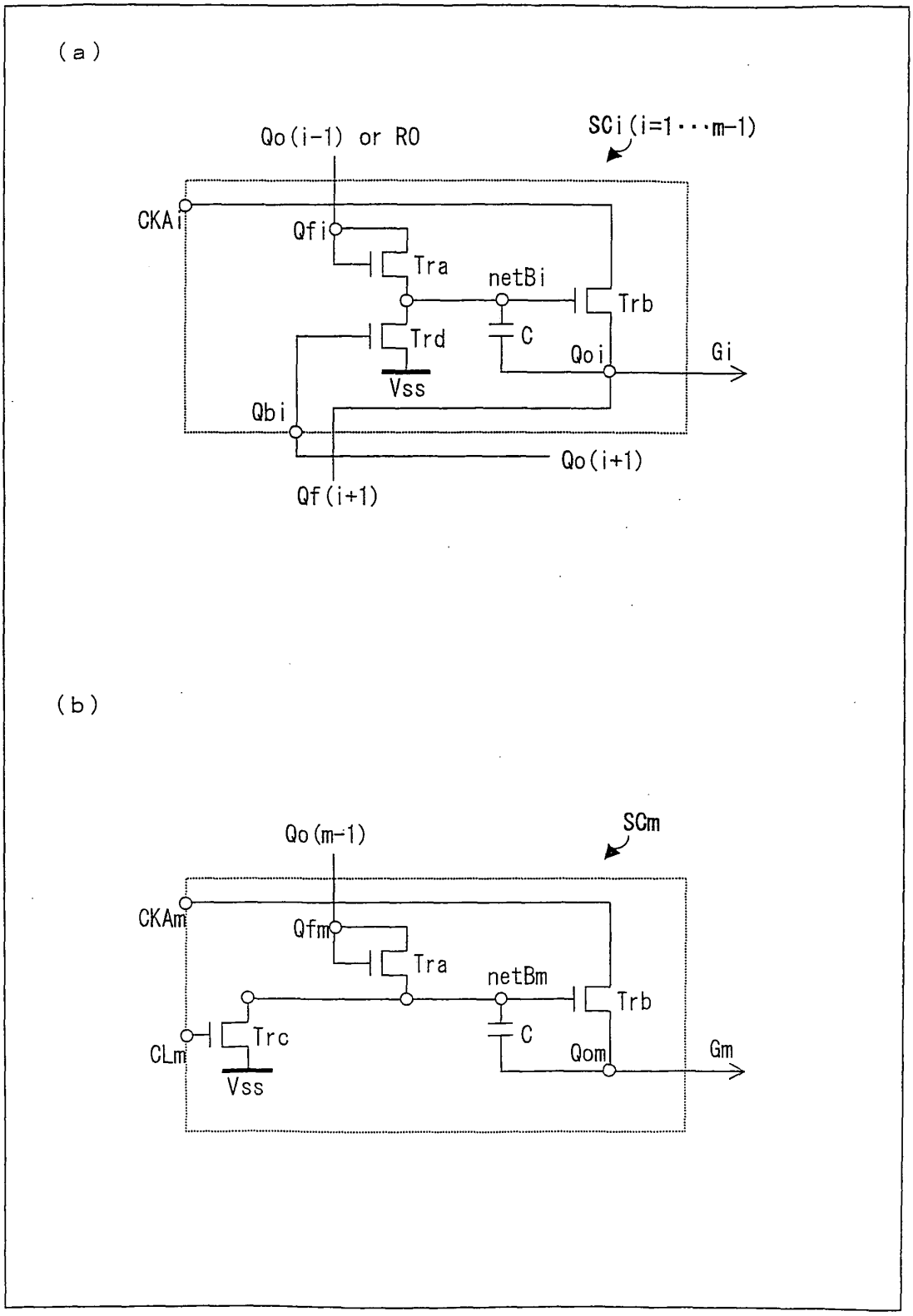

(a)
Qo(i-1) or RO
SCi(i=1・・・m-1)
CKAi
Qfi
Tra
netBi
Trb
Trd
C
Qoi
Gi
Vss
Qbi
Qo(i+1)
Qf(i+1)
(b)
Qo(m-1)
SCm
CKAm
Qfm
Tra
netBm
Trb
Trc
C
CLm
Qom
Gm
Vss

FIG. 27

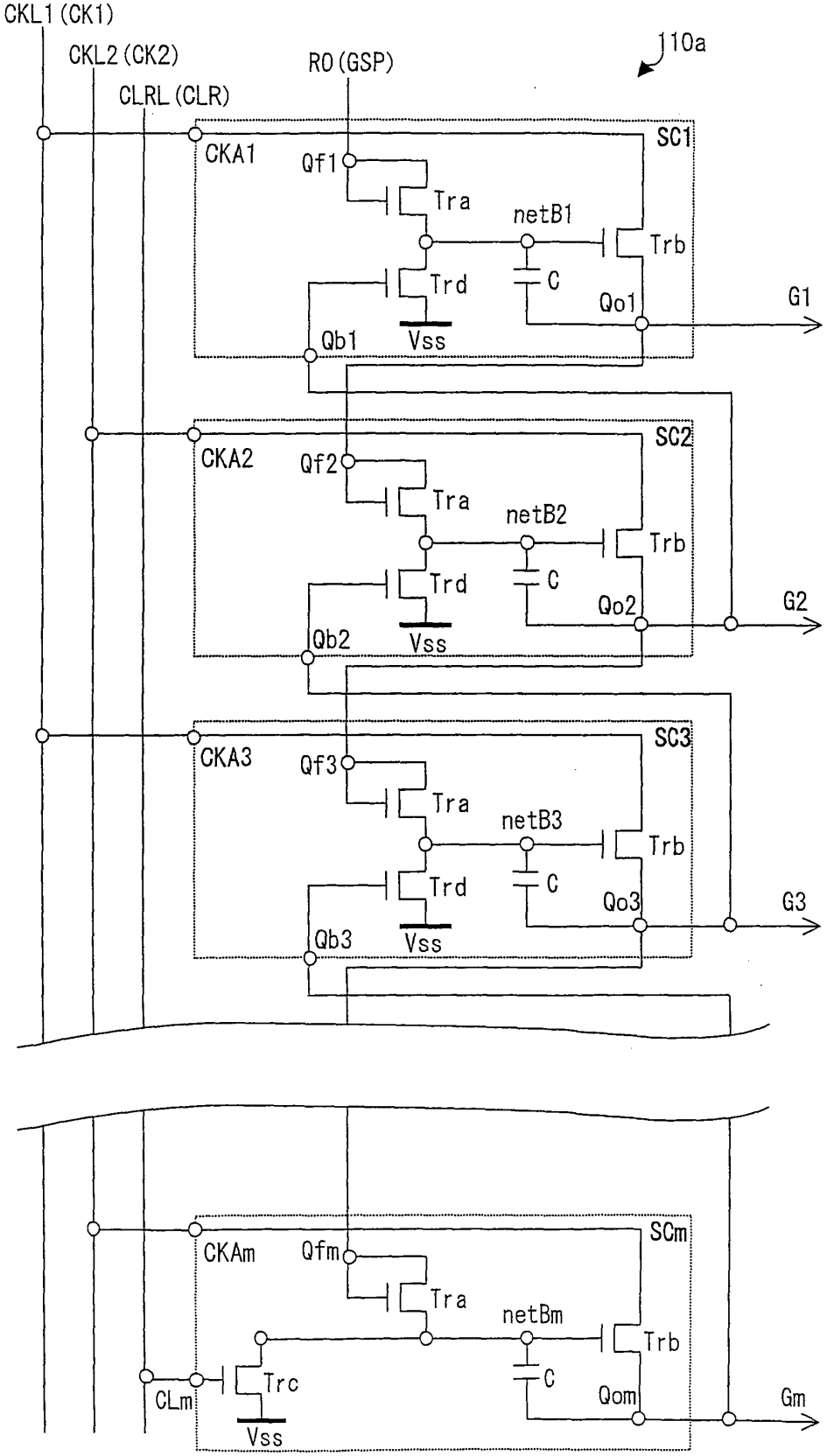

CKL1 (CK1)
CKL2 (CK2)
CLRL (CLR)
RO (GSP)
110a
SC1
CKA1
Qf1
Tra
netB1
Trb
Trd
C
Qo1
G1
Qb1
Vss
SC2
CKA2
Qf2
Tra
netB2
Trb
Trd
C
Qo2
G2
Qb2
Vss
SC3
CKA3
Qf3
Tra
netB3
Trb
Trd
C
Qo3
G3
Qb3
Vss
SCm
CKAm
Qfm
Tra
netBm
Trb
Trc
C
Qom
Gm
CLm
Vss

FIG. 28

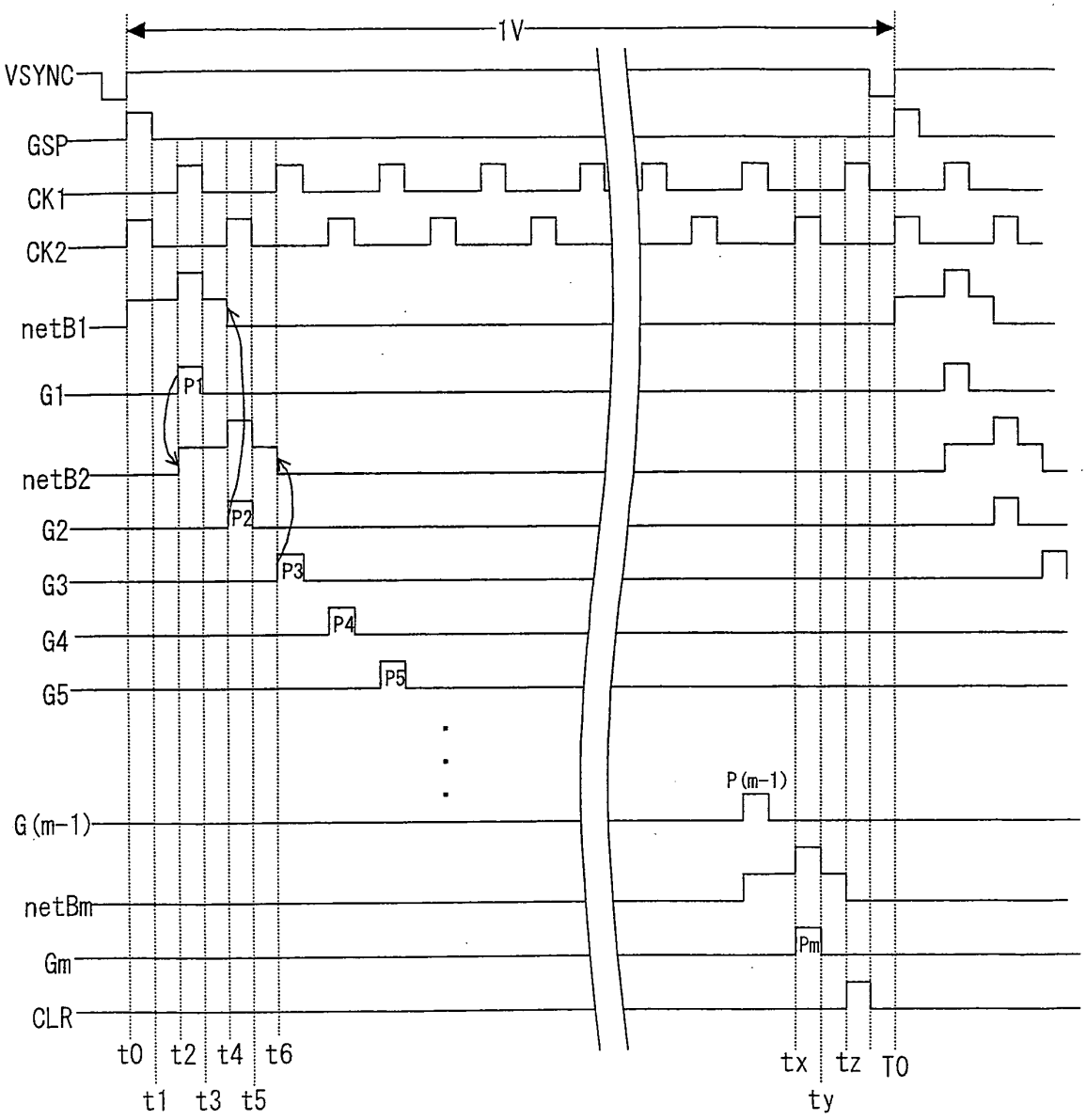

1V
VSYNC
GSP
CK1
CK2
netB1
G1
P1
netB2
G2
P2
G3
P3
G4
P4
G5
P5
P(m-1)
G(m-1)
netBm
Pm
Gm
CLR
t0
t1
t2
t3
t4
t5
t6
tx
ty
tz
T0

FIG. 29

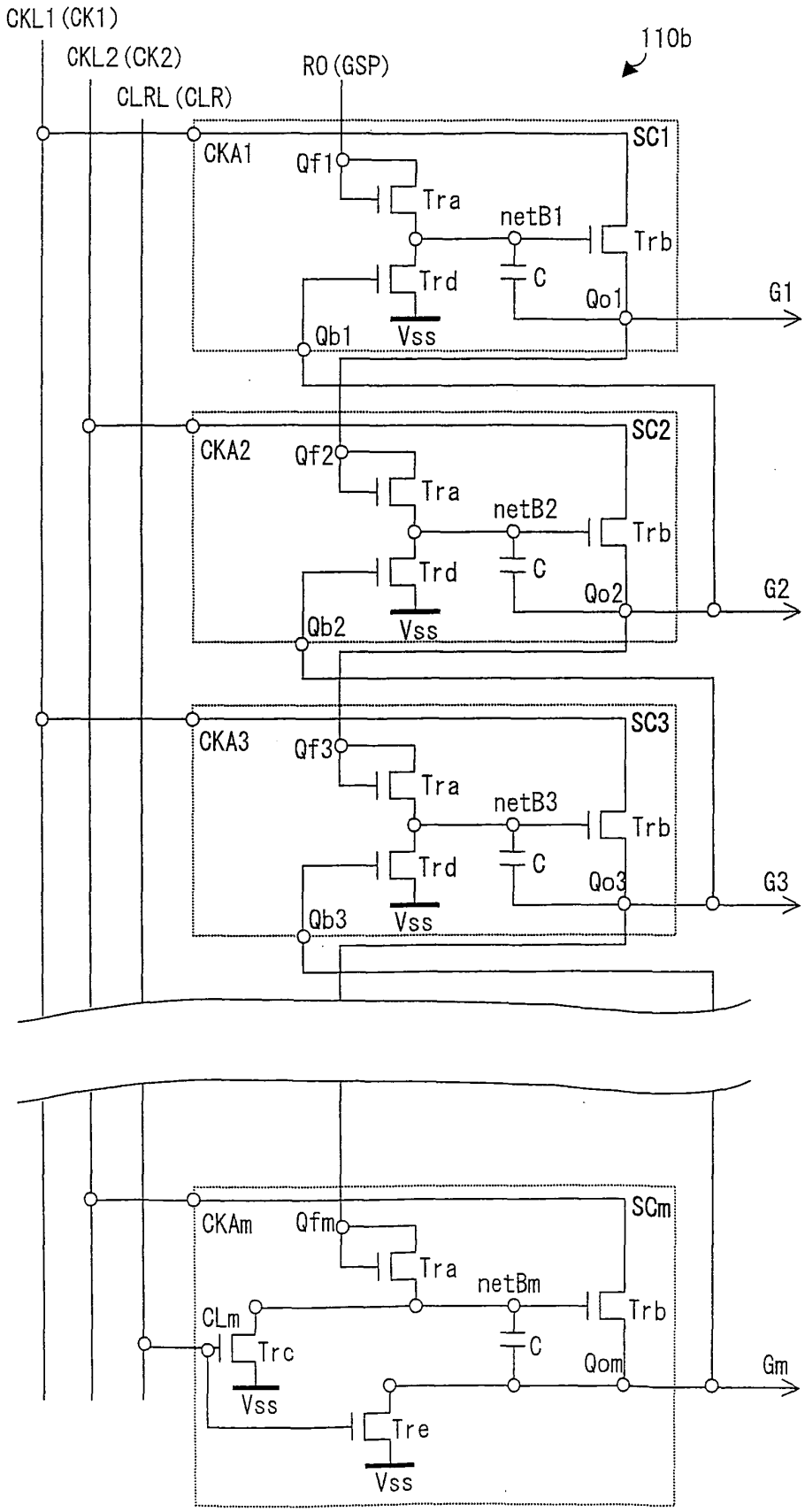
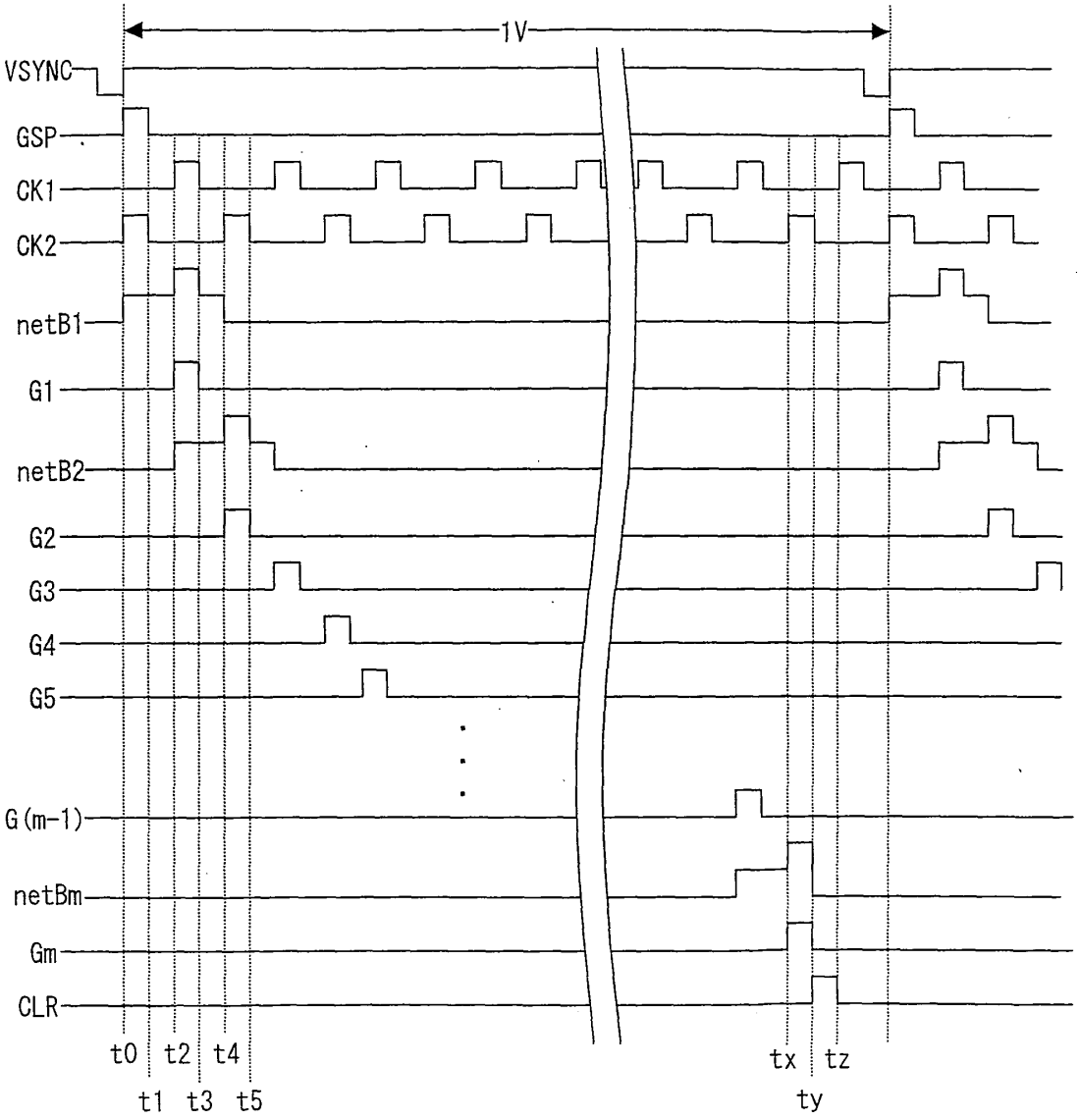

CKL1 (CK1)
CKL2 (CK2)
CLRL (CLR)
RO (GSP)
110b
SC1
CKA1
Qf1
Tra
netB1
Trb
Trd
C
Qo1
G1
Qb1
Vss
SC2
CKA2
Qf2
Tra
netB2
Trb
Trd
C
Qo2
G2
Qb2
Vss
SC3
CKA3
Qf3
Tra
netB3
Trb
Trd
C
Qo3
G3
Qb3
Vss
SCm
CKAm
Qfm
Tra
netBm
Trb
CLm
Trc
C
Qom
Gm
Vss
Tre
Vss

FIG. 30


1V
VSYNC
GSP
CK1
CK2
netB1
G1
netB2
G2
G3
G4
G5
G(m-1)
netBm
Gm
CLR
t0
t1
t2
t3
t4
t5
tx
ty
tz

F I G. 3 1

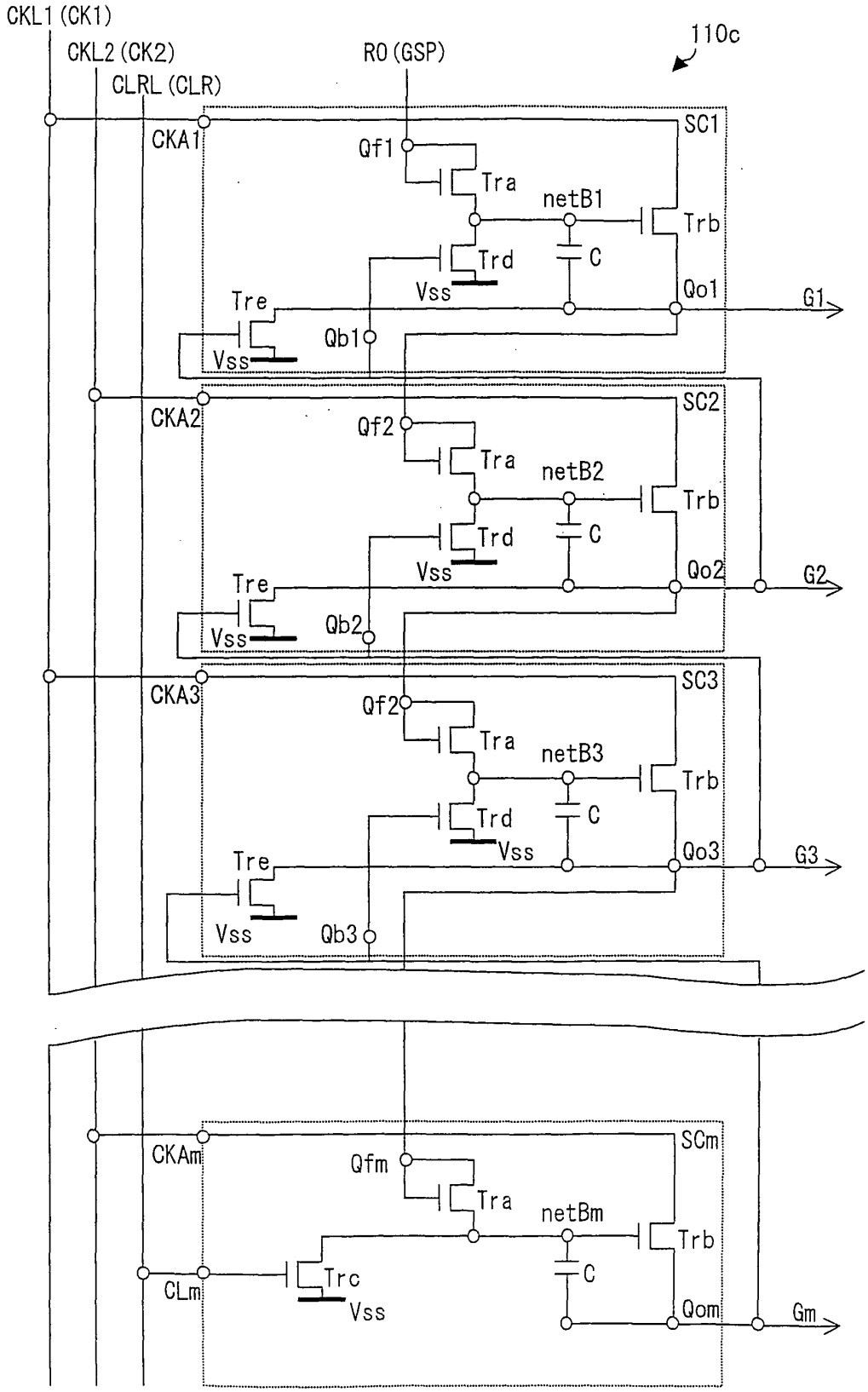

CKL1 (CK1)
CKL2 (CK2)
CLRL (CLR)
RO (GSP)
110c
CKA1
SC1
Qf1
Tra
netB1
Trb
Trd
C
Vss
Qo1
G1
Tre
Qb1
Vss
CKA2
SC2
Qf2
Tra
netB2
Trb
Trd
C
Vss
Qo2
G2
Tre
Qb2
Vss
CKA3
SC3
Qf2
Tra
netB3
Trb
Trd
C
Vss
Qo3
G3
Tre
Vss
Qb3
CKAm
SCm
Qfm
Tra
netBm
Trb
Trc
C
CLm
Vss
Qom
Gm

FIG. 32

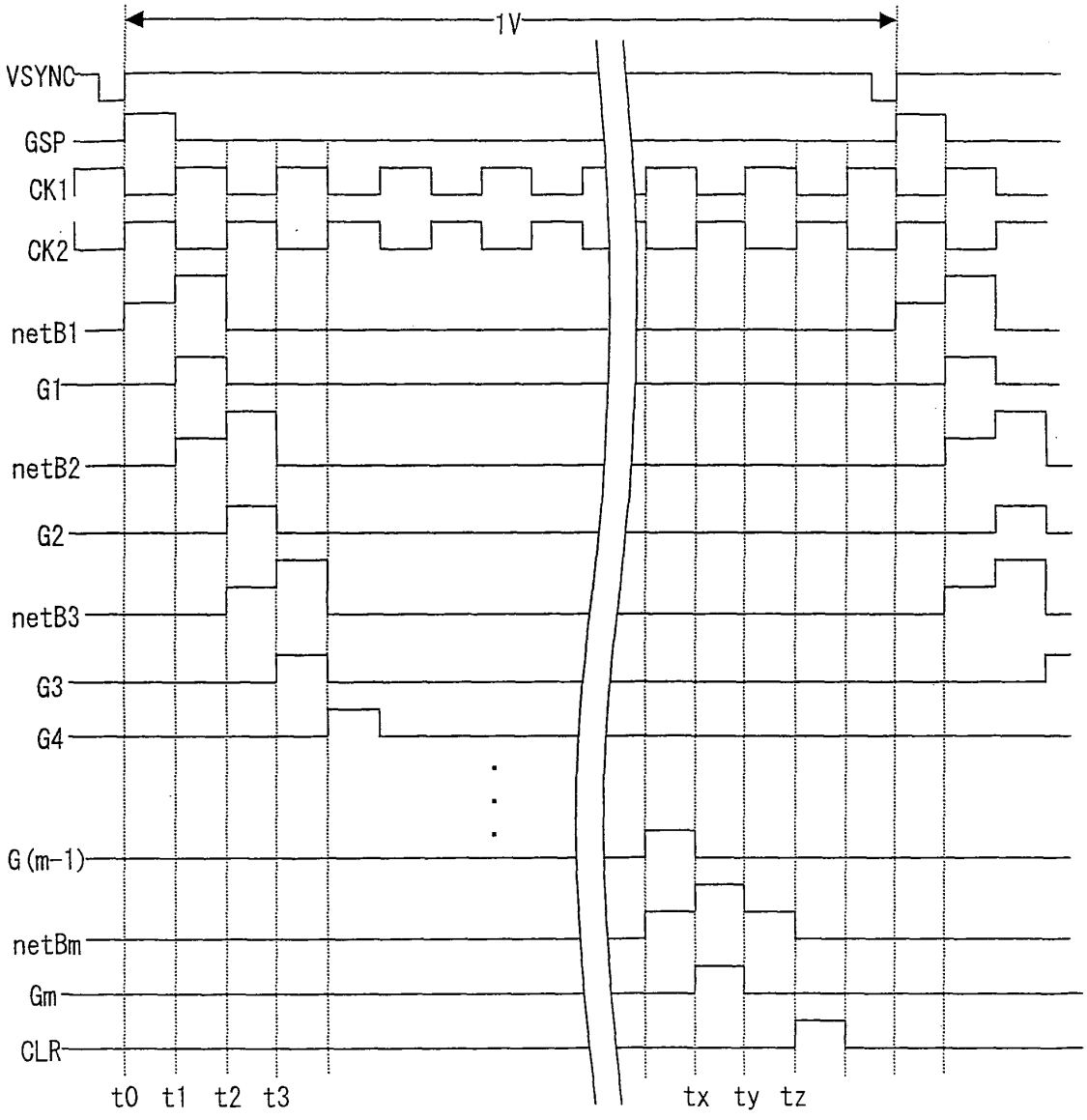

1V
VSYNC
GSP
CK1
CK2
netB1
G1
netB2
G2
netB3
G3
G4
G(m-1)
netBm
Gm
CLR
t0
t1
t2
t3
tx
ty
tz

FIG. 33

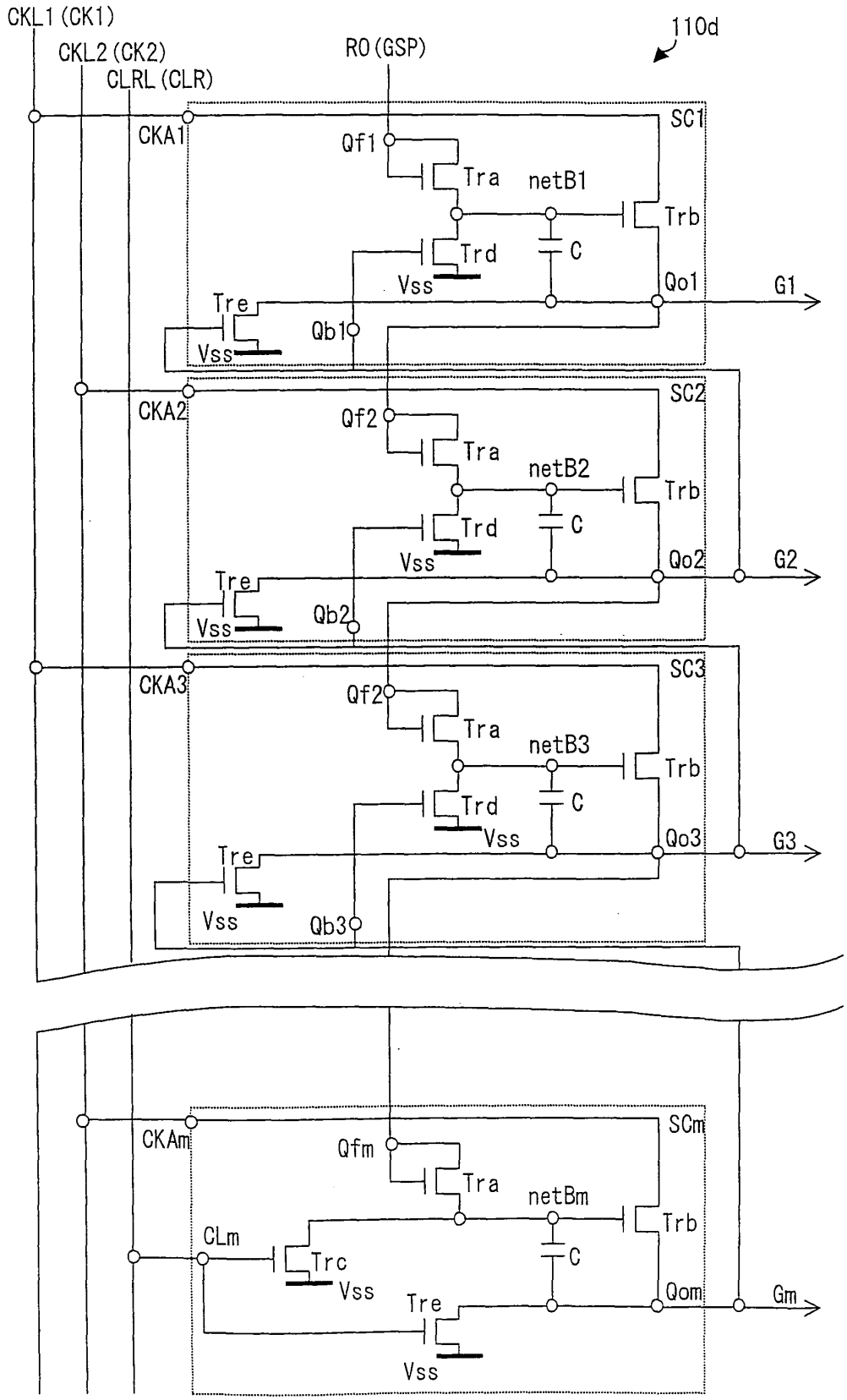

CKL1 (CK1)
CKL2 (CK2)
CLRL (CLR)
RO (GSP)
110d
SC1
CKA1
Qf1
Tra
netB1
Trb
Trd
C
Vss
Qo1
G1
Tre
Qb1
Vss
SC2
CKA2
Qf2
Tra
netB2
Trb
Trd
C
Vss
Qo2
G2
Tre
Qb2
Vss
SC3
CKA3
Qf2
Tra
netB3
Trb
Trd
C
Vss
Qo3
G3
Tre
Vss
Qb3
SCm
CKAm
Qfm
Tra
netBm
Trb
CLm
Trc
Vss
C
Qom
Gm
Tre
Vss

FIG. 34

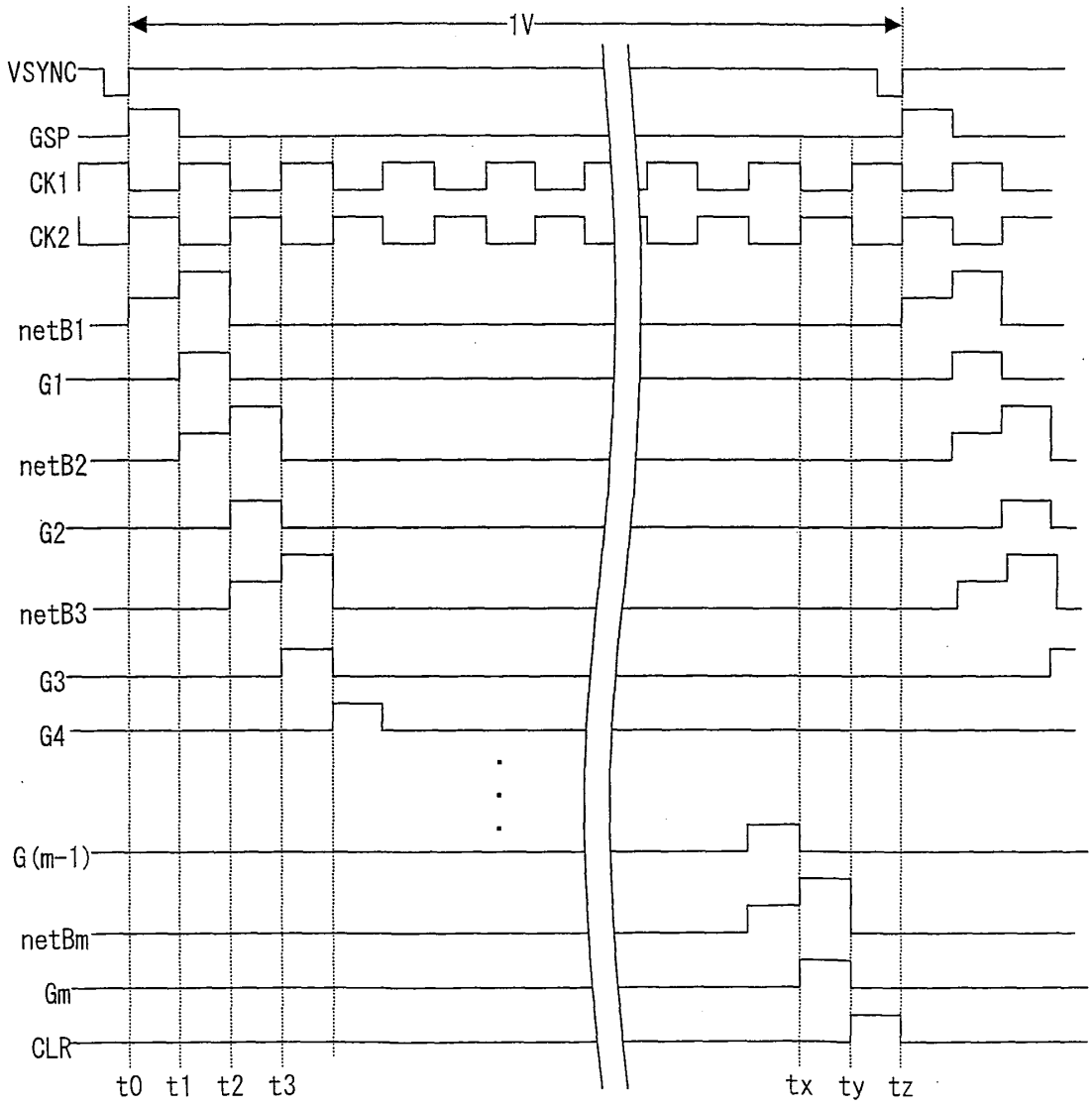

1V
VSYNC
GSP
CK1
CK2
netB1
G1
netB2
G2
netB3
G3
G4
G(m-1)
netBm
Gm
CLR
t0
t1
t2
t3
tx
ty
tz

FIG. 35

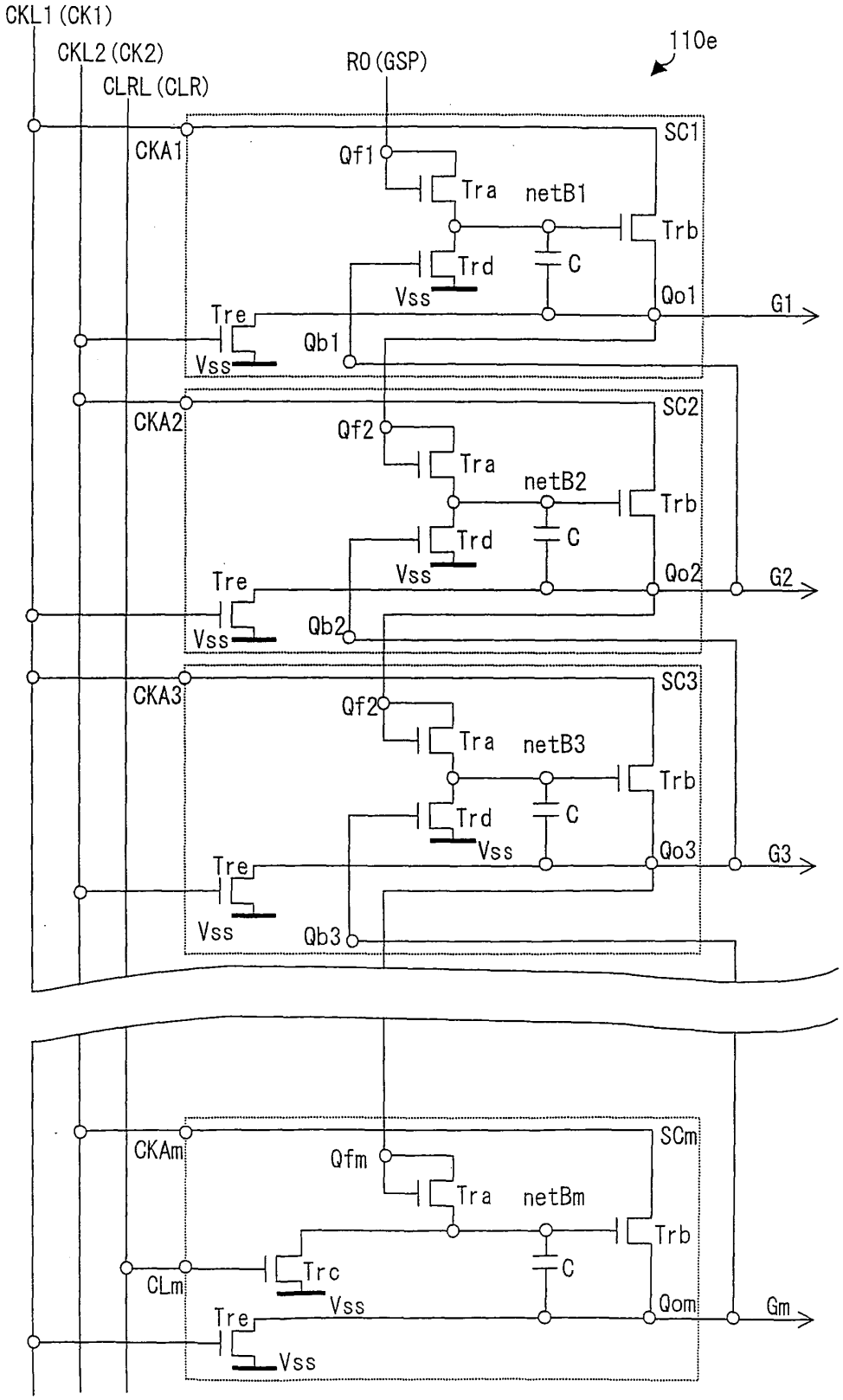

CKL1 (CK1)
CKL2 (CK2)
CLRL (CLR)
RO (GSP)
110e
SC1
CKA1
Qf1
Tra
netB1
Trb
Trd
C
Vss
Qo1
G1
Tre
Qb1
Vss
SC2
CKA2
Qf2
Tra
netB2
Trb
Trd
C
Vss
Qo2
G2
Tre
Qb2
Vss
SC3
CKA3
Qf2
Tra
netB3
Trb
Trd
C
Vss
Qo3
G3
Tre
Vss
Qb3
SCm
CKAm
Qfm
Tra
netBm
Trb
Trc
C
CLm
Vss
Qom
Gm
Tre
Vss

FIG. 36

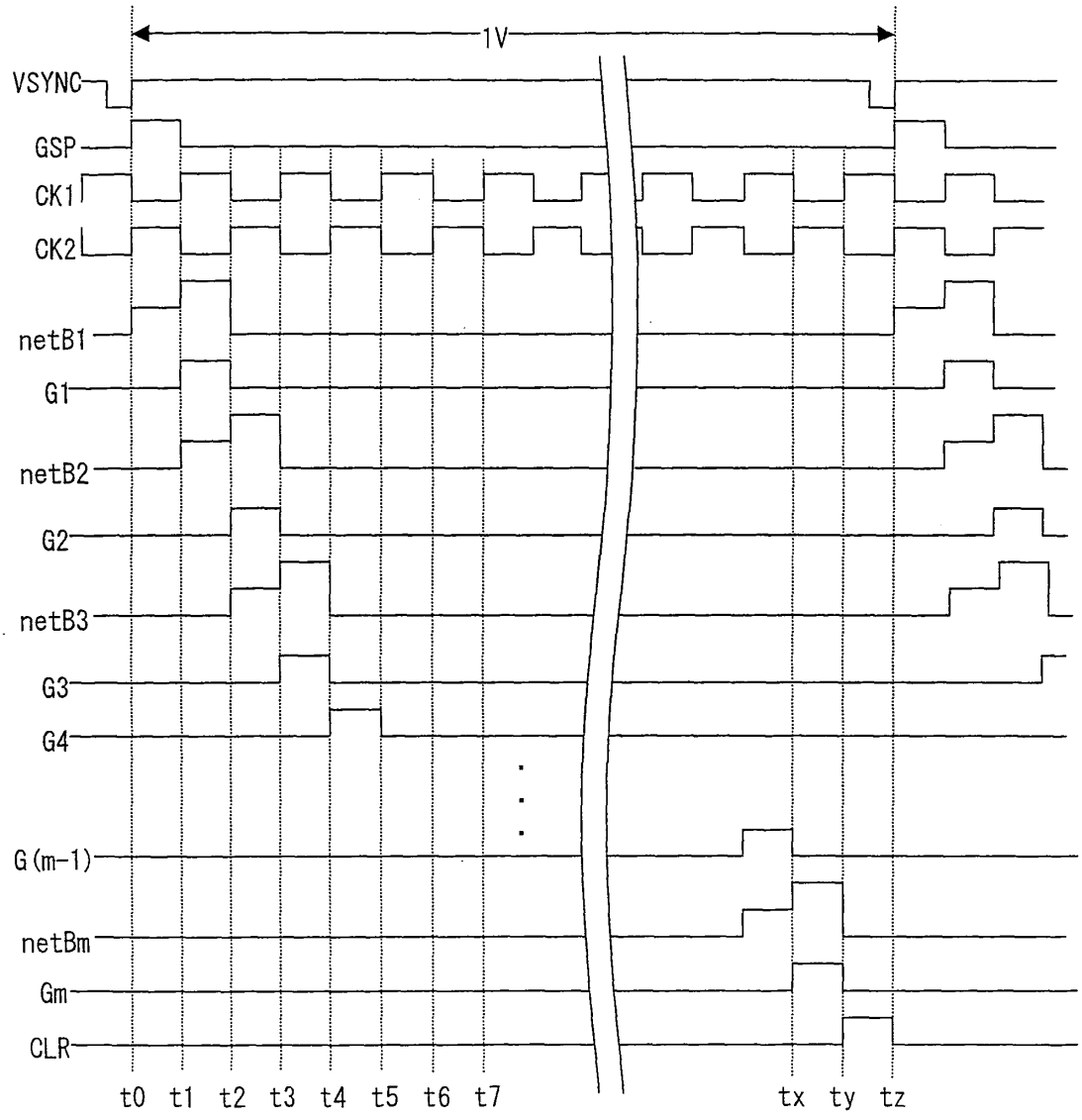

1V
VSYNC
GSP
CK1
CK2
netB1
G1
netB2
G2
netB3
G3
G4
G(m-1)
netBm
Gm
CLR
t0 t1 t2 t3 t4 t5 t6 t7
tx ty tz

FIG. 37

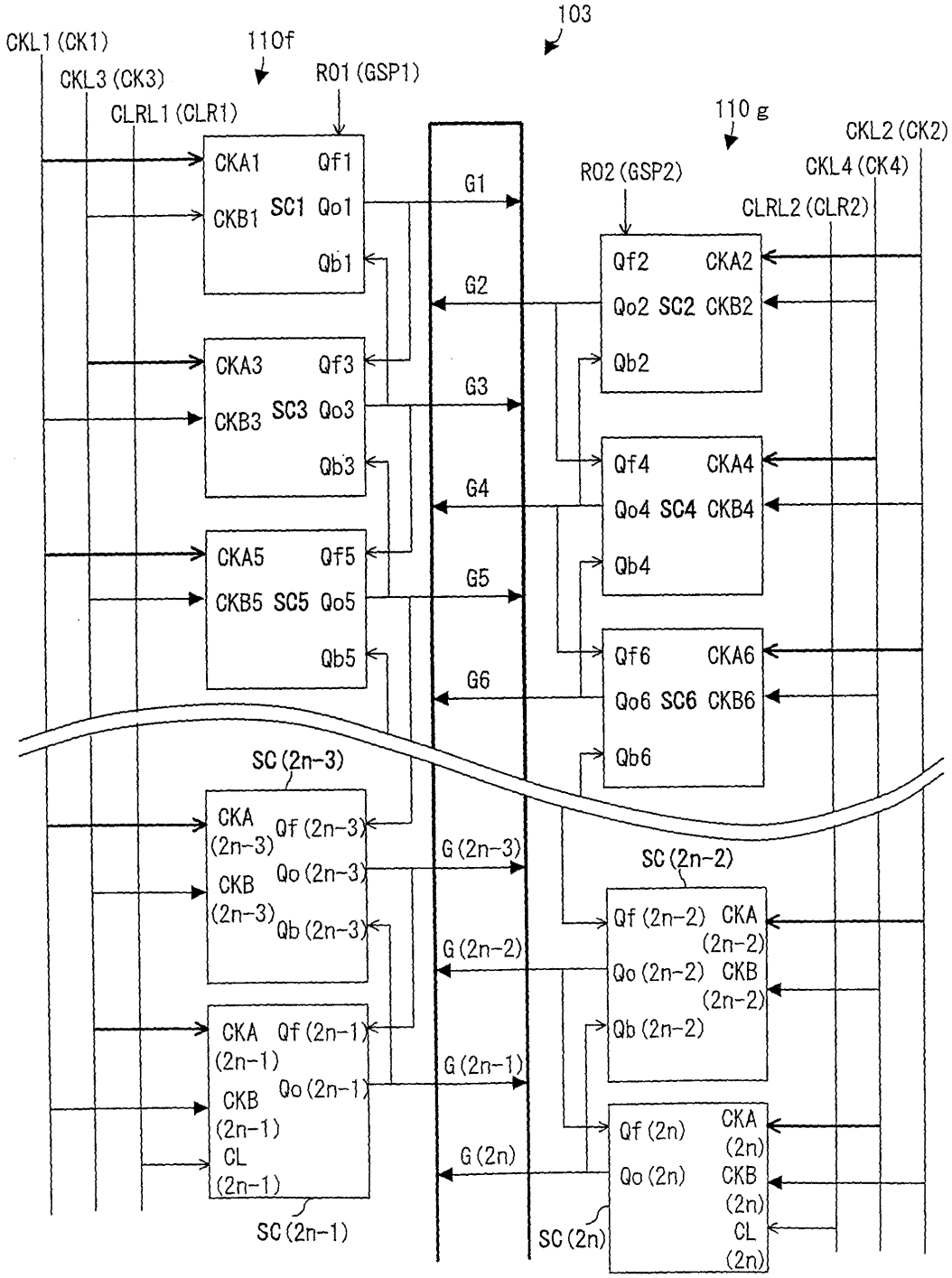

103
CKL1 (CK1)
110f
CKL3 (CK3)
RO1 (GSP1)
CLRL1 (CLR1)
110 g
CKL2 (CK2)
CKL4 (CK4)
RO2 (GSP2)
CLRL2 (CLR2)
CKA1
Qf1
CKB1
SC1
Qo1
Qb1
CKA3
Qf3
CKB3
SC3
Qo3
Qb3
CKA5
Qf5
CKB5
SC5
Qo5
Qb5
Qf2
CKA2
Qo2
SC2
CKB2
Qb2
Qf4
CKA4
Qo4
SC4
CKB4
Qb4
Qf6
CKA6
Qo6
SC6
CKB6
Qb6
G1
G2
G3
G4
G5
G6
SC (2n-3)
CKA (2n-3)
Qf (2n-3)
CKB (2n-3)
Qo (2n-3)
Qb (2n-3)
CKA (2n-1)
Qf (2n-1)
CKB (2n-1)
Qo (2n-1)
CL (2n-1)
SC (2n-1)
G (2n-3)
G (2n-2)
G (2n-1)
G (2n)
SC (2n-2)
Qf (2n-2)
CKA (2n-2)
Qo (2n-2)
CKB (2n-2)
Qb (2n-2)
Qf (2n)
CKA (2n)
Qo (2n)
CKB (2n)
CL (2n)
SC (2n)

FIG. 38

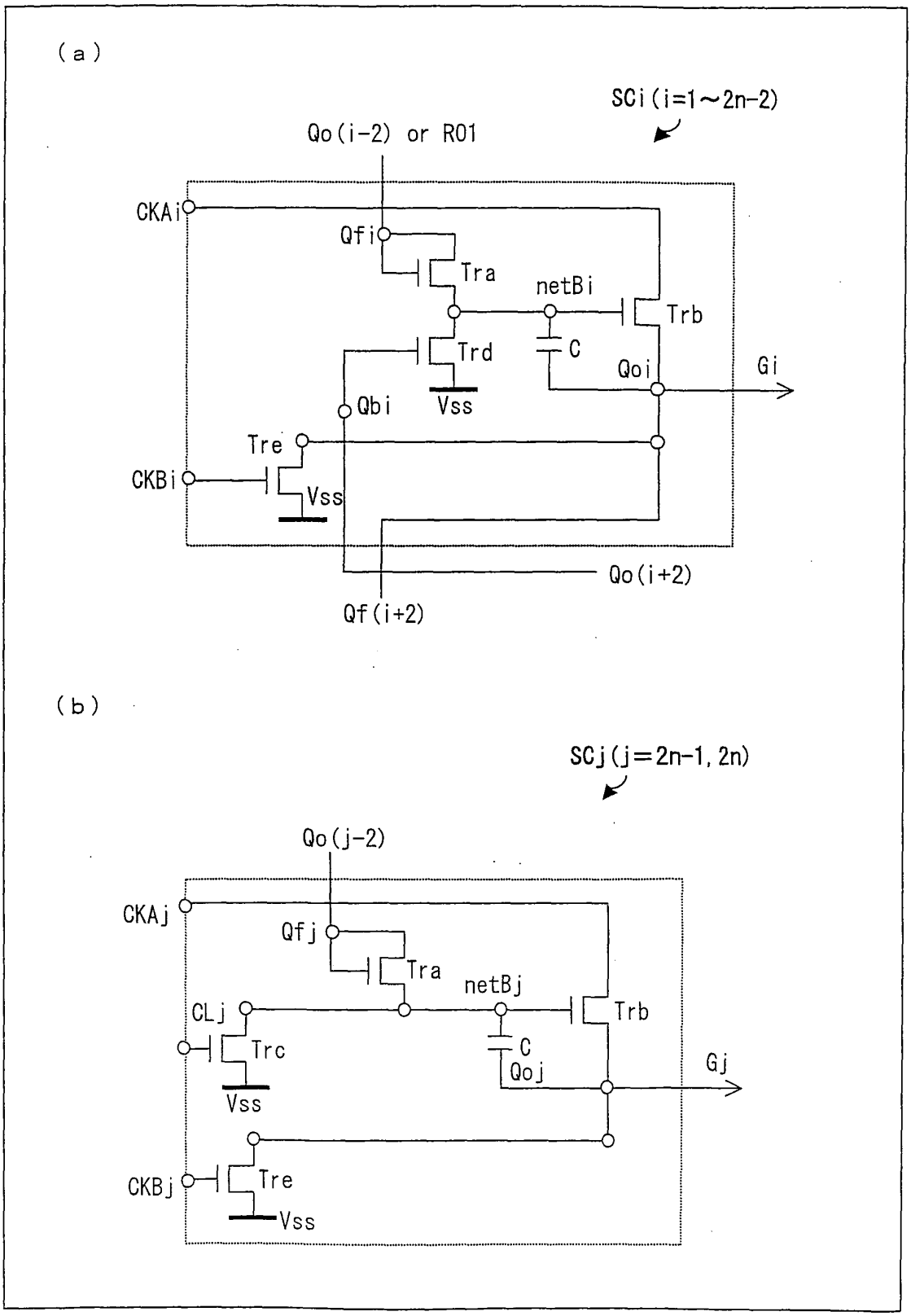

(a)
SCi(i=1～2n-2)
Qo(i-2) or RO1
CKAi
Qfi
Tra
netBi
Trb
Trd
C
Qoi
Gi
Qbi
Vss
Tre
CKBi
Vss
Qo(i+2)
Qf(i+2)
(b)
SCj(j=2n-1, 2n)
Qo(j-2)
CKAj
Qfj
Tra
netBj
CLj
Trb
Trc
C
Qoj
Gj
Vss
CKBj
Tre
Vss

FIG. 39

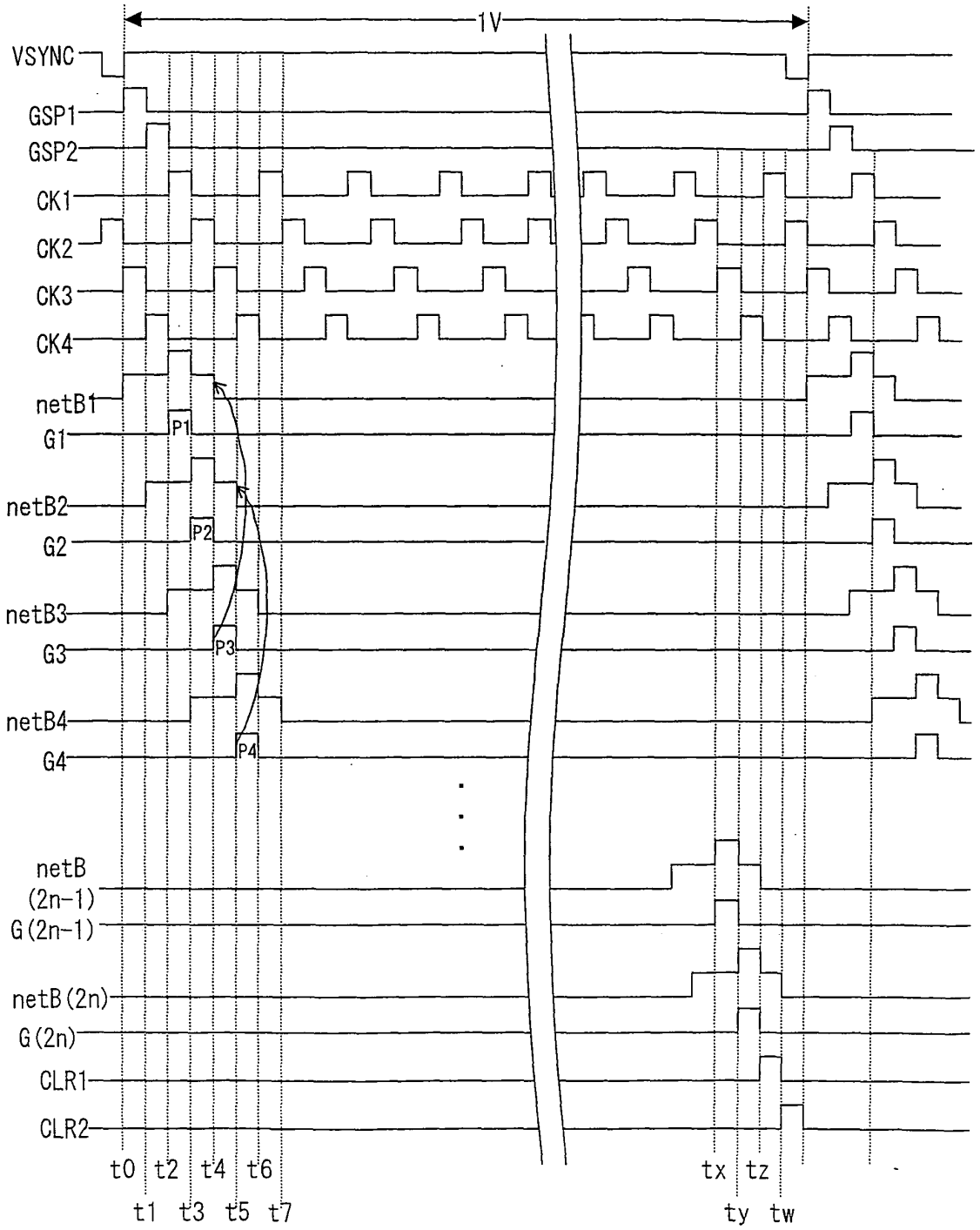

1V
VSYNC
GSP1
GSP2
CK1
CK2
CK3
CK4
netB1
G1
netB2
G2
netB3
G3
netB4
G4
P1
P2
P3
P4
netB (2n-1)
G(2n-1)
netB(2n)
G(2n)
CLR1
CLR2
t0
t1
t2
t3
t4
t5
t6
t7
tx
ty
tz
tw

FIG. 40

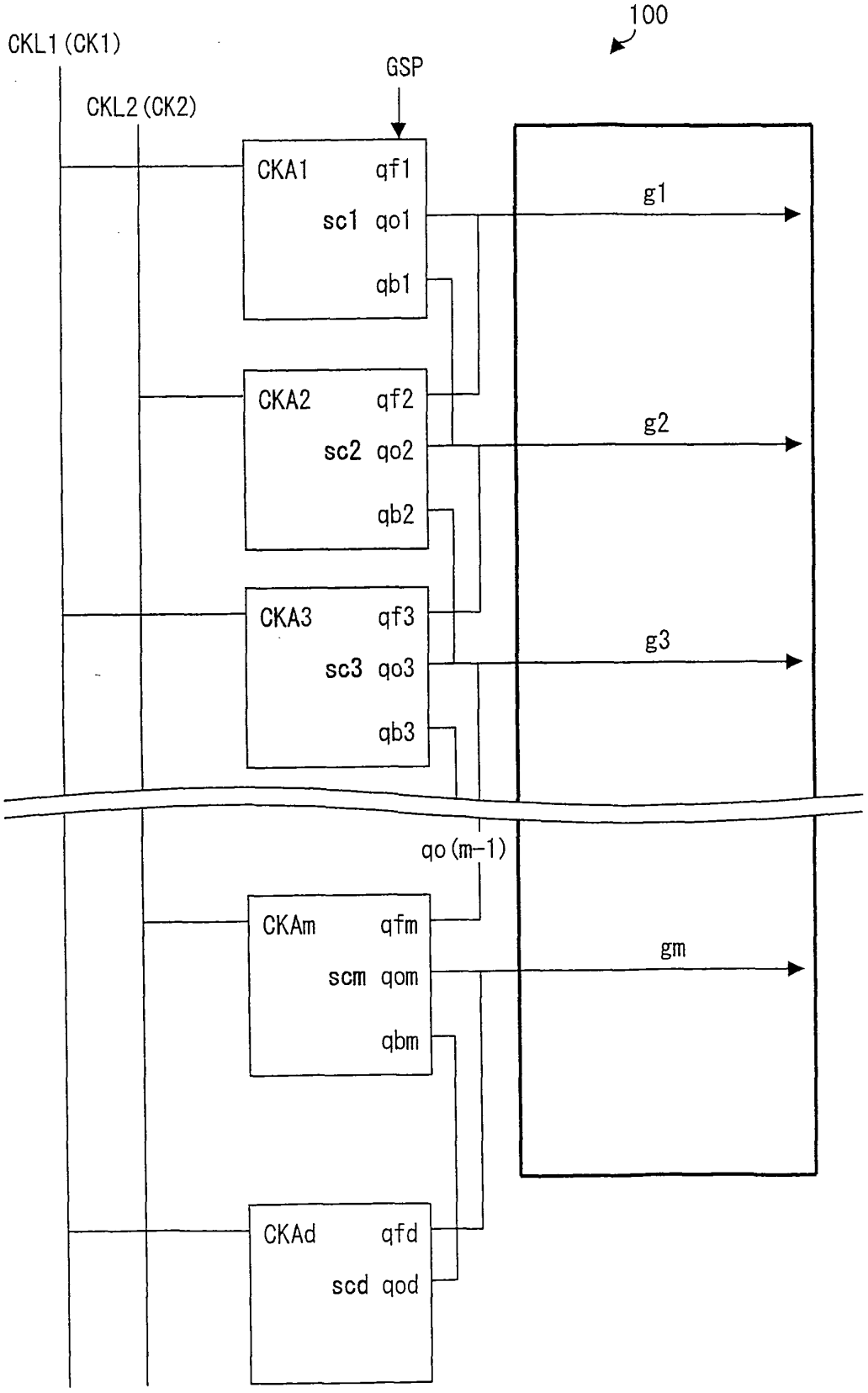

100
CKL1 (CK1)
CKL2 (CK2)
GSP
CKA1
qf1
sc1
qo1
qb1
g1
CKA2
qf2
sc2
qo2
qb2
g2
CKA3
qf3
sc3
qo3
qb3
g3
qo (m-1)
CKAm
qfm
scm
qom
qbm
gm
CKAd
qfd
scd
qod

FIG. 41

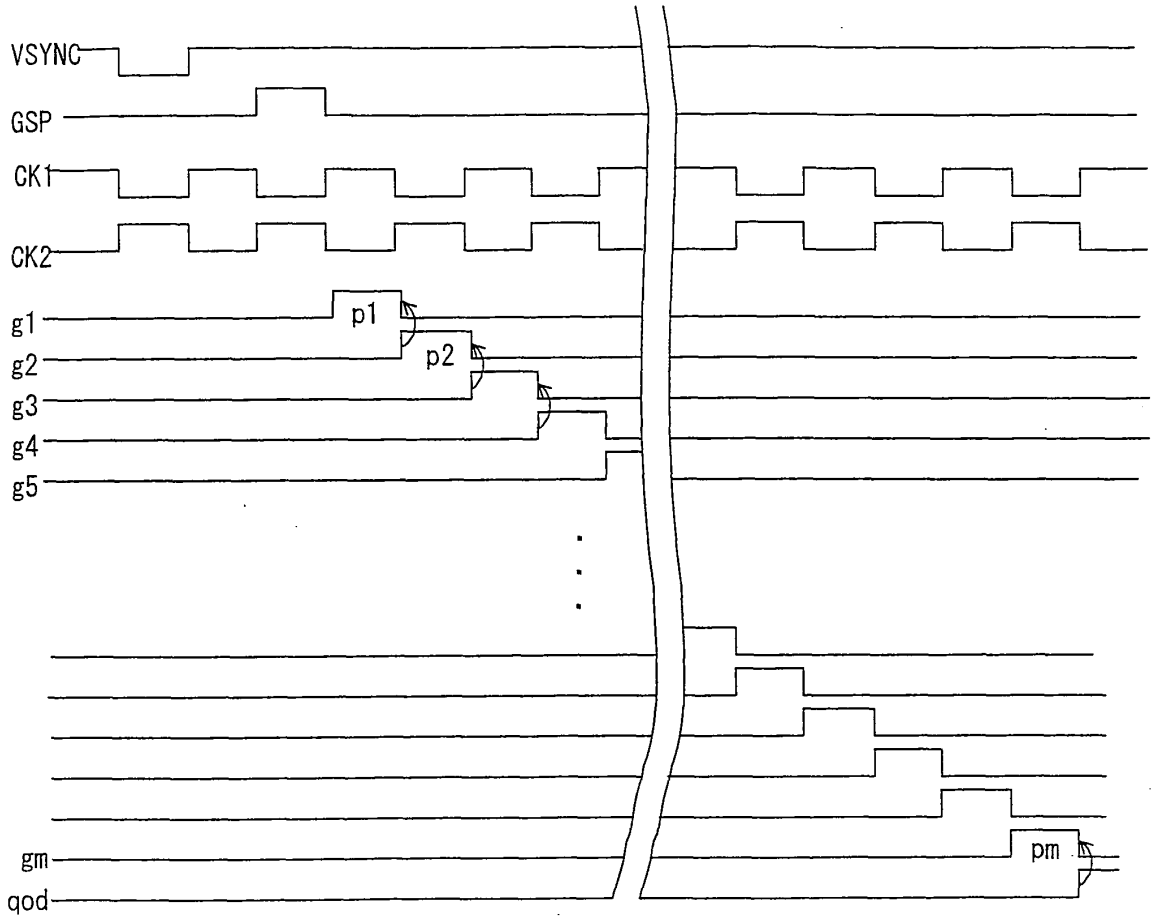
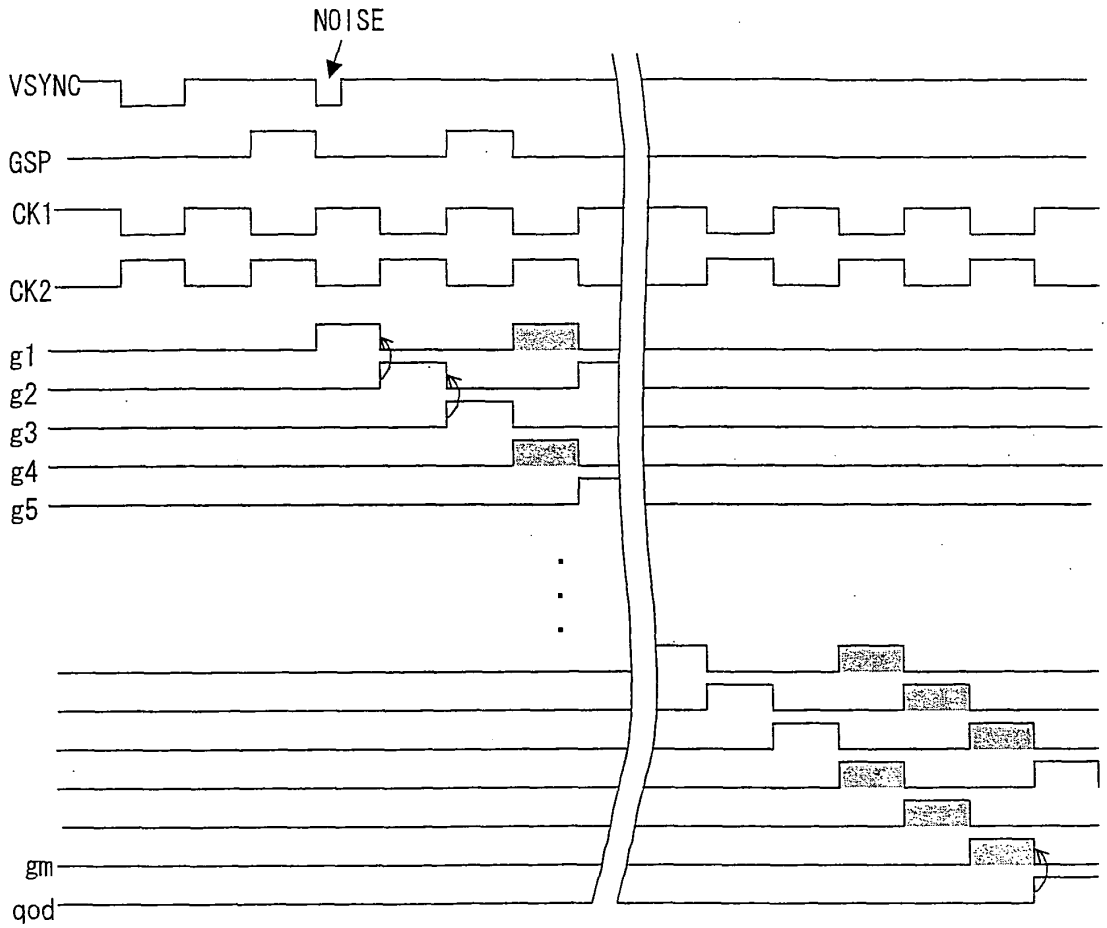


FIG. 42



INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2008/072931

A. CLASSIFICATION OF SUBJECT MATTER
G09G3/36(2006.01)i, *G02F1/133*(2006.01)i, *G09G3/20*(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G09G3/36, G02F1/133, G09G3/20

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1922-1996 Jitsuyo Shinan Toroku Koho 1996-2009
Kokai Jitsuyo Shinan Koho 1971-2009 Toroku Jitsuyo Shinan Koho 1994-2009

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 99/40561 A1 (Seiko Epson Corp.), 12 August, 1999 (12.08.99), Description, page 37, lines 14 to 26 & JP 2001-125071 A & US 6522319 B1 & EP 974952 A1	1-27,32-34
A	JP 2003-167545 A (Sharp Corp.), 13 June, 2003 (13.06.03), Par. Nos. [0007] to [0008], [0059] (Family: none)	1-27,32-34
A	JP 2007-202126 A (Semiconductor Energy Laboratory Co., Ltd.), 09 August, 2007 (09.08.07), Figs. 1 to 2, 5 to 6; Par. Nos. [0113] to [0124] & US 2007/0148793 A1 & KR 10-2007-0070074 A	1-27,32-34

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
02 March, 2009 (02.03.09)	17 March, 2009 (17.03.09)
Name and mailing address of the ISA/ Japanese Patent Office Facsimile No.	Authorized officer Telephone No.

Form PCT/ISA/210 (second sheet) (April 2007)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2008/072931

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

The invention of claims 1 - 27 and 32 - 34 relates to a display panel driving circuit, a shift register and a display device driving method, in which a clear signal is inputted to unit circuits constituting a shift register and in which said clear signal is activated, in the case where at least a synchronizing signal is abnormal, so that no pulse is subsequently outputted from said shift register till the start of the next vertical scanning period.

The invention of claims 28 - 31 and 35 - 36 relates to a display panel driving circuit, a shift register and a display device driving method, in which a clear signal is inputted to a unit circuit to become a final stage constituting a shift register, (continued to extra sheet)

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
1 - 27 and 32 - 34.

Remark on Protest

the

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

Form PCT/ISA/210 (continuation of first sheet (2)) (April 2007)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2008/072931

Continuation of Box No.III of continuation of first sheet(2)

and in which said clear signal is activated after the pulses are outputted from the final stage, so that the signal line selecting signals from the final stage are kept inactive.

Moreover, it is not considered that those two invention groups are correlated to form a single general inventive concept.

Form PCT/ISA/210 (extra sheet) (April 2007)

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- JP 2001273785 A **[0010]**
- JP 2006024350 A **[0011]**
- JP 2007114771 A **[0012]**
- JP 2003167545 A **[0061]**

专利名称(译)	显示面板驱动电路，液晶显示装置，移位寄存器，液晶面板和显示装置驱动方法		
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申请(专利权)人(译)	夏普株式会社		
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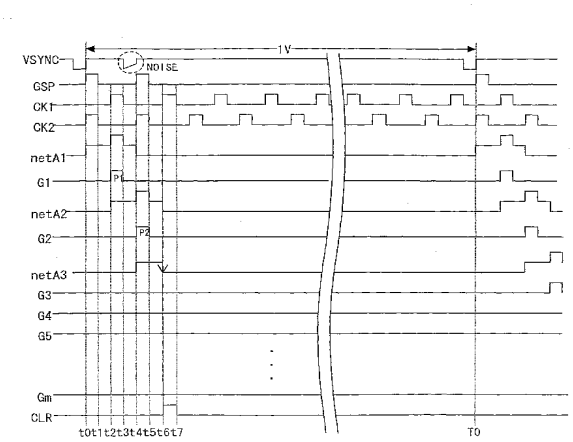
优先权	2008072420 2008-03-19 JP		
其他公开文献	EP2256721A4		
外部链接	Espacenet		

摘要(译)

显示面板驱动电路包括由分级连接的单元电路（SC1至SCm）构成的移位寄存器（10a）。单元电路分别产生信号线选择信号（G1至Gm），该信号线选择信号在相应的特定时间段内被激活以形成相应的脉冲，并且脉冲从各个单元电路依次输出。从第一阶段到结束阶段的序数。每个单元电路接收（i）基于从显示面板驱动电路外部接收的同步信号产生的时钟信号（CK1和CK2），（ii）基于同步信号产生的起始脉冲信号（GSP），或者在与其自身级不同的级中产生的信号线选择信号，以及（iii）清除信号（CLR）。在同步信号中包括异常的情况下使清除信号（CLR）有效，并且从移位寄存器（10a）输出脉冲直到后续的垂直扫描周期开始。该配置实现了显示面板驱动电路，其防止显示无序或抑制给予电源的负载的增加，其中每一个都发生在同步信号（VSYNC，HSYNC或DE）中包括异常的情况下。

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