(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 2 048 538 B1

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
27.02.2013 Bulletin 2013/09

(21) Application number: **08017550.8**

(22) Date of filing: **07.10.2008**

(51) Int Cl.:
G02F 1/1335 *(2006.01)* ***G02F 1/1362*** *(2006.01)*

(54) **Liquid crystal display device**

Flüssigkristallanzeigevorrichtung

Dispositif d'affichage à cristaux liquides

(84) Designated Contracting States:
AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MT NL NO PL PT RO SE SI SK TR

(30) Priority: **09.10.2007 JP 2007263030**

(43) Date of publication of application:
15.04.2009 Bulletin 2009/16

(73) Proprietors:
- **Hitachi Displays, Ltd.**
  Mobara-shi
  Chiba (JP)
- **Panasonic Liquid Crystal Display Co., Ltd.**
  Shikama-ku, Himeji-shi
  Hyogo
  672-8033 (JP)

(72) Inventor: **Ono, Kikuo**
Morabara-shi
Chiba (JP)

(74) Representative: **Kirschner, Klaus Dieter et al**
Puschmann Borchert Bardehle
Patentanwälte Partnerschaft
Postfach 10 12 31
80086 München (DE)

(56) References cited:
KR-A- 20060 119 399
US-A1- 2002 041 354
US-A1- 2002 085 149
US-A1- 2007 103 631

EP 2 048 538 B1

Printed by Jouve, 75001 PARIS (FR)

Description

[0001] The present invention relates to a liquid crystal display device, and in particular, to a technology which is effective when applied to an active matrix type TFT liquid crystal display device.

[0002] Conventional liquid crystal display devices having a liquid crystal display panel where a liquid crystal material is sealed between a pair of substrates include active matrix type TFT liquid crystal display devices. The above described active matrix type TFT liquid crystal display devices (hereinafter simply referred to as liquid crystal display devices) are used for monitors, such as televisions and PC's (personal computers), and displays for portable electronics, such as portable phones.

[0003] In the liquid crystal display panels used in the above described liquid crystal display devices, a number of scanning signal lines, a number of video signal lines, a number of TFT elements (active elements) and a number of pixel electrodes are provided on one substrate (hereinafter referred to as TFT substrate) from among the above described pair of substrates in such a manner that the set of pixels having the above described TFT elements and pixel electrodes connected to the above described TFT elements form a display region.

[0004] In addition, a light blocking film (which may be referred to as black matrix) and color filters, for example, are provided on the other substrate (hereinafter referred to as a facing substrate) from among the above described pair of substrates in the above described liquid crystal display panels. The above described light blocking film is formed of, for example, a conductor or an insulator in mesh form which divides the display region into microscopic regions for each pixel, and in general, extends in such locations as to overlap (face) scanning signal lines, TFT elements and video signal lines on the above described TFT substrate. In addition, the color filters are provided to liquid crystal display panels for color display, and in the case of an RGB type color liquid crystal display panel, for example, red (R), green (G) and blue (B) color filters are provided.

[0005] In addition, in the case where the above described liquid crystal display panel is of a drive system, which is referred to as a longitudinal electrical field drive system (for example, VA system or TN system), counter electrodes (which may also be referred to as common electrodes) which make pairs with the above described pixel electrodes are provided on the above described facing substrate. In addition, in the case where the above described liquid crystal display panel is of a drive system (for example, IPS system), which is referred to as a lateral electrical field drive system, the above described counter electrodes are provided on the above described TFT substrate.

[0006] In addition, in the case of conventional general liquid crystal display devices, one TFT element and one pixel element are effective in one pixel. In the liquid crystal display devices that have been proposed in recent years, however, one pixel is divided into two sub-pixels so that two effective TFT elements and two effective pixel electrodes are provided in this one pixel (see, for example, Japanese Unexamined Patent Publication 2006-309239, corresponding U.S. Application US2007/0008263 A1).

[0007] In the case of conventional general liquid crystal display devices, the region occupied by one pixel in the above described TFT substrates is usually equal to a region surrounded by two adjacent scanning signal lines and two adjacent video signal lines. At this time, the TFT element in one pixel has a gate that is connected to one scanning signal line from among the two adjacent scanning signal lines and a drain (or source) that is connected to one video signal line from among the two adjacent video signal lines. In addition, the source (or drain) of the above described TFT element is connected to a pixel electrode.

[0008] That is to say, in the case of the conventional general liquid crystal display devices, scanning signal lines, of which the number is the same as the number of pixels aligned in the direction in which the above described video signal lines extend, are provided on the above described TFT substrate at approximately the same intervals as the size of one pixel in the direction in which the above described video signal lines extend.

[0009] In addition, the TFT elements of the respective pixels are provided in the vicinity of each scanning signal line. Therefore, in the case of the conventional general liquid crystal display devices, one opening region in the light blocking film provided on the above described facing substrate becomes smaller than the region occupied by one pixel.

[0010] Accordingly, the region occupied by one pixel becomes smaller due to, for example, an increase in the resolution of the liquid crystal display device, the ratio of the opening in each pixel becomes smaller, and such a problem arises that the screen becomes darker.

[0011] In addition, in the case where the ratio of the opening in each pixel is small, for example, such a problem arises that it becomes necessary to provide a backlight having a light source with high brightness in order to make the screen brighter.

[0012] KR 2006/0119399 A shows a liquid crystal display device, including a first substrate and a second substrate which sandwich a liquid crystal material, a number of video signal lines, a number of scanning signal lines, a number of TFT elements and pixel electrodes connected to the TFT elements being formed on the above described first substrate, wherein the above described number of video signal lines and the above described number of scanning signal lines are formed in a matrix with regions surrounded by the video signal lines and the scanning signal lines being pixel regions, and two TFT elements and two pixel electrodes which are respectively connected to the two TFT elements are formed

in each of the above described pixel regions.

[0013] In US 2007/103631 a thin film transistor substrate for a liquid crystal display is disclosed, which can provide a required pixel discharging time, and a liquid crystal display comprising the same are disclosed. The thin film transistor substrate comprises a plurality of unit pixels arranged in an (mxn) matrix array, gate lines disposed one by one for every two unit pixels neighboring in a column direction, wherein one gate signal is simultaneously supplied to the two unit pixels via one gate line, data lines intersecting the gate lines, supplying data signals to the unit pixels in synchronization with the gate signals supplied via the gate lines wherein said data lines are arranged two by two between the unit pixels neighboring in a row direction and a thin film transistor TFT formed at each crossing portion of the gate lines and the data lines and transmitting the data signals to pixel electrodes in response to the gate signals.

[0014] In US 2002/041354 a fringe field switching mode LCD is disclosed. The disclosed comprises a first and a second transparent insulating substrates arranged opposite to each other with a predetermined distance, with a liquid crystal layer including a plurality of liquid crystal molecules interposed between them; a plurality of gate bus lines and data bus lines formed on the first transparent insulating substrate and arranged in a matrix form to define a unit pixel; a thin film transistor formed at the intersection of the gate bus line and the data bus line; a counter electrode disposed in each unit pixel, made of transparent conductor; ; and a pixel electrode arranged in each unit pixel to generate a fringe field with the counter electrode, being insulated with the counter electrode and made of transparent conductor and including a plurality of upper slits and lower slits symmetrical each other with respect to long side of the pixel with a predetermined tilted angle.

[0015] In US 2002/085149 a LCD device and a method for manufacturing the same are disclosed, which can reduce resistance of a common electrode formed on an upper substrate. The LCD device includes first and second substrates facing to each other, a plurality of color filter films formed in each pixel region on the first substrate, a plurality of gate and data lines formed on the color filter films to cross one another to define the pixel regions, a plurality of TFTs formed at crossing points of the plurality of gate and data lines, a plurality of pixel electrodes formed in the pixel regions on the first substrate, a plurality of island shaped first black matrix films formed on portions of the second substrate corresponding to the TFTs, and a plurality of common electrodes formed on an entire surface of the second substrate including the first black matrix films.

[0016] It is an object of the present invention is to provide a technology which makes it possible to increase the ratio of the opening in each pixel in a liquid crystal display device, for example.

[0017] This object is achieved by the liquid crystal display device of claim 1. Preferred embodiments of the invention are characterized in the sub-claims.

[0018] In the liquid crystal display device according to the present invention, the ratio of the openings in each pixel can be increased.

[0019] In the following, the present invention is described in detail together with the embodiments (examples) in reference to the drawings.

Fig 1(a) is a schematic block diagram showing an example of a schematic configuration of a liquid crystal display device;

Fig 1(b) is a schematic plan diagram showing an example of a schematic configuration of a liquid crystal display panel;

Fig 1(c) is a schematic cross sectional diagram showing an example of the configuration of the liquid crystal display panel along line A-A' in Fig 1(b);

Fig 2(a) is a schematic circuit diagram showing an example of the circuit configuration of each pixel in a conventional liquid crystal display panel;

Fig 2(b) is a schematic plan diagram showing an example of the configuration of each pixel in a conventional liquid crystal display panel as viewed from the facing substrate side;

Fig 3(a) is a schematic circuit diagram showing an example of the circuit configuration of each pixel in the liquid crystal display panel according to the present example;

Fig 3(b) is a schematic plan diagram showing an example of the configuration of each pixel in the liquid crystal display panel according to the present example as viewed from the facing substrate side;

Fig 4(a) is a schematic plan diagram showing an example in a plan layout of two pixels sandwiched between two adjacent scanning signal lines in a TFT substrate;

Fig 4(b) is a schematic cross sectional diagram showing an example of the configuration of a liquid crystal display panel along line B-B' in Fig 4(a);

Fig 4(c) is a schematic cross sectional diagram showing an example of the configuration of a liquid crystal display panel along line C-C' in Fig 4(a);

Fig 4(d) is a schematic cross sectional diagram showing an example of the configuration of a liquid crystal display panel along line D-D' in Fig 4(a); and

Fig 5 is a schematic plan diagram showing a modification of the plan layout shown in Fig 4(a).

[0020] Throughout the drawings for describing the examples, the same symbols are attached to the components having the same functions, and the descriptions are not repeated.

[0021] Figs 1(a) to 1(c) are schematic diagrams for describing an example of a schematic configuration of the liquid crystal display device according to the present invention. Fig 1(a) is a schematic block diagram showing an example of a schematic configuration of the liquid crystal display device. Fig 1(b) is a schematic plan diagram showing an example of a schematic configuration of the liquid crystal display panel. Fig 1(c) is a schematic cross sectional diagram showing an example of the configuration of the liquid crystal display panel along line A-A' in Fig 1(b).

[0022] The liquid crystal display device according to the present invention has a liquid crystal display panel 1, a data driver 2, a gate driver 3 and a control circuit substrate 4 as shown in Fig 1 (a), for example. Here, in the case where the liquid crystal display device is of a transmission type or of a semi-transmission type, the liquid crystal display device has a backlight unit (light source) and the like in addition to the above, though omitted in Fig 1 (a).

[0023] The liquid crystal display panel 1 has a number of scanning signal lines GL and a number of video signal lines DL, and the region surrounded by the two scanning signal lines which are placed on the outermost sides and the two video signal lines which are placed on the outermost sides corresponds to the display region DA for an image or a video (display screen), for example. In addition, though omitted in Fig 1 (a), a TFT element and a pixel capacitance (which may be referred to as liquid crystal capacitance) which function as an active element are provided in each pixel that forms the display region DA.

[0024] In addition, the liquid crystal display panel 1 is a display panel in which a liquid crystal material LC is sealed between a TFT substrate 101 and a facing substrate 102 as shown in Figs 1(b) and 1(c), for example. At this time, the TFT substrate 101 and the facing substrate 102 are made to adhere by an annular sealing material 103 surrounding the display region DA so that the liquid crystal material LC is sealed airtight in the space surrounded by the TFT substrate 101, the facing substrate 102 and the sealing material 103. Here, in the liquid crystal display panel 1 shown in Fig 1(b), the direction x is the direction in which the respective scanning signal lines GL extend and the direction y is the direction in which the respective video signal lines DL extend.

[0025] In addition, in the case where the liquid crystal display device is of a transmission type or of a semi-transmission type, a lower polarizing plate 104 and an upper polarizing plate 105 are respectively provided on the surfaces of the TFT substrate 101 and the facing substrate 102 facing outwards; in other words, on the rear surfaces of the substrates facing the liquid crystal material LC. At this time, one or more layers of phase difference plates may be provided between the TFT substrate 101 and the lower polarizing plate 104 and between the facing substrate 102 and the upper polarizing plate 105, respectively.

[0026] In addition, in the case where the liquid crystal display device is of a reflective type, the lower polarizing plate 104 is generally unnecessary, and only the upper polarizing plate 105 and a phase difference plate (not shown) are provided on the facing substrate 102 side.

[0027] The data driver 2 is a drive circuit for generating a video signal, which is applied to each video signal line DL, and controlling the timing according to which the signal is applied. In addition, the gate driver 3 is a drive circuit for controlling the period during which the gate of the TFT element is turned on in the scanning signal applied to each scanning signal line GL, for example.

[0028] In addition, the control circuit substrate 4 is a printed circuit board, which is generally referred to as timing controller (T-CON) substrate, and has a circuit which generates a clock signal CS1 for controlling the operation of the data driver 2 and a clock signal CS2 for controlling the operation of the gate driver 3 on the basis of the clock signal CS inputted from the outside of the liquid crystal display device and outputs the signals to the data driver 2 and the gate driver 3, for example. In addition to this, the control circuit substrate 4 has a circuit which converts the input gradation data Kin inputted from the outside of the liquid crystal display device to an output gradation data Kout which matches the type of display and outputs the resulting data to the data driver 2, and supplies part of the power voltage V inputted from the outside of the liquid crystal display device to the data driver 2 and the gate driver 3, for example.

[0029] Figs 2(a) and 2(b) are schematic diagrams showing an example of the configuration of each pixel in a conventional liquid crystal display panel. Fig 2(a) is a schematic circuit diagram showing an example of the circuit configuration of each pixel in the conventional liquid crystal display panel. Fig 2(b) is a schematic plan diagram showing an example of the configuration of each pixel in the conventional liquid crystal display panel as viewed from the facing substrate side. Here, Figs 2(a) and 2(b) show the circuit configuration for eight pixels, that is, two pixels in the width by four pixels in the length, in the upper left corner portion of the display region DA shown in Figs 1(a) and 1(b). In addition, in the case it is necessary to distinguish the number of scanning signal lines GL from each other in the descriptions in reference to Figs 2(a) and 2(b), the symbols of the respective scanning signal lines are denoted by GL_n (n is either 0, 1, 2, 3 or 4), and in the case where it is necessary to distinguish the number of video signal lines DL, the symbols of the respective video signal lines are denoted by DL_m (m is any of 1, 2 and 3).

[0030] A region occupied by one pixel in the conventional active matrix type TFT liquid crystal display panels (liquid crystal display devices) corresponds to a region surrounded by two adjacent scanning signal lines GL and two adjacent video signal lines DL (for example, the region surrounded by the scanning signal lines GL_1 and GL_2 as well as the video

signal lines DL_1 and DL_2) as shown in Fig 2(a), for example. Here, the scanning signal line GL_0 shown in Fig 2(a) is a dummy scanning signal line which is provided so that the pixels located above the scanning signal line GL_1 have the same circuit configuration as the pixels located beneath the scanning signal lines GL_1, for example.

[0031] At this time, one TFT element Tr and one pixel capacitance C_{LC} are provided in one pixel, for example. The TFT element Tr has a gate connected to one scanning signal line GL from among the two adjacent scanning signal lines GL and a drain connected to one video signal line DL from among the two adjacent video signal lines DL. In addition, the pixel capacitance C_{LC} is formed of a pixel electrode PX connected to the source of the TFT element Tr, a liquid crystal material LC and a counter electrode CT provided on either the TFT substrate 101 or the facing substrate 102.

[0032] Here, though in the present specification, the drain of the TFT element Tr is connected to the video signal line DL and the source is connected to the pixel electrode PX, the opposite case is possible, that is to say, the source may be connected to the video signal line DL and the drain may be connected to the pixel electrode PX. In addition, in actual liquid crystal display devices, the sources and the drains are periodically switched depending on the relationships in the potential between the video signal (gradation voltage) applied to the video signal line DL and the common voltage applied to the counter electrode CT.

[0033] In the case where the liquid crystal display device is of a longitudinal electrical field drive system, the scanning signal lines GL, the video signal lines DL, the TFT elements Tr and the pixel electrodes PX, for example, in the configuration shown in Fig 2(a) are provided on the TFT substrate 101. In addition, in the case where the liquid crystal display device is of a lateral electrical field drive system, the scanning signal lines GL, the video signal lines DL, the TFT elements Tr, the pixel electrodes PX and the counter electrodes CT, for example, in the configuration shown in Fig 2(a) are provided on the TFT substrate 101. In addition, in either case, the scanning signal lines GL, the video signal lines DL, the TFT elements Tr and the pixel electrodes PX are provided so that the plan layout on the TFT substrate 101 reflects the circuit configuration shown in Fig 2(a).

[0034] In addition, a light blocking film in mesh form which extends in such locations as to overlap (face) the scanning signal lines GL and the video signal lines DL is provided on the facing substrate 102 as described above. Therefore, the configuration of the liquid crystal display panel 1 is that of the one shown in Fig 2(b) when viewed from the facing substrate 102 side, and in this configuration, for example, a light blocking film BM is provided in the region that is hatched. Here, in Fig 2(b), thick dotted lines extending in the direction x and dotted lines extending in the direction y in Fig 2(b) are the scanning signal lines GL_n and the video signal lines DL_m in Fig 2(a), respectively. In addition, white rectangular regions surrounded by the light blocking film BM are openings through which light from a backlight unit, for example, transmits, and thus, are regions which are responsible for the gradation display in each pixel.

[0035] In addition, in the case where the conventional liquid crystal display device corresponds to a color display, a number of pixels aligned in the direction in which the video signal lines DL extend (direction y) are responsible for the gradation display for the same color from among the basic colors in the color display. That is to say, in the case of an RGB type color liquid crystal display device, a number of pixels between the two adjacent video signal lines DL_1 and DL_2 are respectively responsible for the gradation display for the same color (for example, red).

[0036] Incidentally, in the conventional liquid crystal display device (liquid crystal display panel 1) as shown in Fig 2(b), the opening in one pixel has a size PWx in the lateral direction (direction x) which is smaller than the gap GLS between two adjacent scanning signal lines GL and a size PWy in the longitudinal direction which is smaller than the gap DLS between two adjacent video signal lines DL. Therefore, in the case where the gap GLS between two adjacent scanning signal lines GL and the gap DLS between two adjacent video signal lines DL become smaller due to an increase in the resolution, for example, the area of the opening in each pixel becomes smaller, and thus, such a problem arises that the ratio of the opening lowers.

Example

[0037] Figs 3(a) and 3(b) are schematic diagrams showing an example of the configuration of the liquid crystal display panel according to one example of the present invention. Fig 3(a) is a schematic circuit diagram showing an example of the circuit configuration of each pixel in the liquid crystal display panel according to the present example. Fig 3(b) is a schematic plan diagram showing an example of the configuration of each pixel in the liquid crystal display panel according to the present example as viewed from the facing substrate side. Here, Figs 3(a) and 3(b) show the circuit configuration for eight pixels, that is to say, two pixels in the width by four pixels in the length in the upper left corner portion of the display region DA shown in Figs 1(a) and 1(b). In addition, in the case where it is necessary to distinguish a number of scanning signal lines GL from each other in the descriptions in reference to Figs 3(a) and 3(b), the symbols of the respective scanning signal lines are denoted by GL_n (n is either 1 or 2), and in the case where it is necessary to distinguish a number of video signal lines DL from each other, the symbols of the respective scanning signal lines are denoted by DL_m (m is any of 1, 2, 3, 4 and 5).

[0038] In the liquid crystal display panel 1 according to the present example, the number of scanning signal lines GL is reduced to half the number of the pixels aligned in the direction in which the video signal lines DL extend (direction

y) as shown in Fig 3(a), for example, so as to be provided at a ratio of 1 for 2 pixels aligned in the direction in which the video signal lines DL extend.

[0039] In addition, the number of video signal lines DL is increased to two times greater than the number of pixels aligned in the direction in which the scanning signal lines GL extend (direction x). At this time, the respective video signal lines DL are provided so that the pixel electrode PX for one pixel is sandwiched between two adjacent video signal lines and two video signal lines run between the pixel electrodes PX of two pixels which are adjacent in the direction in which the scanning signal lines GL extend.

[0040] In addition, in the liquid crystal display panel 1 according to the present example also, one TFT element Tr and one pixel capacitance CLC are provided to one pixel, for example, so that the region occupied by one pixel corresponds to a region surrounded by one scanning signal line GL, a pixel border PB which is adjacent to the scanning signal line GL, and two video signal lines DL which are adjacent to each other with the pixel electrode PX in between. That is to say, in the liquid crystal display panel 1 according to the present example, when a region surrounded by two adjacent scanning signal lines GL (for example, scanning signal lines GL_1 and GL_2) and two adjacent video signal lines DL (for example, video signal lines DL_1 and DL_2) is one pixel region, two TFT elements Tr and two pixel electrodes PX are provided in this one pixel region.

[0041] Here, in the liquid crystal display panel 1 according to the present example, two video signal lines DL (for example, video signal lines DL_1 and DL_2) are allocated for one pixel column made up of a number of pixels aligned in the direction in which the video signal lines extend (direction y), and pixels having a TFT element of which the drain is connected to one of the above described two video signal lines and pixels having a TFT element of which the drain is connected to the other video signal line alternate in this one pixel column.

[0042] In addition, in the above described one pixel column, the gates of the TFT elements in two pixels which are adjacent to each other with one scanning signal line GL in between are connected to the same scanning signal line GL and the drains are connected to different video signal lines.

[0043] In addition, between two adjacent scanning signal lines GL in the above described one pixel column, a pixel having a TFT element of which the gate is connected to one of the two scanning signal lines GL and a pixel having a TFT element of which the gate is connected to the other scanning signal line GL are aligned. At this time, the drains of the TFT elements in the two pixels between the two adjacent scanning signal lines GL are connected to different video signal lines.

[0044] In the case where the liquid crystal display device is of a longitudinal electrical field drive system, the scanning signal lines GL, the video signal lines DL, the TFT elements Tr and the pixel electrodes PX, for example, in the configuration shown in Fig 3(a) are provided on the TFT substrate 101. In addition, in the case where the liquid crystal display device is of a lateral electrical field drive system, the scanning signal lines GL, the video signal lines DL, the TFT elements Tr, the pixel electrodes PX and the counter electrodes CT, for example, in the configuration shown in Fig 3(a) are provided on the TFT substrate 101. In addition, in either case, the scanning signal lines GL, the video signal lines DL, the TFT elements Tr and the pixel electrodes PX are provided so that the plan layout on the TFT substrate 101 reflects the circuit configuration shown in Fig 3(a).

[0045] At this time, the configuration of the liquid crystal display panel 1 as viewed from the facing substrate 102 side is one of that as shown in Fig 3(b), for example, when a light blocking film BM is provided on the facing substrate 102 in such locations as to overlap (face) the scanning signal lines GL and the video signal lines DL as in the prior art. Here, in Fig 3(b) also, the light blocking film BM extends in the hatched region, and white rectangular regions surrounded by the light blocking film BM are openings through which light from a backlight unit, for example, transmits, and are regions which are responsible for the gradation display in each pixel.

[0046] In the liquid crystal display panel 1 according to the present example, the number of the scanning signal lines GL is reduced to half of the number of pixels included in one pixel column, and therefore, any components which block external light (for example, TFT elements) are not provided in the border between two pixels which are provided between two adjacent scanning signal lines GL (pixel border PB). Therefore, it is not necessary to provide a light blocking film in the locations which face the pixel border PB, and thus, one opening can be provided for two pixels placed between two adjacent scanning signal lines GL (one pixel region). At this time, one opening for two pixels located between two adjacent scanning signal lines GL becomes wider by the portion of the light blocking film for the division into the two pixels which is omitted as shown in Fig 2(b), for example. Therefore, in the liquid crystal display panel 1 according to the present example, the ratio of the opening in each pixel becomes higher than that shown in Fig 2(b), and thus, the screen can be prevented from becoming darker.

[0047] Figs 4(a) to 4(d) are schematic diagrams showing an example of the configuration of the TFT substrate in the liquid crystal display panel according to the present example. Fig 4(a) is a schematic plan diagram showing an example of the plan layout for two pixels sandwiched between two adjacent scanning signal lines in the TFT substrate. Fig 4(b) is a schematic cross sectional diagram showing an example of the configuration of the liquid crystal display panel along line B-B' in Fig 4(a). Fig 4(c) is a schematic cross sectional diagram showing an example of the configuration of the liquid crystal display panel along line C-C' in Fig 4(a). Fig 4(d) is a schematic cross sectional diagram showing an example

of the configuration of the liquid crystal display panel along line D-D' in Fig 4(a).

[0048] In the case where the circuit configuration of the liquid crystal display panel according to the present example is applied to a liquid crystal display panel of a lateral electrical field drive system, Figs 4(a) to 4(d) show the plan layout of the TFT substrate 101 and the cross sections of the configuration of the liquid crystal display panel, for example.

[0049] The TFT substrate 101 is a substrate where scanning signal lines GL, video signal lines DL, TFT elements Tr, pixel electrodes PX, counter electrodes CT and an orientation film ORI1 are layered and provided on the surface of an insulating substrate SUB1, such as a glass substrate, and the counter electrodes CT, the scanning signal lines GL and the capacitance holding lines SL are first formed on the surface of the insulating substrate SUB. The counter electrodes CT are formed by etching a conductive film having a high light transmittance, for example, an ITO film. The scanning signal lines GL and the capacitance holding lines SL are formed by etching a conductive film, for example, an aluminum film. At this time, an ITO film and an aluminum film are formed in sequence on the entire surface of the insulating substrate SUB, and after that, the aluminum film is first etched so that the scanning signal lines GL and the capacitance holding lines SL are formed, and then, the ITO film is etched so that the counter electrodes CT are formed.

[0050] Here, an ITO film may be formed and etched so that the counter electrodes CT are formed, and after that, an aluminum film may be formed and etched so that the scanning signal lines GL and the capacitance holding lines SL are formed.

[0051] Furthermore, an aluminum film may be formed and etched so that the scanning signal lines GL and the capacitance holding lines SL are formed, and after that, an ITO film may be formed and etched so that the counter electrodes CT are formed.

[0052] A first insulating layer PAS1, which functions as the gate insulting film of the respective TFT elements, is formed on the surface of the insulating substrate SUB on which the counter electrodes CT and the scanning signal lines GL are formed. The first insulating layer PAS1 is formed of a silicon oxide film or a silicon nitride film, for example.

[0053] A semiconductor layer SC for the respective TFT elements, video signal lines DL and the drain electrodes SD1 and the source electrodes SD2 of the respective TFT elements are formed on the first insulating layer PAS1. The semiconductor layer SC is formed by etching a semiconductor film, such as of amorphous silicon or polycrystal silicon, for example. The video signal lines DL as well as the drain electrodes SD1 and the source electrodes SD2 of the respective TFT elements are formed by etching a conductive film, such as an aluminum film. At this time, the video signal lines DL as well as the drain electrodes SD1 and the source electrodes SD2 of the respective TFT elements are formed after the semiconductor layer SC and part of the drain electrodes SD1 and the source electrodes SD2 extends from the surface of the first insulating layer PAS1 onto the semiconductor layer SC. At this time, the video signal lines DL and the drain electrodes SD1 are integrally formed in general.

[0054] A second insulating layer PAS2 and pixel electrodes PX are formed on the surface of the first insulating layer PAS1 on which the semiconductor layer SC and the video signal lines DL are formed, and the pixel electrodes PX are connected to the source electrodes SD2 via through holes TH. The second insulating layer PAS2 is formed of a silicon oxide film, a silicon nitride film, other organic insulating films or inorganic insulating films, for example. In addition, the pixel electrodes PX are formed by etching a conductive film having a high light transmittance, for example, an ITO film.

[0055] In addition, in the case of a liquid crystal display panel of a lateral electrical field drive system having such a configuration in the cross section, the pixel electrodes PX are in comb form in the plan view where a number of slits (openings) are provided in the regions which overlap the counter electrodes CT.

[0056] At this time, in the case where two pixel electrodes PX sandwiched between two adjacent scanning signal lines GL have such a form in the plan view that the pixel border PB crosses the direction in which the scanning signal lines GL extend as shown in Fig 4(a), for example, a change of color from one pixel to the other (gradation) becomes gradual in the vicinity of the pixel border PB.

[0057] Meanwhile, the facing substrate 102 is a substrate where a light blocking film BM, color filters CF and an orientation film ORI2 are layered and provided on the surface of an insulating substrate SUB2, such as a glass substrate, and the light blocking film BM is first formed on the surface of the insulating substrate SUB2, for example. The light blocking film BM is formed by etching a conductive film having high light blocking properties, for example, of chromium.

[0058] In addition, as shown in Figs 4(b) and 4(c) for example, the light blocking film BM is provided in and extends into such locations as to overlap (face) the scanning signal lines GL and the video signal lines DL in the facing substrate 102. At this time, the light blocking film BM in such locations as to overlap the scanning signal lines GL are formed so as to cover two capacitance holding lines SL which run with the scanning signal lines GL in between, for example.

[0059] In addition, color filters CF are provided on the surface of the insulating substrate SUB2 on which the light blocking film BM is formed, for example. The color filters CF are formed so as to have the same base color in the opening regions of a number of pixels which are aligned in the direction in which the video signal lines DL extend, for example, and have different base colors alternately in the opening regions of a number of pixels which are aligned in the direction in which the scanning signal lines GL extend. That is to say, in the case of an RGB type color liquid crystal display panel, all the opening regions of the number of pixels aligned in the direction in which the video signal lines DL extend are any of the following three colors: red (R), green (G) and blue (B). In addition, as for the number of opening regions aligned

in the direction in which the scanning signal lines DL extend, red opening regions, green opening regions and blue opening regions are repeated in this order, for example.

[0060] In the case where the TFT substrate 101 has a configuration as described above, as shown in Fig 4(d) for example, no problem arises with the display of each pixel even when there is no light blocking film BM in the border portion PB between two pixels (pixel electrodes PX) between two adjacent scanning signal lines GL on the facing substrate 102, and therefore, the ratio of the opening of the two pixels can be increased. Thus, even in the case where the area occupied by one pixel becomes smaller due to an increase in the resolution of the liquid crystal display panel, for example, the brightness of the screen can be maintained. In addition, the brightness of the screen can be maintained without using a backlight unit having high brightness, and therefore, an increase in the power consumption can be prevented.

[0061] Furthermore, the number of the scanning signal lines GL on the liquid crystal display panel 1 according to the present example is half of that used in the general liquid crystal display panels according to the prior art. Therefore, in the case where the period for one frame in the liquid crystal display device using the liquid crystal display panel 1 according to the present example is set to the same time as in the period of one frame in general liquid crystal devices according to the prior art, the time during which a video signal (gradation voltage) is written in the pixel electrode PX of each pixel can be made approximately two times longer than the time for general liquid crystal display devices according to the prior art. Therefore, unevenness in the picture quality and deterioration in the picture quality due to a lack of writing can be reduced in the liquid crystal display device using the liquid crystal display panel 1 according to the present example, for example.

[0062] Conversely, in the case where the time during which a video signal (gradation voltage) is written in the pixel electrode PX of each pixel in the liquid crystal display device using the liquid crystal display panel 1 according to the present example is set to be the same as that in the general liquid crystal display devices according to the prior art, the period for one frame can be made approximately half of the period for one frame in the general liquid crystal display devices according to the prior art. Therefore, it is easy to increase the speed of display (drive), for example, in the liquid crystal display device using the liquid crystal display panel according to the present example.

[0063] Fig 5 is a schematic plan diagram showing a modification of the plan layout shown in Fig 4(a).

[0064] As an example of a plan layout of the TFT substrate 101 in the liquid crystal display panel 1 according to the present example, Fig 4(a) shows an example where two pixel electrodes PX sandwiched between two adjacent scanning signal lines GL have such a form in a plane that the pixel border PB becomes diagonal relative to the direction in which the scanning signal lines GL extend.

[0065] However, the form of the two pixel electrodes PX in a plane sandwiched between two adjacent scanning signal lines GL is not limited to this, and as shown in Fig 5 for example, the pixel border PB may of course have such a form as to be approximately parallel to the direction in which the scanning signal lines GL extend.

[0066] In addition, in the TFT substrate 101 according to the present example, the forms in a plane of the semiconductor layer SC, the drain electrode SD1 and the source electrode SD2 in the TFT elements TR and the direction and the number of slits in the pixel electrodes PX can of course be changed in an appropriate manner.

[0067] Furthermore, though an example of a plan layout on the TFT substrate 101 and a configuration of the liquid crystal display panel 1 in the cross section are cited in the case where the present example is applied to a liquid crystal display panel 1 of a lateral electrical field drive system, the invention is not limited to this, and the arrangement can of course be applied to a liquid crystal display panel 1 of a longitudinal electrical field drive system.

[0068] Though the present invention is concretely described on the basis of the above described example, the present invention is not limited to the above described example, and various modifications are of course possible within the scope of the invention defined by the appended claims.

EXPLANATION OF SYMBOLS

[0069]

1 ...	liquid crystal display panel
101	... TFT substrate
102	... facing substrate
103 ...	sealing material
104 ...	lower polarizing plate
105	... upper polarizing plate
LC ...	liquid crystal material
SUB1, SUB2	... insulating substrates
GL, GL_0, GL_1, GL_2, GL_3, GL_4 ...	scanning signal lines
DL, DL_1, DL_2, DL_3, DL_4, DL_5 ...	video signal lines

PAS1	... first insulating layer
SC ...	semiconductor layer
SD1	... drain electrode
SD2 ...	source electrode
PAS2	... second insulating layer
PX ...	pixel electrode
CT ...	counter electrode
SL ...	capacitance maintaining line
BM ...	light blocking film
CF ...	color filter
ORI1, ORI2 ...	orientation films
Tr ...	TFT element
C_{LC} ...	pixel capacitance
PB ...	pixel border
2 ...	data driver
3 ...	gate driver
4 ...	control circuit substrate

Claims

1. A liquid crystal display device, comprising:

a first insulating substrate (SUB1) and a second insulating substrate (SUB2) which sandwich a layer of liquid crystal material (LC),
a number of video signal lines (DL), a number of scanning signal lines (GL), a number of TFT elements (Tr) and pixel electrodes (PX) connected to the TFT elements (Tr) being formed on said first insulating substrate (SUB1),
a two-dimensional matrix of pixels, the pixels being defined by the arrangement of the video signal lines (DL) and the scanning signal lines (GL), wherein the scanning signal lines (GL) are arranged one by one for every two pixels neighboring in a column direction of the matrix, and wherein the video signal lines (DL) are arranged two by two between the pixels neighboring in a row direction of the matrix,
RGB color filters (CF) of colors red (R), green (G) and blue (B) formed in opening regions of a light blocking film (BM) provided on the surface of the second insulating substrate (SUB2) and aligned with the pixels in plan view,
a TFT element (Tr) and a pixel electrode (PX) which is connected to the TFT element (Tr) are formed in each pixel, wherein the number of scanning signal lines (GL) is half the number of the pixels aligned in each column of the matrix and wherein
the number of video signal lines DL is two times the number of pixels aligned in each row of the matrix **characterized in that**.
the RGB color filters (CF) are formed so as to have the same color in the opening regions corresponding to all pixels which are aligned in a same column of the matrix , and have different colors alternating in the opening regions corresponding to the pixels which are aligned in a same row of the matrix.

2. The liquid crystal display device according to claim 1, wherein one counter electrode (CT) is formed on the first insulating substrate in each pixel.

3. The liquid crystal display device according to claim 1, wherein each pixel electrode has a number of slits, the slits in each pixel electrode extending in two directions.

4. The liquid crystal display device according to claim 3, wherein said slits extend in directions which are not parallel to either said video signal lines (DL) or said scanning signal lines (GL).

5. The liquid crystal display device according to claim 1, wherein the light blocking film is formed in such locations as to overlap said video signal lines (DL) and said scanning signal lines (GL).

Patentansprüche

1. Flüssigkristallanzeigevorrichtung, umfassend:

ein erstes isolierendes Substrat (SUB1) und ein zweites isolierendes Substrat (SUB2), die eine Schicht aus Flüssigkristallmaterial (LC) zwischen sich einschließen,
eine Anzahl von Videosignalleitungen (DL), eine Anzahl von Abtastsignalleitungen (GL), eine Anzahl von TFT-Elementen (Tr) und Pixelelektroden (PX), die mit den TFT-Elementen (Tr) verbunden sind, die auf dem ersten isolierenden Substrat (SUB1) ausgebildet sind,
eine zweidimensionale Matrix aus Pixeln, wobei die Pixel durch die Anordnung der Videosignalleitungen (DL) und der Abtastsignalleitungen (GL) definiert sind, wobei die Abtastsignalleitungen (GL) eins für eins für jeweils zwei Pixel, die in einer Spaltenrichtung der Matrix nebeneinander liegen, angeordnet sind, und wobei die Videosignalleitungen (DL) zwei für zwei zwischen den Pixeln, die in der Spaltenrichtung der Matrix nebeneinander liegen, angeordnet sind,
RGB Farbfilter (CF) der Farben Rot (R), Grün (G) und Blau (B), die in Öffnungsbereichen eines lichtblockierenden Films (BM) ausgebildet sind, der auf der Oberfläche des zweiten isolierenden Substrats (SUB2) vorgesehen und mit den Pixeln in Draufsicht ausgerichtet ist,
ein TFT-Element (Tr) und eine Pixelelektrode (PX), die mit dem TFT-Element (Tr) verbunden ist, sind in jedem Pixel ausgebildet,
wobei die Anzahl der Abtastsignalleitungen (GL) die Hälfte der Anzahl der Pixel beträgt, die in jeder Spalte der Matrix ausgerichtet sind, und wobei
die Anzahl der Videosignalleitungen (DL) das Zweifache der Anzahl der Pixel, die in jeder Zeile der Matrix ausgerichtet sind, beträgt, **dadurch gekennzeichnet, dass** die RGB Farbfilter (CF) so ausgebildet sind, dass sie die gleiche Farbe in den Öffnungsbereichen haben, die allen Pixeln entsprechen, die in derselben Spalte der Matrix ausgerichtet sind und unterschiedliche Farben haben, die in den Öffnungsbereichen abwechselnd entsprechend den Pixeln, die in derselben Zeile der Matrix ausgerichtet sind.

2. Flüssigkristallanzeigevorrichtung nach Anspruch 1, worin eine Gegenelektrode (CT) auf dem ersten isolierenden Substrat in jedem Pixel ausgebildet ist.

3. Flüssigkristallvorrichtung nach Anspruch 1, worin jede Pixelelektrode eine Anzahl von Schlitzen hat, wobei die Schlitze in jeder Pixelelektrode sich in zwei Richtungen erstrecken.

4. Flüssigkristallvorrichtung nach Anspruch 3, worin die Schlitze sich in Richtungen erstrecken, die nicht zu entweder den Videosignalleitungen (DL) oder den Abtastsignalleitungen (GL) parallel sind.

5. Flüssigkristallvorrichtung nach Anspruch 1, wobei der lichtblockierende Film an solchen Stellen ausgebildet ist, dass er die Videosignalleitungen (DL) und die Abtastsignalleitungen (GL) überlappt.

Revendications

1. Dispositif d'affichage à cristaux liquides, comprenant:

- un premier substrat isolant (SUB1) et un second substrat isolant (SUB2) qui enserrent une couche de matériau à cristaux liquides (LC),
- un nombre de lignes de signaux vidéo (DL), un nombre de lignes de signaux de numérisation (GL), un nombre d'éléments (Tr) de TFT et les électrodes de pixels (PX) connectées aux éléments (Tr) de TFT étant formées sur ledit premier substrat isolant (SUB1),
- une matrice bidimensionnelle de pixels, les pixels étant définis par l'arrangement des lignes de signaux vidéo (DL) et des lignes de signaux de numérisation (GL), où les lignes de signaux de numérisation (GL) sont disposées l'une après l'autre pour chaque deux pixels voisins dans une direction des colonnes de la matrice, et où les lignes de signaux vidéo (DL) sont disposées deux par deux entre les pixels voisins dans une direction des lignes de la matrice,
- les filtres de couleur (CF) RGB de couleurs rouge (R), vert (G) et bleu (B) formés dans les régions d'ouverture d'un film de blocage de la lumière (BM) pourvus sur la surface du second substrat isolant (SUB2) et alignés avec les pixels dans la vue en plan,
- un élément (Tr) de TFT et une électrode de pixels (PX) qui est connectée à l'élément (Tr) de TFT sont formés

en chaque pixel,
- où le nombre de lignes de signaux de numérisation (GL) est la moitié du nombre de pixels alignés en chaque colonne de la matrice et où
- le nombre de lignes de signaux vidéo (DL) est deux fois le nombre de pixels alignés en chaque ligne de la matrice **caractérisé en ce que**,
les filtres de couleur (CF) RGB sont formés pour avoir la même couleur dans les régions d'ouverture correspondant à tous les pixels qui sont alignés dans une même colonne de la matrice, et d'avoir des couleurs différentes alternant dans les régions d'ouverture correspondant aux pixels qui sont alignés dans une même ligne de la matrice.

2. Dispositif d'affichage à cristaux liquides selon la revendication 1, où une contre-électrode (CT) est formée sur le premier substrat isolant en chaque pixel.

3. Dispositif d'affichage à cristaux liquides selon la revendication 1, où chaque électrode de pixels présente un nombre de fentes, les fentes en chaque électrode de pixels s'étendant en deux directions.

4. Dispositif d'affichage à cristaux liquides selon la revendication 3, où lesdites fentes s'étendent en directions qui ne sont pas parallèles soit auxdites lignes de signaux vidéo (DL) soit auxdites lignes de signaux de numérisation (GL).

5. Dispositif d'affichage à cristaux liquides selon la revendication 1, où le film de blocage de la lumière est formé dans des tels endroits pour recouvrir lesdites lignes de signaux vidéo (DL) et lesdites lignes de signaux de numérisation (GL).

Fig.1(a)

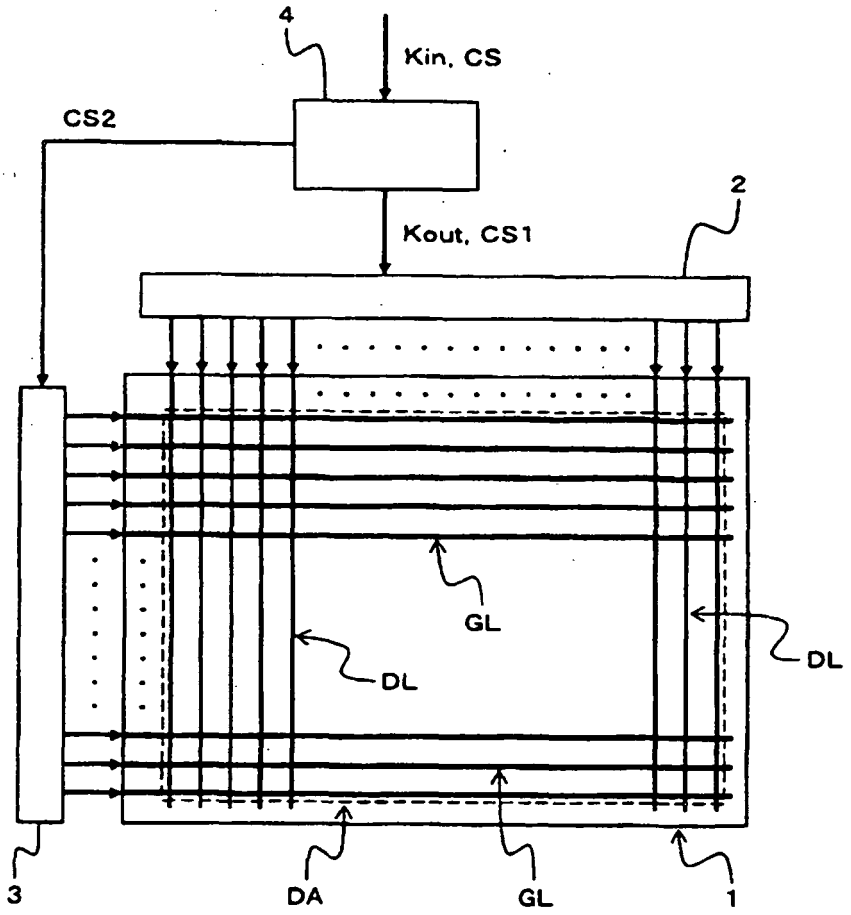


Fig.1(b)

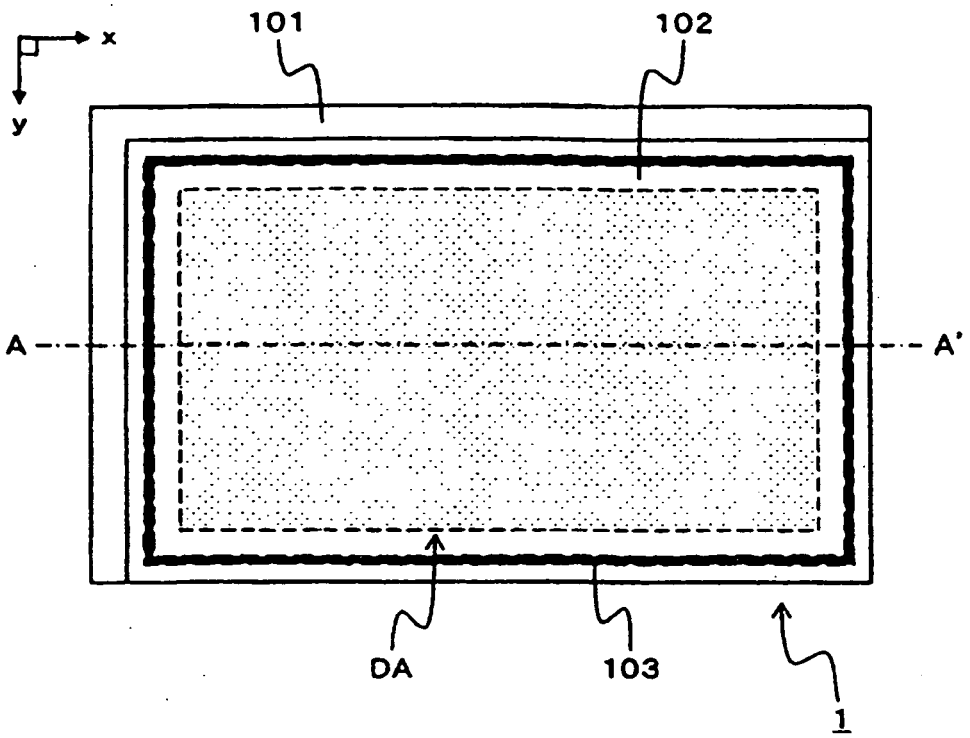


Fig.1(c)

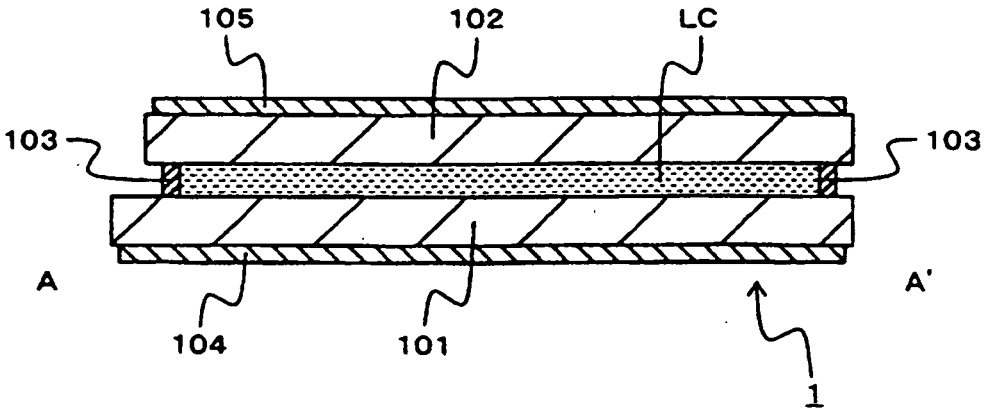


Fig.2(a)

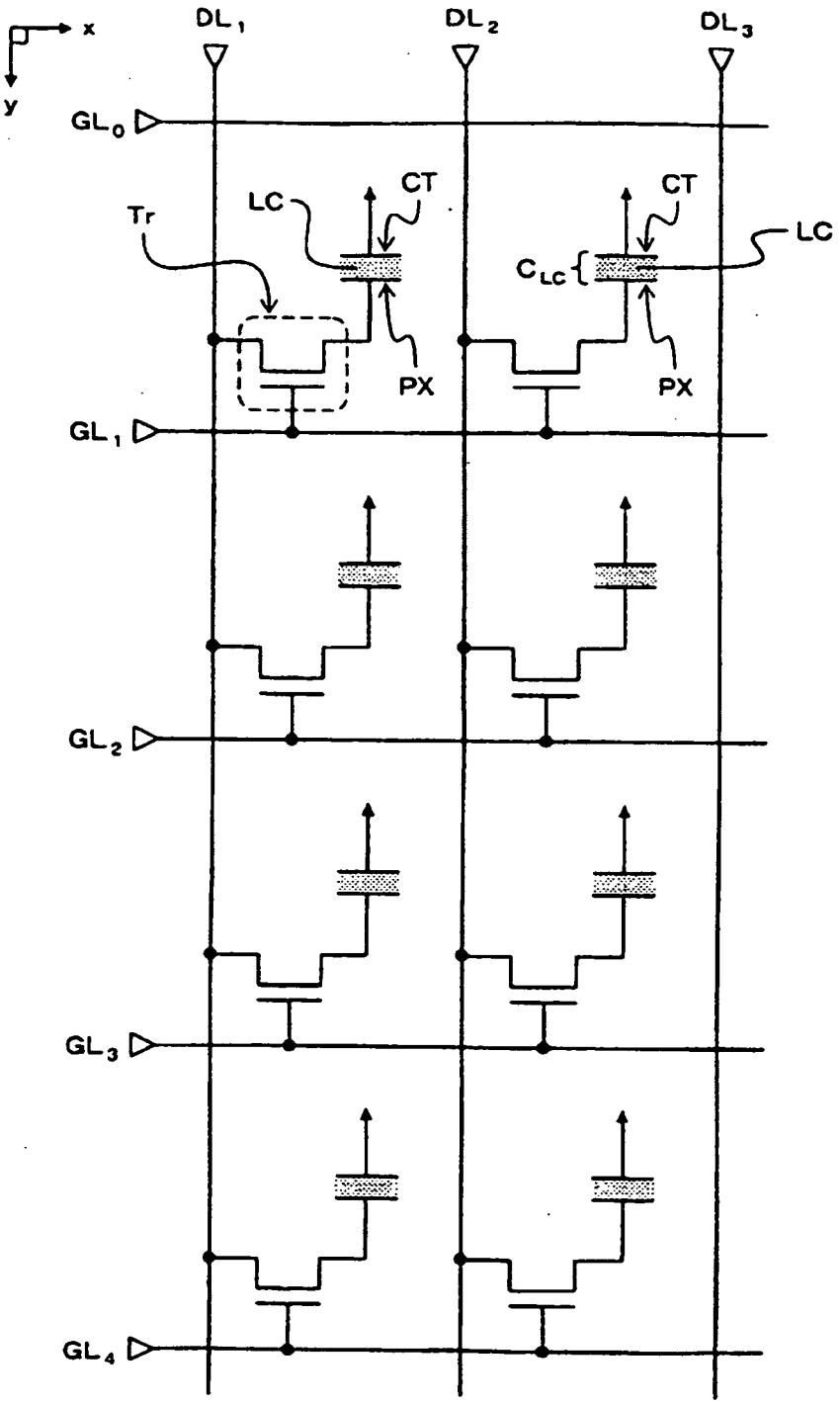


Fig.2(b)

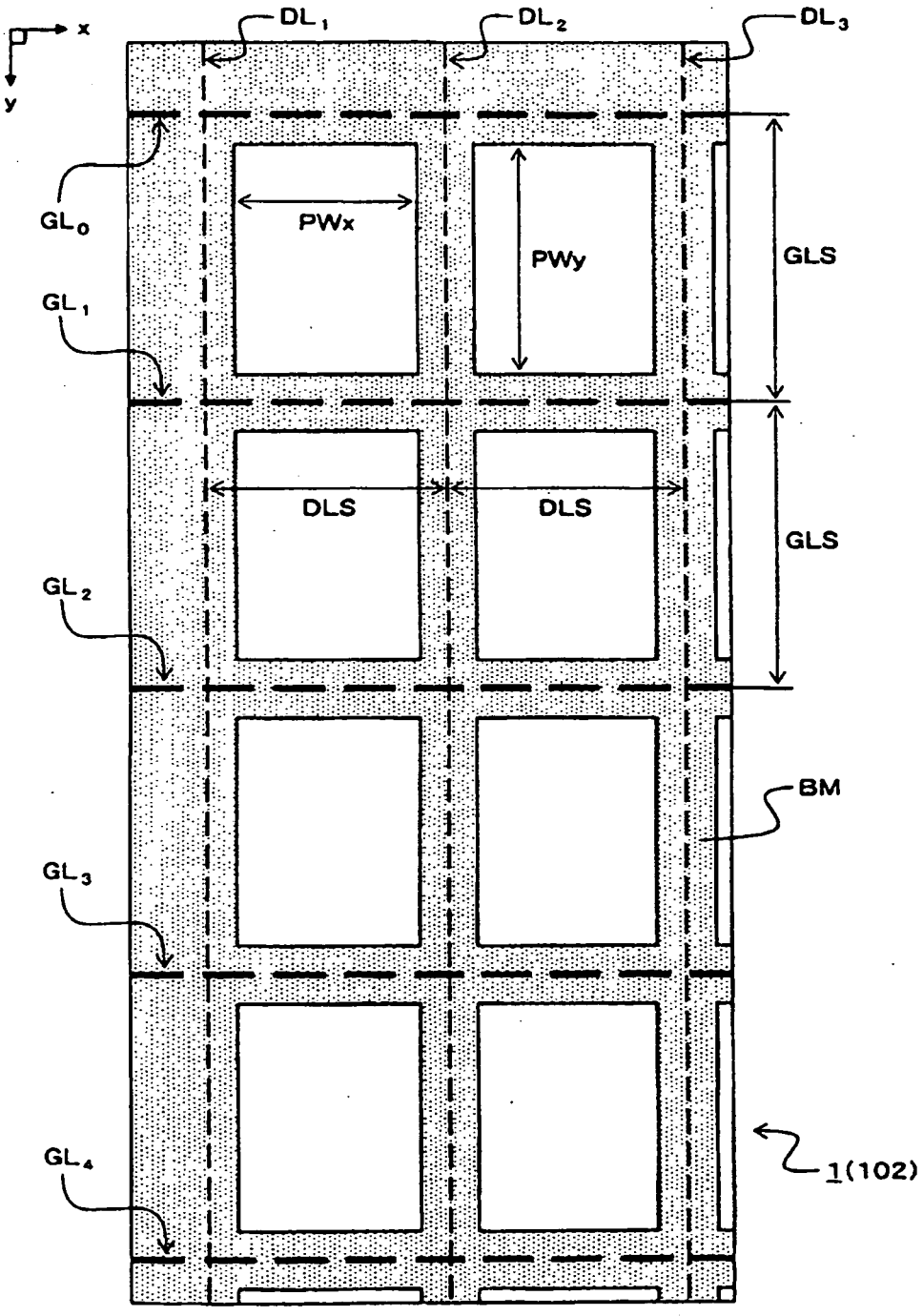

x
y
DL1
DL2
DL3
GL0
GL1
GL2
GL3
GL4
PWx
PWy
GLS
GLS
DLS
DLS
BM
1(102)

Fig.3(a)

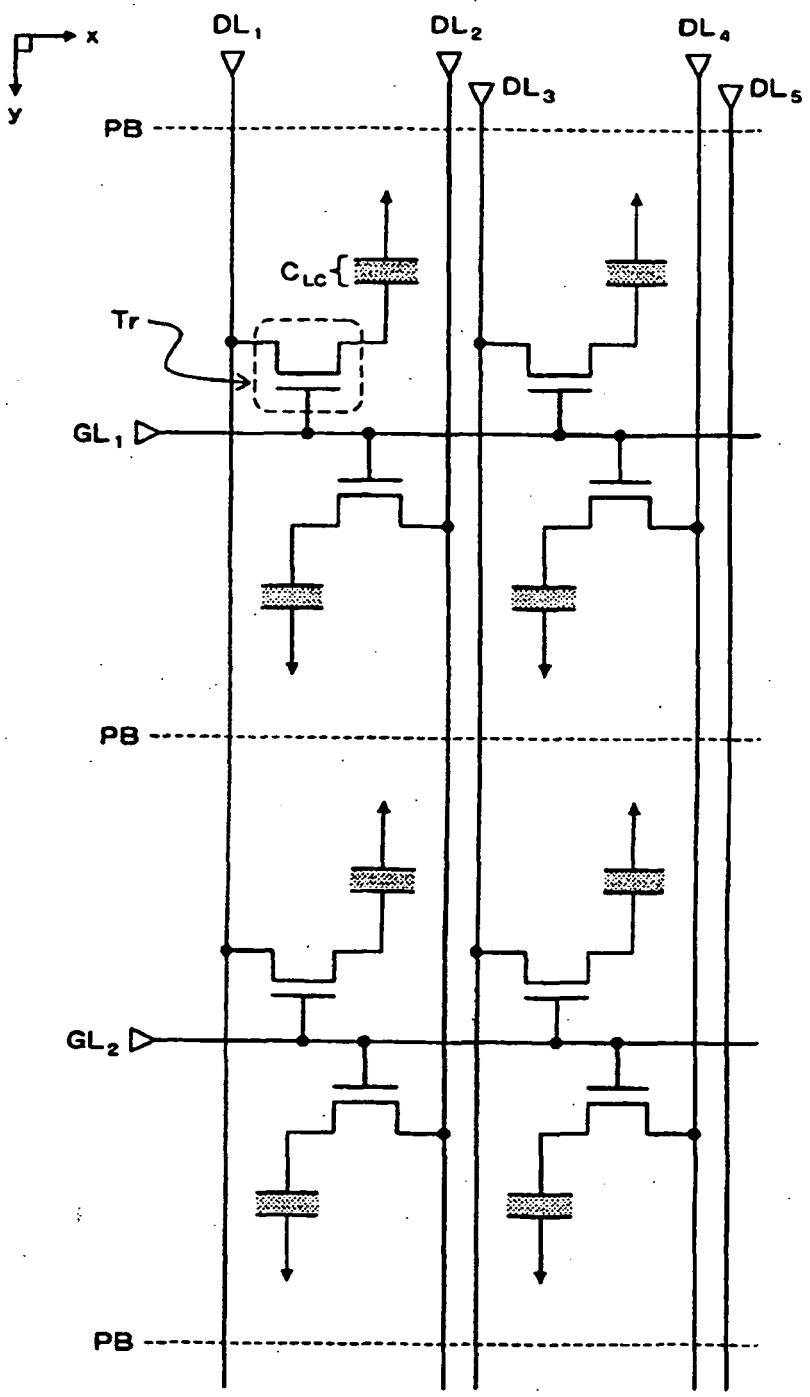


Fig.3(b)

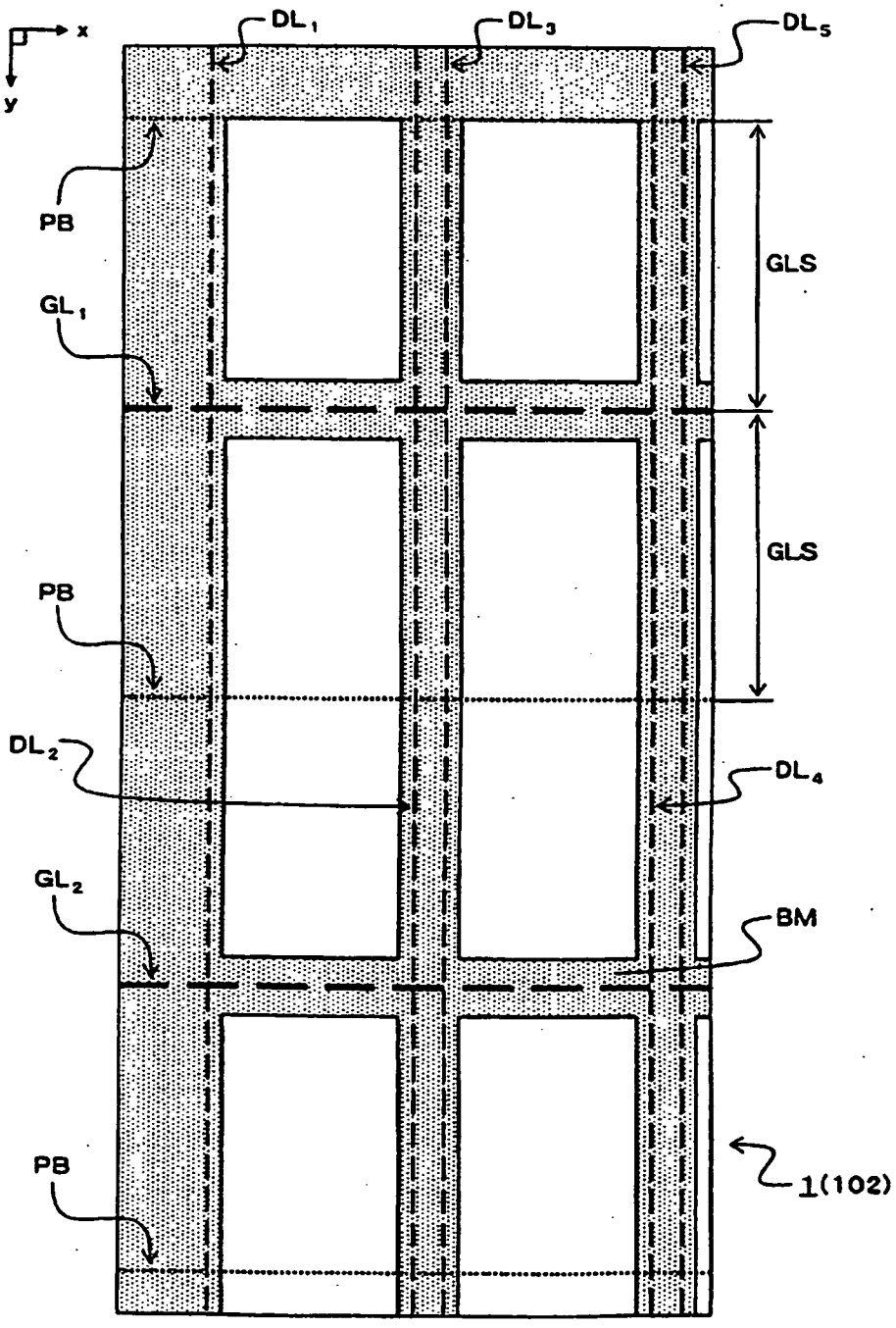


Fig.4(a)

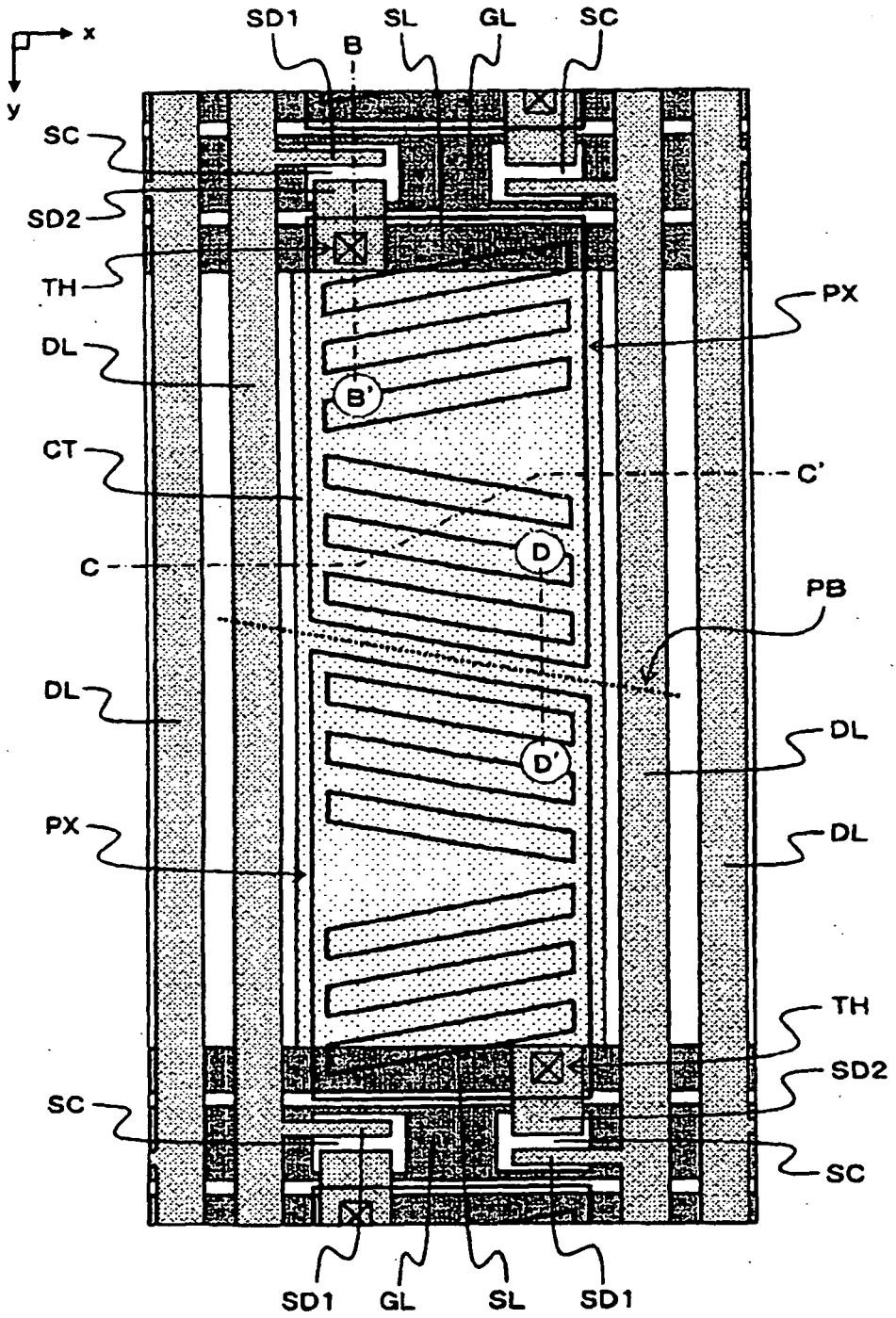

x
y
SD1
B
SL
GL
SC
SC
SD2
TH
PX
DL
B'
CT
C'
C
D
PB
DL
DL
D'
PX
DL
TH
SD2
SC
SC
SD1
GL
SL
SD1

Fig.4(b)

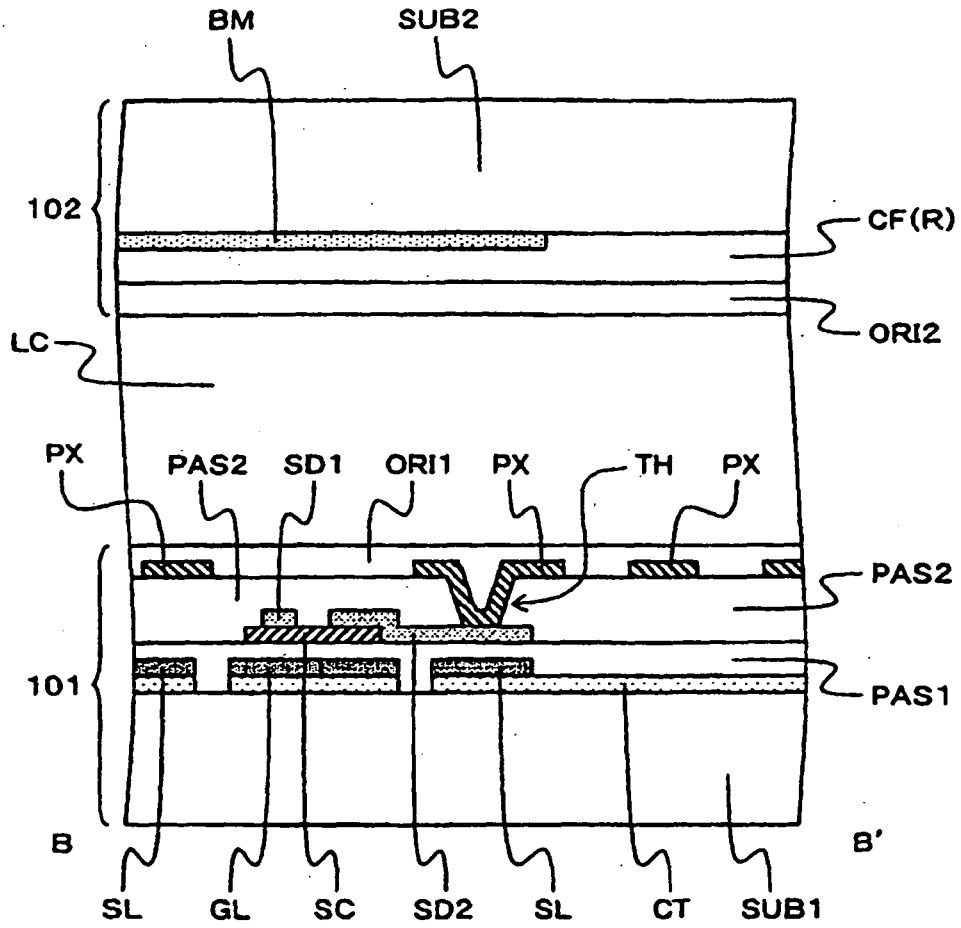

BM
SUB2
102
CF(R)
ORI2
LC
PX
PAS2
SD1
ORI1
PX
TH
PX
PAS2
101
PAS1
B
B'
SL
GL
SC
SD2
SL
CT
SUB1

Fig.4(c)

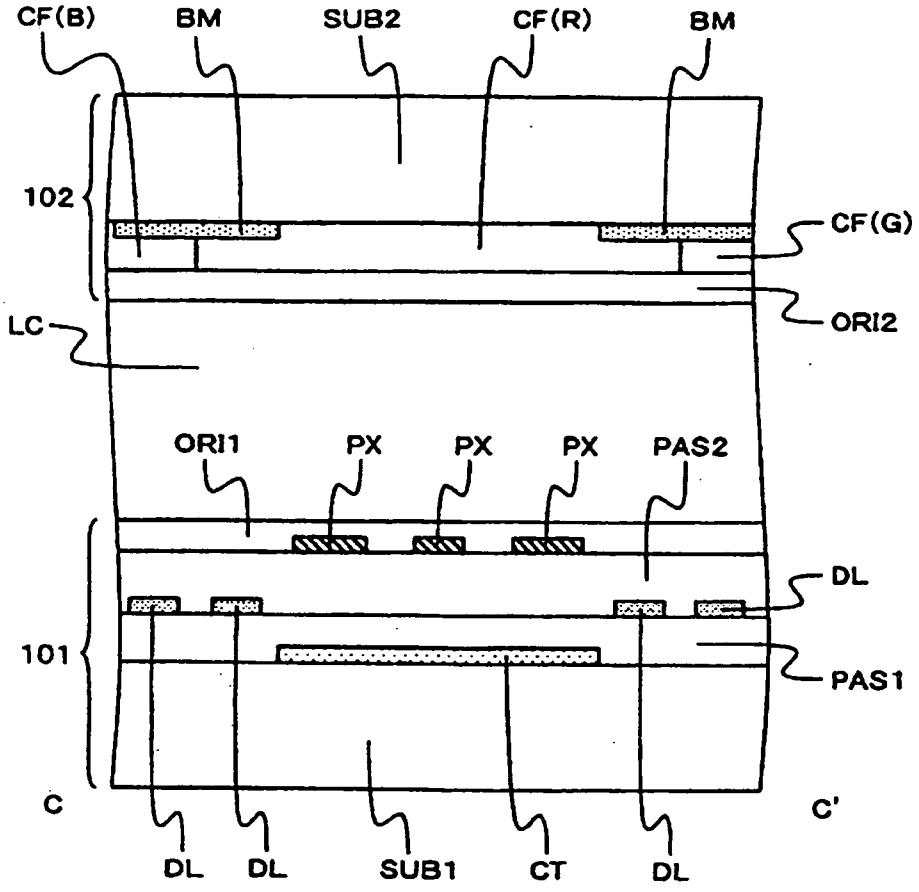

CF(B)
BM
SUB2
CF(R)
BM
102
CF(G)
ORI2
LC
ORI1
PX
PX
PX
PAS2
DL
101
PAS1
C
C'
DL
DL
SUB1
CT
DL

Fig.4(d)

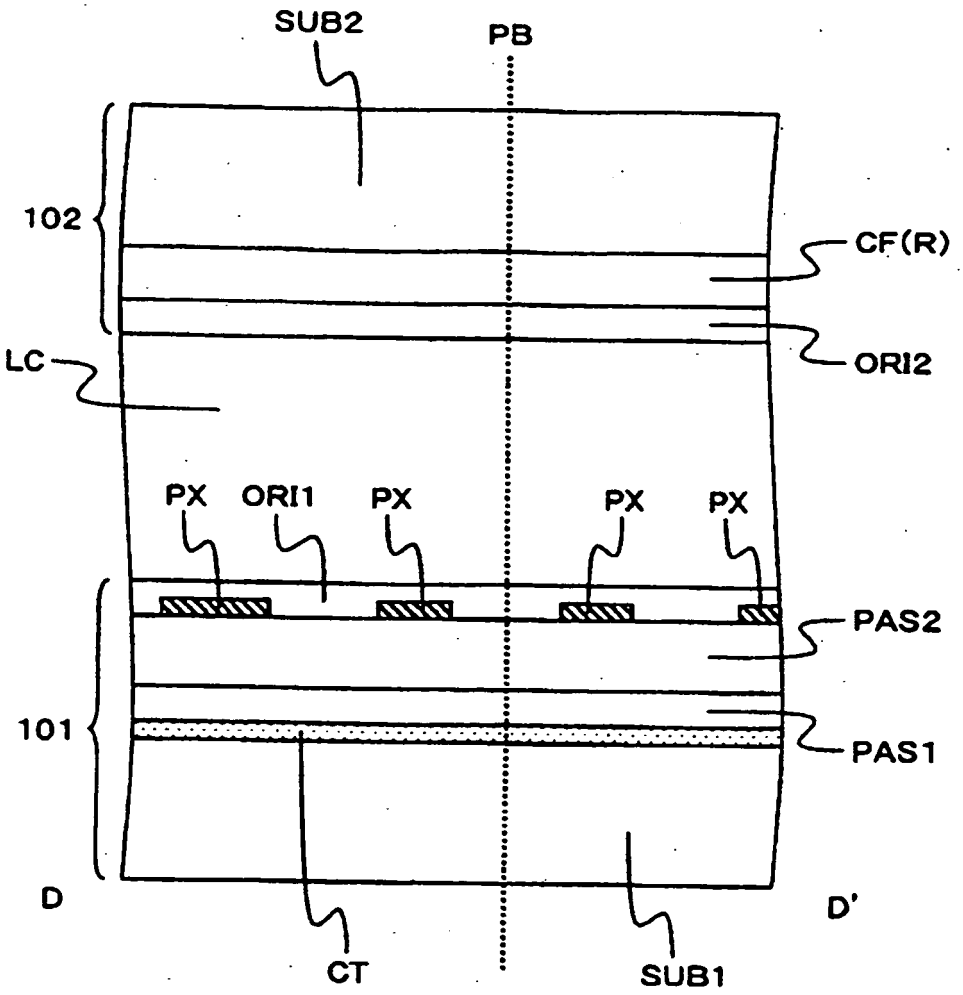
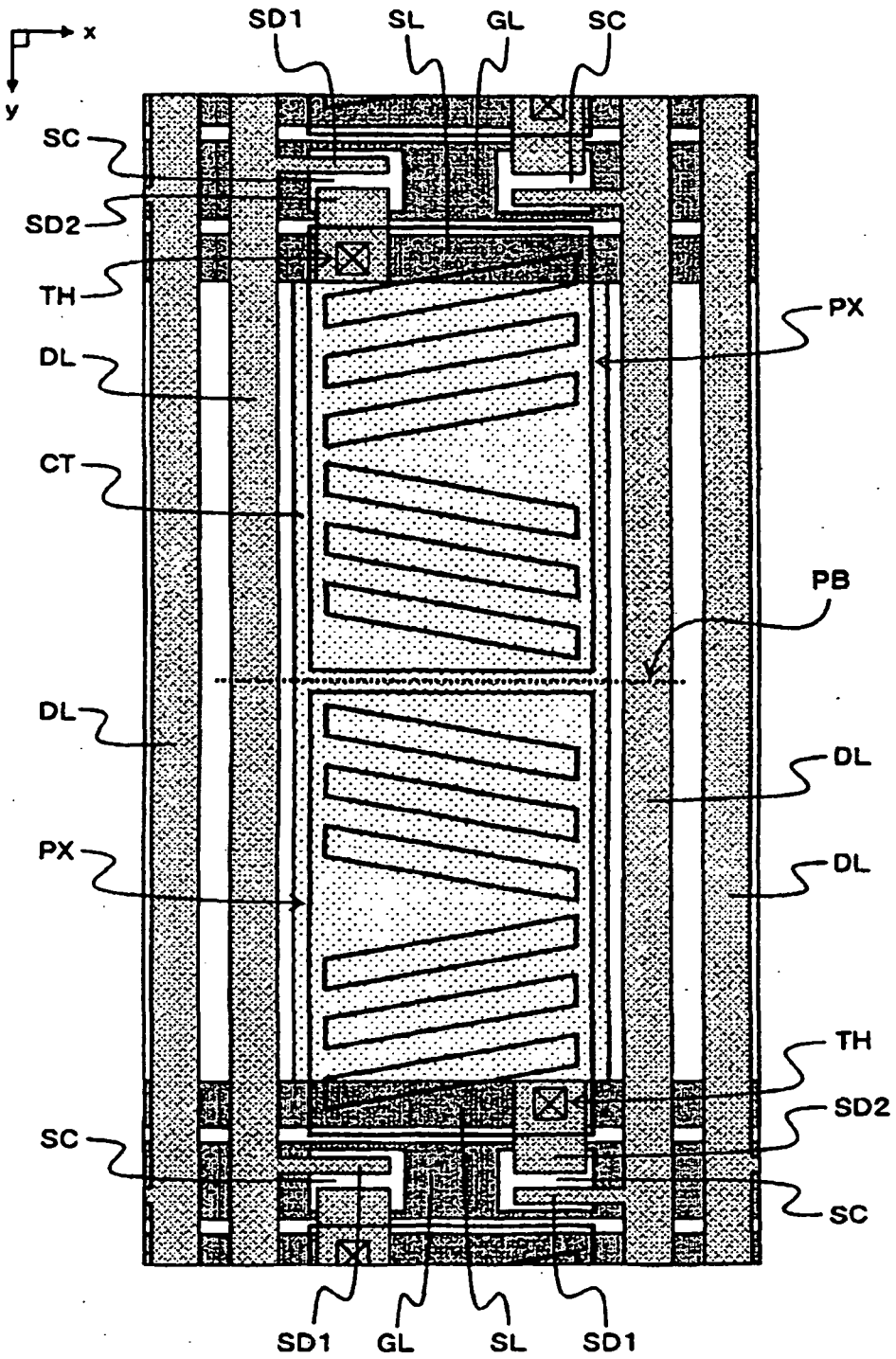


Fig.5


x
y
SD1
SL
GL
SC
SC
SD2
TH
PX
DL
CT
PB
DL
DL
PX
DL
TH
SD2
SC
SC
SD1
GL
SL
SD1

REFERENCES CITED IN THE DESCRIPTION

This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

Patent documents cited in the description

- JP 2006309239 A **[0006]**
- US 20070008263 A1 **[0006]**
- KR 20060119399 A **[0012]**
- US 2007103631 A **[0013]**
- US 2002041354 A **[0014]**
- US 2002085149 A **[0015]**

专利名称(译)	液晶显示装置		
公开(公告)号	EP2048538B1	公开(公告)日	2013-02-27
申请号	EP2008017550	申请日	2008-10-07
[标]申请(专利权)人(译)	株式会社日立显示器		
申请(专利权)人(译)	日立显示器有限公司.		
当前申请(专利权)人(译)	松下液晶显示CO.，LTD. 日立显示器有限公司.		
[标]发明人	ONO KIKUO		
发明人	ONO, KIKUO		
IPC分类号	G02F1/1335 G02F1/1362		
CPC分类号	G02F1/133514 G02F1/133512 G02F1/136286 G02F2201/40		
优先权	2007263030 2007-10-09 JP		
其他公开文献	EP2048538A1		
外部链接	Espacenet		

摘要(译)

为了增加液晶显示装置中每个像素的开口比例，具有有源矩阵型液晶显示板的液晶显示装置包括：两个像素中的TFT元件，它们彼此相邻，具有一条扫描信号线之间分别具有连接到扫描信号线的栅极和连接到不同视频信号线的源极或漏极;在两条相邻的扫描信号线之间，具有TFT元件的像素，其栅极连接到两条扫描信号线之一，而像素的TFT元件的栅极连接到另一条扫描信号线，视频信号线延伸的方向，以及两个TFT元件的源极或漏极连接不同的视频信号线。