(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 2 023 195 A1

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
11.02.2009 Bulletin 2009/07

(51) Int Cl.:
G02F 1/1345 *(2006.01)* ***G02F 1/1362*** *(2006.01)*

(21) Application number: **08012877.0**

(22) Date of filing: **16.07.2008**

(84) Designated Contracting States:
AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MT NL NO PL PT RO SE SI SK TR
Designated Extension States:
AL BA MK RS

(30) Priority: **09.08.2007 KR 20070080355**
09.08.2007 KR 20070080354

(71) Applicant: **LG Display Co., Ltd.**
Seoul 150-721 (KR)

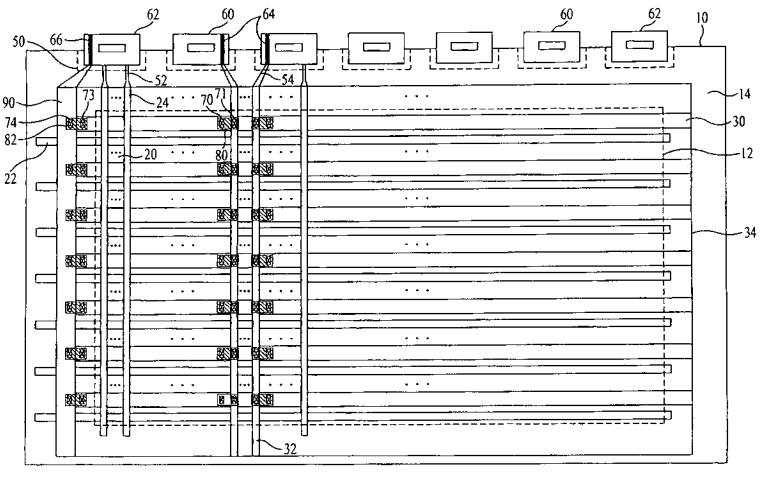
(72) Inventors:
- **Lee, Jae Kyun**
  Suwon-si
  Gyeonggi-do (KR)
- **Oh, Kum Mi**
  Seodaemun-gu
  Seoul (KR)
- **Oh, Jae Young**
  Yeongdeungpo-gu
  Seoul (KR)
- **Shin, Dong Su**
  Anyang-si
  Gyeonggi-do (KR)

(74) Representative: **TER MEER - STEINMEISTER & PARTNER GbR**
Patentanwälte
Mauerkircherstrasse 45
81679 München (DE)

(54) Liquid crystal display device

(57) A liquid crystal display device having uniform common voltage distribution within a display panel (10) is disclosed. The liquid crystal display device includes a display panel (10) including a display area (12) and a non-display area (14) surrounding the display area (12), a plurality of gate lines (22) and data lines (24) arranged on the display area (10) to intersect each other, so as to define a plurality of pixel regions (20), thin-film transistors (21) formed at respective intersections of the gate lines (22) and the data lines (24), pixel electrodes formed on the respective pixel regions and connected to the thin film transistors, a plurality of first common lines (30) provided between the neighboring gate lines and arranged parallel to the gate lines (22), and a plurality of second common lines (32) provided between the neighboring data lines and arranged parallel to the data lines (24), the second common lines (32) being electrically connected to the first common lines (30).

FIG. 1



EP 2 023 195 A1

Description

[0001] This application claims the benefit of the Korean Patent Application No. P2007-080354, filed on August 9, 2007, and of the Korean Patent Application No. P2007-080355, filed on August 9, 2007 which are hereby incorporated by reference as if fully set forth herein.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention relates to a liquid crystal display device, and more particularly, to a liquid crystal display device, which can achieve uniform common voltage distribution within a display panel, resulting in enhanced display quality.

Discussion of the Related Art

[0003] With growth of an information society, there is a demand for development of a novel image display device capable of solving drawbacks of a conventional Cathode Ray Tube (CRT) such as weight and volume thereof. Therefore, a variety of flat panel display devices, including Liquid Crystal Display (LCD) devices, Organic Light Emitting Diodes (OLEDs), Plasma Panel Display (PDP) devices, Surface-conduction Electron-emitter Display (SED) devices, etc., have attracted considerable attention.

[0004] Of the above-mentioned display devices, the most representative display device is an LCD device, which has been widely used from a large-scale TV screen to a small display screen of a mobile phone.

[0005] Such an LCD device is configured in such a manner that a liquid crystal material, exhibiting dielectric anisotropy and refractive index anisotropy, is arranged between two electrodes. After an electric field is generated between the two electrodes, strength of the electric field is adjusted to control transmission of light, whereby a desired display image can be realized.

[0006] That is, the LCD device is not a self-illuminating type display device capable of emitting light by itself, but a light-receiving type display device designed to realize an image upon receiving light from a light source situated therein.

[0007] Generally, the LCD device receives white light from the light source situated therein, and realizes color images using three colors of red, green and blue.

[0008] In the above-described configuration of the LCD device, the two electrodes, used to drive liquid crystals, generally include a pixel electrode and a common electrode, which are connected to a thin film transistor, the pixel electrode receiving a voltage corresponding to an image signal, and the common electrode receiving a common voltage. The liquid crystals can be driven by an electric field generated between the two electrodes.

[0009] However, the above-described conventional LCD device has the following problems.

[0010] Firstly, a common line, which serves to supply a common voltage to a panel of the LCD device, is horizontally formed, and only one or two input terminals to apply the common voltage to the common line are present.

[0011] Therefore, achieving uniform common voltage distribution in a large-scale panel is difficult due to a resistance in the common line, etc. This deteriorates image quality, and may cause afterimages, etc. In particular, in the case of a model for use in televisions, it has a longer horizontal length than a vertical length and therefore, suffers from an increased resistance of the common line. Accordingly, there is a high likelihood of wire breakage and crosstalk.

SUMMARY OF THE INVENTION

[0012] Accordingly, the present invention is directed to a liquid crystal display device that substantially obviates one or more problems due to limitations and disadvantages of the related art.

[0013] An object of the present invention is to provide a liquid crystal display device having uniform common voltage distribution within a liquid crystal display panel.

[0014] Additional advantages, objects, and features of the invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from practice of the invention. The objectives and other advantages of the invention may be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0015] To achieve these objects and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, a liquid crystal display device comprising: a display panel including a display area and a non-display area surrounding the display area; a plurality of gate lines and data lines arranged on the display area to intersect each other, so as to define a plurality of pixel regions; thin-film transistors formed at respective intersections of the gate lines and the data liens; pixel electrodes formed on the respective pixel regions and connected to the thin film transistors; a plurality of first common lines provided between the neighboring gate lines and arranged parallel to the gate lines; and a plurality of second common lines provided between the neighboring data lines and arranged parallel to the data lines, the second common lines being electrically connected to the first common lines.

[0016] The liquid crystal display device may further comprise: a plurality of data pad portions on the non-display area, each data pad portion including data pad lines and common pad lines; first data driver ICs connected to the respective data pad portions except for opposite end data pad portions; second data driver ICs connected to the opposite end data pad portions; and a plu-

rality of first common voltage input terminals provided in at least one of the first data driver ICs for supplying a common voltage to each second common line via the common pad lines.

[0017] The liquid crystal display device may further comprise a common voltage delay restrictor for supplying common voltage control signals to the first and second common lines so as to prevent a common voltage delay phenomenon.

[0018] It is to be understood that both the foregoing general description and the following detailed description of the present invention are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this application, illustrate embodiment(s) of the invention and together with the description serve to explain the principle of the invention. In the drawings:

[0020] FIG. 1 is a plan view illustrating a liquid crystal display device according to a first embodiment of the present invention;

[0021] FIG. 2 is a plan view illustrating a data driver IC;

[0022] FIG. 3 is a plan view illustrating an in-plane switching mode liquid crystal display device according to the first embodiment of the present invention;

[0023] FIG. 4 is a plan view illustrating a liquid crystal display device according to a second embodiment of the present invention;

[0024] FIG. 5 is a plan view illustrating a liquid crystal display device according to a third embodiment of the present invention;

[0025] FIG. 6 is a sectional view of the liquid crystal display device according to the third embodiment of the present invention, illustrating a region where a data line and a second common line connecting pattern overlap each other;

[0026] FIG. 7 is a plan view of the liquid crystal display device according to the third embodiment of the present invention, illustrating line widths of overlapped portions of a data line and a second common line connecting pattern;

[0027] FIG. 8 is a plan view illustrating a liquid crystal display device according to a fourth embodiment of the present invention;

[0028] FIG. 9 is an enlarged plan view of the liquid crystal display device according to the fourth embodiment of the present invention;

[0029] FIG. 10 is a plan view illustrating a liquid crystal display device according to a fifth embodiment of the present invention;

[0030] FIG. 11 is a plan view illustrating a liquid crystal display device according to a sixth embodiment of the present invention;

[0031] FIG. 12 is a plan view illustrating a dual layer configuration of a third common line connecting pattern in the liquid crystal display devices according to the fifth and sixth embodiments of the present invention;

[0032] FIG. 13 is a plan view illustrating a liquid crystal display device according to a seventh embodiment of the present invention;

[0033] FIG. 14 is a plan view illustrating a liquid crystal display device according to an eighth embodiment of the present invention;

[0034] FIG. 15 is a plan view illustrating a liquid crystal display device according to a ninth embodiment of the present invention;

[0035] FIG. 16 is a plan view illustrating a liquid crystal display device according to a tenth embodiment of the present invention;

[0036] FIG. 17 is a plan view illustrating a liquid crystal display device according to an eleventh embodiment of the present invention;

[0037] FIG. 18 is a plan view illustrating a liquid crystal display device according to a twelfth embodiment of the present invention;

[0038] FIG. 19 is a plan view illustrating a liquid crystal display device according to a thirteenth embodiment of the present invention;

[0039] FIG. 20A is a view illustrating common voltage distribution within a display panel of a conventional liquid crystal display device; and

[0040] FIG. 20B is a view illustrating common voltage distribution within a display panel of the liquid crystal display device according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0041] Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

[0042] Hereinafter, a liquid crystal display device according to the present invention will be described in more detail with reference to the accompanying drawings.

[0043] First Embodiment

[0044] FIG. 1 is a plan view illustrating a liquid crystal display device according to a first embodiment of the present invention, FIG. 2 is a plan view illustrating a data driver IC, and FIG. 3 is a plan view illustrating an In-Plane Switching (IPS) mode liquid crystal display device according to the first embodiment of the present invention.

[0045] The liquid crystal display device according to the first embodiment of the present invention, as shown in FIG. 1, includes a display panel 10 consisting of a display area 12 and a non-display area 14 surrounding the display area 12, a plurality of gate lines 22 and data lines 24 formed on the display area 12 to intersect each other to thereby define a plurality of pixel regions 20, a plurality of thin film transistors 21 formed at respective

intersections of the gate lines 22 and the data lines 24, a plurality of pixel electrodes formed on the pixel regions and connected to the respective thin film transistors, a plurality of first common lines 30 formed parallel to the respective gate lines 22, a plurality of second common lines 32 formed parallel to the respective data lines 24 to intersect the first common lines 30, a plurality of data pad portions 50 formed in the non-display area 14 and each constituted by a collection of pad lines including data pad lines 52 and common pad lines 54, a plurality of first data driver ICs 60 connected to the respective data pad portions 50 except for two opposite end data pad portions, and two second data driver ICs 62 connected to the two opposite end data pad portions 50.

[0046] Of the plurality of first data driver ICs 60, at least one first data driver IC 60 is provided with first common voltage input terminal 64 to supply a common voltage to each second common line 32.

[0047] For reference, in the following description, the same reference numerals will be used to refer to the same or like parts.

[0048] The display panel 10 includes two transparent substrates bonded to face each other, between which a liquid crystal layer is interposed.

[0049] Scan signals are sequentially supplied to the display panel 10 through the gate lines 22.

[0050] The plurality of data lines 24 and the plurality of gate lines 22 intersect each other with a gate insulating film (not shown) being interposed therebetween, defining the plurality of pixel regions 20. Data signals are supplied to the display panel 10 through the data lines 24.

[0051] The plurality of pixel regions 20 is arranged, in a matrix, within the display area 12. Each pixel region, for example, is adapted to correspond to any one of red, green and blue.

[0052] As shown in FIG. 3, each thin-film transistor 21 includes a gate electrode 25 branched from the associated gate line 22, a semiconductor layer 23 formed on top of the gate electrode 25, a source electrode 27 branched from the associated data line 24 and located on top of one end of the semiconductor layer 23, and a drain electrode 28 formed opposite the source electrode 27.

[0053] Each pixel electrode 29 formed on the pixel region 20 is connected to the drain electrode 28. Preferably, the pixel electrode 29 is made of, for example, a transparent conductive layer such as Indium Tin Oxide (ITO), Indium Zinc Oxide, or the like.

[0054] The thin film transistor is turned On/Off by the scan signal supplied via the gate line. If the thin film transistor is turned on, the data signal is applied to the pixel electrode.

[0055] The first common lines 30 and the gate lines 22 are arranged in parallel and are formed of the same layer. The second common lines 32 and the data lines 24 are arranged in parallel and are formed of the same layer. The first common lines 30 and the second common lines 32 intersect each other with the gate insulating film (not shown) being interposed therebetween.

[0056] The first common lines 30 and the second common lines 32 are electrically connected to each other and are adapted to stably supply the common voltage to the entire liquid crystal display panel 10. Specifically, the common voltage, input from the exterior, is supplied to the liquid crystal display panel 10 via the first common lines 30 and the second common lines 32. For example, the first common lines 30 and the second common lines 32 are electrically connected to each other by first connecting patterns 80, each of which is patterned to cover both a first contact hole 70 exposing a part of the first common line 30 and a second contact hole 71 exposing a part of the second common line 32. Preferably, the first connecting patterns 80 are formed of the same layer as the pixel electrode 29.

[0057] The reason why the first common lines 30 and the second common lines 32 are connected to each other via the first connecting patterns 80 rather than being directly connected to each other is to prevent addition of a process. Generally, after the thin film transistors are formed and a protective film is deposited over the entire surface of the display panel 10, contact holes are formed in the drain electrodes of the thin film transistors and the pixel electrodes are formed so as to be electrically connected to the drain electrodes through the contact holes. Accordingly, as the first and second contact holes 70 and 71 are formed upon formation of the contact holes in the drain electrodes, and the first connecting patterns 80 are formed upon patterning of the pixel electrodes, there is no additional process.

[0058] The plurality of data pad portions 50 include the plurality of data pad lines 52 connected at one end thereof to the data lines 24 to supply data signals to the data lines 24. The data pad portions 50 may further include the plurality of common pad lines 54 electrically connected at one end thereof to the second common lines 32 to supply the common voltage to the second common lines 32.

[0059] All the data pad lines 52 and the common pad lines 54 are formed of the same layer as the data lines 24. Specifically, the second common lines 32 are integrally formed with the respective common pad lines 54, and the data pad lines 52 are integrally formed with the respective data lines 24.

[0060] The first data driver ICs 60 are mounted, respectively, on the plurality of data pad portions 50 except for the two opposite end data pad portions, and the second data driver ICs 62 are mounted on the two opposite end data pad portions 50.

[0061] At least one of the first data driver ICs 60 has the first common voltage input terminal 64, to which the common voltage is applied. The first common voltage input terminal 64 is connected to the common pad line 54 to input the common voltage to each second common line 32.

[0062] At least one of the second data driver ICs 62 has a second common voltage input terminal 66 to input

the common voltage, too. The second common voltage input terminal 66 is provided at the second data driver IC 62 such that it is connected to a first common line connecting pattern 90. The first common line connecting pattern 90 serves to electrically connect the plurality of first common lines 30 with one another.

[0063] The first common line connecting pattern 90, as shown in FIG. 1, may be provided at the left side and/or right side of the liquid crystal display panel 10. Also, the first common line connecting pattern 90 may be formed of the same layer as the data lines 24. In this case, the first common line connecting pattern 90 is electrically connected to the first common lines 30 by second connecting patterns 82, each of which is patterned to cover both a contact hole 73 exposing a part of the first common line 30 and a contact hole 74 exposing a part of the first common line connecting pattern 90. Preferably, the second connecting patterns 82 are formed of the same layer as the pixel electrodes 29.

[0064] As described above, the liquid crystal display device according to the first embodiment of the present invention supplies the common voltage via the second common lines arranged parallel to the data lines, enabling more uniform supply of the common voltage over the entire display panel.

[0065] An in-plane switching mode liquid crystal display device according to the first embodiment of the present invention, as shown in FIG. 3, includes the first connecting patterns 80, each of which is patterned to cover both the first contact hole 70 exposing a part of the first common line 30 and the second contact hole 71 exposing a part of the second common line 32.

[0066] The pixel electrodes 29 are formed on the respective pixel regions 20 and are electrically connected to the drain electrodes 28 of the thin film transistors 21. Common electrodes 31 are formed between the pixel electrodes 29. Both the common electrodes 31 and the pixel electrodes 29 are formed of the same layer.

[0067] The common electrodes 31 are electrically connected to common line branches 33 branched from the first common lines 33 to the pixel regions via contact holes 72b. The common electrodes 31 are also connected to the second common lines 32 via third contact holes 72a. That is, the first common lines 30 and the second common lines 32 can be electrically connected to each other via the common electrodes 31.

[0068] Second Embodiment

[0069] FIG. 4 is a plan view illustrating an important part of a liquid crystal display device according to a second embodiment of the present invention.

[0070] In the first embodiment of the present invention, the common voltage supplied from the exterior is individually applied to each of the second common lines 32. Therefore, when the common voltage supplied from the exterior fluctuates, there is a likelihood of uneven supply of the common voltage.

[0071] For this reason, in the second embodiment of the present invention, at least one second common line connecting pattern 92 having an island shape is formed in the non-display area 14 between the data pad portions 50 and the display area 12. To assure uniform supply of the common voltage supplied via the first common voltage input terminals 64 of the neighboring data driver ICs 60, the at least two neighboring second common lines 32 and the at least two neighboring common pad lines 54 are connected to the second common line connecting pattern 92.

[0072] In FIG. 4, the common pad lines 54 and the second common lines 32 are formed of the same layer as the data line 24, and the second common line connecting pattern 92 is formed of the same layer as the gate lines 22.

[0073] A contact hole 79 exposing a part of the second common line 32 and a contact hole 76b exposing a part of the second common line connecting pattern 92 are formed. Also, a contact hole 75 exposing a part of the common pad line 54 and a contact hole 76a exposing a part of the second common line connecting pattern 92 are formed. Then, third and fourth connecting patterns 83 and 84 are formed over the contact holes, to connect the second common line 32, the second common line connecting pattern 92 and the common pad line 54 to one another.

[0074] Specifically, each second common line 32 and the second common line connecting pattern 92 are electrically connected to each other by the third connecting pattern 83 through the contact holes 79 and 76b. Each common pad line 54 and the second common line connecting pattern 92 are electrically connected to each other by the fourth connecting pattern 84 through the contact holes 75 and 76b.

[0075] The reason why the common pad line 54 and the second common line 32 are electrically connected to the second common line connecting pattern 92 by the connecting patterns 83 and 84 rather than being directly connected to each other is to prevent addition of a process. Generally, after the thin film transistors are formed and a protective film is deposited over the entire surface of the display panel 10, contact holes are formed in the drain electrodes of the thin film transistors and the pixel electrodes are formed so as to be electrically connected to the drain electrodes through the contact holes. With this procedure, the contact holes are formed after formation of the data lines. To electrically connect the common pad lines 54 and the second common lines 32 to the second common line connecting pattern 92, the contact holes must be formed prior to forming the common pad line 54 and the second common line 32.

[0076] Preferably, the third and fourth connecting patterns 83 and 84 are formed of the same layer as the pixel electrodes 29.

[0077] In the liquid crystal display device according to the second embodiment of the present invention, as shown in FIG. 4, the single second common line connecting pattern 92 is electrically connected to all the common pad lines provided in the neighboring data pad por-

tions 50. In conclusion, the first common voltage input terminals 64 provided in the respective data driver ICs 60 are electrically connected to the second common line connecting pattern 92.

[0078] The second common line connecting pattern 92 takes the form of an island arranged in a gap between the neighboring data driver ICs 60 and therefore, the second common line connecting pattern 92 does not overlap the adjacent data lines 24. This can reduce a parasitic capacitance occurring between the second common line connecting pattern 92 and the data lines 24 and therefore, can prevent uneven common voltage distribution due to an RC delay phenomenon.

[0079] A description of the liquid crystal display device according to the second embodiment of the present invention except for the common pad line, the data line and the second common line is identical to that of the liquid crystal display device according to the first embodiment of the present invention and thus, is replaced by the related description of the first embodiment.

[0080] Third Embodiment

[0081] FIG. 5 is a plan view illustrating an important part of a liquid crystal display device according to a third embodiment of the present invention, FIG. 6 is a sectional view of the liquid crystal display device according to the third embodiment of the present invention, illustrating a region where the data line and the second common line connecting pattern overlap each other, and FIG. 7 is a plan view of the liquid crystal display device according to the third embodiment of the present invention, illustrating line widths of overlapped portions of the data line and the second common line connecting pattern.

[0082] In the liquid crystal display device according to the third embodiment of the present invention, as shown in FIG. 5, the second common line connecting pattern 92 is formed to have an integral structure in the non-display area 14 between the data pad portions 50 and the display area 12, and has the effect of compensating for a minute difference in the common voltage supplied via the respective first common voltage input terminals 64 and the second common voltage input terminals 66.

[0083] A description of the liquid crystal display device according to the third embodiment of the present invention except for the second common line connecting pattern 92, the data line and the second common line connecting pattern is identical to that of the liquid crystal display device according to the second embodiment of the present invention and thus, is replaced by the related description of the second embodiment.

[0084] In the liquid crystal display device according to the third embodiment of the present invention, as shown in FIG. 6, a region where the second common line connecting pattern 92 and the data line 24 overlap each other is preferably provided with a semiconductor layer 23 such that the semiconductor layer 23 is interposed between the data line 24 and the second common line connecting pattern 92.

[0085] Although not described, reference numeral 26 refers to a gate insulating film.

[0086] If the semiconductor layer 23 is interposed between the data line 24 and the second common line connecting pattern 92, the semiconductor layer 23 serves as an insulator, whereby a parasitic capacitance between the second common line connecting pattern 92, to which the common voltage is supplied, and the data line 24 to which the data signal is supplied, can be reduced and consequently, uneven common voltage distribution due to the delay phenomenon can be prevented.

[0087] As shown in FIG. 6, when the data line 24 and the semiconductor layer 23 are etched simultaneously, the semiconductor layer 23 is exposed by a larger width than the data line 24 according to a difference in etching rate. This has the effect of preventing wire breakage in the data line 24 due to rapid height variation.

[0088] The semiconductor layer 23 is formed of the same layer as the semiconductor layer of the thin film transistor.

[0089] In the liquid crystal display device according to the third embodiment of the present invention, as shown in FIG. 7, overlapped portions of the data line 24 and the second common line connecting pattern 92 have different line widths from the remaining portions of the data line 24 and the second common line connecting pattern 92. This has the effect of preventing uneven common voltage distribution due to the delay phenomenon.

[0090] Specifically, the portion of the data line 24, overlapped with the second common line connecting pattern 92, has a greater width W1 than a width W2 of the remaining portion of the data line 24. On the other hand, the portion of the second common line connecting portion 92, overlapped with the data line 24, has a smaller width W3 than a width W4 of the remaining portion of the second common line connecting portion 92.

[0091] With this configuration, a line resistance in the data line 24 is reduced and consequently, a parasitic capacitance between the data line 24 and the second common line connecting pattern 92 is reduced, whereby uneven common voltage distribution due to the delay phenomenon can be substantially prevented.

[0092] Fourth Embodiment

[0093] FIG. 8 is a plan view illustrating an important part of a liquid crystal display device according to a fourth embodiment of the present invention, and FIG. 9 is an enlarged plan view of the liquid crystal display device according to the fourth embodiment of the present invention.

[0094] The liquid crystal display device according to the fourth embodiment of the present invention, as shown in FIG. 8, includes a plurality of the second common line connecting patterns 92, which are separated from one another, and the common voltage can be input via each first data driver IC individually. Specifically, at least two second common line connecting patterns 92 can be connected, separately, to a single data driver IC.

[0095] If the individual input of the common voltage is possible as described above, more efficient circuit tuning

is also possible.

[0096] In the liquid crystal display device according to the fourth embodiment of the present invention, as shown in FIG. 9, the second common lines 32 and the data lines 24 can be alternately arranged. Such alternate arrangement of the data lines 24 and the second common lines 32 has the effect of producing a symmetrical electric field within the display panel. Accordingly, the entire pattern is symmetrical and thus, the electric field can be more uniformly distributed throughout the display panel.

[0097] Although not shown, a description of the liquid crystal display device according to the fourth embodiment of the present invention except for the second common line, the data line and the second common line connecting pattern is identical to that of the liquid crystal display device according to the second embodiment of the present invention and thus, is replaced by the related description of the second embodiment.

[0098] Fifth Embodiment

[0099] FIG. 10 is a plan view illustrating a liquid crystal display device according to a fifth embodiment of the present invention.

[0100] The liquid crystal display device according to the fifth embodiment of the present invention, as shown in FIG. 10, further includes a third common line connecting pattern 94, which is formed in the non-display area 14 at an opposite side of the data pad portions 50 and is used to electrically connect the second common lines 32 to one another. Accordingly, more uniform common voltage distribution within the display panel can be accomplished.

[0101] Preferably, the third common line connecting pattern 94 is formed of the same layer as the second common lines 32. That is, both the third common line connecting pattern 94 and the second common lines 32 are formed of the same line as the data lines 24.

[0102] Sixth Embodiment

[0103] FIG. 11 is a plan view illustrating a liquid crystal display device according to a sixth embodiment of the present invention.

[0104] As shown in FIG. 11, there are provided the third common line connecting pattern 94, which is located in the non-display area 14 at the opposite side of the data pad portions 50 and is used to electrically connect the second common lines 32 to one another, and a pair of the first common line connecting patterns 90, which are formed at left and right sides of the display panel, respectively. Provision of both the third common line connecting pattern 94 and the first common line connecting patterns 90 accomplishes more uniform common voltage distribution.

[0105] The third common line connecting pattern 94, as shown in FIG. 12, may have a dual layer configuration consisting of a first pattern 94a formed of the same layer as the data lines, and a second pattern 94b formed of the same layer as the gate lines.

[0106] Although not shown, a protective insulating film is interposed between the first pattern 94a and the second pattern 94b.

[0107] The first pattern 94a and the second pattern 94b are electrically connected to each other by a fifth connecting pattern 86, which is patterned to cover a contact hole 77 exposing a part of the first pattern 94a and a contact hole 78 exposing a part of the second pattern 94b.

[0108] Preferably, a plurality of the contact holes 77 and 78 and a plurality of the fifth connecting patterns 86 are provided, to obtain a multi-contact structure.

[0109] The dual layer configuration of the third common line connecting pattern 94 causes a further reduction in resistance, resulting in more uniform common voltage distribution.

[0110] Seventh Embodiment

[0111] FIG. 13 is a plan view illustrating the configuration of a liquid crystal display device according to a seventh embodiment of the present invention.

[0112] As shown in FIG. 13, the liquid crystal display device according to the seventh embodiment of the present invention, as compared to the previously described liquid crystal display device according to the first embodiment of the present invention shown in FIG. 1, further includes a common voltage generator 102 to generate a common voltage, and a common voltage delay restrictor 200 to prevent a common voltage delay phenomenon. Other configurations of the present embodiment are identical to those of the first embodiment and thus, the following description focuses upon the common voltage generator 102 and the common voltage delay restrictor 200.

[0113] The common voltage generator 102 and the common voltage delay restrictor 200 may be mounted on a Printed Circuit Board (PCB).

[0114] The common voltage delay restrictor 200 includes a plurality of delay preventing patterns 2001 to 200n to prevent the common voltage delay phenomenon. The plurality of delay preventing patterns 2001 to 200n correspond to the first and second data driver ICs 60 and 62, respectively. For example, there are provided the first to n^{th} delay preventing patterns 2001 to 200n. The first to n^{th} delay preventing patterns 2001 to 200n individually supply common voltage control signals, generated on the basis of a common voltage delay rate, to the respective first and second data driver ICs 60 and 62. More specifically, the first to n^{th} delay preventing patterns 2001 to 200n generate the common voltage control signals, in consideration of a signal delay rate depending on an increased area of the display panel 10 or a signal delay rate depending on an increased length of supply lines connected to the common voltage generator 102. For this, the first to n^{th} delay preventing patterns 2001 to 200n include resistors R1 and Rn and capacitors C1 to Cn, respectively. Namely, the delay rate can be adjusted according to values of the resistors R1 to Rn and the capacitors C1 to Cn included in the respective first to n^{th} delay preventing patterns 2001 to 200n.

[0115] More specifically, the values of the resistors R1

to Rn and the capacitors C1 to Cn provided in the first to n^{th} delay preventing patterns 2001 to 200n must decrease from the first delay preventing pattern 2001 toward the n^{th} delay preventing pattern 200n. In other words, the values of the resistors R1 to Rn and the capacitors C1 to Cn provided in the first to n^{th} delay preventing patterns 2001 to 200n decrease as a common voltage delay rate increases. This is represented by the following Equation:

[0116] R1C1 > R2C2 > R3C3... > RnCn.

[0117] Values of the resistors R1 to Rn and the capacitors C1 to Cn of the respective first to n^{th} delay preventing patterns 2001 to 200n are calculated using the above Equation. Accordingly, the first to n^{th} delay preventing patterns 2001 to 200n can individually supply the common voltage control signals depending on the common voltage delay rate to the first and second data driver ICs 60 and 62, supplying a uniform common voltage to the display panel 10.

[0118] Eighth Embodiment

[0119] FIG. 14 is a plan view illustrating an important part of a liquid crystal display device according to an eighth embodiment of the present invention.

[0120] As shown in FIG. 14, the liquid crystal display device according to the eighth embodiment of the present invention, as compared to the previously described liquid crystal display device according to the second embodiment of the present invention shown in FIG. 4, further includes the common voltage generator 102 to generate a common voltage, and the common voltage delay restrictor 200 to prevent a common voltage delay phenomenon. Other configurations of the present embodiment are identical to those of the second embodiment and thus, the following description focuses upon the common voltage generator 102 and the common voltage delay restrictor 200.

[0121] The common voltage delay restrictor 200 includes the plurality of delay preventing patterns 2001 to 200n. For example, there are provided the first to n^{th} delay preventing patterns 2001 to 200n. The first to n^{th} delay preventing patterns 2001 to 200n are connected individually to the first and second data driver ICs 60 and 62, to supply common voltage control signals to the respective first and second data driver ICs 60 and 62. More specifically, to apply the common voltage control signals from the first to n^{th} delay preventing patterns 2001 to 200n, output lines of the first to n^{th} delay preventing patterns 2001 to 200n are connected to the common voltage input terminals 64 and 66 provided in the respective data driver ICs 60 and 62.

[0122] Ninth Embodiment

[0123] FIG. 15 is a plan view illustrating an important part of a liquid crystal display device according to a ninth embodiment of the present invention.

[0124] As shown in FIG. 15, the liquid crystal display device according to the ninth embodiment of the present invention, as compared to the previously described liquid crystal display device according to the third embodiment of the present invention shown in FIG. 5, further includes the common voltage generator 102 to generate a common voltage, and the common voltage delay restrictor 200 to prevent a common voltage delay phenomenon. Other configurations of the present embodiment are identical to those of the third embodiment and thus, the following description focuses upon the common voltage generator 102 and the common voltage delay restrictor 200.

[0125] The common voltage delay restrictor 200 includes the plurality of delay preventing patterns 2001 to 200n. For example, there are provided the first to n^{th} delay preventing patterns 2001 to 200n. At least one of the plurality of delay preventing patterns 2001 to 200n is connected to the respective first and second data driver ICs 60 and 62, to supply at least one common voltage control signal to the respective data driver ICs 60 and 62.

[0126] Tenth Embodiment

[0127] FIG. 16 is a plan view illustrating an important part of a liquid crystal display device according to a tenth embodiment of the present invention.

[0128] As shown in FIG. 16, the liquid crystal display device according to the tenth embodiment of the present invention, as compared to the previously described liquid crystal display device according to the fourth embodiment of the present invention shown in FIG. 8, further includes the common voltage generator 102 to generate a common voltage, and the common voltage delay restrictor 200 to prevent a common voltage delay phenomenon. Other configurations of the present embodiment are identical to those of the fourth embodiment and thus, the following description focuses upon the common voltage generator 102 and the common voltage delay restrictor 200.

[0129] The common voltage delay restrictor 200 includes the plurality of delay preventing patterns 2001 to 200n. For example, there are provided the first to n^{th} delay preventing patterns 2001 to 200n. At least one of the plurality of delay preventing patterns 2001 to 200n is connected to the respective first and second data driver ICs 60 and 62, to supply at least one common voltage control signal to the respective data driver ICs 60 and 62.

[0130] Eleventh Embodiment

[0131] FIG. 17 is a plan view illustrating an important part of a liquid crystal display device according to an eleventh embodiment of the present invention.

[0132] As shown in FIG. 17, the liquid crystal display device according to the eleventh embodiment of the present invention, as compared to the previously described liquid crystal display device according to the fifth embodiment of the present invention shown in FIG. 10, further includes the common voltage generator 102 to generate a common voltage, and the common voltage delay restrictor 200 to prevent a common voltage delay phenomenon. Other configurations of the present embodiment are identical to those of the fifth embodiment and the common voltage delay restrictor 200 is identical to that of FIG. 13.

[0133] Twelfth Embodiment

[0134] FIG. 18 is a plan view illustrating an important part of a liquid crystal display device according to a twelfth embodiment of the present invention.

[0135] As shown in FIG. 18, the liquid crystal display device according to the twelfth embodiment of the present invention, as compared to the previously described liquid crystal display device according to the sixth embodiment of the present invention shown in FIG. 11, further includes the common voltage generator 102 to generate a common voltage, and the common voltage delay restrictor 200 to prevent a common voltage delay phenomenon. Other configurations of the present embodiment are identical to those of the sixth embodiment and the common voltage delay restrictor 200 is identical to that of FIG. 13.

[0136] Thirteenth Embodiment

[0137] FIG. 19 is a plan view illustrating an important part of a liquid crystal display device according to a thirteenth embodiment of the present invention.

[0138] As shown in FIG. 19, the liquid crystal display device according to the thirteenth embodiment of the present invention, as compared to the previously described liquid crystal display device according to the seventh embodiment of the present invention shown in FIG. 13, further includes gate driver ICs 302 and a LOG-type signal line group 300 connected to each gate driver IC 302, which are formed in the display area 14.

[0139] The LOG type signal line group 300 is made of a gate metal layer in the same manner as the gate lines 22. A resistance value of the LOG type signal line group 300 is proportional to a line length and therefore, exhibits a signal delay as the LOG type signal line group 300 is more distant from the PCB. However, as shown in FIG. 19, when the plurality of delay preventing patterns 2001 to 200n are provided to correspond to the respective first and second data driver ICs 60 and 62 so as to achieve uniform common voltage supply, improved display quality can be accomplished. The plurality of delay preventing patterns 2001 to 200n have the same functions and effects, as described with reference to FIG. 13, and thus, a description thereof will be omitted.

[0140] FIG. 20A is a view illustrating common voltage distribution within a conventional display panel, and FIG. 20B is a view illustrating common voltage distribution in the liquid crystal display device according to the present invention.

[0141] As shown in FIGs. 20A and 20B, the liquid crystal display device according to the embodiments of the present invention can achieve more uniform common voltage distribution than the prior art.

[0142] In particular, in the case of a wide panel having a screen ratio of 16 : 9 suitable for display of moving images, when a common voltage is supplied only via first common lines parallel to gate lines because the display panel is lengthened in a gate line direction, the first common lines undergo an increase in resistance and thus, exhibit serious uneven common voltage distribution due to a delay phenomenon depending on RC time constants. However, in the liquid crystal display device according to the embodiments of the present invention, a common voltage can be supplied via not only the first common lines parallel to the gate lines but also the second common lines parallel to the data lines, achieving a remarkable improvement in uniformity of common voltage distribution.

[0143] Further, the common voltage can be applied to the respective data driver ICs, achieving uniform common voltage distribution and preventing a crosstalk phenomenon.

[0144] Furthermore, the common lines formed vertically and horizontally can prevent wire brakeage failure thereof.

[0145] It will be apparent to those skilled in the art that various modifications and variations can be made in the present invention without departing from the spirit or scope of the inventions. Thus, it is intended that the present invention covers the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

Claims

1. A liquid crystal display device comprising:

a display panel including a display area and a non-display area surrounding the display area;
a plurality of gate lines and data lines arranged on the display area to intersect each other, so as to define a plurality of pixel regions;
thin-film transistors formed at respective intersections of the gate lines and the data liens;
pixel electrodes formed on the respective pixel regions and connected to the thin film transistors;
a plurality of first common lines provided between the neighboring gate lines and arranged parallel to the gate lines; and
a plurality of second common lines provided between the neighboring data lines and arranged parallel to the data lines, the second common lines being electrically connected to the first common lines.

2. The liquid crystal display device according to claim 1, wherein each first common line and each second common line have a first contact hole and a second contact hole at an intersection thereof, and are electrically connected to each other by a first connecting pattern through the first and second contact holes, the first connecting pattern being formed of the same layer as the pixel electrodes.

3. The liquid crystal display device according to claim 1, further comprising:

a plurality of data pad portions on the non-display area, each data pad portion including data pad lines and common pad lines;
first data driver ICs connected to the respective data pad portions except for opposite end data pad portions;
second data driver ICs connected to the opposite end data pad portions; and
at least one first common voltage input terminal provided in at least one of the first data driver ICs for supplying a common voltage to each second common line via the common pad lines.

4. The liquid crystal display device according to claim 3, further comprising:

at least one second common voltage input terminal provided in at least one of the second data driver ICs for supplying a common voltage to plurality of first common lines; and
at least one first common line connecting pattern for supplying the common voltage from the second common voltage input terminal to the plurality of first common lines.

5. The liquid crystal display device according to claim 4, wherein the data pad lines, the common pad lines, the second common lines, and the first common line connecting pattern are formed of the same layer as the data lines.

6. The liquid crystal display device according to claim 4, wherein each first common line and the first common line connecting pattern are electrically connected to each other by a second connecting pattern through a third contact hole exposing a part of the first common line and a fourth contact hole exposing a part of the first common line connecting pattern, the second connecting pattern being formed of the same layer as the pixel electrodes.

7. The liquid crystal display device according to claim 3, further comprising:

a second common line connecting pattern provided on the non-display area between the plurality of data pad portions and the display area, and connecting the common pad lines and the second common lines to each other.

8. The liquid crystal display device according to claim 7, wherein the first common lines and the second common line connecting pattern are formed of the same layer as the gate lines.

9. The liquid crystal display device according to claim 7, wherein each second common line and the second common line connecting pattern are electrically connected to each other by a third connecting pattern through a fifth contact hole exposing a part of the second common line and a sixth contact hole exposing a part of the second common line connecting pattern, the third connecting pattern being formed of the same layer as the pixel electrodes, and
wherein each common pad line and the second common line connecting pattern are electrically connected to each other by a fourth connecting pattern through a seventh contact hole exposing a part of the common pad line and an eighth contact hole exposing a part of the second common line connecting pattern, the fourth connecting pattern being formed of the same layer as the pixel electrodes.

10. The liquid crystal display device according to claim 7, wherein the second common line connecting pattern includes a plurality of island-shaped second common line connecting patterns, each arranged between the data driver ICs and connected to the common pad lines provided in the two neighboring first driver ICs, or at least two island-shaped second common line connecting patterns arranged at each data driver IC and each connecting one common pad line and at least two common pad lines.

11. The liquid crystal display device according to claim 7, wherein a semiconductor layer is interposed between the second common line connecting pattern and the data lines at a region where the second common line connecting pattern and each data line overlap each other.

12. The liquid crystal display device according to claim 11, wherein a portion of each data line overlapped with the second common line connecting pattern has a greater line width than a line width of the remaining portion of the data line, and a portion of the second common line connecting pattern overlapped with the data line has a smaller line width than a line width of the remaining portion of the second common line connecting pattern.

13. The liquid crystal display device according to claim 4, further comprising:

a third common line connecting pattern provided in the non-display area at an opposite side of the data pad portions and electrically connecting the second common lines and the first common line connecting pattern.

14. The liquid crystal display device according to claim 13, wherein the third common line connecting pattern has a dual layer structure consisting of a first pattern formed of the same layer as the data lines and a second pattern formed of the same layer as the gate lines and electrically connected to the first pattern.

15. The liquid crystal display device according to claim 1, further comprising:

a common voltage delay restrictor to supply common voltage control signals to the first and second common lines so as to prevent a common voltage delay phenomenon.

16. The liquid crystal display device according to claim 15, wherein the common voltage delay restrictor includes a plurality of delay preventing patterns, and each delay preventing pattern has at least one resistor and at least one capacitor having different values from those of the other delay preventing patterns.

17. The liquid crystal display device according to claim 16, wherein values of the resistor and the capacitor included in the respective delay preventing patterns decrease as a common voltage delay rate increases.

18. The liquid crystal display device according to claim 16, wherein at least one of the plurality of delay preventing patterns is connected to the respective first and second data driver ICs, to supply at least one common voltage control signal to the respective first and second data driver ICs.

FIG. 1

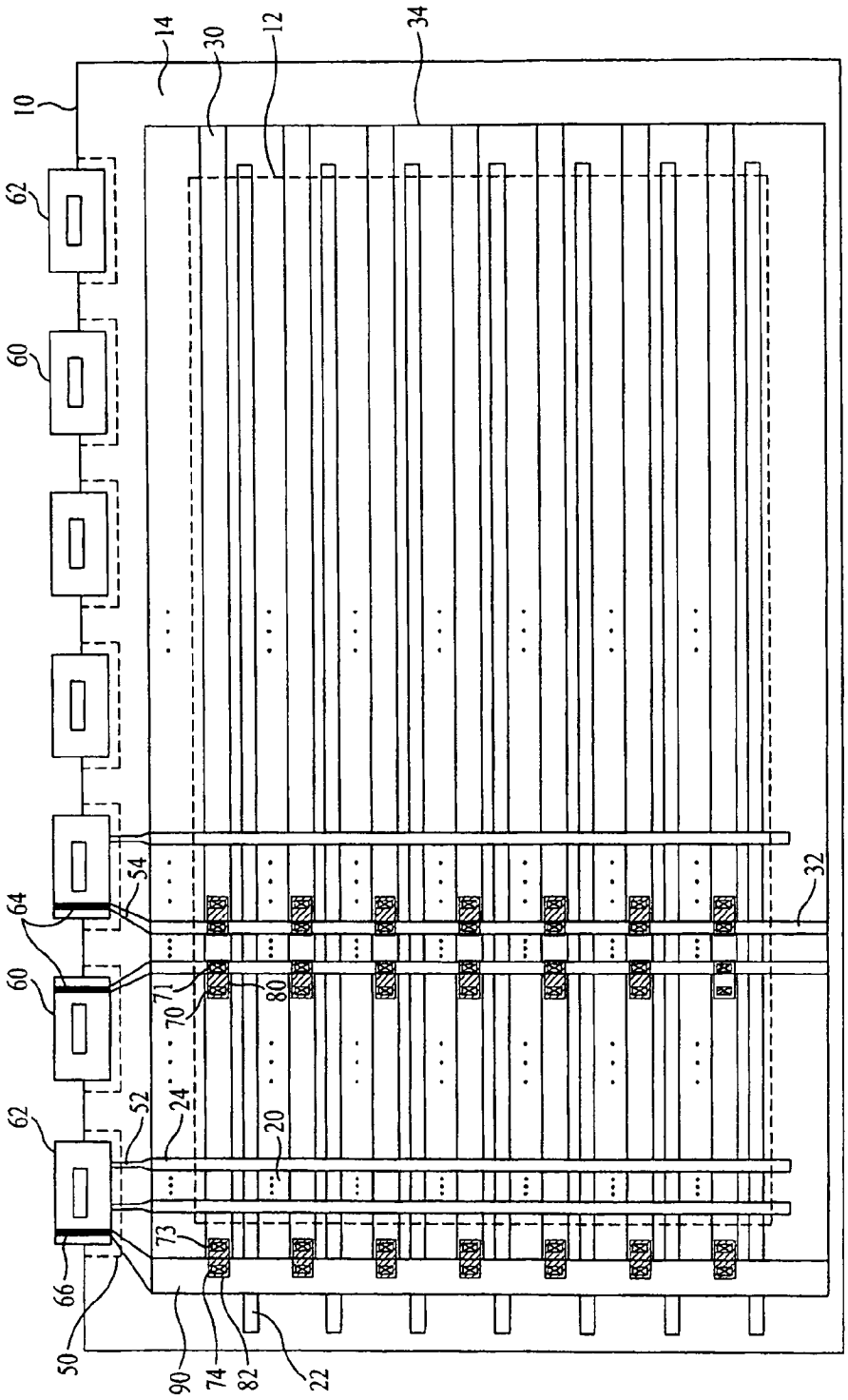

14
30
12
34
10
62
60
60
62
64
54
32
71
70
80
52
24
20
73
66
50
90
74
82
22

FIG. 2

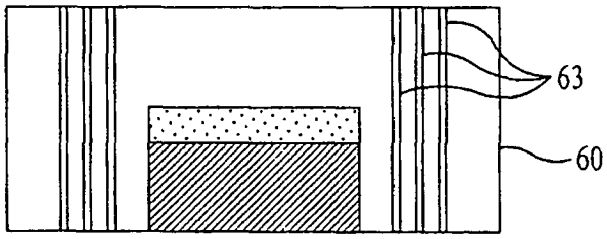


FIG. 3

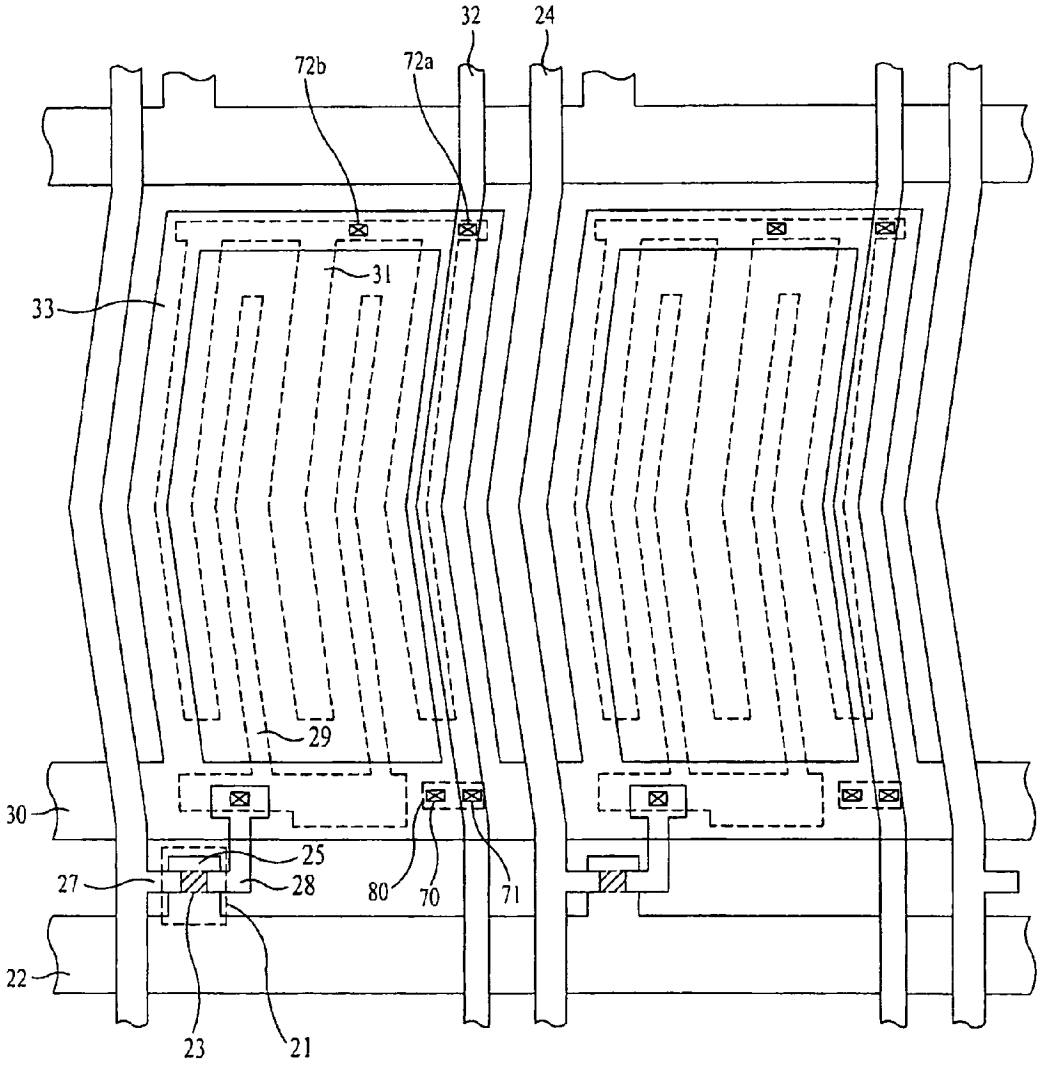


FIG. 4

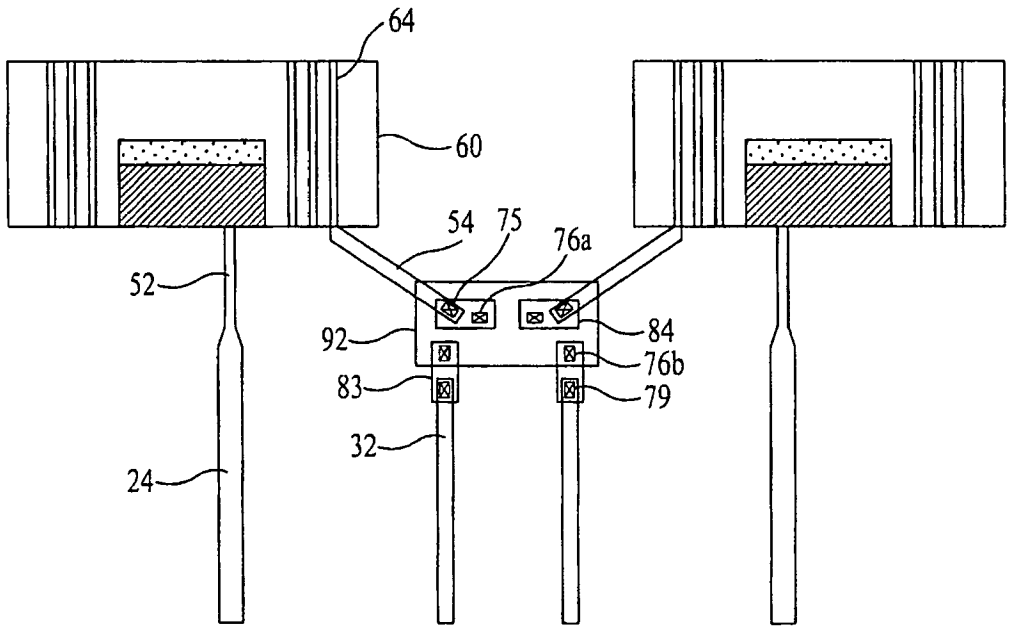


FIG. 5

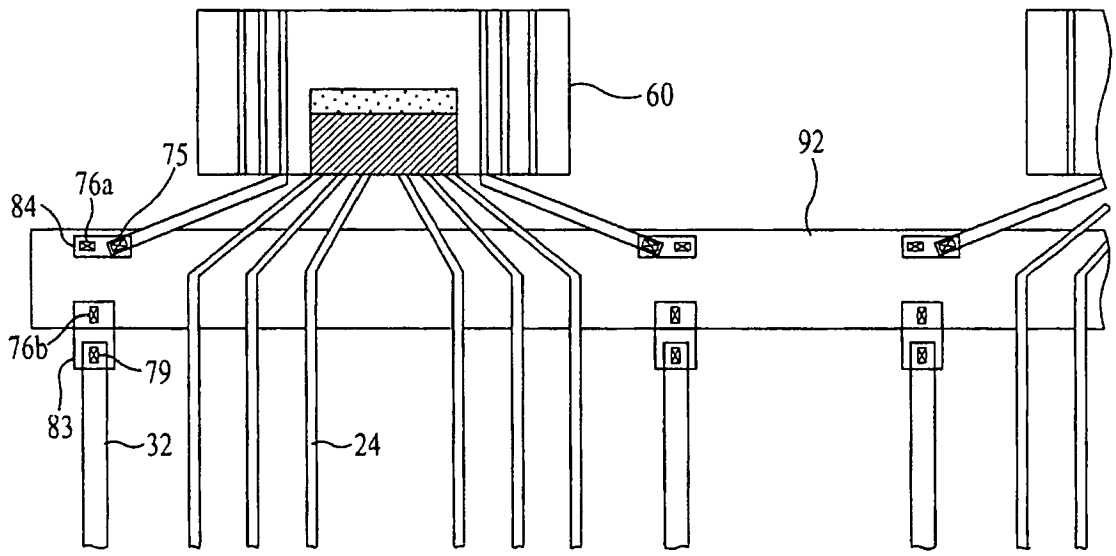


FIG. 6

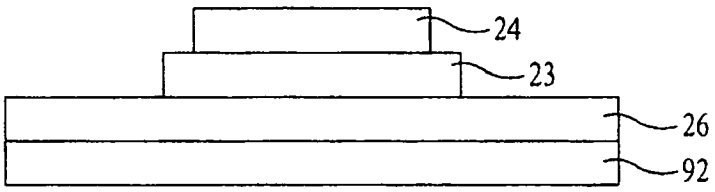


FIG. 7

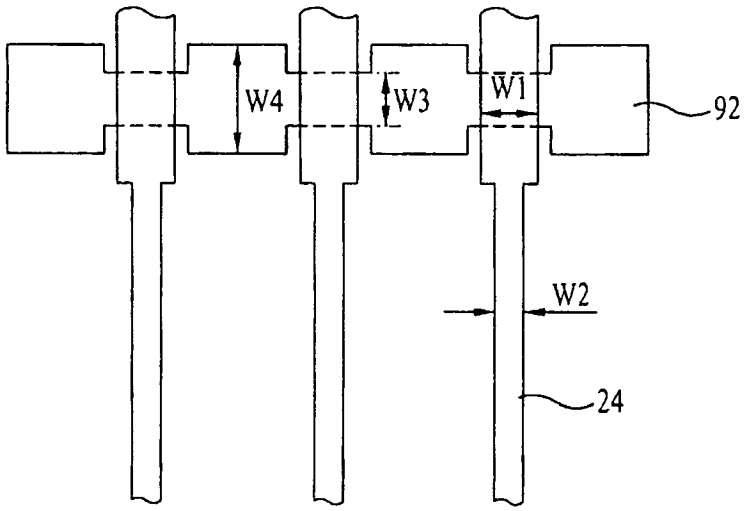


FIG. 8

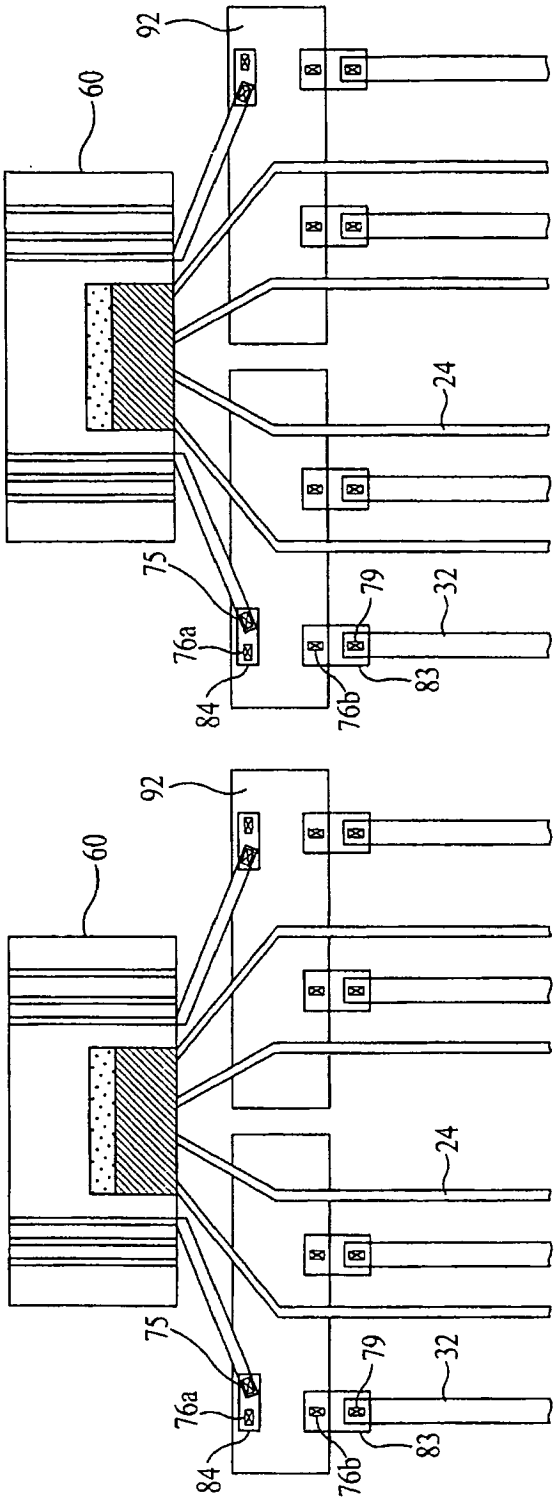


FIG. 9

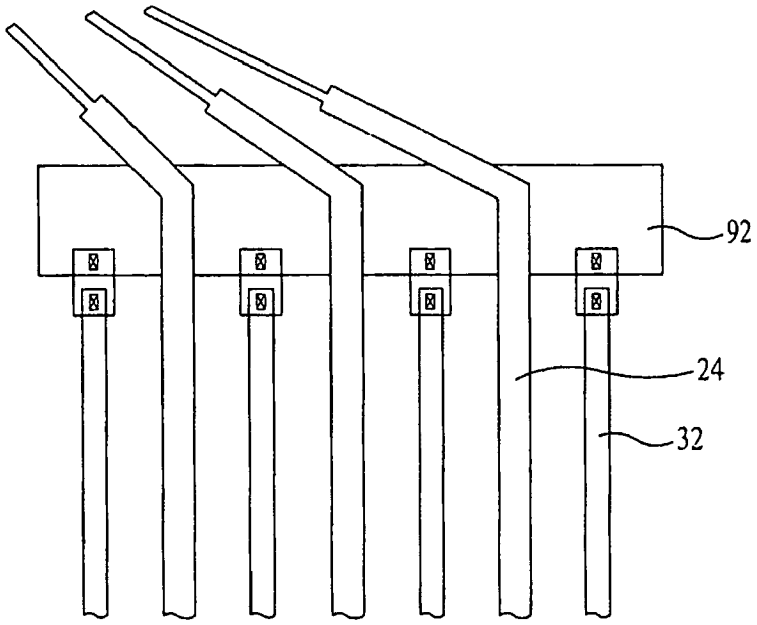


FIG. 10

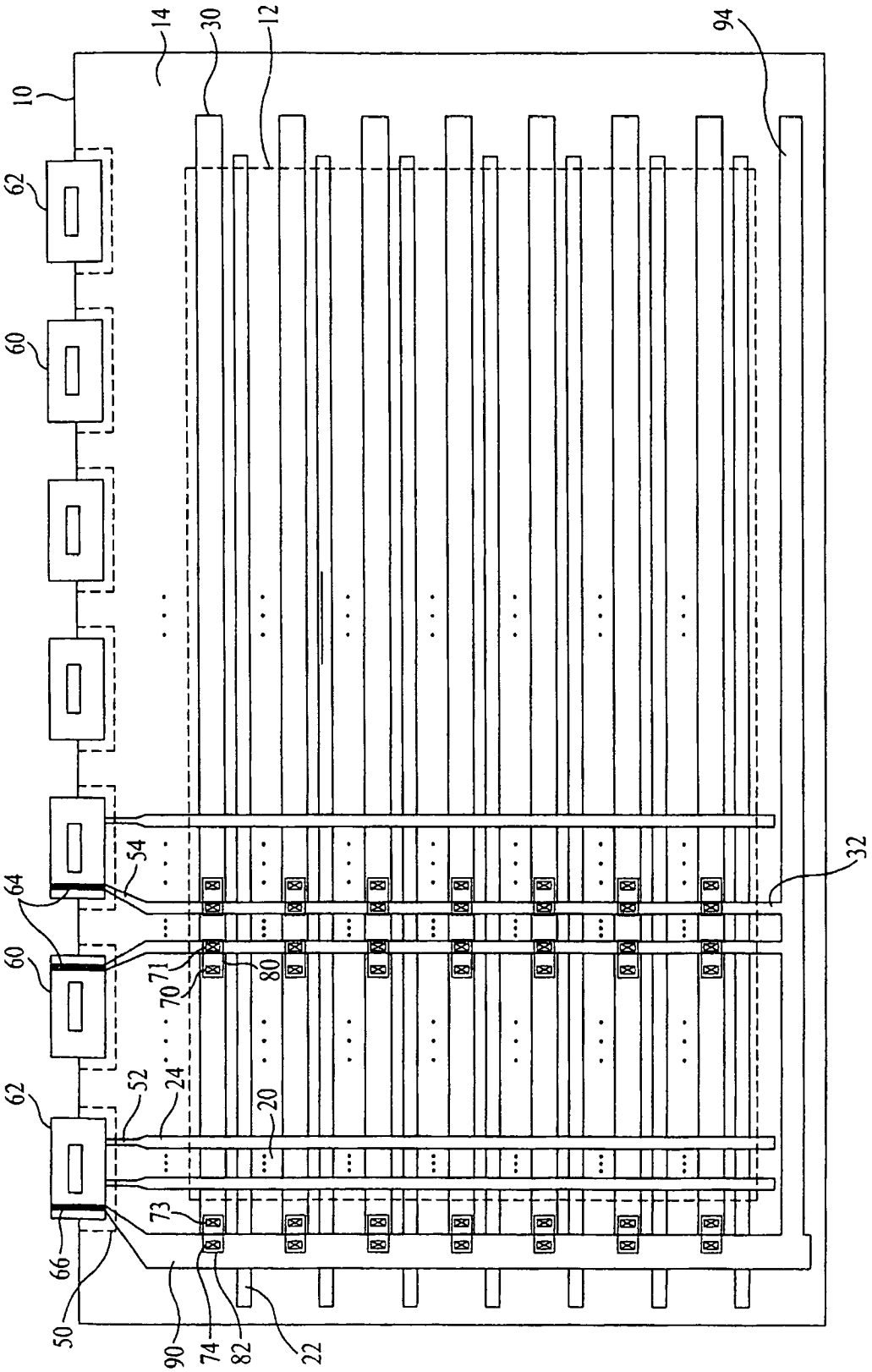

14
30
12
94
10
62
60
54
64
60
71
70
80
32
62
52
24
20
73
66
50
90
74
82
22

FIG. 11

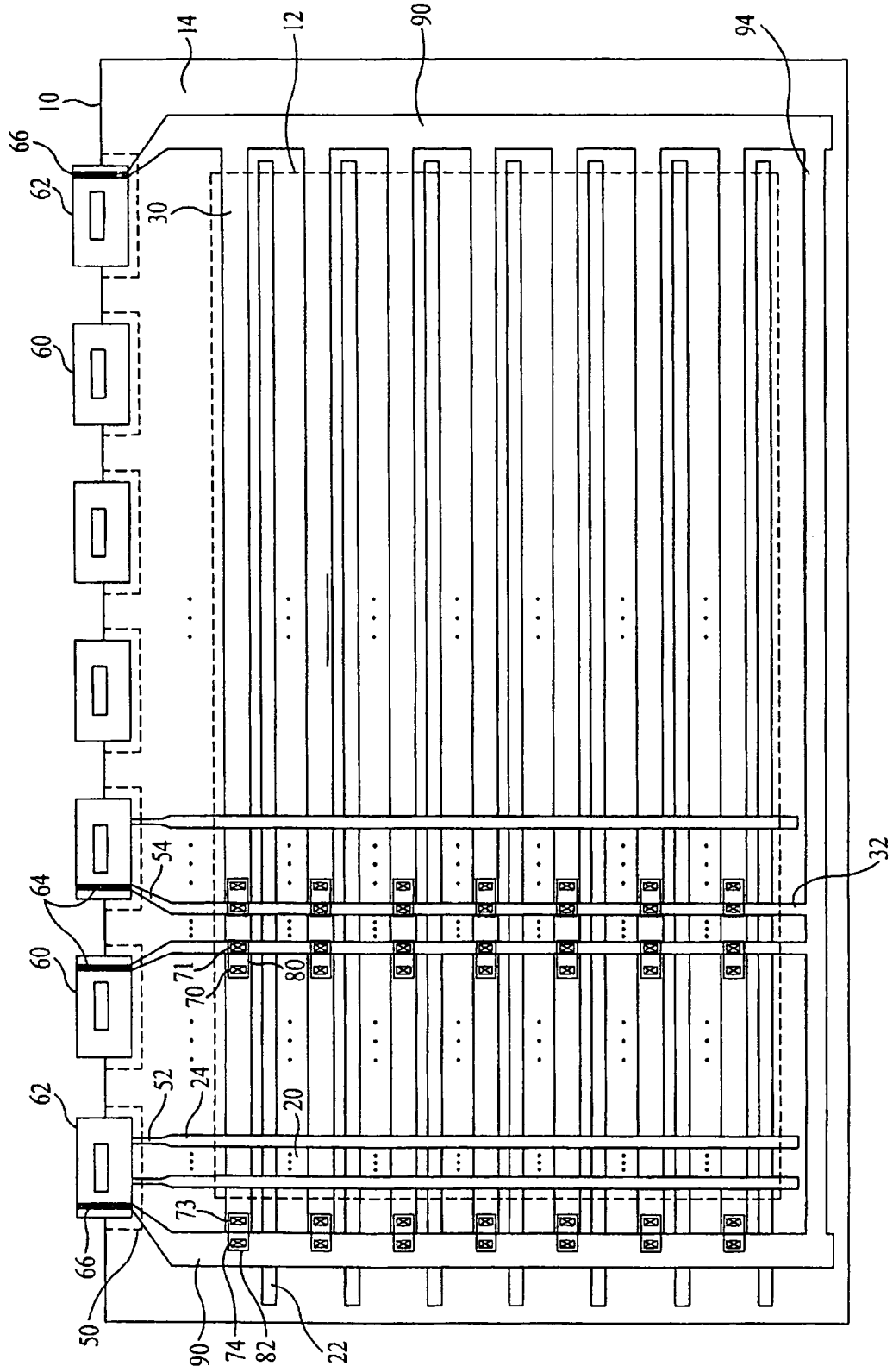


FIG. 12

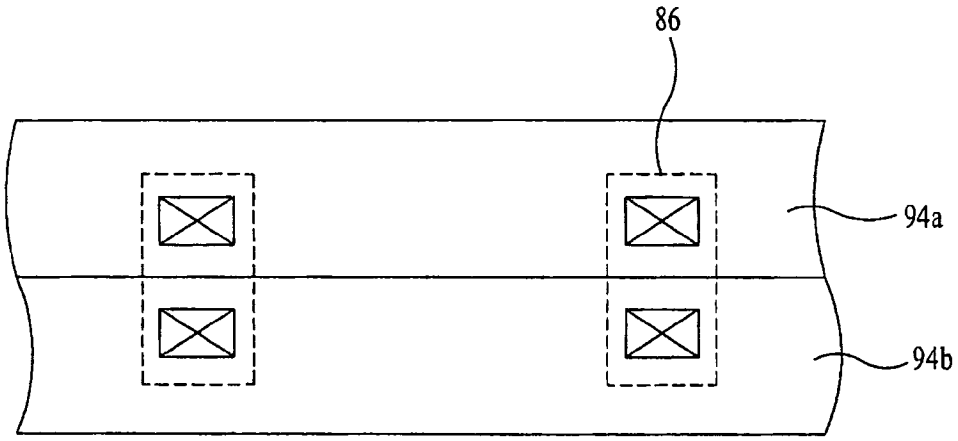


FIG. 13

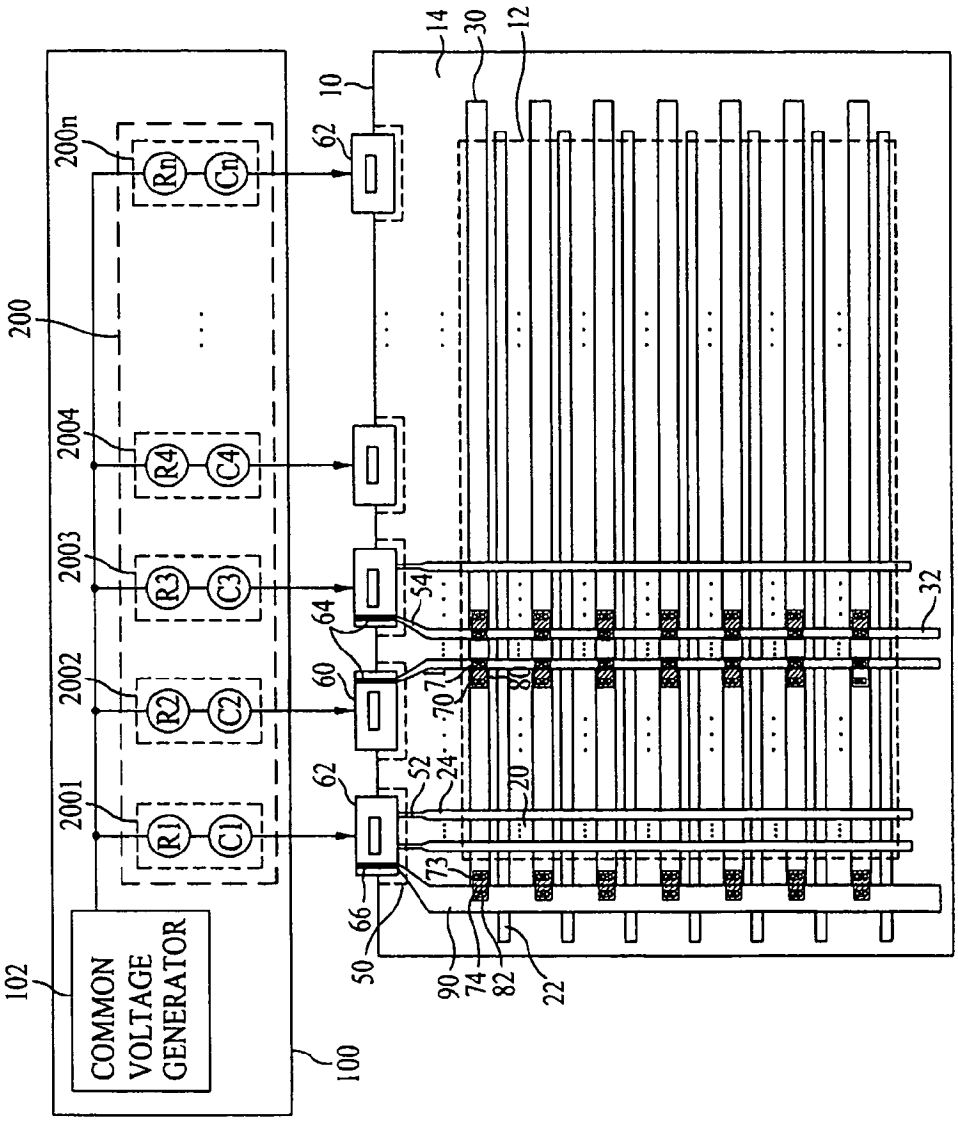

COMMON VOLTAGE GENERATOR
100
102
200
200n
2001
2002
2003
2004
R1
C1
R2
C2
R3
C3
R4
C4
Rn
Cn
10
12
14
20
22
24
30
32
50
52
54
60
62
64
66
70
71
73
74
80
82
90

FIG. 14

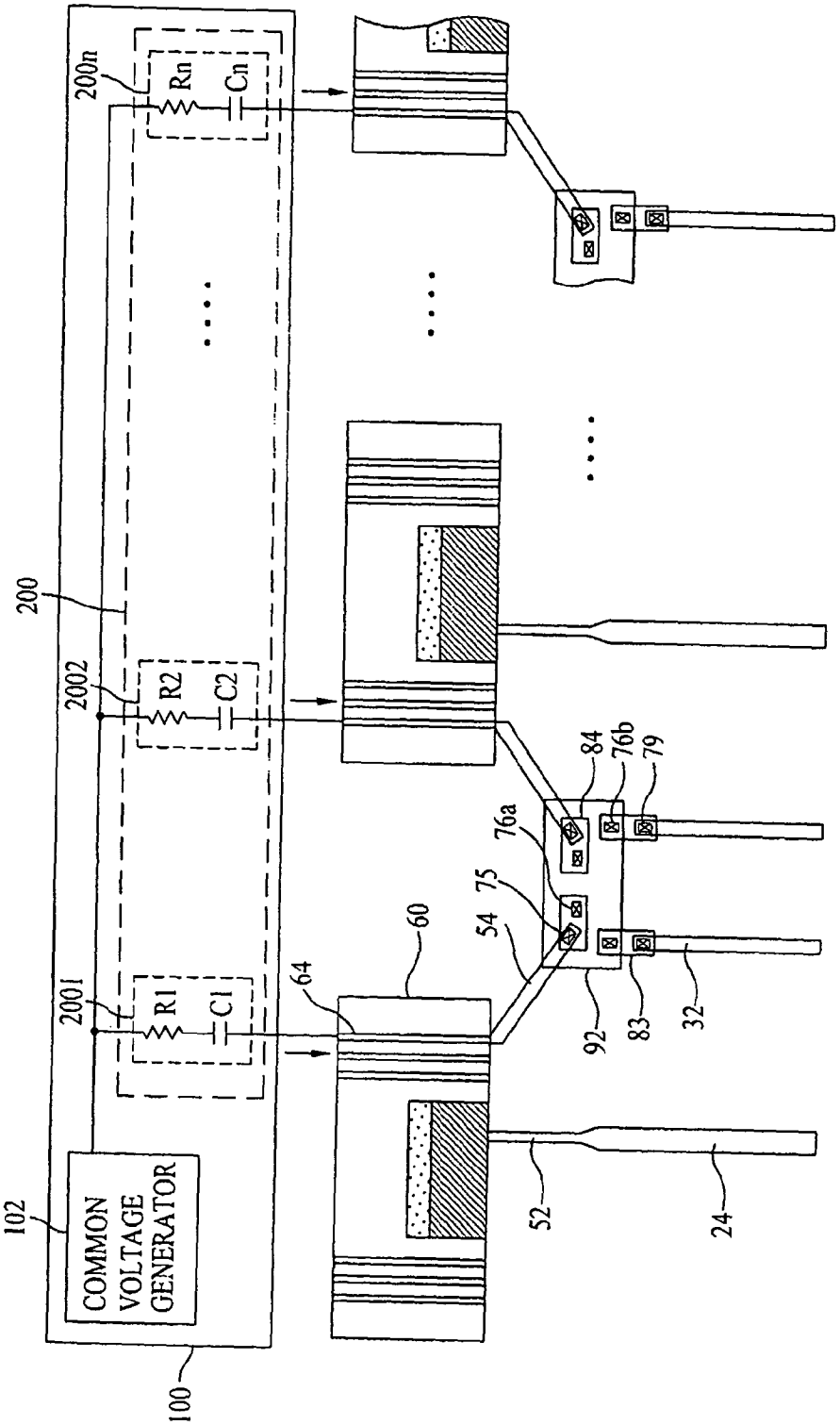

200n
Rn
Cn
200
2002
R2
C2
2001
R1
C1
102
COMMON VOLTAGE GENERATOR
100
64
60
54
75
76a
84
76b
79
92
83
32
52
24

FIG. 15

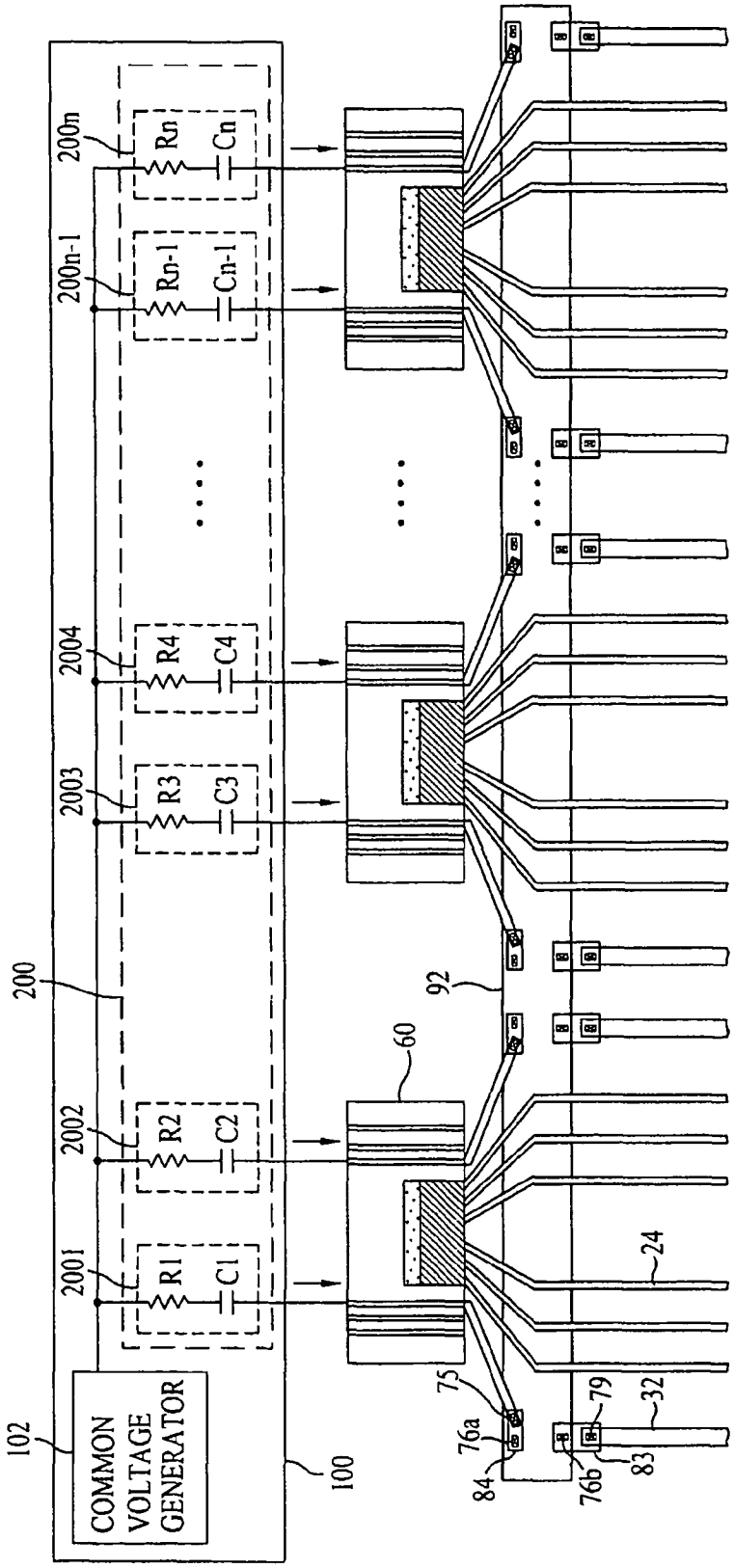

200n
Rn
Cn
200n-1
Rn-1
Cn-1
2004
R4
C4
2003
R3
C3
200
92
60
2002
R2
C2
2001
R1
C1
24
75
79
32
76a
84
76b
83
102
COMMON VOLTAGE GENERATOR
100

FIG. 16

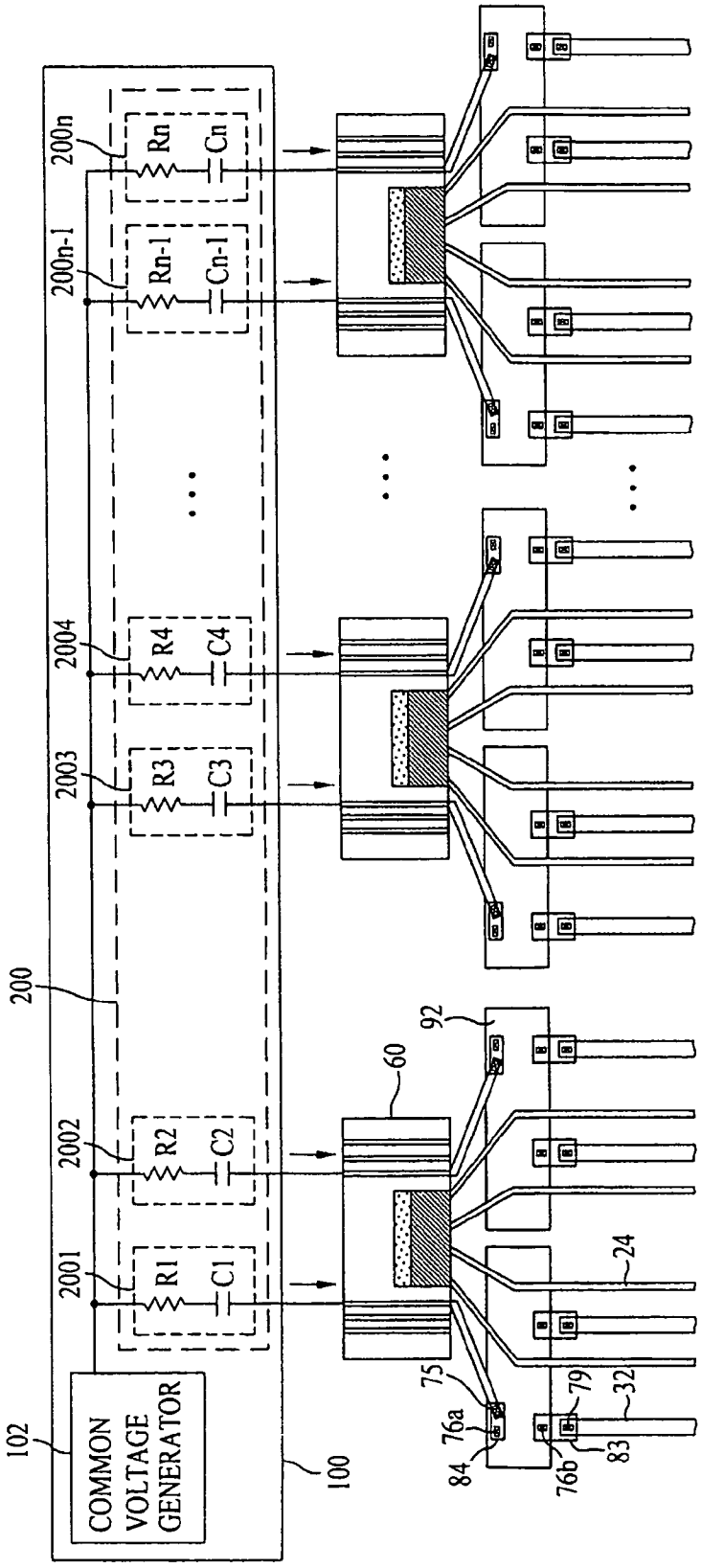

200n
Rn
Cn
200n-1
Rn-1
Cn-1
2004
R4
C4
2003
R3
C3
200
2002
R2
C2
2001
R1
C1
COMMON VOLTAGE GENERATOR
102
100
60
92
24
75
76a
84
79
32
83
76b

FIG. 17

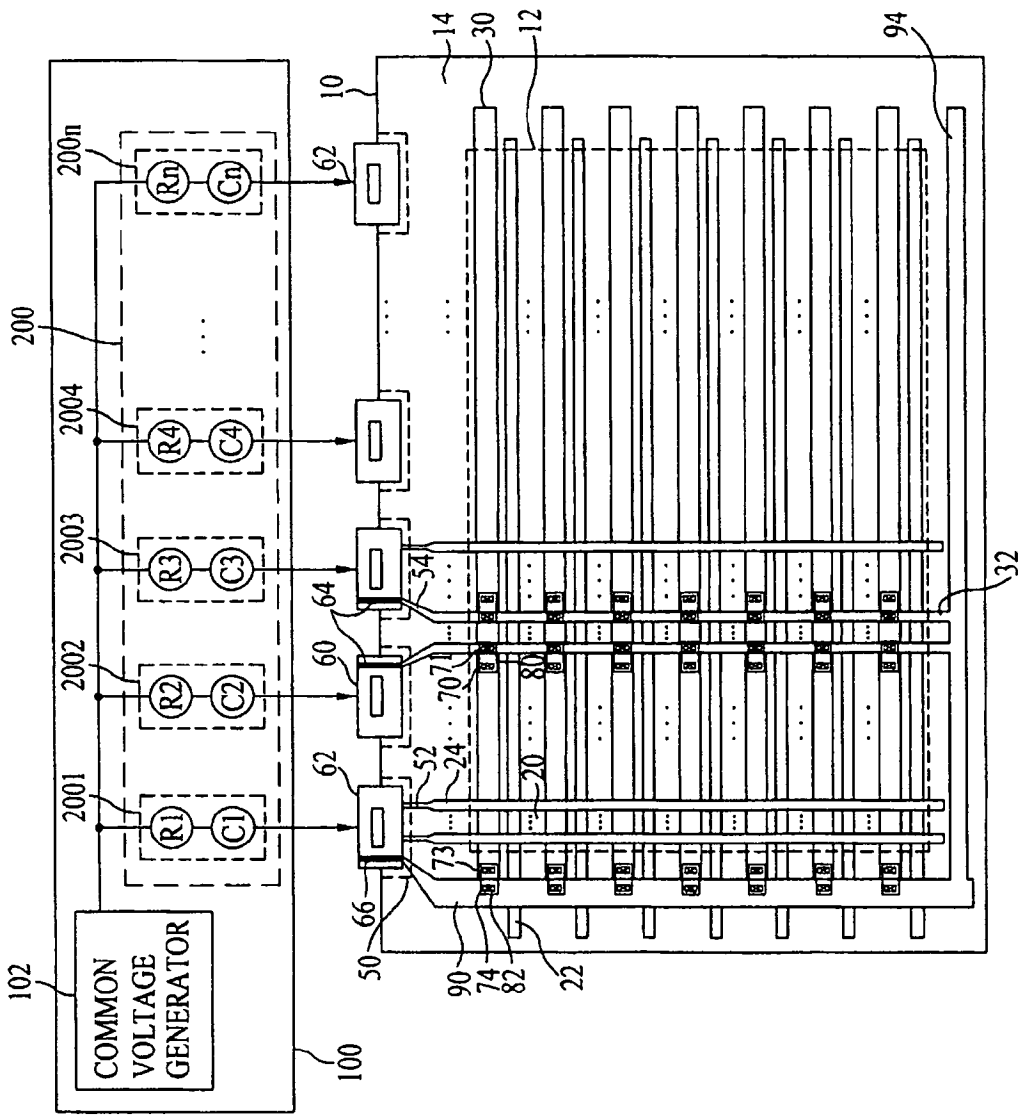

COMMON VOLTAGE GENERATOR
100
102
200
200n
2004
2003
2002
2001
Rn
Cn
R4
C4
R3
C3
R2
C2
R1
C1
10
14
30
12
94
32
34
64
60
62
52
24
20
70
71
80
73
66
50
90
74
82
22

FIG. 18

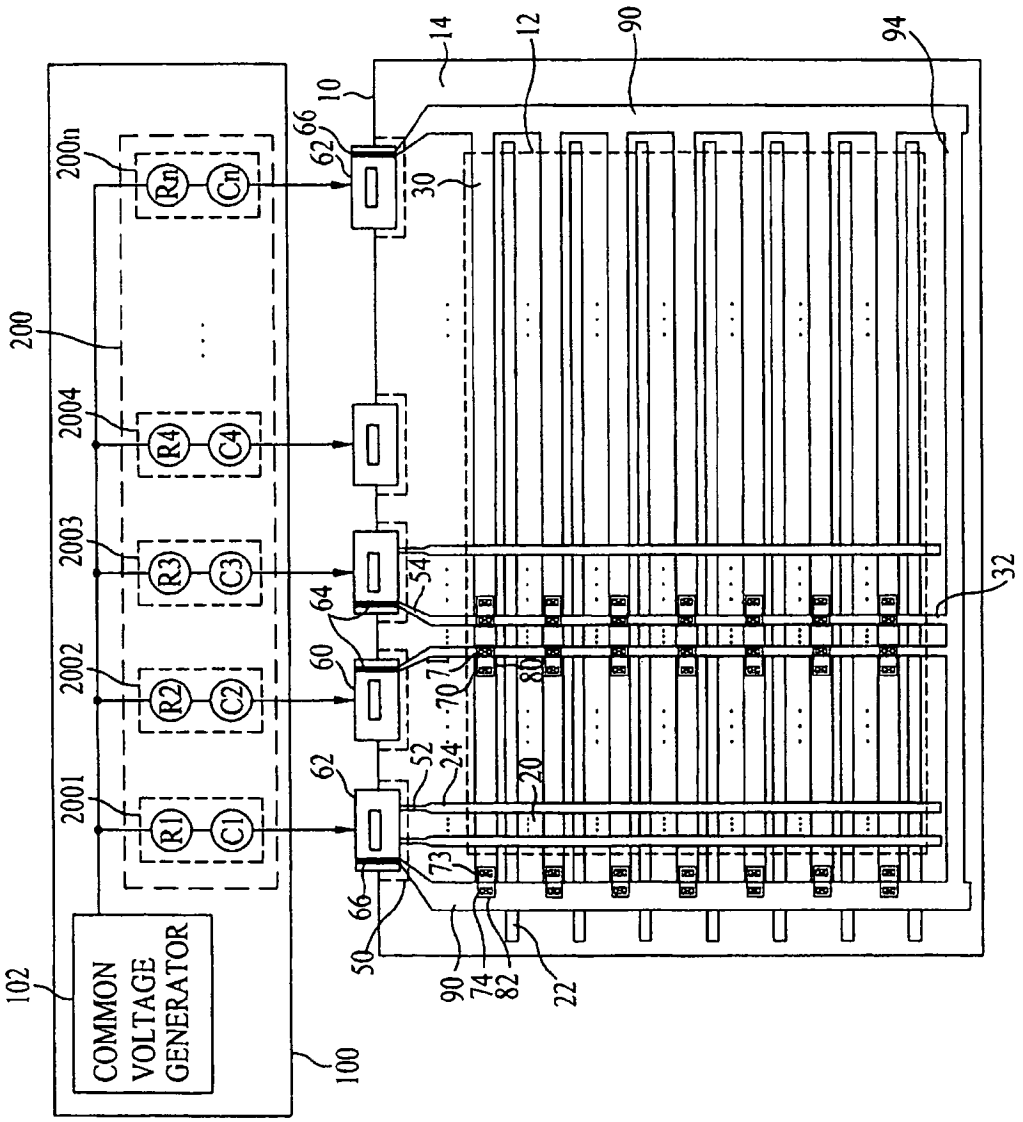

COMMON VOLTAGE GENERATOR
100
102
200
200n
2001
2002
2003
2004
R1
C1
R2
C2
R3
C3
R4
C4
Rn
Cn
10
12
14
20
22
24
30
32
34
50
52
54
60
62
64
66
70
71
73
74
80
82
90
94

FIG. 19

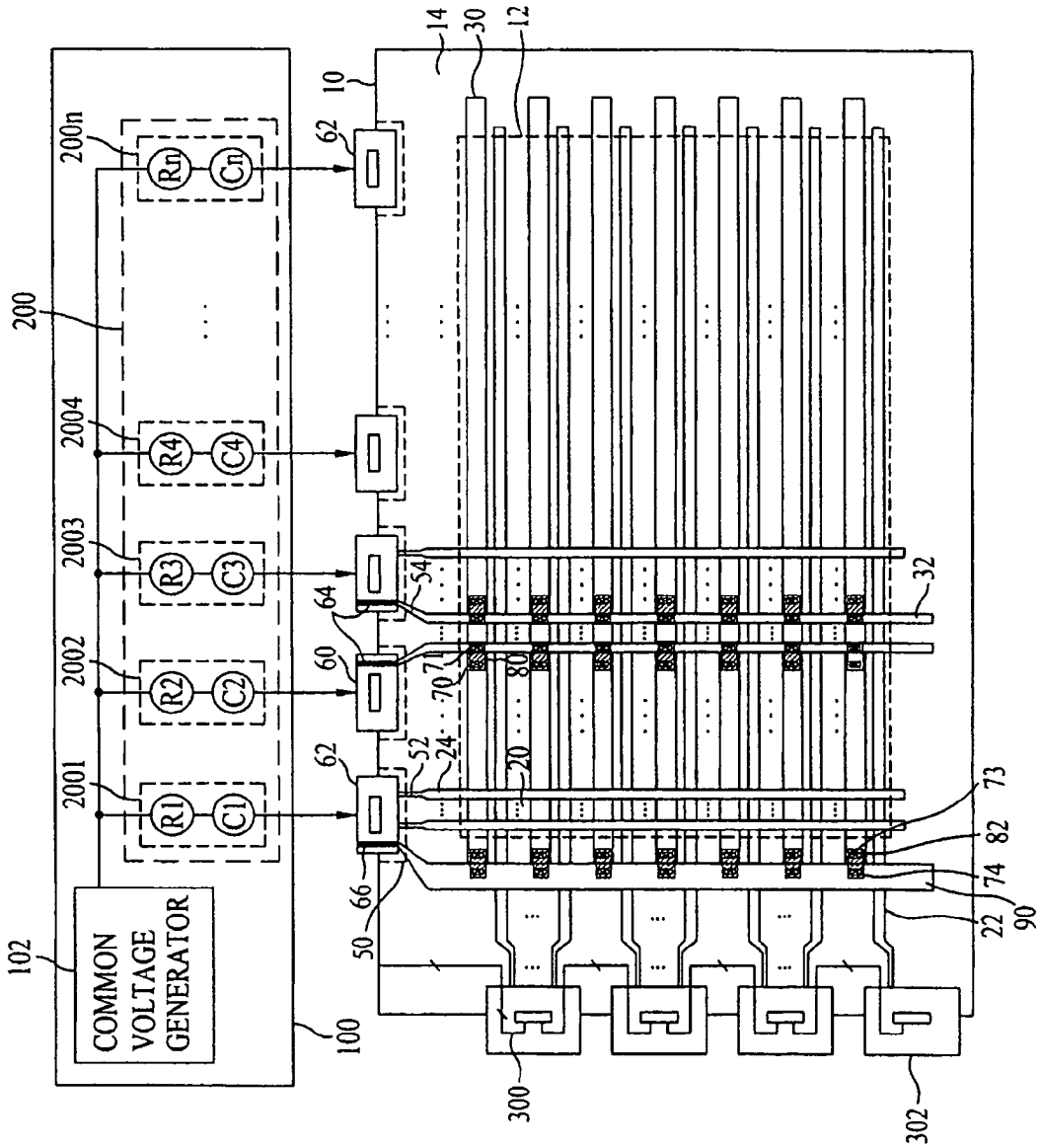
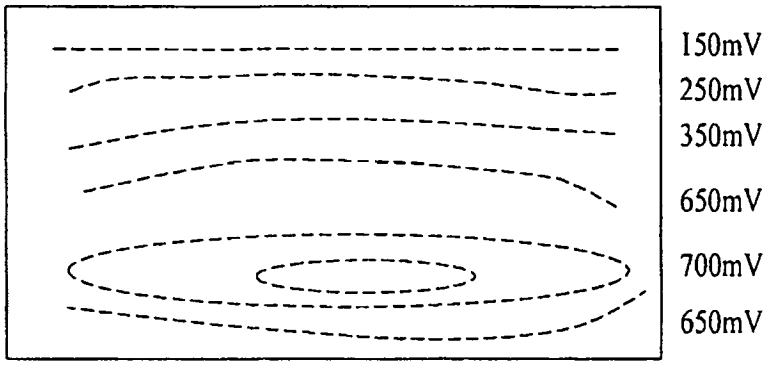
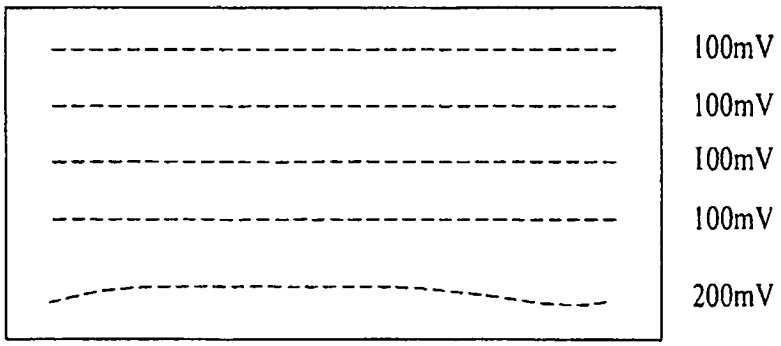

COMMON VOLTAGE GENERATOR
102
100
200
200n
2004
2003
2002
2001
Rn
Cn
R4
C4
R3
C3
R2
C2
R1
C1
10
14
30
12
62
64
60
54
32
52
24
20
70
71
80
66
50
73
82
74
22
90
300
302

FIG. 20A



<Prior Art : Vcom change measurement result>

FIG. 20B



<Improvement : Vcom change measurement result>

Europäisches Patentamt
European Patent Office
Office européen des brevets

EUROPEAN SEARCH REPORT

Application Number
EP 08 01 2877

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	US 2006/001789 A1 (AHN BYUNG C [KR]) 5 January 2006 (2006-01-05) * paragraph [0075]; figure 2 * -----	1-10, 13-18	INV. G02F1/1345 G02F1/1362
X	US 2003/133066 A1 (ONO KIKUO [JP] ET AL) 17 July 2003 (2003-07-17) * figures 1,13 * and the corresponding text passages	1	
A	-----	1-18	
X	US 2003/227590 A1 (OKE RYUTARO [JP] ET AL) 11 December 2003 (2003-12-11) * figures 1,11 * and the corresponding text passages	1	
A	-----	1-18	

TECHNICAL FIELDS SEARCHED (IPC)

G02F
H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
Munich	11 November 2008	Lüssem, Georg

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons
.....
& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

3

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 08 01 2877

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

11-11-2008

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2006001789 A1	05-01-2006	KR 20060000961 A	06-01-2006
US 2003133066 A1	17-07-2003	CN 1432855 A	30-07-2003
		CN 1721934 A	18-01-2006
		CN 1877429 A	13-12-2006
		JP 3881248 B2	14-02-2007
		JP 2003207797 A	25-07-2003
		TW 591282 B	11-06-2004
		US 2006274250 A1	07-12-2006
US 2003227590 A1	11-12-2003	JP 4085170 B2	14-05-2008
		JP 2004012731 A	15-01-2004
		TW 238277 B	21-08-2005

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

REFERENCES CITED IN THE DESCRIPTION

This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

Patent documents cited in the description

- KR P2007080354 **[0001]**
- KR P2007080355 **[0001]**

专利名称(译)	液晶显示装置		
公开(公告)号	EP2023195A1	公开(公告)日	2009-02-11
申请号	EP2008012877	申请日	2008-07-16
[标]申请(专利权)人(译)	乐金显示有限公司		
申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
当前申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
[标]发明人	LEE JAE KYUN OH KUM MI OH JAE YOUNG SHIN DONG SU		
发明人	LEE, JAE KYUN OH, KUM MI OH, JAE YOUNG SHIN, DONG SU		
IPC分类号	G02F1/1345 G02F1/1362		
CPC分类号	G02F1/1345 G02F1/13458 G02F1/136286 G02F2201/121		
优先权	1020070080354 2007-08-09 KR 1020070080355 2007-08-09 KR		
其他公开文献	EP2023195B1		
外部链接	Espacenet		

摘要(译)

公开了一种在显示面板（10）内具有均匀公共电压分布的液晶显示装置。液晶显示装置包括显示面板（10），显示面板（10）包括显示区域（12）和围绕显示区域（12）的非显示区域（14），多条栅极线（22）和数据线（24）布置在显示区域（10）上以彼此交叉，以便限定多个像素区域（20），形成在栅极线（22）和数据线（24）的各个交叉点处的薄膜晶体管（21）），像素电极形成在各个像素区域上并连接到薄膜晶体管，多个第一公共线（30）设置在相邻栅极线之间并且平行于栅极线（22）布置，以及多个第二公共端线（32）设置在相邻数据线之间并且平行于数据线（24）布置，第二公共线（32）电连接到第一公共线（30）。

FIG. 1