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(54) **Liquid crystal display device and method for manufacturing the same**

Flüssigkristallanzeigevorrichtung und Methode zu ihrer Herstellung

Dispositif d'affichage aux cristaux liquides et procédé de son fabrication

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Description

[0001] The present invention relates to a liquid crystal device of active matrix type and to a method for manufacturing the same. In particular, the invention relates to a thin-film transistor formed on one of substrates of a liquid crystal display panel, which makes up the liquid crystal display device. The invention also relates to a method for manufacturing the same.

[0002] A liquid crystal display panel to make up a liquid crystal display device of active matrix type has a liquid crystal interposed between a substrate (an active matrix substrate) and another substrate (a color filter substrate). In a manufacturing process to prepare a thin-film transistor (TFT) on the active matrix substrate, a plurality of gate lines disposed in parallel to each other and comprising metal film such as chromium are prepared on said substrate, and a gate electrode extending from each of said gate lines to each pixel is formed.

[0003] Fig. 17 represents diagrams to explain an equivalent circuit of a display panel of a liquid crystal display device of active matrix type. Fig. 17 (a) is a circuit diagram of the entire device, and Fig. 17 (b) is an enlarged view of the diagram of a pixel unit PXL in Fig. 17 (a). In Fig. 17 (a), a multiple of pixel units PXL are arranged in matrix-like form on a display panel PNL. Each pixel PXL is selected at a scan line driving circuit GDR and is turned on according to a display data signal from a data line (also called "source line") driving circuit DDR.

[0004] Specifically, in response to the gate line GL selected by the scan line driving circuit GDR, a display data (voltage) is sent to a thin-film transistor TFT on the pixel unit PXL of the display panel PNL via a data line DL from the data line driving circuit DDR.

[0005] As shown in Fig. 17 (b), the thin-film transistor TFT to constitute the pixel unit PXL is provided at an intersection of the gate line GL and the data line DL. The gate line GL is connected to a gate electrode GT of the thin-film transistor TFT, and the data line DL is connected to a drain electrode or a source electrode ("drain electrode" at this moment) SD2 of the thin-film transistor TFT.

[0006] The drain electrode or the source electrode ("source electrode" at this moment) SD1 of the thin-film transistor TFT is connected to a pixel electrode PX of a liquid crystal (element) LC. The liquid crystal LC is positioned between a pixel electrode PX and a common electrode CT and is driven by a data (voltage) to be supplied to the pixel electrode PX. An auxiliary capacity Ca to temporarily maintain the data is connected between the drain electrode SD2 and an auxiliary capacity line CL.

[0007] Fig. 18 represents a plan view to show a pixel unit PXL of a display panel PNL shown in Fig. 17 and a cross-sectional view to explain an arrangement of a thin-film transistor TFT to make up the pixel unit PXL. Specifically, Fig. 18 (a) is a plan view of a pixel unit PXL arranged in matrix-like form as shown in Fig. 17, and Fig. 18(b) is a cross-sectional view of the thin-film transistor TFT in the pixel unit PXL along the line A-A'.

[0008] As shown in Fig. 18 (a), in the pixel unit PXL arranged in matrix-like form, the thin-film transistor TFT is disposed at an intersection of the gate line GL and the data line DL. Also, a pixel electrode PX is connected to the thin-film transistor TFT, and an auxiliary capacity is formed with the auxiliary capacity line CL.

[0009] In Fig. 18 (b), in the thin-film transistor TFT, a gate electrode GT and a gate insulator GI to cover the gate electrode GT are prepared on an insulating substrate SUB1. On the insulator, a silicon (Si) semiconductor layer SI, an ohmic contact layer (n^+ Si) NS, a source electrode SD1 and a drain electrode SD2 are sequentially laminated on the insulator.

[0010] To prepare a gate insulator GI, silicon nitride (SiN_x) is deposited to cover the gate line GL and the gate electrode GT, and a plurality of data lines DL are prepared to intersect the gate lines GL. At the same time as the preparation of the data lines DL, the source electrode SD1 and the drain electrode SD2 are formed on the same layer.

[0011] As described above, in a region enclosed by each gate line GL and each data line DL, a unit pixel comprising a pixel unit PXL is provided. This unit pixel has a subpixel of a single color (red, green, or blue) in case of full-color display. Hereinafter, the unit pixel is also simply referred as "pixel". The thin-film transistor (TFT) to make up the pixel unit PXL comprises, as described above, a gate electrode, a silicon semiconductor film prepared by patterning on the gate electrode, an ohmic contact layer (n^+ silicon) separately formed on upper layer of the silicon semiconductor film, and a source electrode and a drain electrode connected respectively to the separated ohmic contact layer.

[0012] On the upper layer of the thin-film transistor, a protective layer PAS is deposited. On it, a pixel electrode PX - preferably made of ITO, is prepared by patterning, and it is connected to the source electrode (or to the drain electrode) SD1 via a contact hole provided in the protective film PAS. An orientation film (not shown) is deposited to cover the pixel electrode PX.

[0013] On the other hand, on another substrate (not shown in the figure), a counter electrode (in Fig. 17 (b)) is prepared via a smooth layer (overcoat layer) and a 3-color filter (in case of full-color display). An orientation film is deposited to cover the counter electrode. An active matrix substrate (i.e. one of the substrates as described above) is superimposed on it, and a liquid crystal is sealed in a gap therebetween.

[0014] The Patented Reference 1 as given below discloses a method for manufacturing lines of the active matrix substrate as described above by means of ink jet coating method. In the Patented Reference 1, the gate electrode of the thin-film transistor TFT is prepared by ink jet coating method using a liquid containing a conductive material. Also,

it is described that a source electrode and a drain electrode of the thin-film transistor are prepared by ink jet coating method using a liquid containing a semiconductor material.

[0015] [Patented Reference 1] JP-2003-318193

5 The gate insulator to be formed on the active matrix substrate of the liquid crystal display panel is provided to insulate the gate line and data line. The thinner the gate insulator is, the more the performance of the thin-film transistor are improved. Also, the thinner the gate insulator is, the finer the auxiliary capacity line can be produced, and this contributes to the improvement of aperture rate. However, when the gate insulator is thinner, cross capacity at the intersection with the data line is increased, and this results in the delay of signal. Also, the counter capacity between the gate line and the counter electrode is also increased. If the gate insulator is designed thicker to reduce the cross capacity and counter capacity, performance of the thin-film transistor are decreased as described above.

10 [0016] It is an object of the present invention to provide a liquid crystal display device, which can be operated at high speed and with high precision by improving performance characteristics of the thin-film transistor without increasing cross capacity and counter capacity. US-A-2005/0095356 describes a liquid crystal display device having a plurality of gate and data lines, which lines intersect via an intermediate insulating layer. That layer covers the gate line and a gate electrode of a thin film transistor extending from the gate line to a region enclosed by the gate and data lines.

15 EP-A-0 750 350 describes a solid state array device having a plurality of pixels with respective thin film transistor switches and a manufacturing method therefor. A plurality of first address lines are arranged perpendicular to a plurality of second address lines. A TFT gate dielectric layer is disposed over the first address lines, and a crossover region supplemental dielectric layer is disposed in respective ones of the crossover regions between the first and second address lines.

20 US-A-5,365,079 describes a liquid crystal display panel and a manufacturing method therefor, the liquid crystal display panel including an additional insulating layer formed between crossing orthogonal source lines and gate lines to provide a higher breakdown voltage between the source lines and gate lines than at the gate insulating layer of the thin film transistors.

25 JP-A-09-045774 describes a film semiconductor device wherein a film transistor and wiring part are stacked on an insulating substrate. The wiring part has a lower wiring and an upper wiring patterned on the insulating substrate, and a composite insulating pad interposed at least in the crossing of both wirings. The composite insulating pad contains a lower insulating film, a middle semiconductor film, and an upper insulating film.

30 [0017] To attain the above object, according to the present invention, another insulator may be provided by applying a further insulator layer with low dielectric constant on an upper or lower surface of the gate insulator layer, locally formed at the intersections of said gate line and said data lines, the peripheral edges of said further insulator layer on each side of each gate line having a tapered form with a gentle slope in cross sectional view, and performance characteristics of the thin-film transistor is improved without increasing cross capacity at the intersection and a capacity from the counter electrode (counter capacity)

35 [0018] Also, according to the present invention, a further insulating material with low dielectric constant may be dropped by ink jet coating-method along the gate line including an intersection with the data line to an upper layer or to a lower layer of a gate insulator to cover the gate line, peripheral edges of said further insulating material with low dielectric constant on each side of each gate line being turned into tapered form with a gentle slope in cross sectional view. Thus, the performance characteristics of the thin-film transistor are improved without increasing cross capacity at the intersection and a capacity (counter capacity) with the counter electrode.

40 [0019] After the formation of the data lines, the source electrode, and the drain electrode, a silicon semiconductor layer is deposited and a semiconductor island is prepared by patterning. Then, the thin-film transistor is provided by preparing an ohmic conduct layer, the source electrode, and the drain electrode. After the formation of a protective film, a pixel electrode connected to the source electrode (or drain electrode) of the thin-film transistor is prepared via a contact hole opened in the protective film. Then, the liquid crystal display panel is prepared by a process already known, and the liquid crystal display device can be provided.

45 [0020] According to the present invention, it is possible to provide coating of an insulating material with low dielectric constant to the extent as necessary only on the intersection of the gate line and the data line or on the gate line including the intersection and to an upper layer or to a lower layer of the gate insulator. Thus, without increasing cross capacity of the intersection and the capacity (counter capacity) with the counter electrode and without the need to remove unnecessary portion and to perform subsequent process, performance characteristics of the thin-film transistor can be improved. When the insulating material is dropped by ink jet coating, peripheral edges of the insulator are prepared in a tapered form with a gentle slope in cross sectional view. Thus, disconnection can be avoided, which may be caused by skipping over as data line goes over the gate line when crossing.

55 IN THE DRAWING

[0021]

Fig. 1 represents plan views to explain essential processes of a method for manufacturing an active matrix substrate of a liquid crystal display panel, which constitutes Embodiment 1 of a liquid crystal display device according to the present invention;

5 Fig. 2 is a cross-sectional view along the line A-A of the active matrix substrate when data lines are prepared in a process (4) as shown in Fig. 1;

Fig. 3 represents plan views to explain essential processes of a method for manufacturing the active matrix substrate of the liquid crystal display panel, which constitutes Embodiment 2 of the liquid crystal display device of the present invention;

10 Fig. 4 is a cross-sectional view along the line A-A of the active matrix substrate when data lines are prepared in a process (4) as shown in Fig. 3;

Fig. 5 represents plan views to explain essential processes of a method for manufacturing the active matrix substrate of the liquid crystal display panel, which constitutes Embodiment 3 of the liquid crystal display device of the present invention;

15 Fig. 6 is a cross-sectional view along the line A-A of the active matrix substrate when data lines are prepared in a process (4) as shown in Fig. 5;

Fig. 7 represents plan views to explain essential processes of a method for manufacturing the active matrix substrate of the liquid crystal display panel, which constitutes Embodiment 4 of the liquid crystal display device of the present invention;

20 Fig. 8 is a cross-sectional view along the line A-A of the active matrix substrate when data lines are prepared in a process (4) as shown in Fig. 7;

Fig. 9 represents plan views to explain essential processes of a method for manufacturing the active matrix substrate of the liquid crystal display panel, which constitutes Embodiment 5 of the liquid crystal display device of the present invention;

25 Fig. 10 is a cross-sectional view of the active matrix substrate along the line B-B when data lines are prepared in the process (4) of Fig. 9 and another substrate is attached to seal the liquid crystal;

Fig. 11 represents plan views to explain essential processes of a method for manufacturing the active matrix substrate of the liquid crystal display panel, which constitutes Embodiment 6 of the liquid crystal display device of the present invention;

30 Fig. 12 is a cross-sectional view of the active matrix substrate along the line B-B when data lines are prepared in the process (4) of Fig. 11 and another substrate is attached to seal the liquid crystal;

Fig. 13 represents plan views to explain essential processes of a method for manufacturing the active matrix substrate of the liquid crystal display panel, which constitutes Embodiment 7 of the liquid crystal display device of the present invention;

35 Fig. 14 is a cross-sectional view of the active matrix substrate along the line B-B when data lines are prepared in the process (4) of Fig. 13 and another substrate is attached to seal the liquid crystal;

Fig. 15 represents plan views to explain essential processes of a method for manufacturing the active matrix substrate of the liquid crystal display panel, which constitutes Embodiment 8 of the liquid crystal display device of the present invention;

40 Fig. 16 is a cross-sectional view of the active matrix substrate along the line B-B when data lines are prepared in the process (4) of Fig. 15 and another substrate is attached to seal the liquid crystal;

Fig. 17 represents an equivalent circuit of a display panel unit of a liquid crystal display device of active matrix type; and Fig. 18 represents drawings to explain an arrangement of a pixel unit PXL of a display panel PNL shown in Fig. 17 and an arrangement of a thin-film transistor TFT to constitute a pixel unit PXL.

45 **[0022]** Detailed description will be given below on embodiments of the present invention referring to the drawings. The structure of the liquid crystal display device of the present invention will be described in connection with the manufacturing method as given below.

[Embodiment 1]

50 **[0023]** Fig. 1 represents plan views to explain essential processes of a method for manufacturing an active matrix substrate of a liquid crystal display panel, which constitutes Embodiment 1 of the liquid crystal display device according to the present invention. Here, description will be given on processes to form data lines and source electrodes and drain electrodes in the processes (1) to (4). First, (1) Preparation of gate electrode: a gate line GL is prepared by patterning on surface of an insulating substrate - preferably a transparent glass substrate. On the gate line GL, a gate electrode GT of a thin-film transistor is provided to protrude on it.

(2) Preparation of island: A gate insulator GI is deposited to cover the entire area of the substrate including the gate

line GL and the gate electrode GT. To form the gate insulator GI, silicon nitride (SiNx) is deposited by CVD (chemical vapor deposition). Then, an amorphous silicon semiconductor layer and an n⁺ silicon semiconductor layer (ohmic contact layer) with silicon mixed with phosphor or the like as impurities are prepared by CVD. By processing the ohmic contact layer, which has been turned to the amorphous silicon semiconductor layer, a silicon semiconductor island SI is formed on upper portion of the gate electrode GT. In this case, the ohmic contact layer to be formed on the upper layer of the island SI is separately prepared as connecting regions of a source electrode and a drain electrode respectively.

(3) Ink jet coating of the crossing portion: Only on a crossing portion where data line crosses the gate insulator GI of the gate line, an insulating material with low dielectric constant is dropped and coated by ink jet coating, and another insulator layer LDP is formed. This another insulator LDP will be referred below as the insulator LDP with low dielectric constant.

(4) Formation of source and channel: On the gate insulator GI, and on the insulator LDP with low dielectric constant on the gate line GL, a source line, i.e. a data line DL, is formed. In this case, the source electrode SD1 and the drain electrode of the thin-film transistor are processed by patterning at the same time, and a channel is provided between the source electrode SD1 and the drain electrode. Then, the active matrix substrate is prepared through a pixel forming process such as formation of a protective film and formation of a pixel electrode and through coating process to form an orientation film.

[0024] Fig. 2 is a cross-sectional view of the active matrix substrate along the line A-A when the data line is prepared in the process (4) shown in Fig. 1. As shown in the figure, a gate line GL is formed on surface of a glass substrate SUB1. The gate insulator GI is formed over the entire surface of the glass substrate SUB1 to cover the gate line GL. On the gate line GL on a portion where the gate line GL and the data line cross each other and on the gate insulator GI, an ink of an insulating material with low dielectric constant such as an aromatic hydrocarbon type organic polymer and polyallyl ether type organic polymer is dropped by ink jet coating method. When this ink is dried up, it is turned to the insulator LDP with low dielectric constant.

[0025] On the 2-layer insulating structure of the gate insulator GI and the insulator LDP with low dielectric constant, the data lines DL are provided to cross. As shown in Fig. 2, peripheral edge of the insulator LDP with low dielectric constant dropped by ink jet coating method and hardened is turned to a tapered form with gentle slope in cross sectional view. As a result, the data line DL crossing the gate line GL runs over the gate line GL with gentle slope in cross sectional view and this prevents breaking of lines caused by skip-over. Between the data line DL and a counter electrode on a color filter substrate (not shown), there is no dielectric substance, which narrows down the distance between electrodes except the above-mentioned crossing portion.

[0026] According to Embodiment 1, it is possible to improve performance characteristics of the thin-film transistor without increasing cross capacity and counter capacity and to provide a liquid crystal display device to be operated at high speed and with high precision.

[Embodiment 2]

[0027] Fig. 3 represents plan views to explain essential processes of a method for manufacturing an active matrix substrate of a liquid crystal display panel, which makes up Embodiment 2 of the liquid crystal display device according to the present invention. Here again, the processes to prepare the data line, the source electrode and drain electrode are described in the order of (1) to (4). Similarly to Embodiment 1, first, (1) Preparation of gate electrode: A gate line GL is prepared by patterning on the surface of an insulating substrate - preferably a transparent glass substrate. On the gate line GL, a gate electrode GT of the thin-film transistor is prepared to protrude.

(2) Ink jet coating of the crossing portion: On the gate line GL and only on the crossing portion where data line intersects, an insulating material with low dielectric constant is coated by ink jet coating, and an insulator LDP with low dielectric constant is prepared.

(3) Preparation of island: A gate insulator GI is deposited over the entire Substrate including the gate line GL, the gate electrode GT, and the insulator LDP with low dielectric constant. The gate insulator GI is formed by silicon nitride (SiNx) by CVD. Similarly by CVD processing, an amorphous silicon semiconductor layer and an n⁺ silicon semiconductor layer (ohmic contact layer) with silicon intermingled with phosphor or the like as impurities are deposited. By processing the ohmic contact layer, which has been turned to the amorphous silicon semiconductor layer, a silicon semiconductor island SI is prepared on upper portion of the gate electrode GT. In this case, the ohmic contact layer to be formed on the upper layer of the island SI is separately prepared as connecting regions of a source electrode and a drain electrode.

(4) Formation of source and channel: On the insulator LDP with low dielectric constant and on the gate insulator GI, and on the gate insulator GI on the intersecting gate line GL, a source line, i.e. a data line DL, is prepared. In

this case, patterning is performed at the same time for the source electrode SD1 and the drain electrode of thin film transistor, and a channel is formed between the source electrode SD1 and the drain electrode. Then, through pixel forming process to form a protective film and a pixel electrode and through coating process to coat an orientation film, an active matrix substrate is prepared.

[0028] Fig. 4 is a cross-sectional view of the active matrix substrate along the line A-A with the data line prepared in the process (4) of Fig. 3. As shown in the figure, the gate line GL is formed on the surface of a glass substrate SUB1. On the gate line GL and on a portion of the gate line GL where the data line intersects, an ink of an insulating material with low dielectric constant such as aromatic hydrocarbon type organic polymer or polyallyl ether type organic polymer is dropped and coated by ink jet coating. When the ink is dried up, it is turned to an insulator LDP with low dielectric constant. Then, a gate insulator GI is formed over the entire surface of the glass substrate SUB1 to cover the gate line GL, which has the insulator LDP with low dielectric constant at the intersection.

[0029] Then, a data line DL is disposed on a 2-layer insulating structure, which comprises the insulator LDP with low dielectric constant and the gate insulator GI. As shown in Fig. 4, peripheral edge of the insulator LDP with low dielectric constant prepared by ink jet coating and hardened is turned to a tapered form with gentle slope. It forms an edge more gently tapered than the gate insulator GI on it. As a result, the data line DL intersecting with the gate line GL goes over the gate line GL at a gentle angle in cross sectional view. Thus, disconnection can be avoided, which may be caused by skip-over when jumping at a steep angle. Between the data line DL and a counter electrode of a color filter substrate (not shown), there is no dielectric substance, which narrows down the distance between electrodes.

[0030] According to Embodiment 2, it is possible to improve performance characteristics of the thin-film transistor without increasing cross capacity and counter capacity and to provide a liquid crystal display device to be operated at high speed and with high precision.

[Embodiment 3]

[0031] Fig. 5 represents plan views to explain essential processes of a method for manufacturing an active matrix substrate of a liquid crystal display panel, which makes up Embodiment 3 of the liquid crystal display device according to the present invention. In Embodiment 3, the gate line and the data line are also prepared by ink jet coating. Description will be given now on the processes to prepare the data line, the source electrode and drain electrode in the order of (1) to (4). First, (1) Preparation of the gate electrode: A gate line and a bank BNK-G to form a groove on the pattern of the gate electrode are provided on the surface of an insulating substrate - preferably a transparent glass substrate. The bank BNK-G and its groove are prepared from a photosensitive resist by photolithographic method. This is the same in the other embodiments. An ink containing conductive particles such as silver or copper is dropped into the groove of the bank BNK-G by ink jet coating and the groove is filled. When the ink is dried up, the gate line GL and the gate electrode GT are prepared by baking.

(2) Preparation of island: A gate insulator GI of SiNx by CVD is deposited over the entire substrate including the gate line GL, the gate electrode GT and the bank BNK-G. Then, by similar CVD processing, an amorphous silicon semiconductor layer and an n⁺ silicon semiconductor layer (ohmic contact layer) with silicon intermingled with phosphor or the like as impurities are deposited. By processing the ohmic contact layer, which has been turned to the amorphous silicon semiconductor layer, a silicon semiconductor island SI is prepared on upper portion of the gate electrode GT. In this case, the ohmic contact layer prepared on the upper layer of the island SI is separately provided as connecting regions of a source electrode and drain electrode respectively.

(3) Ink jet coating of the crossing portion: On the gate insulator GI of the gate line and only on the crossing portion where the data line crosses, an insulating material with low dielectric constant is dropped and coated by ink jet coating, and an insulating layer LDP with low dielectric constant is prepared.

(4) Formation of source and channel: On the surface of the insulating substrate, a data line, a bank BNK-D to form groove on pattern of the source electrode and the drain electrode is provided. The bank BNK-D and its groove are prepared from a photosensitive resist by photolithographic method. This is the same in the other embodiments. An ink containing conductive particles such as silver and copper is dropped into the groove of the bank BNK-D and the groove is filled. When this is dried up, a data line DL, a source electrode SD1 and a drain electrode SD2 are prepared by baking. In this case, a channel is formed between the source electrode SD1 and the drain electrode SD2. Then, an active matrix substrate is prepared through pixel forming process such as the formation of a protective film and a pixel electrode and through coating process to coat an orientation film.

[0032] Fig. 6 is a cross-sectional view of an active matrix substrate along the line A-A with the data line prepared in the process (4) of Fig. 5. As shown in the figure, the gate line GL is prepared in the groove of the bank BNK-G formed on the surface of a glass substrate SUB1. A gate insulator GI is prepared over the entire surface of the glass substrate

SUB1 to cover the gate line GL. On the gate insulator GI, an ink of an insulating material with low dielectric constant such as aromatic hydrocarbon type organic polymer or polyallyl ether type organic polymer is dropped by ink jet coating on the gate line GL and on the gate line GL on a portion where the data line intersects. When this ink is dried up, it is turned to an insulator LDP with low dielectric constant.

[0033] On the 2-layer insulating structure of the gate insulator GI and the insulator LDP with low dielectric constant, the data line DL is prepared to cross it. As shown in Fig. 6, the gate insulator GI is formed flatly on the bank BNK-G. Peripheral edge of the insulator LD with low dielectric constant prepared by ink jet coating and hardened is formed in a tapered form with gentle slope in cross sectional view. As a result, the data line DL to cross the gate line GL goes over the gate line GL with gentle slope in cross sectional view, and disconnection caused by skip-over when jumping at steep angle can be avoided. Between the data line DL and a counter electrode on a color filter substrate (not shown), there is no dielectric substance, which narrows down the distance between electrodes except the intersection as described above.

[0034] According to Embodiment 3, it is possible to improve performance characteristics of the thin-film transistor without increasing cross capacity and counter capacity and to provide a liquid crystal display device to be operated at high speed and with high precision.

[Embodiment 4]

[0035] Fig. 7 represents plan views to explain essential processes of a method for manufacturing an active matrix substrate of a liquid crystal display panel, which makes up Embodiment 4 of the liquid crystal display device of the present invention. Similarly to Embodiment 3, the gate line and data line are prepared in Embodiment 4 by ink jet coating method. Here again, description will be given on the process to prepare the data line, the source electrode and the drain electrode in the order of (1) to (4). First, (1) Preparation of gate electrode: On the surface of an insulating substrate - preferably a transparent glass substrate, a gate line and a bank BNK-G to form a groove on the pattern of the gate line and gate electrode are provided. An ink containing conductive particles such as silver or copper is dropped into the groove of the bank BNK-G to fill it. Then, this is dried up, and a gate line GL and a gate electrode GT are prepared by baking.

(2) Ink jet coating of the crossing portion: On the gate insulator GI of the gate line and only on the crossing portion where the data line crosses, an insulating material with low dielectric constant is dropped by ink jet process, and an insulator LDP with low dielectric constant is prepared.

(3) Preparation of island: A gate insulator GI is deposited over the entire surface of the substrate including the gate line GL, the gate electrode GT, and the bank BNK-G. To prepare the gate insulator GI, silicon nitride (SiN_x) is deposited by CVD. Then, by similar CVD processing, an amorphous silicon semiconductor layer and an n⁺ silicon semiconductor layer (ohmic contact layer) with silicon intermingled with phosphor or the like as impurities are deposited. By processing the ohmic contact layer, which has been turned to the amorphous silicon semiconductor layer, a silicon semiconductor island SI is prepared on upper portion of the gate electrode GT. In this case, the ohmic contact layer formed on the upper layer of the island SI is separately provided as connecting regions of a source electrode and a drain electrode respectively.

(4) Formation of source and channel: On the surface of the insulating substrate, a data line and a bank BNK-D with groove formed on the pattern of the source electrode and the drain electrode are disposed. An ink with conductive particles such as silver or copper is dropped into the groove of the bank BNK-D to fill it. Then, this is dried up, and the data line DL, a source electrode SD1, and a drain electrode SD2 are prepared. In addition, a channel is formed between the source electrode SD1 and the drain electrode SD2. Then, the active matrix substrate is prepared through pixel forming process to form a protective film and a pixel electrode and through coating process to coat an orientation film.

[0036] Fig. 8 is a cross-sectional view of an active matrix substrate along the line A-A with the data line prepared in the process (4) of Fig. 7. As shown in the figure, a gate line GL is prepared in the groove of the bank BNK-G formed on the surface of the glass substrate SUB1. On the gate line GL on a portion where the gate line GL crosses the data line and on the gate insulator GI, an ink of an insulating material with low dielectric constant such as aromatic hydrocarbon type organic polymer, polyallyl ether type organic polymer, etc. is dropped by ink jet coating. When this ink is dried up, it is turned to an insulator LDP with low dielectric constant. The gate insulator GI is prepared over the entire surface of the glass substrate SUB1 to cover the insulator LDP with low dielectric constant.

[0037] On the 2-layer insulating structure of the insulator LDP with low dielectric constant and the gate insulator GI, the data lines DL are formed to cross. As shown in Fig. 8, in the gate insulator GI formed on the insulator LDP with low dielectric constant, peripheral edge is prepared having a tapered form with a gentle slope in cross sectional view because of the bank BNK-G. As a result, disconnection can be avoided, which may be caused by skip-over when the data line DL crossing the gate line GL goes with gentle slope in cross sectional view over the gate line GL. Also between the data

line DL and a counter electrode of a color filter substrate (not shown), there is no dielectric substance, which narrows down distance between electrodes except at the intersection.

[0038] According to Embodiment 4, it is possible to improve performance characteristics of the thin-film transistor without increasing cross capacity and counter capacity and to provide a liquid crystal display device to be operated at high speed and with high precision.

[Embodiment 5]

[0039] Fig. 9 represents plan views to explain essential processes of a method for manufacturing an active matrix substrate of a liquid crystal display panel, which makes up Embodiment 5 of the liquid crystal display device of the present invention. Here again, description will be given on the processes to prepare the data line, the source electrode, and the drain electrode in the order of (1) to (4). First, (1) Preparation of gate electrode: A gate line GL is prepared by patterning on the surface of an insulating substrate - preferably a transparent glass substrate. On the gate line GL, a gate electrode GT of the thin-film transistor is prepared to protrude.

(2) Preparation of an island: A gate insulator GI is deposited to cover the entire surface of the substrate including the gate line GL and the gate electrode GT. The insulator GI is prepared by depositing silicon nitride (SiN_x) by CVD. Then, an amorphous silicon semiconductor layer and an n⁺ silicon semiconductor layer (ohmic contact layer) with silicon intermingled with phosphor or the like as impurities are deposited by similar CVD processing. By processing the ohmic contact layer, which has been turned to the amorphous silicon semiconductor layer, a silicon semiconductor island SI is prepared on upper portion of the gate electrode GT. In this case, the ohmic contact layer formed on the upper layer of the island SI is separately provided as connecting regions of the source electrode and the drain electrode respectively.

(3) Ink jet coating of gate line: On the gate insulator GI of the gate line and not only on the crossing portion where data line crosses but also along the gate line GL, an ink of an insulating material with low dielectric constant is dropped by ink jet process, and an insulator LDP with low dielectric constant is formed. The insulator LDP with low dielectric constant is prepared on upper layers of all of the gate lines GL at least within a display region (a region where a multiple of pixels are arranged in matrix-like form) of the active matrix substrate.

(4) Formation of source and channel: On the gate insulator GI and on the insulator LDP with low dielectric constant on the crossing gate line GL, a source line, i.e. a data line DL, is prepared. In this case, the source electrode SD1 of the thin-film transistor and the drain electrode are prepared at the same time by patterning, and a channel is formed between the source electrode SD1 and the drain electrode. Then, an active matrix substrate is prepared through pixel forming process to form a protective film and a pixel electrode, and through coating process to coat an orientation film.

[0040] Fig. 10 is a cross-sectional view of an active matrix substrate along the line B-B with the data line prepared in the process (4) of Fig. 9, and a liquid crystal is sealed by attaching another substrate on it. As shown in the figure, a gate line GL is prepared on the surface of the glass substrate SUB1, which makes up the active matrix substrate. The gate insulator GI is formed on the entire surface of the glass substrate SUB1 to cover the gate line GL. On the gate line GL and on the gate line GL of a portion where data line crosses and on the gate insulator GI, an ink of an insulating material with low dielectric constant such as aromatic hydrocarbon type organic polymer, polyallyl ether type organic polymer, etc. is dropped by ink jet coating. When this ink is dried up, it is turned to an insulator LDP with low dielectric constant on the insulator GI along the gate line GL.

[0041] On the 2-layer insulating structure of the gate insulator GI and the insulator LDP with low dielectric constant, the data line DL is prepared to cross. As shown in Fig. 10, peripheral edge of the insulator LDF with low dielectric constant is formed in a tapered form with gentle slope in cross sectional view. As a result, disconnection can be avoided, which may be caused by skip-over when the data line DL crossing the gate line GL goes over the gate line GL at a steep angle. Also, between the data line DL and a counter electrode CT of the color filter substrate SUB2, there is no dielectric substance, which narrows down the distance between electrodes except the portion of the gate line GL including the intersection as described above. A liquid crystal LC is sealed between an orientation film ORI1 on the active matrix substrate SUB1 and an orientation film ORI2 on the color filter substrate SUB2.

[0042] According to Embodiment 5, cross capacity and counter capacity are not increased. Between the signal lines such as data line and the counter electrode, there is only an insulator LDP with low dielectric constant on the gate line GL as a dielectric substance to narrow down the distance between electrodes, and it is not a structure to extensively increase the capacity. For this reason, it is possible to provide a liquid crystal display device to be operated at high speed and with high precision without decreasing the performance characteristics of the thin-film transistor.

[Embodiment 6]

[0043] Fig. 11 represents plan views to explain essential processes of a method for manufacturing an active matrix substrate of a liquid crystal display panel, which makes up Embodiment 6 of the liquid crystal display device of the present invention. Here again, description will be given on the processes to prepare the data line, the source electrode, and the drain electrode in the order of (1) to (4). First, (1) Preparation of gate electrode: A gate line GL is prepared by patterning on the surface of an insulating substrate - preferably a transparent glass substrate. On the gate line GL, a gate electrode GT of the thin-film transistor is formed to protrude.

(2) Ink jet coating of the gate line: On the gate line, not only on the crossing portion where data line crosses but also along the gate line GL, an insulating material with low dielectric constant is dropped and coated, and an insulator LDP with low dielectric constant is prepared. The insulator LDP with low dielectric constant is prepared on upper layers of all gate lines GL at least within a display region (a region where a multiple of pixels are arranged in matrix-like form) of the active matrix substrate.

(3) Preparation of island: A gate insulator GI is deposited on the gate line GL, the gate electrode GT, and over the entire surface of the substrate including the insulator LDP with low dielectric constant. To prepare the gate insulator GI, silicon nitride (SiN_x) is deposited by CVD. Then, by similar CVD processing, an amorphous silicon semiconductor layer and an n⁺ silicon semiconductor layer (ohmic contact layer) with silicon intermingled with phosphor or the like as impurities are deposited. By processing the ohmic contact layer, which has been turned to the amorphous silicon semiconductor layer, a silicon semiconductor island SI is prepared on upper portion of the gate electrode GT. In this case, the ohmic contact layer prepared on the upper layer of the island SI is separately provided as connecting regions of the source electrode and the drain electrode respectively.

(4) Formation of source and channel: On the gate insulator GI and on the insulator LDP with low dielectric constant on the intersecting gate line GL, a source line, i.e. a data line DL, is prepared. In this case, patterning is performed at the same time on the source electrode SD1 and the drain electrode of the thin-film transistor, and a channel is formed between the source electrode SD1 and the drain electrode. Then, an active matrix substrate is prepared through pixel forming process to form a protective film and a pixel electrode and through coating process to coat an orientation film.

[0044] Fig. 12 is a cross-sectional view of an active matrix substrate along the line B-B with the data line prepared in the process (4) of Fig. 11, and a liquid crystal is sealed by attaching another substrate. As shown in the figure, the gate line GL is prepared on the surface of the glass substrate SUB1, which makes up the active matrix substrate. An insulator LDP with low dielectric constant is prepared on the gate line GL including a portion where data line crosses and a gate insulator GI is prepared on it. To prepare the insulator LDP with low dielectric constant, an ink of an insulating material with low dielectric constant such as aromatic hydrocarbon type organic polymer, polyallyl ether type organic polymer, etc. is dropped by ink jet coating method. When it is dried up, it is turned to an insulator LDP with low dielectric constant on the gate insulator GI along the gate line GL.

[0045] On the 2-layer insulating structure of the insulator LDP with low dielectric constant and the gate insulator GI, the data line DL is prepared to cross. As shown in Fig. 12, when ink is dropped by ink jet coating method and is hardened, peripheral edge of the insulator LDP with low dielectric constant is prepared in a tapered form with gentle in cross sectional view. As a result, the data line DL crossing the gate line GL goes over the gate line GL at gentle slope in cross sectional view, and disconnection can be avoided, which may be caused by skip-over when jumping at a steep angle. Also, between the data line DL and the counter electrode CT of the color filter substrate SUB2, there is no dielectric substance, which narrows down the distance between electrodes except a portion of the gate line GL including the intersection as described above. A liquid crystal LC is sealed between an orientation film ORI1 on the active matrix substrate SUB1 and an orientation film ORI2 on the color filter substrate SUB2.

[0046] According to Embodiment 6, cross capacity and counter capacity are not increased. Between the signal lines such as data line and the counter electrode, there is only an insulator LDP with low dielectric constant on the gate line as a dielectric substance to narrow down the distance between electrodes, and it is not a structure to extensively increase the capacity. For this reason, it is possible to provide a liquid crystal display device to be operated at high speed and with high precision without decreasing the performance characteristics of the thin-film transistor.

[Embodiment 7]

[0047] Fig. 13 represents plan views to explain essential processes of a method for manufacturing an active matrix substrate of a liquid crystal display panel, which makes up Embodiment 7 of the liquid crystal display device of the present invention. Here again, description will be given on the processes to prepare the data line, the source electrode and the drain electrode in the order of (1) to (4). First, (1) Preparation of gate electrode: A gate line and a bank BNK-G

with groove pattern of the gate electrode are prepared on the surface of the insulating substrate - preferably a transparent glass substrate. An ink containing conductive particles such as silver or copper is dropped into the grooves of the bank BNK-G by ink jet coating method. It is then dried up, and a gate line GL and a gate electrode GT are prepared by baking.

(2) Preparation of island: A gate insulator GI is deposited over the entire surface of the substrate including the gate line GL, the gate electrode GT and the bank BNK-G. To prepare the gate insulator GI, silicon nitride (SiN_x) is deposited by CVD. Then, by similar CVD processing, an amorphous silicon semiconductor layer and an n⁺ silicon semiconductor layer (ohmic contact layer) with silicon intermingled with phosphor or the like as impurities are deposited. By processing the ohmic contact layer, which has been turned to the amorphous silicon semiconductor layer, a semiconductor island SI is prepared on upper portion of the gate electrode GT. In this case, the ohmic contact layer prepared on the upper layer of the island SI is provided separately as connecting regions of the source electrode and the drain electrode respectively.

(3) Ink jet coating of the gate line: On the gate insulator GI of the gate line, and not only on the crossing portion where data line crosses but also along the gate line GL, an ink of an insulating material with low dielectric constant is dropped by ink jet coating method, and an insulator LDP with low dielectric constant is prepared. The insulator LDP with low dielectric constant is formed on upper layers of all gate lines GL at least within a display region (a region where a multiple of pixels are arranged in matrix-like form) of the active matrix substrate.

(4) Formation of source and channel: On the gate insulator GI, and on the insulator LDP with low dielectric constant on the crossing gate line GL, the data line, and the bank BNK-D with groove pattern of the source electrode SD1 and the drain electrode SD2 are prepared. An ink containing conductive particles such as silver or copper is dropped into the groove of the bank BNK-G. Then, it is dried up, and the source line, i.e. the data line DL, and the source electrode SD1 and the drain electrode SD2 are prepared by baking. In this case, a channel is formed between the source electrode SD1 and the drain electrode. Then, an active matrix substrate is prepared through pixel forming process to form a protective film, a pixel electrode, etc. and through coating process to coat the orientation film.

[0048] Fig. 14 is a cross-sectional view of an active-matrix substrate along the line B-B with data line prepared in the process (4) of Fig. 13, and the liquid crystal is sealed by attaching another substrate. As shown in the figure, a gate line GL is prepared on the entire surface of the glass substrate SUB1, which constitutes the active matrix substrate. A gate insulator GI is prepared over the entire surface of the glass substrate SUB1 to cover the gate line GL. The gate insulator GI is prepared in flat form because of the presence of the bank BNK-G. On the gate line where the gate line GL and the data line intersect, and on the gate insulator GI, an ink of an insulating material with low dielectric constant such as aromatic hydrocarbon type organic polymer, polyallyl ether type organic polymer, etc. is dropped by ink jet coating. When the ink is dried up, it is turned to an insulator LDP with low dielectric constant on the gate insulator GI along the gate line GL.

[0049] On the 2-layer insulating structure comprising the gate insulator GI and the insulator LDP with low dielectric constant, a data line DL is prepared to cross. As shown in Fig. 14, when ink is dropped by ink jet coating method and is hardened, peripheral edge of the insulator LD with low dielectric constant is formed in a tapered form with gentle slope in cross sectional view. As a result, the data line DL crossing the gate line GL goes over the gate line GL with gentle slope in cross sectional view, and disconnection can be avoided, which may be caused by skip-over when jumping at a steep angle. Also, between the data line DL and the counter electrode CT of the color filter substrate SUB2, there is no dielectric substance, which narrows down the distance between electrodes except a portion of the gate line GL including the intersection as described above. A liquid crystal LC is sealed between an orientation film ORI1 on the active matrix substrate SUB1 and an orientation film ORI2 on the color filter substrate SUB2.

[0050] According to Embodiment 7, cross capacity and counter capacity are not increased. Between the signal lines such as data line and the counter electrode, there is only an insulator LDP with low dielectric constant on the gate line as a dielectric substance to narrow down the distance between electrodes, and it is not a structure to extensively increase the capacity. For this reason, it is possible to provide a liquid crystal display device to be operated at high speed and with high precision without decreasing the performance characteristics of the thin-film transistor.

[Embodiment 8]

[0051] Fig. 15 represents plan views to explain essential processes of a method for manufacturing an active matrix substrate of a liquid crystal display panel, which makes up Embodiment 8 of the liquid crystal display device of the present invention. Here again, description will be given on the processes to prepare the data line, the source electrode and the drain electrode in the order of (1) to (4). First, (1) Preparation of gate electrode: A gate line and a bank BNK-G with groove pattern of the gate electrode are prepared on the surface of the insulating substrate - preferably a transparent glass substrate. An ink containing conductive particles such as silver or copper is dropped into the grooves of the bank BNK-G by ink jet coating method. It is then dried up, and a gate line GL and a gate electrode GT are prepared by baking.

(2) Ink jet coating of the gate line: On the gate insulator GI of the gate line, and not only on the crossing portion where data line crosses but also along the gate line GL, an ink of an insulating material with low dielectric constant is dropped by ink jet coating method, and an insulator LDP with low dielectric constant is prepared. The insulator LDP with low dielectric constant is formed on upper layers of all gate lines GL at least within a display region (a region where a multiple of pixels are arranged in matrix-like form) of the active matrix substrate.

(3) Preparation of island: A gate insulator GI is deposited over the entire surface of the substrate including the gate line GL, the gate electrode GT and the bank BNK-G. To prepare the gate insulator GI, silicon nitride (SiNx) is deposited by CVD. Then, by similar CVD processing, an amorphous silicon semiconductor layer and an n⁺ silicon semiconductor layer (ohmic contact layer) with silicon intermingled with phosphor or the like as impurities are deposited. By processing the ohmic contact layer, which has been turned to the amorphous silicon semiconductor layer, a semiconductor island SI is prepared on upper portion of the gate electrode GT. In this case, the ohmic contact layer prepared on the upper layer of the island SI is provided separately as connecting regions of the source electrode and the drain electrode respectively.

(4) Formation of source and channel: On the gate insulator GI, and on the insulator LDP with low dielectric constant on the crossing gate line GL, the data line, and the bank BNK-D with groove pattern of the source electrode SD1 and the drain electrode SD2 are prepared. An ink containing conductive particles such as silver or copper is dropped into the groove of the bank BNK-G. Then, it is dried up, and the source line, i.e. the data line DL, and the source electrode SD1 and the drain electrode SD2 are prepared by baking. In this case, a channel is formed between the source electrode SD1 and the drain electrode. Then, an active matrix substrate is prepared through pixel forming process to form a protective film, a pixel electrode, etc. and through coating process to coat the orientation film.

[0052] Fig. 16 is a cross-sectional view of an active matrix substrate along the line B-B with data line prepared in the process (4) of Fig. 15 with the liquid crystal sealed by attaching another substrate. As shown in the figure, a gate line GL is prepared on the surface of the glass substrate SUB1, which makes up the active matrix substrate. Including a portion where the gate line GL and the data line DL intersect, an ink of an insulating material with low dielectric constant such as aromatic hydrocarbon type organic polymer, polyallyl ether type organic polymer, etc. is dropped by ink jet coating method. When the ink is dried up, it is turned to an insulator LDP with low dielectric constant on the gate insulator GI along the gate line GL. A gate insulator GI is prepared on it. The gate insulator GI is prepared in flat form because of the presence of the bank BNK-G.

[0053] On the 2-layer insulating structure comprising the insulator LDP with low dielectric constant and the gate insulator GI, the data line DL is prepared to cross. As shown in Fig. 16, when ink is dropped by ink jet coating method and is hardened, peripheral edge of the insulator LDP with low dielectric constant is formed in a tapered form with gentle slope in cross sectional view. As a result, the data line intersecting the gate line GL goes over the gate line GL at a gentle angle in cross sectional view, and disconnection can be avoided, which may be caused by skip-over when jumping at a steep angle. Also, between the data line DL and the counter electrode CT of the color filter substrate SUB2, there is no dielectric substance, which narrows down the distance between electrodes except a portion of the gate line GL including intersection as described above. A liquid crystal LC is sealed between an orientation film ORI1 on the active matrix substrate SUB1 and an orientation film ORI2 on the color filter substrate SUB2.

[0054] According to Embodiment 8, cross capacity and counter capacity are not increased. Between the signal lines such as data line and the counter electrode, there is only an insulator LDP with low dielectric constant on the gate line as a dielectric substance to narrow down the distance between electrodes, and it is not a structure to extensively increase the capacity. For this reason, it is possible to provide a liquid crystal display device to be operated at high speed and with high precision without decreasing the performance characteristics of the thin-film transistor.

[0055] Here, description will be given on concrete effects of the present invention on capacity at the intersection in Embodiment 3 and on the counter electrode in Embodiment 7.

[0056] Now, description will be given on capacity at the intersection as described in connection with Embodiment 3 by referring to the cross-sectional structure of Fig. 6. Capacity C₀ of the intersection of only the gate insulator GI is given by:

$$C_0 = (\epsilon_{gi} / d_{gi}) S = (7.0 / 0.4) S$$

where

d_{gi}: Thickness of gate insulator GI (0.4 μm)
 ε_{gi}: Dielectric constant of gate insulator GI (7.0)
 S: Area of intersection

when a gate insulator GI is present between the gate line GL and the data line DL at the intersection of both lines.

[0057] Here, it is assumed that the thickness of the insulator LDP with low dielectric constant coated on the gate insulator GI by ink jet coating method is d. Then, the capacity C of the intersection is given by:

$$C = C_0 \{ 1 / (1 + d \epsilon_{gi} / d_{gi} \epsilon) \}$$

where

- d : Thickness of the insulator LDP with low dielectric constant
- ε: Dielectric constant of the insulator LDP with low dielectric constant

[0058] Here, if it is supposed that the dielectric constant E of the insulator LDP with low dielectric constant is approximately 3, and when the thickness d of the insulator LDP with low dielectric constant is changed, the capacity C at the intersection is given as:

$$d = 0.4 \mu m \rightarrow C = 0.30C_0$$

$$d = 0.8 \mu m \rightarrow C = 0.18C_0$$

$$d = 1.2 \mu m \rightarrow C = 0.13C_0$$

[0059] Now, the counter capacity as explained in connection with Embodiment 7 is now described by referring to the cross-sectional structure shown in Fig. 14. The capacity C₀ of the intersection of the gate insulator GI only is given by:

$$C_0 = \{ (\epsilon_{gi} \cdot \epsilon_{lc} / (d_{gi} \epsilon_{lc} + d_{lc} \epsilon_{gi}) \} S$$

where

- d_{gi} : Thickness of gate insulator GI (0.4 μm)
- ε_{gi} : Dielectric constant of gate insulator GI(7.0)
- d_{lc} : Thickness of liquid crystal LC(3.5 μm)
- ε_{lc} : Dielectric constant of liquid crystal LC(8.5)
- S : Area of opposing portion of the gate line GL and the counter electrode CT

[0060] When the insulator LDP with low dielectric constant is prepared by ink jet coating along the gate insulator GI, the counter capacity C is given by:

$$C = C_0 [1 / \{ (1 + (d \epsilon_{gi} \epsilon_{lc}) / (d_{gi} \epsilon_{lc} + d_{lc} \epsilon_{gi}) \epsilon \}]$$

where

- d : Thickness of the insulator LDP with low dielectric constant
- ε : Dielectric constant of the insulator LDP with low dielectric constant

[0061] Here, if it is assumed that dielectric constant ε of the insulator LDP with low dielectric constant is approximately 3, and when the thickness d of the insulator LDP with low dielectric constant is changed, the capacity C of the intersection is given by:

$$d = 1 \mu\text{m} \rightarrow C = 0.58C_0$$

$$d = 2 \mu\text{m} \rightarrow C = 0.41C_0$$

$$d = 3 \mu\text{m} \rightarrow C = 0.32C_0$$

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Claims

1. A liquid crystal display device with a liquid crystal layer (LC) interposed between a first insulating substrate (SUB1) and a second insulating substrate (SUB2), wherein said liquid crystal display device comprises:

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a plurality of gate lines (GL) prepared in parallel to each other and disposed on said first insulating substrate (SUB1);

a plurality of data lines (DL) prepared in parallel to each other and being disposed on said first insulating substrate (SUB1) to intersect the gate lines (GL) via a gate insulator layer (GI) ;

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each of regions enclosed by said gate lines (GL) and said data lines (DL) is regarded as a unit pixel region (PXL), and a region where said plurality of gate lines (GL) and said plurality of data lines (DL) cross each other makes up a display region (PNL) ;

said liquid crystal display device further comprising a plurality of thin-film transistors, each consisting of a gate electrode (GT) extending from a respective gate line (GL) to said unit pixel region, said gate insulator layer (GI) covering said gate line (GL) and said gate electrode (GT), a semiconductor layer (SI) sequentially prepared on said gate insulator layer (GI), an ohmic contact layer (NS) separately prepared on surface of said semiconductor (SI), and a source electrode (SD1) and a drain electrode (SD2) formed on said separated ohmic contact layer (NS); and

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characterised in that the liquid crystal display device comprises a further insulator layer (LDP) with low dielectric constant on an upper or lower surface of the gate insulator layer (GI), locally formed at the intersections of said gate lines (GL) and said data lines (DL), the peripheral edges of said further insulator layer (LDP) on each side of each gate line (GL) having a tapered form with a gentle slope in cross sectional view.

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2. A liquid crystal display device according to claim 1, wherein said further insulator layer (LDP) is provided along said gate lines (GL) in addition to all said intersections.

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3. A liquid crystal display device according to claim 1 or 2, wherein said further insulator layer (LDP) is formed of a heat-resistant resin.

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4. A liquid crystal display device according to claim 1 or 2, wherein said further insulator layer (LDP) is formed of an aromatic hydrocarbon type organic polymer or a polyallyl ether type organic polymer.

5. A method for manufacturing a liquid crystal display device with a liquid crystal layer (LC) interposed between a first insulating substrate (SUB1) and a second insulating substrate (SUB2), said method comprising the steps of:

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preparing a plurality of gate lines (GL) running in parallel to each other on said first insulating substrate (SUB1) ; depositing a gate insulator layer (GI) to cover said first insulating substrate (SUB1) and said gate lines (GL) ; locally preparing a further insulator layer (LDP) with low dielectric constant on said gate insulator layer (GI) at portions of said gate lines (GL); and

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preparing a plurality of data lines (DL) running in parallel to each other and crossing said gate lines (GL) on said gate insulator layer (GI) and said further insulator layer (LDP) at said portions;

characterised in that said insulator layer (LDP) with low dielectric constant is prepared by ink jet coating, peripheral edges of the insulator layer (LDP) with low dielectric constant on each side of the gate lines (GL) being turned into a tapered form with a gentle slope in cross sectional view.

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6. A method for manufacturing a liquid crystal display device with a liquid crystal layer (LC) interposed between a first insulating substrate (SUB1) and a second insulating substrate (SUB2), said method comprising the steps of:

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preparing a plurality of gate lines (GL) running in parallel to each other on said first insulating substrate (SUB1); locally preparing an insulator layer (LDP) with low dielectric constant on said gate lines (GL) at portions of said gate lines (GL);

depositing a gate insulator layer (GI) to cover said first insulating substrate (SUB1), said gate lines (GL) and said insulator layer (LDP) with low dielectric constant; and

preparing a plurality of data lines (DL) running in parallel to each other and crossing said gate lines (GL) on said insulator layer (LDP) with low dielectric constant and said gate insulator layer (GI) at said portions, **characterised in that** said insulator layer (LDP) with low dielectric constant is prepared by ink jet coating, peripheral edges of the insulator layer (LDP) with low dielectric constant (LDP) on each side of the gate lines (GL) being turned into a tapered form with a gentle slope in cross sectional view.

7. A method according to claim 5 or claim 6 wherein said further insulator layer with low dielectric constant (LDP) is prepared along the whole of said gate lines (GL).

8. A method for manufacturing a liquid crystal display device according to one of the claims 5 to 7, said method further comprising a step of:

preparing a thin-film transistor, said thin-film transistor has a semiconductor layer (SI) on said gate insulator layer (GI) and an ohmic contact layer (NS) separately provided on a surface of said semiconductor layer (SI), a source electrode (SD1) and a drain electrode (SD2) being prepared on said separate ohmic contact layer (NS), and a display region (PNL) is made up with unit pixel regions (PXL) to be formed on each portion enclosed by said plurality of gate lines (GL) and said plurality of data lines (DL).

9. A method for manufacturing a liquid crystal display device according to one of claims 5 to 8, wherein said further insulator layer with low dielectric constant (LDP) is formed of a heat-resistant resin.

10. A method for manufacturing a liquid crystal display device according to one of claims 5 to 8, wherein said further insulator layer with low dielectric constant (LDP) is formed of an aromatic hydrocarbon type organic polymer or polyallyl ether type organic polymer.

Patentansprüche

1. Flüssigkristallanzeigevorrichtung mit einer Flüssigkristall- (LC-) Schicht, die zwischen einem ersten isolierenden Substrat (SUB1) und einem zweiten isolierenden Substrat (SUB2) angeordnet ist, worin die Flüssigkristallanzeigevorrichtung Folgendes umfasst:

eine Vielzahl an Gate-Leitungen (GL), die parallel zu einander hergestellt und auf dem ersten isolierenden Substrat (SUB1) angeordnet sind;

eine Vielzahl an Datenleitungen (DL), die parallel zu einander hergestellt und auf dem ersten isolierenden Substrat (SUB1) so angeordnet sind, dass sie die Gate-Leitungen (GL) über eine Gate-Isolationsschicht (GI) hinweg schneiden;

wobei jeder der durch die Gate-Leitungen (GL) und Datenleitungen (DL) eingeschlossenen Bereiche als Einheitspixelbereich (PXL) definiert ist und ein Bereich, in dem die Vielzahl an Gate-Leitungen (GL) und die Vielzahl an Datenleitungen (DL) einander kreuzen, einen Anzeigebereich (PNL) bildet;

wobei die Flüssigkristallanzeigevorrichtung ferner Folgendes umfasst: eine Vielzahl an Dünnschichttransistoren, die jeweils aus einer Gate-Elektrode (GT) bestehen, die sich von jeweils einer Gate-Leitung (GL) zu dem Einheitspixelbereich erstreckt, wobei die Gate-Isolationsschicht (GI) die Gate-Leitung (GL) und die Gate-Elektrode (GT) abdeckt; eine Halbleiterschicht (SI), die sequenziell auf der Gate-Isolationsschicht (GI) hergestellt ist; eine ohmsche Kontaktschicht (NS), die separat auf der Oberfläche der Halbleiterschicht (SI) hergestellt ist; und eine Source-Elektrode (SD1) und eine Drain-Elektrode (SD2), die auf der separaten ohmschen Kontaktschicht (NS) ausgebildet sind;

dadurch gekennzeichnet, dass die Flüssigkristallanzeigevorrichtung eine weitere Isolationsschicht (LDP) mit niedriger Dielektrizitätskonstante auf einer oberen oder unteren Oberfläche der Gate-Isolationsschicht (GI) umfasst, die lokal an den Schnittpunkten der Gate-Leitungen (GL) und der Datenleitungen (DL) ausgebildet ist,

wobei die am Rand gelegenen Kanten der weiteren Isolationsschicht (LDP) auf jeder Seite jeder Gate-Leitung (GL) eine angeschrägte Form mit einem in der Querschnittsansicht flachen Anstieg aufweisen.

2. Flüssigkristallanzeigevorrichtung nach Anspruch 1, worin die weitere Isolationsschicht (LDP) zusätzlich zu allen Schnittpunkten entlang der Gate-Leitungen (GL) bereitgestellt ist.

3. Flüssigkristallanzeigevorrichtung nach Anspruch 1 oder 2, worin die weitere Isolationsschicht (LDP) aus einem

wärmebeständigen Harz ausgebildet ist.

4. Flüssigkristallanzeigevorrichtung nach Anspruch 1 oder 2, worin die weitere Isolationsschicht (LDP) aus einem organischen Polymer vom aromatischen Kohlenwasserstofftyp oder einem organischen Polymer vom Polyallylthertyp ausgebildet ist.

5. Verfahren zur Herstellung einer Flüssigkristallanzeigevorrichtung mit einer Flüssigkristallschicht (LC), die zwischen einem ersten isolierenden Substrat (SUB1) und einem zweiten isolierenden Substrat (SUB2) angeordnet ist, wobei das Verfahren folgende Schritte umfasst:

Herstellen einer Vielzahl an Gate-Leitungen (GL), die parallel zueinander verlaufen, auf dem ersten isolierenden Substrat (SUB1);

Abscheiden einer Gate-Isolationsschicht (GI) zum Abdecken des ersten isolierenden Substrats (SUB1) und der Gate-Leitungen (GL);

lokales Herstellen einer weiteren Isolationsschicht mit niedriger Dielektrizitätskonstante (LDP) auf der Gate-Isolationsschicht (GI) auf Abschnitten der Gate-Leitungen (GL); und

Herstellen einer Vielzahl an Datenleitungen (DL), die parallel zueinander verlaufen und die Gate-Leitungen (GL) auf der Gate-Isolationsschicht (GI) und der weiteren Isolationsschicht (LDP) auf den zuvor genannten Abschnitten kreuzen,

dadurch gekennzeichnet, dass die Isolationsschicht mit niedriger Dielektrizitätskonstante (LDP) durch Tintenstrahlbeschichtung hergestellt wird, wobei die am Rand gelegenen Kanten der Isolationsschicht mit niedriger Dielektrizitätskonstante (LDP) auf jeder Seite der Gate-Leitungen (GL) in eine angeschrägte Form gebracht werden, wobei sie in der Querschnittsansicht einen flachen Anstieg aufweisen.

6. Verfahren zur Herstellung einer Flüssigkristallanzeigevorrichtung mit einer Flüssigkristallschicht (LC), die zwischen einem ersten isolierenden Substrat (SUB1) und einem zweiten isolierenden Substrat (SUB2) angeordnet ist, wobei das Verfahren folgende Schritte umfasst:

Herstellen einer Vielzahl an Gate-Leitungen (GL), die parallel zueinander verlaufen, auf dem ersten isolierenden Substrat (SUB1);

lokales Herstellen einer Isolationsschicht (LDP) mit niedriger Dielektrizitätskonstante auf den Gate-Leitungen (GL) auf Abschnitten der Gate-Leitungen (GL);

Abscheiden einer Gate-Isolationsschicht (GI) zur Abdeckung des ersten Isolationssubstrats (SUB1), der Gate-Leitungen (GL) und der Isolationsschicht (LDP) mit niedriger Dielektrizitätskonstante; und

Herstellen einer Vielzahl an Datenleitungen (DL), die parallel zueinander verlaufen und die Gate-Leitungen (GL) auf der Isolationsschicht (LDP) mit niedriger Dielektrizitätskonstante und der Gate-Isolationsschicht (GI) auf den zuvor genannten Abschnitten kreuzen, **dadurch gekennzeichnet, dass** die Isolationsschicht (LDP) mit niedriger Dielektrizitätskonstante durch Tintenstrahlbeschichtung ausgebildet wird, wobei die am Rand gelegenen Kanten der Isolationsschicht (LDP) mit niedriger Dielektrizitätskonstante auf jeder Seite der Gate-Leitungen (GL) in eine angeschrägte Form gebracht werden, wobei sie in der Querschnittsansicht einen flachen Anstieg aufweisen.

7. Verfahren nach Anspruch 5 oder 6, worin die weitere Isolationsschicht (LDP) mit niedriger Dielektrizitätskonstante entlang aller Gate-Leitungen (GL) hergestellt wird.

8. Verfahren zur Herstellung einer Flüssigkristallanzeigevorrichtung nach einem der Ansprüche 5 bis 7, wobei das Verfahren ferner folgenden Schritt umfasst:

Herstellen eines Dünnschichttransistors, wobei der Dünnschichttransistor eine Halbleiterschicht (SI) auf der Gate-Isolationsschicht (GI) und eine separat bereitgestellte ohmsche Kontaktschicht (NS) auf einer Oberfläche der Halbleiterschicht (SI) aufweist, wobei eine Source-Elektrode (SD1) und eine Drain-Elektrode (SD2) auf der separaten ohmschen Kontaktschicht (NS) hergestellt sind; und ein Anzeigebereich (DNL) aus Einheitspixelbereichen (PXL) ausgebildet wird, die auf jedem durch die Vielzahl an Gate-Leitungen (GL) und die Vielzahl an Datenleitungen (DL) umschlossenen Abschnitten auszubilden sind.

9. Verfahren zur Herstellung einer Flüssigkristallanzeigevorrichtung nach einem der Ansprüche 5 bis 8, worin die weitere Isolationsschicht mit niedriger Dielektrizitätskonstante (LDP) aus einem wärmebeständigen Harz ausgebildet ist.

10. Verfahren zur Herstellung einer Flüssigkristallanzeigevorrichtung nach einem der Ansprüche 5 bis 8, worin die weitere Isolationsschicht (LDP) aus einem organischen Polymer vom aromatischen Kohlenwasserstofftyp oder einem organischen Polymer vom Polyallylethertyp ausgebildet ist.

5

Revendications

1. Dispositif d'affichage à cristaux liquides avec une couche de cristaux liquides (LC) interposée entre un premier substrat isolant (SUB1) et un deuxième substrat isolant (SUB2), où ledit dispositif d'affichage à cristaux liquides comprend:

10

une pluralité de lignes de grille (GL) préparées en parallèle les unes aux autres et disposées sur ledit premier substrat isolant (SUB1);

15

une pluralité de lignes de données (BL) préparées en parallèle les unes aux autres et étant disposées sur ledit premier substrat isolant (SUB1) pour se croiser avec les lignes de grille (GL) par une couche d'isolation de grille (GI);

20

chacune des régions renfermées par lesdites lignes de grille (GL) et lesdites lignes de données (DL) est considérée comme une région de pixels unitaires (PXL), et une région dans laquelle ladite pluralité de lignes de grille (GL) et ladite pluralité de lignes de données (DL) se croisent constitue une région d'affichage (PNL);

25

ledit dispositif d'affichage à cristaux liquides comprend en outre une pluralité de transistors à film mince, chacun consistant en une électrode de grille (GT) s'étendant d'une ligne de grille respective (GL) à ladite région de pixels unitaires, ladite couche d'isolation de grille (GI) couvrant ladite ligne de grille (GL) et ladite électrode de grille (GT), une couche semi-conductrice (SI) séquentiellement préparée sur ladite couche d'isolation de grille (GI), une couche de contact ohmique (NS) préparée séparément sur la surface de ladite couche semi-conductrice (SI), et une électrode source (SD1) et une électrode drain (SD2) formées sur ladite couche de contact ohmique séparée (NS); et

30

caractérisé en ce que le dispositif d'affichage à cristaux liquides comprend une autre couche d'isolation (LDP) avec une faible constante diélectrique sur une surface supérieure ou inférieure de la couche d'isolation de grille (GI), formée localement aux intersections desdites lignes de grille (GL) et desdites lignes de données (DL), les bords périphériques de ladite autre couche d'isolation (LDP) sur chaque côté de chaque ligne de grille (GL) ayant une forme diminuée avec une légère inclinaison vue en section transversale.

35

2. Dispositif d'affichage à cristaux liquides selon la revendication 1, où ladite autre couche d'isolation (LDP) est réalisée le long desdites lignes de grille (GL) en plus de toutes lesdites intersections.

3. Dispositif d'affichage à cristaux liquides selon la revendication 1 ou 2, où ladite autre couche d'isolation (LDP) est réalisée en une résine résistante à la chaleur.

40

4. Dispositif d'affichage à cristaux liquides selon la revendication 1 ou 2, où ladite autre couche d'isolation (LDP) est réalisée à partir d'un polymère organique du type d'hydrocarbure aromatique ou d'un polymère organique du type de polyallyl éther.

45

5. Procédé de fabrication d'un dispositif d'affichage à cristaux liquides avec une couche de cristaux liquides (LC) interposée entre un premier substrat isolant (SUB1) et un deuxième substrat isolant (SUB2), ledit procédé comprenant les étapes de:

préparer une pluralité de lignes de grille (GL) s'étendant parallèlement les unes aux autres sur ledit premier substrat isolant (SUB1);

50

déposer une couche d'isolation de grille (GI) pour couvrir ledit premier substrat isolant (SUB1) et lesdites lignes de grille (GL);

préparer localement une autre couche d'isolation (LDP) d'une faible constante diélectrique sur ladite couche d'isolation de grille (GI) aux portions desdites lignes de grille (GL); et

55

préparer une pluralité de lignes de données (DL) s'étendant parallèlement les unes aux autres et se croisant avec lesdites lignes de grille (GL) sur ladite couche d'isolation de grille (GI) et ladite autre couche d'isolation (LDP) auxdites portions;

caractérisé en ce que ladite couche d'isolation (LDP) d'une faible constante diélectrique est préparée par un revêtement à jet d'encre, les bords périphériques de la couche d'isolation (LDP) d'une faible constante diélectrique (LDP) sur chaque côté des lignes de grille (GL) étant tournés en une forme diminuée avec une légère

inclinaison en une vue en section transversale.

- 5 6. Procédé de fabrication d'un dispositif d'affichage à cristaux liquides avec une couche de cristaux liquides (LC) interposée entre un premier substrat isolant (SUB1) et un deuxième substrat isolant (SUB2), ledit procédé comprenant les étapes de:

préparer une pluralité de lignes de grille (GL) s'étendant parallèlement les unes aux autres sur ledit premier substrat isolant (SUB1);

10 préparer localement une couche d'isolation (LDP) avec une faible constante diélectrique sur lesdites lignes de grille (GL) aux portions desdites lignes de grille (GL);

déposer une couche d'isolation de grille (GI) pour couvrir ledit premier substrat isolant (SUB1), lesdites lignes de grille (GL) et ladite couche d'isolation d'une faible constante diélectrique; et

15 préparer une pluralité de lignes de données (DL) s'étendant parallèlement les unes aux autres et se croisant avec lesdites lignes de grille (GL) sur ladite couche d'isolation (LDP) avec une faible constante diélectrique et ladite couche d'isolation de grille (GI) auxdites portions, **caractérisé en ce que** ladite couche d'isolation (LDP) d'une faible constante diélectrique est préparée par un revêtement à jet d'encre, les bords périphériques de la couche d'isolation (LDP) d'une faible constante diélectrique (LDP) sur chaque côté des lignes de grille (GL) étant tournées en une forme diminuée avec une légère inclinaison vue en section transversale.

- 20 7. Procédé selon la revendication 5 ou la revendication 6, dans lequel ladite autre couche d'isolation d'une faible constante diélectrique (LDP) est préparée le long de l'ensemble desdites lignes de grille (GL).

- 25 8. Procédé de fabrication d'un dispositif d'affichage à cristaux liquides selon l'une des revendications 5 à 7, ledit procédé comprenant en outre une étape de:

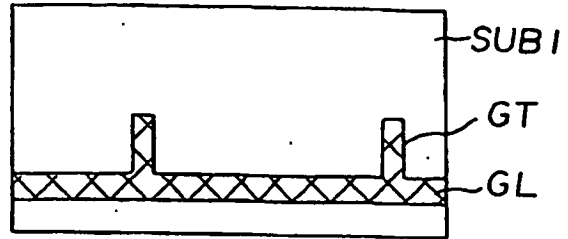
30 préparer un transistor à film mince, ledit transistor à film mince possède une couche semi-conductrice (SI) sur ladite couche d'isolation de grille (GI) et une couche de contact ohmique (NS) réalisée séparément sur une surface de ladite couche semi-conductrice (SI), une électrode source (SD1) et une électrode drain (SD2) étant préparées sur ladite couche de contact ohmique séparée (NS), et une région d'affichage (PNL) est constituée avec des régions de pixels unitaires (PXL) à former sur chaque portion renfermée par ladite pluralité de lignes de grille (GL) et ladite pluralité de lignes de données (DL).

- 35 9. Procédé de fabrication d'un dispositif d'affichage à cristaux liquides selon l'une quelconque des revendications 5 à 8, où ladite autre couche d'isolation avec une faible constante diélectrique (LDP) est réalisée à partir d'une résine résistant à la chaleur.

- 40 10. Procédé de fabrication d'un dispositif d'affichage à cristaux liquides selon l'une quelconque des revendications 5 à 8, où ladite autre couche d'isolation avec une faible constante diélectrique (LDP) est réalisée à partir d'un polymère organique du type d'hydrocarbure aromatique ou d'un polymère organique du type de polyallyl éther.

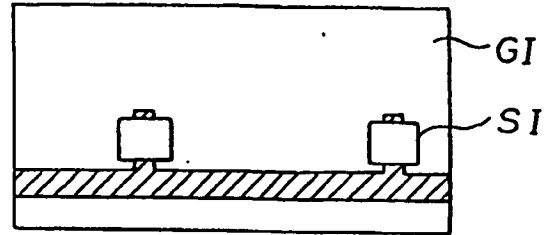
FIG.1

(1) Preparation of gate electrode

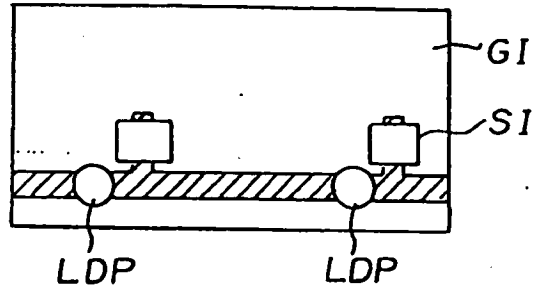


3-layer CVD ↓

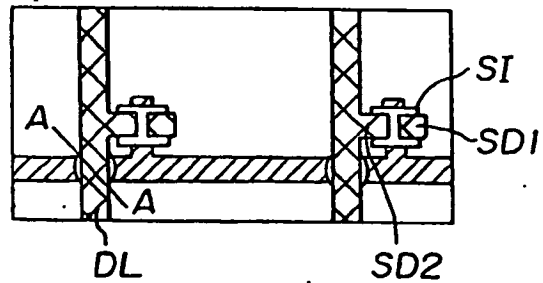
(2) Formation of island



(3) Ink Jet coating of the crossing portion



(4) Formation of source and channel



Formation of pixels

FIG.2

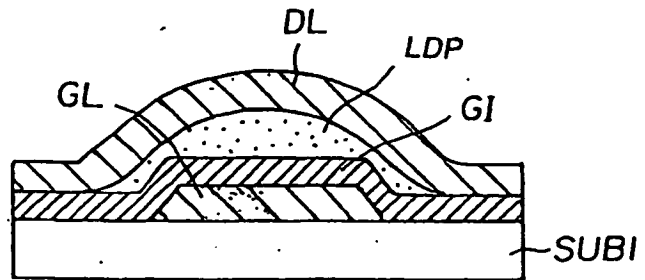


FIG.3

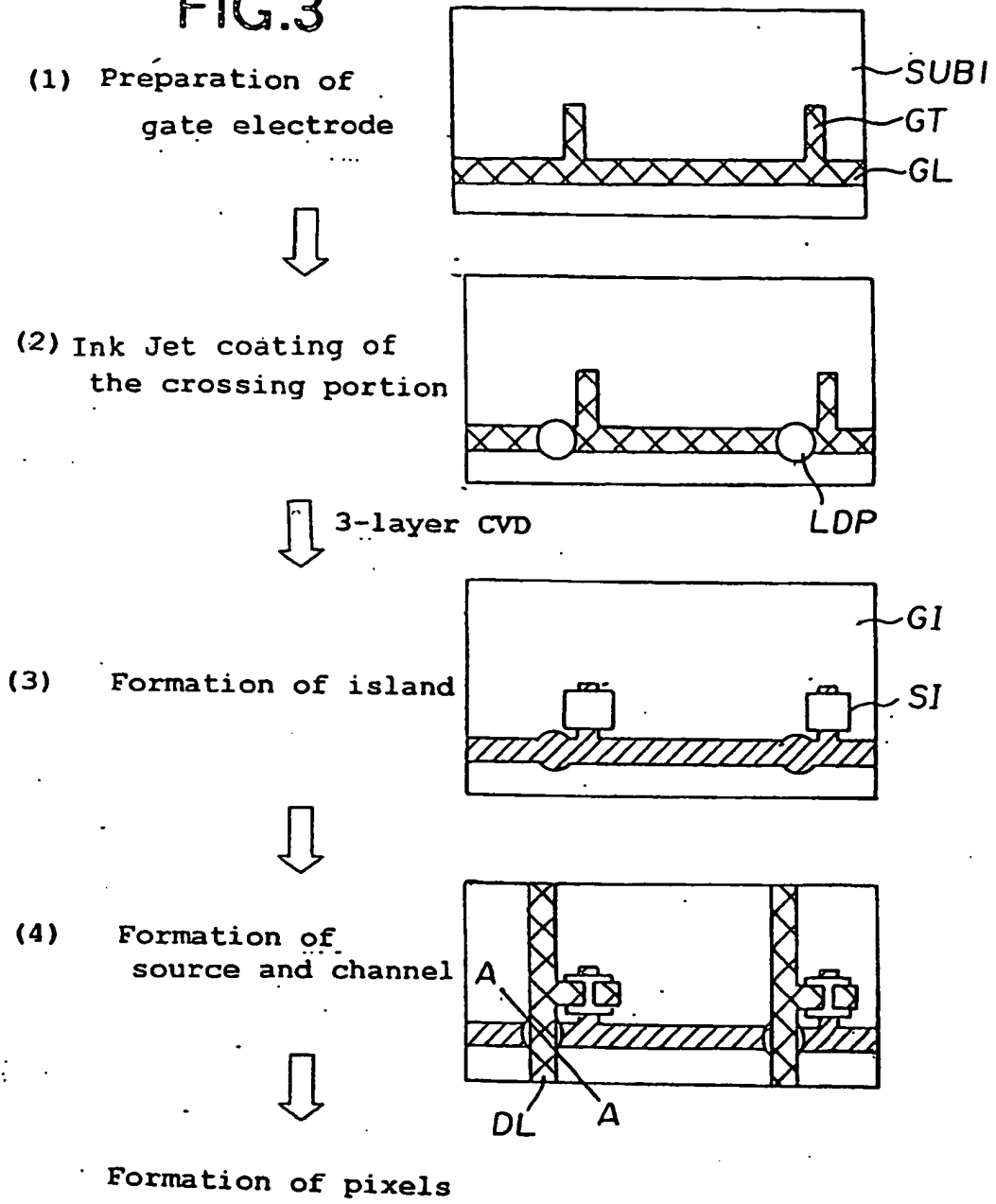


FIG.4

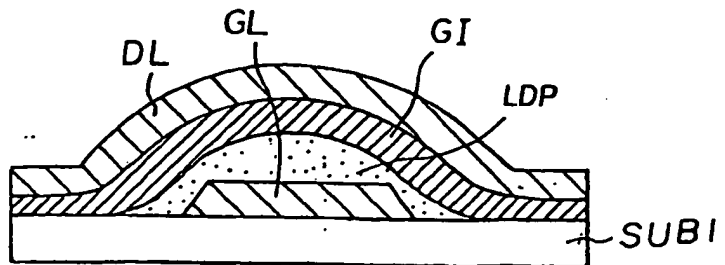


FIG.5

(1) Preparation of gate electrode

3-layer CVD ↓

(2) Formation of island
(or formation of TFT)



(3) Ink Jet coating of the crossing portion



(4) Formation of source and channel



Formation of pixels

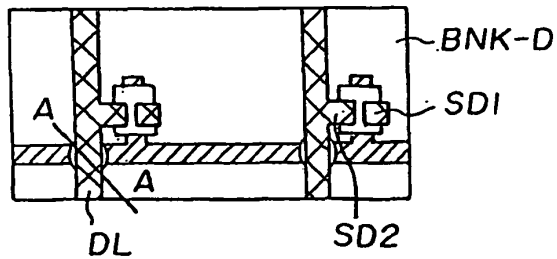
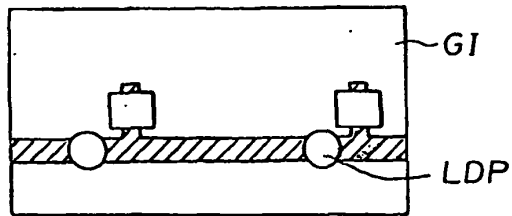
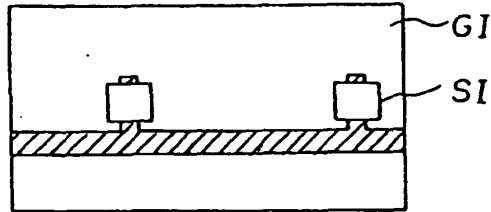
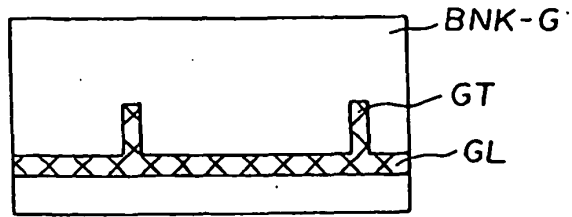


FIG.6

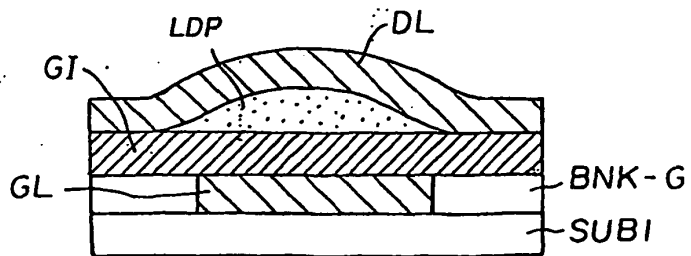
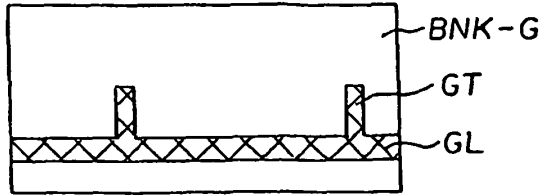
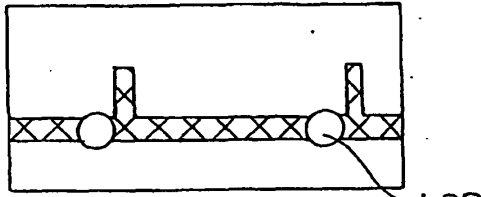


FIG.7

(1) Preparation of gate electrode

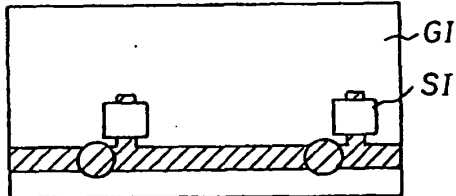


(2) Ink Jet coating of the crossing portion

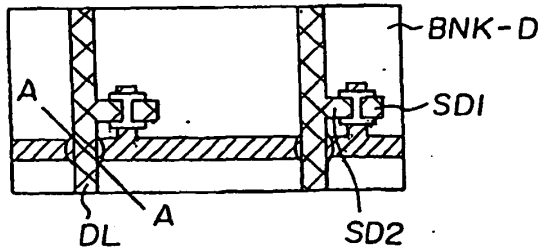


3-layer CVD

(3) Formation of island (or formation of TFT)



(4) Formation of source and channel



Formation of pixels

FIG.8

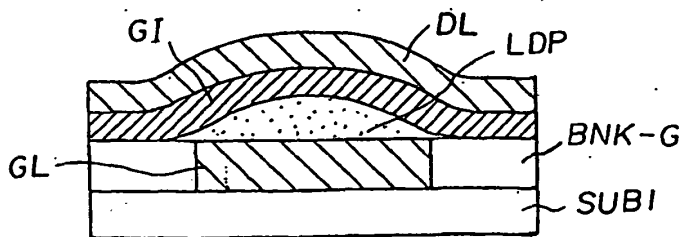
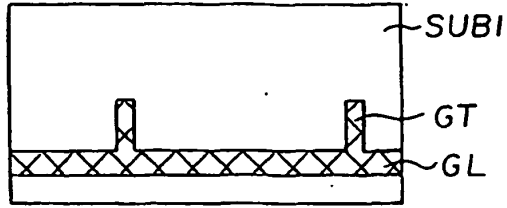


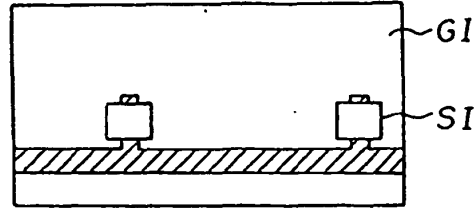
FIG.9

(1) Preparation of gate electrode



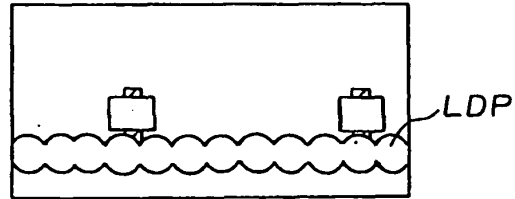
↓ 3-layer CVD

(2) Formation of island



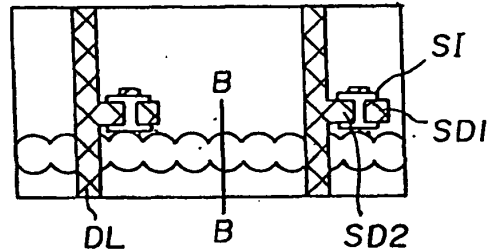
↓

(3) Ink Jet coating of the gate line portion



↓

(4) Formation of source and channel



↓

Formation of pixels

FIG.10

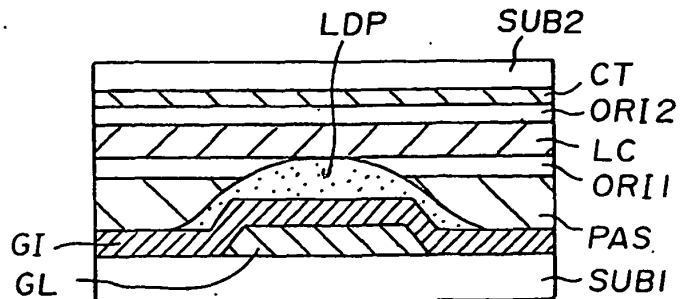
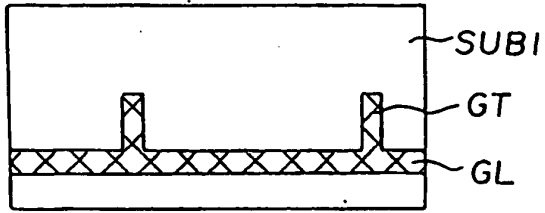
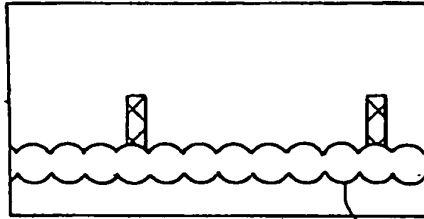


FIG.11

(1) Preparation of gate electrode

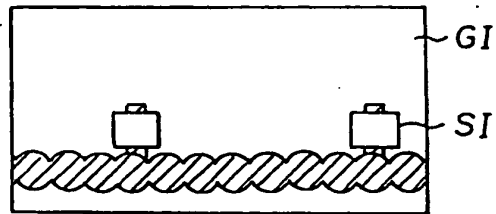


(2) Ink Jet coating of the gate line portion

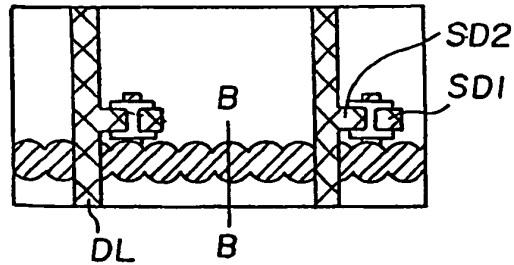


3-layer CVD

(3) Formation of island



(4) Formation of source and channel



Formation of pixels

FIG.12

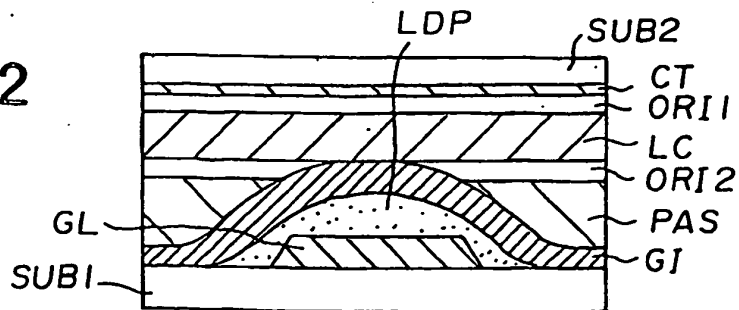
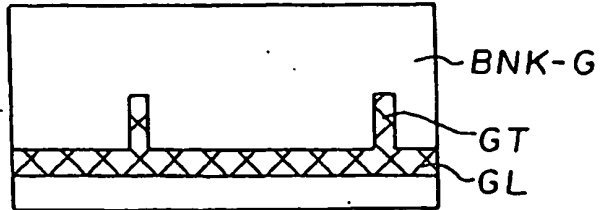


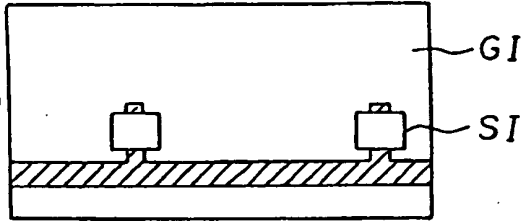
FIG.13

(1) Preparation of gate electrode



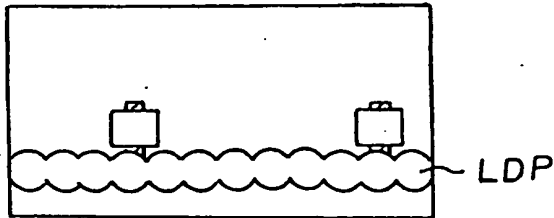
↓ 3-layer CVD

(2) Formation of island (or formation of TFT)



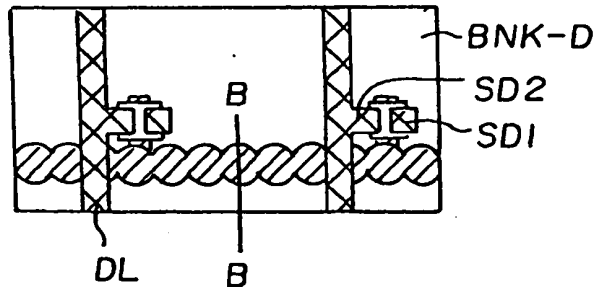
↓

(3) Ink Jet coating of the gate line portion



↓

(4) Formation of source and channel



Formation of pixels

FIG.14

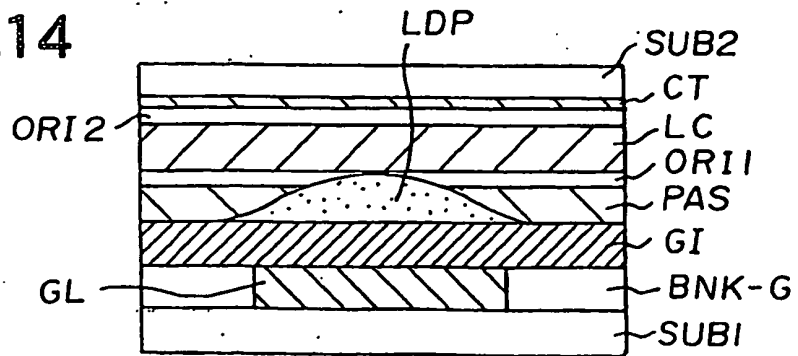


FIG.15

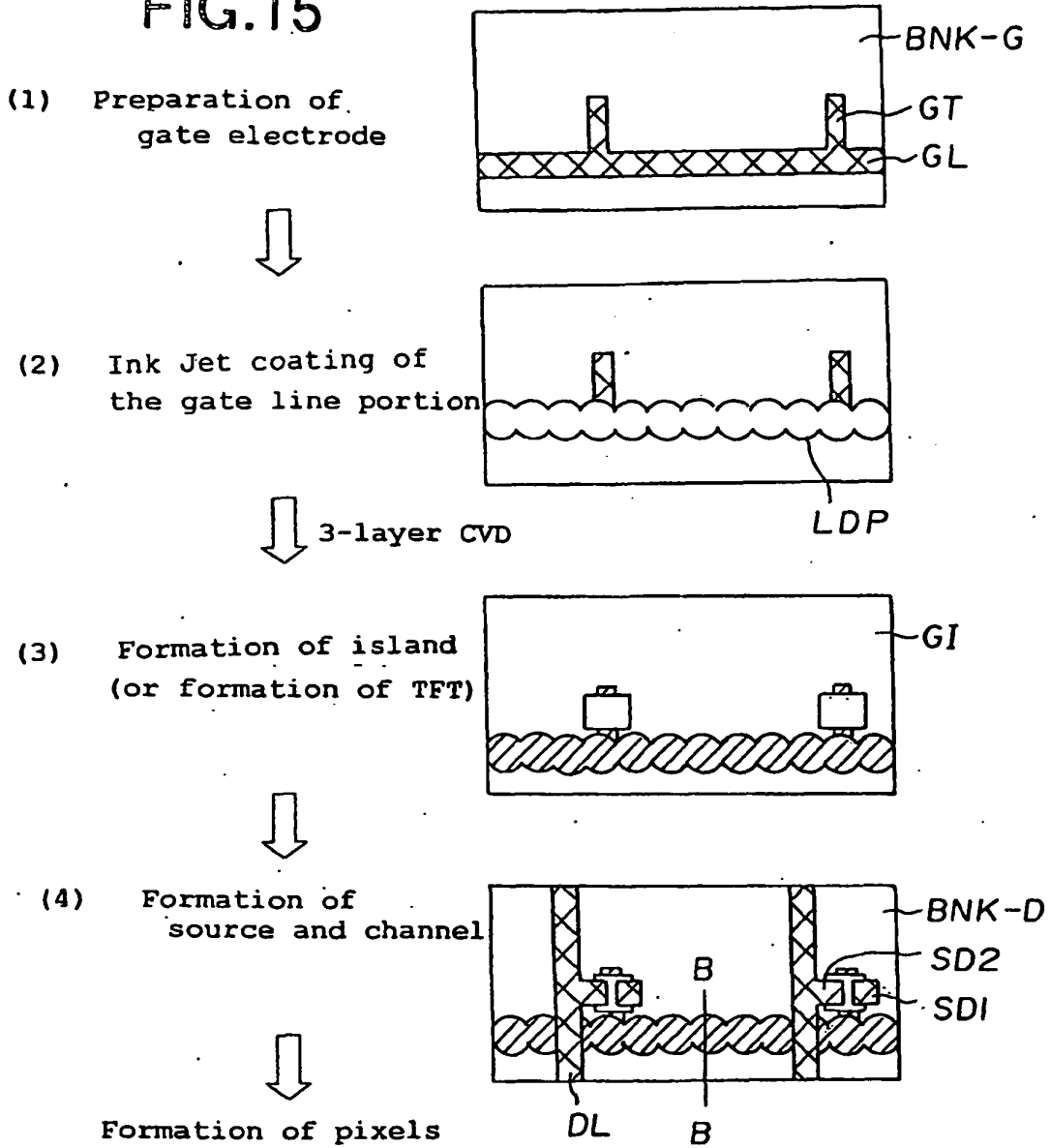


FIG.16

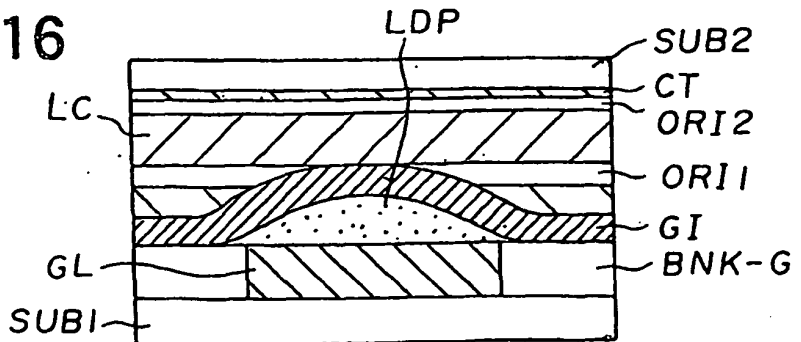


FIG.17(a)

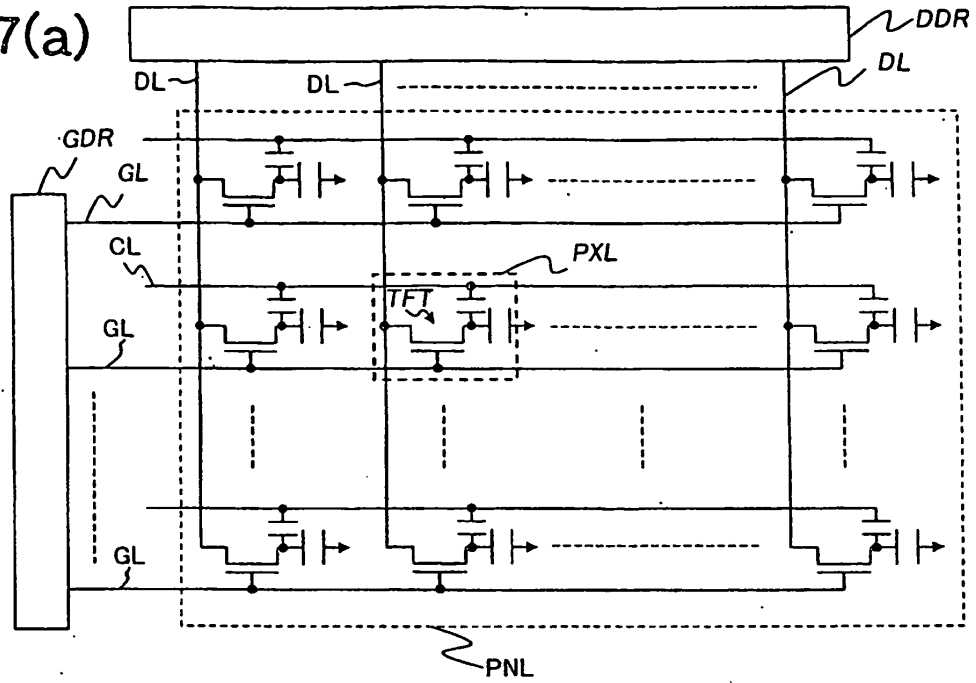


FIG.17(b)

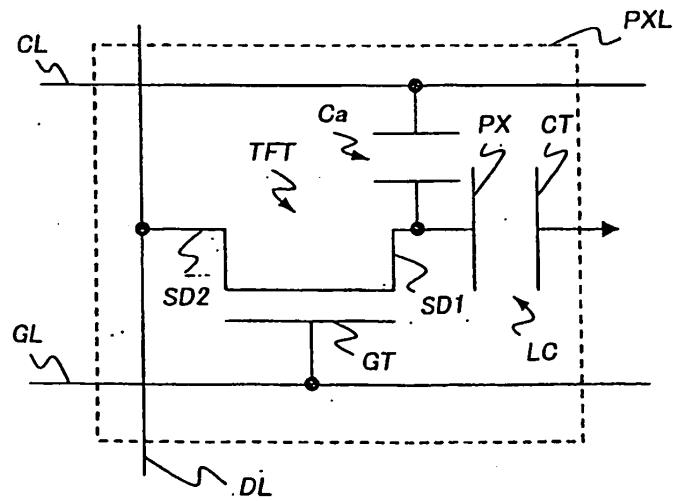


FIG.18(a)

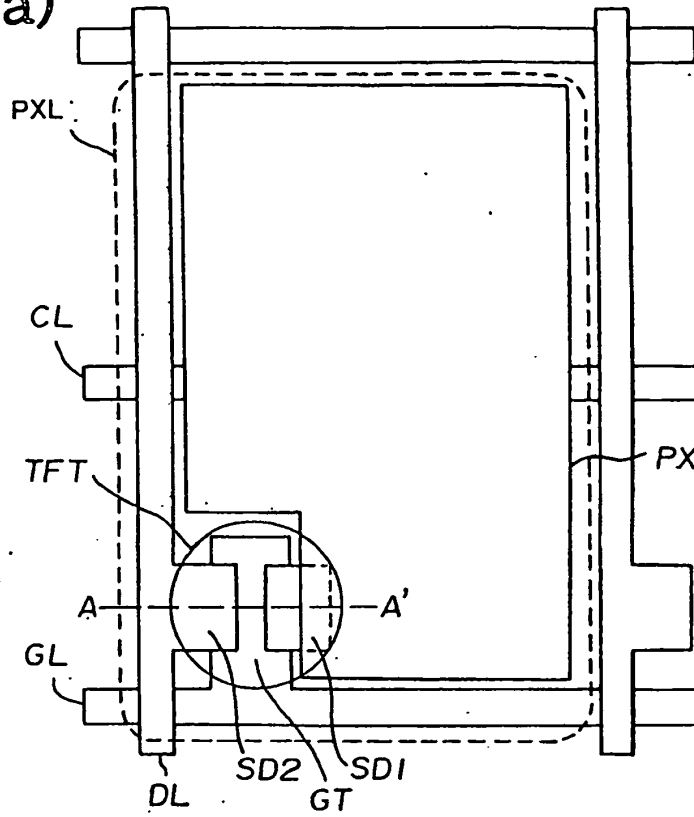
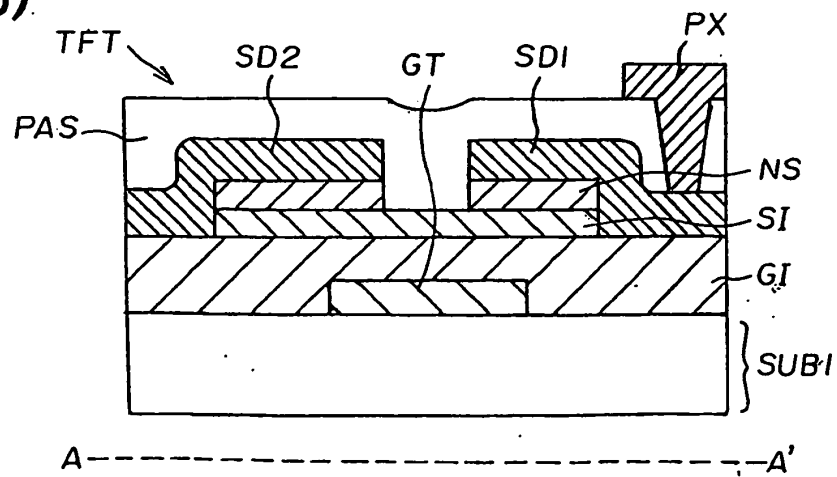


FIG.18(b)



REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

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- US 20050095356 A [0016]
- EP 0750350 A [0016]
- US 5365079 A [0016]
- JP 9045774 A [0016]

专利名称(译)	液晶显示装置及其制造方法		
公开(公告)号	EP1801640B1	公开(公告)日	2009-09-09
申请号	EP2006256296	申请日	2006-12-11
[标]申请(专利权)人(译)	未来视野股份有限公司		
申请(专利权)人(译)	未来愿景INC.		
当前申请(专利权)人(译)	未来愿景INC.		
发明人	YOSHIMOTO, YOSHIKAZU C/O FUTURE VISION INC.		
IPC分类号	G02F1/1362 H01L27/12 H01L21/77 G02F1/1368		
CPC分类号	G02F1/136286 G02F1/1368 G02F2001/13606 H01L27/12 H01L27/124 H01L27/1248 H01L27/1292		
优先权	2005365739 2005-12-20 JP		
其他公开文献	EP1801640A1		
外部链接	Espacenet		

摘要(译)

本发明提供一种液晶显示装置，其通过提高薄膜晶体管的性能而不增加栅极线和数据线的交叉容量而高速且高精度地操作。在构成液晶显示装置的液晶显示面板的有源矩阵基板SUB1上准备的栅极线GL和数据线DL的交叉处的栅极绝缘体GI的上层，低绝缘材料通过喷墨涂覆法降低介电常数以制备另一绝缘体LDP，以改善在硅半导体层SI上制备的薄膜晶体管的性能特性，而不增加所述交叉点上的交叉容量。

$$C_0 = (\epsilon_{gl} / d_{gl}) S = (7.0 / 0.4) S$$