(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 335 343 B1

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
25.07.2012 Bulletin 2012/30

(51) Int Cl.:
G09G 3/36 *(2006.01)* ***G02F 1/1362*** *(2006.01)*

(21) Application number: **02258053.4**

(22) Date of filing: **22.11.2002**

(54) **Liquid crystal display with reduced driving voltage and separate driving circuits for positive and negative voltages**

Flüssigkristallanzeige mit reduzierter Steuerspannung und getrennten Steuerschaltungen für positive und negative Spannungen

Affichage à cristaux liquides avec tension de commande réduite et circuits de commande séparés pour tensions positives et négatives

(84) Designated Contracting States:
DE FR

(30) Priority: **05.02.2002 JP 2002027590**

(43) Date of publication of application:
13.08.2003 Bulletin 2003/33

(73) Proprietor: **Sharp Kabushiki Kaisha**
Osaka-shi, Osaka 545-8522 (JP)

(72) Inventor: **Sasaki, Nobuo,**
c/o Fujitsu Limited
Kawasaki-shi,
Kanagawa 211-8588 (JP)

(74) Representative: **Hitching, Peter Matthew et al**
Haseltine Lake LLP
Lincoln House, 5th Floor
300 High Holborn
London
WC1V 7JH (GB)

(56) References cited:
EP-A- 0 915 453
JP-A- 06 266 315
US-A- 5 436 635
US-A1- 2001 050 664

EP 1 335 343 B1

Printed by Jouve, 75001 PARIS (FR)

Description

[0001] The present invention relates to a liquid crystal display (LCD) and, more particularly, to an active matrix type TFT LCD having a TFT (thin film transistor) as a switching element at each pixel.

[0002] The market of LCDs is rapidly growing because LCDs have become able to provide display quality that sufficiently allows them to replace CRTs which have been typical displays in the related art. They are used as displays of various viewers, cellular phones, PDAs (personal digital assistants), and notebook type personal computers as well as for monitors of desktop computers and television receivers for home use, thanking to their advantage of being flat panels. Thus, LCDs are used as displays that provide from small screens having diagonal dimensions of about 2 inches to large screens having diagonal dimensions in the excess of 40 inches. More and more LCDs are used in various fields as full-color displays capable of displaying still image and dynamic images.

[0003] Referring to the trend in LCD techniques, the main stream has shifted from the passive matrix type that has no switching element in a pixel to the active matrix type that has switching elements such as TFTs. Further, referring to the material of channel regions (active semiconductor layers) of TFTs formed in pixels of active matrix type LCDs, a-Si (amorphous silicon) is being replaced by p-Si (polysilicon) having higher carrier mobility.

[0004] Structure of TFT LCDs will now be briefly described. For example, in the case of a transmission type TFT LCD that employs a back-light unit, a TFT substrate (array substrate) that is a transparent insulated substrate such as a glass substrate and an opposite substrate are combined in a face-to-face relationship with a predetermined cell gap therebetween, and a liquid crystal is sealed between the substrates. A plurality of pixel electrodes are provided in the form of a matrix on the TFT substrate, and the TFT is connected to each of the pixel electrodes. A common electrode is formed on the opposite substrate. In the case of a color display LCD, a color filter (CF) is formed on either the TFT substrate or the opposite substrate. Alignment films are formed at interfaces between the substrates and the liquid crystal layer. Polarizers having a crossed Nicols configuration, for example, are applied to the outside of both substrates.

[0005] Fig. 7 is an equivalent circuit for one pixel of a previously-considered TFT LCD. As shown in Fig. 7, a gate electrode G of a TFT is connected to a gate bus line Lg. A source electrode S of the TFT is connected to a pixel electrode Pe, and a drain electrode D is connected to a data bus line Ld. A liquid crystal layer lc is sandwiched by the pixel electrode Pe and a common electrode Ce to form a liquid crystal capacitance Clc. A storage capacitor Cs is connected in parallel with the liquid crystal capacitance in practice, although not shown.

[0006] A gate voltage Vg is applied to the gate bus line Lg from a gate bus line driving circuit that is not shown. A grayscale voltage Vd is applied to the data bus line Ld from a data bus line driving circuit that is not shown. A common voltage Vcom (= 0 V) is applied to the common electrode Ce.

[0007] The liquid crystal lc is positively or negatively anisotropic in its dielectric constant, which results in a property that the liquid crystal molecules rotate in accordance with the strengthof an electric field applied thereto. The liquid crystal lc is also anisotropic in its refractive index, which results in a property that the polarization of light passing through the liquid crystal lc changes in accordance with the rotation of the liquid crystal molecules. Therefore, when a voltage is applied between the pixel electrode Pe and the common electrode Ce, the liquid crystal molecules rotate in accordance with the value of the applied voltage, which results in a change in the polarization of the light that has been linearly polarized by the entrance side polarizer in the liquid crystal lc. The quantity of the light that passes through the polarizer at the light emitting side is thereby adjusted to display a tone.

[0008] While a voltage of about 5 V can be applied to common liquid crystal materials, when an electric field is continuously applied to the liquid crystal lc only in one direction, the liquid crystal material will be degraded. In order to prevent this, the electric field for driving the liquid crystal is applied to the liquid crystal lc with the polarity thereof inverted in a predetermined cycle. In general, a frame inversion driving is used in which the polarity is inverted in the cycle of display frames.

[0009] A separate pixel electrode Pe is provided for each pixel, and a single electrode is provided as the common electrode Ce such that it will be shared by all pixels. A driving method as shown in Fig. 8 is used to achieve the frame inversion driving with utilizing such common electrode Ce. Fig. 8 shows time in the horizontal direction and voltages in the vertical direction to indicate a relationship between the gate voltage Vg, the grayscale voltage Vd, and the common voltage Vcom.

[0010] As shown in Fig. 8, the common voltage (the potential at the common electrode) Vcom (= 0 V) is constant. The grayscale voltage Vd that ranges up to $\pm$ 2.5 V of the common voltage Vcom is applied to the data bus line Ld. Fig. 8 shows a state in which the grayscale voltage Vd (data) having an absolute value V0 = 2.5 V is output on the data bus line Ld in each frame fn, the polarity of the voltage being inverted in each frame fn.

[0011] When an n-channel type TFT connected to the gate bus line Lg is to be kept off state, a potential Vg (off) is output which has an absolute value that is smaller than the maximum negative polarity grayscale voltage Vd = -V0 (V) by V1 (absolute value). When the TFT is to be kept on state, a potential Vg (on) is output which has an absolute value that is greater than the maximum positive polarity grayscale voltage Vd = +V0 (V) by V2 (absolute value). That is, a gate pulse having a potential Vg = Vg(on) is output to the gate bus line Lg during a period in which the TFT is made to be on

state. The height of the gate pulse is V1 + 2 × V0 + V2. The voltage V1 must be increased when the off-current is poorly disconnected, and the voltage V2 must be increased when the on-current is small for reasons associated with the property of retaining accumulated charges and the data rewriting speed. Therefore, a driving voltage of about 13 V is normally used such the TFT will be reliably turned on and off regardless of the polarity of the same.

[0012] As thus described, a power supply circuit of 13 V is required to drive the previously-considered TFT LCD in spite of the fact that the maximum grayscale voltage Vd required for writing the pixel electrodes Pe is 2.5 V. The driving voltage of 13 V is applied not only to the gate bus line driving circuit but also to switching elements in the data bus line driving circuit for controlling the flow of signals output to the data bus lines Ld. The maximum driving voltage depends on the liquid crystal material used, and some TFT LCDs require a driving voltage of 16 V or 18 V or more that is higher than the voltage in the present example.

[0013] As thus described, in the previously-considered TFT LCD, the power supply voltage for the gate bus line driving circuit and the data bus line driving circuit for driving the liquid crystal lc at each pixel is very much higher than the voltage band of 5 V applied to the liquid crystal lc. Therefore, the TFT must have a high gate withstand voltage and drain withstand voltage. This results in a need for countermeasures including an increase in the thickness of gate oxide films of the TFT, an increase in the channel length, and an increase in the LDD (lightly doped drain) length. However, such countermeasures result in an increase in fluctuation of a threshold voltage Vth of the TFT and a reduction in the on-current of the TFT. Consequently, a further increase of the driving voltage will be required to achieve proper operations in the presence of a great fluctuation of the threshold Vth, and still further increase of the driving voltage will be required to achieve a required switching speed while suppressing any reduction in the on-current. This only results in a vicious cycle, and no reduction of the driving voltage can be achieved. An increase of the driving voltage is problematic also in that it leads to an increase of power consumption and an increase of electromagnetic interference with environment.

[0014] The recent establishment of low temperature polysilicon manufacturing processes has made it possible to fabricate a FET having a channel region formed from p-Si (polysilicon) on a member having a relatively low melting point such as a glass substrate. It therefore becomes possible to fabricate a TFT substrate integral with peripheral circuits in which various circuits including a gate bus line driving circuit and a data bus line driving circuit are incorporated in peripheral regions of a glass substrate on which pixel TFTs are to be fabricated. FETs of the peripheral circuit sections must be formed with a gate length that is as small as possible to allow an operation at a high speed, and they must inevitably be of a low voltage drive type. Further, balanced circuits that consume low power cannot be obtained unless they are of a low voltage drive type.

[0015] When the pixel TFTs are of a high voltage drive type, a mixture of the low voltage drive type FET's and high voltage drive type TFTs must be formed on a single glass substrate, which results in a problem in that the manufacturing process will become complicated and the manufacturing cost will increase. Therefore, to manufacture a TFT substrate integral with peripheral circuits utilizing a low temperature polysilicon manufacturing process, the driving voltage of the pixel TFTs must be reduced to become as close as possible to the driving voltage of the FET's of the peripheral circuits.

[0016] EP 0915453 discloses an active matrix type liquid crystal display apparatus having a plurality of pixels each having a pixel electrode characterized in that two transistors of different conductivity types are connected to each pixel electrode. US 2001/0050644 discloses similar liquid crystal display apparatus and a driving method therefor. US-A-5436635 and JP 06 266315 A both disclose LCD display devices.

[0017] It is desirable to provide a liquid crystal display in which a driving voltage of pixel TFTs is reduced.

[0018] The present invention is defined by the independent claims, to which reference should now be made. Specific embodiments are defined in the dependent claims.

[0019] Reference will now be made, by way of example to the accompanying drawings, in which:

Fig. 1 is an equivalent circuit diagram of four pixels of a TFT LCD according to a first arrangement;
Fig. 2 shows a relationship between a gate voltage Vg, a grayscale voltage Vd, and a common voltage Vcom during frame inversion driving according to the first arrangement;
Fig. 3 is an equivalent circuit diagram of four pixels of a TFT LCD according to a second arrangement;
Fig. 4 shows a relationship between a gate voltage Vg, a grayscale voltage Vd, and a common voltage Vcom during frame inversion driving according to the second arrangement;
Fig. 5 is an equivalent circuit diagram of four pixels of a TFT LCD according to a third arrangement;
Fig. 6 shows a relationship between a gate voltage Vg, a grayscale voltage Vd, and a common voltage Vcom during frame inversion driving according to the third arrangement;
Fig. 7 is an equivalent circuit diagram of one pixel of a previously-considered TFT LCD; and
Fig. 8 shows a relationship between a gate voltage Vg, a grayscale voltage Vd, and a common voltage Vcom during frame inversion driving in the previously-considered circuitry.

[0020] Liquid crystal displays and methods for driving the same in an arrangement will now be described with reference to Figs. 1 to 6. In a liquid crystal display (TFT LCD) embodying the invention, a liquid crystal capacitance is charged

with a positive charge and a negative charge by separate circuit systems (a positive polarity driving circuit system and a negative polarity driving circuit system), respectively. For this purpose, two TFTs are provided at each pixel; one of the TFTs functions as a switching element for writing grayscale data having the positive polarity; and the other TFT functions as a switching element for writing grayscale data having the negative polarity.

[0021] While voltages having the positive and negative polarities are applied to a pixel electrode by a single common driving circuit in a previously-considered TFT LCD, a positive voltage and a negative voltage are respectively applied by separate driving circuits in an arrangement. Therefore, the amplitude of each of grayscale data voltages applied to the TFT to which a positive voltage is to be applied and the TFT to which a negative voltage, can be reduced to half of the amplitude according to the previously-considered circuitry, which makes it possible to suppress gate pulse voltages applied to gate electrodes of the TFTs.

[0022] TFT LCDs and methods of driving the same will now be specifically described with reference to preferred arrangements. The second and third arrangements embody the present invention.

[First Arrangement]

[0023] A TFT LCD of a first arrangement and a method for driving the same will be described with reference to Figs. 1 and 2. First, a schematic configuration of the TFT LCD of the present arrangement will be described with reference to Fig. 1. Fig. 1 shows an equivalent circuit of four pixels P11, P12, P21, and P22 adjacent to each other among a plurality of pixels Pmn provided in the form of a matrix on an insulated substrate. At the pixels Pmn, liquid crystal capacitances Clcmn are formed by sandwiching a liquid crystal lc between pixel electrodes Pe on a TFT substrate and a common electrode Ce on an opposite substrate. A common voltage (common electrode potential) Vcom (= 0 V) is applied to the common electrode Ce.

[0024] In peripheral regions of the substrate adjacent to the region where the pixels are formed, peripheral circuits are formed integrally with the region where the pixels are formed using a low temperature polysilicon manufacturing process, for example. Referring to some of the peripheral circuits, there are formed a gate bus line driving circuit GD1 for positive polarity driving, a gate bus line driving circuit GD2 for negative polarity driving, a data bus line driving circuit DD1 for positive polarity driving, and a data bus line driving circuit DD2 for negative polarity driving.

[0025] Gate bus lines Lg 11, Lg21, Lg31, ... for applying a positive voltage extending in the horizontal direction of the figure are connected to the gate bus line driving circuit GD1 for positive polarity driving. Gate bus lines Lg 12, Lg22, Lg32, ... for applying a negative voltage that adjoin the gate bus lines Lg11, Lg21, Lg31, ... for applying a positive voltage, respectively, and extend in parallel with them are connected to the gate bus line driving circuit GD2 for negative polarity driving.

[0026] Data bus lines Ld 11, Ld21, Ld31, ... for applying a positive voltage extending in the vertical direction of the figure are connected to the data bus line driving circuit DD1 for positive polarity driving. Data bus lines Ld 12, Ld22, ... for applying a negative voltage that adjoin the data bus lines Ld11, Ld21, Ld31, ... for applying a positive voltage, respectively, and extend in parallel with them are connected to the data bus line driving circuit DD2 for negative polarity driving.

[0027] A positive polarity driving circuit system is formed by the gate bus line driving circuit GD1 for positive polarity driving, the gate bus lines Lg11, Lg21, Lg31, ... for applying a positive voltage, the data bus line driving circuit DD1 for positive polarity driving, and the data bus lines Ld11, Ld21, Ld31, ... for applying a positive voltage. The positive polarity driving circuit system is used for charging the liquid crystal capacitances Clcmn with a positive charge by applying a positive voltage between the electrodes Pe of the pixels Pmn and the electrode Ce.

[0028] A negative polarity driving circuit system is formed by the gate bus line driving circuit GD2 for negative polarity driving, the gate bus lines Lg12, Lg22, Lg32, ... for applying a negative voltage, the data bus line driving circuit DD2 for negative polarity driving, and the data bus lines Ld12, Ld22, ... for applying a negative voltage. The negative polarity driving circuit system is used for charging the liquid crystal capacitances Clcmn with a negative charge by applying a negative voltage between the electrodes Pe of the pixels Pmn and the electrode Ce.

[0029] Referring to the pixel P11 by way of example, the pixel P11 is formed with two thin film transistors, i.e., an n-channel TFT n11 as a positive-voltage-applying TFT for applying a data voltage having the positive polarity to the pixel electrode Pe and a p-channel TFT p11 as a negative-voltage-applying TFT for applying a data voltage having the negative polarity to the pixel electrode Pe.

[0030] A source electrode S of the TFT n11 is connected to the pixel electrode Pe; a drain electrode D of the same is connected to the data bus line Ld11 for applying the positive voltage; and a gate electrode G of the same is connected to the gate bus line Lg11 for applying the positive voltage.

[0031] A source electrode S of the TFT p11 is also connected to the pixel electrode Pe; a drain electrode D of the same is connected to the data bus line Ld12 for applying the negative voltage; and a gate electrode G of the same is connected to the gate bus line Lg11 for applying the negative voltage. The rest of the pixels Pmn have the same configuration. Storage capacitors Csmn are connected in parallel with the liquid crystal capacitances Clcmn in practice,

although not shown.

[0032] In the above configuration, when a gate pulse Vg11 (on) for applying the positive voltage is output to the gate bus line Lg11 for applying the positive voltage from the gate bus line driving circuit GD1 for positive polarity driving in a display frame f(2n) (n is a positive integer), TFT n11 and TFT n12, ... whose gate electrodes G are connected to the gate bus line Lg11 for applying the positive voltage are turned on. As a result, grayscale voltages Vd11, Vd21, Vd31, ... output to the data bus lines Ld11, Ld21, Ld31, ..., respectively, from the data bus line driving circuit DD1 for positive polarity driving are written in the pixel electrodes Pe of respective pixels P1n through TFT n1n. When the above operation is performed on all of the gate bus lines Lgm1 for positive polarity driving on the basis of line sequential driving, the writing of grayscale voltages for one frame period is completed.

[0033] When a gate pulse Vg12 (on) for applying the negative voltage is then output to the gate bus line Lg12 for applying the negative voltage from the gate bus line driving circuit GD2 for negative polarity driving in the next display frame f (2n+1), TFTs p11, p12, ... whose gate electrodes G are connected to the gate bus line Lg12 for applying the negative voltage are turned on. As a result, grayscale voltages Vd12, Vd22, ... output to the data bus lines Ld12, Ld22, ... respectively, from the data bus line driving circuit DD2 for negative polarity driving are written in the pixel electrodes Pe of respective pixels P1n through TFTs p1n. When the above operation is performed on all of gate bus lines Lgm2 for negative polarity driving on the basis of line sequential driving, the writing of grayscale voltages for one frame period is completed.

[0034] The display frames f (2n) and f (2n+1) are sequentially and repeatedly driven to perform frame inversion driving.

[0035] A detailed description will now be made based on Fig. 2 and with reference to Fig. 1 on optimum levels (voltages) of gate pulses Vgm1 (on) for applying the positive voltage and gate pulses Vgm2 (on) for applying the negative voltage. In Fig. 2, a time base t is plotted in the horizontal direction and voltage levels are plotted in the vertical direction to indicate a relationship between a gate voltage Vg, a grayscale voltage Vd, and a common voltage Vcom. In Fig. 2, voltage levels of the positive polarity driving circuit system relative to the time base t are shown above the time base t, and voltage levels of the negative polarity driving circuit system relative to the time base t are shown under the time base t. For simplicity of description, Fig. 2 shows the gate pulse Vg11 (on) for applying the positive voltage and the gate pulse Vg12 (on) for applying the negative voltage that are respectively applied to the gate electrodes G of the TFTs n11 and p11 of the pixel P11.

[0036] The common voltage (common electrode potential) Vcom (= 0 V) is constant. In the present arrangement, a maximum positive grayscale voltage Vd11max is +2.5 V, and a maximum negative grayscale voltage Vd12max is -2.5V. A threshold voltage Vthn of the TFT n11 is Vth0 (a typical threshold voltage) $\pm\Delta$, and a threshold voltage Vthp of the TFT p11 is -Vth0 $\pm\Delta$. Let us assume that the typical threshold voltage Vth0 is 3 V and that the fluctuation Δ is 1 V. It is also assumed that VL represents a potential at the pixel electrodes Pe of the TFTs n11 and p11 (see Fig. 1).

[0037] First, the frame inversion driving shown in Fig. 2 will be schematically described. As shown in Fig. 2, a positive grayscale voltage Vd11 (data) is applied to the pixel electrode Pe of the pixel P11 in even-numbered frames f2 and f4, and a negative grayscale voltage Vd12 (data) is applied to the same in odd-numbered frames f1 and f3.

[0038] The magnitude of the gate pulse Vg11 (on) for applying the positive voltage and the gate pulse Vg12 (on) for applying the negative voltage is obtained as V0 + V1 + V2 where the maximum grayscale voltages have an absolute value V0 = 2.5 V and where the gate pulses have an absolute voltage V1 and an absolute voltage V2 as shown in Fig. 2.

[0039] In other words, in order to keep the TFT n11 off, the potential at the gate electrode G of the TFT n11 must be kept lower than a minimum positive grayscale voltage Vd11min = Vcom = 0 V by V1 (absolute value). In order to keep the TFT n11 on, the potential at the gate electrode G of the TFT n11 must be kept higher than the maximum positive grayscale voltage Vd11max V0 = 2.5 V by V2 (absolute value).

[0040] In order to keep the TFT p11 off, the potential at the gate electrode G of the TFT p11 must be kept higher than a minimum negative grayscale voltage Vd12min = Vcom = 0 V by V1 (absolute value). In order to keep the TFT p11 on, the potential at the gate electrode G of the TFT p11 must be kept lower than the maximum negative grayscale voltage Vd12max = -V0 = -2.5 V by V2 (absolute value).

[0041] A description will be first made on the gate pulse Vg11 (on) for applying the positive voltage that is applied to the gate electrode G of the TFT n11 which is an n-channel FET by the positive polarity driving circuit system shown above the time base t in Fig. 2.

[0042] In order for the TFT n11 to be kept off, a potential difference between either voltage Vd11 output to the data bus line Ld11 for applying the positive voltage or voltage VL at the pixel electrode Pe, whichever lower, and the voltage Vg11 output to the gate bus line Lg11 for applying the positive voltage must be smaller than the threshold voltage Vthn of the TFT n11 that is equal to Vth0 $\pm\Delta$. At a point in time t1 in Fig. 2 when the voltage VL at the pixel electrode Pe is -2.5 V, the TFT n11 must be off.

[0043] Specifically,

$$Vg11 - Min(Vd11, VL) < Vth0 - \Delta \qquad \text{Equation 1}$$

Since Vg11 = -V1; Min(Vd11, VL) = -2.5; and Vth0 - Δ = 2, Equation 1 can be rearranged as follows by substituting those values in the same.

$$V1 > 0.5$$

[0044] At a point in time t2 when the voltage VL at the pixel electrode Pe is -2.5 V, the TFT n11 must be off. Therefore, Equation 1 is used just as done at the point in time t1.

$$Vg11 - Min(Vd11, VL) < Vth0 - \Delta \qquad \text{Equation 1}$$

Since Vg11 = -V1; Min(Vd11, VL) = -2.5; and Vth0 - Δ = 2, Equation 1 can be rearranged as follows by substituting those values in the same.

$$V1 > 0.5$$

[0045] At a point in time t3, the grayscale voltage Vd11 = Vd11 (data) = 2.5 V. While the voltage VL at the pixel electrode Pe is -2.5 V at the instance when the TFT n11 is turned on, the voltage VL at the pixel electrode Pe = Vd11 (data) = 2.5 V immediately after the grayscale voltage Vd11 (data) is written in the pixel electrode Pe. The TFT n11 must be kept on until the writing is completed.

[0046] Specifically,

$$Vg11 - Min(Vd11, VL) > Vth0 + \Delta \qquad \text{Equation 2}$$

Since Vg11 = V0 + V2 = 2.5 + V2; Min(Vd11, VL) = 2.5; and Vth0 + Δ = 4, Equation 2 can be rearranged as follows by substituting those values in the same.

$$V2 > 4$$

[0047] At a point in time t4 when the voltage VL at the pixel electrode Pe is 2.5 V, the TFT n11 must be off. Therefore, Equation 1 is used just as done at the point in time t1.

$$Vg11 - Min(Vd11, VL) < Vth0 - \Delta \qquad \text{Equation 1}$$

Since Vg11 = -V1; Min (Vd11, VL) = 2.5; and Vth0 - Δ = 2, Equation 1 can be rearranged as follows by substituting those values in the same.

$$V1 > -4.5$$

[0048] At a point in time t5 when the voltage VL at the pixel electrode Pe is 2.5 V and the voltage Vg11 is 0 V, the TFT n11 must be off.

Since Vg11 = -V1; Min(Vd11, VL) = 0; and Vth0 - Δ = 2, Vg11 - Min(Vd11, VL) = -V1 < 0

[0049] The state at a point in time t6 is the same as that at the point in time t1.

[0050] Therefore, what is required for the gate pulse Vgm1 (on) for applying the positive voltage to be applied to the n-channel TFT n11 is to satisfy relationships expressed by V1 > 0.5 and V2 > 4. What is required for the gate pulse Vgm2 (on) for applying the negative voltage to be applied to the p-channel TFT p11 is to satisfy relationships expressed

by V1 > 0.5 and V2 > 4 because the above discussion is absolutely true except that the polarity is inverted.

[0051] Thus, the gate pulse Vg11 (on) for applying the positive voltage and the gate pulse Vg12 (on) for applying the negative voltage have a minimum voltage amplitude of V0 + V1 + V2 = 2.5 + 0.5 + 4 = 7 V where the threshold voltage Vth0 = 3 V and the fluctuation Δ is 1 V. That is, a power supply voltage of 7 V may be used for both of the positive polarity driving circuit system and the negative polarity driving circuit system.

[0052] As thus described, in the present arrangement, the power supply voltage for the gate bus line driving circuit and the data bus line driving circuit for driving the liquid crystal lc at each pixel can be significantly smaller than that in the related art. It is therefore possible to use TFTs having a relatively low gate withstand voltage and drain withstand voltage as elements for switching pixels. This consequently makes it possible to reduce the thickness of gate oxide films of pixel TFTs, to reduce the channel length thereof, and to reduce the LDD length thereof. Thus, fluctuation of a threshold voltage Vth of TFTs can be reduced, and any reduction in the on-current of TFTs can be suppressed. Further, the reduction of a driving voltage makes it possible to reduce power consumption and to reduce electromagnetic interference with environment.

[0053] When a TFT substrate integral with peripheral circuits is fabricated using a low temperature polysilicon manufacturing process, the peripheral circuit sections can be formed using low voltage drive type FETs, which makes it possible to provide peripheral circuits which are capable of high speed operations, which consume less power, and which are well-balanced.

[0054] Further, since pixel TFTs can be of the low voltage drive type, there is no need for forming a mixture of low voltage drive type FETs and high voltage drive type TFTs on a single glass substrate, which makes it possible to simplify manufacturing processes and to reduce manufacturing costs.

[Second Arrangement]

[0055] A TFT LCD of a second arrangement and a method for driving the same will be described with reference to Figs. 3 and 4. Fig. 3 is an equivalent circuit similar to Fig. 1 for the first arrangement, and it shows a schematic configuration of the TFT LCD of the present arrangement. The TFT LCD of the present arrangement has the same configuration as that of the first arrangement except that the p-channel TFTs pmn of the TFT LCD of the first arrangement are replaced by n-channel TFTs n' mn. Elements that function and operate in a manner similar to that in the first arrangement are indicated by like reference numerals and will not be described.

[0056] Referring to a pixel P11 by way of example, the pixel P11 is formed with two thin film transistors, i.e., an n-channel TFT n11 as a positive-voltage-applying TFT for applying a data voltage having the positive polarity to a pixel electrode Pe and an n-channel TFT n'11 as a negative-voltage-applying TFT for applying a data voltage having the negative polarity to the pixel electrode Pe.

[0057] A source electrode S of the TFT n11 is connected to the pixel electrode Pe; a drain electrode D of the same is connected to a data bus line Ld11 for applying a positive voltage; and a gate electrode G of the same is connected to a gate bus line Lg11 for applying the positive voltage.

[0058] A drain electrode D of the TFT n'11 is connected to the pixel electrode Pe; a source electrode S of the same is connected to a data bus line Ld12 for applying a negative voltage; and a gate electrode G of the same is connected to a gate bus line Lg11 for applying the negative voltage. The rest of the pixels Pmn have the same configuration.

[0059] A detailed description will now be made based on Fig. 4 and with reference to Fig. 3 on optimum levels (voltages) of gate pulses Vgm1 (on) for applying the positive voltage and gate pulses Vgm2 (on) for applying the negative voltage. Fig. 4 indicates a relationship between a gate voltage Vg, a grayscale voltage Vd, and a common voltage Vcom during frame inversion driving of the TFT LCD of the present arrangement under the same conditions as those shown in Fig. 2 for the first arrangement.

[0060] Since the description of the TFT n11 in the first arrangement absolutely applies to the magnitude of a gate pulse Vg11 (on) for applying the positive voltage to be applied to the gate electrode G of the TFT n11 by a positive polarity driving circuit system shown above a time base t in Fig. 4, it is only required that relationships expressed by V1 = 0.5 and V2 = 4 are satisfied. Therefore, a minimum voltage amplitude of the positive polarity driving circuit system is 0.5 + 4 + 2.5 = 7 V.

[0061] A description will now be made on a gate pulse Vg12 (on) for applying the negative voltage to be applied to the gate electrode G of the TFT n' 11 that is an n-channel FET by a negative polarity driving circuit system shown under the time base t in Fig. 4.

[0062] At a point in time t1 in Fig. 4 when a voltage VL at the pixel electrode Pe is -2.5 V, the TFT n'11 must be off.

[0063] Specifically,

$$Vg12 - Min(Vd12, VL) < Vth0 - \Delta \qquad \text{Equation 3}$$

Since Vg12 = -2.5 + V1; Min(Vd12, VL) = -2.5; and Vth0 - Δ = 2, Equation 3 can be rearranged as follows by substituting those values in the same.

$$V1 < 2$$

[0064] At a point in time t2 when the voltage VL at the pixel electrode Pe is -2.5 V, the TFT n'11 must be off. Equation 3 is used just as done at the point in time t1.

$$Vg12 - Min(Vd12, VL) < Vth0 - \Delta \qquad \text{Equation 3}$$

Since Vg12 = -2.5 + V1; Min(Vd12, VL) = -2.5; and Vth0 - Δ = 2, Equation 3 can be rearranged as follows by substituting those values in the same.

$$V1 < 2$$

[0065] At a point in time t3, a positive grayscale voltage Vd11 = Vd11 (data) = 2.5 V is written in the pixel electrode Pe. At this time, a grayscale voltage Vd12 = 0 V. While the voltage VL at the pixel electrode Pe is -2.5 V at the instance when the TFT n11 on the positive polarity side is turned on, the voltage VL at the pixel electrode Pe = Vd11 (data) equals 2.5 V immediately after the grayscale voltage Vd11 (data) is written in the pixel electrode Pe. At this time, the TFT n' 11 on the negative polarity side must be kept off until the writing is completed.

[0066] Specifically,

$$Vg12 - Min(Vd12, VL) < Vth0 + \Delta \qquad \text{Equation 3}$$

Since Vg12 = -V0 + V1 = -2.5 + V1; Min(Vd12, VL) = 0; and Vth0 - Δ = 2, Equation 3 can be rearranged as follows by substituting those values in the same.

$$V1 < 4.5$$

[0067] At a point in time t4 when the voltage VL at the pixel electrode Pe is 2.5 V, the TFT n'11 must be off. Therefore, Equation 3 is used just as done at the point in time t1.

$$Vg12 - Min(Vd12, VL) < Vth0 - \Delta \qquad \text{Equation 3}$$

Since Vg12 = -2.5 + V1; Min (Vd12, VL) = 0; and Vth0 - Δ = 2, Equation 3 can be rearranged as follows by substituting those values in the same.

$$V1 < 0.5$$

[0068] At a point in time t5 when the voltage VL at the pixel electrode Pe is 2.5 V and the voltage Vg12 is 0 V, the TFT n' 11 must be off.

$$Vg12 - Min(Vd12, VL) < Vth0 - \Delta \qquad \text{Equation 3}$$

Since Vg12 = -2.5 + V1; Min(Vd12, VL) = -2.5; and Vth0 - Δ = 2, Equation 3 can be rearranged as follows by substituting those values in the same.

$$V1 < 2$$

[0069] At a point in time t6, the grayscale voltage Vd12 = Vd12 (data) = -2.5 V. While the voltage VL at the pixel electrode Pe is 2.5 V at the instance when the TFT n' 11 is turned on, the voltage VL at the pixel electrode Pe = Vd12 (data) = -2.5 V immediately after the maximum grayscale voltage Vd12 (data) is written in the pixel electrode Pe. The TFT n' 11 must be kept on until the writing is completed.

[0070] Specifically,

$$Vg12 - Min(Vd12, VL) > Vth0 + \Delta \qquad \text{Equation 4}$$

Since Vg12 = V2; Min(Vd12, VL) = -2.5; and Vth0 + Δ = 4, Equation 4 can be rearranged as follows by substituting those values in the same.

$$V2 > 1.5$$

[0071] Therefore, what is required for the gate pulse Vgm2 (on) for applying the negative voltage to be applied to the n-channel TFT n' 11 on the negative polarity side is to satisfy relationships expressed by V1 < 2 and V2 > 1.5.

[0072] Thus, the gate pulse Vg11 (on) for applying the positive voltage has a minimum voltage amplitude of V0 + V1 + V2 = 2.5 + 0.5 + 4 = 7 V, and the gate pulse Vg12 (on) for applying the negative voltage has a minimum voltage amplitude of V0 + V1(= 0) + V2 = 2.5 + 1.5 = 4V where the threshold voltage Vth0 = 3 V and the fluctuation Δ is 1 V. That is, a power supply voltage of 7 V may be used for both of the positive polarity driving circuit system and the negative polarity driving circuit system.

[0073] In general, when the off-current of the TFT is poorly discontinued, the voltage V1 of the TFT nmn on the positive polarity side is increased, and the voltage V1 of the TFT n' mn on the negative polarity side is reduced. When the on-current is small, the voltage V2 of both of the positive TFT nmn and negative TFT n' mn must increased for reasons associated with the property of retaining accumulated charges and the data writing speed. On the contrary, in the present arrangement, since a low driving voltage can be used, the gate oxide films of the TFTs can be made thin, which makes it possible to improve the above-mentioned characteristics of interest. It is therefore possible to minimize the voltages V1 and V2, which consequently allows a further reduction of the power supply voltage.

[Third Arrangement]

[0074] A TFT LCD of a third arrangement and a method for driving the same will be described with reference to Figs. 5 and 6. Fig. 5 is an equivalent circuit similar to Figs. 1 and 3 for the first and second arrangements, and it shows a schematic configuration of the TFT LCD of the present arrangement. The TFT LCD of the present arrangement has the same configuration as that of the second arrangement except that the n-channel TFT nmn and TFT n'mn for the positive and negative polarities of the TFT LCD of the second arrangement are replaced by p-channel TFT pmn and TFT p' mn, respectively. Elements that function and operate in a manner similar to those in the second arrangement are indicated by like reference numerals and will not be described.

[0075] Referring to a pixel P11 by way of example, the pixel P11 is formed with two thin film transistors, i.e., a p-channel TFT p11 as a positive-voltage-applying TFT for applying a data voltage having the positive polarity to a pixel electrode Pe and a p-channel TFT p' 11 as a negative-voltage-applying TFT for applying a data voltage having the negative polarity to the pixel electrode Pe.

[0076] A drain electrode D of the TFT p11 is connected to the pixel electrode Pe, and a source electrode S of the same is connected to a data bus line Ld11 for applying a positive voltage, and a gate electrode G thereof is connected to a gate bus line Lg11 for applying the positive voltage.

[0077] A drain electrode D of the TFT p' 11 is connected to a data bus line Ld12 for applying a negative voltage; a source electrode S of the same is connected to the pixel electrode Pe; and a gate electrode G of the same is connected to the gate bus line Lg11 for applying the negative voltage. The rest of the pixels Pmn have the same configuration.

[0078] Fig. 6 illustrates optimum levels (voltages) of gate pulses Vgm1 (on) for applying the positive voltage and gate pulses Vgm2 (on) for applying the negative voltage in the present arrangement. Fig. 6 indicates a relationship between a gate voltage Vg, a grayscale voltage Vd, and a common voltage Vcom during frame inversion driving of the TFT LCD of the present arrangement under the same conditions as those shown in Fig. 4 for the second arrangement.

[0079] The description of the TFT n11 in the second arrangement absolutely applies to the magnitude of a gate pulse Vg11 (on) for applying the positive voltage to be applied to the gate electrode G of the TFT p11 by a positive polarity driving circuit system shown above a time base t in Fig. 6 except that the polarity is inverted. The description of the TFT

n'11 in the second arrangement absolutely applies to the magnitude of a gate pulse Vg12 (on) for applying the negative voltage to be applied to the gate electrode G of the TFT p' 11 by a negative polarity driving circuit system shown under the time base t in Fig. 6 except that the polarity is inverted.

[0080] It will be apparent from the above that a power supply voltage of 7 V can be used for both of the positive polarity driving circuit system and the negative polarity driving system where a threshold voltage Vth0 = 3 V and fluctuation Δ = 1V. The same effects as in the Arrangement 2 can be achieved.

[0081] As described above, in such an arrangement, since the pulse height of a gate pulse output from a gate bus line driving circuit for driving pixels of an active matrix type LCD can be reduced, a low power supply voltage can be used for the gate bus line driving circuit. Since this makes it possible to use a low power supply voltage for the data bus line driving circuit, a reduction in power consumption can be achieved. Further, the low power supply voltage makes it possible to use a gate oxide film having a smaller thickness, which allows a transistor to operate at a high speed (i.e., to have high transconductance) with less fluctuation of a threshold voltage Vth. The reduction of the fluctuation of the threshold voltage Vth allows a further reduction of the driving voltage. Further, a voltage applied between a drain and a source is also reduced, which makes it possible to form a TFT with a transistor structure that requires a small withstand voltage between the drain and source and that is easily to fabricate.

[0082] Since a pixel structure in such an arrangement results in the increase in the quantities of transistors and wirings per pixel, attention must be paid to a reduction of the aperture ratio. However, the reduction of the aperture ratio can be suppressed by employing a fine wiring pattern. In the case of a reflection type LCD in which a conductive and highly reflective metal such as aluminum is used for pixel electrodes Pe, no reduction of the aperture ratio will occur because the TFTs and bus lines are located on the backside of the pixel electrodes Pe.

[0083] Although a TFT LCD embodying the present invention has a duplex driving circuit for each bus line, any increase in manufacturing cost attributable to the duplex driving circuit for each bus line can be prevented in a configuration integral with peripheral circuits provided using a low temperature polysilicon manufacturing process because each bus line driving circuit can be formed on a glass substrate simultaneously with a pixel region.

[0084] The invention is not limited to the above-described second and third arrangements and may be modified in various ways within the scope of the claims.

[0085] For example, while an arrangement has been described with reference to transmission type LCDs, the invention is not limited to them and may be applied to reflection type LCDs and semi-transmission type LCDs.

[0086] While an arrangement has been described with reference to TFTs utilizing p-Si as an active semiconductor layer, the invention is not limited to them and may be applied to TFTs utilizing a-Si (amorphous silicon) as an active semiconductor layer.

[0087] While an arrangement has been described with reference to LCDs integral with peripheral circuits provided by using a low temperature polysilicon manufacturing process, the invention is not limited to them. The invention may be applied to LCDs in which some or all of peripheral circuits are formed separately from a glass substrate on which pixel TFTs are formed and are wired using TAB mounting or COG mounting.

[0088] As described above, such arrangements make it possible to reduce a driving voltage of a pixel TFT.

Claims

1. A liquid crystal display comprising:

a liquid crystal capacitance (Clc11) formed by sandwiching a liquid crystal between a pixel electrode (Pe) and a common electrode (Ce) facing the pixel electrode;
a positive-voltage-applying TFT (TFTn11) for applying a voltage having a positive polarity to the pixel electrode (Pe) so as to charge the liquid crystal capacitance with a positive charge;
a negative-voltage-applying TFT (TFTp11) for applying a voltage having a negative polarity to the pixel electrode (Pe) so as to charge the liquid crystal capacitance with a negative charge;
a positive polarity driving circuit system operable to generate a positive-voltage-applying gate pulse and to transmit that pulse to a gate electrode (G) of the positive-voltage-applying TFT; and
a negative polarity driving circuit system operable to generate a negative-voltage-applying gate pulse and to transmit that pulse to a gate electrode (G) of the negative-voltage-applying TFT,
wherein:

the circuitry in the positive polarity driving circuit system (GD1 & Lg11) which generates and transmits said positive-voltage-applying gate pulse is provided separately from the circuitry in the negative polarity driving circuit system (GD2 & Lg12) which generates and transmits said negative-voltage-applying gate pulse,

characterised in that:

a conductivity type of channels of the positive-voltage-applying TFT and the negative-voltage-applying TFT is the same; and
said positive-voltage-applying gate pulse has a voltage higher than a voltage of said negative-voltage-applying gate pulse.

2. A liquid crystal display according to claim 1, comprising a plurality of pixels, each said pixel comprising such a liquid crystal capacitance (Clc11, Clc12, Clc21, Clc22) having such a pixel electrode (Pe) and also having such a common electrode (Ce) to which a common voltage is applied when the display is in use.

3. A liquid crystal display according to claim 2, wherein the pixels each have:

such a positive-voltage-applying TFT (TFTn11, TFTn12, TFTn21, TFTn22) for applying a voltage having the positive polarity to the pixel electrode (Pe) of the pixel concerned; and
such a negative-voltage-applying TFT (TFTp11, TFTp12, TFTp21, TFTp22) for applying a voltage having the negative polarity to the said pixel electrode (Pe) of the pixel concerned.

4. A liquid crystal display according to claim 3, wherein the positive polarity driving circuit system has:

a positive-voltage-applying gate bus line (Lg11, Lg21, Lg31) for outputting the positive-voltage-applying gate pulse to the gate electrode (G) of the positive-voltage-applying TFT of at least one of the pixels; and
a positive-voltage-applying data bus line (Ld11, Ld21, Ld22) for outputting a data voltage having the positive polarity to a source (S) or drain (D) electrode of the positive-voltage-applying TFT of the said at least one of the pixels;
wherein the negative polarity driving circuit system has:

a negative-voltage-applying gate bus line (Lg12, Lg22, Lg32) for outputting the negative-voltage-applying gate pulse to the gate electrode (G) of the negative-voltage-applying TFT of the said at least one of the pixels; and
a negative-voltage-applying data bus line (Ld12, Ld22) for outputting a data voltage having the negative polarity to a source (S) or drain (D) electrode of the negative-voltage-applying TFT of the said at least one of the pixels.

5. A liquid crystal display according to claim 4, wherein the positive polarity driving circuit system has:

a gate bus line driving circuit (GD1) for positive polarity driving for outputting the positive-voltage-applying gate pulse to the positive-voltage-applying gate bus line; and
a data bus line driving circuit (DD1) for positive polarity driving for outputting the data voltage having the positive polarity to the positive-voltage-applying data bus line;
wherein the negative polarity driving circuit system has:

a gate bus line driving circuit (GD2) for negative polarity driving for outputting the negative-voltage-applying gate pulse to the negative-voltage-applying gate bus line; and
a data bus line driving circuit (DD2) for negative polarity driving for outputting the data voltage having the negative polarity to the negative-voltage-applying data bus line.

6. A liquid crystal display according to claim 4 or 5, wherein each said positive-voltage-applying TFT and each said negative-voltage-applying TFT is an n-type TFT.

7. A liquid crystal display according to claim 4 or 5, wherein each said positive-voltage-applying TFT and each said negative-voltage-applying TFT is a p-type TFT.

8. A liquid crystal display according to any preceding claim, wherein the positive polarity driving circuit system and the negative polarity driving circuit system are integrally formed on an insulated substrate on which either of the electrodes is formed.

9. A method of driving a liquid crystal display , the display having a liquid crystal capacitance (Clc11) formed by

sandwiching a liquid crystal between a pixel electrode (Pe) and a common electrode (Ce) facing the pixel electrode, a positive-voltage-applying TFT (TFTn11) for applying a voltage having a positive polarity to the pixel electrode (Pe) so as to charge the liquid crystal capacitance with a positive charge, and a negative-voltage-applying TFT (TFTp11) for applying a voltage having a negative polarity to the pixel electrode (Pe) so as to charge the liquid crystal capacitance with a negative charge, the method comprising:

employing a positive polarity driving circuit system to generate a positive-voltage-applying gate pulse and to transmit that pulse to the gate electrode (G) of the positive-voltage-applying TFT; and
employing a negative polarity driving circuit system to generate a negative-voltage-applying gate pulse and to transmit that pulse to the gate electrode (G) of the negative-voltage-applying TFT,
wherein:

the circuitry in the positive polarity driving circuit system (GD1 & Lg11) which is employed to generate and transmit said positive-voltage-applying gate pulse is provided separately from the circuitry in the negative polarity driving circuit system (GD2 & Lg12) which is employed to generate and transmit said negative-voltage-applying gate pulse,

characterised in that:

a conductivity type of channels of the positive-voltage-applying TFT and the negative-voltage-applying TFT is the same; and
said positive-voltage-applying gate pulse has a voltage higher than a voltage of said negative-voltage-applying gate pulse.

Patentansprüche

1. Flüssigkristallanzeige, mit:

einer Flüssigkristallkapazität (Clc11), die durch das Einschichten eines Flüssigkristalls zwischen eine Pixelelektrode (Pe) und eine gemeinsame Elektrode (Ce), die der Pixelelektrode gegenüberliegt, gebildet ist;
einem eine positive Spannung liefernden TFT (TFTn11) zum Anlegen einer Spannung mit einer positiven Polarität an die Pixelelektrode (Pe), um die Flüssigkristallkapazität mit einer positiven Ladung aufzuladen;
einem eine negative Spannung liefernden TFT (TFTp11) zum Anlegen einer Spannung mit einer negativen Polarität an die Pixelelektrode (Pe), um die Flüssigkristallkapazität mit einer negativen Ladung aufzuladen;
einem Treiberschaltungssystem mit positiver Polarität, das betreibbar ist, einen eine positive Spannung liefernden Gate-Impuls zu erzeugen und diesen Impuls an eine Gate-Elektrode (G) des eine positive Spannung liefernden TFTs zu übermitteln; und
einem Treiberschaltungssystem mit negativer Polarität, das betreibbar ist, einen eine negative Spannung liefernden Gate-Impuls zu erzeugen und diesen Impuls an eine Gate-Elektrode (G) des eine negative Spannung liefernden TFTs zu übermitteln;
wobei:

die Schaltungsanordnung in dem Treiberschaltungssystem mit positiver Polarität (GD1 & Lg11), die den eine positive Spannung liefernden Gate-Impuls erzeugt und übermittelt, getrennt von der Schaltungsanordnung in dem Treiberschaltungssystem mit negativer Polarität (GD2 und Lg12), die den eine negative Spannung liefernden Gate-Impuls erzeugt und übermittelt, angeordnet ist,

dadurch gekennzeichnet, dass
ein Leitfähigkeitstyp von Kanälen des eine positive Spannung liefernden TFTs und des eine negative Spannung liefernden TFTs gleich ist; und
der eine positive Spannung liefernde Gate-Impuls eine höhere Spannung als der eine negative Spannung liefernde Gate-Impuls aufweist.

2. Flüssigkristallanzeige nach Anspruch 1, die mehrere Pixel enthält, wobei jedes Pixel eine solche Flüssigkristallkapazität (Clc11, Clc12, Clc21, Clc22) enthält, die eine solche Pixelelektrode (Pe) besitzt und die auch eine solche gemeinsame Elektrode (Ce), an die eine gemeinsame Spannung angelegt wird, wenn die Anzeige im Einsatz ist, besitzt.

3. Flüssigkristallanzeige nach Anspruch 2, wobei jedes der Pixel besitzt:

einen solchen eine positive Spannung liefernden TFT (TFTn11, TFTn12, TFTs21, TFTn22) zum Anlegen einer Spannung mit einer positiven Polarität an die Pixelelektrode (Pe) des entsprechenden Pixels; und
einen solchen eine negative Spannung liefernden TFT (TFTp11, TFTp12, TFTp21, TFTp22) zum Anlegen einer Spannung mit einer negativen Polarität an die Pixelelektrode (Pe) des entsprechenden Pixels.

4. Flüssigkristallanzeige nach Anspruch 3, wobei das Treiberschaltungssystem mit positiver Polarität aufweist:

eine eine positive Spannung liefernde Gate-Busleitung (Lg11, Lg21, Lg31), um den eine positive Spannung liefernden Gate-Impuls zu der Gate-Elektrode (G) des eine positive Spannung liefernden TFTs von mindestens einem Pixel auszugeben; und
eine eine positive Spannung liefernde Datenbusleitung (Ld11, Ld21, LD31), um eine Datenspannung, die eine positive Polarität aufweist, an eine Source- (S-) oder eine Drain- (D-) Elektrode des eine positive Spannung liefernden TFTs des mindestens einen Pixels auszugeben;
wobei das Treiberschaltungssystem mit negativer Polarität aufweist:

eine eine negative Spannung liefernde Gate-Busleitung (Lg12, Lg22, Lg32), um den eine negative Spannung liefernden Gate-Impuls an die Gate-Elektrode (G) des eine negative Spannung liefernden TFTs von mindestens einem Pixel auszugeben; und
eine eine negative Spannung liefernde Datenbusleitung (Ld12, Ld22), um eine Datenspannung, die eine negative Polarität aufweist, an eine Source- (S-) oder eine Drain- (D-) Elektrode des eine negative Spannung liefernden TFTs des mindestens einen Pixels auszugeben.

5. Flüssigkristallanzeige nach Anspruch 4, wobei das Treiberschaltungssystem mit positiver Polarität aufweist:

eine Gate-Busleitungs-Treiberschaltung (GD1) zum Ansteuern mit einer positiven Polarität, um den eine positive Spannung liefernden Gate-Impuls an die eine positive Spannung liefernde Gatebusleitung auszugeben; und
eine Datenbusleitungs-Treiberschaltung (DD1) zum Ansteuern mit einer positiven Polarität, um die Datenspannung mit einer positiven Polarität an die eine positive Spannung liefernde Datenbusleitung auszugeben;
wobei das Treiberschaltungssystem mit negativer Polarität aufweist:

eine Gate-Busleitungs-Treiberschaltung (GD1) zum Ansteuern mit einer negativen Polarität, um den eine negative Spannung liefernden Gate-Impuls an die eine negative Spannung liefernde Gatebusleitung auszugeben; und
eine Datenbusleitungs-Treiberschaltung (DD2) zum Ansteuern mit einer negativen Polarität, um die Datenspannung, die eine negative Polarität aufweist, an die eine negative Spannung liefernde Datenbusleitung auszugeben.

6. Flüssigkristallanzeige nach Anspruch 4 oder 5, wobei jeder eine positive Spannung liefernder TFT und jeder eine negative Spannung liefernder TFT ein n-leitender TFT ist.

7. Flüssigkristallanzeige nach Anspruch 4 oder 5, wobei jeder eine positve Spannung liefernder TFT und jeder eine negative Spannung liefernder TFT ein p-leitender TFT ist.

8. Flüssigkristallanzeige nach einem der vorstehenden Ansprüche, wobei das Treiberschaltungssystem mit positiver Polarität und das Treiberschaltungssystem mit negativer Polarität einteilig auf einem isolierten Substrat, auf dem eine der Elektroden gebildet ist, gebildet ist.

9. Verfahren zum Antreiben einer Flüssigkristallanzeige, wobei die Flüssigkristallanzeige eine Flüssigkristallkapazität (Clc11), die durch das Einschichten eines Flüssigkristalls zwischen eine Pixelelektrode (Pe) und eine gemeinsame Elektrode (Ce), die der Pixelelektrode gegenüberliegt, gebildet wird, einen eine positive Spannung liefernden TFT (TFTn11) zum Anlegen einer Spannung mit einer positiven Polarität an die Pixelelektrode (Pe), um die Flüssigkristallkapazität mit einer positiven Ladung aufzuladen, und einen eine negative Spannung liefernden TFT (TFTp11) zum Anlegen einer Spannung mit einer negativen Polarität an die Pixelelektrode (Pe), um die Flüssigkristallkapazität mit einer negativen Spannung aufzuladen, aufweist, wobei das Verfahren Folgendes enthält:

Anwenden eines Treiberschaltungssystems mit einer positiven Polarität, um einen eine positive Spannung

liefernden Gate-Impuls zu erzeugen und diesen Impuls an die Gate-Elektrode (G) des eine positive Spannung liefernden TFTs zu übermitteln; und
Anwenden eines Treiberschaltungssystems mit einer negativen Polarität, um einen eine negative Spannung liefernden Gate-Impuls zu erzeugen und diesen Impuls an die Gate-Elektrode (G) des eine negative Spannung liefernden TFTs zu übermitteln, wobei:

die Schaltungsanordnung in dem Treiberschaltungssystem mit positiver Polarität (GD1 & Lg11), die verwendet wird, um einen eine positive Spannung liefernden Gate-Impuls zu erzeugen und zu übermitteln, getrennt von der Schaltung in dem Treiberschaltungssystem mit negativer Polarität (GD2 & Lg12), die verwendet wird, um einen eine negative Spannung liefernden Gate-Impuls zu erzeugen und zu übermitteln, angeordnet ist,

dadurch gekennzeichnet, dass
ein Leitfähigkeitstyp von Kanälen des eine positive Spannung liefernden TFTs und des eine negative Spannung liefernden TFTs gleich ist; und
der eine positive Spannung liefernde Gate-Impuls eine höhere Spannung als der eine negative Spannung liefernde Gate-Impuls aufweist.

Revendications

1. Afficheur à cristaux liquides comprenant :

une capacitance de cristaux liquides (C1c11) formée en intercalant un cristal liquide entre une électrode de pixel (Pe) et une électrode commune (Ce) en regard de l'électrode de pixel ;
un transistor à couches minces (TFT) à application de tension positive (TFTn11) pour appliquer une tension ayant une polarité positive à l'électrode de pixel (Pe) de manière à charger la capacitance de cristaux liquide d'une charge positive ;
un transistor TFT à application de tension négative (TFTp11) pour appliquer une tension ayant une polarité négative à l'électrode de pixel (Pe) de manière à charger la capacitance de cristaux liquides d'une charge négative ;
un système de circuits d'attaque à polarité positive apte à générer une impulsion de grille à application de tension positive et à transmettre cette impulsion à une électrode de grille (G) du transistor TFT à application de tension positive ; et
un système de circuits d'attaque à polarité négative apte à générer une impulsion de grille à application de tension négative et à transmettre cette impulsion à une électrode de grille (G) du transistor TFT à application de tension négative,
dans lequel :

le montage de circuits dans le système de circuits d'attaque à polarité positive (GD1 & Lg11) qui génère et transmet ladite impulsion de grille à application de tension positive est prévu séparément du montage de circuits dans le système de circuits d'attaque à polarité négative (GD2 & Lg12) qui génère et transmet ladite impulsion de grille à application de tension négative,

caractérisé en ce que :

un type de conductivité de canaux du transistor TFT à application de tension positive et du transistor TFT à application de tension négative est le même ; et
ladite impulsion de grille à application de tension positive a une tension supérieure à une tension de ladite impulsion de grille à application de tension négative.

2. Afficheur à cristaux liquides conformément à la revendication 1 comprenant une pluralité de pixels, chacun desdits pixels comprenant une telle capacitance de cristaux liquides (C1c11, C1c12, C1c21, C1c22) ayant une telle électrode de pixel (Pe) et ayant également une telle électrode commune (Ce) à laquelle une tension commune est appliquée lorsque l'afficheur est en utilisation.

3. Afficheur à cristaux liquides conformément à la revendication 2, dans lequel les pixels comprennent chacun :

un tel transistor TFT à application de tension positive (TFTn11, TFTn12, TFTn21, TFTn22) pour appliquer une tension ayant la polarité positive à l'électrode de pixel (Pe) du pixel en question ; et
un tel transistor TFT à application de tension négative (TFTp11, TFTp12, TFTp21, TFTp22) pour appliquer une tension ayant la polarité négative à ladite électrode de pixel (Pe) du pixel concerné.

4. Afficheur à cristaux liquides conformément à la revendication 3, dans lequel le système de circuits d'attaque à polarité positive comprend :

une ligne de bus de grille à application de tension positive (Lg11, Lg21, Lg31) pour délivrer en sortie l'impulsion de grille à application de tension positive à l'électrode de grille (G) du transistor TFT à application de tension positive d'au moins l'un des pixels ; et
une ligne de bus de données à application de tension positive (Ld11, Ld21, Ld22) pour délivrer en sortie une tension de données ayant la polarité positive à une électrode de source (S) ou de drain (D) du transistor TFT à application de tension positive dudit ou desdits pixels ;
dans lequel le système de circuits d'attaque à polarité négative comprend :

une ligne de bus de grille à application de tension négative (Lg12, Lg22, Lg32) pour délivrer en sortie l'impulsion de grille à application de tension négative à l'électrode de grille (G) du transistor TFT à application de tension négative dudit ou desdits pixels ; et
une ligne de bus de données à application de tension négative (Ld12, Ld22) pour délivrer en sortie une tension de données ayant la polarité négative à une électrode de source (S) ou de drain (D) du transistor TFT à application de tension négative dudit ou desdits pixels.

5. Afficheur à cristaux liquides conformément à la revendication 4, dans lequel le système de circuits d'attaque à polarité positive comprend :

un circuit d'attaque de ligne de bus de grille (GD1) pour une attaque à polarité positive afin de délivrer en sortie l'impulsion de grille à application de tension positive à la ligne de bus de grille à application de tension positive ; et
un circuit d'attaque de ligne de bus de données (DD1) pour une attaque à polarité positive afin de délivrer en sortie la tension de données ayant la polarité positive à la ligne de bus de données à application de tension positive ;
dans lequel le système de circuits d'attaque à application de tension négative comprend :

un circuit d'attaque de ligne de bus de grille (GD2) pour une attaque à polarité négative afin de délivrer en sortie l'impulsion de grille à application de tension négative à la ligne de bus de grille à application de tension négative ; et
un circuit d'attaque de ligne de bus de données (DD2) pour une attaque à polarité négative afin de délivrer en sortie la tension de données ayant une polarité négative à la ligne de bus de données à application de tension négative.

6. Afficheur à cristaux liquides conformément à la revendication 4 ou 5, dans lequel ledit transistor TFT à application de tension positive et ledit transistor TFT à application de tension négative sont chacun un transistor TFT de type n.

7. Afficheur à cristaux liquides conformément à la revendication 4 ou 5 dans lequel ledit transistor TFT à application de tension positive et ledit transistor TFT à application de tension négative sont chacun un transistor TFT de type p.

8. Afficheur à cristaux liquides conformément à l'une quelconque des revendications précédentes, dans lequel le système de circuits d'attaque à polarité positive et le système de circuits d'attaque à polarité négative sont formés d'un seul tenant sur un substrat isolé sur lequel est formée l'une quelconque des électrodes.

9. Procédé d'attaque d'afficheur à cristaux liquides, l'afficheur ayant une capacitance de cristaux liquides (C1c11) formée en intercalant un cristal liquide entre une électrode de pixel (Pe) et une électrode commune (Ce) en regard de l'électrode de pixel, un transistor TFT à application de tension positive (TFTn11) pour appliquer une tension ayant une polarité positive à l'électrode de pixel (Pe) de manière à charger la capacitance de cristaux liquides d'une charge positive, et un transistor TFT à application de tension négative (TFTp11) pour appliquer une tension ayant une polarité négative à l'électrode de pixel (Pe) afin de charger la capacitance de cristaux liquides d'une charge négative, le procédé comprenant :

l'utilisation d'un système de circuits d'attaque à polarité positive pour générer une impulsion de grille à application de tension positive et pour transmettre cette impulsion à l'électrode de grille (G) du transistor TFT à application de tension positive ; et
l'utilisation d'un système de circuits d'attaque à polarité négative pour générer une impulsion de grille à application de tension négative et pour transmettre cette impulsion à l'électrode de grille (G) du transistor TFT à application de tension négative,
dans lequel :

le montage de circuits dans le système de circuits d'attaque à polarité positive (GD1 & Lg11) qui est utilisé pour générer et transmette ladite impulsion de grille à application de tension positive est prévu séparément du montage de circuits dans le système de circuits d'attaque à polarité négative (GD2 & Lg12) qui est utilisé pour générer et transmette ladite impulsion de grille à application de tension négative,

caractérisé en ce que :

un type de conductivité de canaux du transistor TFT à application de tension positive et du transistor TFT à application de tension négative est le même ; et
ladite impulsion de grille à application de tension positive a une tension supérieure à une tension de ladite impulsion de grille à application de tension négative.

FIG.1

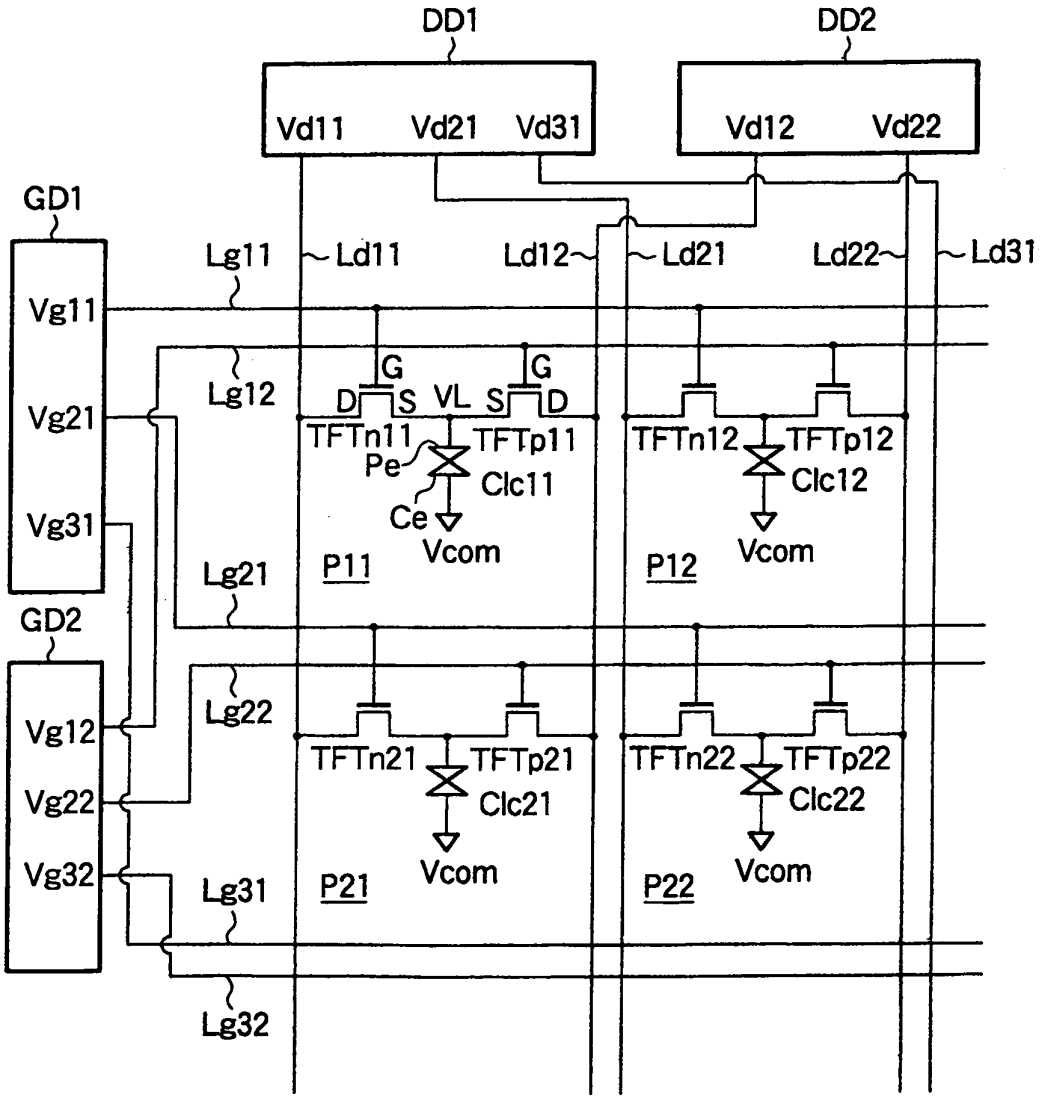

DD1
DD2
Vd11
Vd21
Vd31
Vd12
Vd22
GD1
Lg11
Ld11
Ld12
Ld21
Ld22
Ld31
Vg11
Vg21
Vg31
Lg12
G
D
S
VL
S
D
TFTn11
TFTp11
Pe
Clc11
Ce
Vcom
TFTn12
TFTp12
Clc12
Vcom
P11
P12
Lg21
GD2
Vg12
Vg22
Vg32
Lg22
TFTn21
TFTp21
Clc21
Vcom
TFTn22
TFTp22
Clc22
Vcom
P21
P22
Lg31
Lg32

FIG.2

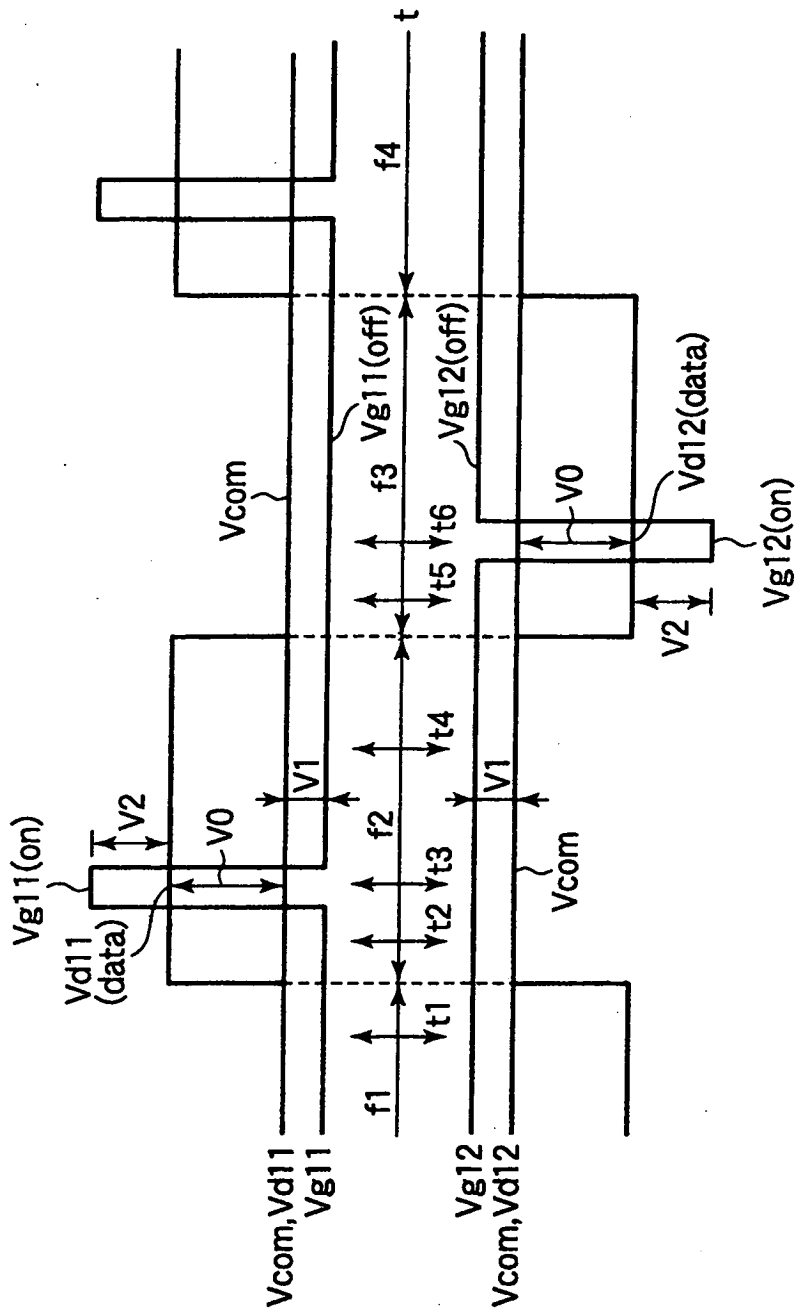

t
f4
f3
f2
f1
t6
t5
t4
t3
t2
t1
Vg11(off)
Vg12(off)
Vcom
Vd12(data)
V0
Vg12(on)
V2
V1
Vg11(on)
Vd11
(data)
Vcom,Vd11
Vg11
Vg12
Vcom,Vd12

FIG.3

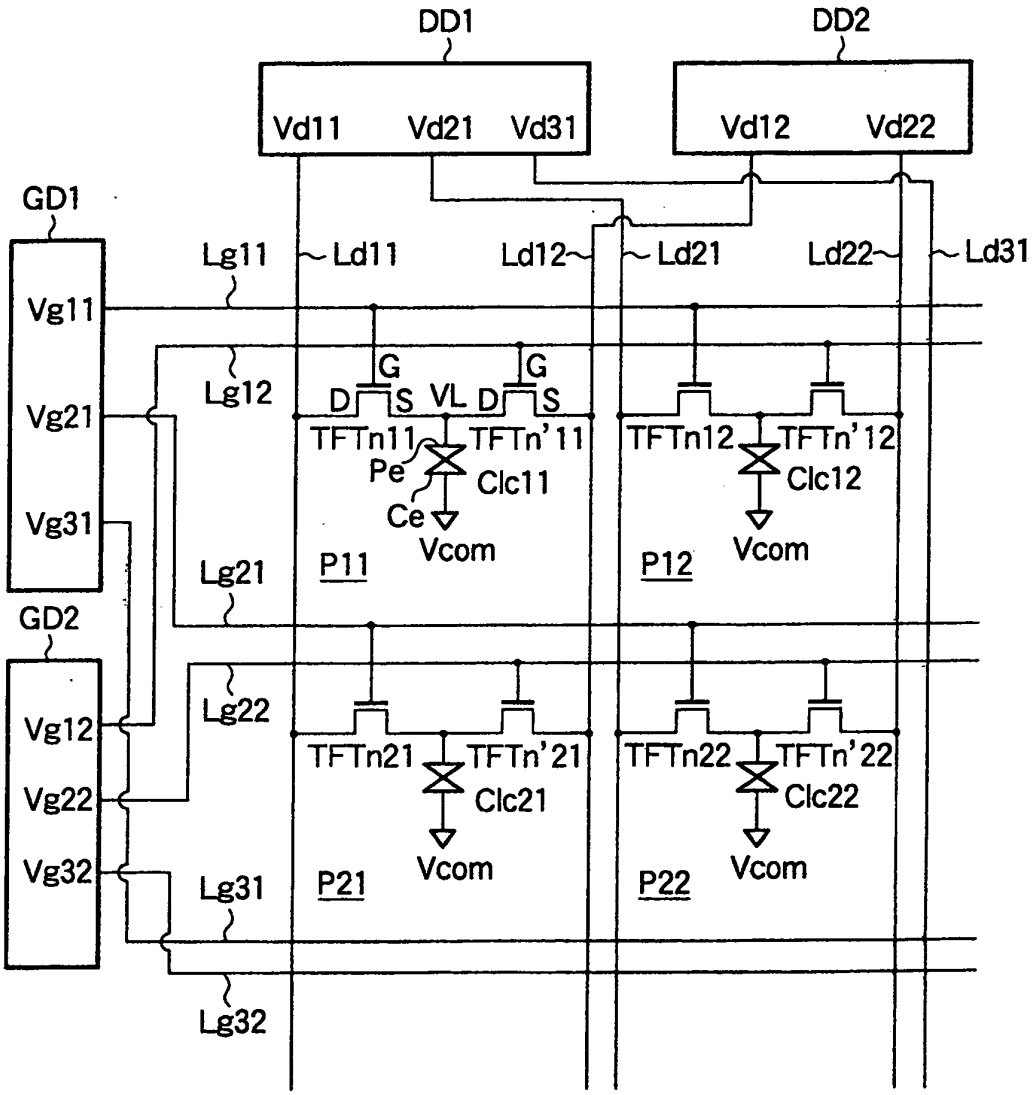

DD1
DD2
Vd11
Vd21
Vd31
Vd12
Vd22
GD1
Lg11
Ld11
Ld12
Ld21
Ld22
Ld31
Vg11
Vg21
Vg31
Lg12
G
D
S
VL
TFTn11
TFTn'11
TFTn12
TFTn'12
Pe
Ce
Clc11
Clc12
Vcom
P11
P12
Lg21
GD2
Vg12
Vg22
Vg32
Lg22
TFTn21
TFTn'21
TFTn22
TFTn'22
Clc21
Clc22
P21
P22
Lg31
Lg32

FIG.4

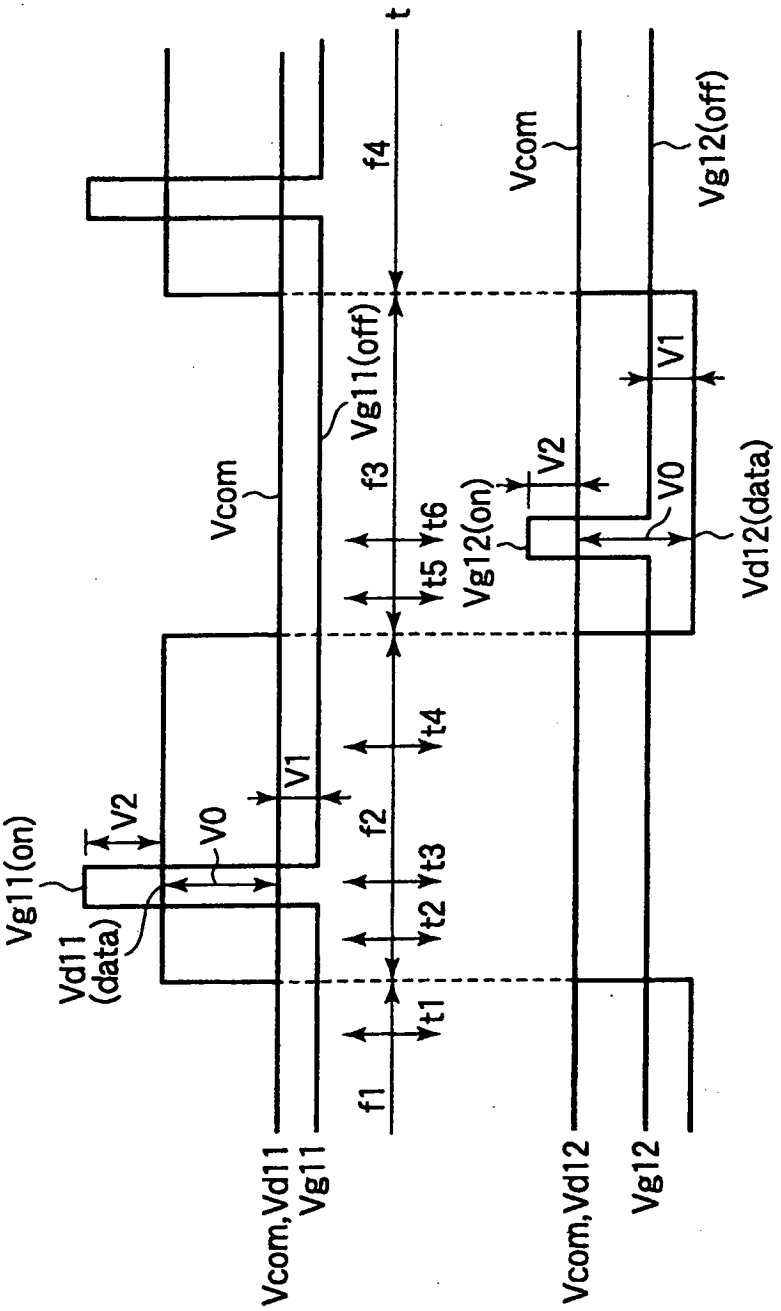

t
f4
f3
f2
f1
t6
t5
t4
t3
t2
t1
Vcom
Vg11(off)
Vg11(on)
Vd11
(data)
V2
V0
V1
Vcom,Vd11
Vg11
Vcom
Vg12(off)
Vg12(on)
V2
V0
V1
Vd12(data)
Vcom,Vd12
Vg12

FIG.5

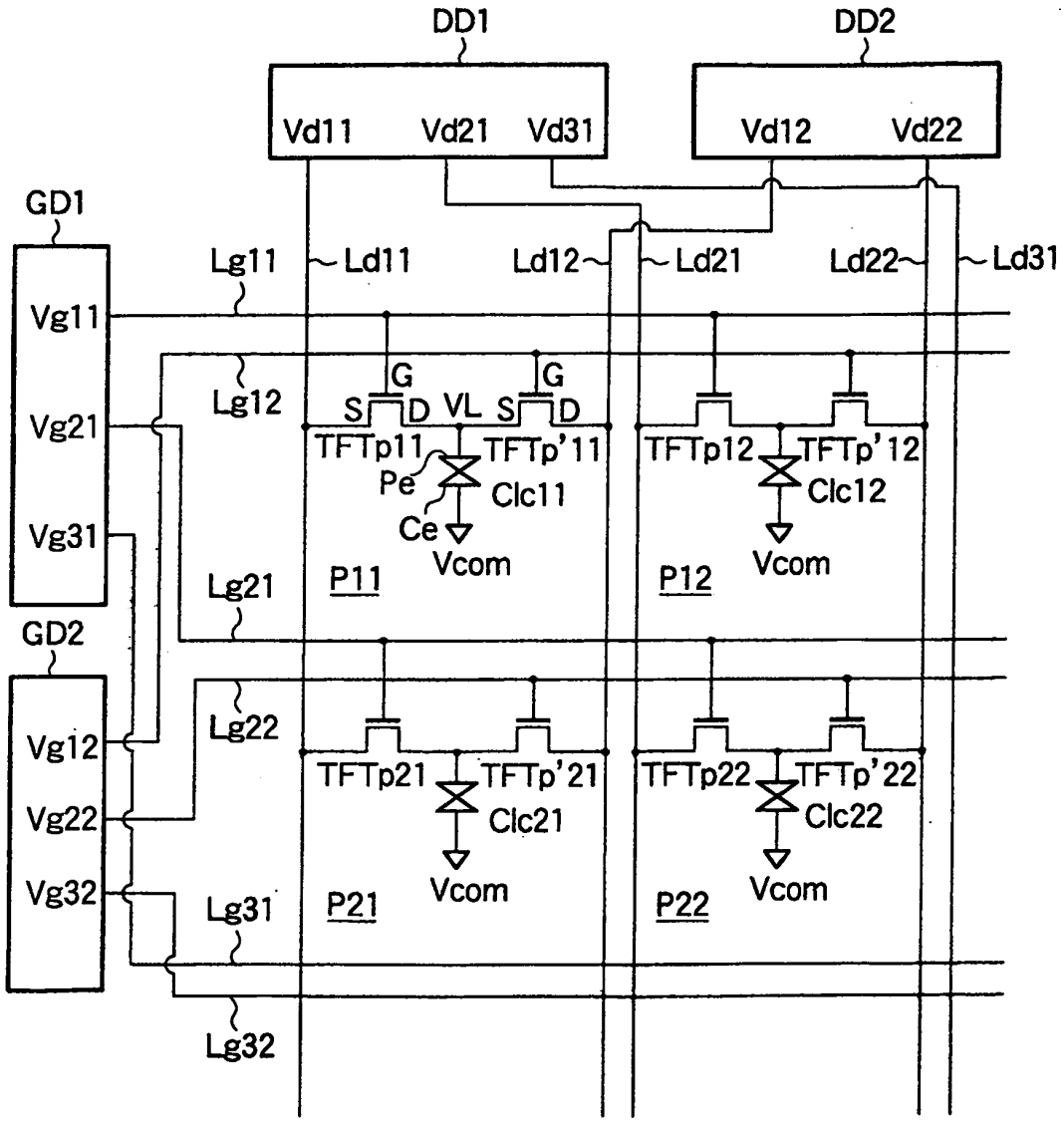

DD1
DD2
Vd11
Vd21
Vd31
Vd12
Vd22
GD1
Lg11
Ld11
Ld12
Ld21
Ld22
Ld31
Vg11
Vg21
Vg31
Lg12
G
S
D
VL
TFTp11
TFTp'11
TFTp12
TFTp'12
Pe
Clc11
Ce
Vcom
Clc12
P11
P12
Lg21
GD2
Vg12
Vg22
Vg32
Lg22
TFTp21
TFTp'21
TFTp22
TFTp'22
Clc21
Clc22
P21
P22
Lg31
Lg32

FIG.6

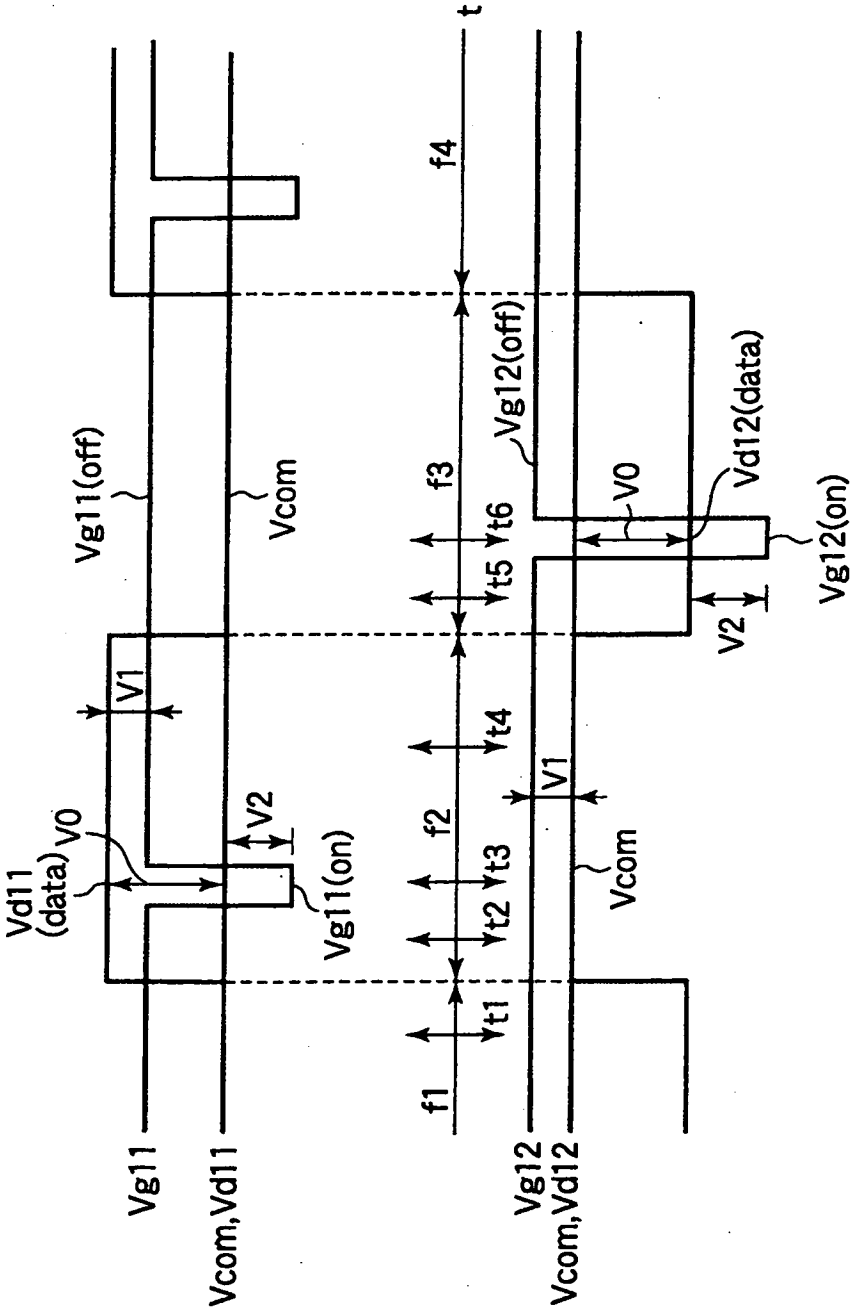

t
f4
f3
f2
f1
t6
t5
t4
t3
t2
t1
Vg11(off)
Vcom
Vg12(off)
Vd12(data)
V0
Vg12(on)
V2
V1
Vd11
(data)
V0
V2
Vg11(on)
V1
Vcom
Vg11
Vcom,Vd11
Vg12
Vcom,Vd12

FIG.7

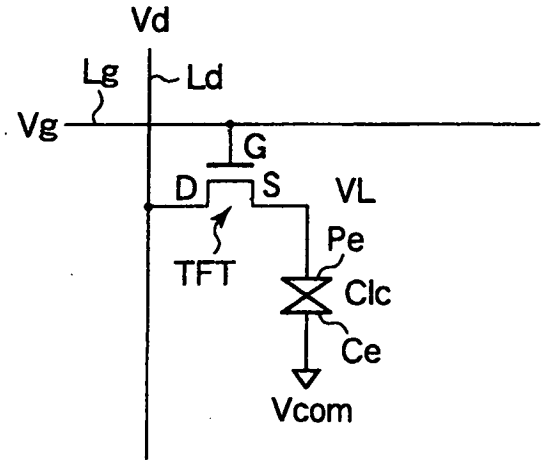
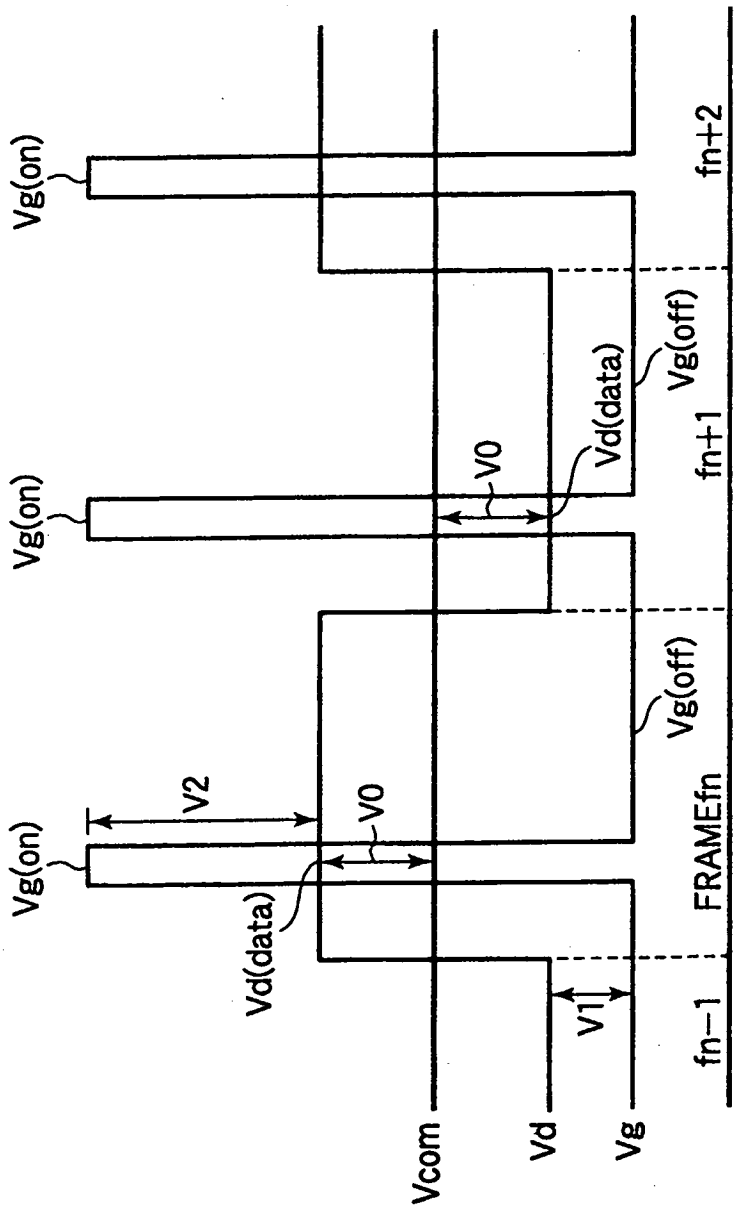


FIG.8


Vg(on)
Vg(on)
Vg(on)
V2
V0
V0
Vd(data)
Vd(data)
Vg(off)
Vg(off)
FRAMEfn
fn+2
fn+1
fn−1
V1
Vcom
Vd
Vg

REFERENCES CITED IN THE DESCRIPTION

This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

Patent documents cited in the description

- EP 0915453 A **[0016]**
- US 20010050644 A **[0016]**
- US 5436635 A **[0016]**
- JP 6266315 A **[0016]**

专利名称(译)	具有降低的驱动电压的液晶显示器和用于正电压和负电压的单独驱动电路		
公开(公告)号	EP1335343B1	公开(公告)日	2012-07-25
申请号	EP2002258053	申请日	2002-11-22
[标]申请(专利权)人(译)	富士通株式会社		
申请(专利权)人(译)	FUJITSU LIMITED		
当前申请(专利权)人(译)	夏普株式会社		
发明人	SASAKI, NOBUO, C/O FUJITSU LIMITED		
IPC分类号	G09G3/36 G02F1/1362 G02F1/1368 G02F1/133 G09G3/20		
CPC分类号	G09G3/3659 G02F1/136286 G02F2001/136245 G09G3/3614 G09G2300/0823 G09G2310/06		
优先权	2002027590 2002-02-05 JP		
其他公开文献	EP1335343A2 EP1335343A3		
外部链接	Espacenet		

摘要(译)

提供一种有源矩阵型TFT LCD，其中像素TFT的驱动电压降低。像素（P11）由两个薄膜晶体管（TFTn11，TFTp11）形成，即，施加正电压的n沟道TFT（TFTn11），用于向像素电极施加具有正极性的数据电压（Vd11）（ Pe）和施加负电压的p沟道TFT（TFTp11），用于向像素电极（Pe）施加具有负极性的数据电压（Vd12）。施加正电压的TFT（TFTn11）的源电极（S）连接到像素电极（Pe）;其漏极（D）连接到用于施加正电压的数据总线（Ldll）（Vd11）;并且其栅极（G）连接到用于施加正电压（Vd11）的玛瑙总线（Lg11）。另一TFT（TFTp11）的源电极（S）也连接到像素电极（Pe）;其漏极（D）连接到用于施加负电压（Vd12）的数据总线（Ldl2）;并且其栅极（G）连接到用于施加负电压（Vd12）的栅极总线（Vg12）。