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(54) Display device with memory integrated on the display substrate

Anzeigevorrichtung mit im Anzeigesubstrat integriertem Speicher

Dispositif d' affichage avec mémoire integrée sur le substrat d' affichage

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- **PATENT ABSTRACTS OF JAPAN vol. 1997, no. 01, 31 January 1997 (1997-01-31) & JP 08 227283 A (SEIKO EPSON CORP), 3 September 1996 (1996-09-03) & US 2002/145602 A1 (MATSUEDA YOJIRO) 10 October 2002 (2002-10-10)**
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Description

TECHNICAL FIELD

[0001] The present invention relates to display devices. More particularly, the invention relates to a drive circuit or the like to make display on a liquid crystal display (LCD: Liquid Crystal Display) or an organic EL display (OELD: Organic Electro Luminescent Display).

BACKGROUND OF THE INVENTION

[0002] Recently, display devices using liquid crystal (hereinafter, referred to as display) are spreading at conspicuous pace. The display of this type is low in power consumption and improved in saving space in comparison with a CRT display. Accordingly, it is important to make use of the merits of such a display and produce a display that is lower in power consumption and improved in saving space.

[0003] Fig. 11 is a block diagram of a system to implement display through a display device with a TFT display. This system is constituted with an image signal source 100 and a TFT liquid crystal display panel 101. The image signal source 100 is formed, at least, by a CPU 100A, a RAM 100B, a frame memory 100C and an LCD controller 100D. The CPU 100A is operation control means to transmit display data while exchanging data with the RAM 100B as a general-purpose memory. This memory RAM 100B is not especially provided only as a display memory, and hence requires specifically a memory to store data for display. It can be the frame memory 100C. The frame memory 100C temporarily stores display data for one screen of a liquid crystal panel 101C (hereinafter, the data for one pixel is given as display data, and each binary signal forming the display data is referred to as an image signal). The LCD controller 100D is to implement transmission control or the like of display data, in order to display in timing the display data stored in the frame memory 100C in display positions on the liquid crystal panel 101C. Although for the CRT there is a need to transmit the display data through conversion into analog data, the display data herein is transmitted by an image signal as digital data on the assumption that the interface of the liquid crystal display corresponds to digital data. If the image signal is digital data, D/A conversion is not required on the side of the TFT liquid crystal display panel 101.

[0004] Meanwhile, the TFT liquid crystal display panel 101 is structured with a scanning line driver 101A, a digital data driver 101B and a liquid crystal panel 101C. The scanning line driver 101A controls display in a scanning line (row) direction on the basis of timing data transmitted from the LCD controller 100D. The digital data driver 101B can receive and process digital-data image signal. The digital data driver 101B controls display in a data-line (column) direction on the basis of timing data transmitted from the LCD controller 100D. Thereupon, display tonal level is also controlled. The liquid crystal panel 101C is a panel having TFTs (Thin Film Transistors) to make display under the control of the scanning line driver 101A and digital data driver 101B.

[0005] In such a system, the LCD controller 100D must transmit to the digital data driver 101B the display-data image signal for the entire screen temporarily stored in the frame memory 100C. Moreover, transmission timing by progressive scanning is fixed. Consequently, there is a need to transmit image signals in timing also for the display data on the pixels not requiring display change. Due to this, there is an increase in useless data transmission amount and hence increase in power consumption. Thus, reduction of power consumption cannot be achieved.

[0006] Therefore, it is an object of the present invention to obtain a display device of a space-saved design having a structure for achieving consumption-power reduction and moreover taking into consideration layout efficiency particularly for the case of integrally forming the peripheral circuit over a glass substrate.

[0007] JP082277283 discloses an image display matching with an optional gradation display charactristic by providing a data conversion circuit converting the digital input video data of n bits to n+m bits and a digital data driver of n+m bits. The digital image signal data of (n) bits are converted to the digital image signal data of n+m bits by a data conversion circuit. A gamma characteristic correcting ROM is used as the data conversion circuit.

[0008] US2002/145602 discloses a driving method for a liquid crystal display wherein an n-bit digital image data is converted to (n+m)-bit data with a g-correction table, and displayed by the use of a (n+m)-bit D/A converter. A peripheral-driver logic section is driven with a low-voltage common power source. Data input to the D/A converter is not reversed and the power to the D/A converter is made alternating to apply an AC voltage to aligned crystal layer. A circuit is provided in order to compensate for a delay time in the driver.

[0009] Abbot et al: "Equipping a line of memories with spare cells", Electronics, VNU Business Publications, Vol. 54, No. 15, pp. 127 - 130 (1981), discloses a device wherein a line of memories is equipped with spare cells to create redundancy.

[0010] US5815136 discloses a liquid crystal display which has a liquid crystal panel having a plurality of data lines and a plurality of scanning lines arranged in a matrix form with pixels being formed at intersections of the data and scanning lines, a scanning circuit for successively applying a voltage to the scanning lines, and a liquid crystal driver for receiving display data from an external device to apply a voltage corresponding to the display data to the data lines. The scanning circuit includes a synchronizing signal generating circuit for generating a frame display synchronizing signal indicative of a frame period for display of image on the liquid crystal panel and a line display synchronizing signal indicative of a line period for image display on the liquid crystal panel. The liquid crys-

tal driver includes a display memory accessed through a memory interface for reading and writing of data, the display memory storing therein display data corresponding to the pixels.

[0011] EP0286309 discloses a display control unit which is combined with a display device including X and Y side electrodes and a display element sandwiched between the X and Y side electrodes. The display control unit includes a plurality of lines for supplying voltages having different values to the X and Y side electrodes, a switch for connecting the lines with the electrodes or disconnecting the lines from the electrodes, and a unit for controlling the switch within a selection period of the X or Y side electrodes.

[0012] EP0456394 discloses an architecture for a memory array having a random access port and a serial access port configured and operable to provide selectively different ordering of the data bits at the two ports. The pixel data at the serial access port is structured to coincide by row with the raster scan of the video display.

DISCLOSURE OF THE INVENTION

[0013] A display device of the invention of claim 1, comprises: an active matrix display section having a plurality of scanning lines extending in a row direction of the active matrix display section; a plurality of data lines formed in a grid form, whereby in the grid the intersections of a scanning line with a data line corresponds to dots which are the smallest controllable units of display; a plurality of active elements located at each intersection of a scanning line with a data line; a scanning line driver section that drives said plurality of scanning lines; a data line driver that drives the plurality of data lines; a plurality of memory cells arranged in a matrix having a plurality of rows and a plurality of columns; a column decoder section that selects said memory cells for storing an input image signal; and a selection switch section that controls transmission of first image signals to the plurality of memory cells, the active matrix display section, the plurality of memory cells and the selection switch section being formed on one substrate, the plurality of memory cells being formed between the active matrix display section and the selection switch section, the plurality of memory cells being arranged such that the plurality of memory cells store first image signals supplied through the selection switch, and the display device being arranged such that second image signals that are generated based on the first image signals are supplied to one data line of the plurality of data lines characterized in that, the number of said plurality of memory cells is sufficient to store an image signal for display control of all of the dots on one row of the active matrix display section and wherein the plurality of memory cells is allocated to have a row length that is smaller than the length in the row direction of said active matrix display section and is formed in a multi-stage structure.

[0014] In this invention, where the memory cell cannot be allocated corresponding to the length in the row direction of the active matrix display section by the increase of the memory cell in amount of one dot for example due to increase in the number of tonal levels, the structure and the formation is made by providing multi-stages.

[0015] In this invention, where integral formation is made using polysilicon TFTs including a peripheral circuit on an insulating substrate, for example, of a glass substrate, or a quartz substrate, memory cells of the memory cell section are allocated in the number capable of storing an image signal for display control of at least the dots on one row of the active matrix display section corresponding to a length in a row direction of the active matrix display section in order to achieve space saving, besides the column decoder section, column select switch section and data line driver section.

[0016] It is noted that the points "allocated corresponding to a length in a column direction" and "allocated corresponding to a row direction" mean that, for example, in the memory cell section, the length in the row direction thereof corresponds to a length in the row direction of the active matrix display section. More specifically, this means "the length in the row direction is equal to or smaller than the length in the row direction of the active matrix display section". The meaning of "equal to or smaller than" is either that the both are equal or that the former is small as compared to the latter. In the invention, however, for example the length in the row direction of the memory cell section may be satisfactorily somewhat greater (e.g. about several %) than the length in the row direction of the active matrix display section.

[0017] In brief, for the memory cell section, for example, it is satisfactory, where integrating it together with the active matrix display section on a substrate, to avoid the occurrence of a useless space on the substrate due to non-correspondence of the dimensions of the memory cell section to the dimensions of the active matrix display section. The occurrence of a useless space is meant, for example, to cause a comparatively broad space that no circuit is provided on the substrate in an area of the active matrix display section along a row-direction-side end because the length in the row direction of the memory cell section is largely longer than the length in the row direction of the active matrix display section.

[0018] A display device of the invention of the characterizing portion of claim 1 structures redundant in the number of the memory cells allocated corresponding to the length in the row direction of the active matrix display section.

[0019] In this invention, even if structuring redundantly in the number of the memory cells in the number capable of storing the image signal for display control of the dots on one row of the active matrix display section, they are allocated on the basis of the length in the row direction of the active matrix display section (e.g. to have a length in the row direction smaller than the length in the row direction of the active matrix display section).

[0020] A display device of the invention of claim 2 is

that the memory cell section connects the memory cells in the number capable of storing an image signal for display control of the one-row dots to each of the word lines in the number equal to the number of the scanning lines and is structured with a memory array corresponding to dot arrangement of the active matrix display section, and a word line driver section for selecting and driving the word lines is further integrated on and integrally formed with the substrate.

[0021] In this invention, the memory cell section is structured by a memory array corresponding to the dot arrangement of the active matrix display section to store an image signal required for displaying one screen thereby providing a structure capable of reducing data amount externally exchanged and achieving reduction in power consumption. Also, in order to store due to the array structure, on the substrate is integrated and integrally formed therewith a word line driver section to select and drive the word lines provided equal in the number to the scanning lines.

[0022] A display device of the invention of claim 3 is that, on the basis of an address signal representative of a display position and a storage position, the scanning line driver section selects the scanning lines and the word line driver section selects the word lines.

[0023] In this invention, a scanning line and a word line can be selected randomly by an address signal to secure the freedom in storage or display with respect to the column direction.

[0024] A display device of the invention of claim 4 is that the same address signal is inputted to the scanning line driver section and the word line driver section.

[0025] In this invention, in order to simplify the interconnections, the same lines can be shared by the scanning line driver section and the word line driver section. Consequently, the same address signal can be inputted in the same timing.

[0026] A display device of the invention of claim 5 is that independent address signals are inputted to the scanning line driver section and the word line driver section.

[0027] In this invention, in order to enhance the freedom in storage and display operations, independent address signals are inputted to the scanning line driver section and the word line driver section, e.g. operation timing can be made different.

[0028] A display device of the invention of claim 6 is that the scanning line driver section operates to select and drive the scanning lines on the basis of the address signal only when a scanning line driver control signal is inputted, and the word line driver section operates to select and drive the word lines on the basis of the address signal only when a word line driver control signal is inputted.

[0029] In this invention, in order to simplify the interconnections while enhancing the freedom of storage and display operations, the scanning line driver section can perform selection and driving operations of a scanning lines on the basis of an address signal only when a scanning line driver control signal is inputted and the word line driver section perform selection and driving operations of a word line on the basis of the address signal only when a word line driver control signal is inputted.

[0030] A display device of the invention of claim 7 is that the column decoder section selects the memory cell to store an inputted image signal on the basis of the address signal.

[0031] In this invention, the column decoder section can select randomly a memory cell to store an image signal due to the address signal and secure the freedom in storage and display with respect to the row direction.

[0032] A display device of the invention of claim 8 is that one pixel comprises three dots provided for displaying red, blue and green as light source colors, the image signal being input on the basis of a unit of one-pixel, and the column decoder section selects the memory cell in an amount of one pixel.

[0033] In this invention, where the display device performs color displays, the three dots provided for displaying the colors of red, blue and green as light source colors are taken as one pixel to input an image signal on the basis of a unit of one-pixel as a display change unit. The column decoder section selects memory cells in an amount of the one pixel on the basis of that input.

[0034] A display device of the invention of claim 9 is that one pixel comprises three dots provided for displaying red, blue and green as light source colors, the image signal being input on the basis of a unit of a plurality of pixels, and the column decoder section selects the memory cells in an amount of the plurality of pixels.

[0035] In this invention, where the display device performs color displays, in order to decrease the drive frequency, the three dots provided for displaying the colors of red, blue and green as light source colors are taken as one pixel to input an image signal on the basis of a unit of a plurality of pixels. The column decoder section selects memory cells in an amount of the plurality of pixels on the basis of that input.

[0036] A display device of the invention of claim 10 is that an input interconnection for the image signal to be stored in the memory cell and the column selection switch section are formed on a side opposite to the active matrix display section sandwiching the memory cell section.

[0037] In this invention, crossover of interconnections is decreased to improve reduction in consumption power. Also, in order to prevent noise superposition due to the effect of switching or the like, the image-signal input interconnections and the column selection switch section are formed on a side opposite to the active matrix display section sandwiching the memory cell section.

[0038] A display device of the invention of claim 11 is that the word lines are provided in the number of integer times the number of the scanning lines, and the memory cell section structured by a memory array connecting, by grouping, the memory cells in the number capable of storing the image signal for display control of the one-row

dots of the active matrix display section to the word lines in the number of the integer times.

[0039] In this invention, where the memory cell cannot be allocated corresponding to the length in the row direction of the active matrix display section, for example, by memory-cell increase for one dot due to the increase of tonal levels, the structure and the formation is made by providing a plurality of rows.

[0040] A display device of the invention of claim 12 is that the memory cell section is structured by a memory array having the memory cells that are in the number capable of storing the image signal for display control of a plurality of rows of the dots of the active matrix display section and allocated to have a row length smaller than the length in the row direction of the active matrix display section.

[0041] In this invention, where a plurality of rows of memory cells are allocated corresponding to the length in the row direction of the active matrix display section, in order to save space, the memory cells in the number capable of storing an image signal for display control of a plurality of rows of dots of the active matrix display section are structured by a memory array assigned corresponding to the length in the row direction of the active matrix display section.

[0042] A display device of the invention of claim 13 further comprises a timing controller section for controlling timing of transmitting the address signal, and a memory controller section for controlling to transmit the first image signal, integrated on a semiconductor or an insulating substrate and integrally formed therewith.

[0043] In this invention, the peripheral circuits required for controlling display are all integrally formed systematically on the same substrate.

[0044] A display device of the invention of claim 14 is that a D/A converter is provided between the active matrix display section and the memory cell section, thereby converting the image signal comprising a digital signal stored in the memory cell into an analog signal, followed by supplying to the active matrix display section.

[0045] In this invention, in order to display in an analog-compatible active matrix display section, a D/A converter is provided between the active matrix display section and the memory cell section. In the D/A converter, the image signal after converting into an analog signal is supplied to the active matrix display section.

[0046] A display device of the invention of claim 15 is that the active matrix display section and the memory cell section are directly coupled to supply the image signal comprising a digital signal stored in the memory cell section to the active matrix display section.

[0047] In this invention, display is made in the active matrix display section compatible with digital signals. No D/A converter or the like is provided between the active matrix display section and the memory cell section. The image signal remained in the digital signal is supplied to the active matrix display section.

[0048] A display device of the invention of claim 16 is that the active matrix display section performs digital drive through area tonal level, time-division tonal level or a combination thereof.

[0049] In this invention, the active matrix display section compatible with digital signals makes display through area tonal level, time-division tonal level or a combination of the both.

BRIEF DESCRIPTION OF THE DRAWINGS

[0050]

Fig. 1 is a block diagram representing a concept of a system including a display device according to a first embodiment of the present invention.
Fig. 2 is a diagram representing in detail a panel 1.
Fig. 3 is a diagram representing in detail a panel 1A according to a second embodiment of the invention.
Fig. 4 is a diagram representing in detail a panel 1B according to a third embodiment of the invention.
Fig. 5 is a diagram representing in detail a panel 1C according to a fourth embodiment of the invention.
Fig. 6 is a diagram representing in detail a panel 1D according to a fifth embodiment of the invention.
Fig. 7 is a diagram representing in detail a panel 1E according to a sixth embodiment of the invention.
Fig. 8 is a diagram showing a circuit arrangement of an active-matrix OEL section 8.
Fig. 9 is a diagram representing in detail a panel 1F according to a seventh embodiment of the invention.
Fig. 10 is a diagram showing a circuit arrangement of an active-matrix LCD section 2A.
Fig. 11 is a block diagram of a system for display through a display device by a TFT display.

[0051] No protection is sought for a display device comprising both an active matrix display section having a plurality of scanning lines extending in a row direction and a plurality of memory cells, wherein the active matrix display section and the plurality of memory cells are formed on one substrate, and wherein the plurality of memory cells are allocated to have a row length that is equal to the length in the row direction of the active matrix display section.

BEST MODE FOR CARRYING OUT THE INVENTION

Embodiment 1

[0052] Fig. 1 is a block diagram showing a concept of a system including a display device according to Embodiment 1 of the present invention. Fig. 1 represents a concept called system-on-panel (SOP). SOP is the concept to form a peripheral circuit for display or the like over a glass substrate, and moreover to integrally form TFTs or the like together with the peripheral circuit by the use of poly-silicon or the like without using chips of ICs or the like. Due to this, the panel can be directly coupled to the

CPU while achieving low cost, high reliability and space saving.

[0053] In Fig. 1, an image signal source 110 is configured by a CPU 110A to transmit display data. Herein, the display data is transmitted with image signals as digital data, similarly to the conventional configuration shown in Fig. 11. If the image signal is digital data, D/A conversion is not required on the side of a panel 1, correspondingly achieving the reduction in size and power consumption. Meanwhile, the panel 1 is configured with an active-matrix LCD section 2, a scanning line driver 3, a digital data driver 4, a frame memory section 5, a memory controller 6 and a timing controller 7. The active-matrix LCD section 2 corresponds to a display drive section in the present invention.

[0054] Fig. 2 is a figure representative in detail of the panel 1. The active-matrix LCD section 2 is a part for actual display by use of active elements of TFTs, diodes or the like. The active-matrix LCD section 2 is arrayed with pixels in the number of $i \times j$. Because the present embodiment assumes a color display, three dots (termed also as sub-pixels) of R (Red), G(green) and B (Blue) as light-source colors are constituted as one pixel. For a monochromatic display, the pixel equals to the dot. The dot areas include data lines, scanning lines and active elements (e.g. switching elements by transistors, diodes or the like) arranged corresponding to the intersections of them. The active elements respectively have pixel electrodes to form a capacitance through a liquid crystal to a counter electrode. The voltage applied between the pixel electrode and the counter electrode controls the optical rotatory power due to liquid-crystal molecules, making display control on each dot. Moreover, even if the active element turns off the switch, the pixel electrode can sustain its displaying state owing to the storage charge before refreshing (display data rewriting) in the next time. The switch operation to the active elements and control of the charge supply to the pixel electrodes are implemented by driving a data line and scanning line (supplying current).

[0055] It is a scanning line driver 3 that controls to drive a scanning line. The scanning line driver 3 is formed by a row decoder 31 and a scanning line drive buffer 32. The row decoder 31 selects a scanning line to be driven on the basis of address data inputted. The scanning line drive buffer 32 actually drives the scanning line selected by a row decoder 31.

[0056] Meanwhile, it is a digital data driver 4 that controls to drive a data line. The digital data driver 4 is formed by a k-bit DAC section 41 as a D/A converter. Herein, a frame memory section 5 will be explained before explaining the operation of the k-bit DAC section 41.

[0057] The frame memory section 5 is configured by a column decoder 51, an input control circuit 52, a column selection switch section 53, a memory row decoder 54, a word driver 55, a memory cell section 56 and a sense amplifier section 57. The column decoder 51 selects one pixel out of one row (line) of pixels (in the number of j) on the basis of input address data. This ultimately results in selection of a to-be-driven data line. The input control circuit 52 is a circuit to control an image signal ($k \times 3$) in one-pixel amount transmitted in parallel from the memory controller 6. The column selection switch section 53 is provided in the number of pixels on one line (i.e. $k \times 3 \times j$) with reference to one-pixel image signal ($k \times 3$) as a unit. Each column selection switch performs switching on the basis of column decoder 51 selection and image signal, driving a bit line. Herein, the input control circuit 52 and column selection switch section 53 is arranged on a side opposite to the active-matrix LCD section 2 while sandwiching the memory cell section 56. This reduces interconnection crossing over, thus achieving simplification and consumption-power reduction. Moreover, by the operation of the input control circuit 52 and column selection switch section 53, no noise will be interposed over the analog-driven LCD 2. Thus, noise reduction in display can be achieved.

[0058] The memory row decoder 54 selects a word line on the basis of input address data, in order to store to a desired memory cell of the memory cell section 56 forming the memory array, as described later. The word driver 55 actually drives a word line selected by the memory row decoder 54. Consequently, the image signal is stored as the pixel display data to the memory cells in the number of $k \times 3$ that are connected to the word line selected by the memory row decoder 54 and corresponding to the pixels selected by the column decoder 51.

[0059] Meanwhile, the memory cell section 56 has memory cells in the number of $k \times 3 \times i \times j$ to constitute a memory array of i-lines $\times$ k $\times$ 3 $\times$ j-columns. This number of memory cells is the number required for each dot of R, G or B of the display having a screen of $i \times j$ pixels to make display with brightness in a tonal level of 2k. In Fig. 2, k = 3 is given to enable setting with eight tonal-levels of brightness. This number of memory cells is the number of memory cells required, at least, to store an image signal in amount of one screen. For example, in some circuits, a circuit configuration is given with redundant memory cells for the necessity of securing operation stability.

[0060] Herein, space saving will be achieved to a greater extent as the size of the glass substrate become equal to the size of the active-matrix LCD section 2 as an actual display part. That is, if the memory cells are arranged such that the length of the memory cell section 56 in the row direction is smaller than the length of the active-matrix LCD section 2 in the row direction, the memory cells in one column can be arranged most efficiently with a saved space width. Consequently, because the length of memory-cell arrangement in the row direction required to control 1-dot display is smaller than a pitch of dots, the length of the entire frame memory section 5 in the row direction is given smaller than the length of the active-matrix LCD section 2 in the row direction. Design is made in Fig. such that the length in the row direction of k-bit memory cell arrangement equals to each pitch of

dots. Each sense amplifier (or selection switch) of the sense amplifier section 57 and each k-bit DAC of the k-bit DAC section 41 are also designed based upon each pitch of dots.

[0061] Also, the number of rows of the memory array is made equal to the number of scanning lines i so that the memory frame section 5 can store display data in amount of 1 screen. Consequently, it is possible to carry out storage with correspondence between a display-positioned pixel and a memory cell provided on a dot-by-dot basis. In order to achieve only space saving, it is satisfactory to have at least one row of memory cells without the especial necessity of constituting a memory array having the number of rows equal to the number of scanning lines. However, in order to reduce the data transmission amount over the system overall and low power consumption, memory cells are required in amount enough to store display data in amount of 1 screen with correspondence. Accordingly, an image signal in amount of display data for a to-be-rewritten pixel is satisfactorily transmitted from the CPU 110A. If no rewriting is made, the digital data driver 4 satisfactorily deals with the image-signal data stored in the memory cell section 56 as it is.

[0062] Each sense amplifier constituting the sense amplifier section 57 is connected on column (bit line) -by-column basis. Herein, the use of the sense amplifier is for the case each memory cell of the memory cell section 56 is configured by a dynamic memory. In the case of configuration with a static memory, selection switches are used in configuration instead of sense amplifiers.

[0063] The k-bit DAC section 41 constituting the digital data driver 4 is configured by k-bit DACs in the number of $3 \times j$. Each k-bit DAC is inputted with digital data based on the image signal stored on certain memory cells in the number of k through the bit lines in the number of k. The k-bit DAC converts the data-based value into a tonal level, depending upon which tonal level a data line is driven. In the LCD, alternating-current drive is required for the purpose of extending the life of liquid crystal. Accordingly, digital data cannot be used as it is but must be analog-converted. In this manner, display control is made, on the basis of display data, on the dot at an intersection of a driven scanning line and a data line.

[0064] Herein, the digital data driver 4 and the frame memory section 5 of the invention are directly coupled (integrated) to drive-operate the data line by the direct use of stored digital data. Accordingly, for convenience (in relation to Fig. 1), the digital data driver 4 is configured by the k-bit DAC section 41, and the frame memory section 5 is configured by the column decoder 51, the input control circuit 52, the column selection switch section 53, the memory row decoder 54, the word driver 55, the memory cell section 56 and the sense amplifier section 57. However, actually such distinction cannot be exactly made if considering the operational relationship between the digital data driver and the frame memory in the conventional use.

[0065] The memory controller 6 controls as $k \times 3$ image signals in order to store the display data transmitted from the CPU 110A into the frame memory section 5. Also, the timing controller 7 has at least an address buffer 71 and transmits an address signal to the row decoder 31, column decoder 51 and memory row decoder 54 in order to store or display the display data transmitted from the CPU 110A.

[0066] In the case of configuring the memory by chips or the like, it is problematic in what way fine provision can be made within the chip and layout be given by taking interconnection, etc into consideration. Where the peripheral circuit such as the memory on a glass substrate, conception differs from that. It is the active-matrix LCD section 2 as an actual display part that occupies over the greatest area on the glass substrate. Moreover, the pitch of pixels (ultimately the entire size) is fixed. Consequently, it is the problem that the system, such as peripheral circuits, is laid out with efficiency in accordance with the size. Although the memory cells can be lessened if considering space saving without considering consumption power, the reduction of consumption power requires memory cells for storing data in amount of one screen. Therefore, the present embodiment aims at presenting the most efficient layout on the basis of establishing a peripheral circuit in order for reducing consumption power.

[0067] Next, explanation will be made on the operation of display on the basis of Fig. 2. The CPU 110A transmits display data where to provide change in display. Consequently, where the image does not change, no display data is transmitted. When changing the display, an address signal is transmitted representative of a point (pixel) to be changed in display. Also, a display-data image signal is transmitted. Herein, the frame memory section 5 is provided with word lines corresponding in the number to scanning lines, to enable to store display data (image signal) in amount of one screen corresponding to the respective dots. Moreover, the row decoder 31 and the memory row decoder 54 are provided to enable selection of a scanning line and word line. Accordingly, a scanning line can be selected and driven randomly according to an address signal without requiring sequential scanning, which is convenient for rewriting display data as required. Also, in order to achieve space saving by simplifying the interconnections and reducing the circuit area, the same address signal is inputted to the row decoder 31 and the memory row decoder 54, respectively causing the corresponding sections to store and display in the same timing. As for the column decoder 51, random pixel selection can be made according to an address signal, random writing can be made without the necessity of sequential writing to the pixels (dots) on the same scanning line.

[0068] In the case of not providing change in display, the digital data of the image signal stored in the frame memory section 5 is used as it is for making display, wherein no data transmission and reception is made to and from the CPU 110A. However, because the LCD

requires alternating-current drive, there is a need of drive using pixel-inversion drive while refreshing at least at a required minimum frequency. This control is made with the scanning line driver 3 and the digital data driver 4. If the frequency is lowered, consumption-power reduction can be made but flicker occurs due to punch-through voltage or the like. Therefore, in order to make flicker not conspicuous while reducing power consumption, the state of display is maintained with refreshing at a frequency, for example, of 30 Hz for still images (liquid crystal driven at 15 Hz).

[0069] As concerned with the frame memory section 5, if the memory cells are constituted by static memories, there is no need to rewrite data (refresh). However, if constituted by dynamic memories, there is a necessity of refreshing in such timing as can hold the storage.

[0070] As above, according to the first embodiment, where a system including not only a display part but also peripheral circuit on a substrate as in SOP is integrally formed on a substrate, in the memory cell section 56 of the frame memory section 5, memory cells are formed to be arranged such that the length in the row direction of arrangement of memory cells with an amount required for controlling one-dot display is smaller than a pitch of dots, i.e., the length in the row direction of the memory cell section 56 is smaller than the length in the row direction of the active-matrix LCD section 2. Accordingly, it is possible to arrange memory cells in amount of one row with saved space width.

[0071] Also, this is similarly made for the sense amplifier section 57 and k-bit DAC section 41, achieving space saving.

[0072] Also, the number of rows of the memory array is given the same as the number of scanning lines (i) to enable the frame memory section 5 to store display data (image signal) in amount of one screen. Accordingly, it is possible to store data in amount of one screen with correspondence between the pixel in each position and the memory cell of the memory cell section 56. The image signal only in amount of display data for a to-be-rewritten pixel is satisfactorily transmitted from the CPU 110A. Accordingly, the data transmission amount over the entire system can be decreased, and space-saved forming can be made with the maximum efficiency while achieving the reduction of power consumption.

[0073] Also, because the row decoder 31 and the memory row decoder 54 are provided to enable selection of a scanning line and word line to be driven on the basis of an address signal, a scanning line can be selected and driven randomly according to an address signal without the necessity of sequential scanning. This is convenient for rewriting display data as required.

[0074] Also, because the same address signal is inputted to the row decoder 31 and the memory row decoder 54 to cause the respective corresponding points to perform storage and display in the same timing, space saving can be made due to simplification of interconnections and reduction of circuit area.

[0075] Also, because the row decoder 51 can randomly select a pixel according to an address signal, random writing can be made without the necessity of sequential writing to the pixels (dots) on the same scanning line. This is convenient for rewriting display data as required.

[0076] Also, because the input control circuit 52 and the column selection switch section 53 are arranged on a side opposite to the active-matrix LCD section 2 sandwiching the memory cell section 56, crossover of interconnections is decreased thus achieving simplicity and consumption-power reduction. Moreover, there occurs no noise superposition over the analog-driven LCD 2 due to operation of the input control circuit 52 and column selection switch section 53, thus reducing noise in display.

[0077] Furthermore, because the memory controller 6 and the timing controller 7 are integrally formed on the panel 1, the panel 1 can be directly coupled to the CPU 110A, thus providing cost reduction, reliability and space saving for the system entirety.

Embodiment 2

[0078] Fig. 3 is a figure showing in detail a panel 1A according to a second embodiment of the invention. The panel 1A of Fig. 3 differs from the panel 1 of Fig. 2 in that address signals are independently inputted to the row decoder 31 and the memory row decoder 54. Due to this, it is possible to make the timing of storage different from the timing of display operations. The drive frequency is higher than that of storage and display operations in simultaneous timing. However, various forms of driving is feasible, e.g., address data is transmitted to the memory row decoder 54 in certain timing to make storage operation, and then address data is transmitted to the row decoder 31 in the next timing to make display.

[0079] As above, according to the second embodiment, because address signals are independently inputted respectively to the row decoder 31 and the memory row decoder 54, it is possible to enhance the freedom for selecting a drive method.

Embodiment 3

[0080] Fig. 4 is a figure showing in detail a panel 1B according to a third embodiment of the invention. The panel 1B of Fig. 4 differs from the panel 1 of Fig. 2 in that a scanning line-select-control signal line and a word line-select-control signal line are respectively laid from the address buffer 71 to the row decoder 31A and the memory row decoder 54A, to transmit a scanning line-select-control signal and a word-line-select-control signal. The same address signal is inputted to the row decoder 31A and the memory row decoder 54A. However, the row decoder 31A is allowed to select a scanning line only during the period that a scanning line-select-control signal is on. Also, the memory row decoder 54A similarly is allowed to select a word line only during the period that

a word-line-select-control signal is on. Consequently, storage and display operations can be made in different timing depending upon control of on-off of these signals.

[0081] As above, according to the third embodiment, the scanning line-select period of the row decoder 31A is limited on the basis of the scanning line-select-control signal and the word-line-select period of the memory row decoder 54A is limited on the basis of the word-line-select-control signal. Therefore, it is possible to enhance the freedom for selecting a drive method for storage and display operations. Accordingly, various ones of drive control are feasible depending on the method.

Embodiment 4

[0082] Fig. 5 is a figure representing in detail a panel 1C according to a fourth embodiment of the invention. The panel 1C of Fig. 5 differs from the panel 1B of Fig. 4 in that a column selection switch section 53A, a sense amplifier section 57A and memory cell section 56A are laid out taking into account a case such as k = 6. Also, the column decoder 51A and the input control circuit 52A respectively deal with signals in two times due to k = 6, as compared to the column decoder 51 and the input control circuit 52 (besides this, different from the panel 1 of Fig. 2 in that there are a scanning line-select-control signal line and a word-line-select-control signal line). As described before, if the memory cells are arranged such that the length in the row direction of the memory cell section 56 is smaller than the length in the row direction of the active-matrix LCD section 2, then the memory cells in one column can be arranged most efficiently with a saved space width. Accordingly, it is ideal to arrange the memory cells in amount of k bits in the row direction to have a length smaller than the pitch of dots. However, if increasing the tonal level, the value of k increases (64 tonal levels at k = 6, display possible in about 260 thousand colors). That is, there is an increase in the number of memory cells to store 1-dot data. Due to this, it is to be considered that the arrangement of memory cells in amount of k bits as they are will exceed the pitch of dots. Accordingly, the present embodiment has a memory array in a multi-stage configuration in the memory cell section 56A, wherein the memory cells are laid out and integrally formed to have such an arrangement that the length in the row direction of the memory cell section 56A is smaller than the length in the row direction of the active-matrix LCD section 2.

[0083] Meanwhile, it is to be considered as another way of thinking that the number of memory-array rows is provided integer times the number of scanning lines to constitute a 1-dot memory cells in a plurality of rows. In this case, the k-bit DAC section 41 time-division-processes digital data to drive the data line.

[0084] As above, according to the fourth embodiment, where the length of arrangement of k-bit memory cells in the row direction cannot be given smaller than the pitch of dots, the memory array is made in a multi-stage configuration to have layout and integral formation such that the length in the row direction of the memory cell section 56A is smaller than the length in the row direction of the active-matrix LCD section 2. Accordingly, it is possible to facilitate interconnections between the memory cell section 56A and the k-bit DAC section 41. Thus, space saving can be achieved.

Embodiment 5

[0085] Fig. 6 is a figure representing in detail a panel 1D according to a fifth embodiment of the invention. The panel 1D of Fig. 6 differs from the panel 1B of Fig. 4 in arrangement of memory cells in the memory cell section 56B, and in that the image signals for two pixels are simultaneously inputted so that the column decoder 51B can select two pixels simultaneously. Furthermore, the input control circuit 52A and the column selection switch section 53A respectively deal with signals in two times as compared to the input control circuit 52 and the column selection switch section 53A.

[0086] The fourth embodiment explained on the case that the length of arrangement of memory cells in amount of k bits is longer than the pitch of pixels. Conversely, the length of arrangement of memory cells in amount of plurality of pixels (dots) is smaller than the pitch of one pixel (dot), it is possible to further save the space by laying out and integrally forming the memory cells in amount of a plurality of pixels (dots) arranged corresponding to the one-pixel (dot) pitch. However, in this case, the same number of word lines as the scanning lines are provided to provide memory cells , corresponding to the dots without sharing the word lines. It is noted that in this case the sense amplifier section 57 can be shared.

[0087] Also, in the first to fourth embodiments the row decoder 51 was configured to select one pixel, as in Fig. 2 to Fig. 5. However, the present invention is not limited to this but may be made to select integer-times simultaneously. In this case, the image signal is inputted in proportion to the multiple.

[0088] As above, according to the fifth embodiment, where the length of arrangement with memory cells in amount of plurality of pixels (dots) is smaller than the length of one-pixel (dot) pitch, the memory cells in amount of plurality of pixels (dots) are laid out and integrally formed by arrangement corresponding to the one-pixel pitch. Accordingly, space saving can be further achieved. Moreover, the sense amplifier section 57 can be shared. Also, because the column decoder 51B can select two pixels simultaneously, the drive frequency can be lowered and power-consumption reduction be achieved despite interconnection is complicate. Also, sufficient operation is obtained even if driven by the active elements inferior in characteristic to the single-crystal FETs.

Embodiment 6

[0089] Fig. 7 is a figure representing in detail a panel

1E according to a sixth embodiment of the invention. The panel 1E of Fig. 7 differs from the panel 1 of Fig. 2 in that the section for actual display is made as a digital-compatible active-matrix OEL section 8 as a display drive section and in that the k-bit DAC section 41 is not used.

[0090] OEL (organic Electro Luminescent) means an organic EL element. This OEL element is a spontaneous luminescent device different from liquid crystal. Consequently, the device has the following features and is expected in the display field and other fields.

(1) wide view angle
(2) reduction of weight and thickness feasible
(3) high contrast ratio
(4) low power consumption (back light not required)
(5) multi-color feasible due to molecular design
(6) high-definition display feasible owing to current drive

[0091] Fig. 8 is a figure showing a circuit arrangement of an active-matrix OEL section 8. Fig. 8 shows an arrangement with two pixels. As described before, LCD requires alternating-current drive for the purpose of extending the life of liquid crystal. Consequently, analog conversion is generally implemented without using digital data as it is. Where making OEL luminous, usually digital data is analog-converted, e.g. two transistor scheme is used to hold the converted analog signal (data) on a capacitance or the like. The output current of the transistor is controlled with the converted analog data to control the luminescence of OEL. It is noted that OEL is driven on direct current (DC drive). On the other hand, as shown in Fig. 8, it is possible to deal with digital data such as an image signal, as it is, stored on each memory.

[0092] Next, explanation will be made on a method for displaying display data stored on the frame memory by exemplifying the dot of R1 (R of a pixel on the first column). R1 is provided with seven OEL elements to display eight tone levels. The seven OEL elements are grouped with one OEL element, two OEL elements and four OEL elements respectively, connected to R1S, R1T and R1U corresponding to each bit line. The difference in tonal level is expressed by luminescent area. Accordingly, at tonal level 0, R1S, R1T and R1U are not driven so as not to emit at any of the elements. At tonal level 1, R1S is driven to make one OEL element luminous. Similarly, at tonal level 2, R1T is driven to make two OEL elements luminous, and at tonal level 3, R1S and R1T are driven to make three OEL elements luminous. Tonal level is represented by the combination of them. This is true for the dots of G and B.

[0093] Herein, OEL may be DC driven, and refresh due to inversion drive is usually unnecessary where change in displaying is not required. It is noted that a dynamic circuit is used in Fig. 8. Accordingly, even if there is no change in displaying, there is need to maintain displaying by refreshing at a constant time interval on the basis of the data stored in each memory cell in the frame memory section 5.

[0094] Although Fig. 7 describes corresponding to Fig. 2 as the first embodiment, it is needless to say that the active-matrix OEL section 8 is applicable to the display devices employing the respective panels of the second to fifth embodiments.

[0095] Also, although the sixth embodiment shows the example to implement digital drive due to so-called area tonal level, it may be, for example, in an arrangement to make digital drive by time-division drive or an arrangement to make digital drive by the combination of area tonal level and time-division drive. In order to provide time-division drive, on-off signals may be applied, in synchronism with a timing signal repeated with a constant period, to the OEL elements in periods different on a bit-by-bit basis corresponding to the digital signal on each bit of each pixel.

[0096] As above, according to the sixth embodiment, because OEL element as spontaneous luminescent device is used for display, it is possible not only to obtain the effects of the first to fifth embodiments but also to reduce power consumption and weight due to unnecessity of back light. Moreover, because tonal representation is feasible by using the digital data to be stored in the frame memory section 5 , as it is, without analog conversion, there is no need to use such a circuit as DAC. The peripheral circuit can be saved in space and reduced in power consumption.

Embodiment 7

[0097] Fig. 9 is a figure representing in detail a panel 1F according to a seventh embodiment of the invention. The panel 1F of Fig. 9 differs from the panel 1E of Fig. 7 in that the section for actual display is made as an active-matrix LCD section 2A as a display drive section.

[0098] Incidentally, the panel 1F of Fig. 9 differs from the panel 1 of Fig. 2 in that the section for actual display is made as a digital-compatible active-matrix LCD section 2A and in that the k-bit DAC section 41 is not employed.

[0099] Fig. 10 is a figure showing a circuit arrangement of the active-matrix LCD section 2A. Fig. 10 shows an arrangement with two pixels. As described before, because LCD requires alternate-current drive for the purpose of extending the life of liquid crystal, analog conversion is generally made without using digital data as it is. The configuration of Fig. 10 is made to deal with digital data such as the image signal stored on each memory cell, as it is, as hereinafter described.

[0100] Next, a method for displaying the display data stored in the frame memory will be explained by exemplifying the dot of R1 (R on the first column pixel). R1 has three liquid crystal regions respectively covered with independent pixel electrodes in order to represent eight tonal levels. The three liquid crystal regions are in area ratio of 1: 2: 4 and connected to R1S, R1T and R1U corresponding to each bit line. Meanwhile, the region of the active-matrix LCD section 2A other than the liquid

crystal regions, i.e. the entire region excepting the pixel electrodes, are shaded. Accordingly, the difference of tonal level is represented as an area of the liquid crystal region in a transmissive state. Hence, at tonal level 0, R1S, R1T and R1U are not driven to make every liquid crystal region in a shade state. At tonal level 1, R1S is driven to make the liquid crystal region of the area ratio 1 in a transmissive state. Similarly, at tonal level 2, R1T is driven to make the liquid crystal region of the area ratio 2 in a transmissive state, and at tonal level 3, R1S and R1T are driven to make the liquid crystal regions of the area ratio 1 and area ratio 2 in a transmissive state. Tonal level is represented by this combination. This is true for the dots of G and B.

[0101] In this embodiment, a rectangular wave is supplied to the common feed line VLC to apply voltage to each liquid crystal region. The voltage of the rectangular wave to be supplied to the common feed line VLC is a voltage that positive and negative potentials can completely raise the liquid crystal. Also, the frequency of the rectangular wave is the same as the frequency of an alternating-current drive in the usual liquid crystal display device. This realizes a digital-compatible active-matrix LCD section 2A.

[0102] Incidentally, because Fig. 10 of the present embodiment uses a dynamic circuit similarly to Fig. 8 of the sixth embodiment, there is a need to sustain displaying by refreshing at a constant time interval on the basis of the data stored on each memory cell of the frame memory section 5.

[0103] Although Fig. 9 describes corresponding to Fig. 2 as the first embodiment, it is needless to say that the digital-compatible active-matrix LCD section 2A is applicable to the display devices employing the respective panels of the second to fifth embodiments.

[0104] Although the seventh embodiment explained the arrangements or the like on the assumption of the transmissive type LCD, the similar idea is applicable even in a reflective type LCD. In a reflective type LCD, because the devices can be arranged at an underside of the pixel electrodes, more complicated circuit will be feasible and advantageous for achieving multi-bit.

[0105] Also, although the seventh embodiment shows the example to implement digital drive due to so-called area tonal level, it may be, for example, in an arrangement to make digital drive by time-division drive or an arrangement to make digital drive by the combination of area tonal level and time-division drive. In order to provide time-division drive, on-off signals may be applied, in synchronism with a timing signal repeated with a constant period, to the liquid crystal in periods different on a bit-by-bit basis corresponding to the digital signal on each bit of each pixel.

[0106] As above, according to the seventh embodiment, because the digital data to be stored in the frame memory section 5 can be used as it is without analog conversion to provide tonal representation, there is no need to use such a circuit as DAC. The peripheral circuit can be saved in space and reduced in power consumption.

Embodiment 8

[0107] Incidentally, although the above embodiments explained on the assumption of the color display, the present invention can cope with a monochromatic display.

INDUSTRIAL APPLICABILITY

[0108] As above, according to the invention of claim 1, where integral formation is made using TFTs including a peripheral circuit for example on polysilicon, memory cells of the memory cell section in the number capable of storing an image signal for display control of at least the dots on one row of the active matrix display section were allocated corresponding to a length in the row direction of the active matrix display section, besides the column decoder section, column selection switch section and data line driver section (e.g. the column decoder section, column selection switch section, data line driver and memory cell section allocated to have a row length smaller than the length in the row direction of the active matrix display section). Accordingly, the memory cells in one row can be efficiently arranged in a space-saved width.

[0109] Also, according to the invention of the characterizing portion of claim 1, even if structuring redundantly in the number of the memory cells in the number capable of storing the image signal for display control of the dots on one row of the active matrix display section, they are allocated on the basis of the length in the row direction of the display section (e.g. to have a length in the row direction smaller than the length in the row direction of the active matrix display section). Accordingly, the space-saved width can be achieved with efficiency.

[0110] Also a multi-stage structure is given in the structure and the formation. Accordingly, even where the memory cell cannot be allocated corresponding to the length in the row direction of the active matrix display section because, for example, of increase in the memory cell in amount of one dot due to increase in the number of tonal levels, the interconnections can be facilitated and space saving be achieved.

[0111] Also, according to the invention of claim 2, a word line driver section for selecting and driving the word lines provided in the number equal to the scanning lines is further integrated on and being formed integrally with the substrate, and the memory cell section is structured by a memory array corresponding to the dot arrangement of the active matrix display section, to store an image signal required for display over one screen. Accordingly, external exchange of data amount is decreased, achieving reduction in power consumption.

[0112] Also, according to the invention of claim 3, the scanning line driver section and word line driver section is made to select a scanning line and word line to be

driven on the basis of an address signal. Accordingly, no sequential scanning is required, and random selection and drive of the scanning line can be made in accordance with the address signal. This is convenient in rewriting display data as required.

[0113] Also, according to the invention of claim 4, because the same lines are shared in the scanning line driver section and the word line driver section, it is possible to achieve space saving due to simplification of interconnections and reduction in circuit area.

[0114] Also, according to the invention of claim 5, because independent address signals are inputted to the scanning line driver section and the word line driver section, it is possible to enhance the freedom in storage and display operations.

[0115] Also, according to the invention of claim 6, scanning line driver section operates to select and drive the scanning line on the basis of the address signal only when a scanning line driver control signal is inputted and the word line driver section operates to select and drive the word line on the basis of the address signal only when a word line driver control signal is inputted. Accordingly, it is possible to enhance the freedom in selecting a driving way of storage and display operations. Due to this, a variety of drive control is feasible depending on the method.

[0116] Also, according to the invention of claim 7, the column decoder section is made to randomly select a memory cell to store an image signal due to the address signal. Accordingly, there is no need to write sequentially onto the dots on the same scanning line, and random writing can be made. This is convenient in rewriting display data as required.

[0117] Also, according to the invention of claim 8, image signals are inputted on one-pixel-unit basis, based on an input of which the column decoder section selects a memory cell in amount of one pixel as a display-change unit thus being convenient.

[0118] Also, according to the invention of claim 9, image signals are inputted on a plurality-of-pixel-unit basis, wherein the column decoder section selects a memory cell in amount of a plurality of pixels based on an input thereof. Accordingly, interconnections may be complicated but drive frequency can be decreased thus achieving reduction in power consumption. Also, sufficient operation is available if driving with the active element inferior in characteristic to single crystal FET.

[0119] Also, according to the invention of claim 10, the image-signal-input interconnection and column selection switch section are formed on a side opposite to the active matrix display section sandwiching the memory cell section. Accordingly, it is possible to achieve the reduction in power consumption by decreasing the crossover of interconnections and prevent superposition of noise on the display screen due to the effects of switching or the like.

[0120] Also, according to the invention of claim 11, the structure is made by a plurality of rows. Accordingly, where the memory cell cannot be allocated corresponding to the length in the row direction of the active matrix display section because, for example, of increase in the memory cell in amount of one dot due to increase in the number of tonal levels, it is possible to suppress the length in the row direction despite the length in the column direction broadens.

[0121] Also, according to the inventions of claim 12, where a plurality of rows of memory cells can be allocated corresponding to the length in the row direction of the active matrix display section, the memory cells in the number capable of storing an image signal for display control of a plurality of rows of dots of the active matrix display section are structured by a memory array allocated corresponding to the length in the row direction of the active matrix display section (e.g. the memory cells allocated to have a length in the row direction smaller than the length in the row direction of the active matrix display section). Accordingly, space saving is further achieved.

[0122] Also, according to the invention of claim 13, a timing controller section for controlling timing of transmitting the address signal and a memory controller section for controlling to transmit the image signal are further integrated on the substrate and integrally formed therewith, to systematically, integrally forming all the peripheral circuit required for display control on the same substrate. Accordingly, the system entirety can be made at low cost, reliable and space-saved.

[0123] Also, according to the invention of claim 14, a D/A converter is provided between the active matrix display section and the memory cell section to supply the image signal converted into an analog signal to the active matrix display section. Accordingly, display can be made by the active matrix display section compatible with analog signals.

[0124] Also, according to the inventions of claim 15, the active matrix display section and the memory cell section are directly coupled together to directly supply an image signal comprising a digital signal to the active matrix display section. Accordingly, display can be made by the active matrix display section compatible with digital signals, and consumption power can be reduced.

Claims

1. A display device comprising:

an active matrix display section (2) having a plurality of scanning lines extending in a row direction of the active matrix display section;
a plurality of data lines formed in a grid form, whereby in the grid the intersections of a scanning line with a data line corresponds to dots which are the smallest controllable units of display;
a plurality of active elements located at each in-

tersection of a scanning line with a data line;
a scanning line driver section (3) arranged to drive said plurality of scanning lines;
a data line driver (4) arranged to drive the plurality of data lines;
a plurality of memory cells (56) arranged in a matrix having a plurality of rows and a plurality of columns;
a column decoder section (51) arranged to select said memory cells for storing an input image signal; and
a selection switch section (53) arranged to control transmission of first image signals to the plurality of memory cells (56),
the active matrix display section (2), the plurality of memory cells (56) and the selection switch section (53) being formed on one substrate, the plurality of memory cells (56) being formed between the active matrix display section (2) and the selection switch section (53),
the plurality of memory cells (56) being arranged such that the plurality of memory cells (56) store first image signals supplied through the selection switch (53), and
the display device being arranged such that second image signals that are generated based on the first image signals are supplied to one data line of the plurality of data lines,
wherein the number of said plurality of memory cells (56) is sufficient to store an image signal for display control of all of the dots on one row of the active matrix display section (2) and,
wherein the plurality of memory cells (56) is allocated to have a row length that is smaller than the length in the row direction of said active matrix display section (2) and is formed in a multistage structure.

2. The display device according to claim 1, wherein said memory cell section (56) connects said memory cells in the number capable of storing an image signal for display control of the one-row dots to each of word lines in the number equal to the number of said scanning lines and is structured with a memory array corresponding to dot arrangement of said active matrix display section (2), and
a word line driver section (55) for selecting and driving said word lines being further integrated on and integrally formed with said substrate.

3. The display device according to claim 2, wherein, on the basis of an address signal representative of a display position and a storage position, said scanning line driver section (3) selects said scanning lines and said word line driver section (55) selects said word lines.

4. The display device according to claim 3, wherein the same address signal is inputted to said scanning line driver section (3) and said word line driver section (55).

5. The display device according to claim 3, wherein independent address signals are inputted to said scanning line driver section (3) and said word line driver section (55).

6. The display device according to claim 3, wherein said scanning line driver section (3) operates to select and drive said scanning lines on the basis of the address signal only when a scanning line driver control signal is inputted, and said word line driver section (55) operates to select and drive said word lines on the basis of the address signal only when a word line driver control signal is inputted.

7. The display device according to claim 3, wherein said column decoder section (51) selects the memory cell to store an inputted image signal on the basis of the address signal.

8. The display device according to claim 7, wherein one pixel comprises three dots provided for displaying red, blue and green as light source colors, the image signal is inputted on the basis of a unit of one-pixel, and said column decoder section (51) selects the memory cell in an amount of one pixel.

9. The display device according to claim 7, wherein one pixel comprises three dots provided for displaying red, blue and green as light source colors, the image signal is inputted on the basis of a unit of a plurality of pixels, and said column decoder section (51) selects the memory cell in an amount of a plurality of pixels.

10. The display device according to claim 1, wherein an input interconnection for the image signal to be stored in said memory cell and said column selection switch section (53) are formed on a side opposite to said active matrix display section (2) sandwiching said memory cell section (56) therebetween.

11. The display device according to claim 1, wherein said memory cell section connects said memory cells in the number capable of storing an image signal for display control of the one-row dots to each of word lines, and said word lines are provided in the number of integer times the number of the scanning lines, and said memory cell section (56) is structured by a memory array connecting, by grouping, the memory cells in the number capable of storing the image signal for display control of the one-row dots of said active matrix display section (2) to the word lines in the number of the integer times.

12. The display device according to claim 1, wherein said memory cell section (56) is structured by a memory array having the memory cells that are in the number capable of storing the image signal for display control of a plurality of rows of the dots of said active matrix display section (2).

13. The display device according to any one of claims 3 to 12 further comprising:

a timing controller section (7) for controlling timing of transmitting the address signal, and
a memory controller section (6) for controlling to transmit the first image signal,
integrated on a semiconductor or an insulating substrate and integrally formed therewith.

14. The display device according to claim 1, wherein a D/A converter is provided between said active matrix display section (2) and said memory cell section (56) for converting the first image signal comprising a digital signal stored in the memory cell into an analog signal, followed by supplying to said active matrix display section (2).

15. The display device according to claim 1, wherein said active matrix display section (2) and said memory cell section (56) are directly coupled to supply the image signal comprising a digital signal stored in said memory cell section (56) to said active matrix display section (2).

16. The display device according to claim 15 wherein said active matrix display section (2) performs digital drive through area tonal level, time-division tonal level or a combination thereof.

Patentansprüche

1. Anzeigevorrichtung, umfassend:

einen Aktivmatrix-Anzeigeabschnitt (2) mit mehreren Abtastleitungen, die sich in eine Reihenrichtung des Aktivmatrix-Anzeigeabschnitts erstrecken;
mehrere Datenleitungen, die in einer Gitterform gebildet sind;
wobei in dem Gitter die Schnittpunkte einer Abtastleitung mit einer Datenleitung Punkten entsprechen, die die kleinsten steuerbaren Anzeigeeinheiten sind;
mehrere aktive Elemente, die sich an jedem Schnittpunkt einer Abtastleitung mit einer Datenleitung befinden;
einen Abtastleitungstreiberabschnitt (3), der zum Ansteuern der mehreren Abtastleitungen ausgebildet ist;
einen Datenleitungstreiber (4), der zum Ansteuern der mehreren Datenleitungen ausgebildet ist;
mehrere Speicherzellen (56), die in einer Matrix mit mehreren Reihen und mehreren Spalten angeordnet sind;
einen Spaltendekodierabschnitt (51), der zum Auswählen der Speicherzellen zum Speichern eines eingegebenen Bildsignals ausgebildet ist; und
einen Wählschalterabschnitt (53), der zum Steuern der Übertragung erster Bildsignale zu den mehreren Speicherzellen (56) ausgebildet ist,
wobei der Aktivmatrix-Anzeigeabschnitt (2), die mehreren Speicherzellen (56) und der Wählschalterabschnitt (53) auf einem Substrat gebildet sind, wobei die mehreren Speicherzellen (56) zwischen dem Aktivmatrix-Anzeigeabschnitt (2) und dem Wählschalterabschnitt (53) gebildet sind,
wobei die mehreren Speicherzellen (56) so angeordnet sind, dass die mehreren Speicherzellen (56) erste Bildsignale speichern, die durch den Wählschalter (53) zugeleitet werden, und
die Anzeigevorrichtung so angeordnet ist, dass zweite Bildsignale, die auf der Basis der ersten Bildsignale erzeugt werden, einer Datenleitung der mehreren Datenleitungen zugeleitet werden,
wobei die Anzahl der mehreren Speicherzellen (56) ausreichend ist, um ein Bildsignal zur Anzeigesteuerung aller der Punkte einer Reihe des Aktivmatrix-Anzeigeabschnitts (2) zu speichern, und
wobei die mehreren Speicherzellen (56) so zugeordnet sind, dass sie eine Reihenlänge aufweisen, die kleiner als die Länge in der Reihenrichtung des Aktivmatrix-Anzeigeabschnitts (2) ist, und mit einer mehrstufigen Struktur gebildet sind.

2. Anzeigevorrichtung nach Anspruch 1, wobei der Speicherzellenabschnitt (56) die Speicherzellen in der Anzahl verbindet, dass sie ein Bildsignal zur Anzeigesteuerung der einreihigen Punkte für jede der Wortleitungen in der Anzahl speichern können, die der Anzahl der Abtastleitungen gleich ist, und mit einer Speicheranordnung gestaltet ist, die einer Punktanordnung des Aktivmatrix-Anzeigeabschnitts (2) entspricht, und
ein Wortleitungstreiberabschnitt (55) zum Selektieren und Ansteuern der Wortleitungen des Weiteren auf dem Substrat integriert und integral mit diesem gebildet ist.

3. Anzeigevorrichtung nach Anspruch 2, wobei auf der Basis eines Adresssignals, das für eine Anzeigepo-

sition und eine Speicherposition repräsentativ ist, der Abtastleitungstreiberabschnitt (3) die Abtastleitungen wählt und der Wortleitungstreiberabschnitt (55) die Wortleitungen wählt.

4. Anzeigevorrichtung nach Anspruch 3, wobei dasselbe Adresssignal in den Abtastleitungstreiberabschnitt (3) und den Wortleitungstreiberabschnitt (55) eingegeben wird.

5. Anzeigevorrichtung nach Anspruch 3, wobei unabhängige Adresssignale in den Abtastleitungstreiberabschnitt (3) und den Wortleitungstreiberabschnitt (55) eingegeben werden.

6. Anzeigevorrichtung nach Anspruch 3, wobei der Abtastleitungstreiberabschnitt (3) zum Selektieren und Ansteuern der Abtastleitungen auf der Basis nur des Adresssignals arbeitet, wenn ein Abtastleitungstreiber-Steuersignal eingegeben wird, und der Wortleitungstreiberabschnitt (55) zum Selektieren und Ansteuern der Wortleitungen auf der Basis nur des Adresssignals arbeitet, wenn ein Wortleitungstreiber-Steuersignal eingegeben wird.

7. Anzeigevorrichtung nach Anspruch 3, wobei der Spaltendekodierabschnitt (51) die Speicherzelle zum Speichern eines eingegebenen Bildsignals auf der Basis des Adresssignals wählt.

8. Anzeigevorrichtung nach Anspruch 7, wobei ein Pixel drei Punkte umfasst, die zum Anzeigen von Rot, Blau und Grün als Lichtquellenfarben vorgesehen sind, wobei das Bildsignal auf der Basis einer Einheit von einem Pixel eingegeben wird und der Spaltendekodierabschnitt (51) die Speicherzelle in einer Menge eines Pixels wählt.

9. Anzeigevorrichtung nach Anspruch 7, wobei ein Pixel drei Punkte umfasst, die zum Anzeigen von Rot, Blau und Grün als Lichtquellenfarben vorgesehen sind, wobei das Bildsignal auf der Basis einer Einheit von mehreren Pixeln eingegeben wird und der Spaltendekodierabschnitt (51) die Speicherzelle in einer Menge von mehreren Pixeln wählt.

10. Anzeigevorrichtung nach Anspruch 1, wobei eine Eingangsverbindung für das Bildsignal, das in der Speicherzelle gespeichert werden soll, und der Spaltenwählschalterabschnitt (53) an einer Seite gebildet sind, die dem Aktivmatrix-Anzeigeabschnitt (2) gegenüber liegt, während der Speicherzellabschnitt (56) dazwischen liegt.

11. Anzeigevorrichtung nach Anspruch 1, wobei der Speicherzellenabschnitt die Speicherzellen in der Anzahl verbindet, die zum Speichern eines Bildsignals zur Anzeigesteuerung der einreihigen Punkte zu jeder der Wortleitungen notwendig sind, und die Wortleitungen in der Anzahl von ganzen vielfachen der Anzahl der Abtastleitungen vorgesehen sind, und der Speicherzellenabschnitt (56) durch eine Speicheranordnung gestaltet ist, die durch Gruppierung die Speicherzellen in der Anzahl verbindet, die zum Speichern des Bildsignals zur Anzeigesteuerung der einreihigen Punkte des Aktivmatrix-Anzeigeabschnitts (2) zu den Wortleitungen in der Anzahl ganzer Vielfacher imstande sind.

12. Anzeigevorrichtung nach Anspruch 1, wobei der Speicherzellenabschnitt (56) aus einer Speicheranordnung gebildet ist, die die Speicherzellen in der Anzahl aufweist, die zum Speichern des Bildsignals zur Anzeigesteuerung mehrerer Reihen der Punkte des Aktivmatrix-Anzeigeabschnitts (2) imstande ist.

13. Anzeigevorrichtung nach einem der Ansprüche 3 bis 12, des Weiteren umfassend:

einen Zeitsteuerungsabschnitt (7) zum Steuern des Zeitverlaufs der Übertragung des Adresssignals, und
einen Speichersteuerungsabschnitt (8) zum Steuern der Übertragung des ersten Bildsignals, integriert auf einem Halbleiter oder einem isolierenden Substrat und integral mit diesem gebildet.

14. Anzeigevorrichtung nach Anspruch 1, wobei ein D/A-Wandler zwischen dem Aktivmatrix-Anzeigeabschnitt (2) und dem Speicherzellenabschnitt (56) zum Umwandeln des ersten Bildsignals, das ein digitales Signal umfasst, das in der Speicherzelle gespeichert ist, in ein analoges Signal vorgesehen ist, gefolgt von der Zuleitung zu dem Aktivmatrix-Anzeigeabschnitt (2).

15. Anzeigevorrichtung nach Anspruch 1, wobei der Aktivmatrix-Anzeigeabschnitt (2) und der Speicherzellenabschnitt (56) zum Zuleiten des Bildsignals, das ein digitales Signal umfasst und in dem Speicherzellenabschnitt (56) gespeichert ist, zu dem Aktivmatrix-Anzeigeabschnitt (2) direkt gekoppelt sind.

16. Anzeigevorrichtung nach Anspruch 15, wobei der Aktivmatrix-Anzeigeabschnitt (2) eine digitale Ansteuerung durch Flächentonpegel, Zeitmultiplextonpegel oder eine Kombination davon ausführt.

Revendications

1. Dispositif d'affichage comprenant :

une section d'affichage à matrice active (2) ayant une pluralité de lignes de balayage s'éten-

dant dans une direction de rangée de la section d'affichage à matrice active ;
une pluralité de lignes de données formées en forme de grille,
moyennant quoi, dans la grille, les intersections entre une ligne de balayage avec une ligne de données correspondent à des points qui sont les plus petites unités contrôlables de l'afficheur ;
une pluralité d'éléments actifs situés à chaque intersection entre une ligne de balayage et une ligne de données ;
une section de commande de ligne de balayage (3) étudiée pour commander ladite pluralité de lignes de balayage ;
un dispositif de commande de ligne de données (4) étudié pour commander la pluralité des lignes de données ;
une pluralité de cellules de mémoire (56) disposées en une matrice ayant une pluralité de rangées et une pluralité de colonnes ;
une section de décodage de colonne (51) étudiée pour sélectionner lesdites cellules de mémoire pour stocker un signal d'image d'entrée ; et
une section de commutation de sélection (53) étudiée pour contrôler la transmission de premiers signaux d'image à l'attention de la pluralité des cellules de mémoire (56),
la section d'affichage à matrice active (2), la pluralité des cellules de mémoire (56) et la section de commutation de sélection (53) étant formées sur un substrat, la pluralité des cellules de mémoire (56) étant formées entre la section d'affichage à matrice active (2) et la section de commutation de sélection (53),
la pluralité des cellules de mémoire (56) étant étudiées de manière à ce que la pluralité des cellules de mémoire (56) stockent des premiers signaux d'image fournis par l'intermédiaire du commutateur de sélection (53), et
le dispositif d'affichage étant étudié de manière à ce que des deuxièmes signaux d'image, lesquels sont générés sur la base des premiers signaux d'image, soient fournis à une ligne de données parmi la pluralité des lignes de données,
dans lequel le nombre de ladite pluralité de cellules de mémoire (56) est suffisant pour stocker un signal d'image pour le contrôle d'affichage de tous les points d'une rangée de la section d'affichage à matrice active (2), et
dans lequel la pluralité des cellules de mémoire (56) est destinée à avoir une longueur de rangée qui est plus petite que la longueur en direction de rangée de ladite section d'affichage à matrice active (2) et est formée avec une structure à plusieurs étages.

2. Dispositif d'affichage selon la revendication 1, dans lequel ladite section de cellule de mémoire (56) connecte lesdites cellules de mémoire en un nombre capable de stocker un signal d'image pour le contrôle d'affichage des points d'une rangée à chacune des lignes de mot en un nombre égal au nombre desdites lignes de balayage et est structurée avec un réseau de cellules de mémoire correspondant à un agencement de points de ladite section d'affichage à matrice active (2), et
une section de commande de ligne de mot (55) pour sélectionner et commander lesdites lignes de mot étant par ailleurs intégrée sur ledit substrat et intégralement formée avec celui-ci.

3. Dispositif d'affichage selon la revendication 2, dans lequel, sur la base d'un signal d'adresse représentatif d'une position d'affichage et d'une position de stockage, ladite section de commande de ligne de balayage (3) sélectionne lesdites lignes de balayage et ladite section de commande de ligne de mot (55) sélectionnant lesdites lignes de mot.

4. Dispositif d'affichage selon la revendication 3, dans lequel le même signal d'adresse est introduit dans ladite section de commande de ligne de balayage (3) et ladite section de commande de ligne de mot (55).

5. Dispositif d'affichage selon la revendication 3, dans lequel des signaux d'adresse indépendants sont introduits dans ladite section de commande de ligne de balayage (3) et ladite section de commande de ligne de mot (55).

6. Dispositif d'affichage selon la revendication 3, dans lequel ladite section de commande de ligne de balayage (3) fonctionne de manière à sélectionner et commander lesdites lignes de balayage sur la base du signal d'adresse seulement lorsqu'un signal de contrôle de commande de ligne de balayage est introduit, et ladite section de commande de ligne de mot (55) fonctionnant de manière à sélectionner et commander lesdites lignes de mot sur la base du signal d'adresse seulement lorsqu'un signal de contrôle de commande de ligne de mot est introduit.

7. Dispositif d'affichage selon la revendication 3, dans lequel ladite section de décodage de colonne (51) sélectionne la cellule de mémoire afin de stocker un signal d'image qui est entré sur la base du signal d'adresse.

8. Dispositif d'affichage selon la revendication 7, dans lequel un pixel comprend trois points fournis pour afficher du rouge, du bleu et du vert en tant que couleurs de source de lumière, le signal d'image étant introduit sur la base d'une unité d'un pixel, et ladite

section de décodage de colonne (51) sélectionnant la cellule de mémoire en une quantité de un pixel.

9. Dispositif d'affichage selon la revendication 7, dans lequel un pixel comprend trois points fournis pour afficher du rouge, du bleu et du vert en tant que couleurs de source de lumière, le signal d'image étant introduit sur la base d'une unité d'une pluralité de pixels, et ladite section de décodage de colonne (51) sélectionnant la cellule de mémoire en une quantité d'une pluralité de pixels.

10. Dispositif d'affichage selon la revendication 1, dans lequel une interconnexion d'entrée pour le signal d'image à stocker dans ladite cellule de mémoire et ladite section de commutation de sélection de colonne (53) sont formées d'un côté opposé à ladite section d'affichage à matrice active (2) en prenant en sandwich ladite section de cellule de mémoire (56) entre elles.

11. Dispositif d'affichage selon la revendication 1, dans lequel ladite section de cellule de mémoire connecte lesdites cellules de mémoire en un nombre capable de stocker un signal d'image pour le contrôle d'affichage des points d'une rangée à chacune des lignes de mot, et lesdites lignes de mot étant fournies en un nombre multiple de l'entier du nombre de lignes de balayage, et ladite section de cellule de mémoire (56) étant structurée par un réseau de cellules de mémoire connectant, grâce à un regroupement, les cellules de mémoire en un nombre capable de stocker le signal d'image pour le contrôle d'affichage des points d'une rangée de ladite section d'affichage à matrice active (2) aux lignes de mot en un nombre multiple de l'entier.

12. Dispositif d'affichage selon la revendication 1, dans lequel ladite section de cellule de mémoire (56) est structurée par un réseau de cellules de mémoire ayant les cellules de mémoire qui sont d'un nombre capable de stocker le signal d'image pour le contrôle d'affichage d'une pluralité de rangées des points de ladite section d'affichage à matrice active (2).

13. Dispositif d'affichage selon l'une quelconque des revendications 3 à 12, comprenant par ailleurs :

une section de contrôle de temps (7) pour contrôler le temps de transmission du signal d'adresse, et
une section de contrôle de mémoire (6) pour le contrôle afin de transmettre le premier signal d'image,
intégrées sur un semi-conducteur ou un substrat isolant et intégralement formées avec celui-ci.

14. Dispositif d'affichage selon la revendication 1, dans lequel un convertisseur N/A est fourni entre ladite section d'affichage à matrice active (2) et ladite section de cellule de mémoire (56) pour convertir le premier signal d'image comprenant un signal numérique stocké dans la cellule de mémoire en un signal analogique, avec ensuite la fourniture à ladite section d'affichage à matrice active (2).

15. Dispositif d'affichage selon la revendication 1, dans lequel ladite section d'affichage à matrice active (2) et ladite section de cellule de mémoire (56) sont directement couplées afin de fournir le signal d'image comprenant un signal numérique stocké dans ladite section de cellule de mémoire (56) à l'attention de ladite section d'affichage à matrice active (2).

16. Dispositif d'affichage selon la revendication 15, dans lequel ladite section d'affichage à matrice active (2) effectue une commande numérique par l'intermédiaire d'un niveau tonal de région, un niveau tonal à répartition dans le temps ou une combinaison de ceux-ci .

FIG.1

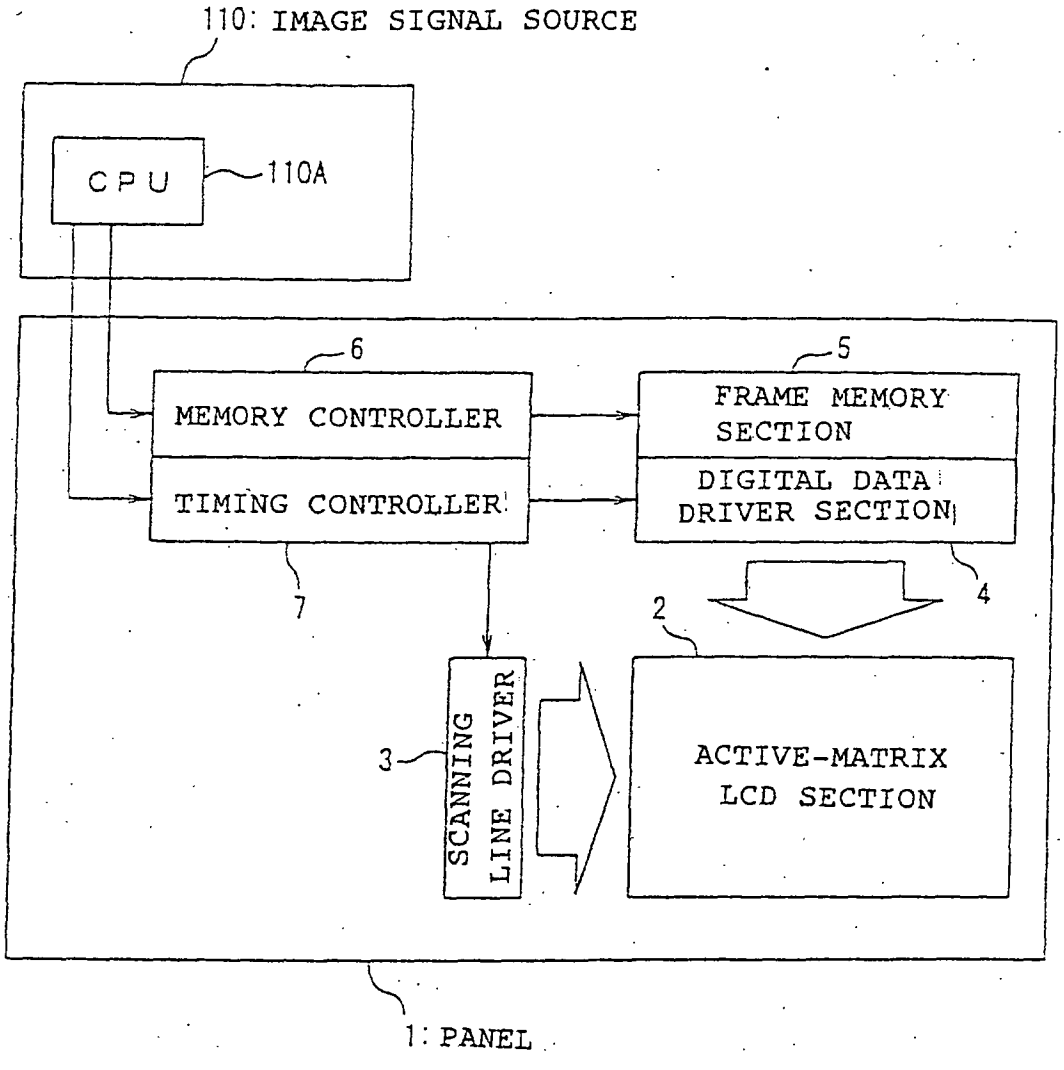

110: IMAGE SIGNAL SOURCE
CPU
110A
6
MEMORY CONTROLLER
TIMING CONTROLLER
7
5
FRAME MEMORY SECTION
DIGITAL DATA DRIVER SECTION
4
2
3
SCANNING LINE DRIVER
ACTIVE-MATRIX LCD SECTION
1: PANEL

FIG.2

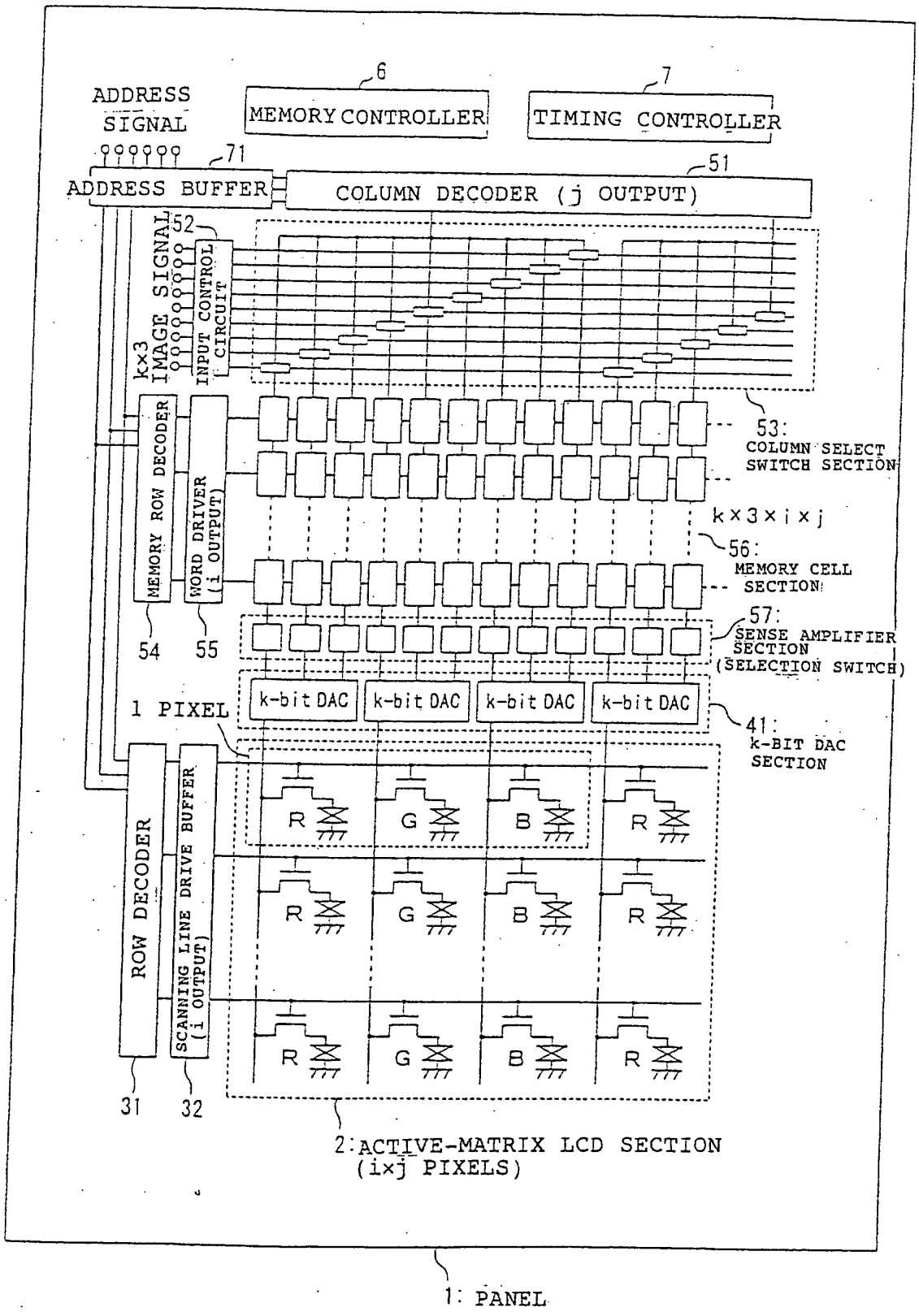

ADDRESS SIGNAL
6
MEMORY CONTROLLER
7
TIMING CONTROLLER
71
ADDRESS BUFFER
51
COLUMN DECODER (j OUTPUT)
52
INPUT CONTROL CIRCUIT
k×3 IMAGE SIGNAL
MEMORY ROW DECODER
WORD DRIVER (i OUTPUT)
53: COLUMN SELECT SWITCH SECTION
k×3×i×j
56: MEMORY CELL SECTION
57: SENSE AMPLIFIER SECTION (SELECTION SWITCH)
54
55
k-bit DAC
k-bit DAC
k-bit DAC
k-bit DAC
41: k-BIT DAC SECTION
1 PIXEL
R
G
B
R
ROW DECODER
SCANNING LINE DRIVE BUFFER (i OUTPUT)
31
32
2: ACTIVE-MATRIX LCD SECTION (ixj PIXELS)
1: PANEL

FIG.3

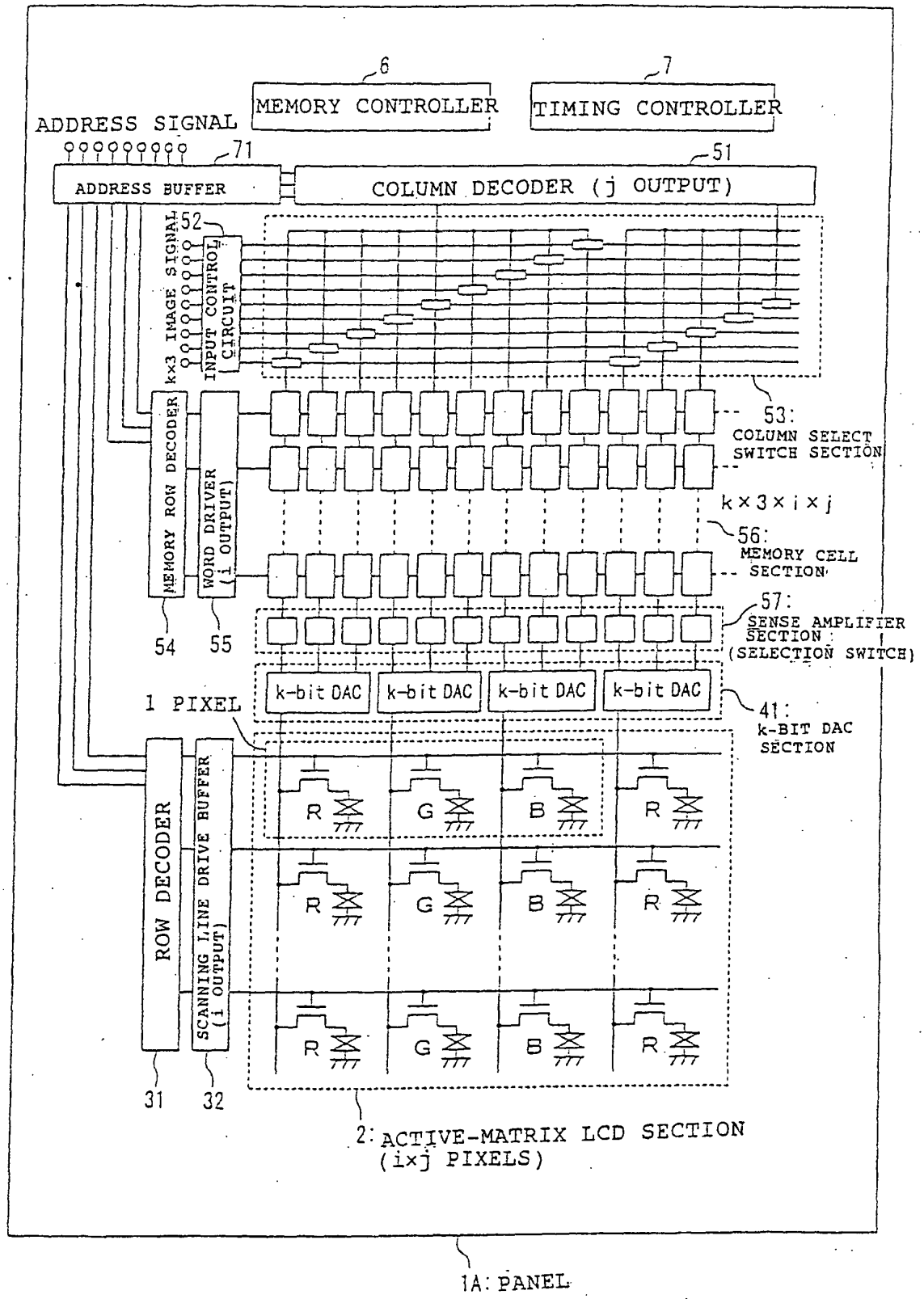

6
MEMORY CONTROLLER
7
TIMING CONTROLLER
ADDRESS SIGNAL
71
ADDRESS BUFFER
51
COLUMN DECODER (j OUTPUT)
52
k×3 IMAGE SIGNAL
INPUT CONTROL CIRCUIT
MEMORY ROW DECODER
WORD DRIVER (i OUTPUT)
53: COLUMN SELECT SWITCH SECTION
k×3×i×j
56: MEMORY CELL SECTION
57: SENSE AMPLIFIER SECTION (SELECTION SWITCH)
54
55
1 PIXEL
k-bit DAC
k-bit DAC
k-bit DAC
k-bit DAC
41: k-BIT DAC SECTION
R
G
B
R
ROW DECODER
SCANNING LINE DRIVE BUFFER (i OUTPUT)
31
32
2: ACTIVE-MATRIX LCD SECTION (i×j PIXELS)
1A: PANEL

FIG.4

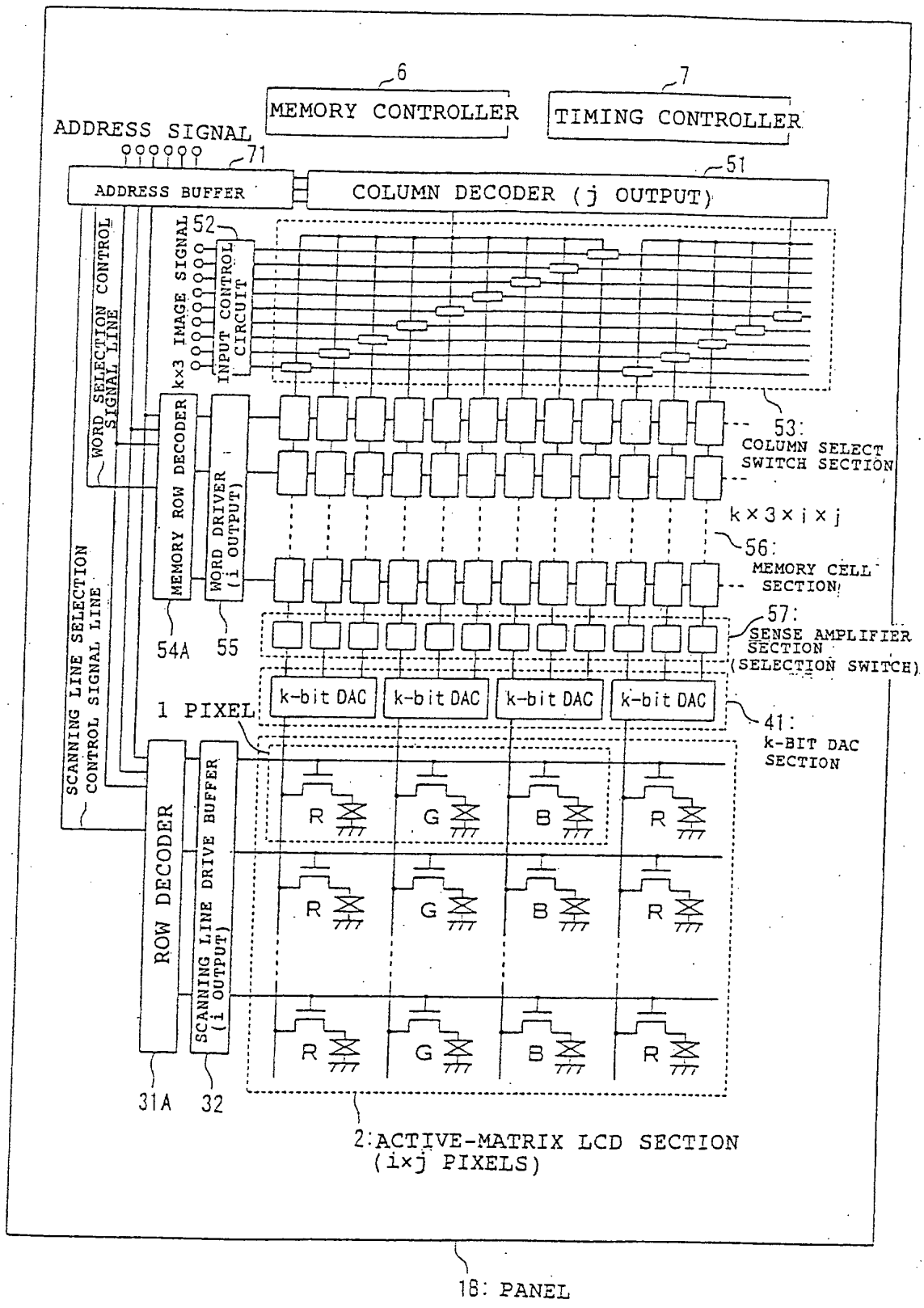

6
MEMORY CONTROLLER
7
TIMING CONTROLLER
ADDRESS SIGNAL
71
ADDRESS BUFFER
51
COLUMN DECODER (j OUTPUT)
52
k×3 IMAGE SIGNAL
INPUT CONTROL CIRCUIT
WORD SELECTION CONTROL SIGNAL LINE
MEMORY ROW DECODER
WORD DRIVER (i OUTPUT)
53: COLUMN SELECT SWITCH SECTION
k×3×i×j
56: MEMORY CELL SECTION
57: SENSE AMPLIFIER SECTION (SELECTION SWITCH)
54A
55
k-bit DAC
k-bit DAC
k-bit DAC
k-bit DAC
41: k-BIT DAC SECTION
1 PIXEL
SCANNING LINE SELECTION CONTROL SIGNAL LINE
ROW DECODER
SCANNING LINE DRIVE BUFFER (i OUTPUT)
R
G
B
R
31A
32
2: ACTIVE-MATRIX LCD SECTION (i×j PIXELS)
18: PANEL

FIG.5

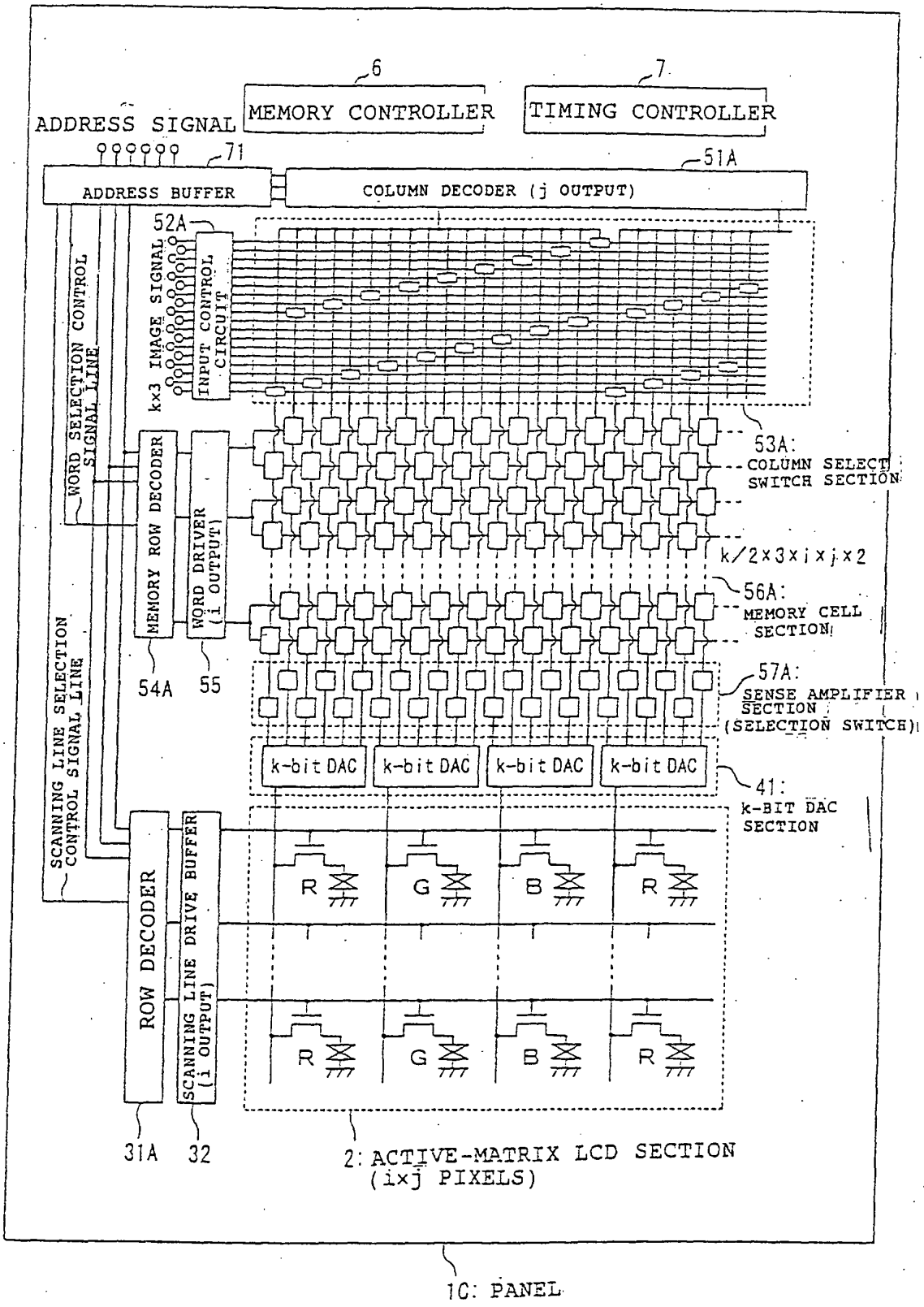

6
MEMORY CONTROLLER
7
TIMING CONTROLLER
ADDRESS SIGNAL
71
ADDRESS BUFFER
51A
COLUMN DECODER (j OUTPUT)
52A
kx3 IMAGE SIGNAL
INPUT CONTROL CIRCUIT
WORD SELECTION CONTROL SIGNAL LINE
MEMORY ROW DECODER
WORD DRIVER (i OUTPUT)
53A:
COLUMN SELECT SWITCH SECTION
k/2x3xixjx2
56A:
MEMORY CELL SECTION
54A
55
57A:
SENSE AMPLIFIER SECTION (SELECTION SWITCH)
k-bit DAC
k-bit DAC
k-bit DAC
k-bit DAC
41:
k-BIT DAC SECTION
SCANNING LINE SELECTION CONTROL SIGNAL LINE
ROW DECODER
SCANNING LINE DRIVE BUFFER (i OUTPUT)
R
G
B
R
R
G
B
R
31A
32
2: ACTIVE-MATRIX LCD SECTION (ixj PIXELS)
1C: PANEL

FIG.6

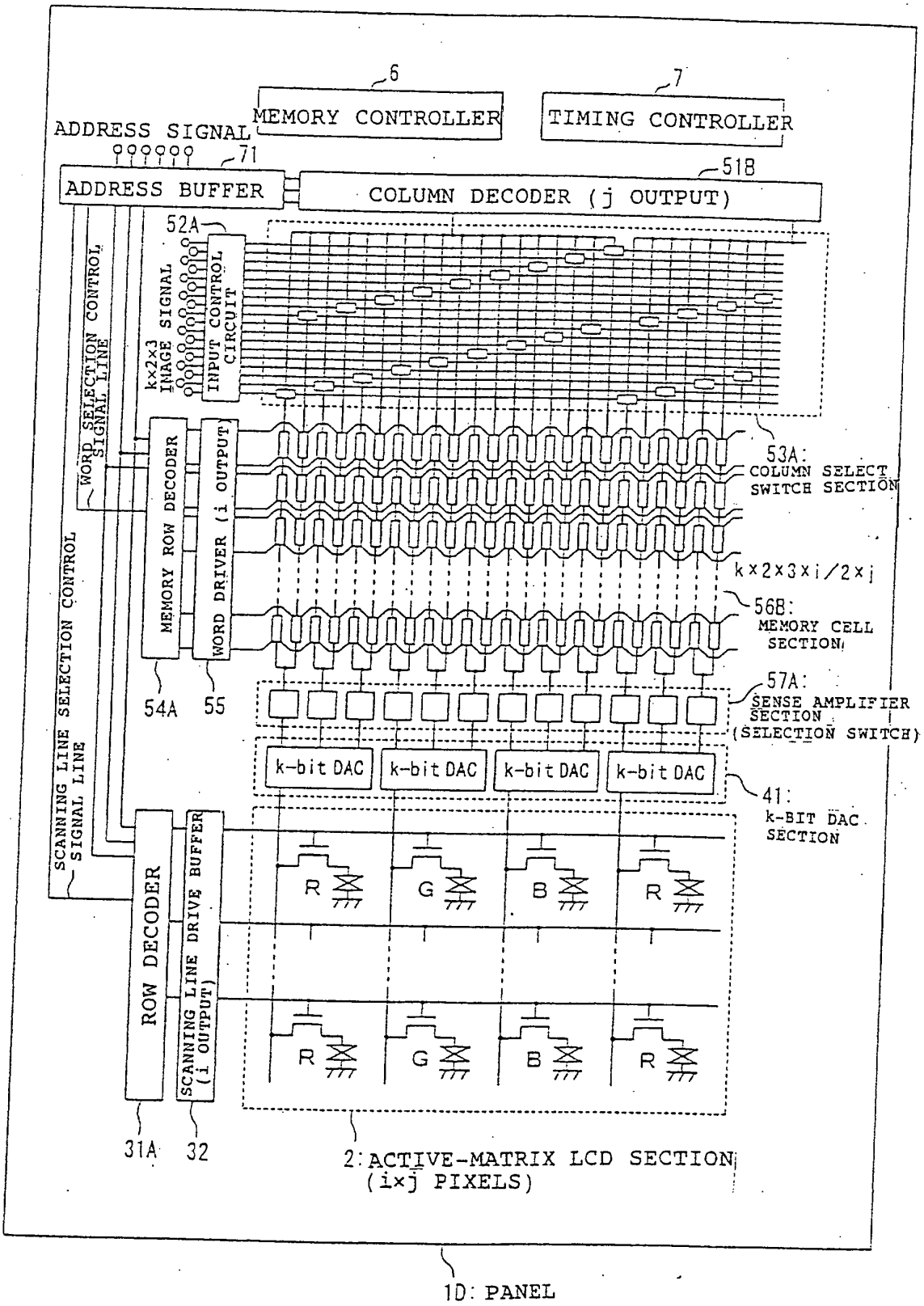

6
MEMORY CONTROLLER
7
TIMING CONTROLLER
ADDRESS SIGNAL
71
ADDRESS BUFFER
51B
COLUMN DECODER (j OUTPUT)
52A
INPUT CONTROL CIRCUIT
k×2×3 IMAGE SIGNAL
WORD SELECTION CONTROL SIGNAL LINE
MEMORY ROW DECODER
WORD DRIVER (i OUTPUT)
53A: COLUMN SELECT SWITCH SECTION
k×2×3×i/2×j
56B: MEMORY CELL SECTION
57A: SENSE AMPLIFIER SECTION (SELECTION SWITCH)
54A
55
SCANNING LINE SELECTION CONTROL SIGNAL LINE
k-bit DAC
k-bit DAC
k-bit DAC
k-bit DAC
41: k-BIT DAC SECTION
ROW DECODER
SCANNING LINE DRIVE BUFFER (i OUTPUT)
R
G
B
R
R
G
B
R
31A
32
2: ACTIVE-MATRIX LCD SECTION (i×j PIXELS)
1D: PANEL

FIG.7

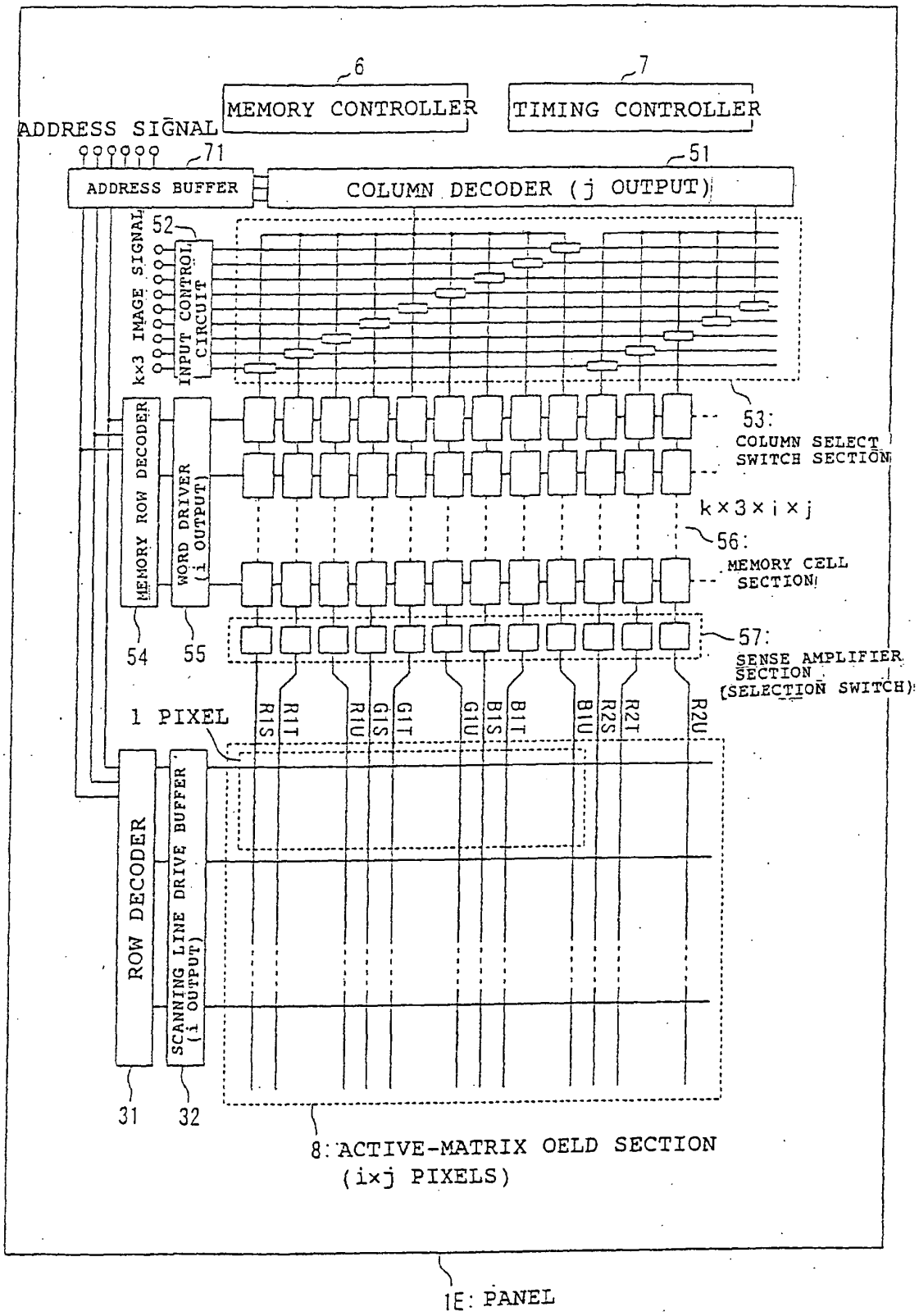

6
MEMORY CONTROLLER
7
TIMING CONTROLLER
ADDRESS SIGNAL
71
ADDRESS BUFFER
51
COLUMN DECODER (j OUTPUT)
52
k×3 IMAGE SIGNAL
INPUT CONTROL CIRCUIT
MEMORY ROW DECODER
WORD DRIVER (i OUTPUT)
53:
COLUMN SELECT SWITCH SECTION
k×3×i×j
56:
MEMORY CELL SECTION
54
55
57:
SENSE AMPLIFIER SECTION (SELECTION SWITCH)
1 PIXEL
R1S
R1T
R1U
G1S
G1T
G1U
B1S
B1T
B1U
R2S
R2T
R2U
ROW DECODER
SCANNING LINE DRIVE BUFFER (i OUTPUT)
31
32
8: ACTIVE-MATRIX OELD SECTION
(i×j PIXELS)
1E: PANEL

FIG. 8

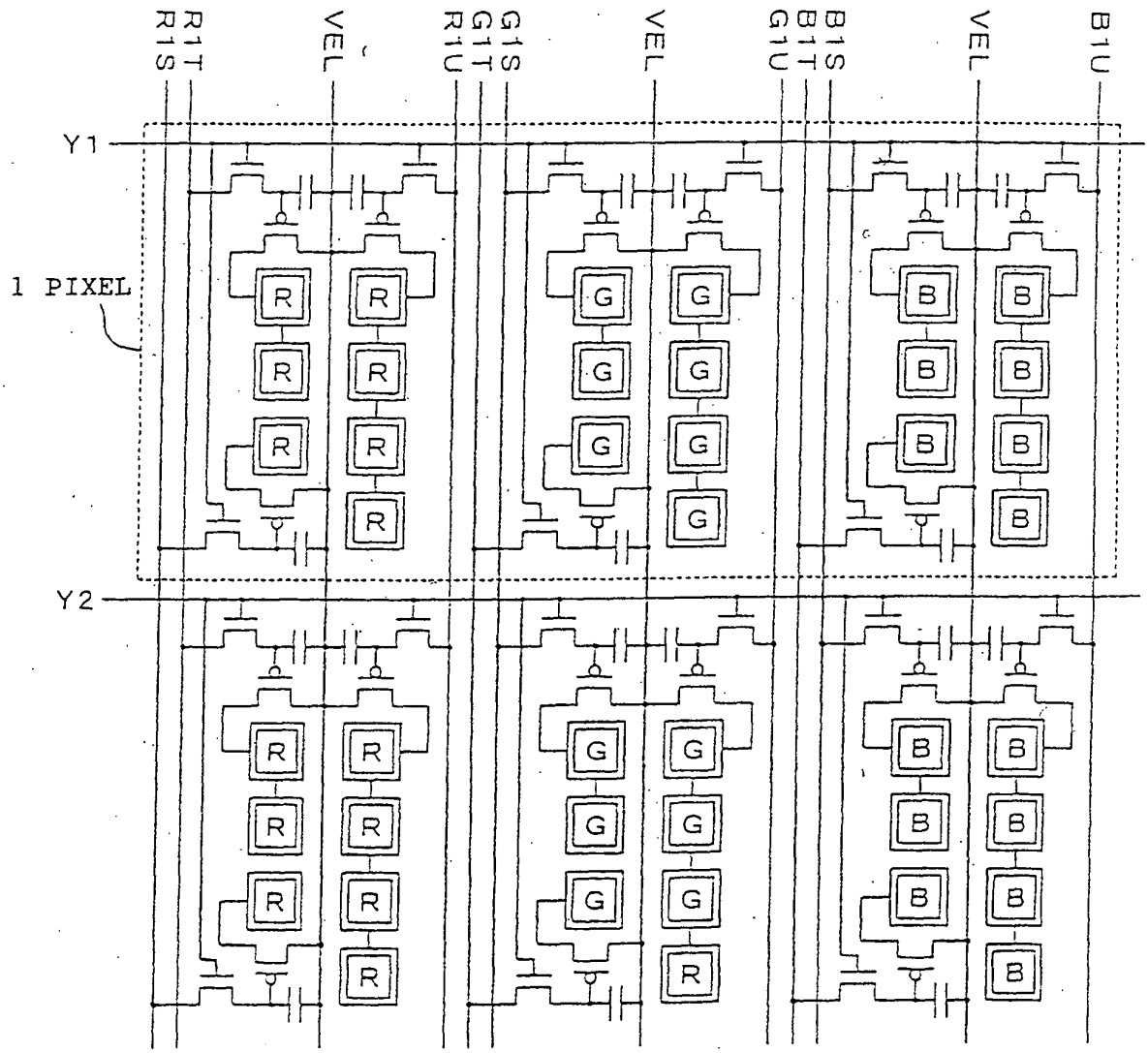


FIG.9

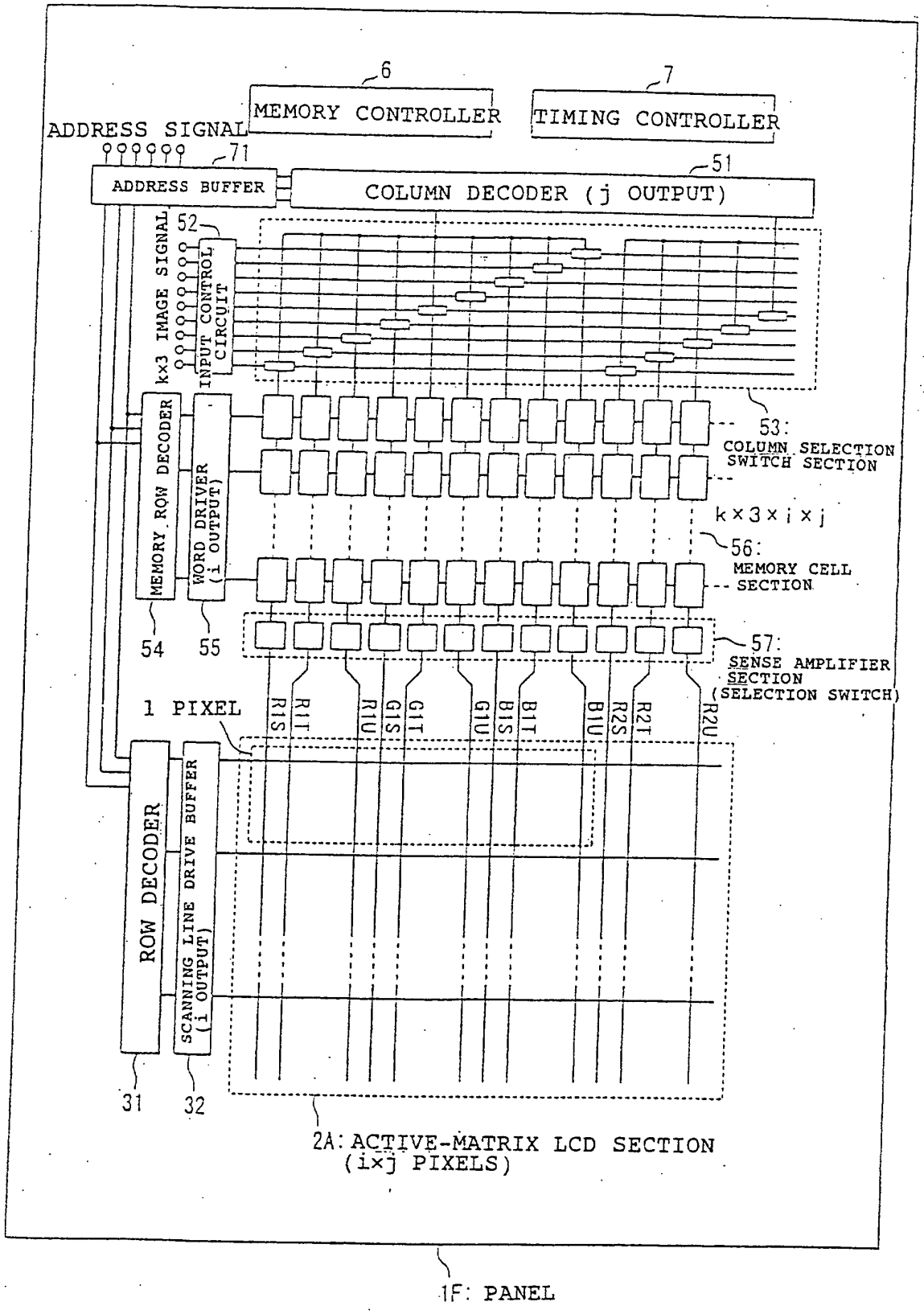

6
MEMORY CONTROLLER
7
TIMING CONTROLLER
ADDRESS SIGNAL
71
ADDRESS BUFFER
51
COLUMN DECODER (j OUTPUT)
52
kx3 IMAGE SIGNAL
INPUT CONTROL CIRCUIT
MEMORY ROW DECODER
WORD DRIVER (i OUTPUT)
53: COLUMN SELECTION SWITCH SECTION
kx3xixj
56: MEMORY CELL SECTION
54
55
57: SENSE AMPLIFIER SECTION (SELECTION SWITCH)
1 PIXEL
R1S
R1T
R1U
G1S
G1T
G1U
B1S
B1T
B1U
R2S
R2T
R2U
ROW DECODER
SCANNING LINE DRIVE BUFFER (i OUTPUT)
31
32
2A: ACTIVE-MATRIX LCD SECTION (ixj PIXELS)
1F: PANEL

FIG.10

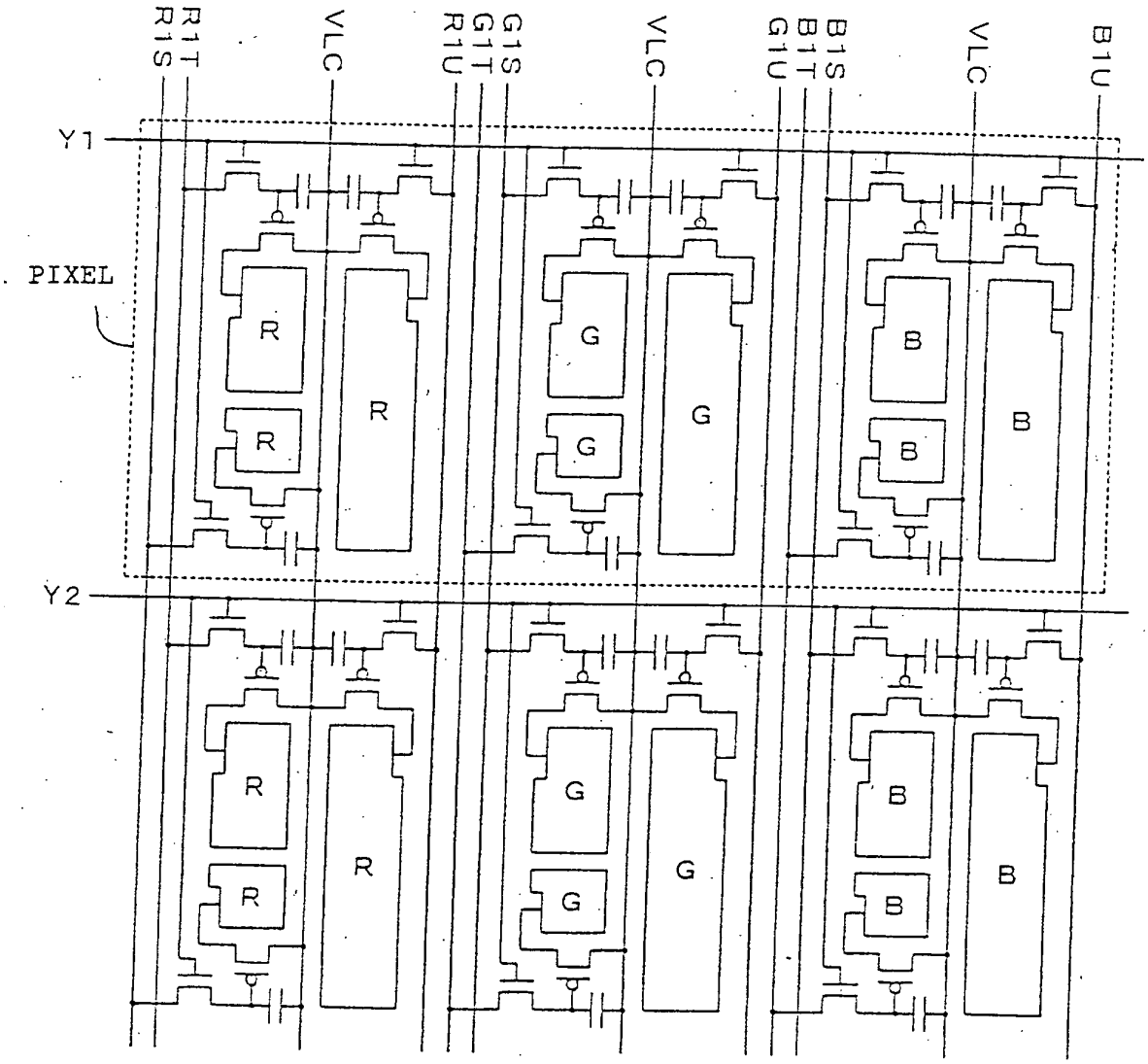
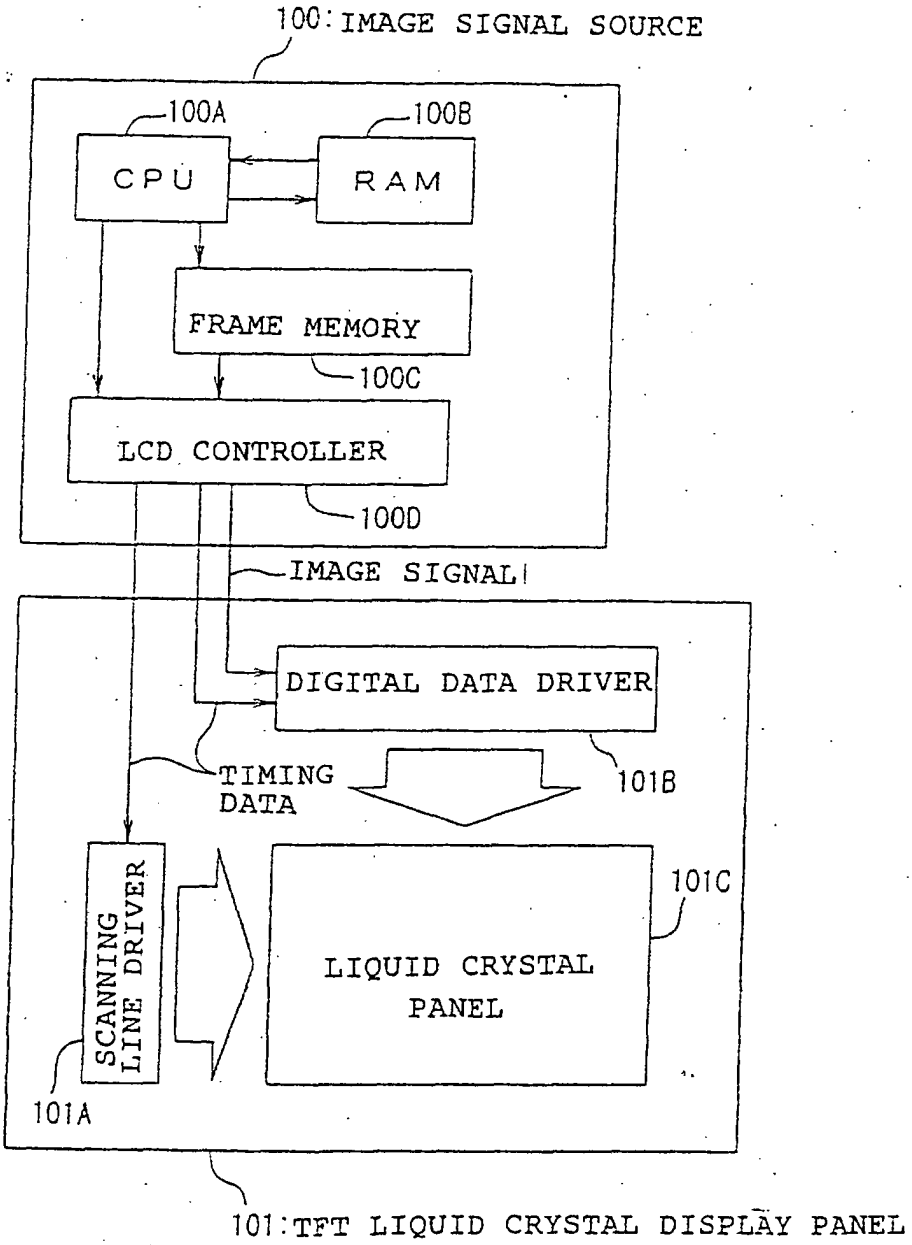


FIG.11


100: IMAGE SIGNAL SOURCE
100A
100B
CPU
RAM
FRAME MEMORY
100C
LCD CONTROLLER
100D
IMAGE SIGNAL
DIGITAL DATA DRIVER
TIMING DATA
101B
SCANNING LINE DRIVER
LIQUID CRYSTAL PANEL
101C
101A
101: TFT LIQUID CRYSTAL DISPLAY PANEL

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- JP 082277283 B **[0007]**
- US 2002145602 A **[0008]**
- US 5815136 A **[0010]**
- EP 0286309 A **[0011]**
- EP 0456394 A **[0012]**

Non-patent literature cited in the description

- **Abbot et al.** Equipping a line of memories with spare cells'', Electronics. *VNU Business Publications,* 1981, vol. 54 (15), 127-130 **[0009]**

专利名称(译)	具有集成在显示基板上的存储器的显示装置		
公开(公告)号	EP1146501B1	公开(公告)日	2011-03-30
申请号	EP2000966521	申请日	2000-10-16
[标]申请(专利权)人(译)	精工爱普生株式会社		
申请(专利权)人(译)	SEIKO EPSON CORPORATION		
当前申请(专利权)人(译)	SEIKO EPSON CORPORATION		
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发明人	MATSUEDA, YOJIRO		
IPC分类号	G09G3/36 G02F1/133 G09G3/32		
CPC分类号	G09G3/2074 G09G3/3233 G09G3/3291 G09G3/3648 G09G3/3688 G09G5/393 G09G5/395 G09G2300/0408 G09G2300/0443 G09G2300/0809 G09G2300/0842 G09G2310/027		
代理机构(译)	斯特，CLIFFORD MARK		
优先权	1999294996 1999-10-18 JP		
其他公开文献	EP1146501A4 EP1146501A1		
外部链接	Espacenet		

摘要(译)

为了在玻璃基板上一体地形成外围电路的情况下，考虑布局效率等来获得显示装置。集成在基板上并与其一体形成有源矩阵LCD部分2，其具有多个扫描线和多个数据线，这些数据线以对应于点的网格形式形成，并且有源元件根据各个交叉点使用a进行显示控制。通过驱动扫描线和数据线的液晶，用于选择扫描线的行解码器31，具有能够存储用于至少一个点的显示控制的图像信号的数量的存储单元的存储单元部分56显示驱动部分的行，并且对应于显示驱动部分的行方向上的长度分配，列解码器部分51用于选择要与输入的图像信号一起存储的存储单元，列选择开关部分53接通列解码器部分51和图像信号的选择以及将图像信号存储到所选择的存储单元的基础，以及k比特DAC部分41f或者根据存储在存储单元部分中的图像信号驱动数据线。

FIG.1