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(54) **LIQUID CRYSTAL DISPLAY DEVICE AND METHOD FOR DRIVING THE SAME**

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Description

[0001] This application claims the benefit of Korean Patent Application No. 10-2016-0067776 filed on May 31, 2016.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention relates to a display device comprising red (R) subpixels, green (G) subpixels, blue (B) subpixels, and white (W) subpixels and a method for driving the same.

Discussion of the Related Art

[0003] A liquid crystal display displays an image by controlling an electric field applied to liquid crystal molecules according to a data voltage. Driven by the development of processing technology and driving technology, active-matrix liquid-crystal displays have dropped in price and increased in performance, and thus are one of the most widely used displays across almost all display applications, from small mobile devices to large televisions.

[0004] A liquid crystal display has a liquid crystal display panel, a backlight unit for illuminating the liquid crystal display panel, a source drive integrated circuit (hereinafter also referred to as integrated circuit, IC) for supplying data voltages to data lines of the liquid crystal display panel, a gate drive IC for supplying gate pulses (or scan pulses) to gate lines (or scan lines) of the liquid crystal display panel, a control circuit for controlling the ICs, and a light source drive circuit for driving the light source of the backlight unit.

[0005] A liquid crystal display comprising red (R) subpixels, green (G) subpixels, blue (B) subpixels, and white (W) subpixels is now being developed. Hereinafter, such a display device will be referred to as an "RGBW-type display device". In the following, a white (W) subpixel will be referred as a white-colored subpixel. So, the RGBW-type display device preferably comprises subpixels of four different colors, namely red, green, blue and white. The W subpixels can adjust the brightness of the backlight unit. By increasing the brightness of individual pixels, the brightness of the backlight unit can be lowered, thus resulting in lower power consumption of the liquid crystal display.

[0006] Triple Rate Driving, short: TRD, is known as a technology that triples the data driving frequency of a pixel array, in order to reduce the number of source drive ICs (IC) in a liquid crystal display.

[0007] In a liquid crystal display with a typical pixel structure, RGB data voltages are supplied to one pixel's subpixels through three data lines during one horizontal period. In contrast, in the TRD technology, RGB data voltages are sequentially supplied to RGB subpixels though one data line. For example, an R data voltage is supplied to a red subpixel during a 1/3 horizontal period. Subsequently, a G data voltage is supplied to a green subpixel during a 1/3 horizontal period, and a B data voltage is then supplied to a blue subpixel during a 1/3 horizontal period. Thus, the TRD technology enables to reduce the number of data lines to 1/3, as compared to the typical pixel structure.

[0008] The TRD technology has the following problems when used in RGBW-type display devices.

[0009] First of all, data voltages supplied to subpixels of the same color connected to the same gate line may be dominated to one polarity. Due to this, a common voltage, which is a reference voltage for liquid crystals, may be shifted to the dominant polarity, thus causing horizontal crosstalk.

[0010] Secondly, if the polarity of a data voltage is reversed by column inversion to reduce heat generated from the source drive ICs, polarity banding phenomenon may occur. Polarity banding phenomenon means that neighboring subpixels are charged with data voltages of the same polarity. Polarity banding phenomenon causes uneven brightness. If there is polarity banding phenomenon, especially in neighboring subpixels of the same color, it leads to unevenness in brightness and color reproduction.

[0011] Thirdly, the source drive ICs generate more heat since more data voltage transitions occur with a specific color.

[0012] CN 103 185 996 A discloses a bigrid-driven transversely arranged RGBW (Red Green Blue White) pixel structure, a driving method thereof and a display panel. The pixel structure comprises a plurality of pixel units in array repeated permutation, wherein each pixel unit comprises two main pixel areas, eight thin film transistors, two grid lines and four data cables; each main pixel area comprises four subsidiary pixel areas; each data cable is electrically connected with the source electrodes of the two thin film transistors, and different data cables are electrically connected with different thin film transistors; and the grid electrodes of the two thin film transistors electrically connected with the same data cable are respectively in electric connection with different grid lines. Wwhen the grid lines of the pixel structure scan pixels in different rows in the same frame, the potential polarity of a signal of each data cable is always unchanged, so that a reversion picture of the pixel points is obtained; and as the polarities of the data cables do not need to be frequently reversed, the driving frequency of the data cables is lowered, and accordingly, the power consumption of a panel is reduced.

[0013] US 2015/379947 A1 discloses a display device that includes a pixel array including a first set of subpixels of

first to fourth colors and a second set of subpixels of the first to fourth colors. The display device also includes a data driver configured to generate first data voltages and second data voltages, the first data voltages having a first polarity with respect to a common voltage that is applied to the pixel array and the second data voltages having a second polarity with respect to the common voltage that is different than the first polarity, and wherein the data driver applies the first data voltages of the first polarity to the first set of subpixels of the first to fourth colors via the data line and subsequently applies the second data voltages of the second polarity to the second set of subpixels of the first to fourth colors via the data line.

[0014] EP 2 953 127 A2 discloses a display device that includes a plurality of gate lines extending in a first direction; a plurality of data lines extending in a second direction that intersects the first direction; and a plurality of pixels connected to the gate lines and the data lines, wherein the pixels include pixels h-th row pixels (h is a natural number) and (h+1)-th row pixels, which are adjacent to each other in the second direction, with a (k+1)-th gate line (k is a natural number) therebetween among the gate lines; and a first pixel displaying a first color and connected to the (k+1)-th gate line among the h-th row pixels and a second pixel displaying the first color and connected to the (k+1)-th gate line among the (h+1)-th row pixels are spaced apart from each other in the first direction and receive different polarities of data voltages.

[0015] EP 2 998 955 A2 discloses a display device that includes a pixel array having a plurality of pixels arranged in a matrix form based on a crossing structure of data lines and gate lines, a data driver having a plurality of output channels and configured to output a data voltage, a multiplexer configured to distribute the data voltage output from the data driver to the data lines in response to first and second control signals, and a gate driver configured to output a gate pulse synchronized with the data voltage in a non-sequential manner. The first and second control signals are in antiphase, and a switching cycle of the first and second control signals is one horizontal period or two horizontal period.

SUMMARY

[0016] Accordingly, the present invention is directed to a liquid crystal display device, preferably RGBW-type display device, which can reduce heat generation from source drive ICs and improve picture quality, in order to drive a display panel comprising subpixels of different colors, e.g. RGBW subpixels.

[0017] The above identified objects are solved by the features of the independent claims. An exemplary embodiment of the present invention provides a liquid crystal display device comprising: a data driver that reverses the polarity of data voltages for charging subpixels on a preset cycle and supplies the data voltages to data lines; and a gate driver that supplies gate pulses to gate lines in synchronization with the data voltages.

[0018] In a pixel array where the pixels are arranged, the first-color subpixels are arranged at positions where (4i+1)th row lines (i is a positive integer) and odd-numbered column lines intersect, the second-color subpixels are arranged at positions where the (4i+1)th row lines and even-numbered column lines intersect. The third-color subpixels are arranged at positions where (4i+2)th row lines and the odd-numbered column lines intersect, and the fourth-color subpixels are arranged at positions where the (4i+2)th row lines and the even-numbered column lines intersect. The second-color subpixels are arranged at positions where (4i+3)th row lines and the odd-numbered column lines intersect, and the first-color subpixels are arranged at positions where the (4i+3)th row lines and the even-numbered column lines intersect. The fourth-color subpixels are arranged at positions where (4i+4)th row lines and the odd-numbered column lines intersect, and the third-color subpixels are arranged at positions where the (4i+4)th row lines and the even-numbered column lines intersect.

[0019] In the following description the term "first side" is referred to a "right side (=right)" of a subpixel arrangement and the term "second side" is referred to a "left side (=left)" of the same subpixel arrangement when considered its top/bottom view. The "right side (=first side)" is arranged on an opposite side of the "left side (second side)" of the same subpixel or the same subpixels or the same subpixel arrangement. The term "side" is referred to a "lateral side" of the subpixel that is located in parallel to "column lines" of signal lines on the display panel and that is located vertical to "row lines" in that display panel when considered its top/bottom view.

[0020] In the following description the term "column line" is referred to an orientation of a signal line, preferably a data line, in the display panel that is in parallel to the "first side" or the "second side". Respectively the term "row line" is referred to an orientation of another signal line, preferably a gate line, in the same display panel that is arranged vertical to the first side or the second side in that display panel.

[0021] According to a preferred embodiment, the first color- and second-color subpixels may be arranged on the (4i+1)th row lines comprise thin-film transistors, TFTs, that supply data voltages from the data lines to the right of the subpixels to the pixel electrodes. The third-color- and fourth-color subpixels are preferably arranged on the (4i+2)th row lines comprise TFTs that supply data voltages from the data lines to the left of the subpixels to the pixel electrodes. The first color- and second-color subpixels are preferably arranged on the (4i+3)th row lines comprise TFTs that supply data voltages from the data lines to the right of the subpixels to the pixel electrodes. The third-color- and fourth-color subpixels may be arranged on the (4i+4)th row lines comprise TFTs that supply data voltages from the data lines to the left of the subpixels to the pixel electrodes.

[0022] According to a preferred exemplary embodiment, the data driver may supply the data lines with data voltages whose polarity is reversed on a cycle of every 4 horizontal periods. Preferably, the gate driver sequentially supplies the gate pulses to the gate lines in order: first gate line, second gate line, third gate line, and fourth gate line. Preferably, the polarity of the data voltages supplied to the data lines is reversed on data voltages of the first color, and there is a difference of 2 horizontal periods between the polarity reversal timing of data voltages supplied to the odd-numbered data lines and the polarity reversal timing of data voltages supplied to the even-numbered data lines.

[0023] According to a preferred exemplary embodiment, the first color is blue, the second color is red, the third color is white, and the fourth color is green.

[0024] According to a preferred exemplary embodiment, the first color- and second-color subpixels arranged on the (4i+1)th row lines may comprise TFTs (thin-film transistors) that supply data voltages from the data lines to the right of the subpixels to the pixel electrodes. Preferably, the third-color- and fourth-color subpixels arranged on the (4i+2)th row lines may comprise TFTs that supply data voltages from the data lines to the right of the subpixels to the pixel electrodes. Preferably, the first color- and second-color subpixels arranged on the (4i+3)th row lines may comprise TFTs that supply data voltages from the data lines to the left of the subpixels to the pixel electrodes. Preferably, the third-color- and fourth-color subpixels arranged on the (4i+4)th row lines may comprise TFTs that supply data voltages from the data lines to the left of the subpixels to the pixel electrodes.

[0025] According to a preferred exemplary embodiment, the data driver supplies the data lines with data voltages whose polarity is reversed on a cycle of every 4 horizontal periods, and simultaneously reverses the polarity of the data voltages supplied to the odd-numbered data lines and the polarity of the data voltages supplied to the even-numbered data lines. Preferably, the polarity of the data voltages supplied to the odd-numbered data lines is reversed on data voltages of the fourth color, and the polarity of the data voltages supplied to the even-numbered data lines is reversed on data voltages of the third color. Preferably, the gate driver outputs the gate pulses in order: first gate pulse, second gate pulse, third gate pulse, and fourth gate pulse. Preferably, among link lines connecting output channels of the gate driver and the gate lines, the link lines connecting the output channels of the second and third gate pulses and the second and third gate lines intersect so that the third gate pulse is applied to the second gate line after the second gate pulse is applied to the third gate line.

[0026] According to a preferred exemplary embodiment, the first color- and second-color subpixels arranged on the (4i+1)th row lines may comprise TFTs (thin-film transistors) that supply data voltages from the data lines to the right of the subpixels to the pixel electrodes. Preferably, the third-color- and fourth-color subpixels arranged on the (4i+2)th row lines may comprise TFTs that supply data voltages from the data lines to the right of the subpixels to the pixel electrodes. Preferably, the first color- and second-color subpixels arranged on the (4i+3)th row lines may comprise TFTs that supply data voltages from the data lines to the right of the subpixels to the pixel electrodes. Preferably, the third-color- and fourth-color subpixels arranged on the (4i+4)th row lines may comprise TFTs that supply data voltages from the data lines to the left of the subpixels to the pixel electrodes.

[0027] According to a preferred exemplary embodiment, the data driver supplies the data lines with data voltages whose polarity is reversed on a cycle of every 4 horizontal periods. Preferably, the polarity of the data voltages is supplied to the odd-numbered data lines is reversed on data voltages of the fourth color, and the polarity of the data voltages supplied to the even-numbered data lines is reversed on data voltages of the second color, the fourth data voltage after reversal of the polarity of a data voltage supplied to each data line is a data voltage of the fourth color, and there is a difference of 1 horizontal period between the polarity reversal timing of data voltages supplied to the odd-numbered data lines and the polarity reversal timing of data voltages supplied to the even-numbered data lines. Preferably, the gate driver may output the gate pulses in order: first gate pulse, second gate pulse, third gate pulse and fourth gate pulse. Preferably, among link lines connecting output channels of the gate driver and the gate lines, the link lines connecting the output channels of the second and third gate pulses and the second and third gate lines intersect so that the third gate pulse is applied to the second gate line after the second gate pulse is applied to the third gate line.

[0028] According to a preferred exemplary embodiment, the first color- and second-color subpixels arranged on the (4i+1)th row lines may comprise TFTs (thin-film transistors) that supply data voltages from the data lines to the left of the subpixels to the pixel electrodes. Preferably, the third-color- and fourth-color subpixels arranged on the (4i+2)th row lines may comprise TFTs that supply data voltages from the data lines to the right of the subpixels to the pixel electrodes. Preferably, the first color- and second-color subpixels arranged on the (4i+3)th row lines may comprise TFTs that supply data voltages from the data lines to the right of the subpixels to the pixel electrodes. Preferably, the third-color- and fourth-color subpixels arranged on the (4i+4)th row lines may comprise TFTs that supply data voltages from the data lines to the right of the subpixels to the pixel electrodes.

[0029] According to a preferred exemplary embodiment, the data driver supplies the data lines with data voltages whose polarity is reversed on a cycle of every 4 horizontal periods. Preferably, the polarity of the data voltages supplied to the data lines is reversed on data voltages of the fourth color, and there is a difference of 1 horizontal period between the polarity reversal timing of data voltages supplied to the odd-numbered data lines and the polarity reversal timing of data voltages supplied to the even-numbered data lines. Preferably, the gate driver outputs the gate pulses in order:

first gate pulse, second gate pulse, third gate pulse, and fourth gate pulse. Preferably, among link lines connecting output channels of the gate driver and the gate lines, the link lines connecting the output channels of the second and third gate pulses and the second and third gate lines intersect so that the third gate pulse is applied to the second gate line after the second gate pulse is applied to the third gate line.

[0030] According to a preferred exemplary embodiment, the first color is white, the second color is green, the third color is red, and the fourth color is blue.

[0031] According to an exemplary embodiment there is provided a method for driving a liquid crystal display device that comprises a plurality of data lines, a plurality of gate lines intersecting the data lines, a plurality of first-color subpixels, a plurality of second-color subpixels, a plurality of third-color subpixels, and a plurality of fourth-color subpixels according to one of the preceding claims, comprising the steps of: Supplying the data lines with data voltages whose polarity is reversed on a cycle of every 4 horizontal periods by means of a data driver; Suppling gate pulses to the gate lines in synchronization with the data voltages in the order: first gate line, second gate line, third gate line, and fourth gate line by means of a data driver, wherein the data driver supplies the data lines with data voltages whose polarity is reversed on a cycle of every 4 horizontal periods; and wherein, among link lines connecting output channels of the gate driver and the gate lines, the link lines connecting the output channels of the second and third gate pulses and the second and third gate lines intersect so that the third gate pulse is applied to the second gate line after the second gate pulse is applied to the third gate line.

BRIEF DESCRIPTION OF THE DRAWINGS

[0032] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention. In the drawings:

FIG. 1 is a block diagram of a liquid crystal display device according to an exemplary embodiment of the present invention;

FIGS. 2 and 3 are views showing a pixel array structure and a data voltage charging sequence according to a first exemplary embodiment of the present invention;

FIG. 4 is a waveform diagram showing output signals from source drive ICs and a gate driver for driving the pixel array of FIGS. 2 and 3;

FIGS. 5A to 5G are views showing which subpixels are lit up and their polarity, when white, red, green, blue, yellow, cyan, and magenta patterns are displayed on the pixel array according to the first exemplary embodiment of the present invention;

FIGS. 6A to 6G are views showing data voltages when the colors of FIGS. 5A to 5G are displayed on the pixel array;

FIGS. 7 and 8 are views showing a pixel array structure and a data voltage charging sequence according to a second exemplary embodiment of the present invention;

FIG. 9 is a waveform diagram showing output signals from source drive ICs and a gate driver for driving the pixel array of FIGS. 7 and 8;

FIGS. 10A to 10G are views showing which subpixels are lit up and their polarity, when white, red, green, blue, yellow, cyan, and magenta patterns are displayed on the pixel array according to the second exemplary embodiment of the present invention;

FIGS. 11A to 11G are views showing data voltages when the colors of FIGS. 10A to 10G are displayed on the pixel array;

FIGS. 12 and 13 are views showing a pixel array structure and a data voltage charging sequence according to a third exemplary embodiment of the present invention;

FIG. 14 is a waveform diagram showing output signals from source drive ICs and a gate driver for driving the pixel array of FIGS. 12 and 13;

FIGS. 15A to 15G are views showing which subpixels are lit up and their polarity, when white, red, green, blue, yellow, cyan, and magenta patterns are displayed on the pixel array according to the third exemplary embodiment of the present invention;

FIGS. 16A to 16G are views showing data voltages when the colors of FIGS. 15A to 15G are displayed on the pixel array;

FIGS. 17 and 18 are views showing a pixel array structure and a data voltage charging sequence according to a fourth exemplary embodiment of the present invention;

FIG. 19 is a waveform diagram showing output signals from source drive ICs and a gate driver for driving the pixel array of FIGS. 17 and 18;

FIGS. 20A to 20G are views showing which subpixels are lit up and their polarity, when white, red, green, blue, yellow, cyan, and magenta patterns are displayed on the pixel array according to the fourth exemplary embodiment

of the present invention; and

FIGS. 21A to 21G are views showing data voltages when the colors of FIGS. 20A to 20G are displayed on the pixel array.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

[0033] Hereinafter, exemplary embodiments of the present invention will be described in detail with reference to the attached drawings. Throughout the specification, like reference numerals denote substantially like components. In describing the present invention, detailed descriptions of known functions or configurations related to the present invention will be omitted when it is deemed that they may unnecessarily obscure the subject matter of the present invention.

[0034] Referring to FIG. 1, a liquid crystal display device according to the present invention has a display panel 100 with a pixel array and a display panel drive circuit for writing data for an input image to the display panel 100. A backlight unit for evenly illuminating the display panel 100 may be disposed under the display panel 100.

[0035] In order to reduce the number of source drive ICs, this display device supplies red data (hereinafter, "R data"), green data (hereinafter, "G data"), blue data (hereinafter, "B data), and white data (hereinafter, "W data") to pixels through one data line, preferably only one data line.

[0036] The display panel 100 comprises an upper substrate and a lower substrate that face each other with a liquid crystal layer in between. A pixel array on the display panel 100 comprises pixels that are arranged in a matrix by the intersections of data lines S1 to Sm and gate lines G1 to Gn.

[0037] Each pixel may comprise subpixels of two colors, three colors, or four colors, among an R subpixel for R data to be written to it, a G subpixel for G data to be written to it, a B subpixel for B data to be written to it, and a W subpixel for W data to be written to it. In a case where one pixel comprises subpixels of four colors, each pixel may comprise RGBW subpixels. In a case where one pixel comprises subpixels of three colors, a first pixel may comprise WRG subpixels and a second pixel neighboring the first pixel may comprise BWR subpixels. In this case, a preset subpixel rendering algorithm may be used to distribute a data value for the color each pixel lacks among one or more surrounding pixels to compensate for the color. Each subpixel is longer along the row line X than along the column line Y and has a TFT.

[0038] An arrangement of colors in the pixel array are as shown in FIGS 2 and 3, FIGS. 7 and 8, FIGS. 12 and 13, and FIGS. 17 and 18. In this pixel array, first-color subpixels and second-color subpixels are alternately arranged on the (4i+1)th row lines L1 and L5 (i is a positive integer). The first-color subpixels are arranged at positions where the (4i+1)th row lines L1 and L5 and the odd-numbered column lines C1 and C3 intersect. The second-color subpixels are arranged at positions where the (4i+1)th row lines L1 and L5 and the even-numbered column lines C2 and C4 intersect.

[0039] Third-color subpixels and fourth-color subpixels are alternately arranged on the (4i+2)th row lines L2 and L6. The third-color subpixels are arranged at positions where the (4i+2)th row lines L2 and L6 and the odd-numbered column lines C1 and C3 intersect. The fourth-color subpixels are arranged at positions where the (4i+2)th row lines L2 and L6 and the even-numbered column lines C2 and C4 intersect.

[0040] Second-color subpixels and first-color subpixels are alternately arranged on the (4i+3)th row lines L3 and L7. The second-color subpixels are arranged at positions where the (4i+3)th row lines L3 and L7 and the odd-numbered column lines C1 and C3 intersect. The first-color subpixels are arranged at positions where the (4i+3)th row lines L3 and L7 and the even-numbered column lines C2 and C4 intersect.

[0041] Fourth-color subpixels and third-color subpixels are alternately arranged on the (4i+4)th row lines L4 and L8. The fourth-color subpixels are arranged at positions where the (4i+4)th row lines L4 and L8 and the odd-numbered column lines C1 and C3 intersect. The third-color subpixels are arranged at positions where the (4i+4)th row lines L4 and L8 and the even-numbered column lines C2 and C4 intersect.

[0042] The structure and driving method of the pixel array will be described in detail in conjunction with FIGS. 2 to 21G.

[0043] The lower substrate of the display panel 100 comprises data lines S1 to Sm, gate lines G1 to Gn, TFTs (Thin-Film Transistors), pixel electrodes PXL connected to the TFTs, and storage capacitors Cst connected to the pixel electrodes PXL. Each pixel displays an image of video data by adjusting the amount of light transmission by using liquid crystal molecules, which are driven by a voltage difference between the pixel electrode PXL charged with a data voltage through the TFT and a common electrode COM to which a common voltage V com is applied.

[0044] A black matrix and a color filter array comprising color filters ae formed on the upper substrate of the display panel 100. The common electrode COM may be formed on the upper substrate in the case of vertical electric field-driven type, such as TN (Twisted Nematic) mode and VA (Vertical Alignment) mode, and may be formed on the lower substrate, along with the pixel electrodes, in the case of horizontal electric field-driven type, such as IPS (In-Plane Switching) mode and FFS (Fringe Field Switching) mode. Polarizers are attached to the upper and lower substrates of the display panel 100, respectively, and alignment films for setting a pre-tilt angle of liquid crystals are formed on them.

[0045] The liquid crystal display device of this invention may be implemented in any form, including a transmissive liquid crystal display, a semi-transmissive liquid crystal display, and a reflective liquid crystal display. The transmissive liquid crystal display and the semi-transmissive liquid crystal display require a backlight unit. The backlight unit may be

implemented as a direct-type backlight unit or an edge-type backlight unit.

[0046] The display panel drive circuit writes data for an input image to the pixels. The display panel drive circuit comprises a data driver 102, a gate driver 104, a timing controller 20, etc.

[0047] The data driver 102 comprises at least one source drive IC. Data output channels of the source drive ICs are connected to the data lines S1 to Sm of the pixel array. The source drive ICs receive data for an input image from the timing controller 20. Digital video data transmitted to the source drive ICs comprises R data, G data, B data, and W data. The source drive ICs convert the data to positive/negative gamma compensation voltages under the control of the timing controller 20 and output positive/negative data voltages. The source drive ICs reverse the polarity of data voltages on a predetermined cycle under the control of the timing controller 20 and output the data voltages to the data lines S1 to Sm. The predetermined cycle is 4 horizontal periods, for example, in the following embodiments, but the present invention is not limited to this.

[0048] The source drive ICs reverse the polarity of data voltages supplied through one data line, once for every 4 dots, in response to a polarity control signal POL from the timing controller 20. Here, a dot refers to a subpixel. The source drive ICs keep the same polarity for data voltages of four colors sequentially supplied through one data line, then reverse their polarity by 4-dot inversion, and then output data voltages of reversed polarity. Thus, the polarity reversal cycle for data voltages output from the source drive ICs is long, which leads to less data voltage transitions and lower power consumption. Consequently, the power consumption and heat generation of the source drive ICs can be reduced.

[0049] An R data voltage, a G data voltage, a B data voltage, and a W data voltage are supplied to RGBW subpixels through one data line. Accordingly, the liquid crystal display device of the present invention can reduce the number of data lines and the number of source drive ICs compared to the conventional art, even with the same resolution on the display panel.

[0050] Because of the correlation between the polarity reversal cycle of the source drive ICs and the pixel array structure, neighboring subpixels of the same color along the row line direction (x) and the column line direction (y) have opposite polarity. Since neighboring subpixels of the same color have opposite polarity, there is no polarity banding phenomenon between neighboring subpixels of the same color. Moreover, for subpixels of the same color, the sum of subpixels with positive polarity (+) is equal to the sum of subpixels with negative polarity (-). Thus, the sum of subpixels with positive polarity (+) and the sum of subpixels with negative polarity (-) may cancel each other out when added together, thereby attaining the balance of polarity without dominant polarity. As a result, the display device of this invention has no noise such as vertical lines since there is no polarity banding phenomenon in which neighboring subpixels of the same color have the same polarity, and no common voltage shift occurs because of the balance of polarity, thereby reproducing an input image with a picture quality that is crosstalk-free.

[0051] The gate driver 104 sequentially supplies gate pulses to the gate lines G1 to Gn under the control of the timing controller 20. The gate pulses output from the gate driver 104 are synchronized with positive/negative video data voltages with which the pixels are charged. To reduce the IC cost, the gate driver 104 may be formed directly on the lower substrate of the display panel 100, along with the pixel array, in the manufacturing process.

[0052] Output channels of the gate driver 104 and the gate lines G1 to Gn of the pixel array are connected one to one through link lines. In the following embodiments, the output sequence of gate pulses may be different on some gate lines. In this case, some of the link lines that connect the output channels of the gate driver 104 to the gate lines may intersect so that gate pulses are supplied to the pixel array in a non-sequential manner, without changing the output channels of the gate driver 104. Thus, although the gate driver 104 outputs gate pulses sequentially, starting from the first output channel, the gate pulses may be applied non-sequentially to the gate lines 14 of the pixel array.

[0053] The timing controller 20 converts an input image's RGB data received from a host system 24 to RGBW data and transmits it to the data driver 102. A mini LVDS (low-voltage differential signaling) interface or an EPI (embedded panel interface) interface may be used as an interface for data transmission between the timing controller 20 and the source drive ICs of the data driver 102. The EPI interface may use the interface technologies which were proposed in Korean Patent Application No. 10-2008-0127458 (2008-12-15), U.S. Patent Application No. 12/543,996 (2009-08-19), Korean Patent Application No. 10-2008-0127456 (2008-12-15), U.S. Patent Application No. 12/461,652 (2009-08-19), Korean Patent Application No. 10-2008-0132466 (2008-12-23), and U.S. Patent Application No. 12/537,341 (2009-08-07) field by the applicant of this patent application.

[0054] The timing controller 20 receives timing signals synchronized with input image data from the host system 24. The timing signals include a vertical synchronization signal Vsync, a horizontal synchronization signal Hsync, a data enable signal DE, a dot clock DCLK, etc. The timing controller 20 controls the operation timings of the data driver 102 and gate driver 104 based on timing signals Vsync, Hsync, DE, and DCLK that are received along with pixel data for an input image. The timing controller 20 may transmit a polarity control signal POL for controlling the polarity of the pixel array to each of the source drive ICs of the data driver 102. The mini LVDS interface transmits the polarity control signal through a separate control line. The EPI interface is an interface technology that encodes polarity control information into a control data packet transmitted between a clock training pattern for CDR (Clock and Data Recovery) and an RGBW data packet, and that transmits the encoded polarity control information to each of the source drive ICs.

[0055] The timing controller 20 may convert RGB data for an input image to RGBW data by using a well-known gain calculation algorithm. Any well-known gain calculation algorithm may be used. For example, the white calculation algorithms proposed in Korean Patent Application No. 10-2005-0039728 (2005. 05. 12), Korean Patent Application No. 10-2005-0052906 (2005. 06. 20), Korean Patent Application No. 10-2005-0066429 (2007. 07. 21), and Korean Patent Application No. 10-2006-0011292 (2006. 02. 06) filed by the applicant of this patent application are applicable. Moreover, the timing controller 20 may execute a preset subpixel rendering algorithm to distribute a data value among neighboring pixels.

[0056] The host system 24 may be any one of the following: a television system, a set-top box, a navigation system, a DVD player, a personal computer (PC), a home theater system, and a phone system.

[0057] FIGS. 2 and 3 are views showing a pixel array structure and a data voltage charging sequence according to a first exemplary embodiment of the present invention. FIG. 4 is a waveform diagram showing output signals from source drive ICs and a gate driver for driving the pixel array of FIGS. 2 and 3. The pixel array on the display panel 100 has a repeating structure of 4*8 subpixels as in FIG. 3.

[0058] ①, ②, ③, and ④ in FIG. 2 represent a charging sequence of subpixels. In FIGS. 2 and 3, "L1~ L8" represent row lines on the display panel 100. Subpixels of two colors are arranged on each of the row lines along a horizontal direction (x-axis direction). "C1~C4" represent column lines on the display panel 100. Subpixels of four colors are arranged on each of the column lines along a vertical direction (y-axis direction). Rxy, Gxy, Bxy, and Wxy in FIG. 3 represent an R subpixel at an xy position, a G subpixel at an xy position, a B subpixel at an xy position, and a W subpixel at an xy position.

[0059] Referring to FIGS. 2 and 3, B subpixels B11, B12, B51, and B52 and R subpixels R11, R12, R51, and R52 are alternately arranged on the (4i+1)th row lines L1 and L5 (i is a positive integer). The B subpixels B11, B12, B51, and B52 are arranged at positions where the (4i+1)th row lines L1 and L5 and the odd-numbered column lines C1 and C3 intersect. The R subpixels R11, R12, R51, and R52 are arranged at positions where the (4i+1)th row lines L1 and L5 and the even-numbered column lines C2 and C4 intersect.

[0060] The subpixels of first and second colors B and R arranged on the (4i+1)th row lines L1 and L5 comprise TFTs arranged at the intersections of the data lines to the right and the (4i+1)th gate lines G1 and G5, respectively. Each TFT supplies a data voltage from the data line to the right of the subpixel to the pixel electrode. The TFT of the B11 subpixel is referred to as a first TFT, the TFT of the R11 subpixel as a second TFT, the TFT of the B12 subpixel as a third TFT, and the TFT of the R12 subpixel as a fourth TFT. The first TFT supplies a B data voltage from the second data line S2 to the pixel electrode PXL of the B11 subpixel, in response to a first gate pulse from the first gate line G1. The second TFT supplies an R data voltage from the third data line S3 to the pixel electrode PXL of the R11 subpixel, in response to the first gate pulse from the first gate line G1. The third TFT supplies a B data voltage from the fourth data line S4 to the pixel electrode PXL of the B12 subpixel, in response to the first gate pulse from the first gate line G1. The fourth TFT supplies an R data voltage from the fifth data line S5 to the pixel electrode PXL of the R12 subpixel, in response to the first gate pulse from the first gate line G1.

[0061] W subpixels W21, W22, W61, and W62 and G subpixels G21, G22, G61, and G62 are alternately arranged on the (4i+2)th row lines L2 and L6. The W subpixels W21, W22, W61, and W62 are arranged at positions where the (4i+2)th row lines L2 and L6 and the odd-numbered column lines C1 and C3 intersect. The G subpixels G21, G22, G61, and G62 are arranged at positions where the (4i+2)th row lines L2 and L6 and the even-numbered column lines C2 and C4 intersect.

[0062] In the following description the term "first side" is referred to a "right side (=right)" of a subpixel arrangement and the term "second side" is referred to a "left side (=left)" of the same subpixel arrangement when considered its top/bottom view. The "right side (=first side)" is arranged on an opposite side of the "left side (second side)" of the same subpixel or the same subpixels or the same subpixel arrangement. The term "side" is referred to a "lateral side" of the subpixel that is located in parallel to "column lines" of signal lines on the display panel and that is located vertical to "row lines" in that display panel when considered its top/bottom view.

[0063] In the following description the term "column line" is referred to an orientation of a signal line, preferably a data line, in the display panel that is in parallel to the "first side" or the "second side". Respectively the term "row line" is referred to an orientation of another signal line, preferably a gate line, in the same display panel that is arranged vertical to the first side or the second side in that display panel.

[0064] The subpixels of third and fourth colors W and G arranged on the (4i+2)th row lines L2 and L6 comprise TFTs arranged at the intersections of the data lines to the left (second side) and the (4i+2)th gate lines G2 and G6, respectively. Each TFT supplies a data voltage from the data line to the left (second side) of the subpixel to the pixel electrode. The TFT of the W21 subpixel is referred to as a fifth TFT, the TFT of the G21 subpixel as a sixth TFT, the TFT of the W22 subpixel as a seventh TFT, and the TFT of the G22 subpixel as an eighth TFT. The fifth TFT supplies a W data voltage from the first data line S1 to the pixel electrode PXL of the W21 subpixel, in response to a second gate pulse from the second gate line G2. The sixth TFT supplies a G data voltage from the second data line S2 to the pixel electrode PXL of the G21 subpixel, in response to the second gate pulse from the second gate line G2. The seventh TFT supplies a W data voltage from the third data line S3 to the pixel electrode PXL of the W22 subpixel, in response to the second

gate pulse from the second gate line G2. The eighth TFT supplies a G data voltage from the fourth data line S4 to the pixel electrode PXL of the G22 subpixel, in response to the second gate pulse from the second gate line G2.

[0065] R subpixels R31, R32, R71, and R72 and B subpixels B31, B32, B71, and B72 are alternately arranged on the (4i+3)th row lines L3 and L7. The R subpixels R31, R32, R71, and R72 are arranged at positions where the (4i+3)th row lines L3 and L7 and the odd-numbered column lines C1 and C3 intersect. The B subpixels B31, B32, B71, and B72 are arranged at positions where the (4i+3)th row lines L3 and L7 and the even-numbered column lines C2 and C4 intersect.

[0066] The subpixels of the first and second colors B and R arranged on the (4i+3)th row lines L3 and L7 comprise TFTs arranged at the intersections of the data lines to the right (first side) and the (4i+3)th gate lines G3 and G7, respectively. Each TFT supplies a data voltage from the data line to the right (first side) of the subpixel to the pixel electrode. The TFT of the R31 subpixel is referred to as a ninth TFT, the TFT of the B31 subpixel as a tenth TFT, the TFT of the R32 subpixel as an eleventh TFT, and the TFT of the B32 subpixel as a twelfth TFT. The ninth TFT supplies an R data voltage from the second data line S2 to the pixel electrode PXL of the R31 subpixel, in response to a third gate pulse from the third gate line G3. The tenth TFT supplies a B data voltage from the third data line S3 to the pixel electrode PXL of the B31 subpixel, in response to the third gate pulse from the third gate line G3. The eleventh TFT supplies an R data voltage from the fourth data line S4 to the pixel electrode PXL of the R32 subpixel, in response to the third gate pulse from the third gate line G3. The twelfth TFT supplies a B data voltage from the fifth data line S5 to the pixel electrode PXL of the B32 subpixel, in response to the third gate pulse from the third gate line G3.

[0067] G subpixels G41, G42, G81, and G82 and W subpixels W41, W42, W81, and W82 are alternately arranged on the (4i+4)th row lines L4 and L8. The G subpixels G41, G42, G81, and G82 are arranged at positions where the (4i+4)th row lines L4 and L8 and the odd-numbered column lines C1 and C3 intersect. The W subpixels W41, W42, W81, and W82 are arranged at positions where the (4i+4)th row lines L4 and L8 and the even-numbered column lines C2 and C4 intersect.

[0068] The subpixels of the third and fourth colors W and G arranged on the (4i+4)th row lines L4 and L8 comprise TFTs arranged at the intersections of the data lines to the left (second side) and the (4i+4)th gate lines G4 and G8, respectively. Each TFT supplies a data voltage from the data line to the left (second side) of the subpixel to the pixel electrode. The TFT of the G41 subpixel is referred to as a thirteenth TFT, the TFT of the W41 subpixel as a fourteenth TFT, the TFT of the G42 subpixel as a fifteenth TFT, and the TFT of the W42 subpixel as a sixteenth TFT. The thirteenth TFT supplies a G data voltage from the first data line S1 to the pixel electrode PXL of the G41 subpixel, in response to a fourth gate pulse from the fourth gate line G4. The fourteenth TFT supplies a W data voltage from the second data line S2 to the pixel electrode PXL of the W41 subpixel, in response to the fourth gate pulse from the fourth gate line G4. The fifteenth TFT supplies a G data voltage from the third data line S3 to the pixel electrode PXL of the G42 subpixel, in response to the fourth gate pulse from the fourth gate line G4. The sixteenth TFT supplies a W data voltage from the fourth data line S4 to the pixel electrode PXL of the W42 subpixel, in response to the fourth gate pulse from the fourth gate line G4.

[0069] In order to reverse the polarity of data voltages once for every 4 dots, the source drive ICs output data voltages of the four colors with first polarity during 4 horizontal periods 4H, in order: B data, G data, R data, and W data, and then output data voltages of the four colors with second polarity in the above order during the next 4 horizontal periods 4H. The polarity of the data voltages supplied to the data lines S1 to Sm is reversed on the B data voltages. Once the data voltage polarity is reversed on the B data voltages, data voltages of the same polarity are supplied to the data lines, in order: B data voltage, G data voltage, R data voltage, and W data voltage. The polarity of the data voltage may be reversed every frame by the source drive ICs.

[0070] As shown in FIG. 4, the timing controller 20 controls in such a way that there is a difference of 2 horizontal periods between the polarity reversal timing of data voltages supplied to the odd-numbered data lines S1, S3, and S5 and the polarity reversal timing of data voltages supplied to the even-numbered data lines S2 and S4, in order to keep the balance of polarity between subpixels of the same color on each row line and each column line.

[0071] Gate pulses output from the gate driver 104 are sequentially supplied to the gate lines G1 to G8. Link lines connecting output channels of the gate driver 104 and the gate lines G1 to G8 do not intersect. Thus, gate pulses are sequentially applied to the gate lines G1 to G8, starting from the first gate line G1.

[0072] In order to write data for an input image to the pixels of the pixel array shown in FIGS. 2 and 3, the polarity of data voltages is reversed on a cycle of every 4 horizontal periods by the source drive ICs, and gate pulses are sequentially applied to the gate lines G1 to Gn in order: G1, G2, ... G8.

[0073] FIGS. 5A to 6G show how data voltage transitions occur when a test pattern of various colors is displayed on the pixel array according to the first exemplary embodiment of the present invention. It is assumed that the white-level voltage (or highest voltage) for data voltages before polarity reversal is 1 V. In this case, the data voltages begin their transition from 1 V. Here, a data voltage transition means that a large amount of electric current is generated when a data voltage output from the source drive ICs changes, causing the source drive IC to consume current and generate heat. When a polarity reversal occurs in a way that the white-level voltage changes its polarity from first polarity to second polarity, a data voltage transition occurs with a voltage swing of 2 V.

[0074] FIGS. 5A to 5G are views showing which subpixels are lit up and their polarity, when white, red, green, blue, yellow, cyan, and magenta patterns are displayed on the pixel array according to the first exemplary embodiment of the present invention. FIGS. 6A to 6G are views showing data voltages when the colors of FIGS. 5A to 5G are displayed on the pixel array. The arrows in FIGS. 6A to 6G indicate data voltage transitions.

[0075] Referring to FIGS. 5A and 6A, when a white pattern is displayed on the pixels of the pixel array, the R subpixels, G subpixels, B subpixels, and W subpixels are all lit up at the white level. In the white pattern, the RGBW data voltages are the white-level voltage. For the white pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 3 change twice with a voltage swing of 2 V during 8 horizontal periods 8H. At these data voltages, the temperature of heat generated from the source drive ICs is 246 °C, as seen from Table 1.

[0076] Referring to FIGS. 5B and 6B, when a red pattern is displayed on the pixels of the pixel array, only the R subpixels are lit up at the white level. In the red pattern, the R data voltage is the white-level voltage (or highest voltage), and the data voltages of the other colors are the black-level voltage (or lowest voltage). For the red pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 3 change twice with a voltage swing of 1 V during 8 horizontal periods 8H. At these data voltages, the temperature of heat generated from the source drive ICs is 201 °C, as seen from Table 1.

[0077] Referring to FIGS. 5C and 6C, when a green pattern is displayed on the pixels of the pixel array, only the G subpixels are lit up at the white level. In the green pattern, the G data voltage is the white-level voltage (or highest voltage), and the data voltages of the other colors are the black-level voltage (or lowest voltage). For the green pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 3 change twice with a voltage swing of 1 V during 8 horizontal periods 8H. At these data voltages, the temperature of heat generated from the source drive ICs is 201 °C, as seen from Table 1.

[0078] Referring to FIGS. 5D and 6D, when a blue pattern is displayed on the pixels of the pixel array, only the B subpixels are lit up at the white level. In the blue pattern, the B data voltage is the white-level voltage (or highest voltage), and the data voltages of the other colors are the black-level voltage (or lowest voltage). For the blue pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 3 change twice with a voltage swing of 1 V during 8 horizontal periods 8H. At these data voltages, the temperature of heat generated from the source drive ICs is 201 °C, as seen from Table 1.

[0079] Referring to FIGS. 5E and 6E, when a yellow pattern is displayed on the pixels of the pixel array, the G subpixels and the R subpixels are lit up at the white level. In the yellow pattern, the G data voltage and the R data voltage are the white-level voltage (or highest voltage), and the data voltages of the other colors are the black-level voltage (or lowest voltage). For the yellow pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 3 change twice with a voltage swing of 1 V during 8 horizontal periods 8H. At these data voltages, the temperature of heat generated from the source drive ICs is 201 °C, as seen from Table 1.

[0080] Referring to FIGS. 5F and 6F, when a cyan pattern is displayed on the pixels of the pixel array, the G subpixels and the B subpixels are lit up at the white level. In the cyan pattern, the G data voltage and the B data voltage are the white-level voltage, and the data voltages of the other colors are the black-level voltage. For the cyan pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 3 change twice with a voltage swing of 1 V during 8 horizontal periods 8H. At these data voltages, the temperature of heat generated from the source drive ICs is 201 °C, as seen from Table 1.

[0081] Referring to FIGS. 5G and 6G, when a magenta pattern is displayed on the pixels of the pixel array, the B subpixels and the R subpixels are lit up at the white level. In the magenta pattern, the B data voltage and the R data voltage are the white-level voltage (or highest voltage), and the data voltages of the other colors are the black-level voltage (or lowest voltage). For the magenta pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 3 change four times with a voltage swing of 1 V during 8 horizontal periods 8H. At these data voltages, the temperature of heat generated from the source drive ICs is 355 °C, as seen from Table 1.

[0082] In the first exemplary embodiment (FIGS. 2 to 4) of the present invention, the balance of polarity may be attained for each color without polarity banding phenomenon, and therefore input images may be reproduced with high picture quality. In the first exemplary embodiment (FIGS. 2 to 4) of the present invention, the power consumption and heat generation of the source drive ICs may be kept at moderate levels for every color except for magenta.

[0083] FIGS. 7 and 8 are views showing a pixel array structure and a data voltage charging sequence according to a second exemplary embodiment of the present invention. FIG. 9 is a waveform diagram showing output signals from source drive ICs and a gate driver for driving the pixel array of FIGS. 7 and 8. The pixel array on the display panel 100 has a repeating structure of 4*8 subpixels as in FIG. 8.

[0084] Referring to FIGS. 7 and 8, W subpixels W11, W12, W51, and W52 and G subpixels G11, G12, G51, and G52 are alternately arranged on the (4i+1)th row lines L1 and L5. The W subpixels W11, W12, W51, and W52 are arranged at positions where the (4i+1)th row lines L1 and L5 and the odd-numbered column lines C1 and C3 intersect. The G subpixels G11, G12, G51, and G52 are arranged at positions where the (4i+1)th row lines L1 and L5 and the even-numbered column lines C2 and C4 intersect.

[0085] The subpixels of first and second colors W and G arranged on the (4i+1)th row lines L1 and L5 comprise TFTs arranged at the intersections of the data lines to the right (first side) and the (4i+1)th gate lines G1 and G5, respectively. Each TFT supplies a data voltage from the data line to the right (first side) of the subpixel to the pixel electrode. The TFT of the W11 subpixel is referred to as a first TFT, the TFT of the G11 subpixel as a second TFT, the TFT of the W12 subpixel as a third TFT, and the TFT of the G12 subpixel as a fourth TFT. The first TFT supplies a W data voltage from the second data line S2 to the pixel electrode PXL of the W11 subpixel, in response to a first gate pulse from the first gate line G1. The second TFT supplies a G data voltage from the third data line S3 to the pixel electrode PXL of the G11 subpixel, in response to the first gate pulse from the first gate line G1. The third TFT supplies a W data voltage from the fourth data line S4 to the pixel electrode PXL of the W12 subpixel, in response to the first gate pulse from the first gate line G1. The fourth TFT supplies a G data voltage from the fifth data line S5 to the pixel electrode PXL of the G12 subpixel, in response to the first gate pulse from the first gate line G1.

[0086] R subpixels R21, R22, R61, and R62 and B subpixels B21, B22, B61, and B62 are alternately arranged on the (4i+2)th row lines L2 and L6. The R subpixels R21, R22, R61, and R62 are arranged at positions where the (4i+2)th row lines L2 and L6 and the odd-numbered column lines C1 and C3 intersect. The B subpixels B21, B22, B61, and B62 are arranged at positions where the (4i+2)th row lines L2 and L6 and the even-numbered column lines C2 and C4 intersect.

[0087] The subpixels of third and fourth colors R and B arranged on the (4i+2)th row lines L2 and L6 comprise TFTs arranged at the intersections of the data lines to the right (first side) and the (4i+2)th gate lines G2 and G6, respectively. Each TFT supplies a data voltage from the data line to the right (first side) of the subpixel to the pixel electrode. The TFT of the R21 subpixel is referred to as a fifth TFT, the TFT of the B21 subpixel as a sixth TFT, the TFT of the R22 subpixel as a seventh TFT, and the TFT of the B22 subpixel as an eighth TFT. The fifth TFT supplies an R data voltage from the second data line S2 to the pixel electrode PXL of the R21 subpixel, in response to a third gate pulse from the second gate line G2. The sixth TFT supplies a B data voltage from the third data line S3 to the pixel electrode PXL of the B21 subpixel, in response to the third gate pulse from the second gate line G2. The seventh TFT supplies an R data voltage from the fourth data line S4 to the pixel electrode PXL of the R22 subpixel, in response to the third gate pulse from the second gate line G2. The eighth TFT supplies a B data voltage from the fifth data line S5 to the pixel electrode PXL of the B22 subpixel, in response to the third gate pulse from the second gate line G2.

[0088] G subpixels G31, G32, G71, and G72 and W subpixels W31, W32, W71, and W72 are alternately arranged on the (4i+3)th row lines L3 and L7. The G subpixels G31, G32, G71, and G72 are arranged at positions where the (4i+3)th row lines L3 and L7 and the odd-numbered column lines C1 and C3 intersect. The W subpixels W31, W32, W71, and W72 are arranged at positions where the (4i+3)th row lines L3 and L7 and the even-numbered column lines C2 and C4 intersect.

[0089] The subpixels of the first and second colors W and G arranged on the (4i+3)th row lines L3 and L7 comprise TFTs arranged at the intersections of the data lines to the left (second side) and the (4i+3)th gate lines G3 and G7, respectively. Each TFT supplies a data voltage from the data line to the left (second side) of the subpixel to the pixel electrode. The TFT of the G31 subpixel is referred to as a ninth TFT, the TFT of the W31 subpixel as a tenth TFT, the TFT of the G32 subpixel as an eleventh TFT, and the TFT of the W32 subpixel as a twelfth TFT. The ninth TFT supplies a G data voltage from the first data line S1 to the pixel electrode PXL of the G31 subpixel, in response to a second gate pulse from the third gate line G3. The tenth TFT supplies a W data voltage from the second data line S2 to the pixel electrode PXL of the W31 subpixel, in response to the second gate pulse from the third gate line G3. The eleventh TFT supplies a G data voltage from the third data line S3 to the pixel electrode PXL of the G32 subpixel, in response to the second gate pulse from the third gate line G3. The twelfth TFT supplies a W data voltage from the fourth data line S4 to the pixel electrode PXL of the W32 subpixel, in response to the second gate pulse from the third gate line G3.

[0090] B subpixels B41, B42, B81, and B82 and R subpixels R41, R42, R81, and R82 are alternately arranged on the (4i+4)th row lines L4 and L8. The B subpixels B41, B42, B81, and B82 are arranged at positions where the (4i+4)th row lines L4 and L8 and the odd-numbered column lines C1 and C3 intersect. The R subpixels R41, R42, R81, and R82 are arranged at positions where the (4i+4)th row lines L4 and L8 and the even-numbered column lines C2 and C4 intersect.

[0091] The subpixels of the third and fourth colors R and B arranged on the (4i+2)th row lines L4 and L8 comprise TFTs arranged at the intersections of the data lines to the left (second side) and the (4i+4)th gate lines G4 and G8, respectively. Each TFT supplies a data voltage from the data line to the left (second side) of the subpixel to the pixel electrode. The TFT of the B41 subpixel is referred to as a thirteenth TFT, the TFT of the R41 subpixel as a fourteenth TFT, the TFT of the B42 subpixel as a fifteenth TFT, and the TFT of the R42 subpixel as a sixteenth TFT. The thirteenth TFT supplies a B data voltage from the first data line S1 to the pixel electrode PXL of the B41 subpixel, in response to a fourth gate pulse from the fourth gate line G4. The fourteenth TFT supplies an R data voltage from the second data line S2 to the pixel electrode PXL of the R41 subpixel, in response to the fourth gate pulse from the fourth gate line G4. The fifteenth TFT supplies a B data voltage from the third data line S3 to the pixel electrode PXL of the B42 subpixel, in response to the fourth gate pulse from the fourth gate line G4. The sixteenth TFT supplies an R data voltage from the fourth data line S4 to the pixel electrode PXL of the R42 subpixel, in response to the fourth gate pulse from the fourth gate line G4.

[0092] In order to reverse the polarity of data voltages once for every 4 dots, the source drive ICs output data voltages with first polarity during 4 horizontal periods 4H, and then output data voltages with second polarity during the next 4 horizontal periods 4H.

[0093] The data voltages supplied to the odd-numbered data lines S1, S3, and S5 are output from the source drive ICs during 4 horizontal periods 4H, in order: first data voltage of the fourth color B, second data voltage of the fourth color B, first data voltage of the second color G, and second data voltage of the second color G, and then their polarity is reversed. The first and second data voltages of the fourth color B are sequentially supplied to the B subpixels B21 and B42. The first and second data voltages of the second color G are sequentially supplied to the G subpixels G51 and G72. The polarity of the data voltages supplied to the odd-numbered data lines S1, S3, and S5 is reversed on the data voltages of the fourth color B.

[0094] The data voltages supplied to the even-numbered data lines S2 and S4 are output from the source drive ICs during 4 horizontal periods 4H, in order: first data voltage of the third color R, second data voltage of the third color R, first data voltage of the first color W, and second data voltage of the first color W, and then their polarity is reversed. The first and second data voltages of the third color R are sequentially supplied to the R subpixels R21 and R41. The first and second data voltages of the first color W are sequentially supplied to the W subpixels W51 and W71. The polarity of the data voltages supplied to the even-numbered data lines S2 and S4 is reversed on the data voltages of the third color R.

[0095] As shown in FIG. 8 and 9, the source drive ICs simultaneously reverse the polarity of the data voltages supplied to the odd-numbered data lines S1, S3, and S5 and the polarity of the data voltages supplied to the even-numbered data lines S2 and S4, under the control of the timing controller 20.

[0096] Link lines LNK connecting (4i+2)th and (4i+3)th output channels 2 and 3 of the gate driver 104 and the (4i+2)th and (4i+3)th gate lines G2, G3, G6, and G7 intersect, with an insulating layer in between. Due to this, as shown in FIG. 9, although the gate driver 104 outputs a third gate pulse through the third output channel 3 after outputting a second gate pulse through the second output channel 2, the third gate pulse is applied to the second gate line G2 after the second gate pulse is applied to the third gate line G3. Accordingly, gate pulses are applied to the gate lines G1 to G8 in order: G1, G3, G2, G4, G5, G7, G6, and G8.

[0097] FIGS. 10A to 11G show how data voltage transitions occur when a test pattern of various colors is displayed on the pixel array according to the second exemplary embodiment of the present invention.

[0098] FIGS. 10A to 10G are views showing which subpixels are lit up and their polarity, when white, red, green, blue, yellow, cyan, and magenta patterns are displayed on the pixel array according to the second exemplary embodiment of the present invention. FIGS. 11A to 11G are views showing data voltages when the colors of FIGS. 10A to 10G are displayed on the pixel array. The arrows in FIGS. 11A to 11G indicate data voltage transitions.

[0099] Referring to FIGS. 10A and 11A, when a white pattern is displayed on the pixels of the pixel array, the R subpixels, G subpixels, B subpixels, and W subpixels are all lit up at the white level. In the white pattern, the RGBW data voltages are the white-level voltage. For the white pattern to be displayed on the pixel array, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 8 change twice with a voltage swing of 2 V during 8 horizontal periods 8H. At these data voltages, the temperature of heat generated from the source drive ICs is 246 °C, as seen from Table 1.

[0100] Referring to FIGS. 10B and 11B, when a red pattern is displayed on the pixels of the pixel array, only the R subpixels are lit up at the white level. In the red pattern, the R data voltage is the white-level voltage, and the data voltages of the other colors are the black-level voltage. For the red pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 8 change once with a voltage swing of 1 V during 8 horizontal periods 8H. Since the data voltages applied to the odd-numbered data lines S1, S3, and S5 undergo no transition to the white-level voltage, the average number of transitions in data voltage applied to the data lines S1 to S5 during the 8 horizontal periods is 1. At these data voltages, the temperature of heat generated from the source drive ICs is 150 °C, as seen from Table 1.

[0101] Referring to FIGS. 10C and 11C, when a green pattern is displayed on the pixels of the pixel array, only the G subpixels are lit up at the white level. In the green pattern, the G data voltage is the white-level voltage, and the data voltages of the other colors are the black-level voltage. For the green pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 8 change twice with a voltage swing of 1 V during 8 horizontal periods 8H. Since the data voltages applied to the even-numbered data lines S2 and S4 undergo no transition to the white-level voltage while the data voltages applied to the odd-numbered data lines S1, S3, and S5 undergo four transitions, the average number of transitions in data voltage applied to the data lines S1 to S5 during the 8 horizontal periods is 2. At these data voltages, the temperature of heat generated from the source drive ICs is 201 °C, as seen from Table 1.

[0102] Referring to FIGS. 10D and 11D, when a blue pattern is displayed on the pixels of the pixel array, only the B subpixels are lit up at the white level. In the blue pattern, the B data voltage is the white-level voltage (or highest voltage), and the data voltages of the other colors are the black-level voltage (or lowest voltage). For the blue pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 8 change once with a voltage swing of 1 V during 8 horizontal periods 8H. Since the data voltages applied to the even-numbered data lines S2 and S4 undergo no transition

to the white-level voltage, the average number of transitions in data voltage applied to the data lines S1 to S5 during the 8 horizontal periods is 1. At these data voltages, the temperature of heat generated from the source drive ICs is 142 °C, as seen from Table 1.

[0103] Referring to FIGS. 10E and 11E, when a yellow pattern is displayed on the pixels of the pixel array, the G subpixels and the R subpixels are lit up at the white level. In the yellow pattern, the G data voltage and the R data voltage are the white-level voltage, and the data voltages of the other colors are the black-level voltage. For the yellow pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 8 change three times with a voltage swing of 1 V during 8 horizontal periods 8H. Since the data voltages applied to the odd-numbered data lines S1, S3, and S5 undergo four transitions while the data voltages applied to the even-numbered data lines S2 and S4 undergo two transitions, the average number of transitions in data voltage applied to the data lines S1 to S5 during the 8 horizontal periods is 3. At these data voltages, the temperature of heat generated from the source drive ICs is 222 °C, as seen from Table 1.

[0104] Referring to FIGS. 10F and 11F, when a cyan pattern is displayed on the pixels of the pixel array, the G subpixels and the B subpixels are lit up at the white level. In the cyan pattern, the G data voltage and the B data voltage are the white-level voltage, and the data voltages of the other colors are the black-level voltage. For the cyan pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 8 change once with a voltage swing of 1 V during 8 horizontal periods 8H. Since the data voltages applied to the even-numbered data lines S2 and S4 undergo no transition to the white-level voltage, the average number of transitions in data voltage applied to the data lines S1 to S5 during the 8 horizontal periods is 1. At these data voltages, the temperature of heat generated from the source drive ICs is 150 °C, as seen from Table 1.

[0105] Referring to FIGS. 10G and 11G, when a magenta pattern is displayed on the pixels of the pixel array, the B subpixels and the R subpixels are lit up at the white level. In the magenta pattern, the B data voltage and the R data voltage are the white-level voltage, and the data voltages of the other colors are the black-level voltage. For the magenta pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 8 change twice with a voltage swing of 1 V during 8 horizontal periods 8H. At these data voltages, the temperature of heat generated from the source drive ICs is 201 °C, as seen from Table 1.

[0106] In the second exemplary embodiment (FIGS. 7 to 9) of the present invention, the balance of polarity may be attained for each color without polarity banding phenomenon, and therefore input images may be reproduced with high picture quality. However, the data voltages supplied to the data lines are applied simultaneously and hence the amount of charge in the pixels varies with each row line, which may create horizontal lines visible along the row line direction. In the second exemplary embodiment (FIGS. 7 to 9) of the present invention, the power consumption and heat generation of the source drive ICs may be reduced for every color.

[0107] FIGS. 12 and 13 are views showing a pixel array structure and a data voltage charging sequence according to a third exemplary embodiment of the present invention. FIG. 14 is a waveform diagram showing output signals from source drive ICs and a gate driver for driving the pixel array of FIGS. 12 and 13. The pixel array on the display panel 100 has a repeating structure of 4*8 subpixels as in FIG. 13.

[0108] Referring to FIGS. 12 and 13, W subpixels W11, W12, W51, and W52 and G subpixels G11, G12, G51, and G52 are alternately arranged on the (4i+1)th row lines L1 and L5. The W subpixels W11, W12, W51, and W52 are arranged at positions where the (4i+1)th row lines L1 and L5 and the odd-numbered column lines C1 and C3 intersect. The G subpixels G11, G12, G51, and G52 are arranged at positions where the (4i+1)th row lines L1 and L5 and the even-numbered column lines C2 and C4 intersect.

[0109] The subpixels of first and second colors W and G arranged on the (4i+1)th row lines L1 and L5 comprise TFTs arranged at the intersections of the data lines to the right (first side) and the (4i+1)th gate lines G1 and G5, respectively. Each TFT supplies a data voltage from the data line to the right (first side) of the subpixel to the pixel electrode. The TFT of the W11 subpixel is referred to as a first TFT, the TFT of the G11 subpixel as a second TFT, the TFT of the W12 subpixel as a third TFT, and the TFT of the G12 subpixel as a fourth TFT. The first TFT supplies a W data voltage from the second data line S2 to the pixel electrode PXL of the W11 subpixel, in response to a first gate pulse from the first gate line G1. The second TFT supplies a G data voltage from the third data line S3 to the pixel electrode PXL of the G11 subpixel, in response to the first gate pulse from the first gate line G1. The third TFT supplies a W data voltage from the fourth data line S4 to the pixel electrode PXL of the W12 subpixel, in response to the first gate pulse from the first gate line G1. The fourth TFT supplies a G data voltage from the fifth data line S5 to the pixel electrode PXL of the G12 subpixel, in response to the first gate pulse from the first gate line G1.

[0110] R subpixels R21, R22, R61, and R62 and B subpixels B21, B22, B61, and B62 are alternately arranged on the (4i+2)th row lines L2 and L6. The R subpixels R21, R22, R61, and R62 are arranged at positions where the (4i+2)th row lines L2 and L6 and the odd-numbered column lines C1 and C3 intersect. The B subpixels B21, B22, B61, and B62 are arranged at positions where the (4i+2)th row lines L2 and L6 and the even-numbered column lines C2 and C4 intersect.

[0111] The subpixels of third and fourth colors R and B arranged on the (4i+2)th row lines L2 and L6 comprise TFTs arranged at the intersections of the data lines to the right and the (4i+2)th gate lines G2 and G6, respectively. Each TFT

supplies a data voltage from the data line to the right of the subpixel to the pixel electrode. The TFT of the R21 subpixel is referred to as a fifth TFT, the TFT of the B21 subpixel as a sixth TFT, the TFT of the R22 subpixel as a seventh TFT, and the TFT of the B22 subpixel as an eighth TFT.

[0112] The fifth TFT supplies an R data voltage from the second data line S2 to the pixel electrode PXL of the R21 subpixel, in response to a third gate pulse from the second gate line G2. The sixth TFT supplies a B data voltage from the third data line S3 to the pixel electrode PXL of the B21 subpixel, in response to the third gate pulse from the second gate line G2. The seventh TFT supplies an R data voltage from the fourth data line S4 to the pixel electrode PXL of the R22 subpixel, in response to the third gate pulse from the second gate line G2. The eighth TFT supplies a B data voltage from the fifth data line S5 to the pixel electrode PXL of the B22 subpixel, in response to the third gate pulse from the second gate line G2.

[0113] G subpixels G31, G32, G71, and G72 and W subpixels W31, W32, W71, and W72 are alternately arranged on the (4i+3)th row lines L3 and L7. The G subpixels G31, G32, G71, and G72 are arranged at positions where the (4i+3)th row lines L3 and L7 and the odd-numbered column lines C1 and C3 intersect. The W subpixels W31, W32, W71, and W72 are arranged at positions where the (4i+3)th row lines L3 and L7 and the even-numbered column lines C2 and C4 intersect.

[0114] The subpixels of the first and second colors W and G arranged on the (4i+3)th row lines L3 and L7 comprise TFTs arranged at the intersections of the data lines to the right (first side) and the (4i+3)th gate lines G3 and G7, respectively. Each TFT supplies a data voltage from the data line to the right (first side) of the subpixel to the pixel electrode. The TFT of the G31 subpixel is referred to as a ninth TFT, the TFT of the W31 subpixel as a tenth TFT, the TFT of the G32 subpixel as an eleventh TFT, and the TFT of the W32 subpixel as a twelfth TFT. The ninth TFT supplies a G data voltage from the second data line S2 to the pixel electrode PXL of the G31 subpixel, in response to a second gate pulse from the third gate line G3. The tenth TFT supplies a W data voltage from the third data line S3 to the pixel electrode PXL of the W31 subpixel, in response to the second gate pulse from the third gate line G3. The eleventh TFT supplies a G data voltage from the fourth data line S4 to the pixel electrode PXL of the G32 subpixel, in response to the second gate pulse from the third gate line G3. The twelfth TFT supplies a W data voltage from the fifth data line S5 to the pixel electrode PXL of the W32 subpixel, in response to the second gate pulse from the third gate line G3.

[0115] B subpixels B41, B42, B81, and B82 and R subpixels R41, R42, R81, and R82 are alternately arranged on the (4i+4)th row lines L4 and L8. The B subpixels B41, B42, B81, and B82 are arranged at positions where the (4i+4)th row lines L4 and L8 and the odd-numbered column lines C1 and C3 intersect. The R subpixels R41, R42, R81, and R82 are arranged at positions where the (4i+4)th row lines L4 and L8 and the even-numbered column lines C2 and C4 intersect.

[0116] The subpixels of the third and fourth colors R and B arranged on the (4i+4)th row lines L4 and L8 comprise TFTs arranged at the intersections of the data lines to the left (second side) and the (4i+4)th gate lines G4 and G8, respectively. Each TFT supplies a data voltage from the data line to the left (second side) of the subpixel to the pixel electrode. The TFT of the B41 subpixel is referred to as a thirteenth TFT, the TFT of the R41 subpixel as a fourteenth TFT, the TFT of the B42 subpixel as a fifteenth TFT, and the TFT of the R42 subpixel as a sixteenth TFT. The thirteenth TFT supplies a B data voltage from the first data line S1 to the pixel electrode PXL of the B41 subpixel, in response to a fourth gate pulse from the fourth gate line G4. The fourteenth TFT supplies an R data voltage from the second data line S2 to the pixel electrode PXL of the R41 subpixel, in response to the fourth gate pulse from the fourth gate line G4. The fifteenth TFT supplies a B data voltage from the third data line S3 to the pixel electrode PXL of the B42 subpixel, in response to the fourth gate pulse from the fourth gate line G4. The sixteenth TFT supplies an R data voltage from the fourth data line S4 to the pixel electrode PXL of the R42 subpixel, in response to the fourth gate pulse from the fourth gate line G4.

[0117] In order to reverse the polarity of data voltages once for every 4 dots, the source drive ICs output data voltages with first polarity during 4 horizontal periods 4H, and then output data voltages with second polarity during the next 4 horizontal periods 4H.

[0118] The data voltages supplied to the odd-numbered data lines S1, S3, and S5 are output from the source drive ICs during 4 horizontal periods 4H, in order: data voltage of the second color G, data voltage of the first color W, data voltage of the fourth color B, and data voltage of the fourth color B, and then their polarity is reversed. The polarity of the data voltages supplied to the odd-numbered data lines S1, S3, and S5 is reversed on the data voltages of the fourth color B.

[0119] The data voltages supplied to the even-numbered data lines S2 and S4 are output from the source drive ICs during 4 horizontal periods 4H, in order: data voltage of the first color W, data voltage of the second color G, data voltage of the third color R, and data voltage of the third color R, and then their polarity is reversed. The polarity of the data voltages supplied to the even-numbered data lines S2 and S4 is reversed on the data voltages of the second color G. Among the data voltages supplied to the data lines S1 to Sm, the fourth data voltage after polarity change - that is, the data voltage immediately before polarity reversal - is a data voltage of the first color W.

[0120] As shown in FIG. 14, the timing controller 20 controls in such a way that there is a difference of 1 horizontal period 1H between the polarity reversal timing of data voltages supplied to the odd-numbered data lines S1, S3, and

S5 and the polarity reversal timing of data voltages supplied to the even-numbered data lines S2 and S4.

[0121] Link lines LNK connecting (4i+2)th and (4i+3)th output channels 2 and 3 of the gate driver 104 and the (4i+2)th and (4i+3)th gate lines G2, G3, G6, and G7 intersect, with an insulating layer in between. Due to this, as shown in FIG. 14, although the gate driver 104 outputs a third gate pulse through the third output channel 3 after outputting a second gate pulse through the second output channel 2, the third gate pulse is applied to the second gate line G2 after the second gate pulse is applied to the third gate line G3. Accordingly, gate pulses are applied to the gate lines G1 to G8 in order: G1, G3, G2, G4, G5, G7, G6, and G8.

[0122] FIGS. 15A to 16G show how data voltage transitions occur when a test pattern of various colors is displayed on the pixel array according to the third exemplary embodiment of the present invention.

[0123] FIGS. 15A to 15G are views showing which subpixels are lit up and their polarity, when white, red, green, blue, yellow, cyan, and magenta patterns are displayed on the pixel array according to the third exemplary embodiment of the present invention. FIGS. 16A to 16G are views showing data voltages when the colors of FIGS. 15A to 15G are displayed on the pixel array. The arrows in FIGS. 16A to 16G indicate data voltage transitions.

[0124] Referring to FIGS. 15A and 16A, when a white pattern is displayed on the pixels of the pixel array, the R subpixels, G subpixels, B subpixels, and W subpixels are all lit up at the white level. In the white pattern, the RGBW data voltages are the white-level voltage. For the white pattern to be displayed on the pixel array, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 13 change twice with a voltage swing of 2 V during 8 horizontal periods 8H. At these data voltages, the temperature of heat generated from the source drive ICs is 246 °C, as seen from Table 1.

[0125] Referring to FIGS. 15B and 16B, when a red pattern is displayed on the pixels of the pixel array, only the R subpixels are lit up at the white level. In the red pattern, the R data voltage is the white-level voltage, and the data voltages of the other colors are the black-level voltage. For the red pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 13 change once with a voltage swing of 1 V during 8 horizontal periods 8H. Since the data voltages applied to the odd-numbered data lines S1, S3, and S5 undergo no transition to the white-level voltage, the average number of transitions in data voltage applied to the data lines S1 to S5 during the 8 horizontal periods is 1. At these data voltages, the temperature of heat generated from the source drive ICs is 150 °C, as seen from Table 1.

[0126] Referring to FIGS. 15C and 16C, when a green pattern is displayed on the pixels of the pixel array, only the G subpixels are lit up at the white level. In the green pattern, the G data voltage is the white-level voltage, and the data voltages of the other colors are the black-level voltage. For the green pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 13 change twice with a voltage swing of 1 V during 8 horizontal periods 8H. At these data voltages, the temperature of heat generated from the source drive ICs is 201 °C, as seen from Table 1.

[0127] Referring to FIGS. 15D and 16D, when a blue pattern is displayed on the pixels of the pixel array, only the B subpixels are lit up at the white level. In the blue pattern, the B data voltage is the white-level voltage, and the data voltages of the other colors are the black-level voltage. For the blue pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 13 change once with a voltage swing of 1 V during 8 horizontal periods 8H. Since the data voltages applied to the even-numbered data lines S2 and S4 undergo no transition to the white-level voltage, the average number of transitions in data voltage applied to the data lines S1 to S5 during the 8 horizontal periods is 1. At these data voltages, the temperature of heat generated from the source drive ICs is 142 °C, as seen from Table 1.

[0128] Referring to FIGS. 15E and 16E, when a yellow pattern is displayed on the pixels of the pixel array, the G subpixels and the R subpixels are lit up at the white level. In the yellow pattern, the G data voltage and the R data voltage are the white-level voltage, and the data voltages of the other colors are the black-level voltage. For the yellow pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 13 change twice with a voltage swing of 1 V during 8 horizontal periods 8H. At these data voltages, the temperature of heat generated from the source drive ICs is 203 °C, as seen from Table 1.

[0129] Referring to FIGS. 15F and 16F, when a cyan pattern is displayed on the pixels of the pixel array, the G subpixels and the B subpixels are lit up at the white level. In the cyan pattern, the G data voltage and the B data voltage are the white-level voltage, and the data voltages of the other colors are the black-level voltage. For the cyan pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 13 change twice with a voltage swing of 1 V during 8 horizontal periods 8H. At these data voltages, the temperature of heat generated from the source drive ICs is 194 °C, as seen from Table 1.

[0130] Referring to FIGS. 15G and 16G, when a magenta pattern is displayed on the pixels of the pixel array, the B subpixels and the R subpixels are lit up at the white level. In the magenta pattern, the B data voltage and the R data voltage are the white-level voltage, and the data voltages of the other colors are the black-level voltage. For the magenta pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 13 change twice with a voltage swing of 1 V during 8 horizontal periods 8H. At these data voltages, the temperature of heat generated from the source drive ICs is 202 °C, as seen from Table 1.

[0131] As can be seen from above, in the third exemplary embodiment (FIGS. 12 to 14) of the present invention, the balance of polarity may be attained for each color without polarity banding phenomenon, and therefore input images

may be reproduced with high picture quality. In the third exemplary embodiment (FIGS. 12 to 14) of the present invention, the power consumption and heat generation of the source drive ICs may be reduced for every color.

[0132] FIGS. 17 and 18 are views showing a pixel array structure and a data voltage charging sequence according to a fourth exemplary embodiment of the present invention. FIG. 19 is a waveform diagram showing output signals from source drive ICs and a gate driver for driving the pixel array of FIGS. 17 and 18. The pixel array on the display panel 100 has a repeating structure of 4*8 subpixels as in FIG. 18. In FIGS. 17 and 18, the B and R above the first row line L1 indicate dummy subpixels that are charged with dummy data voltages prior to charging the first row line L1.

[0133] Referring to FIGS. 17 and 18, W subpixels W11, W12, W51, and W52 and G subpixels G11, G12, G51, and G52 are alternately arranged on the (4i+1)th row lines L1 and L5. The W subpixels W11, W12, W51, and W52 are arranged at positions where the (4i+1)th row lines L1 and L5 and the odd-numbered column lines C1 and C3 intersect. The G subpixels G11, G12, G51, and G52 are arranged at positions where the (4i+1)th row lines L1 and L5 and the even-numbered column lines C2 and C4 intersect.

[0134] The subpixels of first and second colors W and G arranged on the (4i+1)th row lines L1 and L5 comprise TFTs arranged at the intersections of the data lines to the left (second side) and the (4i+1)th gate lines G1 and G5, respectively. Each TFT supplies a data voltage from the data line to the left (second side) of the subpixel to the pixel electrode. The TFT of the W11 subpixel is referred to as a first TFT, the TFT of the G11 subpixel as a second TFT, the TFT of the W12 subpixel as a third TFT, and the TFT of the G12 subpixel as a fourth TFT. The first TFT supplies a W data voltage from the first data line S1 to the pixel electrode PXL of the W11 subpixel, in response to a first gate pulse from the first gate line G1. The second TFT supplies a G data voltage from the second data line S2 to the pixel electrode PXL of the G11 subpixel, in response to the first gate pulse from the first gate line G1. The third TFT supplies a W data voltage from the third data line S3 to the pixel electrode PXL of the W12 subpixel, in response to the first gate pulse from the first gate line G1. The fourth TFT supplies a G data voltage from the fourth data line S4 to the pixel electrode PXL of the G12 subpixel, in response to the first gate pulse from the first gate line G1.

[0135] R subpixels R21, R22, R61, and R62 and B subpixels B21, B22, B61, and B62 are alternately arranged on the (4i+2)th row lines L2 and L6. The R subpixels R21, R22, R61, and R62 are arranged at positions where the (4i+2)th row lines L2 and L6 and the odd-numbered column lines C1 and C3 intersect. The B subpixels B21, B22, B61, and B62 are arranged at positions where the (4i+2)th row lines L2 and L6 and the even-numbered column lines C2 and C4 intersect.

[0136] The subpixels of third and fourth colors R and B arranged on the (4i+2)th row lines L2 and L6 comprise TFTs arranged at the intersections of the data lines to the right (first side) and the (4i+2)th gate lines G2 and G6, respectively. Each TFT supplies a data voltage from the data line to the right (first side) of the subpixel to the pixel electrode. The TFT of the R21 subpixel is referred to as a fifth TFT, the TFT of the B21 subpixel as a sixth TFT, the TFT of the R22 subpixel as a seventh TFT, and the TFT of the B22 subpixel as an eighth TFT. The fifth TFT supplies an R data voltage from the second data line S2 to the pixel electrode PXL of the R21 subpixel, in response to a third gate pulse from the second gate line G2. The sixth TFT supplies a B data voltage from the third data line S3 to the pixel electrode PXL of the B21 subpixel, in response to the third gate pulse from the second gate line G2. The seventh TFT supplies an R data voltage from the fourth data line S4 to the pixel electrode PXL of the R22 subpixel, in response to the third gate pulse from the second gate line G2. The eighth TFT supplies a B data voltage from the fifth data line S5 to the pixel electrode PXL of the B22 subpixel, in response to the third gate pulse from the second gate line G2.

[0137] G subpixels G31, G32, G71, and G72 and W subpixels W31, W32, W71, and W72 are alternately arranged on the (4i+3)th row lines L3 and L7. The G subpixels G31, G32, G71, and G72 are arranged at positions where the (4i+3)th row lines L3 and L7 and the odd-numbered column lines C1 and C3 intersect. The W subpixels W31, W32, W71, and W72 are arranged at positions where the (4i+3)th row lines L3 and L7 and the even-numbered column lines C2 and C4 intersect.

[0138] The subpixels of the first and second colors W and G arranged on the (4i+3)th row lines L3 and L7 comprise TFTs arranged at the intersections of the data lines to the right (first side) and the (4i+3)th gate lines G3 and G7, respectively. Each TFT supplies a data voltage from the data line to the right (first side) of the subpixel to the pixel electrode. The TFT of the G31 subpixel is referred to as a ninth TFT, the TFT of the W31 subpixel as a tenth TFT, the TFT of the G32 subpixel as an eleventh TFT, and the TFT of the W32 subpixel as a twelfth TFT. The ninth TFT supplies a G data voltage from the second data line S2 to the pixel electrode PXL of the G31 subpixel, in response to a second gate pulse from the third gate line G3. The tenth TFT supplies a W data voltage from the third data line S3 to the pixel electrode PXL of the W31 subpixel, in response to the second gate pulse from the third gate line G3. The eleventh TFT supplies a G data voltage from the fourth data line S4 to the pixel electrode PXL of the G32 subpixel, in response to the second gate pulse from the third gate line G3. The twelfth TFT supplies a W data voltage from the fifth data line S5 to the pixel electrode PXL of the W32 subpixel, in response to the second gate pulse from the third gate line G3.

[0139] B subpixels B41, B42, B81, and B82 and R subpixels R41, R42, R81, and R82 are alternately arranged on the (4i+4)th row lines L4 and L8. The B subpixels B41, B42, B81, and B82 are arranged at positions where the (4i+4)th row lines L4 and L8 and the odd-numbered column lines C1 and C3 intersect. The R subpixels R41, R42, R81, and R82 are arranged at positions where the (4i+4)th row lines L4 and L8 and the even-numbered column lines C2 and C4 intersect.

[0140] The subpixels of the third and fourth colors R and B arranged on the (4i+4)th row lines L4 and L8 comprise TFTs arranged at the intersections of the data lines to the right (first side) and the (4i+4)th gate lines G4 and G8, respectively. Each TFT supplies a data voltage from the data line to the right (first side) of the subpixel to the pixel electrode. The TFT of the B41 subpixel is referred to as a thirteenth TFT, the TFT of the R41 subpixel as a fourteenth TFT, the TFT of the B42 subpixel as a fifteenth TFT, and the TFT of the R42 subpixel as a sixteenth TFT. The thirteenth TFT supplies a B data voltage from the second data line S2 to the pixel electrode PXL of the B41 subpixel, in response to a fourth gate pulse from the fourth gate line G4. The fourteenth TFT supplies an R data voltage from the third data line S3 to the pixel electrode PXL of the R41 subpixel, in response to the fourth gate pulse from the fourth gate line G4. The fifteenth TFT supplies a B data voltage from the fourth data line S4 to the pixel electrode PXL of the B42 subpixel, in response to the fourth gate pulse from the fourth gate line G4. The sixteenth TFT supplies an R data voltage from the fifth data line S5 to the pixel electrode PXL of the R42 subpixel, in response to the fourth gate pulse from the fourth gate line G4.

[0141] In order to reverse the polarity of data voltages once for every 4 dots, the source drive ICs output data voltages with first polarity during 4 horizontal periods 4H, and then output data voltages with second polarity during the next 4 horizontal periods 4H.

[0142] The data voltages supplied to the odd-numbered data lines S1, S3, and S5 are output from the source drive ICs during 4 horizontal periods 4H, in order: data voltage of the third color R, data voltage of the first color W, data voltage of the first color W, and data voltage of the fourth color B, and then their polarity is reversed. The polarity of the data voltages supplied to the odd-numbered data lines S1, S3, and S5 is reversed on the data voltages of the fourth color B.

[0143] The data voltages supplied to the even-numbered data lines S2 and S4 are output from the source drive ICs during 4 horizontal periods 4H, in order: data voltage of the fourth color B, data voltage of the second color G, data voltage of the second color G, and data voltage of the third color R, and then their polarity is reversed. The polarity of the data voltages supplied to the even-numbered data lines S2 and S4 is reversed on the data voltages of the fourth color B.

[0144] As shown in FIG. 19, the timing controller 20 controls in such a way that there is a difference of 1 horizontal period 1H between the polarity reversal timing of data voltages supplied to the odd-numbered data lines S1, S3, and S5 and the polarity reversal timing of data voltages supplied to the even-numbered data lines S2 and S4.

[0145] Link lines LNK connecting (4i+2)th and (4i+3)th output channels 2 and 3 of the gate driver 104 and the (4i+2)th and (4i+3)th gate lines G2, G3, G6, and G7 intersect, with an insulating layer in between. Due to this, as shown in FIG. 19, although the gate driver 104 outputs a third gate pulse through the third output channel 3 after outputting a second gate pulse through the second output channel 2, the third gate pulse is applied to the second gate line G2 after the second gate pulse is applied to the third gate line G3. Accordingly, gate pulses are applied to the gate lines G1 to G8 in order: G1, G3, G2, G4, G5, G7, G6, and G8.

[0146] FIGS. 20A to 21G show how data voltage transitions occur when a test pattern of various colors is displayed on the pixel array according to the fourth exemplary embodiment of the present invention.

[0147] FIGS. 20A to 20G are views showing which subpixels are lit up and their polarity, when white, red, green, blue, yellow, cyan, and magenta patterns are displayed on the pixel array, according to the fourth exemplary embodiment of the present invention. FIGS. 21A to 21G are views showing data voltages when the colors of FIGS. 20A to 20G are displayed on the pixel array. The arrows in FIGS. 21A to 21G indicate data voltage transitions.

[0148] Referring to FIGS. 20A and 21A, when a white pattern is displayed on the pixels of the pixel array, the R subpixels, G subpixels, B subpixels, and W subpixels are all lit up at the white level. In the white pattern, the RGBW data voltages are the white-level voltage. For the white pattern to be displayed on the pixel array, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 18 change twice with a voltage swing of 2 V during 8 horizontal periods 8H. At these data voltages, the temperature of heat generated from the source drive ICs is 246 °C, as seen from Table 1.

[0149] Referring to FIGS. 20B and 21B, when a red pattern is displayed on the pixels of the pixel array, only the R subpixels are lit up at the white level. In the red pattern, the R data voltage is the white-level voltage, and the data voltages of the other colors are the black-level voltage. For the red pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 18 change three times with a voltage swing of 1 V during 8 horizontal periods 8H. At these data voltages, the temperature of heat generated from the source drive ICs is 222 °C, as seen from Table 1.

[0150] Referring to FIGS. 20C and 21C, when a green pattern is displayed on the pixels of the pixel array, only the G subpixels are lit up at the white level. In the green pattern, the G data voltage is the white-level voltage, and the data voltages of the other colors are the black-level voltage. For the green pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 18 change once with a voltage swing of 1 V during 8 horizontal periods 8H. At these data voltages, the temperature of heat generated from the source drive ICs is 150 °C, as seen from Table 1.

[0151] Referring to FIGS. 20D and 21D, when a blue pattern is displayed on the pixels of the pixel array, only the B subpixels are lit up at the white level. In the blue pattern, the B data voltage is the white-level voltage, and the data voltages of the other colors are the black-level voltage. For the blue pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 18 change twice with a voltage swing of 1 V during 8 horizontal periods 8H. At these

data voltages, the temperature of heat generated from the source drive ICs is 201 °C, as seen from Table 1.

[0152] Referring to FIGS. 20E and 21E, when a yellow pattern is displayed on the pixels of the pixel array, the G subpixels and the R subpixels are lit up at the white level. In the yellow pattern, the G data voltage and the R data voltage are the white-level voltage (or highest voltage), and the data voltages of the other colors are the black-level voltage (or lowest voltage). For the yellow pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 18 change three times with a voltage swing of 1 V during 8 horizontal periods 8H. At these data voltages, the temperature of heat generated from the source drive ICs is 222 °C, as seen from Table 1.

[0153] Referring to FIGS. 20F and 21F, when a cyan pattern is displayed on the pixels of the pixel array, the G subpixels and the B subpixels are lit up at the white level. In the cyan pattern, the G data voltage and the B data voltage are the white-level voltage, and the data voltages of the other colors are the black-level voltage. For the cyan pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 18 change twice with a voltage swing of 1 V during 8 horizontal periods 8H. At these data voltages, the temperature of heat generated from the source drive ICs is 201 °C, as seen from Table 1.

[0154] Referring to FIGS. 20G and 21G, when a magenta pattern is displayed on the pixels of the pixel array, the B subpixels and the R subpixels are lit up at the white level. In the magenta pattern, the B data voltage and the R data voltage are the white-level voltage, and the data voltages of the other colors are the black-level voltage. For the magenta pattern, the data voltages supplied to the 8 lines L1 to L8 of subpixels shown in FIG. 18 change three times with a voltage swing of 1 V during 8 horizontal periods 8H. At these data voltages, the temperature of heat generated from the source drive ICs is 255 °C, as seen from Table 1.

[0155] As can be seen from above, in the fourth exemplary embodiment (FIGS. 17 to 19) of the present invention, the balance of polarity may be attained for each color without polarity banding phenomenon, and therefore input images may be reproduced with high picture quality. In the fourth exemplary embodiment (FIGS. 17 to 19) of the present invention, the power consumption and heat generation of the source drive ICs may be reduced for every color.

[0156] The following Table 1 shows the number of transitions in data voltage supplied to 8 lines during 8 horizontal periods, the data voltage swing, and the resulting temperature of heat generated from the source drive ICs in the first through fourth exemplary embodiment of the present invention, when colors of white, red, green, blue, yellow, cyan, and magenta are displayed.

[Table 1]

Color Pattern	First Exemplar Embodiment (FIGS. 2~4)		Second Exemplary Embodiment (FIGS. 7-9)		Third Exemplary Embodiment (FIGS. 12~14)		Fourth Exemplary Embodiment (FIGS. 17~19)	
	Number of Transitions within 8 lines	Expected Temperature of Heat Generation (°C)	Number of Transitions within lines	Expected Temperature of Heat Generation (°C)	Number of Transitions within 8 lines	Expected Temperature of Heat Generation (°C)	Number of Transitions within 8 lines	Expected Temperature of Heat Generation (°C)
White	2(2V)/8 H	246	2(2V)/8 H	246	2(2V)/8 H	246	2(2V)/8 H	246
Red	2/8H	201	1/8H	150	1/8H	150	3/8H	222
Green	2/8H	201	2/8H	201	2/8H	201	1/8H	150
Blue	2/8H	201	1/8H	142	1/8H	142	2/8H	201
Yellow	2/8H	201	3/8H	222	2/8H	203	3/8H	222
Cyan	2/8H	201	1/8H	150	2/8H	194	2/8H	201
Magenta	4/8H	355	2/8H	201	2/8H	202	3/8H	255

[0157] As described previously, in the present invention, the balance of polarity can be attained for each color without polarity banding phenomenon by optimizing an arrangement of colors on a display panel comprising subpixels of four colors, and therefore input images can be reproduced with high picture quality. Moreover, the power consumption and heat generation of the source drive ICs can be improved.

[0158] Although embodiments have been described with reference to a number of illustrative embodiments thereof, it should be understood that numerous other modifications and embodiments can be devised by those skilled in the art that will fall within the scope of the principles of this disclosure. More particularly, various variations and modifications are possible the component parts and/or arrangements of the subject combination arrangement within the scope of the disclosure, the drawings and the appended claims. In addition to variations and modifications in the component parts and/or arrangements, alternative uses will also be apparent to those skilled in the art.

Claims

1. A liquid crystal display device that comprises a display panel (100) with a pixel array and a display panel drive circuit for writing an input image to the display panel (100);
wherein the display panel drive circuit comprises a data driver (102), a gate driver (108), and a timing controller (110) wherein the display panel comprises a plurality data lines in a first direction and a plurality of gate lines in a second direction, wherein the first direction is orthogonal to the second direction; wherein the pixel array has a plurality of subpixels, and wherein each sub-pixel is arranged at a corresponding intersection of a data line (S1 to Sm) and a gate line (G1 to Gn) ; wherein the plurality of pixels comprise a plurality of first-color subpixels, a plurality of second-color subpixels, a plurality of third-color subpixels, and a plurality of fourth-color subpixels, being four mutually different colors, wherein each of the subpixels comprises a thin-film transistor, hereinafter referred to as TFT, that is connected to a pixel electrode of this respective subpixel; wherein the pixel array comprises a repeating subpixel matrix consisting of 8 subpixels arranged in a first to fourth directly adjacent rows of subpixels and first to second directly adjacent columns of subpixels, wherein the first row of the repeating subpixel matrix consists of a first-color subpixel (B11, B12) in the first column and a second-color subpixel (R11, R12) in the second column, wherein the second row of the repeating subpixel matrix consists of a third-color subpixel (W21, W22) in the first column and a fourth-color subpixel (G21, G22) in the second column, wherein the third row of the repeating subpixel matrix consists of a second-color subpixel (R31, R32) in the first column and a first-color subpixel (B31, B32) in the second column, wherein the fourth row of the repeating subpixel matrix consists of a fourth-color subpixel (G41, G42) in the first column and a third-color subpixel (W41, W42) in the second column, wherein the TFT of each of the subpixels of the first and third rows of the repeating subpixel matrix is connected to a respective directly adjacent data line on the right side of the subpixel, and wherein the TFT of each of the subpixels of the second and fourth rows of the repeating subpixel matrix is connected to a respective directly adjacent data line on the left side of the subpixel; wherein a gate electrode of the TFT of each of the subpixels of each row is connected to a gate line uniquely corresponding to each row; wherein the data driver (102) has source ICs, wherein data output channels of the source ICs are connected to the plurality of data lines (S1 to Sm), wherein the source ICs are configured to receive the data voltages and a polarity control signal (POL) from the timing controller (20) and are configured to reverse the polarity of data voltages supplied through one data line in response to the polarity control signal (POL) for charging subpixels on a preset cycle and are configured to supply the data voltages to the data lines (S1 to Sm), wherein the timing controller and the source ICs are configured such that, in response to the polarity control signal (POL), the polarity of the data voltages supplied to each of the data lines is reversed every 4 horizontal periods,
wherein the timing controller is configured to generate a polarity control signal (POL) for each of the source ICs so that there is a difference of 2 horizontal periods between the polarity reversal timing of data voltages supplied to odd-numbered data lines and the polarity reversal timing of data voltages supplied to even-numbered data lines so that neighbouring subpixels of the same color in the same row have opposite polarity and that neighbouring subpixels of the same color in the same column have opposite polarity.

2. The liquid crystal display device of claim 1, wherein the gate driver (104) is configured to supply gate pulses to the gate lines (G1 to Gn) in synchronization with the data voltages.

3. The liquid crystal display device of claim 2, wherein the gate driver (104) is configured to sequentially supply gate pulses to the gate lines (G1 to Gn) in order: first gate line (G1), second gate line (G2), third gate line (G3), and fourth gate line (G4).

4. The liquid crystal display device of one of the preceding claims, wherein the data driver (102) is configured to supply the data lines (S1 to Sm) with data voltages whose polarity is reversed on a cycle of every 4 horizontal periods.

5. The liquid crystal display device of one of the preceding claims, wherein the third-color- and fourth-color subpixels arranged on the (4i+2)th row lines (L2, L6) comprise TFTs that are configured to supply data voltages from the data lines (S1 to Sm) to the second side of the subpixels to the pixel electrodes, and wherein the first color- and second-color subpixels arranged on the (4i+3)th row lines (L3, L7) comprise TFTs that are configured to supply data voltages from the data lines (S1 to Sm) to the first side of the subpixels to the pixel electrodes, wherein the second side of the subpixels is opposite to the first side of that subpixel.

6. The liquid crystal display device of one of the claims 1 to 4, wherein the third-color- and fourth-color subpixels arranged on the (4i+2)th row lines (L2, L6) comprise TFTs that are configured to supply data voltages from the data lines (S1 to Sm) to the first side of the subpixels to the pixel electrodes, and the first-color- and second-color subpixels arranged on the (4i+3)th row lines (L3, L7) comprise TFTs that are configured to supply data voltages from the data lines (S1 to Sm) to the second side of the subpixels to the pixel electrodes, wherein the second side of the subpixels is opposite to the first side of that subpixels.

7. The liquid crystal display device of claim 6, wherein the data driver (102) is configured to supply the data lines (S1 to Sm) with the data voltages whose polarity is reversed on a cycle of every 4 horizontal periods, and is configured to simultaneously reverse the polarity of the data voltages supplied to the odd-numbered data lines (S1, S3, S5) and the polarity of the data voltages supplied to the even-numbered data lines (S2, S4),
wherein the polarity of the data voltages supplied to the odd-numbered data lines (S1, S3, S5) is reversed on data voltages of the fourth color, and the polarity of the data voltages supplied to the even-numbered data lines (S2, S4) is reversed on data voltages of the third color,
wherein, among link lines (LNK) connecting output channels of the gate driver (104) and the gate lines (G1 to Gn), the link lines (LNK) connecting the output channels of the second and third gate pulses and the second and third gate lines (G2, G3) intersect so that the third gate pulse is applied to the second gate line (G2) after the second gate pulse is applied to the third gate line (G3).

8. The liquid crystal display device of one of the claims 1 to 4, wherein the third-color- and fourth-color subpixels arranged on the (4i+2)th row lines (L2, L6) comprise TFTs that are configured to supply data voltages from the data lines (S1 to Sm) to the first side of the subpixels to the pixel electrodes, and the first color- and second-color subpixels arranged on the (4i+3)th row lines (L3, L7) comprise TFTs that are configured to supply data voltages from the data lines (S1 to Sm) to the first side of the subpixels to the pixel electrodes.

9. The liquid crystal display device of claim 8, wherein the polarity of the data voltages is supplied to the odd-numbered data lines (S1, S3, S5) is reversed on data voltages of the fourth color, and the polarity of the data voltages supplied to the even-numbered data lines (S2, S4) is reversed on data voltages of the second color, the fourth data voltage after reversal of the polarity of a data voltage supplied to each data line is a data voltage of the fourth color, and there is a difference of 1 horizontal period between the polarity reversal timing of data voltages supplied to the odd-numbered data lines (S1, S3, S5) and the polarity reversal timing of data voltages supplied to the even-numbered data lines (S2, S4),
wherein, among link lines (LNK) connecting output channels of the gate driver (104) and the gate lines (G1 to Gn), the link lines (LNK) connecting the output channels of the second and third gate pulses and the second and third gate lines (G2, G3) intersect so that the third gate pulse is applied to the second gate line (G2) after the second gate pulse is applied to the third gate line (G3).

10. The liquid crystal display device of one of the claims 1 to 4, wherein the first color- and second-color subpixels arranged on the (4i+1)th row lines (L1, L5) comprise TFTs (thin-film transistors) that are configured to supply data voltages from the data lines (S1 to Sm) to the second side of the subpixels to the pixel electrodes, the third-color- and fourth-color subpixels arranged on the (4i+2)th row lines (L2, L6) comprise TFTs that are configured to supply data voltages from the data lines (S1 to Sm) to the first side of the subpixels to the pixel electrodes, the first color- and second-color subpixels arranged on the (4i+3)th row lines (L3, L7) comprise TFTs that are configured to supply data voltages from the data lines (S1 to Sm) to the first side of the subpixels to the pixel electrodes, and the third-color- and fourth-color subpixels arranged on the (4i+4)th row lines (L4, L8) comprise TFTs that are configured to supply data voltages from the data lines (S1 to Sm) to the first side of the subpixels to the pixel electrodes, wherein the second side of the subpixels is opposite to the first side of that subpixels.

11. The liquid crystal display device of claim 10, wherein the polarity of the data voltages supplied to the data lines (S1 to Sm) is reversed on data voltages of the fourth color, and there is a difference of 1 horizontal period between the polarity reversal timing of data voltages supplied to the odd-numbered data lines (S1, S3, S5) and the polarity

reversal timing of data voltages supplied to the even-numbered data lines (S2, S4),
wherein, among link lines (LNK) connecting output channels of the gate driver (104) and the gate lines (G1 to Gn), the link lines (LNK) connecting the output channels of the second and third gate pulses and the second and third gate lines (G2, G3) intersect so that the third gate pulse is applied to the second gate line (G2) after the second gate pulse is applied to the third gate line (G3).

12. The liquid crystal display device of one of the preceding claims, wherein the first color is white (W), the second color is green (G), the third color is red (R), and the fourth color is blue (B).

13. A method for driving a liquid crystal display device according to one of the preceding claims, the display device comprises a display panel (100) with a pixel array and a display panel drive circuit for writing an input image to the display panel (100); wherein the display panel drive circuit comprises a data driver (102), a gate driver (108), and a timing controller (110), wherein the pixel array has a plurality of subpixels arranged in a matrix by intersections of data lines (S1 to Sm) and gate lines (G1 to Gn) intersecting the data lines (S1 to Sm), wherein the plurality of pixels comprises a plurality of first-color subpixels, a plurality of second-color subpixels, a plurality of third-color subpixels, and a plurality of fourth-color subpixels according to one of the preceding claims being four mutually different colors, wherein each of the colored subpixels comprises a thin-film transistor, TFT, that is connected to a pixel electrode of this respective subpixel, wherein the TFTs of the first-color subpixels and the second-color subpixels arranged on the (4i+1)th row lines (L1, L5), wherein i is a positive integer, are configured to supply data voltages from first data lines of the plurality of data lines (S1 to Sm) to respective pixel electrodes, wherein the first data lines are arranged on a first side of these subpixels, wherein the TFTs of the third-color- and fourth-color subpixels arranged on the (4i+4)th row lines (L4, L8) are configured to supply data voltages from second data lines of the plurality of data lines (S1 to Sm) to respective pixel electrodes, wherein the second data lines are arranged on a second side of these subpixels, wherein the second side is opposite to the first side, wherein first-color subpixels are arranged at positions where (4i+1)th row lines (L1, L5), wherein i is a positive integer, and odd-numbered column lines (C1, C3) intersect and are arranged at positions where the (4i+3)th row lines (L3, L7) and the even-numbered column lines (C2, C4) intersect, wherein the second-color subpixels are arranged at positions where the (4i+1)th row lines (LI, L5) and even-numbered column lines (C2, C4) intersect and are arranged at positions where (4i+3)th row lines (L3, L7) and the odd-numbered column lines (C1, C3) intersect, wherein the third-color subpixels are arranged at positions where (4i+2)th row lines (L2, L6) and the odd-numbered column lines (C1, C3) intersect and are arranged at positions where the (4i+4)th row lines (L4, L8) and the even-numbered column lines (C2, C4) intersect, wherein the fourth-color subpixels are arranged at positions where the (4i+2)th row lines (L2, L6) and the even-numbered column lines (C2, C4) intersect and are arranged at positions where (4i+4)th row lines (L4, L8) and the odd-numbered column lines (C1, C3) intersect, comprising the steps of:

Supplying the data lines (S1 to Sm) with data voltages whose polarity is reversed on a cycle of every 4 horizontal periods by means of a data driver (102) having source drive ICs, wherein data output channels of the source drive ICs are connected to the data lines (S1 to Sm), wherein data output channels of the source ICs are connected to the plurality of data lines (S1 to Sm), wherein the source ICs are configured to receive the data voltages and a polarity control signal (POL) from the timing controller (20) to reverse the polarity of data voltages supplied through one data line in response to the polarity control signal (POL) for charging the subpixels;
Suppling gate pulses to the gate lines (G1 to Gn) in synchronization with the data voltages in the order: first gate line (G1), second gate line (G2), third gate line (G3), and fourth gate line (G4) by means of a data driver (102), wherein in response to the polarity control signal (POL), the polarity of the data voltages supplied to the first data lines is kept the same for data voltages of the four colors with a first polarity and thereafter the polarity of the data voltages supplied to the first data lines is reversed to a second polarity, wherein the second polarity is reverse to the first polarity,
wherein in the polarity control signal there is a difference of at least two data voltage supply durations between the polarity reversal timing of data voltages supplied to the first data lines and the polarity reversal timing of data voltages supplied to the second data lines; and
wherein, among link lines connecting output channels of the gate driver (104) and the gate lines (G1 to Gn), the link lines connecting the output channels of the second and third gate pulses and the second and third gate lines (G2, G3) intersect so that the third gate pulse is applied to the second gate line (G2) after the second gate pulse is applied to the third gate line (G3).

Patentansprüche

1. Flüssigkristallanzeigevorrichtung, die eine Anzeigetafel (100) mit einer Pixelanordnung und eine Anzeigetafelansteuerungsschaltung zum Schreiben eines Eingangsbildes auf die Anzeigetafel (100) umfasst;
wobei die Anzeigetafelansteuerungsschaltung eine Datenansteuerung (102), eine Gate-Ansteuerung (108) und eine Zeitsteuereinheit (100) umfasst, wobei die Anzeigetafel mehrere Datenleitungen in einer ersten Richtung und mehrere Gate-Leitungen in einer zweiten Richtung umfasst, wobei die erste Richtung senkrecht zu der zweiten Richtung ist;
wobei die Pixelanordnung mehrere Unterpixel besitzt und wobei jedes Unterpixel an einer entsprechenden Kreuzung einer Datenleitung (S1 bis Sm) und einer Gate-Leitung (G1 bis Gn) angeordnet ist;
wobei die mehreren Pixel mehrere Unterpixel einer ersten Farbe, mehrere Unterpixel einer zweiten Farbe, mehrere Unterpixel einer dritten Farbe und mehrere Unterpixel einer vierten Farbe umfassen, die vier voneinander verschiedene Farben sind, wobei jedes der Unterpixel einen Dünnschichttransistor umfasst, nachstehend als TFT bezeichnet, der mit einer Pixelelektrode dieses jeweiligen Unterpixels verbunden ist;
wobei die Pixelanordnung eine sich wiederholende Unterpixelmatrix umfasst, die aus 8 Unterpixeln besteht, die in einer ersten bis vierten unmittelbar benachbarten Reihe von Unterpixeln und einer ersten bis zweiten unmittelbar benachbarten Spalte von Unterpixeln angeordnet sind, wobei die erste Reihe der sich wiederholenden Unterpixelmatrix aus einem Unterpixel einer ersten Farbe (B11, B12) in der ersten Spalte und einem Unterpixel einer zweiten Farbe (R11, R12) in der zweiten Spalte besteht, wobei die zweite Reihe der sich wiederholenden Unterpixelmatrix aus einem Unterpixel einer dritten Farbe (W21, W22) in der ersten Spalte und einem Unterpixel einer vierten Farbe (G21, G22) in der zweiten Spalte besteht, wobei die dritte Reihe der sich wiederholenden Unterpixelmatrix aus einem Unterpixel einer zweiten Farbe (R31, R32) in der ersten Spalte und einem Unterpixel einer ersten Farbe (B31, B32) in der zweiten Spalte besteht, wobei die vierte Reihe der sich wiederholden Unterpixelmatrix aus einem Unterpixel einer vierten Farbe (G41, G42) in der ersten Spalte und einem Unterpixel einer dritten Farbe (W41, W42) in der zweiten Spalte besteht, wobei der TFT jedes der Unterpixel der ersten und dritten Reihe der sich wiederholenden Unterpixelmatrix mit einer jeweiligen unmittelbar benachbarten Datenleitung auf der rechten Seite des Unterpixels verbunden ist und wobei der TFT jedes der Unterpixel der zweiten und vierten Reihe der sich wiederholenden Unterpixelmatrix mit einer jeweiligen unmittelbar benachbarten Datenleitung auf der linken Seite des Unterpixels verbunden ist; wobei eine Gate-Elektrode des TFT jedes der Unterpixel jeder Reihe mit einer Gate-Leitung, die eindeutig jeder Reihe entspricht, verbunden ist;
wobei die Datenansteuerung (102) Source-ICs besitzt, wobei die Datenausgangskanäle der Source-ICs mit den mehreren Datenleitungen (S1 bis Sm) verbunden sind, wobei die Source-ICs konfiguriert sind, die Datenspannungen und ein Polaritätssteuersignal (POL) von der Zeitsteuereinheit (20) zu empfangen, und konfiguriert sind, die Polarität der durch eine Datenleitung gelieferten Datenspannungen als Reaktion auf das Polaritätssteuersignal (POL) zum Laden von Unterpixeln auf einem voreingestellten Zyklus umzukehren, und konfiguriert sind, die Datenspannungen an die Datenleitungen (S 1 bis Sm) zu liefern,
wobei die Zeitsteuereinheit und die Source-ICs derart konfiguriert sind, dass als Reaktion auf das Polaritätssteuersignals (POL) die Polarität der Datenspannungen, die an jede der Datenleitungen geliefert werden, alle 4 horizontalen Perioden umgekehrt wird,
wobei die Zeitsteuereinheit konfiguriert ist, ein Polaritätssteuersignal (POL) für jede der Source-ICs zu erzeugen, so dass es einen Unterschied von 2 horizontalen Perioden zwischen der Polaritätsumkehrzeitvorgabe von Datenspannungen, die an ungeradzahlige Datenleitungen geliefert werden, und der Polaritätsumkehrzeitvorgabe von Datenspannungen, die an geradzahlige Datenleitungen geliefert werden, gibt, so dass benachbarte Unterpixel derselben Farbe in derselben Reihe entgegengesetzte Polarität aufweisen und dass benachbarte Unterpixel derselben Farbe in derselben Spalte entgegengesetzte Polarität aufweisen.

2. Flüssigkristallanzeigevorrichtung nach Anspruch 1, wobei die Gate-Ansteuerung (104) konfiguriert ist, die Gate-Impulse an die Gate-Leitungen (G1 bis Gn) in Synchronisation mit den Datenspannungen zu liefern.

3. Flüssigkristallanzeigevorrichtung nach Anspruch 2, wobei die Gate-Ansteuerung (104) konfiguriert ist, sequenziell Gate-Impulse an die Gate-Leitungen (G1 bis Gn) in der folgenden Reihenfolge zu liefern: erste Gate-Leitung (G1), zweite Gate-Leitung (G2), dritte Gate-Leitung (G3) und vierte Gate-Leitung (G4).

4. Flüssigkristallanzeigevorrichtung nach einem der vorhergehenden Ansprüche, wobei die Datenansteuerung (102) konfiguriert ist, die Datenleitungen (S1 bis Sm) mit Datenspannungen zu versorgen, deren Polarität auf einem Zyklus von je 4 horizontalen Perioden umgekehrt ist.

5. Flüssigkristallanzeigevorrichtung nach einem der vorhergehenden Ansprüche, wobei die Unterpixel der dritten Farbe

und der vierten Farbe, die auf den Leitungen (L2, L6) der (4i+2)-ten Reihe angeordnet sind, TFTs umfassen, die konfiguriert sind, Datenspannungen von den Datenleitungen (S1 bis Sm) an die zweite Seite der Unterpixel an die Pixelelektroden zu liefern, und wobei die Unterpixel der ersten Farbe und der zweiten Farbe, die auf den Leitungen (L3, L7) der (4i+3)-ten Reihe angeordnet sind, TFTs umfassen, die konfiguriert sind, Datenspannungen von den Datenleitungen (S1 bis Sm) an die erste Seite der Unterpixel an die Pixelelektroden zu liefern, wobei die zweite Seite der Unterpixel der ersten Seite dieses Unterpixels gegenüberliegt.

6. Flüssigkristallanzeigevorrichtung nach einem der Ansprüche 1 bis 4, wobei die Unterpixel der dritten Farbe und der vierten Farbe, die auf den Leitungen (L2, L6) der (4i+2)-ten Reihe angeordnet sind, TFTs umfassen, die konfiguriert sind, Datenspannungen von den Datenleitungen (S1 bis Sm) an die erste Seite der Unterpixel an die Pixelelektroden zu liefern, und die Unterpixel der ersten Farbe und der zweiten Farbe, die auf den Leitungen (L3, L7) der (4+3)-ten Reihe angeordnet sind, TFTs umfassen, die konfiguriert sind, Datenspannungen von den Datenleitungen (S1 bis Sm) an die zweite Seite der Unterpixel an die Pixelelektroden zu liefern, wobei die zweite Seite der Unterpixel der ersten Seite dieser Unterpixel gegenüberliegt.

7. Flüssigkristallanzeigevorrichtung nach Anspruch 6, wobei die Datenansteuerung (102) konfiguriert ist, die Datenleitungen (S1 bis Sm) mit den Datenspannungen, deren Polarität auf einem Zyklus von je 4 horizontalen Perioden umgekehrt ist, zu versorgen, und konfiguriert ist, die Polarität der Datenspannungen, die an die ungeradzahligen Datenleitungen (S1, S3, S5) geliefert werden, und die Polarität der Datenspannungen, die an die geradzahligen Datenleitungen (S2, S4) geliefert werden, gleichzeitig umzukehren,
wobei die Polarität der Datenspannungen, die an die ungeradzahligen Datenleitungen (S1, S3, S5) geliefert werden, an Datenspannungen der vierten Farbe umgekehrt wird und die Polarität der Datenspannungen, die an die geradzahligen Datenleitungen (S2, S4) geliefert werden, an Datenspannungen der vierten Farbe umgekehrt wird,
wobei sich unter den Verbindungsleitungen (LNK), die Ausgangskanäle der Gate-Ansteuerung (104) und die Gate-Leitungen (G1 bis Gn) verbinden, jene Verbindungsleitungen (LNK), die die Ausgangskanäle des zweiten und des dritten Gate-Impulses verbinden, und die zweite und die dritte Gate-Leitung (G2, G3) kreuzen, so dass der dritte Gate-Impuls an die zweite Gate-Leitung (G2) angelegt wird, nachdem der zweite Gate-Impuls an die dritte Gate-Leitung (G3) angelegt wird.

8. Flüssigkristallanzeigevorrichtung nach einem der Ansprüche 1 bis 4, wobei die Unterpixel der dritten Farbe und der vierten Farbe, die auf den Leitungen (L2, L6) der (4i-2)-ten Reihe angeordnet sind, TFTs umfassen, die konfiguriert sind, Datenspannungen von den Datenleitungen (S1 bis Sm) an die erste Seite der Unterpixel an die Pixelelektroden zu liefern und die Unterpixel der ersten Farbe und der zweiten Farbe, die auf den Leitungen (L3, L7) der (4i+3)-ten Reihe angeordnet sind, TFTs umfassen, die konfiguriert sind, Datenspannungen von den Datenleitungen (S1 bis Sm) an die erste Seite der Unterpixel an die Pixelelektroden zu liefern.

9. Flüssigkristallanzeigevorrichtung nach Anspruch 8, wobei die Polarität der Datenspannungen, die an die ungeradzahligen Datenleitungen (S1, S3, S5) geliefert werden, an Datenspannungen der vierten Farbe umgekehrt wird, und die Polarität der Datenspannungen, die an die geradzahligen Datenleitungen (S2, S4) geliefert werden, an Datenspannungen der zweiten Farbe umgekehrt wird, die vierte Datenspannung nach der Umkehrung der Polarität einer an jede Datenleitung gelieferten Datenspannung eine Datenspannung der vierten Farbe ist und es einen Unterschied 1 horizontalen Periode zwischen der Polaritätsumkehrzeitvorgabe von Datenspannungen, die an die ungeradzahligen Datenleitungen (S1, S3, S5) geliefert werden, und der Polaritätsumkehrzeitvorgabe von Datenspannungen, die an die geradzahligen Datenleitungen (S2, S4) geliefert werden, gibt,
wobei sich unter den Verbindungsleitungen (LNK), die Ausgangskanäle der Gate-Ansteuerung (104) und die Gate-Leitungen (G1 bis Gn) verbinden, jene Verbindungsleitungen (LNK), die die Ausgangskanäle des zweiten und des dritten Gate-Impulses verbinden, und die zweiten und dritten Gate-Leitungen (G2, G3) kreuzen, so dass der dritte Gate-Impuls an die zweite Gate-Leitung (G2) angelegt wird, nachdem der zweite Gate-Impuls an die dritte Gate-Leitung (G3) angelegt wird.

10. Flüssigkristallanzeigevorrichtung nach einem der Ansprüche 1 bis 4, wobei die Unterpixel der ersten Farbe und der zweiten Farbe, die auf den Leitungen (L1, L5) der (4i+1)-ten Reihe angeordnet sind, TFTs (Dünnschichttransistoren) umfassen, die konfiguriert sind, Datenspannungen von den Datenleitungen (S1 bis Sm) an die zweite Seite der Unterpixel an die Pixelelektroden zu liefern, die Unterpixel der dritten Farbe und der vierten Farbe, die auf den Leitungen (L2, L6) der (4i+2)-ten Reihe angeordnet sind, TFTs umfassen, die konfiguriert sind, Datenspannungen von den Datenleitungen (S1 bis Sm) an die erste Seite der Unterpixel an die Pixelelektroden zu liefern, die Unterpixel der ersten Farbe und der zweiten Farbe, die auf den Leitungen (L3, L7) der (4i+3)-ten Reihe angeordnet sind, TFTs umfassen, die konfiguriert sind, Datenspannungen von den Datenleitungen (S1 bis Sm) an die erste Seite der

Unterpixel an die Pixelelektroden zu liefern und die Unterpixel der dritten Farbe und der vierten Farbe, die auf den Leitungen (L4, L8) der (4i+4)-ten Reihe angeordnet sind, TFTs umfassen, die konfiguriert sind, Datenspannungen von den Datenleitungen (S1 bis Sm) an die erste Seite der Unterpixel an die Pixelelektroden zu liefern, wobei die zweite Seite der Unterpixel der ersten Seite dieser Unterpixel gegenüberliegt.

11. Flüssigkristallanzeigevorrichtung nach Anspruch 10, wobei die Polarität der Datenspannungen, die an die Datenleitungen (S1 bis Sm) geliefert werden, an Datenspannungen der vierten Farbe umgekehrt wird, und es einen Unterschied von 1 horizontalen Periode zwischen der Polaritätsumkehrzeitvorgabe von Datenspannungen, die an die ungeradzahligen Datenleitungen (S1, S3, S5) geliefert werden, und der Polaritätsumkehrzeitvorgabe von Datenspannungen, die an die geradzahligen Datenleitungen (S2, S4) geliefert werden, gibt,
wobei sich unter den Verbindungsleitungen (LNK), die Ausgangskanäle der Gate-Ansteuerung (104) und die Gate-Leitungen (G1 bis Gn) verbinden, jene Verbindungsleitungen (LNK), die die Ausgangskanäle des zweiten und des dritten Gate-Impulses verbinden, und die zweiten und dritten Gate-Leitungen (G2, G3) kreuzen, so dass der dritte Gate-Impuls an die zweite Gate-Leitung (G2) angelegt wird, nachdem der zweite Gate-Impuls an die dritte Gate-Leitung (G33) angelegt wird.

12. Flüssigkristallanzeigevorrichtung nach einem der vorhergehenden Ansprüche, wobei die erste Farbe Weiß (W) ist, die zweite Farbe Grün (G) ist, die dritte Farbe Rot (R) ist und die vierte Farbe Blau (B) ist.

13. Verfahren zum Ansteuern einer Flüssigkristallanzeigevorrichtung nach einem der vorhergehenden Ansprüche, wobei die Anzeigevorrichtung eine Anzeigetafel (100) mit einer Pixelanordnung und eine Anzeigetafelansteuerungsschaltung zum Schreiben eines Eingangsbilds auf die Anzeigetafel (100) umfasst; wobei die Anzeigetafelansteuerungsschaltung eine Datenansteuerung (102), eine Gate-Ansteuerung (108) und eine Zeitsteuereinheit (110) umfasst, wobei die Pixelanordnung mehrere Unterpixel besitzt, die in einer Matrix durch Kreuzungen von Datenleitungen (S1 bis Sm) und Gate-Leitungen (G1 bis Gn), die die Datenleitungen (S1 bis Sm) kreuzen, angeordnet sind, wobei die mehreren Pixel mehrere Unterpixel einer ersten Farbe, mehrere Unterpixel einer zweiten Farbe, mehrere Unterpixel einer dritten Farbe und mehrere Unterpixel einer vierten Farbe umfassen, gemäß einem der vorhergehenden Ansprüche, die vier voneinander verschiedene Farben sind, wobei jedes der farbigen Unterpixel einen Dünnschichttransistor, TFT, umfasst,
der mit einer Pixelelektrode dieses jeweiligen Unterpixels verbunden ist, wobei die TFTs der Unterpixel der ersten Farbe und die Unterpixel der zweiten Farbe, die auf den Leitungen (L1, L5) der (4i+1)-ten Reihe angeordnet sind, wobei i eine positive ganze Zahl ist, konfiguriert sind, Datenspannungen von den ersten Datenleitungen der mehreren Datenleitungen (S1 bis Sm) an jeweilige Pixelelektroden zu liefern, wobei die ersten Datenleitungen auf einer ersten Seite dieser Unterpixel angeordnet sind, wobei die TFTs der Unterpixel der dritten Farbe und der vierten Farbe, die auf den Leitungen (L4, L8) der (4i+4)-ten Reihe angeordnet sind, konfiguriert sind, Datenspannungen von zweiten Datenleitungen der mehreren Datenleitungen (S1 bis Sm) an jeweilige Pixelelektroden zu liefern, wobei die zweiten Datenleitungen auf einer zweiten Seite dieser Unterpixel angeordnet sind, wobei die zweite Seite der ersten Seite gegenüberliegt, wobei die Unterpixel der ersten Farbe an Positionen angeordnet sind, wo sich Leitungen (L1, L5) der (4i+1)-ten Reihe, wobei i eine positive ganze Zahl ist, und ungeradzahlige Leitungen (C1, C3) kreuzen, und an Positionen angeordnet sind, wo sich die Leitungen (L3, L7) der (4i+3)-ten Reihe und die geradzahligen Spaltenleitungen (C2, C4) kreuzen, wobei die Unterpixel der zweiten Farbe an Positionen angeordnet sind, wo sich die Leitungen (L1, L5) der (4i+1)-ten Reihe und die geradzahligen Spaltenleitungen (C2, C4) kreuzen, und an Positionen angeordnet sind, wo sich die Leitungen (L3, L7) der (4i+3)-ten Reihe und die ungeradzahligen Spaltenleitungen (C1, C3) kreuzen, wobei die Unterpixel der dritten Farbe an Positionen angeordnet sind, wo sich die Leitungen (L2, L6) der (4i+2)-ten Reihe und die ungeradzahligen Spaltenleitungen (C1, C3) kreuzen, und an Positionen angeordnet sind, wo sich die Leitungen (L4, L8) der (4i+4)-ten Reihe und die geradzahligen Spaltenleitungen (C2, C4) kreuzen, wobei die Unterpixel der vierten Farbe an Positionen angeordnet sind, wo sich die Leitungen (L2, L6) der (4i+2)-ten Reihe und die geradzahligen Spaltenleitunen (C2, C4) kreuzen, und an Positionen angeordnet sind, wo sich die Leitungen (L4, L8) der (4i+4)-ten Reihe und die ungeradzahligen Spaltenleitungen (C1, C3) kreuzen, das die Schritte umfasst:

Versorgen der Datenleitungen (S1 bis Sm) mit Datenspannungen, deren Polarität auf einem Zyklus von je 4 horizontalen Perioden mit Hilfe einer Datenansteuerung (102) mit Source-Ansteuerungs-ICs umgekehrt wird, wobei die Datenausgangskanäle der Source-Ansteuerungs-ICs mit den Datenleitungen (S1 bis Sm) verbunden sind, wobei die Datenausgangskanäle der Source-ICs mit den mehreren Datenleitungen (S1 bis Sm) verbunden sind, wobei die Source-ICs konfiguriert sind, die Datenspannungen und ein Polaritätssteuersignal (POL) von der Zeitsteuereinheit (20) zu empfangen, um die Polarität von Datenspannungen, die durch eine Datenleitung geliefert werden, als Reaktion auf das Polaritätssteuersignal (POL) zum Laden der Unterpixel umzukehren;

Liefern von Gate-Impulsen an die Gate-Leitungen (G1 bis Gn) in Synchronisation mit den Datenspannungen in der Reihenfolge: erste Gate-Leitung (G1), zweite Gate-Leitung (G2), dritte Gate-Leitung (G3) und vierte Gate-Leitung (G4) mit Hilfe einer Datenansteuerung (102),
wobei als Reaktion auf das Polaritätssteuersignal (POL) die Polarität der Datenspannungen, die an die ersten Datenleitungen geliefert werden, für Datenspannungen der vier Farben mit einer ersten Polarität dieselbe gehalten wird und danach die Polarität der Datenspannungen, die an die ersten Datenleitungen geliefert werden, zu einer zweiten Polarität umgekehrt werden, wobei die zweite Polarität umgekehrt zu der ersten Polarität ist, wobei das Polaritätssteuersignal dort ein Unterschied von mindestens zwei Datenspannungslieferdauern zwischen der Polaritätsumkehrzeitvorgabe von Datenspannungen, die an die ersten Datenleitungen geliefert werden, und der Polaritätsumkehrzeitvorgabe von Datenspannungen, die an die zweiten Datenleitungen geliefert werden, ist; und
wobei sich unter den Verbindungsleitungen, die Ausgangskanäle der Gate-Ansteuerung (104) und die Gate-Leitungen (G1 bis Gn) verbinden, jene Verbindungsleitungen, die die Ausgangskanäle des zweiten und des dritten Gate-Impulses verbinden, und die zweiten und dritten Gate-Leitungen (G2, G3) kreuzen, so dass der dritte Gate-Impuls an die zweite Gate-Leitung (G2) angelegt wird, nachdem der zweite Gate-Impuls an die dritte Gate-Leitung (G3) angelegt wird.

Revendications

1. Dispositif d'affichage à cristaux liquides comprenant un panneau d'affichage (100) avec un réseau de pixels et un circuit de pilotage de panneau d'affichage pour écrire une image d'entrée sur le panneau d'affichage (100) ;
dans lequel le circuit de pilotage de panneau d'affichage comprend un circuit d'attaque de données (102), un circuit d'attaque de grille (108), et un organe de commande de timing (110), dans lequel le panneau d'affichage comprend une pluralité de lignes de données dans un premier sens et une pluralité de lignes de grille dans un deuxième sens, dans lequel le premier sens est orthogonal au deuxième sens ;
dans lequel le réseau de pixels comporte une pluralité de sous-pixels, et dans lequel chaque sous-pixel est agencé à une intersection correspondante d'une ligne de données (S1 à Sm) et d'une ligne de grille (G1 à Gn) ;
dans lequel la pluralité de pixels comprennent une pluralité de sous-pixels de première couleur, une pluralité de sous-pixels de deuxième couleur, une pluralité de sous-pixels de troisième couleur, et une pluralité de sous-pixels de quatrième couleur, les quatre couleurs étant différentes l'une de l'autre, dans lequel chacun des sous-pixels comprend un transistor à film mince, TFT, qui est raccordé à une électrode de pixel de ce sous-pixel respectif ;
dans lequel le réseau de pixels comprend une matrice de sous-pixels à répétition se composant de 8 sous-pixels agencés dans des première à quatrième rangées directement adjacentes de sous-pixels et des première et deuxième colonnes directement adjacentes de sous-pixels, dans lequel la première rangée de la matrice de sous-pixels à répétition se compose d'un sous-pixel de première couleur (B11, B12) dans la première colonne et d'un sous-pixel de deuxième couleur (R11, R12) dans la deuxième colonne, dans lequel la deuxième rangée de la matrice de sous-pixels à répétition se compose d'un sous-pixel de troisième couleur (W21, W22) dans la première colonne et d'un sous-pixel de quatrième couleur (G21, G22) dans la deuxième colonne, dans lequel la troisième rangée de la matrice de sous-pixels à répétition se compose d'un sous-pixel de deuxième couleur (R31, R32) dans la première colonne et d'un sous-pixel de première couleur (B31, B32) dans la deuxième colonne, dans lequel la quatrième rangée de la matrice de sous-pixels à répétition se compose d'un sous-pixel de quatrième couleur (G41, G42) dans la première colonne et d'un sous-pixel de troisième couleur (W41, W42) dans la deuxième colonne, dans lequel le TFT de chacun des sous-pixels des première et troisième rangées de la matrice de sous-pixels à répétition est raccordé à une ligne de données directement adjacente respective sur le côté droit du sous-pixel, et dans lequel le TFT de chacun des sous-pixels des deuxième et quatrième rangées de la matrice de sous-pixels à répétition est raccordé à une ligne de données directement adjacente respective sur le côté gauche du sous-pixel ; dans lequel une électrode de grille du TFT de chacun des sous-pixels de chaque rangée est raccordée à une ligne de grille correspondant de manière unique à chaque rangée ;
dans lequel le circuit d'attaque de données (102) comporte des IC de source, dans lequel des canaux de sortie de données des IC de source sont raccordés à la pluralité de lignes de données (S1 à Sm), dans lequel les IC de source sont configurés pour recevoir les tensions de données et un signal de commande de polarité (POL) en provenance de l'organe de commande de timing (20) et sont configurés pour inverser la polarité de tensions de données fournies par l'intermédiaire d'une ligne de données en réponse au signal de commande de polarité (POL) pour charger des sous-pixels sur un cycle préréglé et sont configurés pour fournir les tensions de données aux lignes de données (S1 à Sm),
dans lequel l'organe de commande de timing et les IC de source sont configurés de sorte que, en réponse au signal de commande de polarité (POL), la polarité des tensions de données fournies à chacune des lignes de données

est inversée toutes les 4 périodes horizontales,
dans lequel l'organe de commande de timing est configuré pour générer un signal de commande de polarité (POL) pour chacun des IC de source de sorte qu'il existe une différence de 2 périodes horizontales entre le timing d'inversion de polarité de tensions de données fournies à des lignes de données de numéros impairs et le timing d'inversion de polarité de tensions de données fournies à des lignes de données de numéros pairs afin que des sous-pixels voisins de la même couleur dans la même rangée présentent une polarité opposée et des sous-pixels voisins de la même couleur dans la même colonne présentent une polarité opposée.

2. Dispositif d'affichage à cristaux liquides selon la revendication 1, dans lequel le circuit d'attaque de grille (104) est configuré pour fournir des impulsions de grille aux lignes de grille (G1 à Gn) en synchronisation avec les tensions de données.

3. Dispositif d'affichage à cristaux liquides selon la revendication 2, dans lequel le circuit d'attaque de grille (104) est configuré pour fournir séquentiellement des impulsions de grille aux lignes de grille (G1 à Gn) dans l'ordre suivant : première ligne de grille (G1), deuxième ligne de grille (G2), troisième ligne de grille (G3), et quatrième ligne de grille (G4).

4. Dispositif d'affichage à cristaux liquides selon l'une des revendications précédentes, dans lequel le circuit d'attaque de données (102) est configuré pour fournir, aux lignes de données (S1 à Sm), des tensions de données dont la polarité est inversée sur un cycle toutes les 4 périodes horizontales.

5. Dispositif d'affichage à cristaux liquides selon l'une des revendications précédentes, dans lequel les sous-pixels de troisième couleur et de quatrième couleur agencés sur les (4i+2)èmes lignes de rangée (L2, L6) comprennent des TFT qui sont configurés pour fournir des tensions de données des lignes de données (S1 à Sm) sur le deuxième côté des sous-pixels aux électrodes de pixel, et dans lequel les sous-pixels de première couleur et de deuxième couleur agencés sur les (4i+3)èmes lignes de rangée (L3, L7) comprennent des TFT qui sont configurés pour fournir des tensions de données des lignes de données (S1 à Sm) sur le premier côté des sous-pixels aux électrodes de pixel, dans lequel le deuxième côté des sous-pixels est à l'opposé du premier côté de ce sous-pixel.

6. Dispositif d'affichage à cristaux liquides selon l'une des revendications 1 à 4, dans lequel les sous-pixels de troisième couleur et de quatrième couleur agencés sur les (4i+2)èmes lignes de rangée (L2, L6) comprennent des TFT qui sont configurés pour fournir des tensions de données des lignes de données (S1 à Sm) sur le premier côté des sous-pixels aux électrodes de pixel, et dans lequel les sous-pixels de première couleur et de deuxième couleur agencés sur les (4i+3)èmes lignes de rangée (L3, L7) comprennent des TFT qui sont configurés pour fournir des tensions de données des lignes de données (S1 à Sm) sur le deuxième côté des sous-pixels aux électrodes de pixel, dans lequel le deuxième côté des sous-pixels est à l'opposé du premier côté de ces sous-pixels.

7. Dispositif d'affichage à cristaux liquides selon la revendication 6, dans lequel le circuit d'attaque de données (102) est configuré pour fournir, aux lignes de données (S1 à Sm), les tensions de données dont la polarité est inversée sur un cycle toutes les 4 périodes horizontales, et est configuré pour inverser simultanément la polarité des tensions de données fournies aux lignes de données de numéros impairs (S1, S3, S5) et la polarité des tensions de données fournies aux lignes de données de numéros pairs (S2, S4),
dans lequel la polarité des tensions de données fournies aux lignes de données de numéros impairs (S1, S3, S5) est inversée sur des tensions de données de la quatrième couleur, et la polarité des tensions de données fournies aux lignes de données de numéros pairs (S2, S4) est inversée sur des tensions de données de la troisième couleur,
dans lequel, parmi des lignes de liaison (LNK) raccordant des canaux de sortie du circuit d'attaque de grille (104) et les lignes de grille (G1 à Gn), les lignes de liaison (LNK) raccordant les canaux de sortie des deuxième et troisième impulsions de grille et les deuxième et troisième lignes de grille (G2, G3) sont en intersection de sorte que la troisième impulsion de grille soit appliquée à la deuxième ligne de grille (G2) après que la deuxième impulsion de grille est appliquée à la troisième ligne de grille (G3) .

8. Dispositif d'affichage à cristaux liquides selon l'une des revendications 1 à 4, dans lequel les sous-pixels de troisième couleur et de quatrième couleur agencés sur les (4i+2)èmes lignes de rangée (L2, L6) comprennent des TFT qui sont configurés pour fournir des tensions de données des lignes de données (S1 à Sm) sur le premier côté des sous-pixels aux électrodes de pixels, et les sous-pixels de première couleur et de deuxième couleur agencés sur les (4i+3)èmes lignes de rangée (L3, L7) comprennent des TFT qui sont configurés pour fournir des tensions de données des lignes de données (S1 à Sm) sur le premier côté des sous-pixels aux électrodes de pixels.

9. Dispositif d'affichage à cristaux liquides selon la revendication 8, dans lequel la polarité des tensions de données fournies aux lignes de données de numéros impairs (S1, S3, S5) est inversée sur des tensions de données de la quatrième couleur, et la polarité des tensions de données fournies aux lignes de données de numéros pairs (S2, S4) est inversée sur des tensions de données de la deuxième couleur, la quatrième tension de données après l'inversion de la polarité d'une tension de données fournie à chaque ligne de données est une tension de données de la quatrième couleur, et il existe une différence de 1 période horizontale entre le timing d'inversion de polarité de tensions de données fournies aux lignes de données de numéros impairs (S1, S3, S5) et le timing d'inversion de polarité de tensions de données fournies aux lignes de données de numéros pairs (S2, S4),
dans lequel, parmi des lignes de liaison (LNK) raccordant des canaux de sortie du circuit d'attaque de grille (104) et les lignes de grille (G1 à Gn), les lignes de liaison (LNK) raccordant les canaux de sortie des deuxième et troisième impulsions de grille et les deuxième et troisième lignes de grille (G2, G3) sont en intersection de sorte que la troisième impulsion de grille soit appliquée à la deuxième ligne de grille (G2) après que la deuxième impulsion de grille est appliquée à la troisième ligne de grille (G3) .

10. Dispositif d'affichage à cristaux liquides selon l'une des revendications 1 à 4, dans lequel les sous-pixels de première couleur et de deuxième couleur agencés sur les (4i+1)èmes lignes de rangée (L1, L5) comprennent des TFT (transistors à film mince) qui sont configurés pour fournir des tensions de données des lignes de données (S1 à Sm) sur le deuxième côté des sous-pixels aux électrodes de pixel, les sous-pixels de troisième couleur et de quatrième couleur agencés sur les (4i+2)èmes lignes de rangée (L2, L6) comprennent des TFT qui sont configurés pour fournir des tensions de données des lignes de données (S1 à Sm) sur le premier côté des sous-pixels aux électrodes de pixel, les sous-pixels de première couleur et de deuxième couleur agencés sur les (4i+3)èmes lignes de rangée (L3, L7) comprennent des TFT qui sont configurés pour fournir des tensions de données des lignes de données (S1 à Sm) sur le premier côté des sous-pixels aux électrodes de pixel, et les sous-pixels de troisième couleur et de quatrième couleur agencés sur les (4i+4)èmes lignes de rangée (L4, L8) comprennent des TFT qui sont configurés pour fournir des tensions de données des lignes de données (S1 à Sm) sur le premier côté des sous-pixels aux électrodes de pixel, dans lequel le deuxième côté des sous-pixels est à l'opposé du premier côté de ces sous-pixels.

11. Dispositif d'affichage à cristaux liquides selon la revendication 10, dans lequel la polarité des tensions de données fournies aux lignes de données (S1 à Sm) est inversée sur des tensions de données de la quatrième couleur, et il existe une différence de 1 période horizontale entre le timing d'inversion de polarité de tensions de données fournies aux lignes de données de numéros impairs (S1, S3, S5) et le timing d'inversion de polarité de tensions de données fournies aux lignes de données de numéros pairs (S2, S4),
dans lequel, parmi des lignes de liaison (LNK) raccordant des canaux de sortie du circuit d'attaque de grille (104) et les lignes de grille (G1 à Gn), les lignes de liaison (LNK) raccordant les canaux de sortie des deuxième et troisième impulsions de grille et les deuxième et troisième lignes de grille (G2, G3) sont en intersection de sorte que la troisième impulsion de grille soit appliquée à la deuxième ligne de grille (G2) après que la deuxième impulsion de grille est appliquée à la troisième ligne de grille (G3) .

12. Dispositif d'affichage à cristaux liquides selon l'une des revendications précédentes, dans lequel la première couleur est le blanc (W), la deuxième couleur est le vert (G), la troisième couleur est le rouge (R), et la quatrième couleur est le bleu (B).

13. Procédé de pilotage d'un dispositif d'affichage à cristaux liquides selon l'une des revendications précédentes, le dispositif d'affichage comprenant un panneau d'affichage (100) avec un réseau de pixels et un circuit de pilotage de panneau d'affichage pour écrire une image d'entrée sur le panneau d'affichage (100) ; dans lequel le circuit de pilotage de panneau d'affichage comprend un circuit d'attaque de données (102), un circuit d'attaque de grille (108), et un organe de commande de timing (110), dans lequel le réseau de pixels comporte une pluralité de sous-pixels agencés dans une matrice par des intersections de lignes de données (S1 à Sm) et de ligne de grille (G1 à Gn) en intersection avec les lignes de données (S1 à Sm), dans lequel la pluralité de pixels comprennent une pluralité de sous-pixels de première couleur, une pluralité de sous-pixels de deuxième couleur, une pluralité de sous-pixels de troisième couleur, et une pluralité de sous-pixels de quatrième couleur selon l'une des revendications précédentes, les quatre couleurs étant différentes l'une de l'autre, dans lequel chacun des sous-pixels de couleur comprend un transistor à film mince, TFT, qui est raccordé à une électrode de pixel de ce sous-pixel respectif, dans lequel les TFT des sous-pixels de première couleur et des sous-pixels de deuxième couleur agencés sur les (4i+1)èmes lignes de rangée (L1, L5), où i est un nombre entier positif, sont configurés pour fournir des tensions de données de premières lignes de données de la pluralité de lignes de données (S1 à Sm) à des électrodes de pixel respectives, dans lequel les premières lignes de données sont agencées sur un premier côté de ces sous-pixels, dans lequel

les TFT des sous-pixels de troisième couleur et de quatrième couleur agencés sur les (4i+4)èmes lignes de rangée (L4, L8) sont configurés pour fournir des tensions de données de deuxièmes lignes de données de la pluralité de lignes de données (S1 à Sm) à des électrodes de pixel respectives, dans lequel les deuxièmes lignes de données sont agencées sur un deuxième côté de ces sous-pixels, dans lequel le deuxième côté est à l'opposé du premier côté, dans lequel des sous-pixels de première couleur sont agencés à des positions auxquelles des (4i+1)èmes lignes de rangée (L1, L5), où i est un nombre entier positif, et des lignes de colonne de numéros impairs (C1, C3) sont en intersection et sont agencés à des positions auxquelles des (4i+3)èmes lignes de rangée (L3, L7) et des lignes de colonne de numéros pairs (C2, C4) sont en intersection, dans lequel les sous-pixels de deuxième couleur sont agencés à des positions auxquelles des (4i+1)èmes lignes de rangée (L1, L5) et des lignes de colonne de numéros pairs (C2, C4) sont en intersection et sont agencés à des positions auxquelles des (4i+3)èmes lignes de rangée (L3, L7) et les lignes de colonne de numéros impairs (C1, C3) sont en intersection, dans lequel les sous-pixels de troisième couleur sont agencés à des positions auxquelles des (4i+2)èmes lignes de rangée (L2, L6) et les lignes de colonne de numéros impairs (C1, C3) sont en intersection et sont agencés à des positions auxquelles les (4i+4)èmes lignes de rangée (L4, L8) et les lignes de colonne de numéros pairs (C2, C4) sont en intersection, dans lequel les sous-pixels de quatrième couleur sont agencés à des positions auxquelles les (4i+2)èmes lignes de rangée (L2, L6) et les lignes de colonne de numéros pairs (C2, C4) sont en intersection et sont agencés à des positions auxquelles des (4i+4)èmes lignes de rangée (L4, L8) et les lignes de colonne de numéros impairs (C1, C3) sont en intersection, comprenant les étapes de :

la fourniture, aux lignes de données (S1 à Sm), de tensions de données dont la polarité est inversée sur un cycle toutes les 4 périodes horizontales au moyen d'un circuit d'attaque de données (102) comportant des IC de pilotage de source, dans lequel des canaux de sortie de données des IC de pilotage de source sont raccordés aux lignes de données (S1 à Sm), dans lequel des canaux de sortie de données des IC de source sont raccordés à la pluralité de lignes de données (S1 à Sm), dans lequel les IC de source sont configurées pour recevoir les tensions de données et un signal de commande de polarité (POL) en provenance de l'organe de commande de timing (20) pour inverser la polarité de tensions de données fournies par l'intermédiaire d'une ligne de données en réponse au signal de commande de polarité (POL) pour charger les sous-pixels ;
la fourniture d'impulsions de grille aux lignes de grille (G1 à Gn) en synchronisation avec les tensions de données dans l'ordre de : première ligne de grille (G1), deuxième ligne de grille (G2), troisième ligne de grille (G3) et quatrième ligne de grille (G4) au moyen d'un circuit d'attaque de données (102),
dans lequel, en réponse au signal de commande de polarité (POL), la polarité des tensions de données fournies aux premières lignes de données est maintenue identique pour des tensions de données des quatre couleurs avec une première polarité, puis la polarité des tensions de données fournies aux premières lignes de données est inversée à une deuxième polarité, dans lequel la deuxième polarité est l'inverse de la première polarité,
dans lequel, dans le signal de commande de polarité, il existe une différence d'au moins deux durées d'alimentation de tension de données entre le timing d'inversion de polarité de tensions de données fournies aux premières lignes de données et le timing d'inversion de polarité de tensions de données fournies aux deuxièmes lignes de données ; et
dans lequel, parmi des lignes de liaison raccordant des canaux de sortie du circuit d'attaque de grille (104) et les lignes de grille (G1 à Gn), les lignes de liaison raccordant les canaux de sortie des deuxième et troisième impulsions de grille et les deuxième et troisième lignes de grille (G2, G3) sont en intersection de sorte que la troisième impulsion de grille soit appliquée à la deuxième ligne de grille (G2) après que la deuxième impulsion de grille est appliquée à la troisième ligne de grille (G3).

FIG. 1

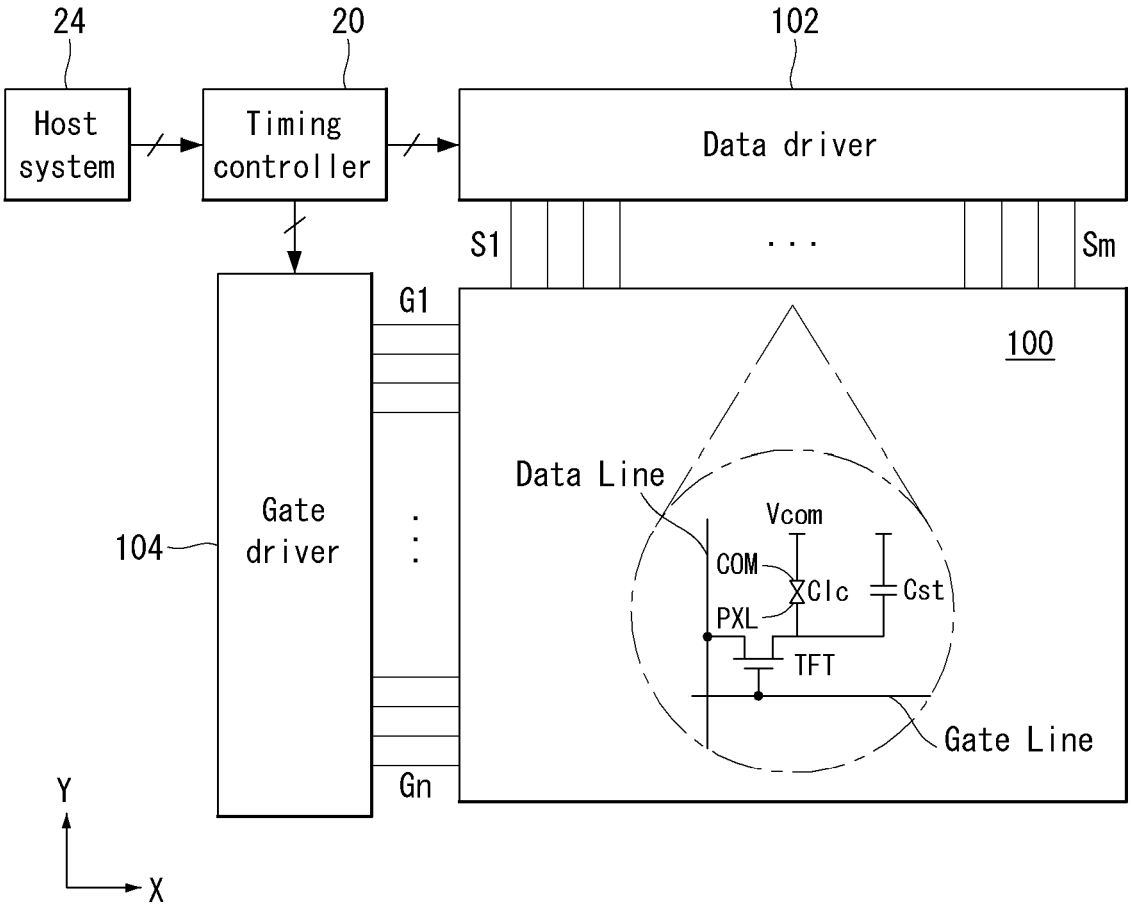

24
20
102
Host system
Timing controller
Data driver
S1
...
Sm
G1
100
Data Line
Gate driver
104
Vcom
COM
Clc
Cst
PXL
TFT
Gate Line
Gn
Y
X

FIG. 2

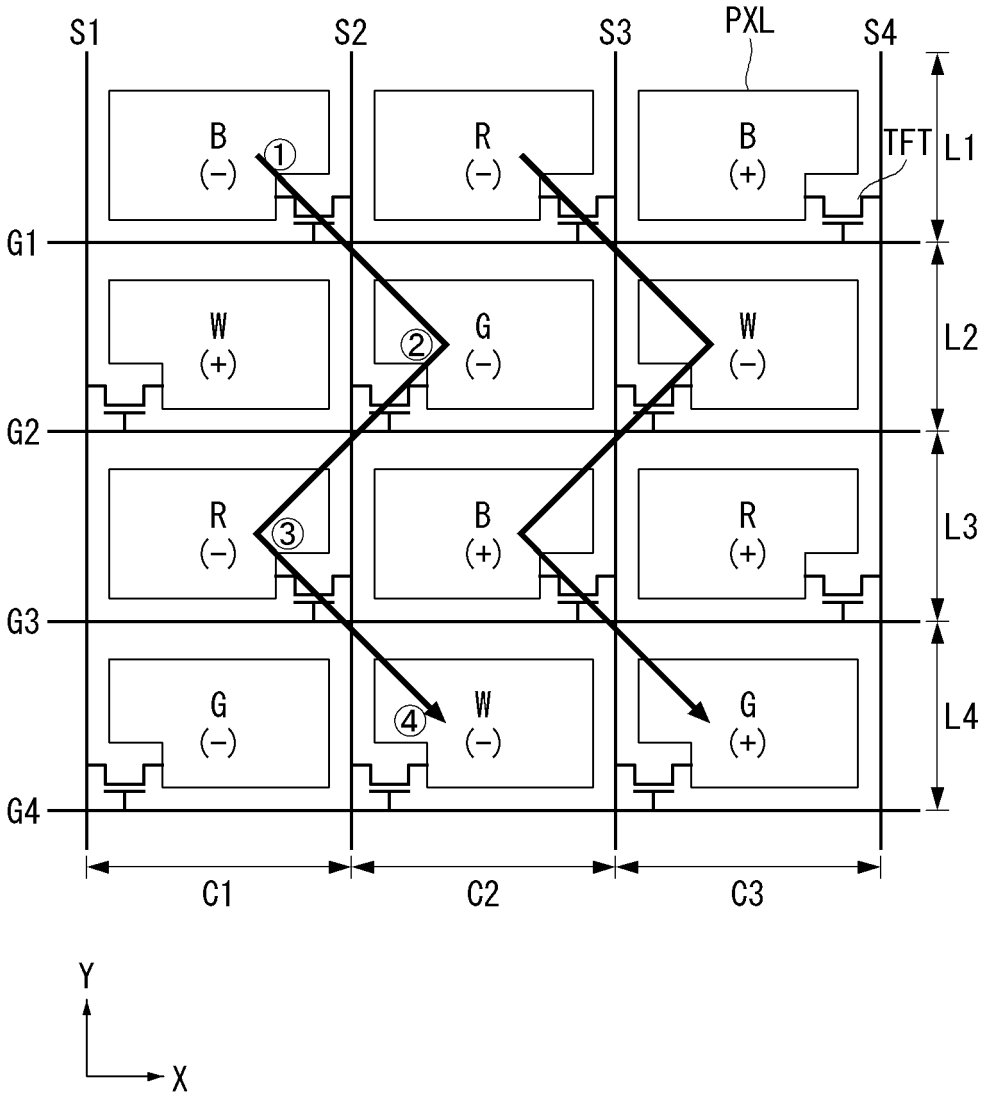

S1
S2
S3
PXL
S4
TFT
L1
L2
L3
L4
G1
G2
G3
G4
B (−)
①
R (−)
B (+)
W (+)
②
G (−)
W (−)
R (−)
③
B (+)
R (+)
G (−)
④
W (−)
G (+)
C1
C2
C3
Y
X

FIG. 3

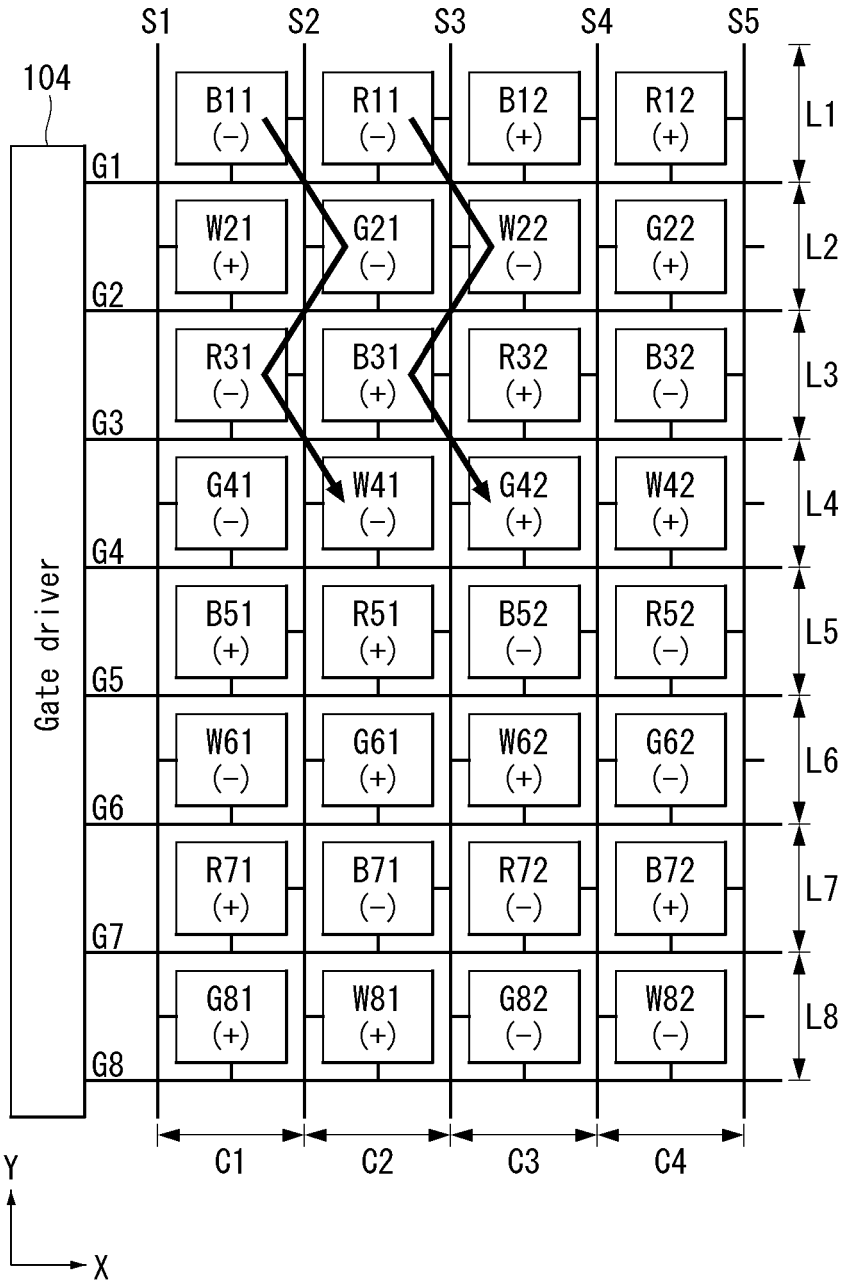

S1
S2
S3
S4
S5
104
Gate driver
G1
G2
G3
G4
G5
G6
G7
G8
B11 (−)
R11 (−)
B12 (+)
R12 (+)
W21 (+)
G21 (−)
W22 (−)
G22 (+)
R31 (−)
B31 (+)
R32 (+)
B32 (−)
G41 (−)
W41 (−)
G42 (+)
W42 (+)
B51 (+)
R51 (+)
B52 (−)
R52 (−)
W61 (−)
G61 (+)
W62 (+)
G62 (−)
R71 (+)
B71 (−)
R72 (−)
B72 (+)
G81 (+)
W81 (+)
G82 (−)
W82 (−)
L1
L2
L3
L4
L5
L6
L7
L8
C1
C2
C3
C4
Y
X

FIG. 4

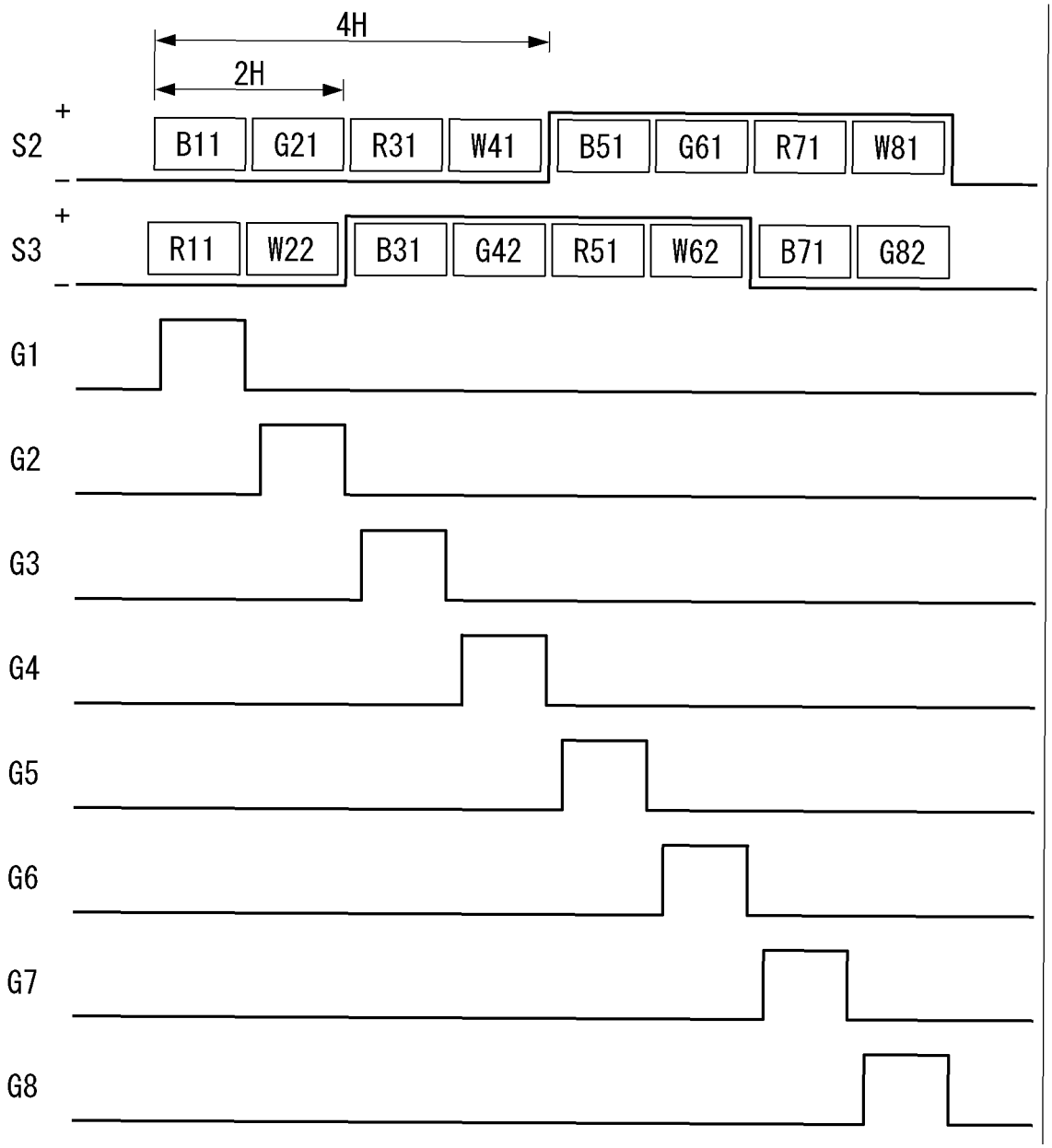
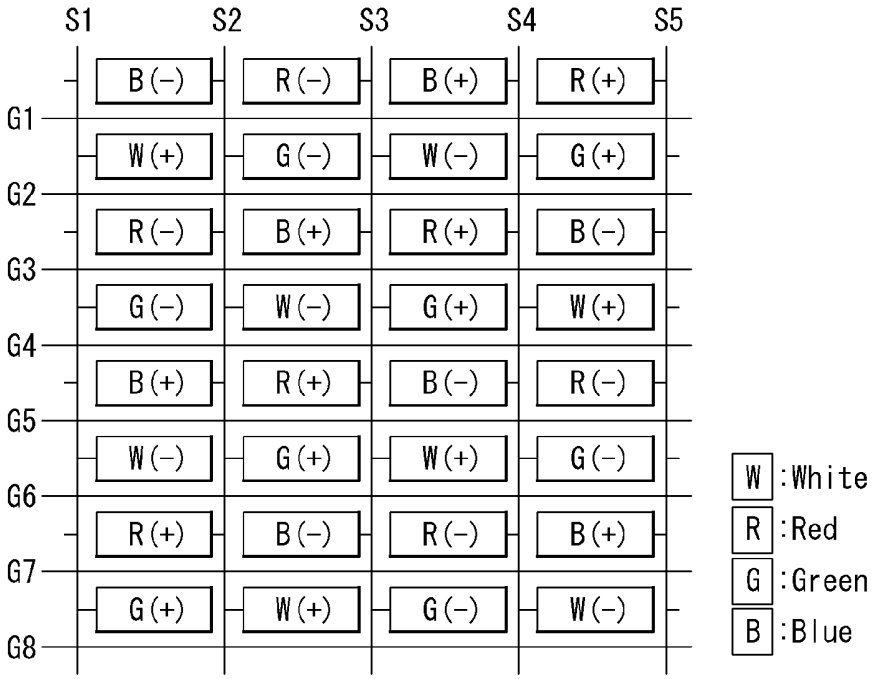
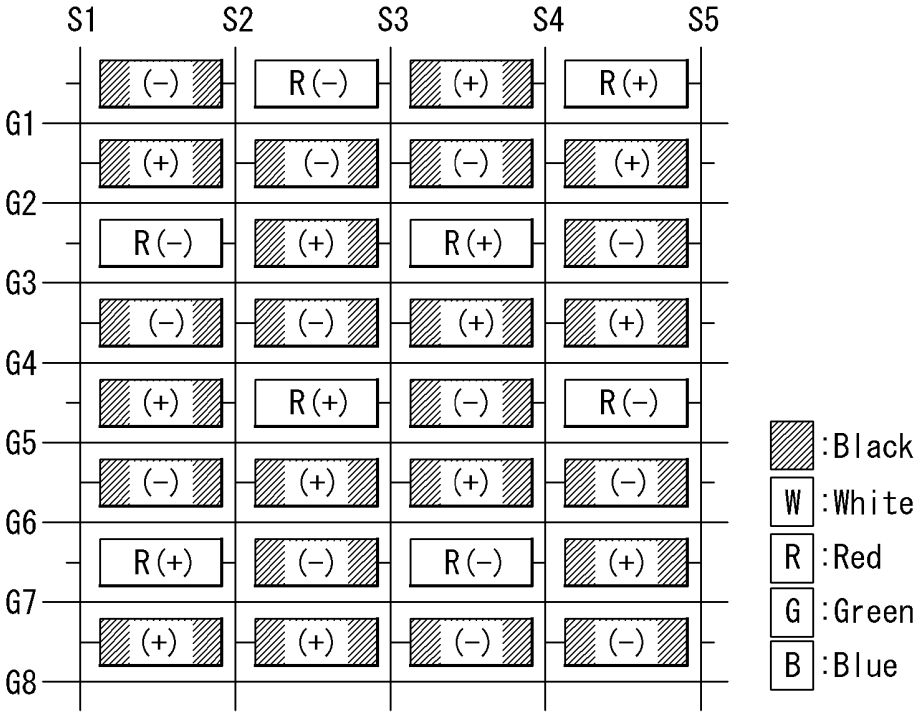

4H
2H
S2
+
−
B11
G21
R31
W41
B51
G61
R71
W81
S3
+
−
R11
W22
B31
G42
R51
W62
B71
G82
G1
G2
G3
G4
G5
G6
G7
G8

FIG. 5A



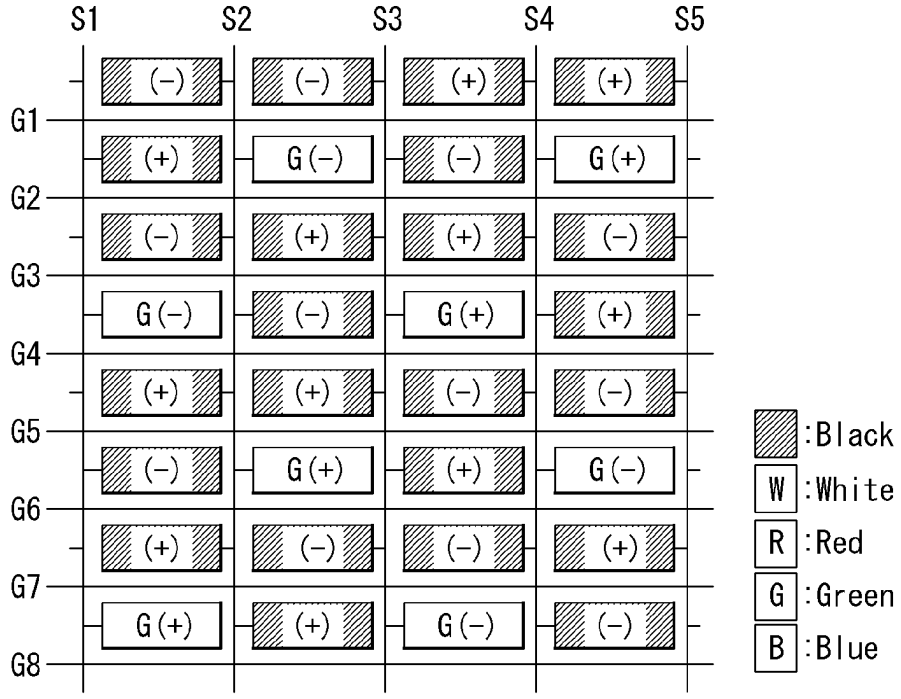
<White>

FIG. 5B



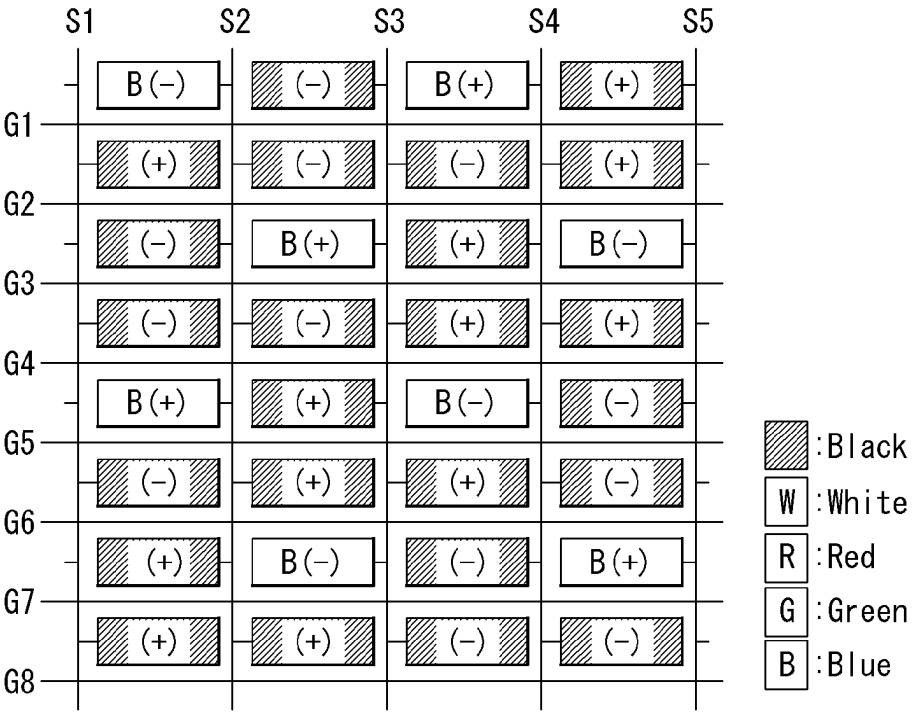
<Red>

FIG. 5C



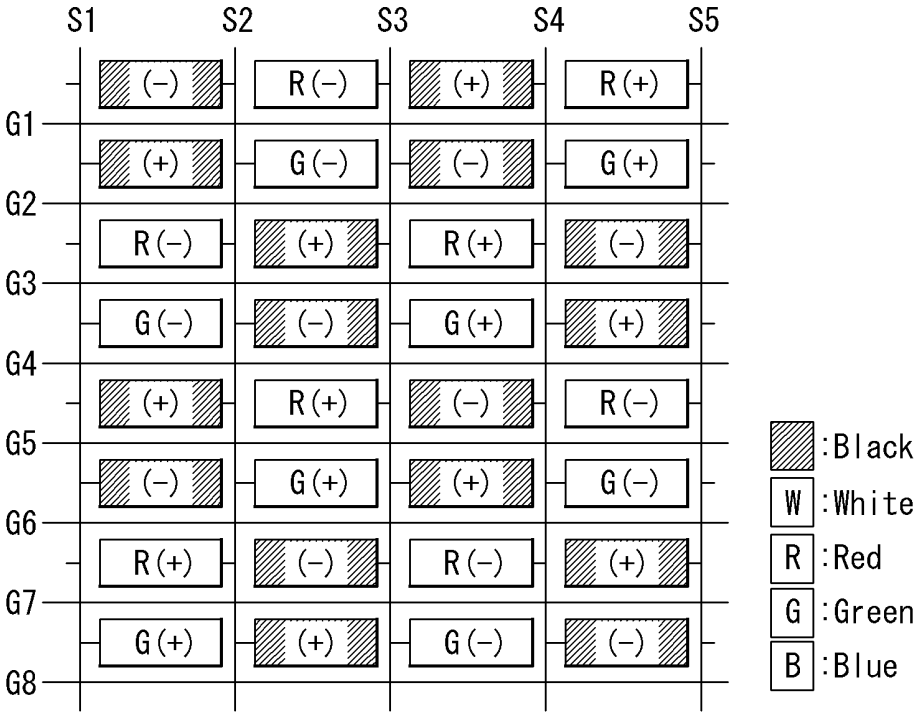
<Green>

FIG. 5D



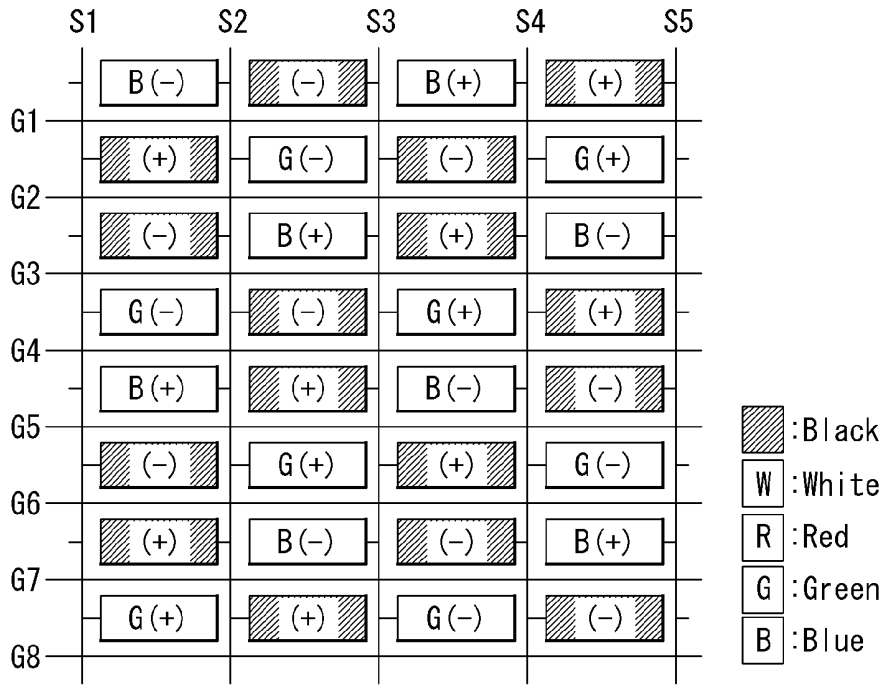
<Blue>

FIG. 5E



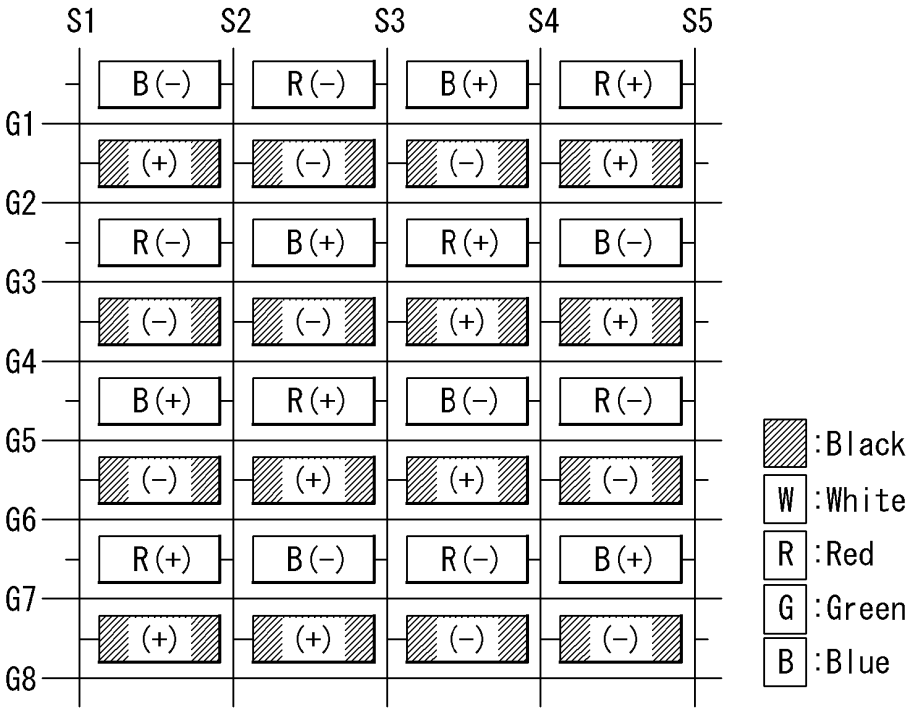
<Yellow>

FIG. 5F



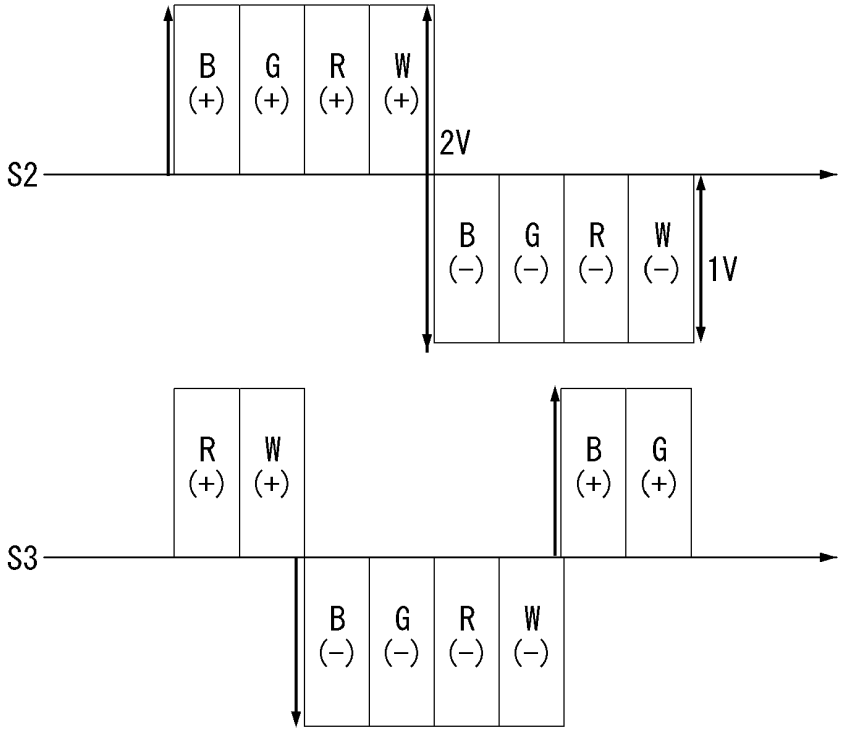
<Cyan>

FIG. 5G



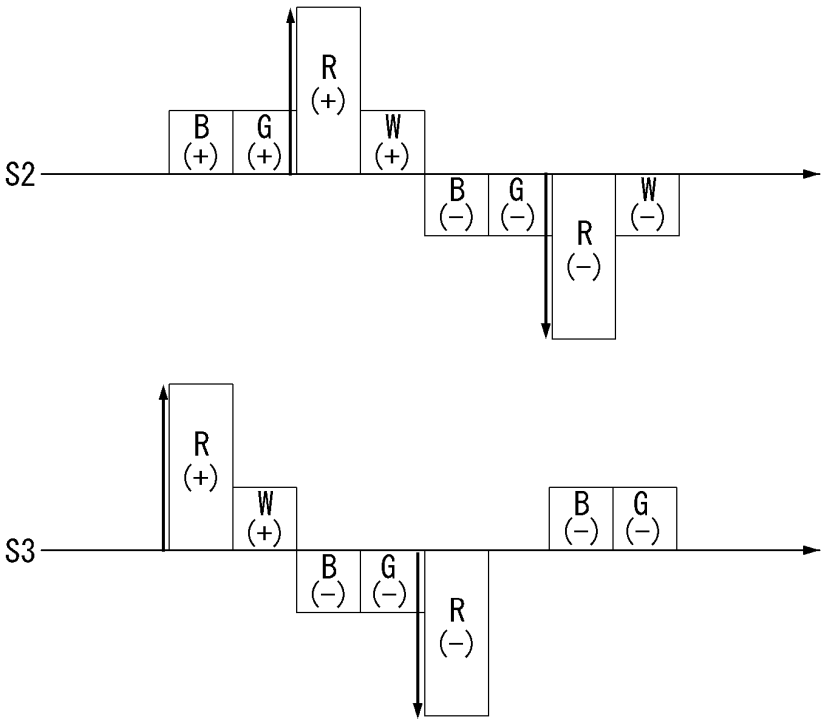
<Magenta>

FIG. 6A



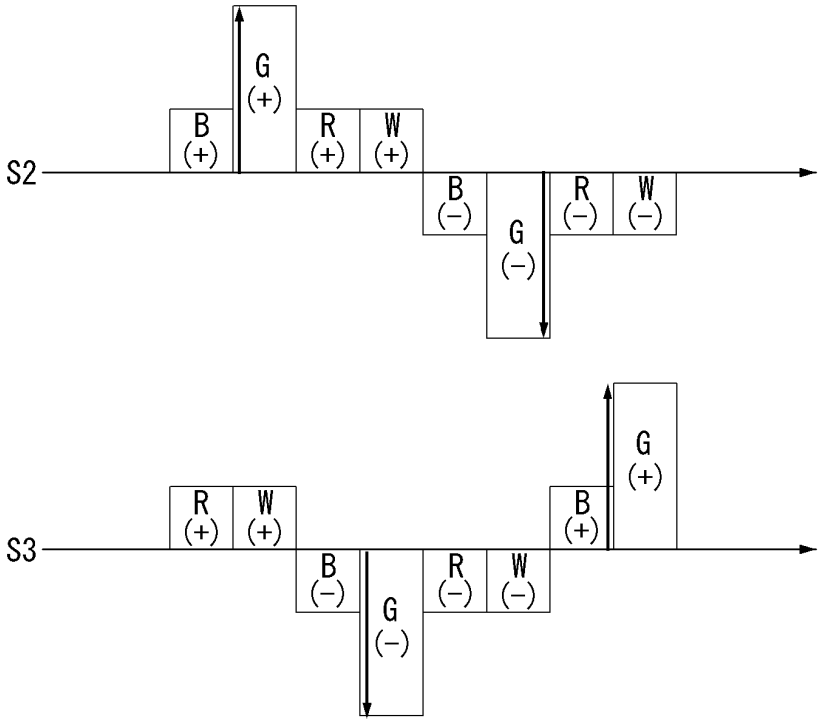
<White>

FIG. 6B



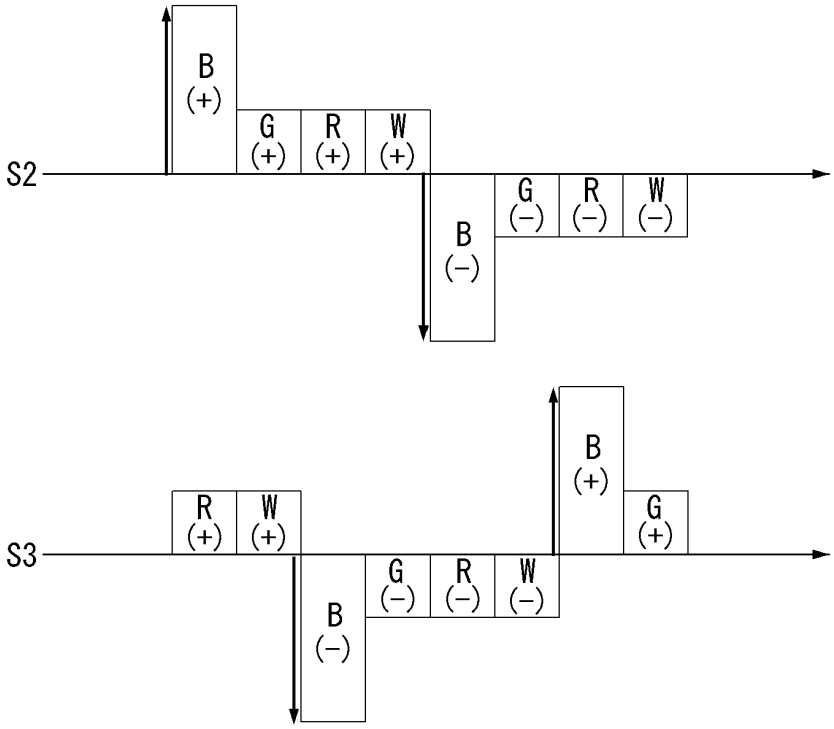
<Red>

FIG. 6C



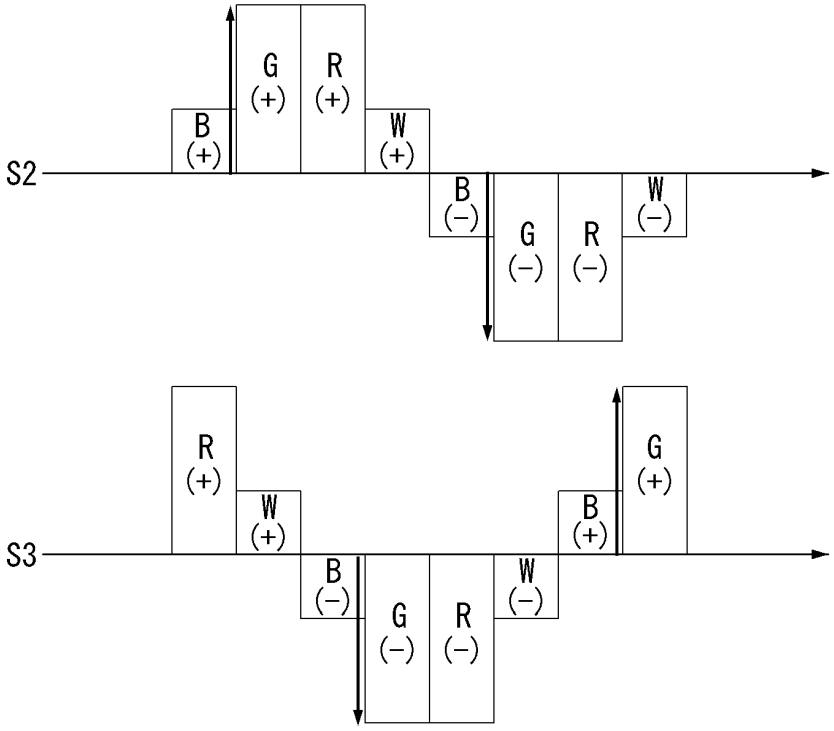
<Green>

FIG. 6D



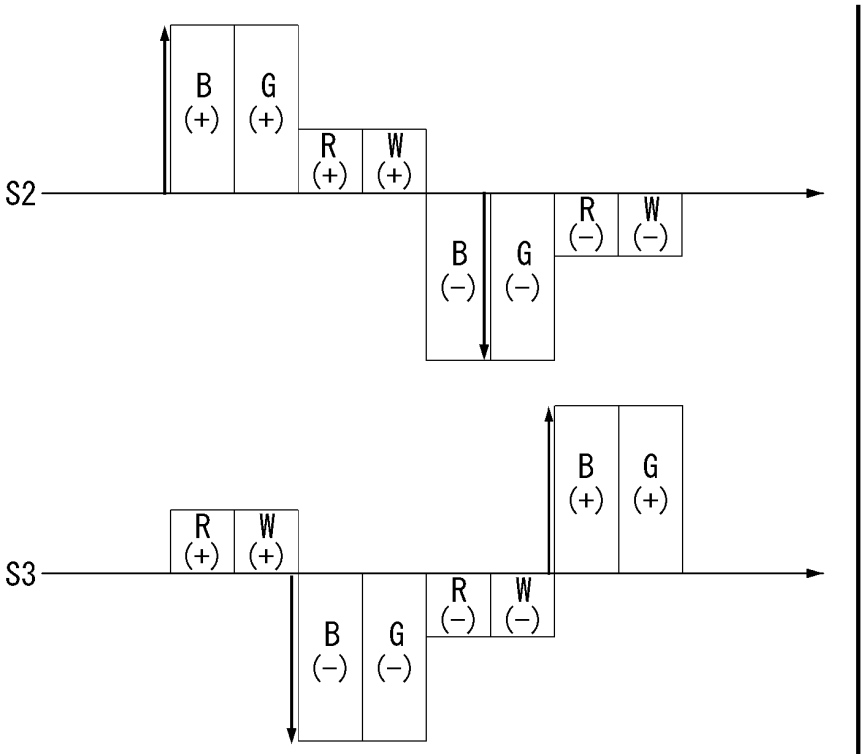
<Blue>

FIG. 6E



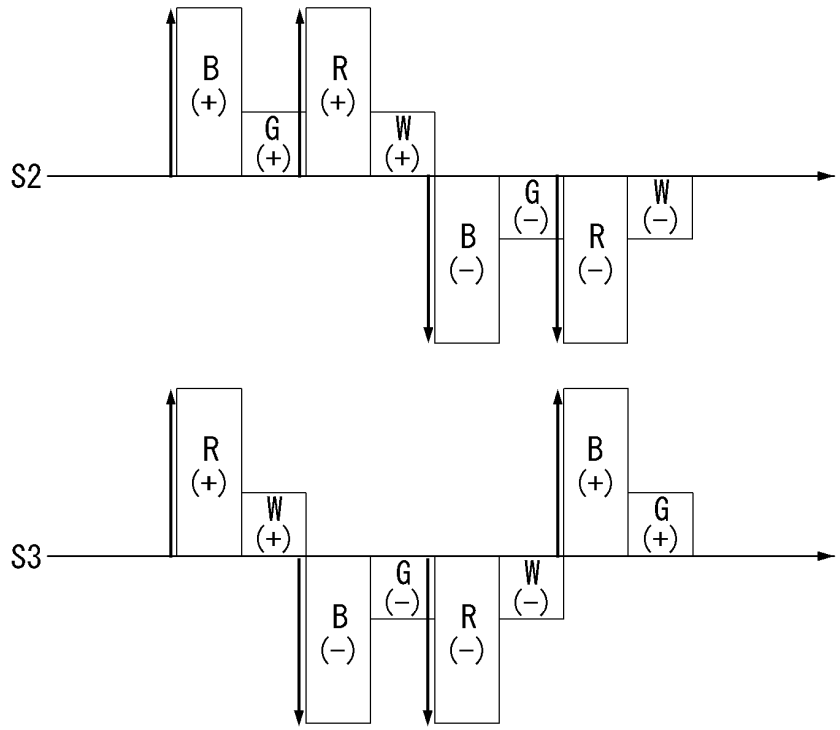
<Yellow>

FIG. 6F



<Cyan>

FIG. 6G



<Magenta>

FIG. 7

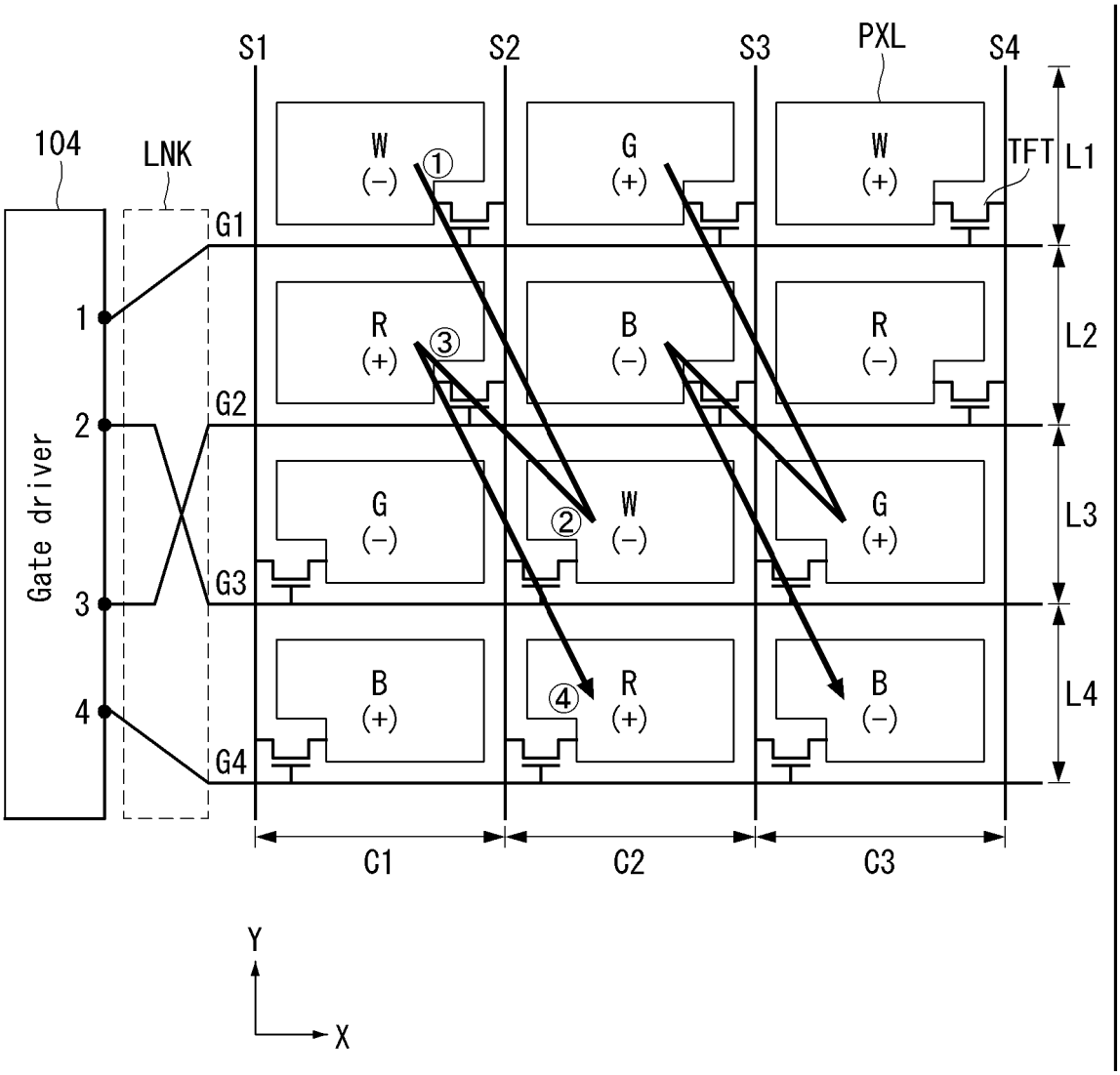

S1
S2
S3
PXL
S4
104
LNK
TFT
L1
L2
L3
L4
G1
G2
G3
G4
Gate driver
1
2
3
4
W (−)
G (+)
W (+)
R (+)
B (−)
R (−)
G (−)
W (−)
G (+)
B (+)
R (+)
B (−)
①
②
③
④
C1
C2
C3
Y
X

FIG. 8

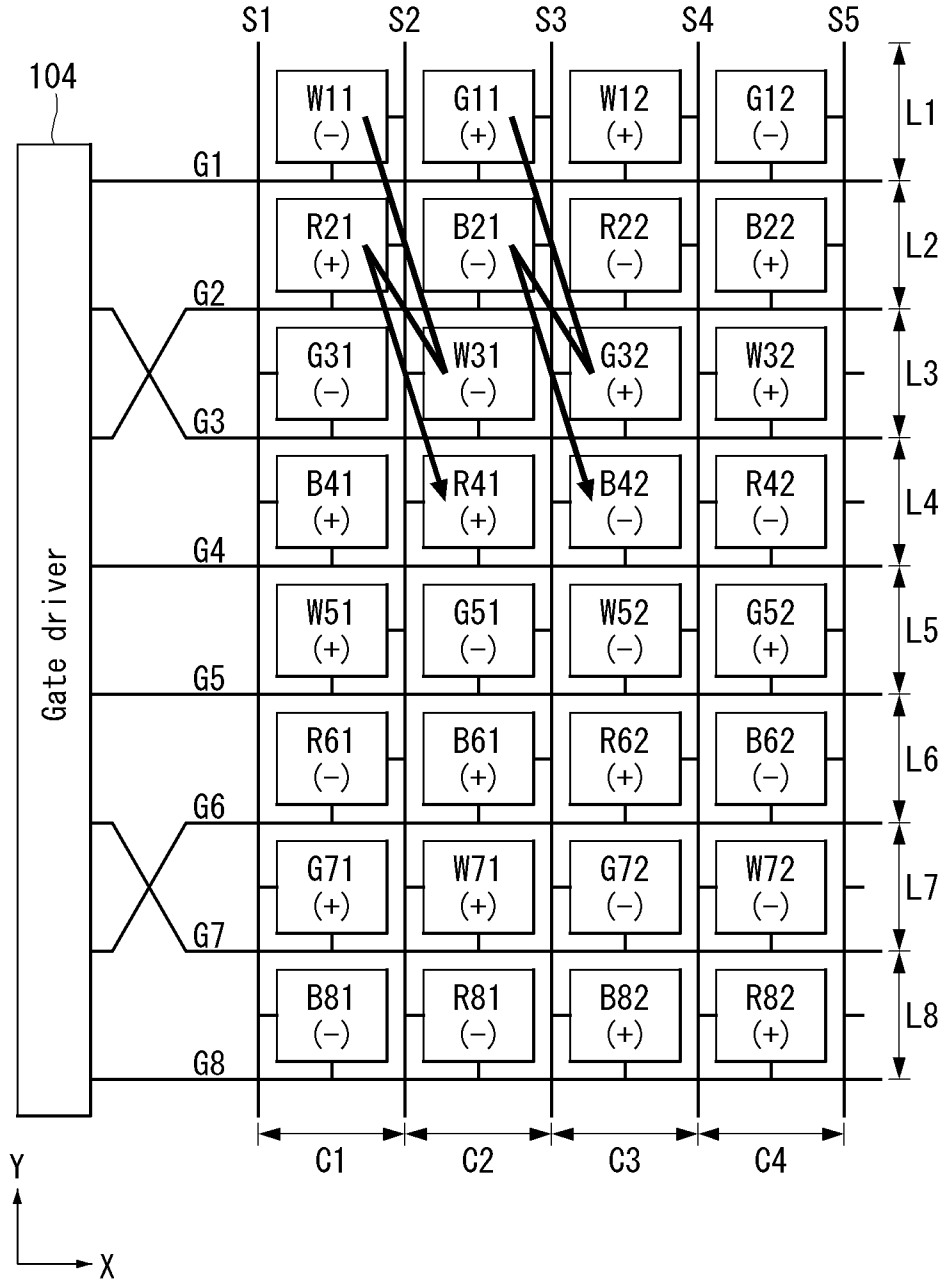

S1
S2
S3
S4
S5
104
Gate driver
G1
G2
G3
G4
G5
G6
G7
G8
W11 (−)
G11 (+)
W12 (+)
G12 (−)
R21 (+)
B21 (−)
R22 (−)
B22 (+)
G31 (−)
W31 (−)
G32 (+)
W32 (+)
B41 (+)
R41 (+)
B42 (−)
R42 (−)
W51 (+)
G51 (−)
W52 (−)
G52 (+)
R61 (−)
B61 (+)
R62 (+)
B62 (−)
G71 (+)
W71 (+)
G72 (−)
W72 (−)
B81 (−)
R81 (−)
B82 (+)
R82 (+)
L1
L2
L3
L4
L5
L6
L7
L8
C1
C2
C3
C4
Y
X

FIG. 9

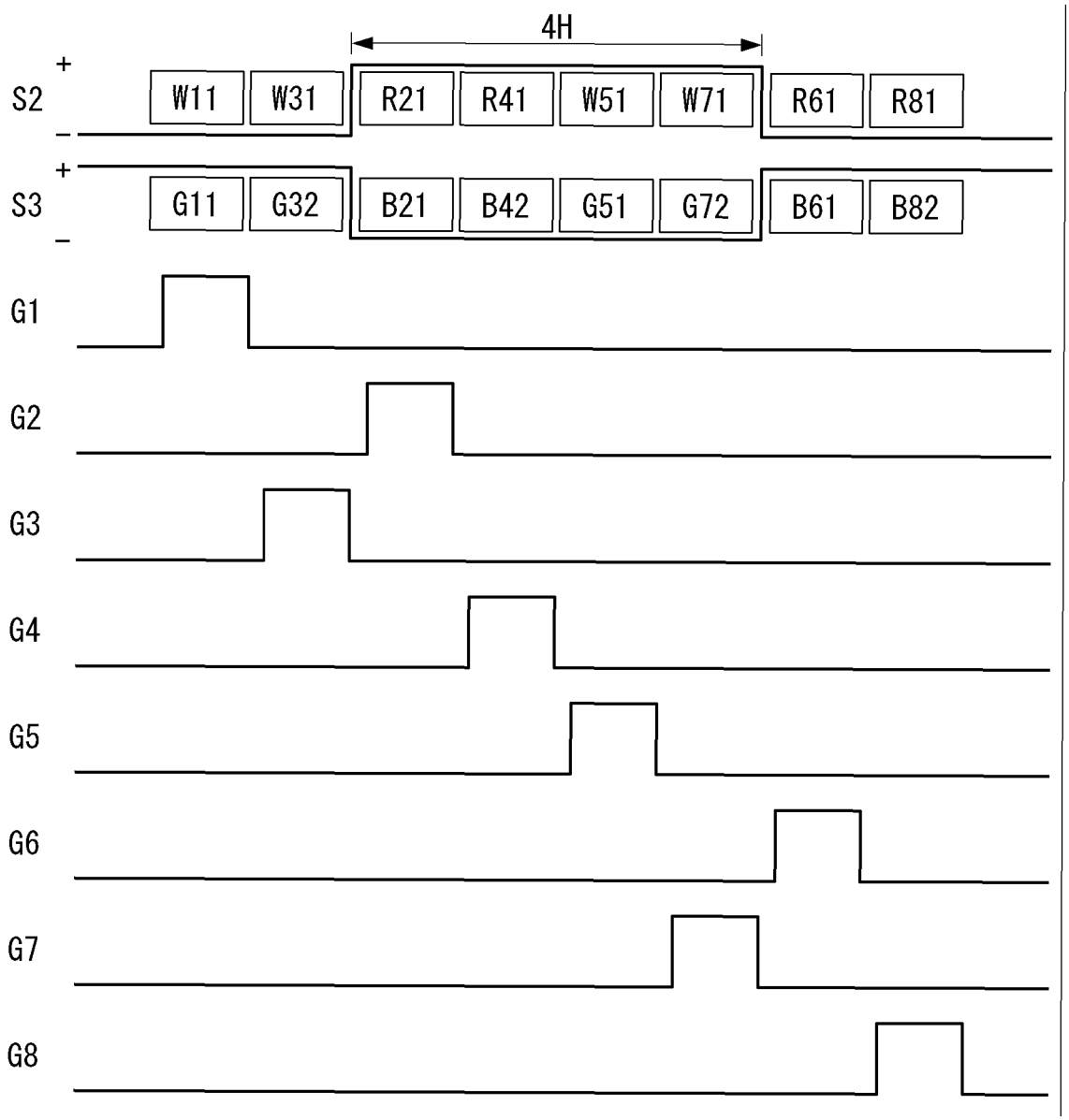
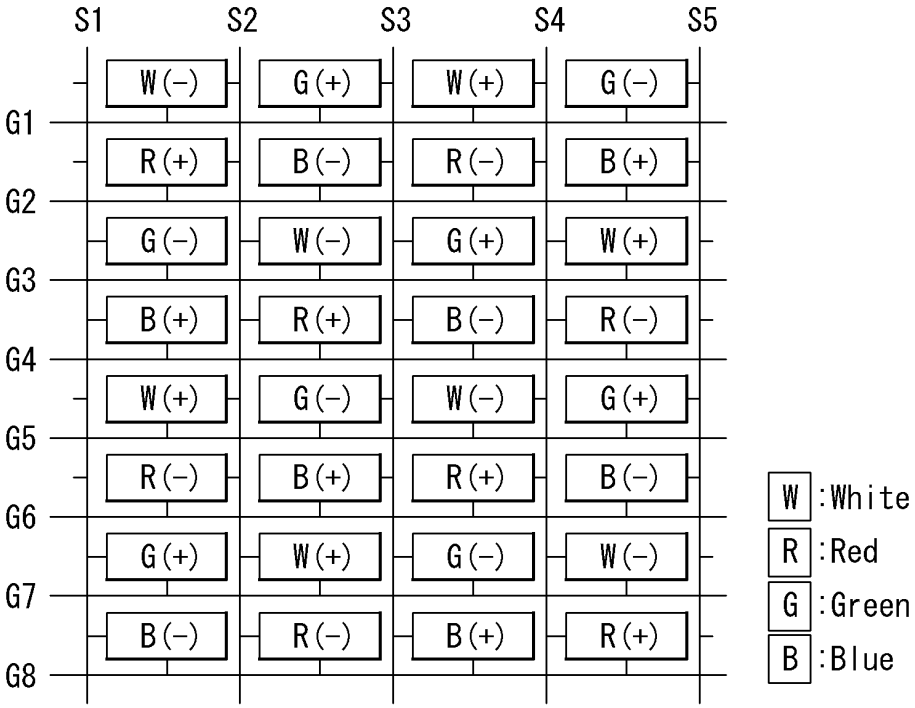
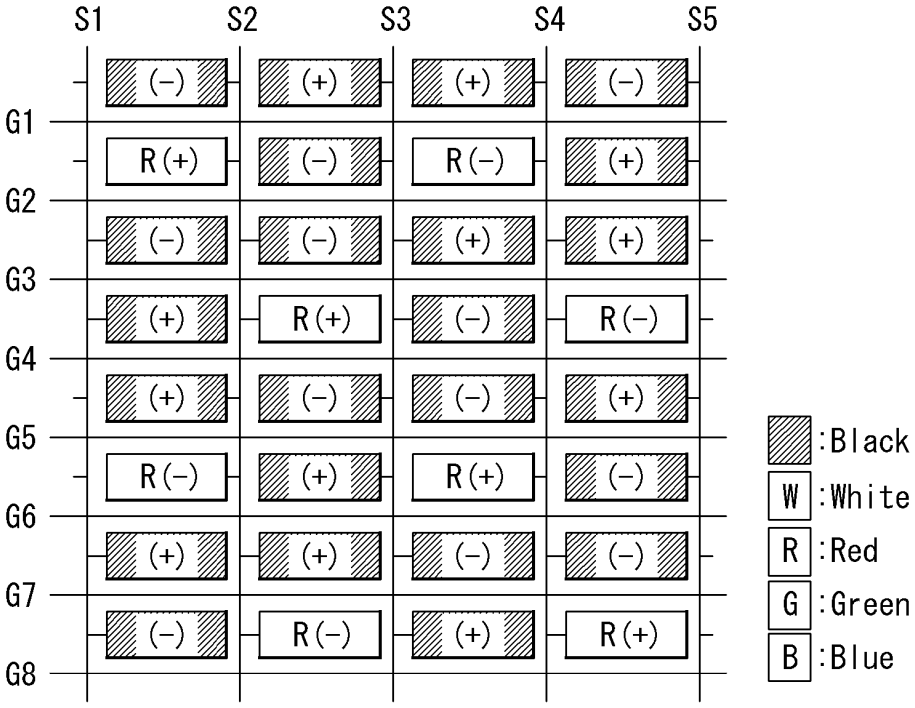

4H
S2
+
−
W11
W31
R21
R41
W51
W71
R61
R81
S3
+
−
G11
G32
B21
B42
G51
G72
B61
B82
G1
G2
G3
G4
G5
G6
G7
G8

FIG. 10A



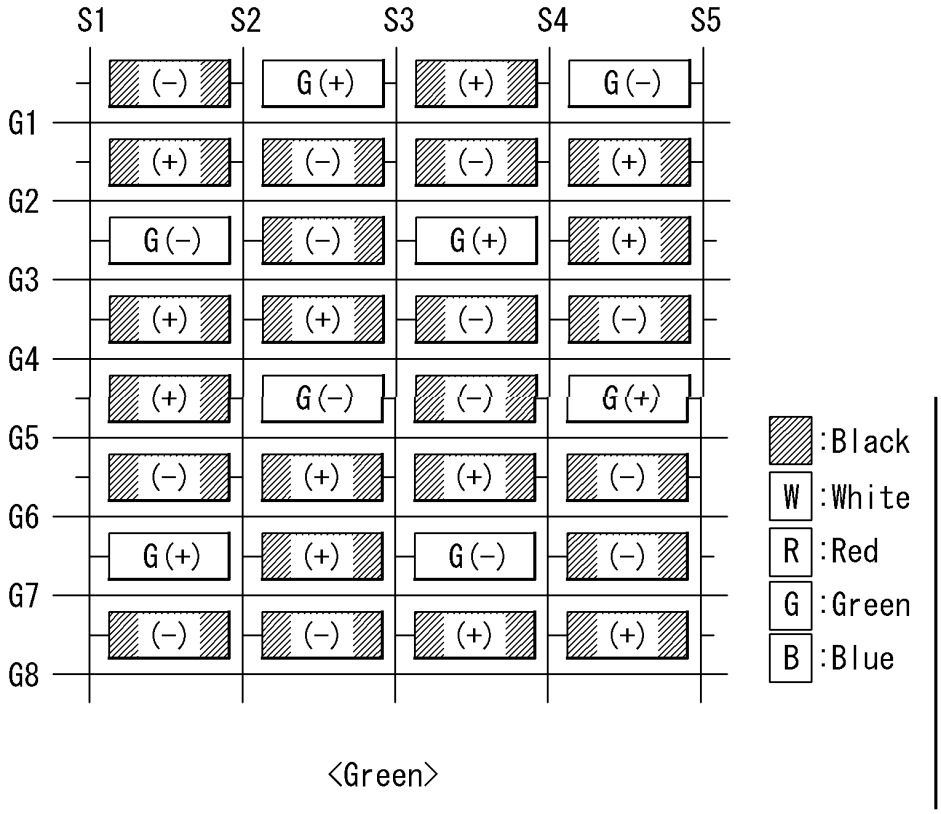
<White>

FIG. 10B



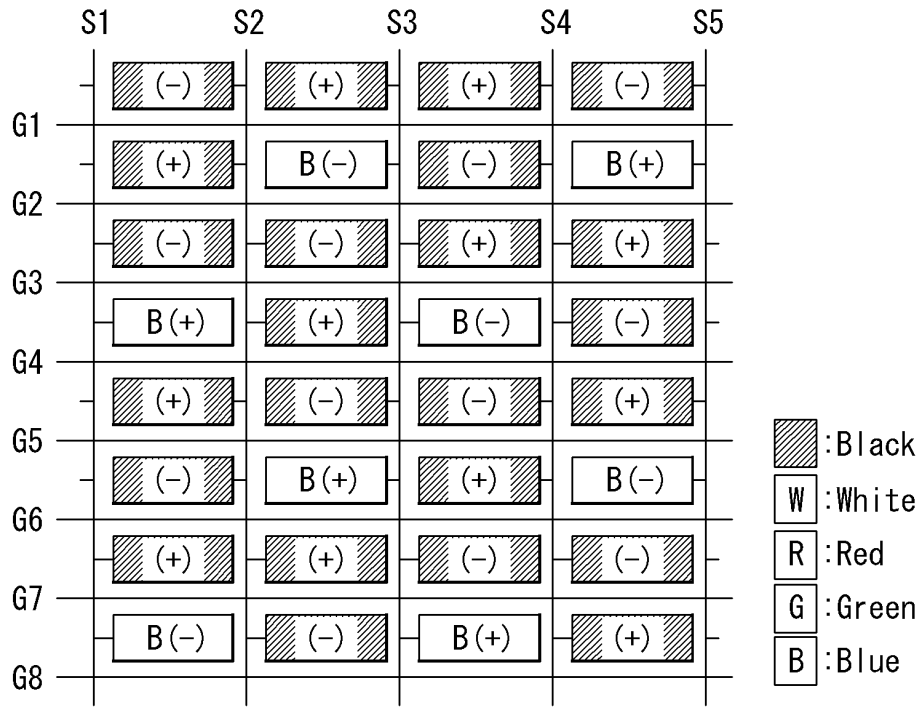
<Red>

FIG. 10C



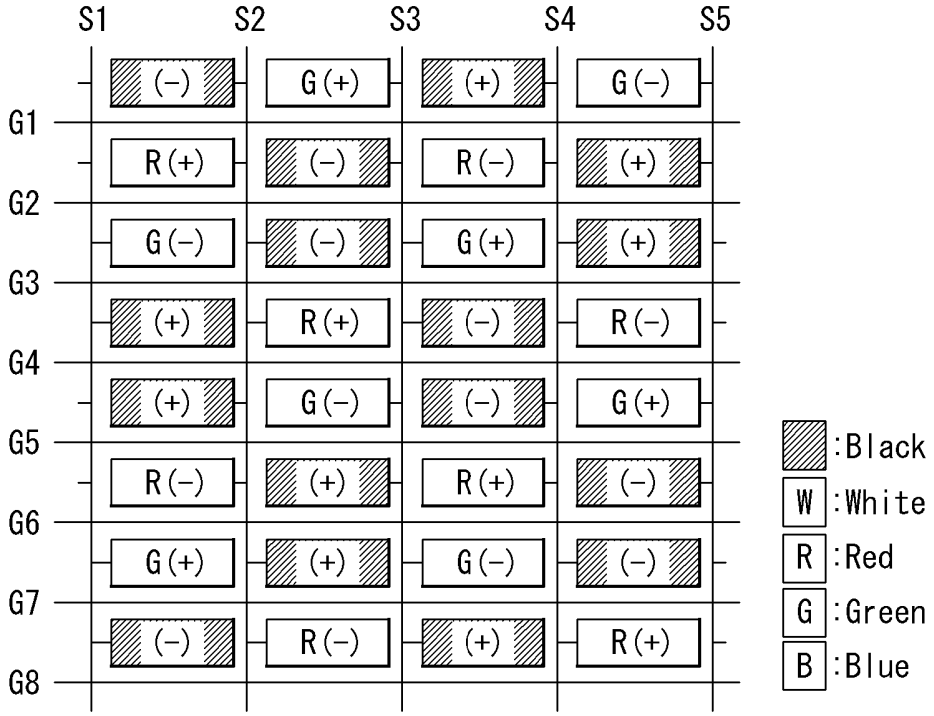
<Green>

FIG. 10D



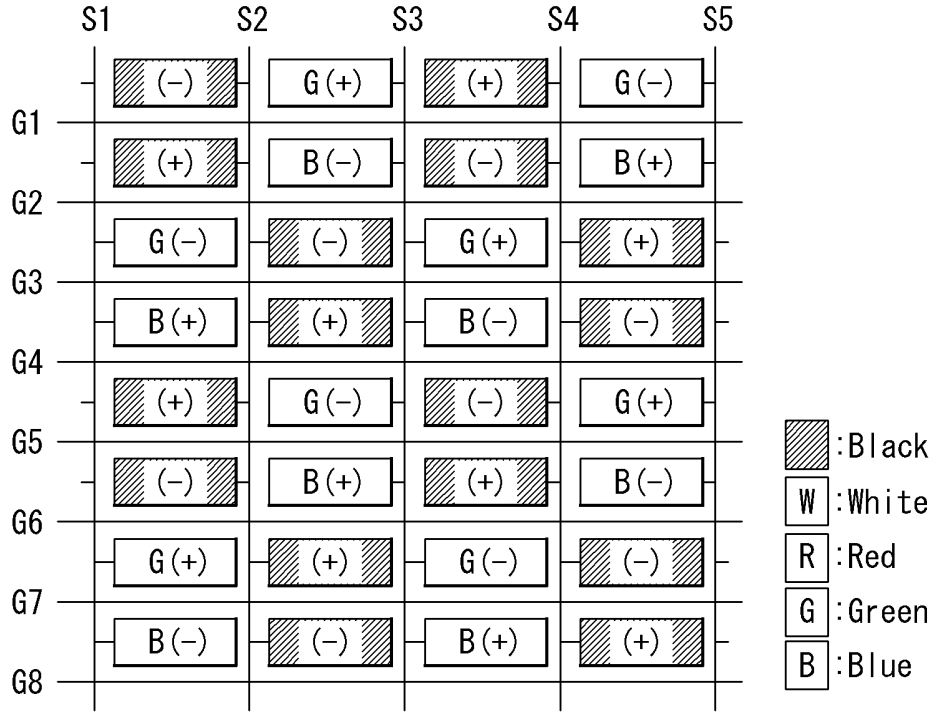
<Blue>

FIG. 10E



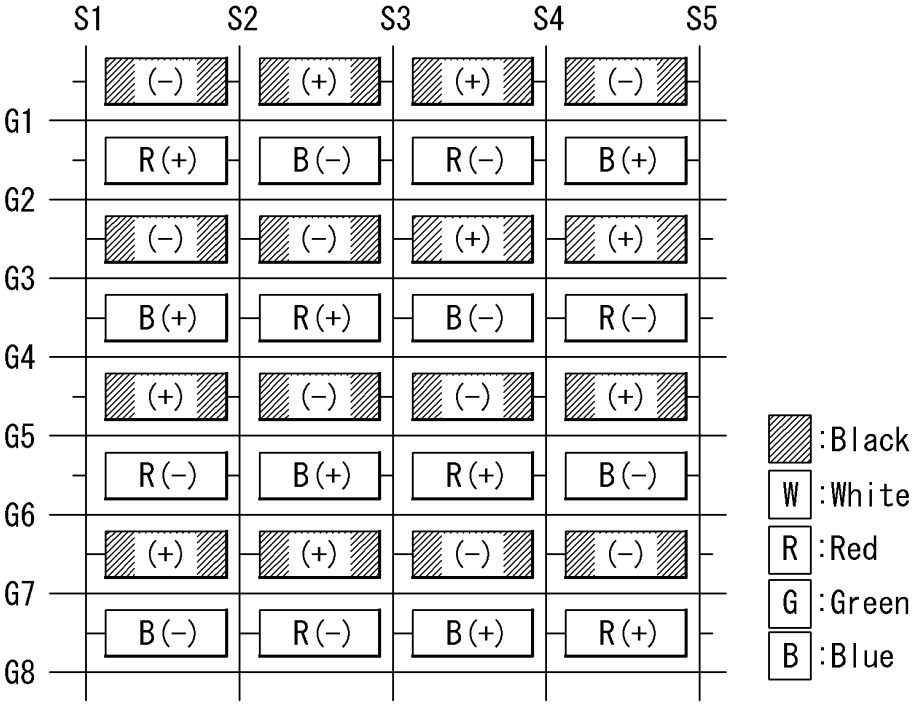
<Yellow>

FIG. 10F



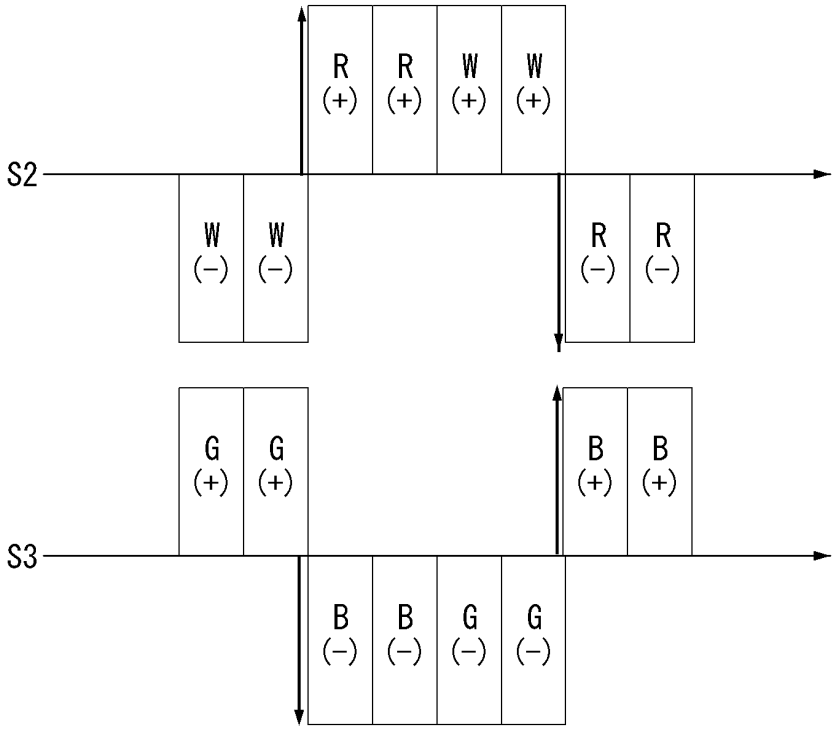
<Cyan>

FIG. 10G



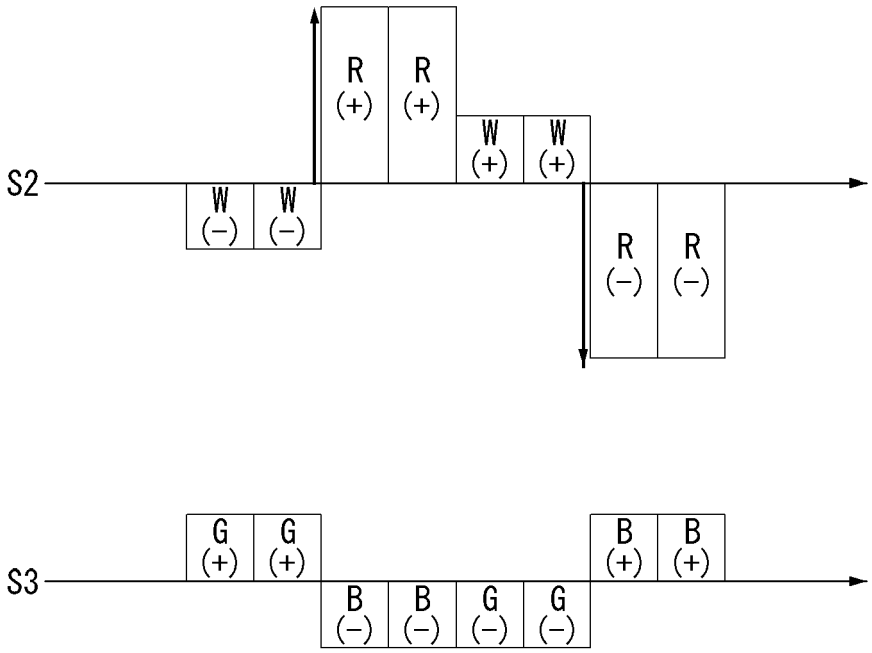
<Magenta>

FIG. 11A



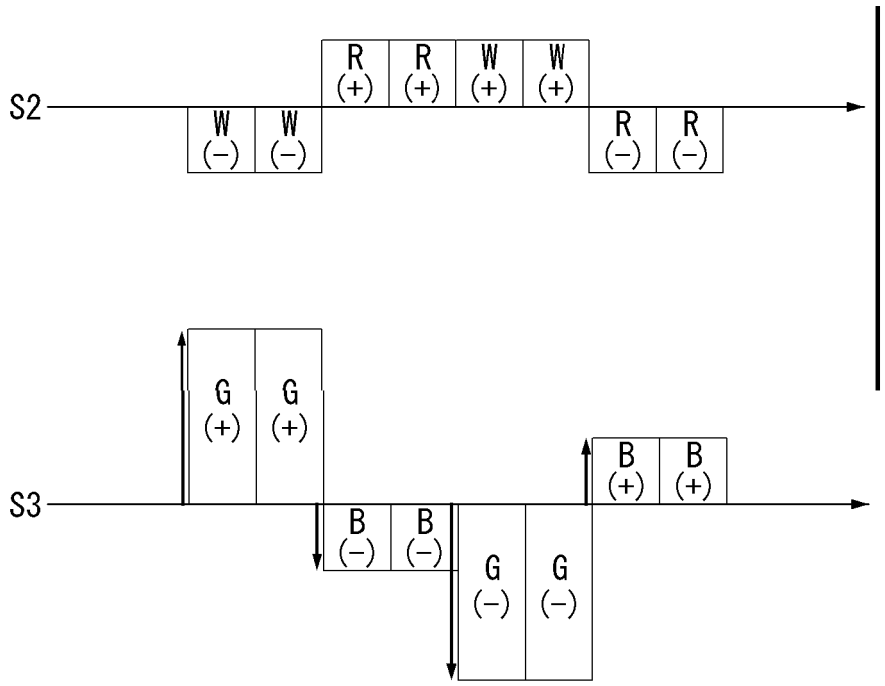
<White>

FIG. 11B



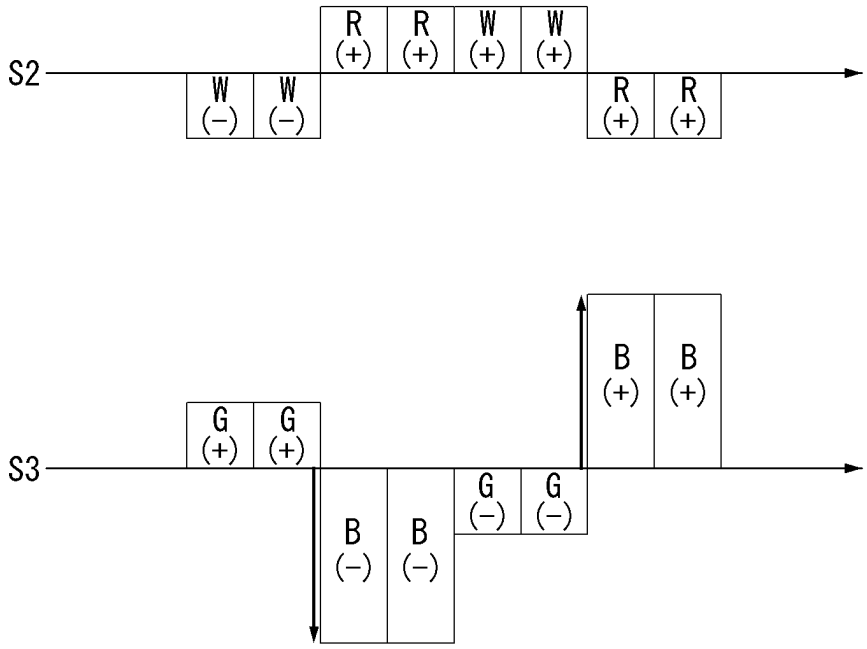
<Red>

FIG. 11C



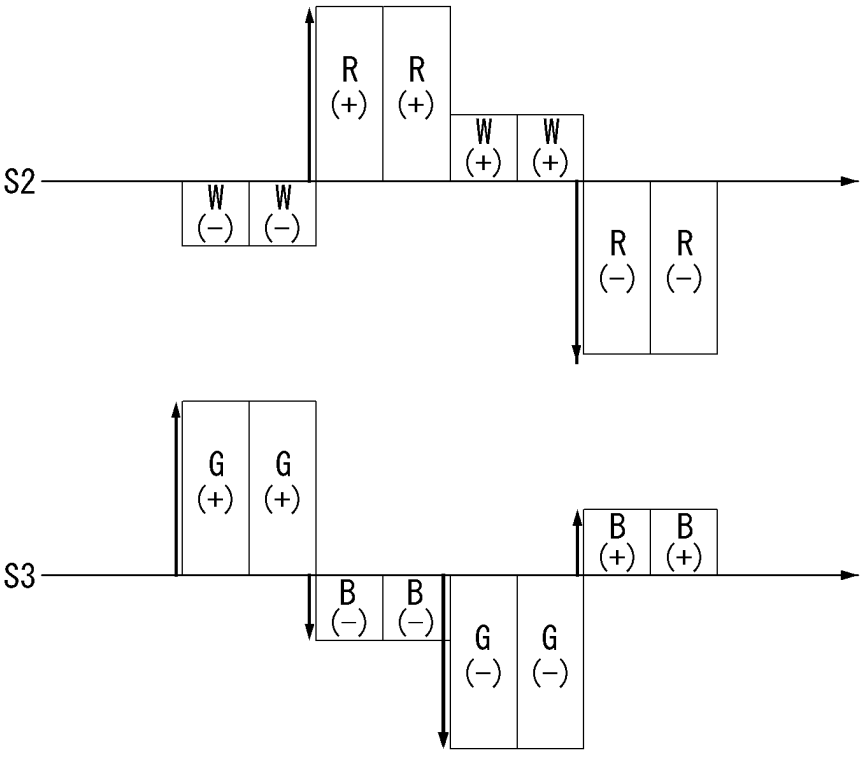
<Green>

FIG. 11D



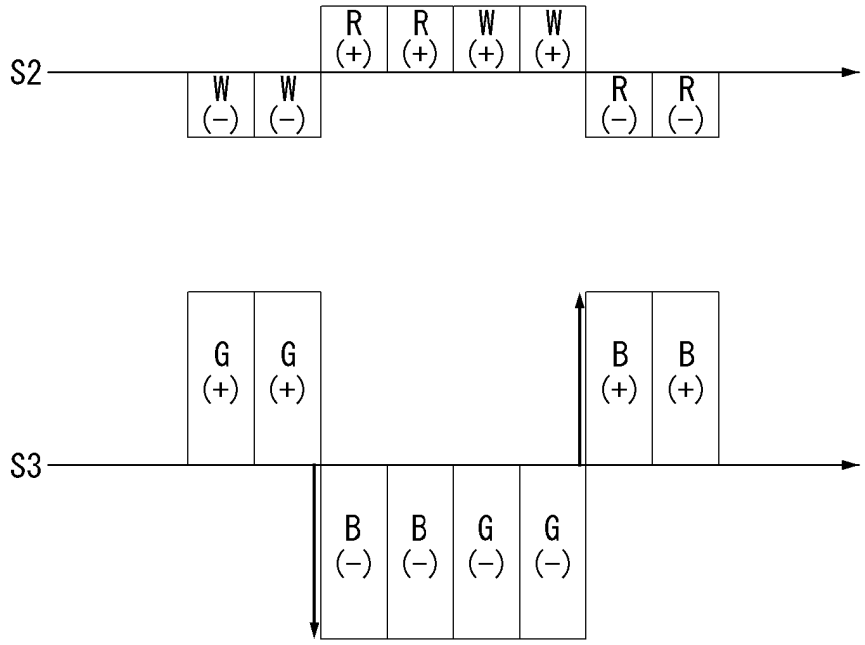
<Blue>

FIG. 11E



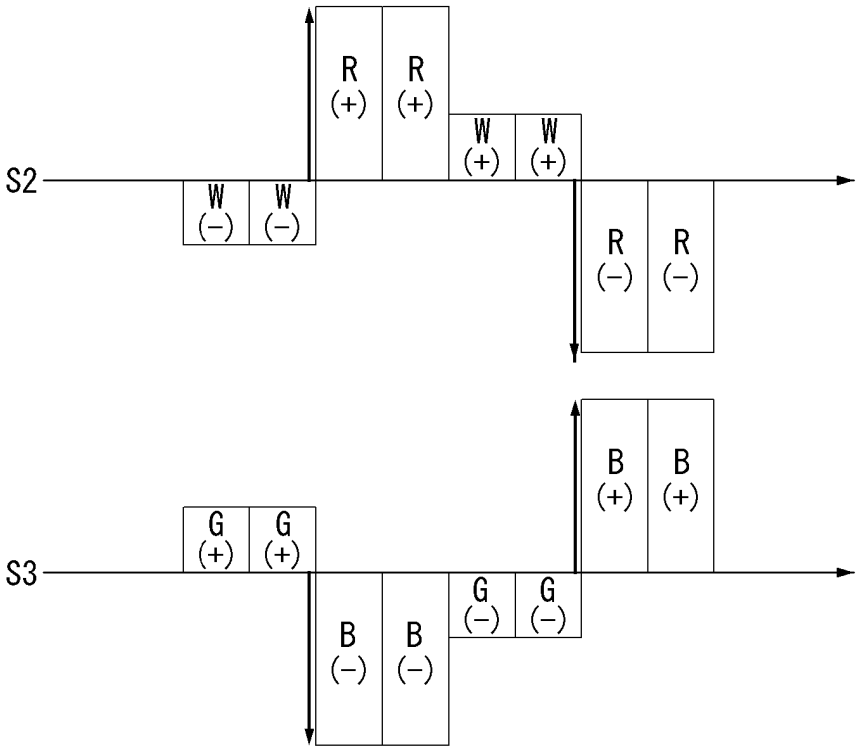
<Yellow>

FIG. 11F



<Cyan>

FIG. 11G



<Magenta>

FIG. 12

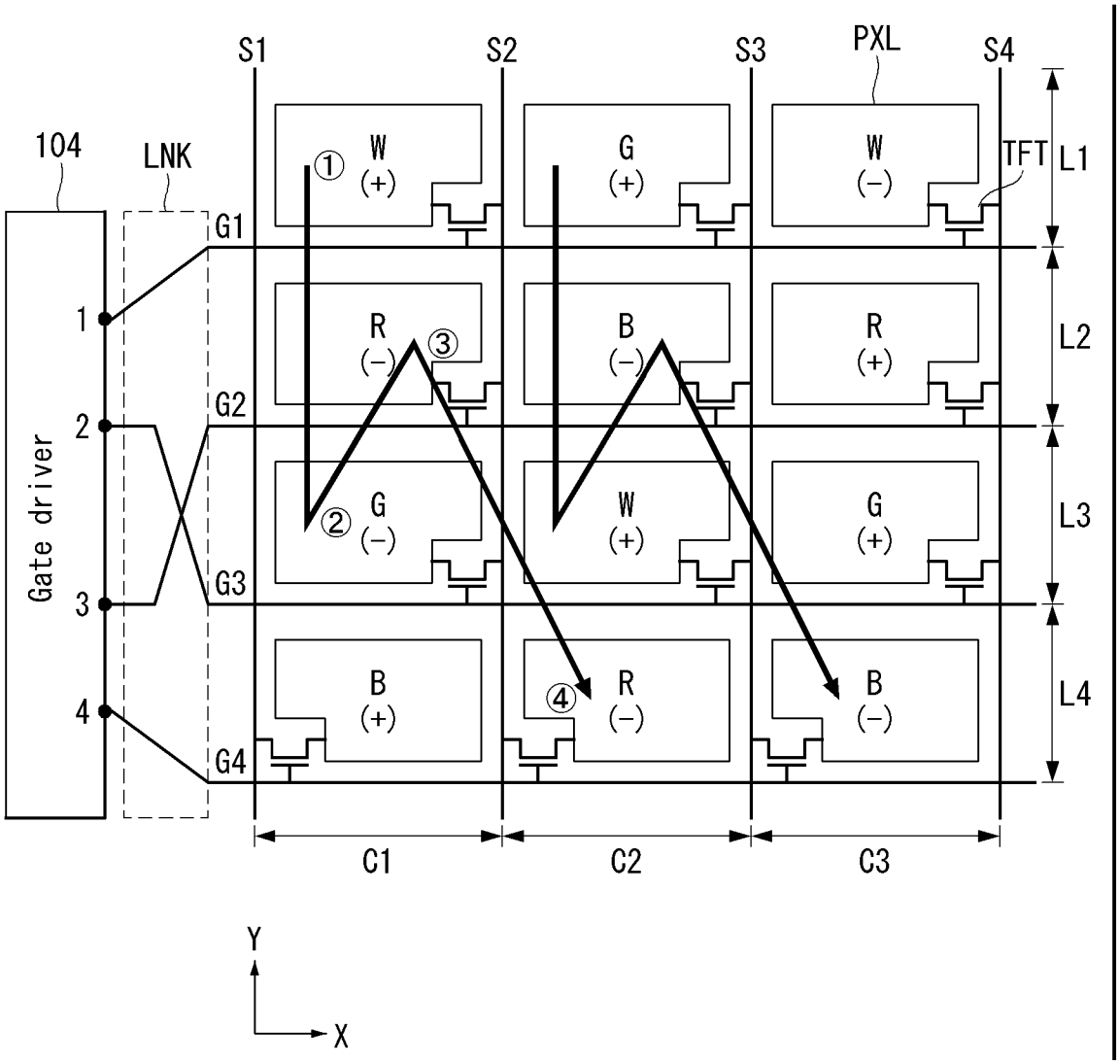

S1
S2
S3
PXL
S4
104
LNK
TFT
L1
L2
L3
L4
G1
G2
G3
G4
Gate driver
1
2
3
4
W (+)
G (+)
W (−)
R (−)
B (−)
R (+)
G (−)
W (+)
G (+)
B (+)
R (−)
B (−)
①
②
③
④
C1
C2
C3
Y
X

FIG. 13

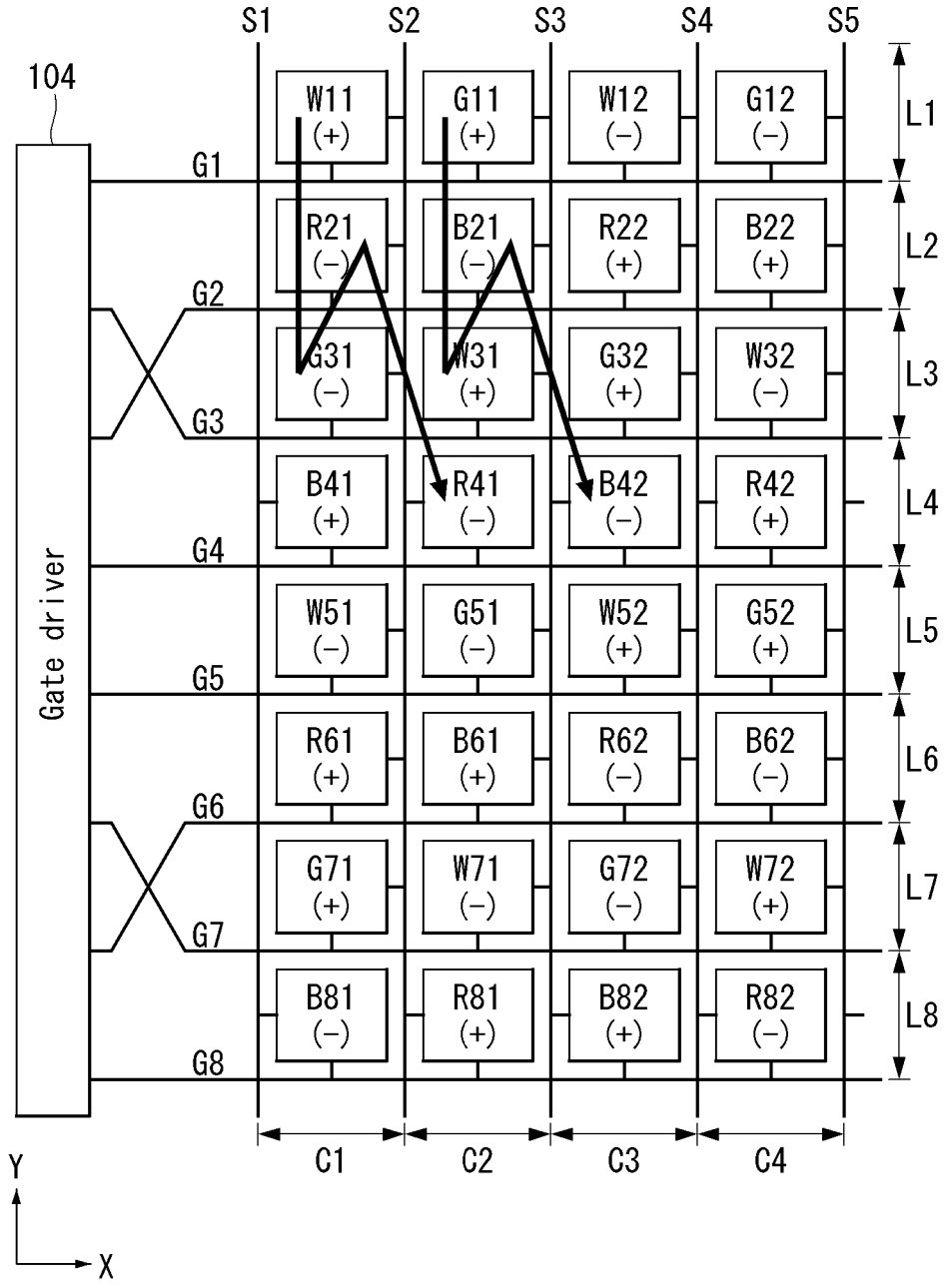

S1
S2
S3
S4
S5
104
Gate driver
G1
G2
G3
G4
G5
G6
G7
G8
W11 (+)
G11 (+)
W12 (−)
G12 (−)
R21 (−)
B21 (−)
R22 (+)
B22 (+)
G31 (−)
W31 (+)
G32 (+)
W32 (−)
B41 (+)
R41 (−)
B42 (−)
R42 (+)
W51 (−)
G51 (−)
W52 (+)
G52 (+)
R61 (+)
B61 (+)
R62 (−)
B62 (−)
G71 (+)
W71 (−)
G72 (−)
W72 (+)
B81 (−)
R81 (+)
B82 (+)
R82 (−)
L1
L2
L3
L4
L5
L6
L7
L8
C1
C2
C3
C4
Y
X

FIG. 14

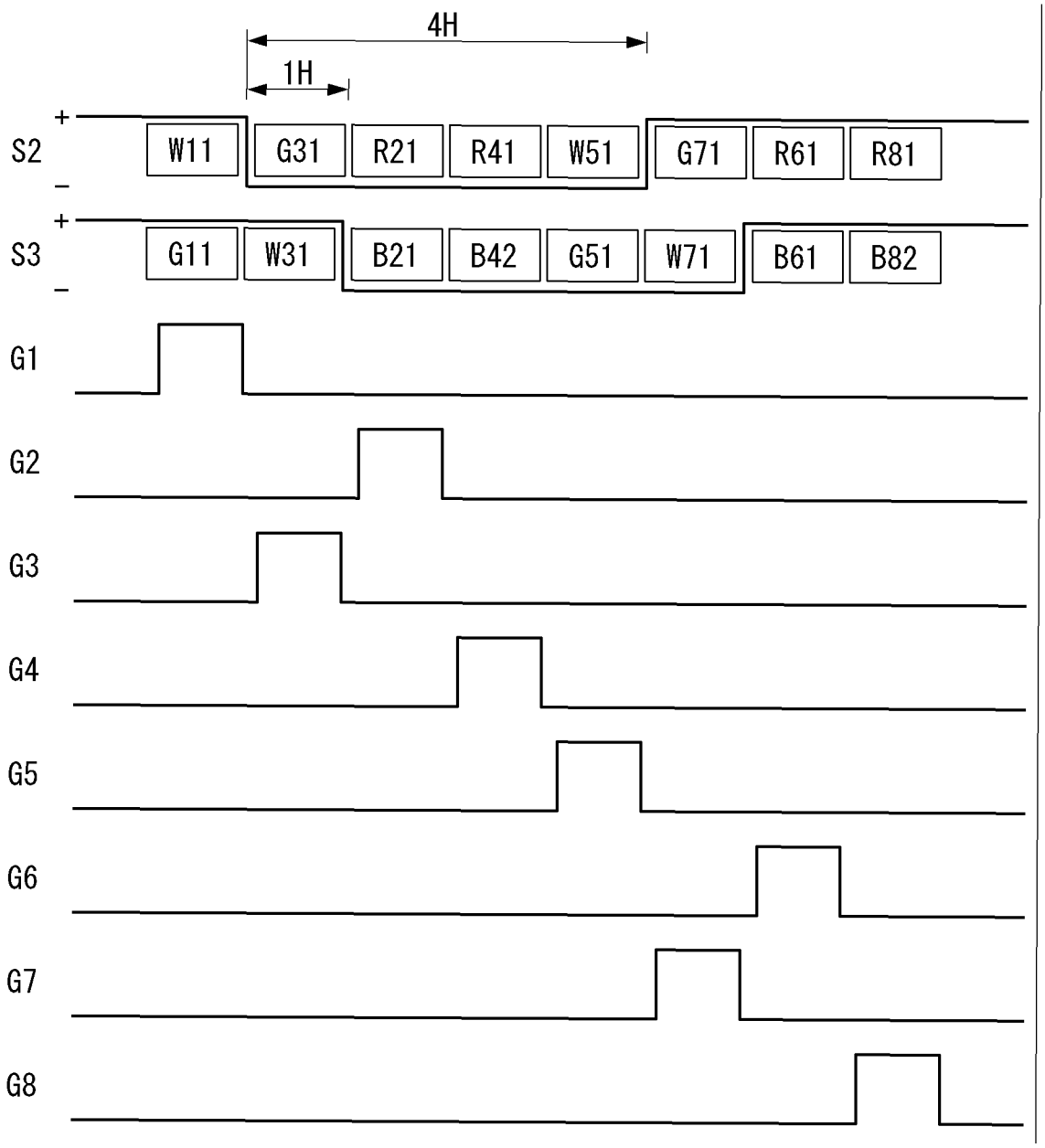
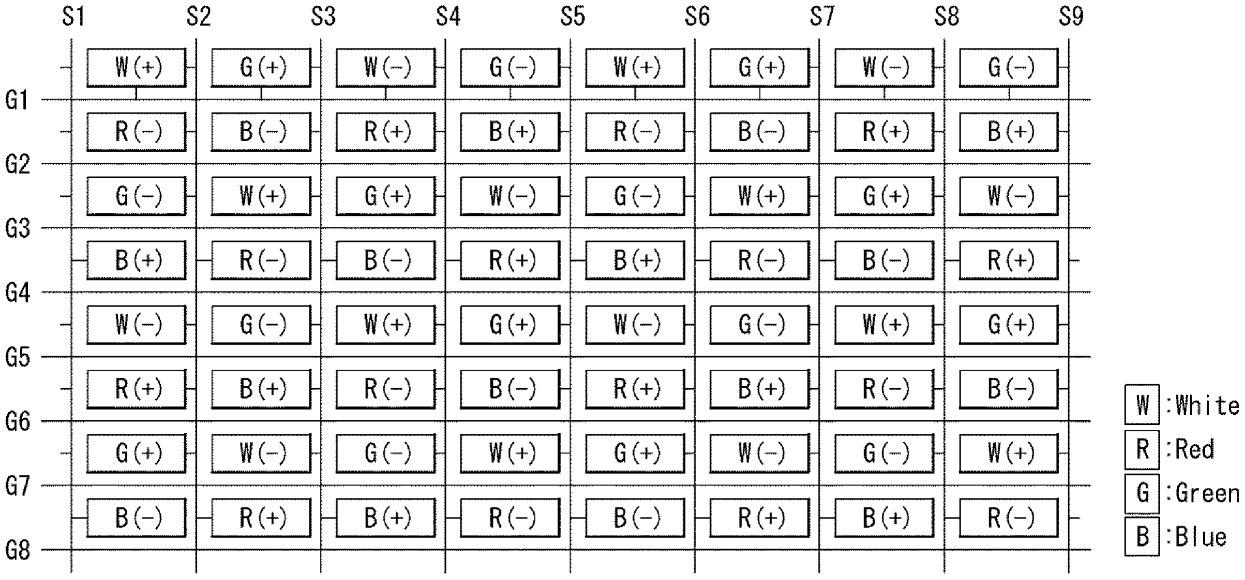
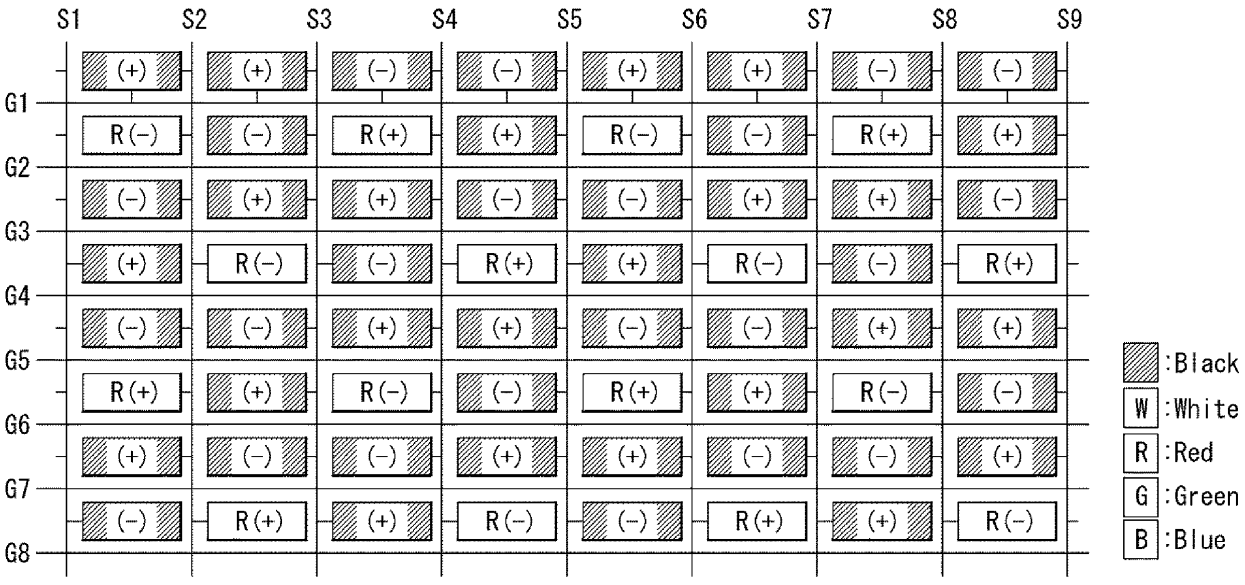

4H
1H
S2
+
−
W11
G31
R21
R41
W51
G71
R61
R81
S3
+
−
G11
W31
B21
B42
G51
W71
B61
B82
G1
G2
G3
G4
G5
G6
G7
G8

FIG. 15A



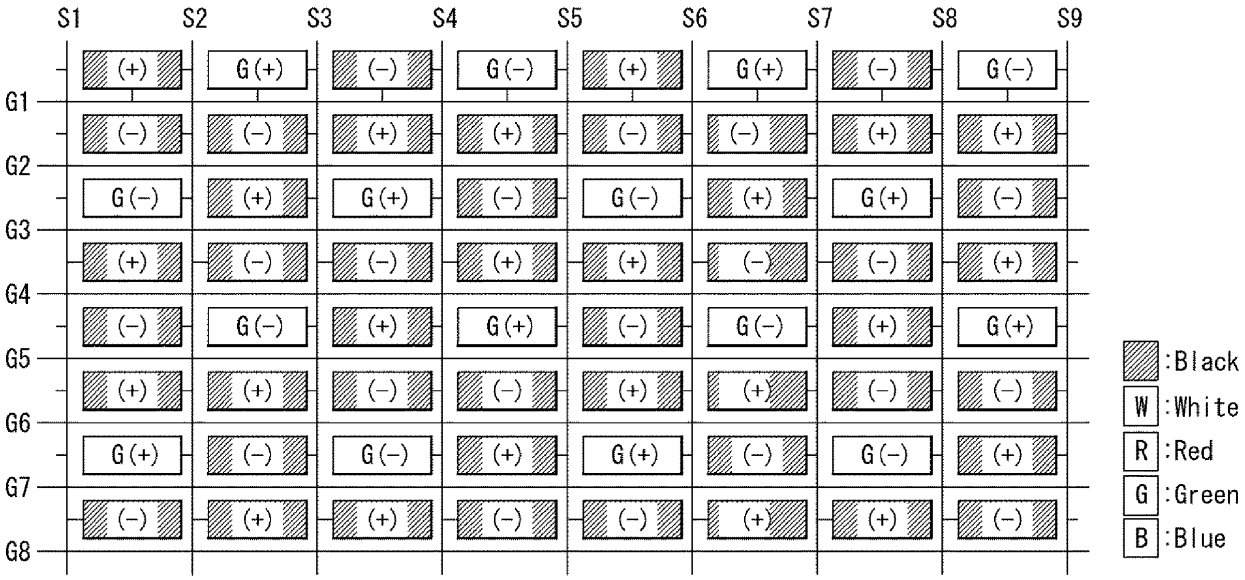
<White>

FIG. 15B


S1
S2
S3
S4
S5
S6
S7
S8
S9
G1
G2
G3
G4
G5
G6
G7
G8
:Black
W :White
R :Red
G :Green
B :Blue

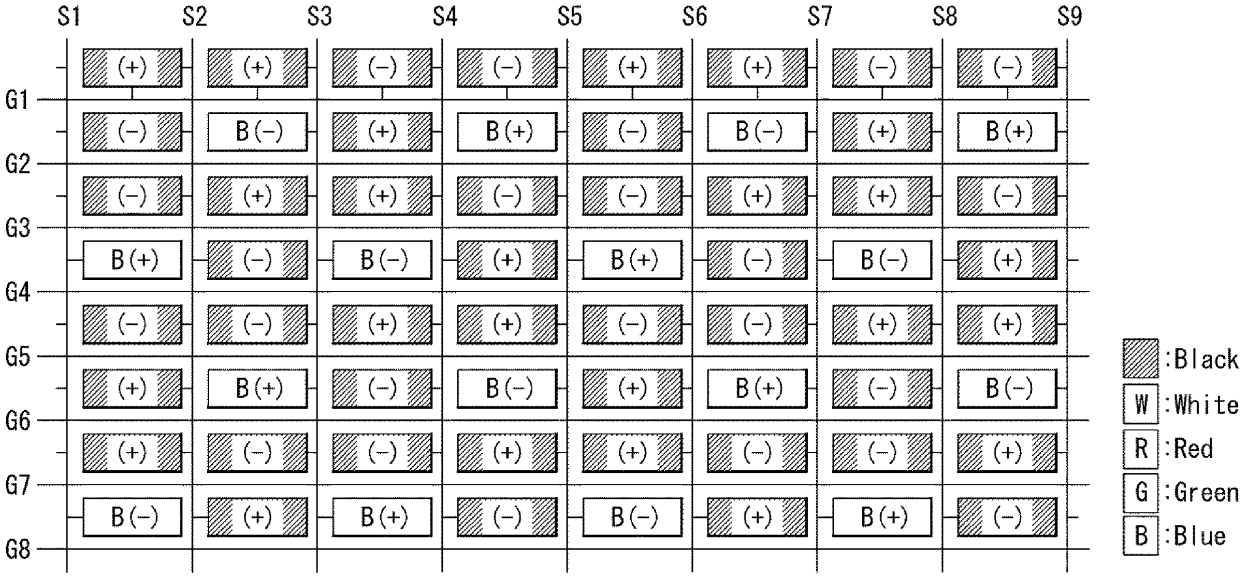
<Red>

FIG. 15C



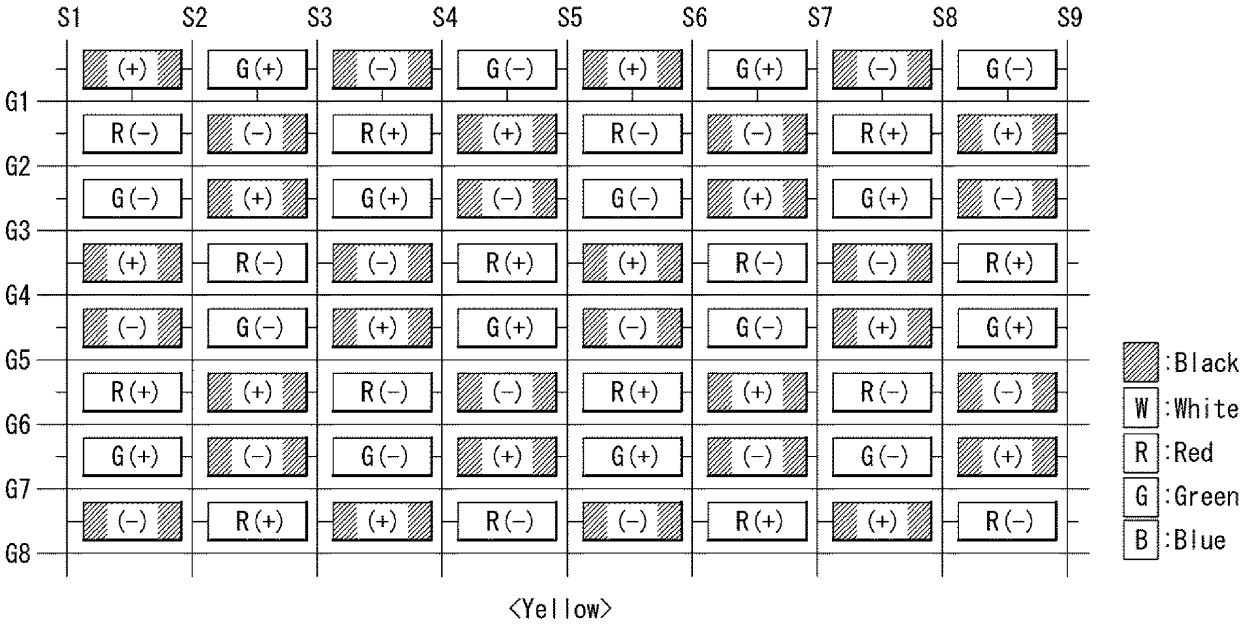
<Green>

FIG. 15D


S1
S2
S3
S4
S5
S6
S7
S8
S9
G1
G2
G3
G4
G5
G6
G7
G8
:Black
W :White
R :Red
G :Green
B :Blue

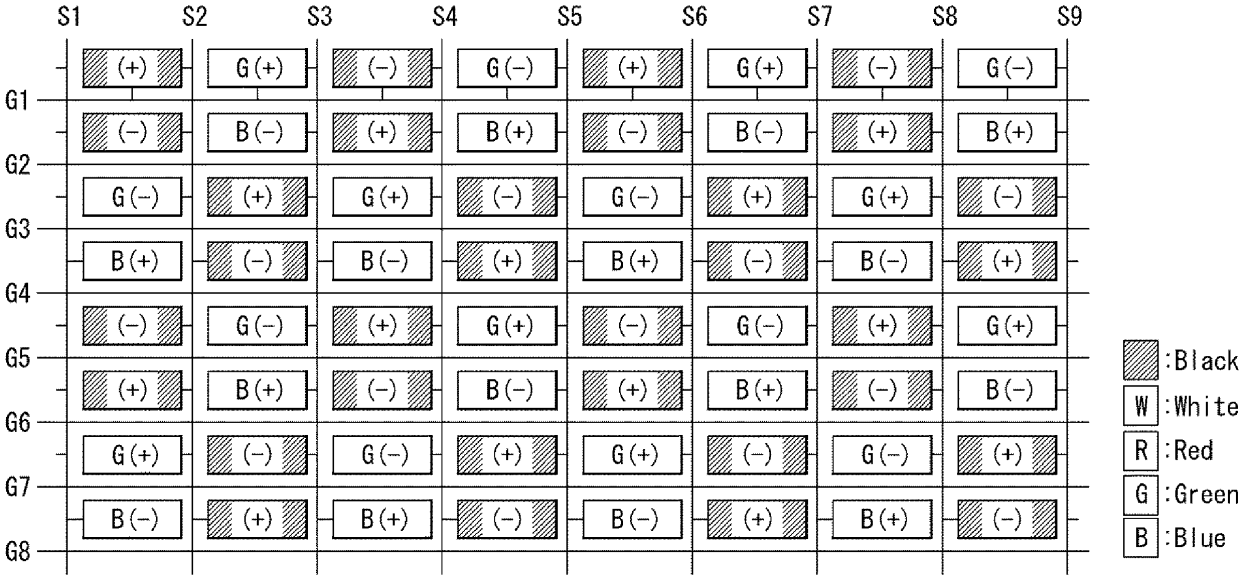
<Blue>

FIG. 15E



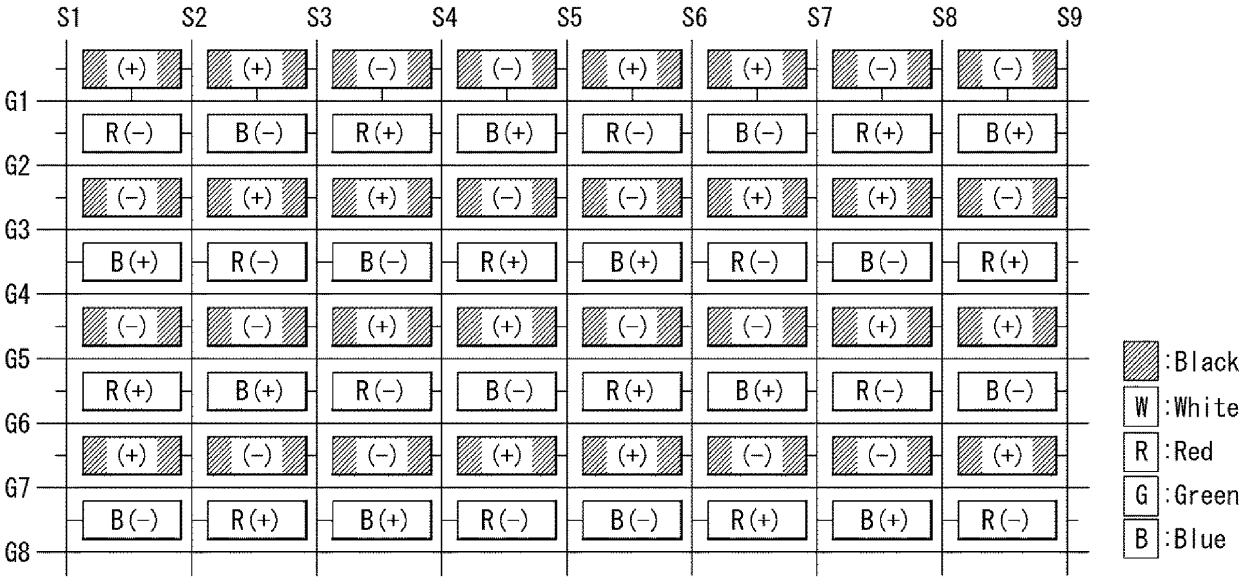
<Yellow>

FIG. 15F


S1
S2
S3
S4
S5
S6
S7
S8
S9
G1
G2
G3
G4
G5
G6
G7
G8
:Black
W :White
R :Red
G :Green
B :Blue

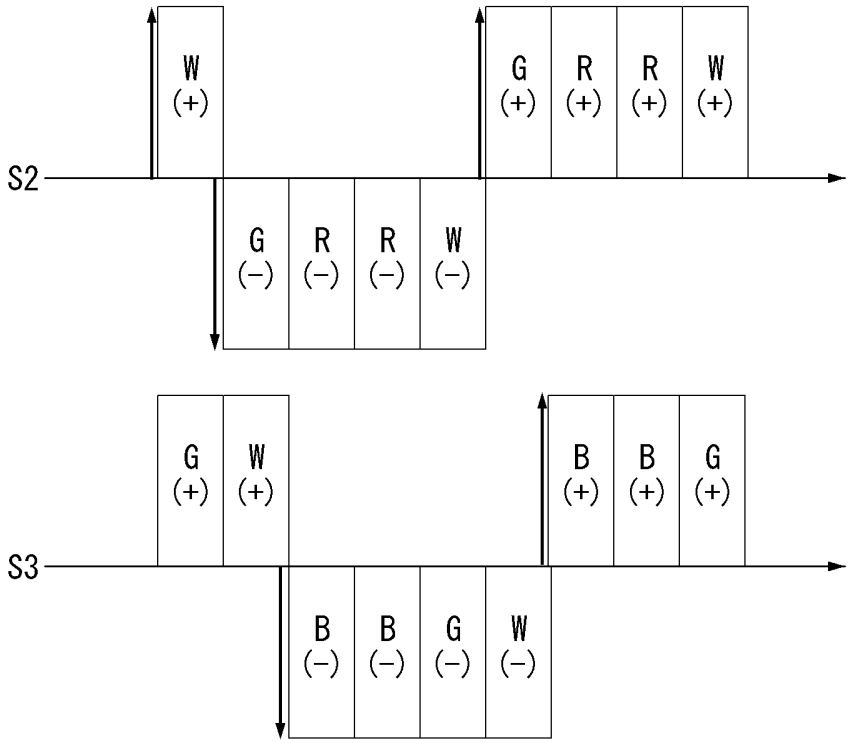
<Cyan>

FIG. 15G



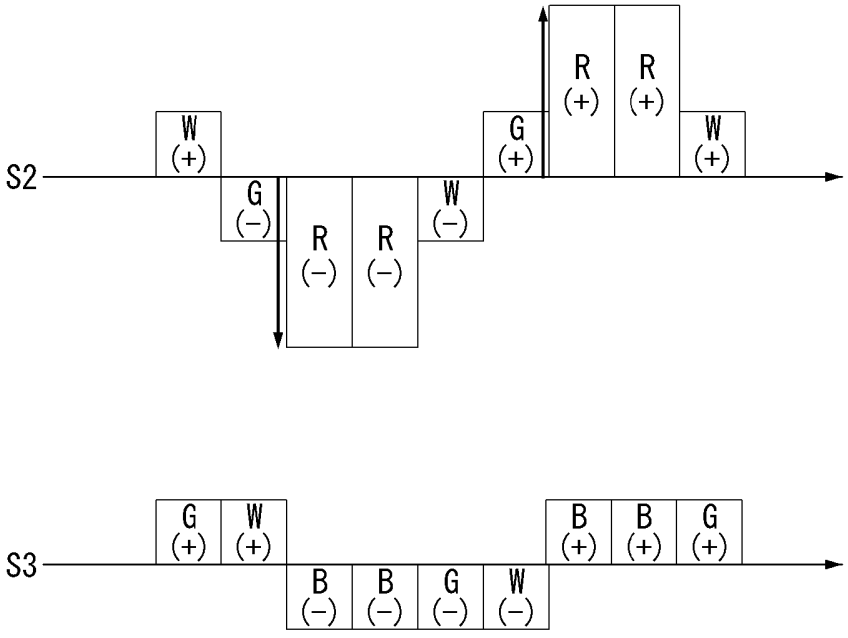
<Magenta>

FIG. 16A



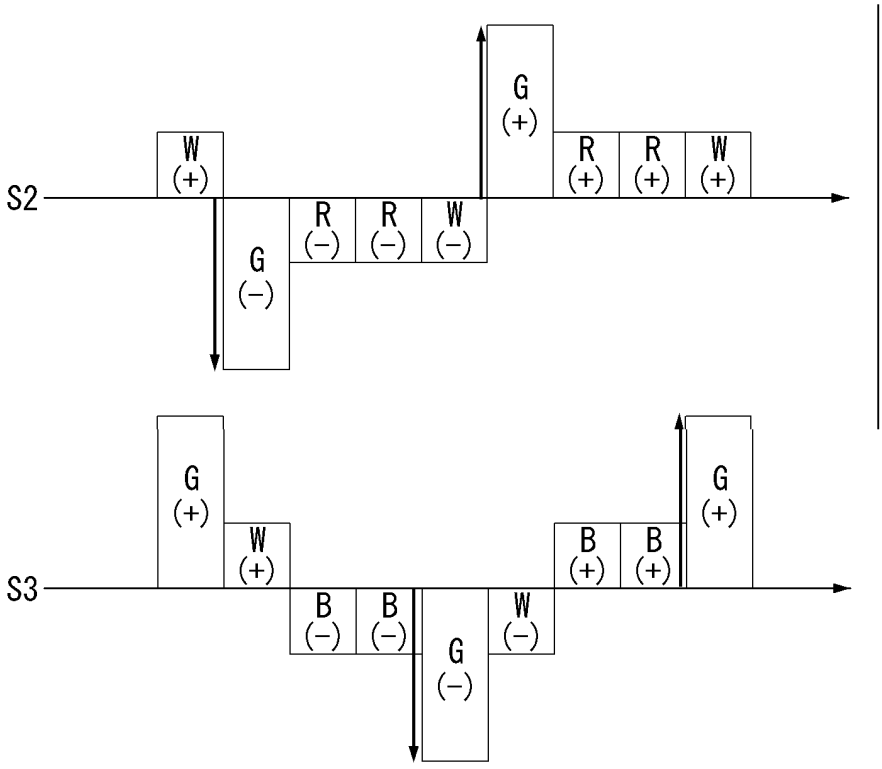
<White>

FIG. 16B



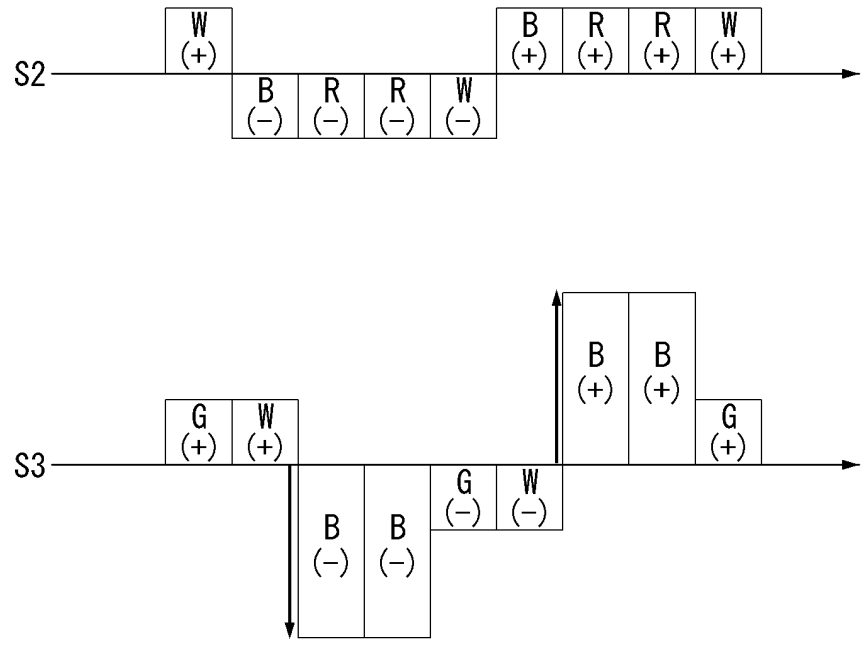
<Red>

FIG. 16C



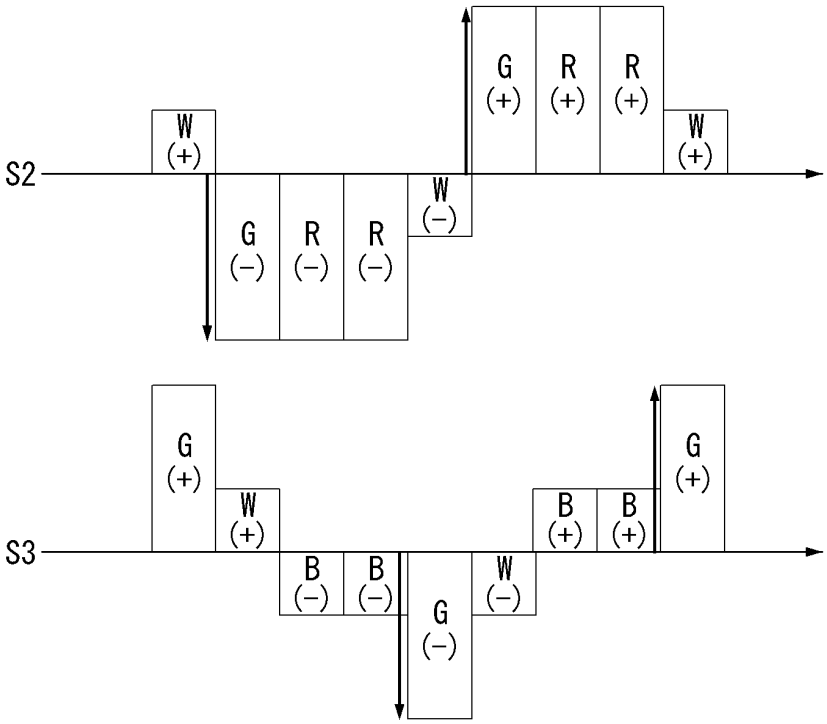
<Green>

FIG. 16D



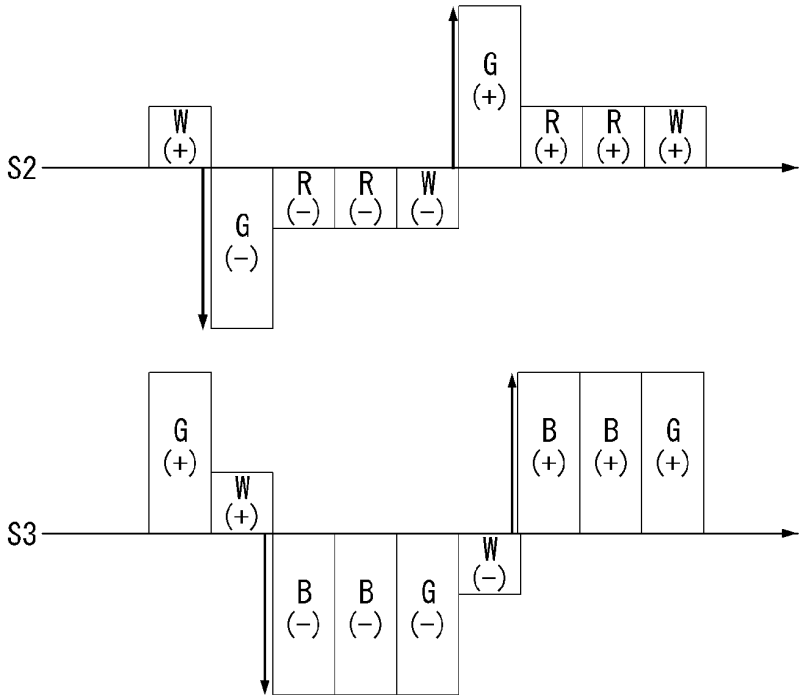
<Blue>

FIG. 16E



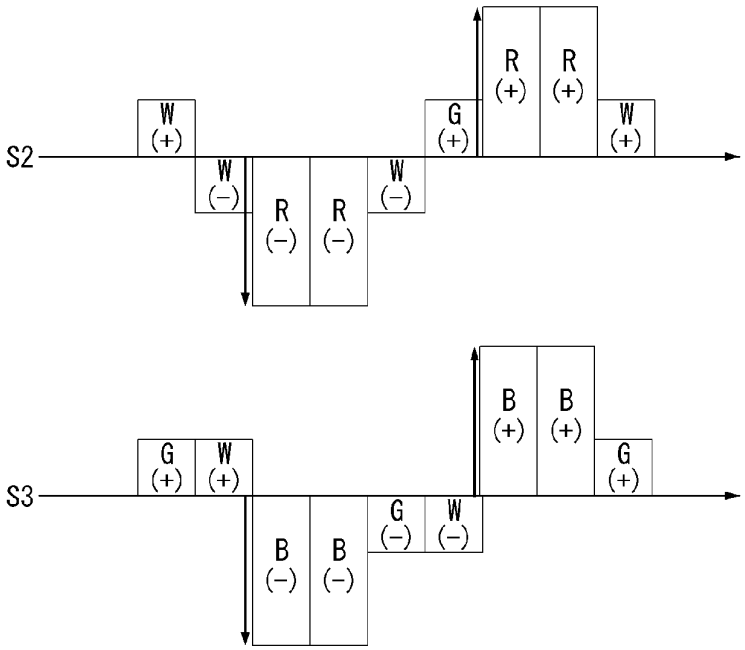
<Yellow>

FIG. 16F



<Cyan>

FIG. 16G



<Magenta>

FIG. 17

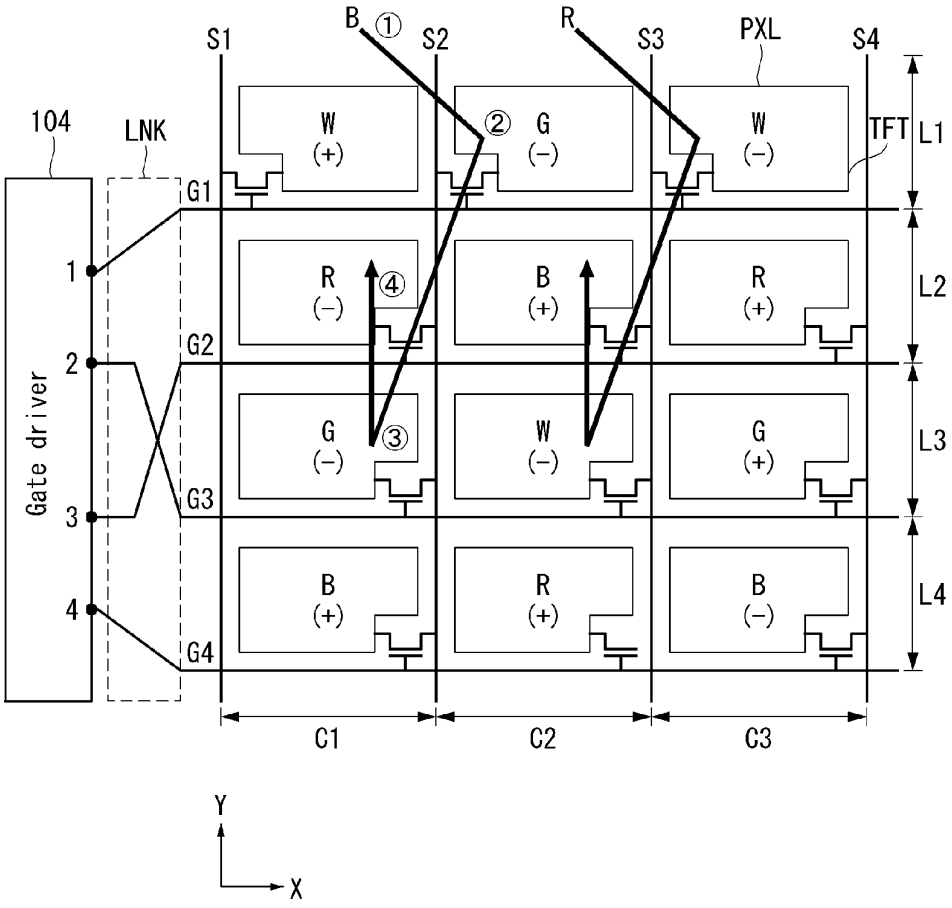


FIG. 18

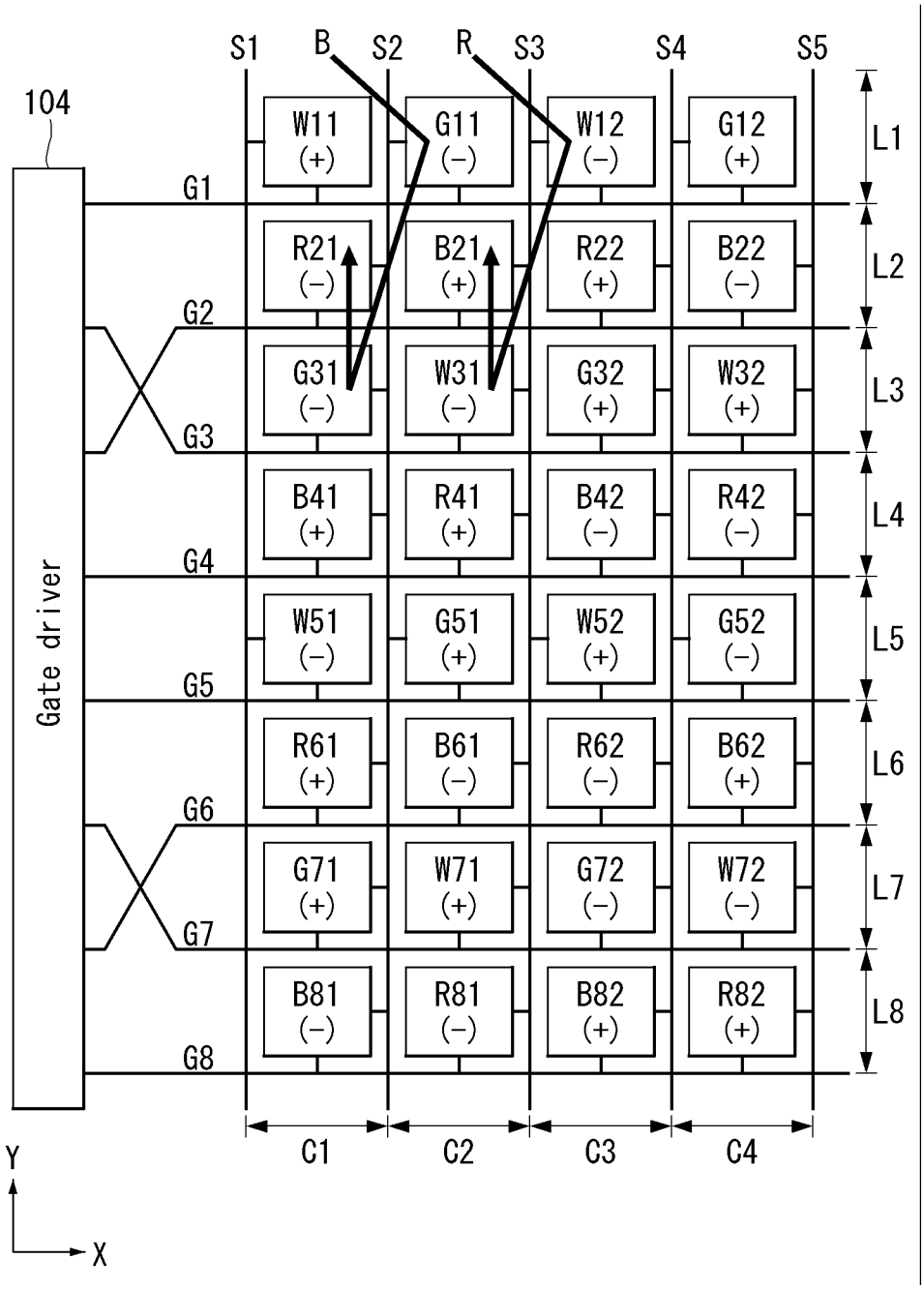

S1
B
S2
R
S3
S4
S5
104
W11 (+)
G11 (−)
W12 (−)
G12 (+)
L1
G1
R21 (−)
B21 (+)
R22 (+)
B22 (−)
L2
G2
G31 (−)
W31 (−)
G32 (+)
W32 (+)
L3
G3
B41 (+)
R41 (+)
B42 (−)
R42 (−)
L4
G4
W51 (−)
G51 (+)
W52 (+)
G52 (−)
L5
G5
R61 (+)
B61 (−)
R62 (−)
B62 (+)
L6
G6
G71 (+)
W71 (+)
G72 (−)
W72 (−)
L7
G7
B81 (−)
R81 (−)
B82 (+)
R82 (+)
L8
G8
Gate driver
C1
C2
C3
C4
Y
X

FIG. 19

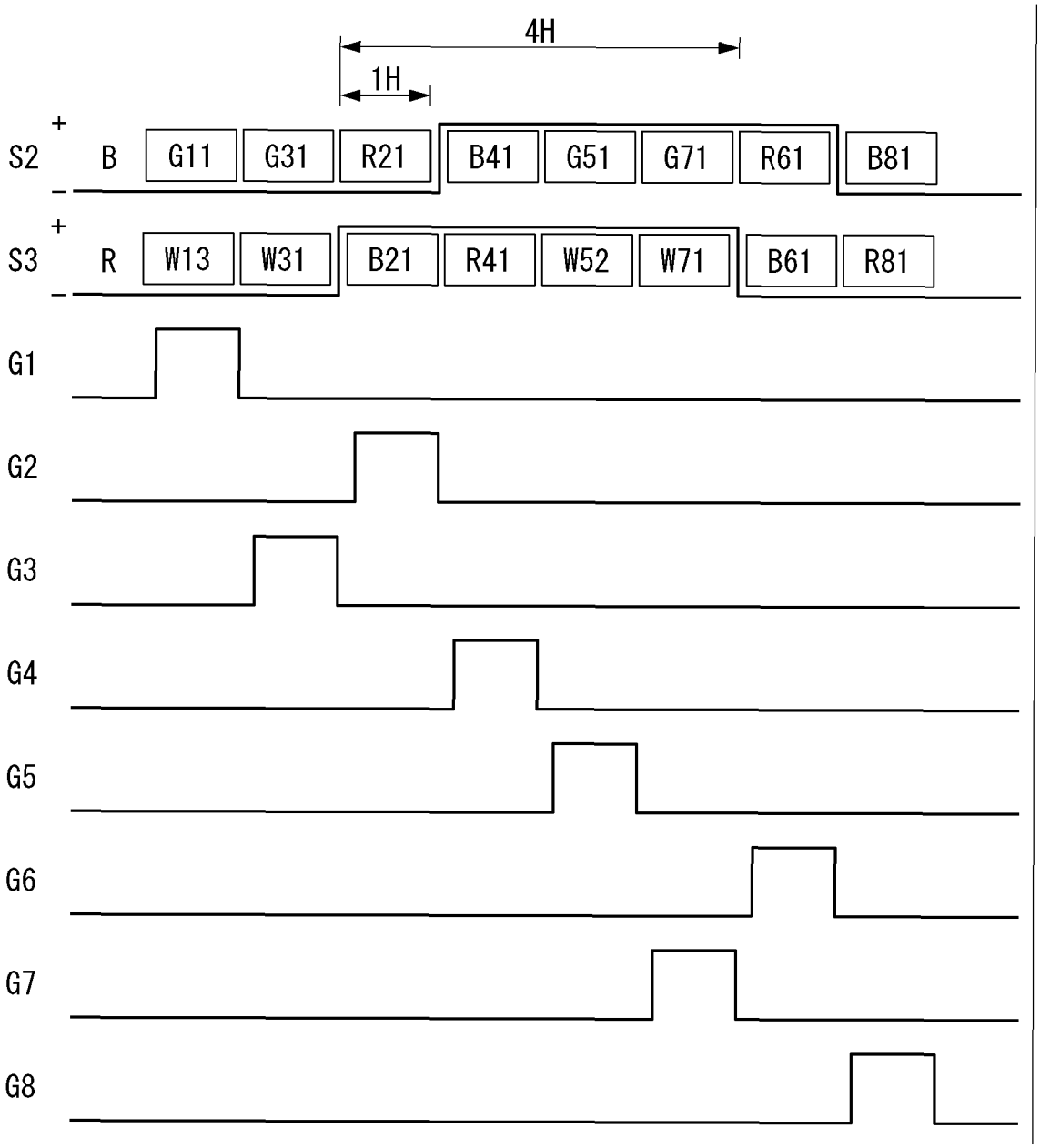
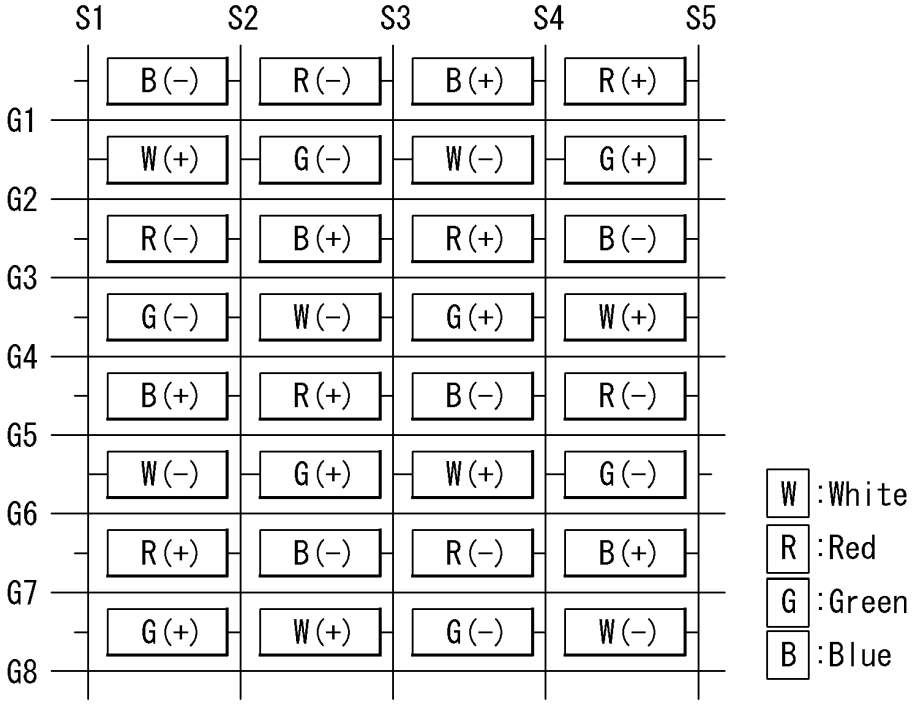
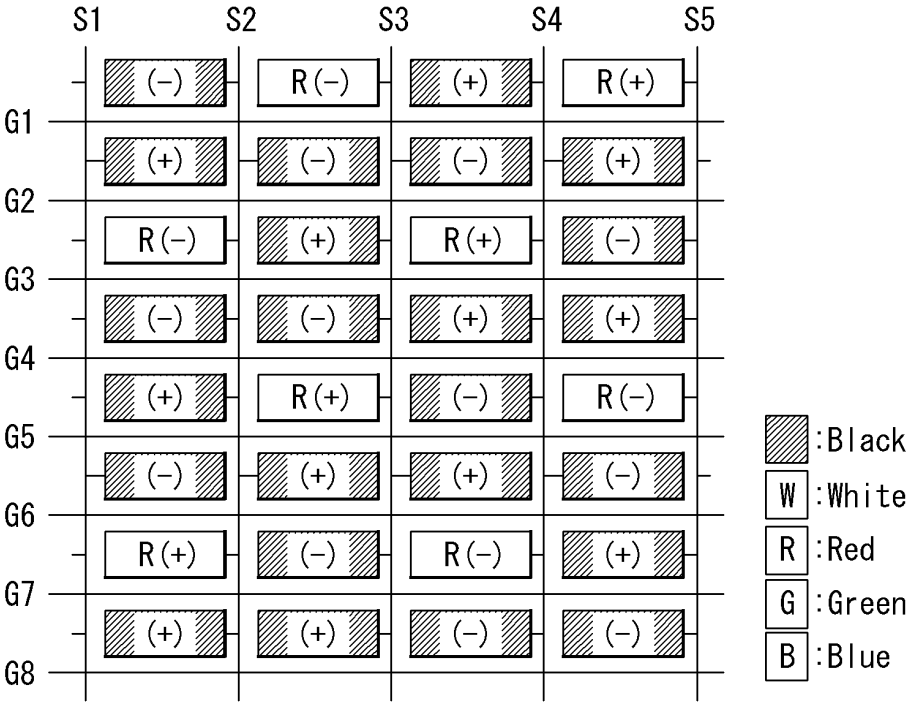

4H
1H
S2
+
B
G11
G31
R21
B41
G51
G71
R61
B81
−
S3
+
R
W13
W31
B21
R41
W52
W71
B61
R81
−
G1
G2
G3
G4
G5
G6
G7
G8

FIG. 20A



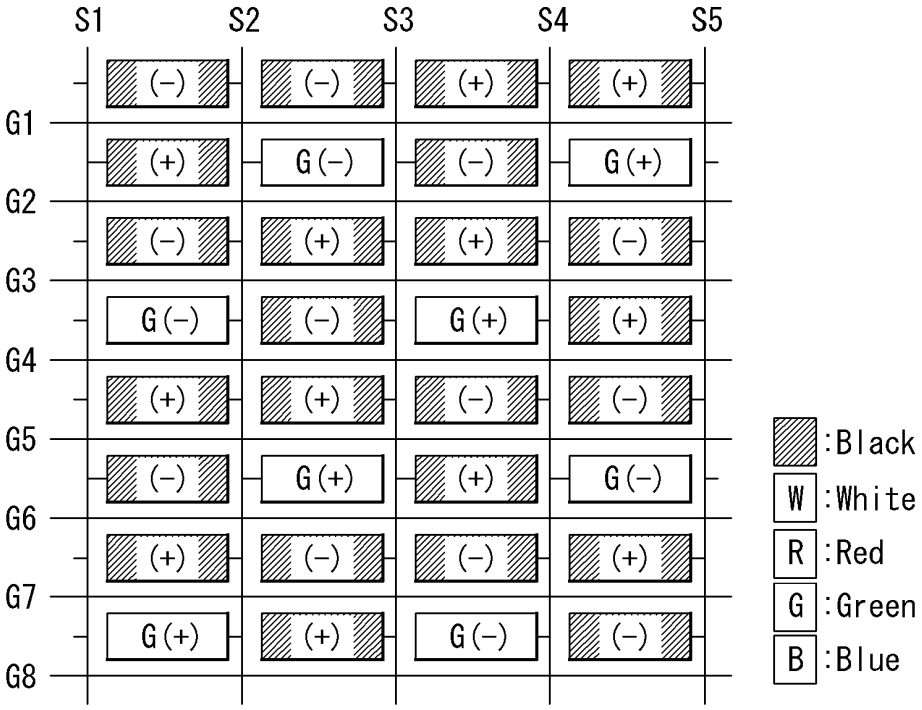
<White>

FIG. 20B



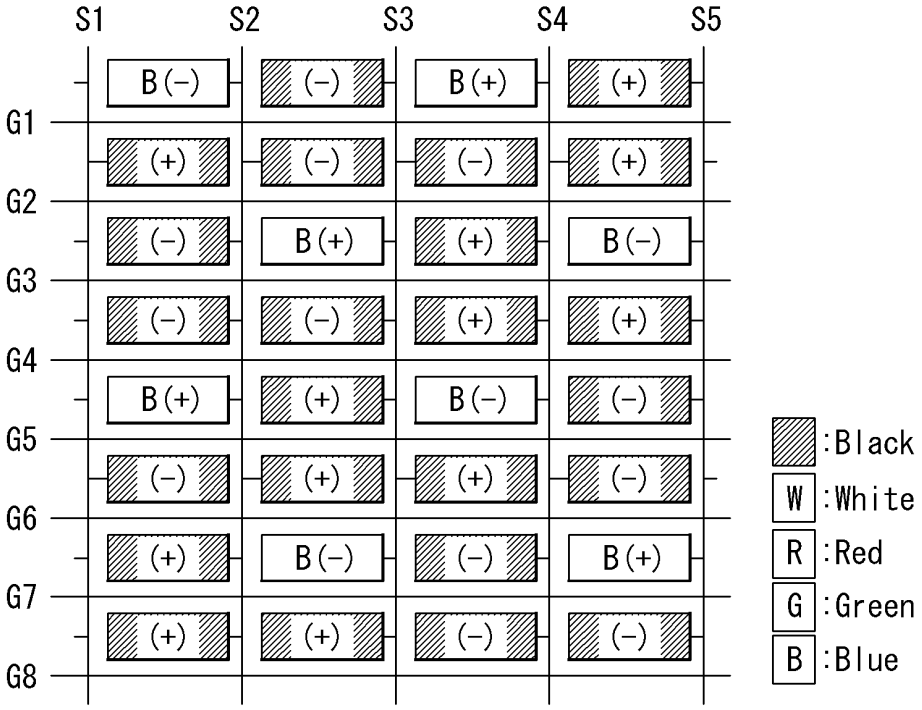
<Red>

FIG. 20C



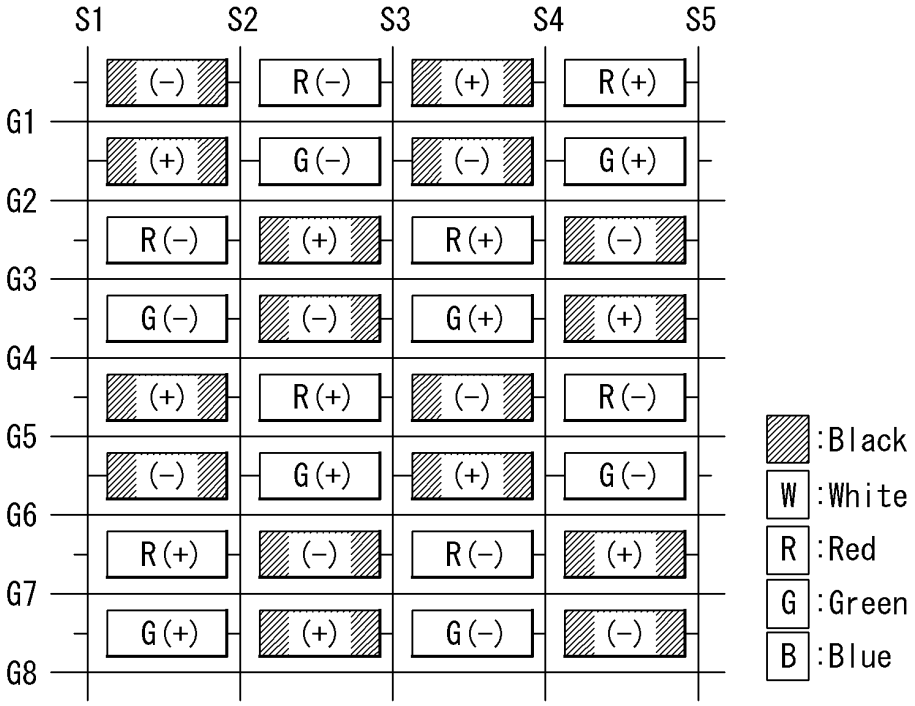
<Green>

FIG. 20D



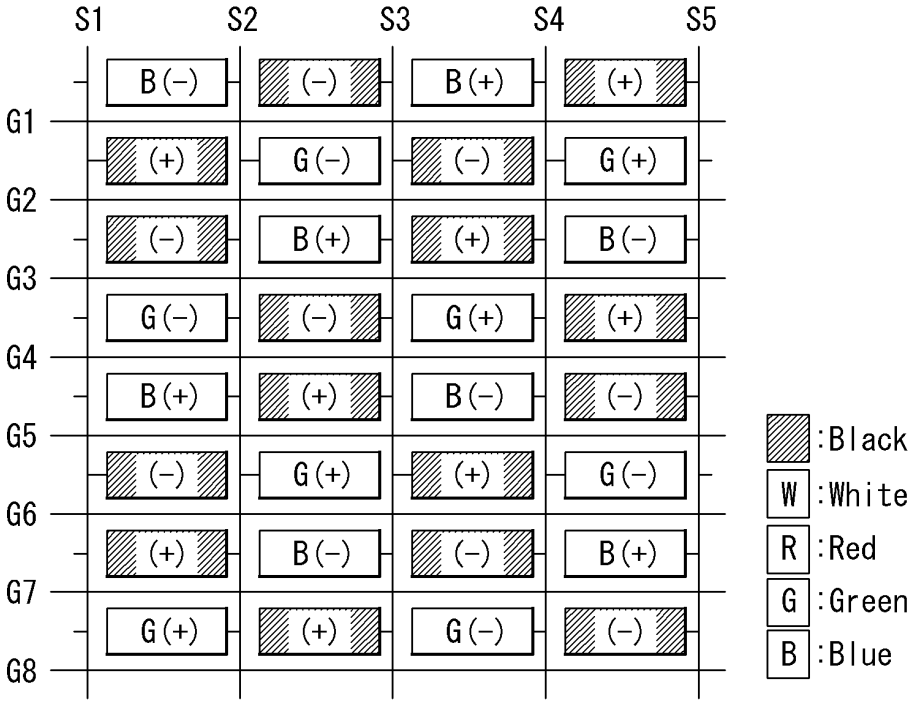
<Blue>

FIG. 20E



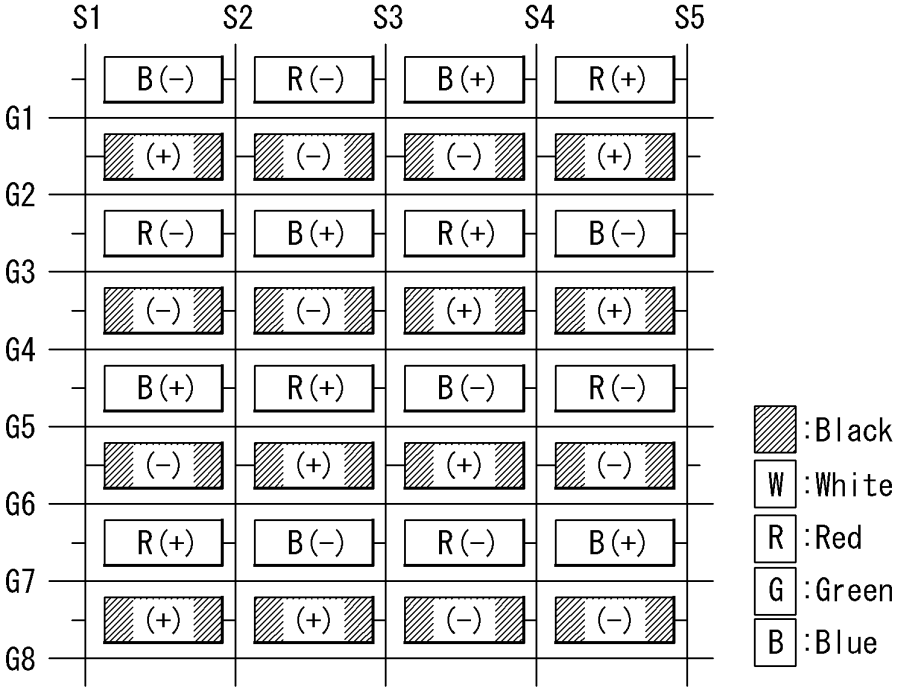
<Yellow>

FIG. 20F



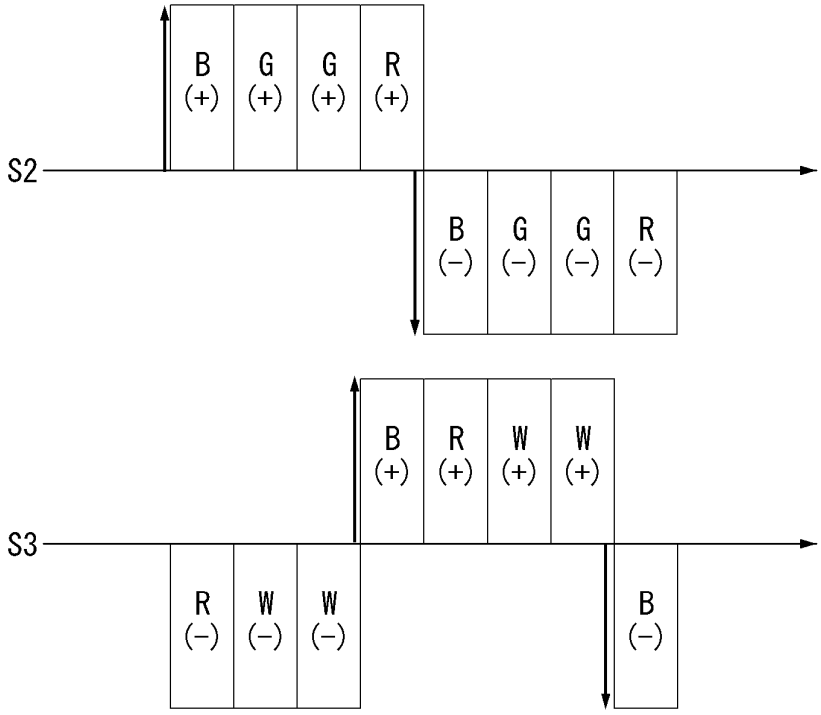
<Cyan>

FIG. 20G



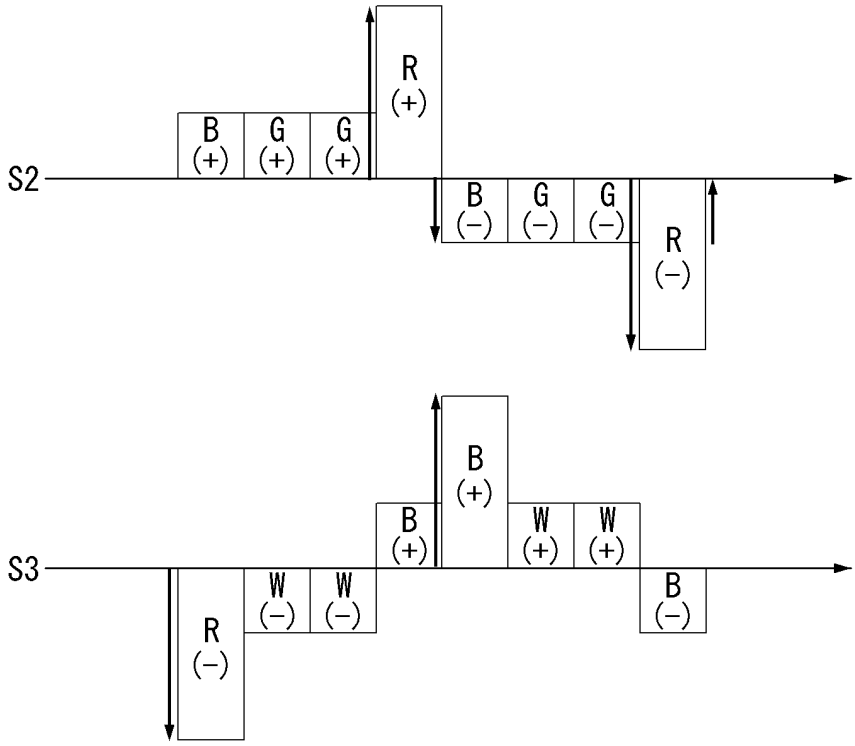
<Magenta>

FIG. 21A



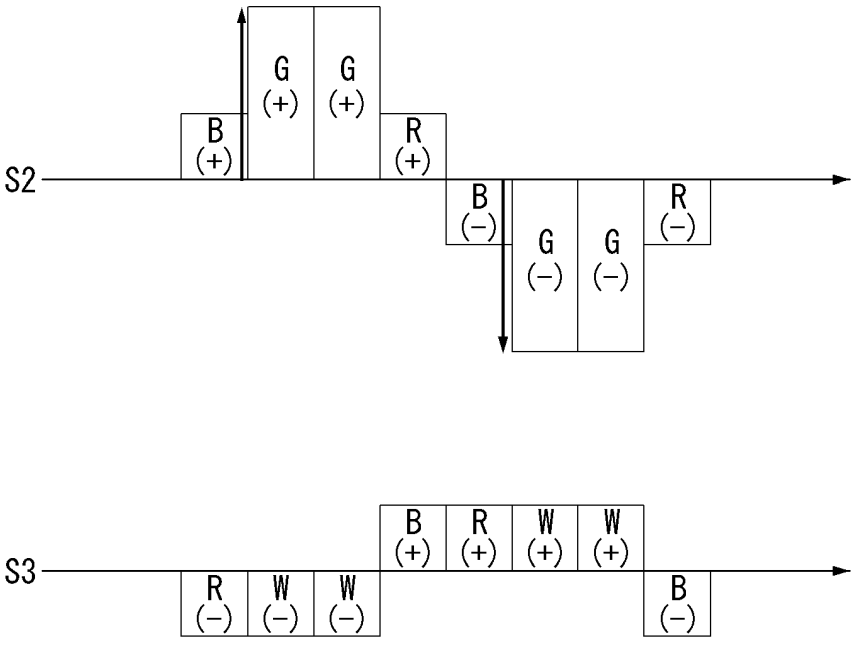
<White>

FIG. 21B



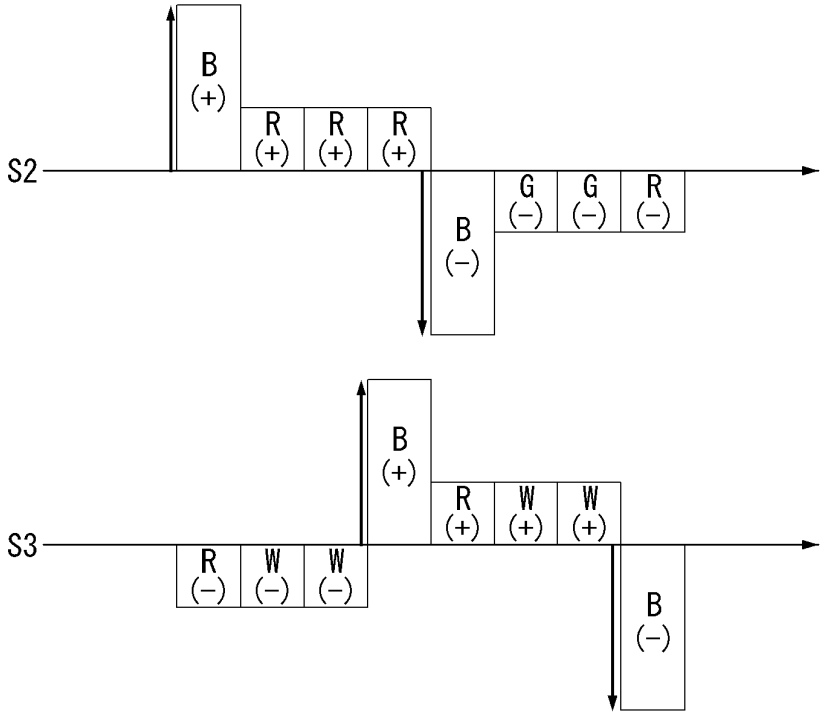
<Red>

FIG. 21C



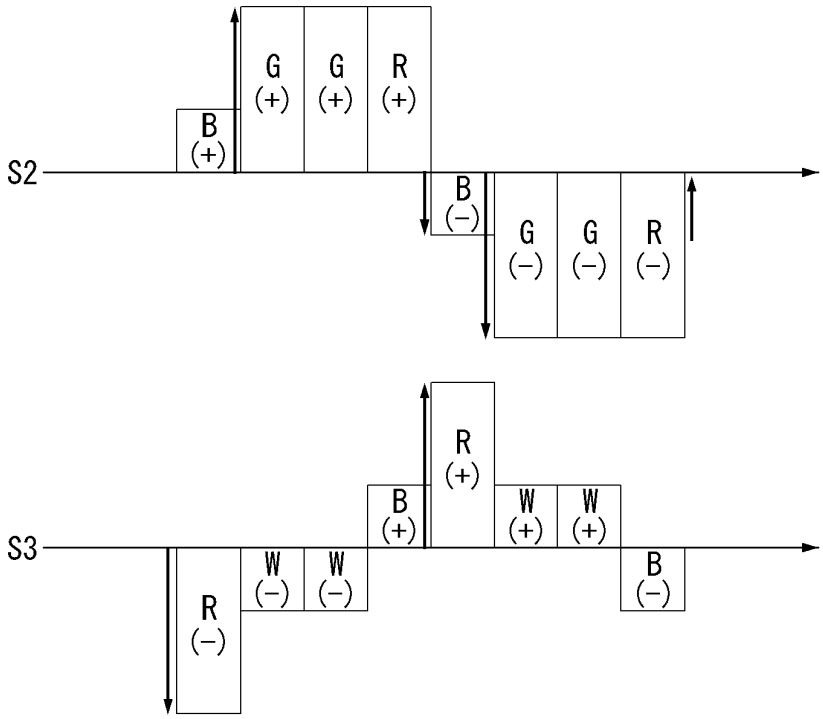
<Green>

FIG. 21D



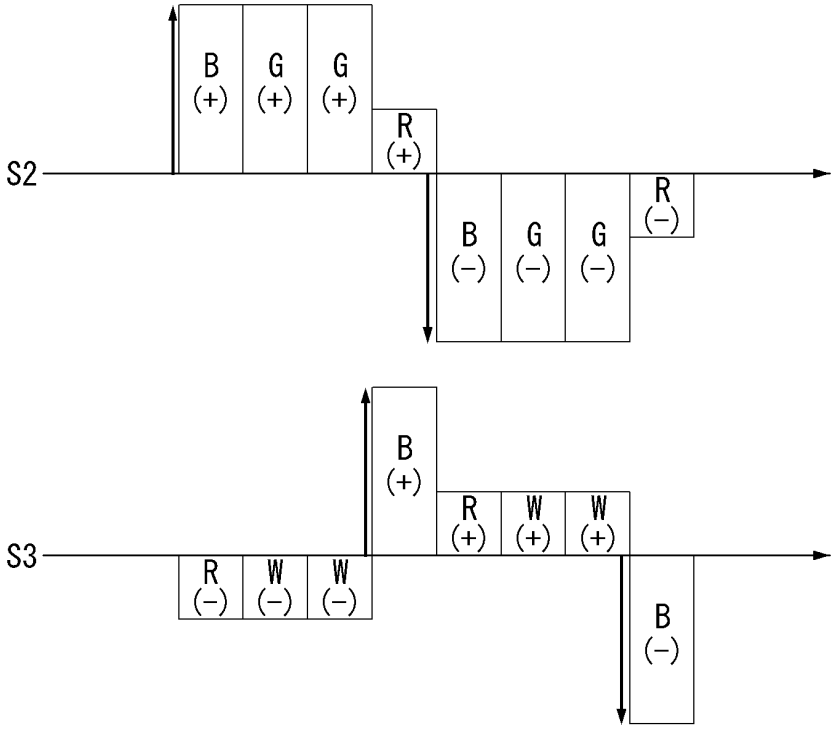
<Blue>

FIG. 21E



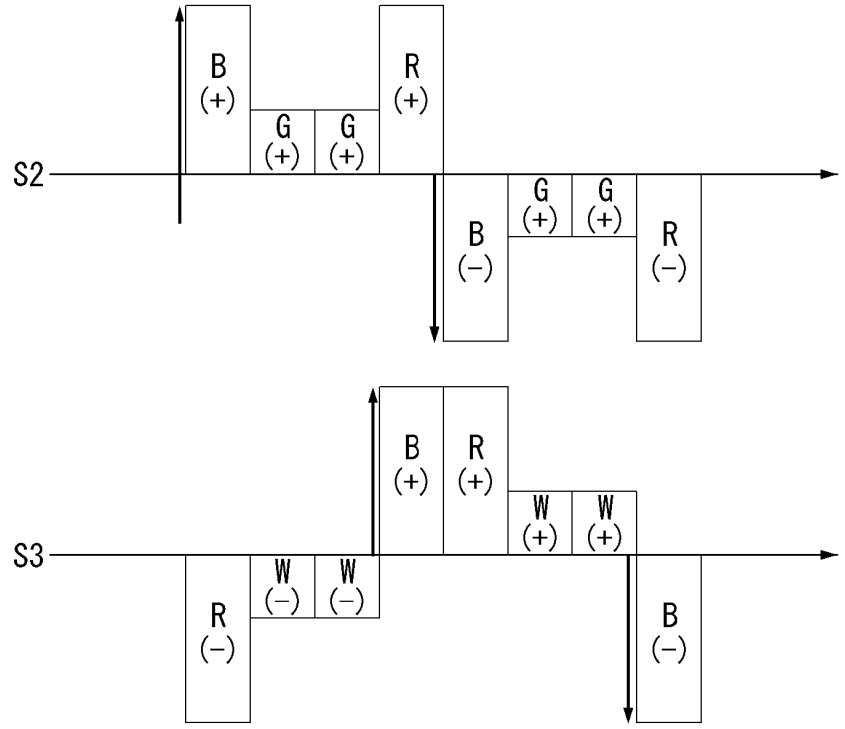
<Yellow>

FIG. 21F



<Cyan>

FIG. 21G



<Magenta>

REFERENCES CITED IN THE DESCRIPTION

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- US 1020080127456 A **[0053]**
- US 46165209 A **[0053]**
- KR 1020080132466 **[0053]**
- US 53734109 A **[0053]**
- KR 1020050039728 **[0055]**
- KR 1020050052906 **[0055]**
- KR 1020050066429 **[0055]**
- KR 1020060011292 **[0055]**

专利名称(译)	液晶显示装置及其驱动方法		
公开(公告)号	EP3252753B1	公开(公告)日	2019-07-03
申请号	EP2017173175	申请日	2017-05-29
[标]申请(专利权)人(译)	乐金显示有限公司		
申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
当前申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
[标]发明人	SANG WOOKYU		
发明人	SANG, WOOKYU		
IPC分类号	G09G3/36		
CPC分类号	G02F1/1362 G09G3/3674 G09G3/3685 G09G3/3607 G09G3/3614 G09G3/3648 G09G3/3677 G09G3/3688 G09G2300/0426 G09G2300/0452 G09G2310/0213 G09G2310/0218 G02F1/13 G02F2001/1635 G09G3/3406 G09G3/3413 G09G3/364 G09G3/3659 G09G2320/0646		
优先权	1020160067776 2016-05-31 KR		
其他公开文献	EP3252753A1		
外部链接	Espacenet		

摘要(译)

公开了一种液晶显示装置及其驱动方法。第一颜色子像素布置在第（4i + 1）行线（i是正整数）和奇数列线相交的位置处，并且第二颜色子像素布置在（4i + 1）的位置处第n行和偶数列线相交。第三颜色子像素布置在第（4i + 2）行和奇数列行相交的位置处，第四颜色子像素布置在第（4i + 2）行和偶数的位置处 - 编号的列线相交。

FIG. 1