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(54) ARRAY SUBSTRATE, PREPARATION METHOD THEREFOR, AND DISPLAY DEVICE

ARRAYSUBSTRAT, HERSTELLUNGSVERFAHREN DAFÜR UND ANZEIGEVORRICHTUNG

SUBSTRAT DE RÉSEAU, SON PROCÉDÉ DE PRÉPARATION, ET DISPOSITIF D'AFFICHAGE

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Description

Field of the Invention

[0001] The present invention relates to the field of liquid crystal display technology, and particularly to an array substrate, a manufacturing method thereof and a display device.

Background of the Invention

[0002] With the development in technology and process of thin film transistors of flat panel display devices, liquid crystal panels are developing to have high resolution and high definition. Fig. 1 is a structure of color filter (comprising a color filter 107 and a black matrix 106) on Array (COA), i.e., a COA array substrate, and since there is no problem of light leak due to substrates alignment, width of the black matrix 106 can be effectively reduced, thus increasing aperture ratio of a pixel and further improving transmittance of the panel. When COA technology is combined with Advanced Super Dimension Switch liquid crystal display technology which mainly depends on in-plane rotation of liquid crystal molecules, light leak in an oblique direction can be effectively prevented, and further occurrence of color mixing can be avoided. Thus, this technology has become one of the competitive technologies in high-definition products.

[0003] As shown in Fig. 1, generally, a basic structure of a COA array substrate includes a pattern including a thin film transistor formed on a substrate 101, wherein the thin film transistor may be of top-gate type or bottom-gate type, and a bottom-gate type thin film transistor is taken as an example here. The thin film transistor specifically includes: a gate 102, a gate insulating layer 103 covering the gate 102, an active region 104 provided on the gate insulating layer 103 and source and drain 105, and the source and drain 105 are connected to the active region 104. A light filtering layer 107 is provided on the substrate 101 on which the thin film transistor has been formed; a planarization layer 108 is provided on the light filtering layer to eliminate level difference; then a first electrode layer (common electrode) 110, a passivation layer 111 (PVX) and a second electrode layer (pixel electrode) 112 are sequentially provided, wherein the second electrode layer (pixel electrode) 112 is connected to the drain 105 of the thin film transistor through a contacting via 109 penetrating through the passivation layer 111, the first electrode layer (common electrode) 110, the planarization layer 108 and the light filtering layer. In this case, since at the contacting via 109, liquid crystals may be irregularly arranged and thus light leak may occur, the drain 105 needs to be lengthened, so as to avoid light leak. However, an increase in the length of the drain 105 will result in decreased aperture ratio and increased power consumption of the product. Moreover, since the contacting via 109 is relatively deep, and its opening at the top is relatively large, the aperture ratio of the COA array substrate is further affected. Further, the relatively deep contacting via 109 may likely lead to disconnection, which results in that the pixel electrode is disconnected with the drain and the pixel cannot be charged.

[0004] Korean patent application KR 2013 0054772 A discloses a color filter layer which is formed on a pixel area by crossing a gate line and a data line, wherein an organic insulation layer includes an opening unit which exposes a TFT(Thin Film Transistor). A pixel electrode is directly connected to the TFT through the opening unit. A passivation layer is formed on the organic insulation layer including the pixel electrode. A plurality of common electrodes is formed on the passivation layer and is overlapped with the pixel electrode.

[0005] Chinese patent application CN 103 309 081 A discloses an array substrate and a manufacturing method thereof and a display device, and relates to the field of display. The display device can lower the influence of an alignment deviation of the array substrate and a color film substrate on the transmittance rate and avoid light leak caused by the alignment deviation. The array substrate comprises a substrate, a plurality of pixels formed on the substrate, black matrixes for spacing the pixels, and patterned color resistance layers, wherein a grid electrode, a grid insulation layer, a semiconductor layer, a source electrode and a drain electrode are arranged on the substrate in a region where the black matrixes are located; first and second electrodes used for generating an electric field to drive liquid crystals are arranged on the substrate in a region corresponding to the pixels; the second electrode is arranged above the first electrode; and each color resistance layer is arranged between the grid insulation layer and a layer on which the second electrode is and distributed in the region corresponding to the pixels. The array substrate is used for improving the display device and is capable of increasing the transmittance rate of the display device.

Summary of the Invention

[0006] Technical problem to be solved by the present invention includes providing an array substrate having an improved aperture ratio, a manufacturing method thereof and a display device, in view of the above defects in the existing array substrates.

[0007] To solve the above technical problem, the present invention provides an array substrate according to claim 1, which comprises: a light filtering layer provided on a substrate with a thin film transistor formed thereon, a planarization layer covering the light filtering layer, and a pixel electrode provided above the planarization layer, the array substrate further comprises: a third electrode layer connected to a drain of the thin film transistor and extending onto the light filtering layer; and a contacting via penetrating through the planarization layer and provided above a portion of the third electrode layer on the light filtering layer, the pixel electrode being connected to the third electrode layer through the contacting via.

[0008] The drain of the array substrate of the present invention is electrically connected to the pixel electrode through the third electrode layer connected to the drain and extending onto the light filterubg layer, the contacting via penetrating through the planarization layer is provided above a portion of the third electrode layer on the light filtering layer, and the pixel electrode is connected to the third electrode layer through the contacting via. Since the contacting via of the present invention, compared to the contacting via for connecting the drain to the pixel electrode in the prior art, obviously has a smaller opening, and the drain does not need to be lengthened, the aperture ratio is apparently improved.

[0009] Preferably, the light filtering layer comprises a color filter and a black matrix, the pixel electrode is positioned above the color filter, the black matrix is at least positioned above the thin film transistor, the color filter and the black matrix are provided alternately on the substrate, and the third electrode layer extends onto the color filter or extends onto the black matrix.

[0010] Preferably, the array substrate further comprises a passivation layer and a common electrode sequentially provided on the pixel electrode.

[0011] Alternatively, the array substrate further comprises a passivation layer and a common electrode provided between the pixel electrode and the planarization layer, the common electrode and the passivation layer are sequentially provided on the planarization layer and the contacting via penetrates through the planarization layer and the passivation layer.

[0012] Further preferably, materials of the pixel electrode and the common electrode are indium tin oxide.

[0013] To solve the technical problem of the present invention, the present invention further provides a manufacturing method of the above array substrate, which comprises steps of:

forming, on a substrate with a thin film transistor formed thereon, a pattern including a light filtering layer through a patterning process;

forming, on the substrate subjected to the above step, a third electrode layer connected to a drain of the thin film transistor and extending onto the light-filtering layer through a patterning process;

forming, on the substrate subjected to the above steps, a planarization layer, and forming a contacting via penetrating through the planarization layer above a portion of the third electrode layer on the light filtering layer; and

forming, on the substrate subjected to the above steps, a pattern including a pixel electrode through a patterning process, wherein the pixel electrode is connected to the third electrode layer through the contacting via penetrating through the planarization layer.

[0014] Preferably, the light filtering layer comprises a color filter and a black matrix, the pixel electrode is formed above a the color filter, the black matrix is at least formed above the thin film transistor, the color filter and the black matrix are provided alternately on the substrate, and the third electrode layer extends onto the color filter or extends onto the black matrix.

[0015] Preferably, the manufacturing method further comprises steps of:

forming a passivation layer on the pixel electrode; and

forming, on the passivation layer, a pattern including a common electrode through a patterning process.

[0016] Alternatively, after forming the planarization layer and before forming, above a portion of the third electrode layer on the light filtering layer, the contacting via penetrating through the planarization layer, the manufacturing method further comprises steps of:

forming, on the planarization layer, a pattern including a common electrode through a patterning process; and

forming a passivation layer on the common electrode,

wherein the contacting via penetrating through the planarization layer and formed above a portion of the third electrode layer on the light filtering layer also penetrates through the passivation layer.

[0017] The manufacturing method of the array substrate of the present invention is simple and is easy to implement.

[0018] A technical solution used to solve the technical problem of the present invention is a display device, which comprises the above array substrate.

[0019] As the display device of the present invention includes the above array substrate, its aperture ratio is increased.

Brief Description of the Drawings

[0020]

Fig. 1 is a schematic diagram of a structure of an array substrate of the prior art;

Fig. 2 is a schematic diagram of a structure of an array substrate according to an embodiment of the present invention;

Fig. 3 is a schematic diagram of a structure of another array substrate according to an embodiment of the present invention; and

Fig. 4 is a schematic diagram of a structure of still another array substrate according to an embodiment of the present invention.

[0021] Reference numerals: 101, substrate; 102, gate; 103, gate insulating layer; 104, active region; 105, source/drain; 106, black matrix; 107, color filter; 108,

planarization layer; 109, contacting via; 110, first electrode layer; 111, passivation layer; 112, second electrode layer; 113, third electrode layer.

Detailed Description of the Embodiments

[0022] To enable those skilled in the art to better understand the technical solutions of the present invention, the present invention will be further described in detail below in conjunction with the accompanying drawings and the specific implementations.

Embodiment 1:

[0023] As shown in Figs. 2 to 4, the present embodiment provides an array substrate, which comprises a thin film transistor provided on a substrate 101. It should be noted that the thin film transistor may be of top-gate type or bottom-gate type, and a bottom-gate type thin film transistor is taken as an example here. The thin film transistor specifically comprises: a gate 102, a gate insulating layer 103 covering the gate 102, an active region 104 provided on the gate insulating layer 103, and source and drain 105 connected to the active region 104. The array substrate further comprises a light filtering layer (comprising a color filter and a black matrix) provided on the substrate 101 with the thin film transistor formed thereon, a planarization layer 108 covering the light filtering layer, a pixel electrode provided on the planarization layer 108, and a third electrode layer 113 connected to the drain 105 of the thin film transistor and extending onto the light filtering layer (at least covering a portion of the light filtering layer). Preferably, one end of the third electrode layer 113 is connected to the drain 105 of the thin film transistor and the other end thereof extends onto an upper surface of the light filtering layer. Here, a contacting via 109 penetrating through the planarization layer 108 is provided above a portion of the third electrode layer 113 on the light filtering layer, and the pixel electrode is connected to the third electrode layer 113 through the contacting via 109 and is then connected to the drain 105 of the thin film transistor.

[0024] The drain 105 of the thin film transistor on the array substrate of the present embodiment is connected to the pixel electrode through the third electrode layer 113 extending onto the light filtering layer, without lengthening the length of the drain 105, and therefore, the aperture ratio of the array substrate will not be affected. In particular, as the third electrode layer 113 extends onto a portion of the light filtering layer, only a contacting via 109 that penetrates through the planarization layer 108 above a portion of the third electrode layer 113 on the light filtering layer needs to be formed. The contacting via 109, compared to the contacting via in the prior art, has a shallower depth and a narrower opening width, and as a result, compared to an existing array substrate, the array substrate provided by the present embodiment has an apparently improved aperture ratio.

[0025] As shown in Figs. 2 to 4, the second electrode layer 112 is provided above the first electrode layer 110 and is spaced apart from the first electrode layer 110 by the passivation layer 111. Of the first electrode layer 110 and the second electrode layer 112, the electrode that is connected to the drain 105 of the thin film transistor through the third electrode layer 113 is the pixel electrode, and the other electrode is the common electrode. Specific description is given below.

[0026] As shown in Fig. 2, as a case of the present embodiment, preferably, the third electrode layer 113 extends onto the color filter 107 (e.g., red filter, green filter, blue filter) (covering a portion of the color filter 107), and the first electrode layer 110 is positioned above the color filter 107. In this case, a contacting via 109 penetrating through the planarization layer 108 is formed above a portion of the third electrode layer 113 on the color filter 107, so that the third electrode layer 113 is connected to the first electrode layer 110. In this case, the drain 105 of the thin film transistor does not need to be lengthened, depth and opening width of the contacting via 109 penetrating through the planarization layer 108 are smaller than those of the contacting via of the existing array substrate shown in Fig. 1, and therefore, the aperture ratio of the array substrate of the present embodiment can be apparently improved.

[0027] Alternatively, as shown in Fig. 3, preferably, the third electrode layer 113 may extend onto the black matrix 106 (covering a portion of the black matrix 106), and the black matrix 106 covers the thin film transistor (the black matrix 106 is used for avoiding light leak in an area where the thin film transistor is positioned). In this case, a contacting via 109 penetrating through the planarization layer 108 is formed above a portion of the third electrode layer 113 on the black matrix 106, so that the third electrode layer 113 is connected to the first electrode layer 110. Since the black matrix 106 is provided above the thin film transistor, the contacting via 109 is provided above the black matrix 106, and obviously, the depth and opening width of the contacting via 109 are smaller than those of the contacting via of the existing array substrate shown in Fig. 1, and therefore, the aperture ratio of the array substrate of the present embodiment is apparently improved.

[0028] It should be noted that, in the above array substrate shown in Fig. 2 or 3, the first electrode layer 110 is pixel electrode, the pixel electrode is provided on the planarization layer 108, further, the passivation layer 111 and the second electrode layer 112 are sequentially formed on the pixel electrode, the second electrode layer 112 is common electrode, and the pixel electrode (the first electrode layer 110) is connected to the third electrode layer 113 through the contacting via 109 and is thus connected to the drain 105 of the thin film transistor.

[0029] Alternatively, as shown in Fig. 4, the first electrode layer 110 may be common electrode, the second electrode layer 112 may be pixel electrode, the common electrode is provided on the planarization layer 108, fur-

ther, the passivation layer 111 and the pixel electrode are sequentially formed on the common electrode, the pixel electrode is connected to the third electrode layer 113 through the contacting via 109 and is thus connected to the drain 105 of the thin film transistor. In this case, the contacting via 109 penetrates through both the planarization layer 108 and the passivation layer 111.

[0030] In addition, in the case of Fig. 4, the third electrode layer 113 may extend onto the color filter 107, and other structures are similar to those shown in Fig. 4. That is, the pixel electrode is connected to the third electrode layer 113 through the contacting via 109 penetrating through both the planarization layer 108 and the passivation layer 111, and is thus connected to the drain 105 of the thin film transistor.

[0031] In the present embodiment, the first electrode layer 110 is a plate-shaped electrode, or may be a strip-shaped electrode; the second electrode layer 112 above the first electrode layer 110 is a strip-shaped electrode. According to electric field direction, an ADS mode liquid crystal display is adopted in this case. Needless to say, liquid crystal display of other mode may also be adopted. Further preferably, materials of the pixel electrode and the common electrode are both indium tin oxide, and of course other transparent conductive material can also be adopted.

Embodiment 2

[0032] The present embodiment provides a manufacturing method of an array substrate, which comprises steps as below.

[0033] At step 1, a pattern including a thin film transistor is formed through a patterning process on a substrate 101, wherein, the thin film transistor is of top-gate type or bottom-gate type. Here, description is given by taking a case that a bottom-gate type thin film transistor is manufactured as an example. Specifically, a gate is formed on the substrate 101 through processes such as sputtering, exposure, development, etching, stripping and the like, a gate insulating layer 103 is formed on the gate 102 through Plasma Enhanced Chemical Vapor Deposition or the like, an active region 104 is formed on the gate insulating layer 103 through processes such as sputtering, exposure, development, etching, stripping and the like, and source and drain 105, which are connected to the active region 104, are formed on the active region 104 through processes such as sputtering, exposure, development, etching, stripping and the like.

[0034] Here, the gate 102 may be a single layer or a laminated film with multiple layers formed from one or more materials selected from molybdenum (Mo), molybdenum-niobium alloy (MoNb), aluminum (Al), neodymium-aluminum alloy (AlNd), titanium (Ti) and Copper (Cu), and preferably is a signal layer or a laminated film with multiple layers formed from Mo, Al or an alloy containing Mo and/or Al, and the gate 102 has a thickness of 100nm ~500nm.

[0035] In the present embodiment, the gate insulating layer 103 may be a laminated film with multiple layers formed from one or two materials selected from silicon oxide (SiOx), silicon nitride (SiNx), hafnium oxide (HfOx), silicon oxynitride (SiON), aluminum oxide (AlOx) and the like. Thickness of the gate insulating layer 103 is controlled to be within 100~600nm, and may be adjusted according to actual condition.

[0036] The active region 104 may be formed from a film containing In (indium), Ga (gallium), Zn (zinc), ○ (oxygen) Sn (tin), etc. through sputtering, and the film must contain oxygen and two or more other elements, for example, indium gallium zinc oxide (IGZO), indium zinc oxide (IZO), indium tin oxide (InSnO), indium gallium tin oxide (InGaSnO), etc. Material of the oxide semiconductor active layer preferably is IGZO or IZO, and thickness thereof preferably is controlled be to within 10~100nm.

[0037] The source and drain 105 may be a single layer or a laminated film with multiple layers formed from one or more materials selected from molybdenum (Mo), molybdenum-niobium alloy (MoNb), aluminum (Al), neodymium-aluminum alloy (AlNd), titanium (Ti) and Copper (Cu), and preferably is a signal layer or a laminated film with multiple layers formed from Mo, Al or an alloy containing Mo and/or Al.

[0038] At step 2, on the substrate 101 subjected to the above step, a pattern including a light filtering layer is formed through a patterning process. Here, the light filtering layer comprises a color filter 107 and a black matrix 106. Specifically, on the substrate 101 on which the thin film transistor has been formed, the black matrix (BM) 106 is formed through processes such as coating, exposure, development, baking and the like, and on the substrate 101 on which the black matrix 106 has been formed, the color filter 107, i.e., color filters 107 of a red, green or blue (RGB) sub-pixel for example, is formed through processes such as coating, exposure, development, baking and the like. In the array substrate, the black matrices 106 and the color filters 107 are provided alternately.

[0039] At step 3, on the substrate 101 subjected to the above steps, a third electrode layer 113 connected to the drain 105 of the thin film transistor and extending onto the light filtering layer is formed through processes such as sputtering, exposure, development, etching, stripping and the like. In this case, the third electrode layer 113 preferably extends onto the color filter 107, or may extend onto the black matrix 106. Specifically, one end of the third electrode layer 113 is connected to the drain 105 of the thin film transistor, and the other end thereof extends onto the color filter 107 or the black matrix 106, and preferably onto an upper surface of the color filter 107 or the black matrix 106. The third electrode layer 113 preferably adopts a conductive material, and generally adopts a metal material, such as copper, aluminium, silver, etc. In a case that the third electrode layer 113 adopts a metal material and said other end thereof extends onto the upper surface of the color filter 107, on the premise that

good electrical connection between the third electrode layer 113 and the pixel electrode can be guaranteed, projection of the third electrode layer 113 on the substrate 101 may be as small as possible, and preferably within the projection of the drain 105 of the thin film transistor on the substrate 101, so as to reduce influence on the aperture ratio. At step 4, on the substrate 101 subjected to the above steps, a planarization layer 108 is formed to eliminate level difference between color filters 107 of different colors and black matrices 106. Here, material of the planarization layer 108 is generally silicon dioxide, silicon nitride, aluminum oxide, etc.

[0040] At step 5, on the substrate 101 subjected to the above steps, a contacting via 109 penetrating through the planarization layer 108 is formed above a portion of the third electrode layer 113 on the light filtering layer. Here, if the third electrode layer 113 extends onto the color filter 107, the contacting via 109 penetrating through the planarization layer 108 is formed above a portion of the third electrode layer 113 on the color filter 107 accordingly; if the third electrode layer 113 extends onto the black matrix 106, the contacting via 109 penetrating through the planarization layer 108 is formed above a portion of the third electrode layer 113 on the black matrix 106 accordingly.

[0041] At step 6, on the substrate 101 subjected to the above steps, a pattern including a pixel electrode is formed through a patterning process, and the pixel electrode is connected to the third electrode layer 113 through the contacting via 109. Here, material of the pixel electrode is preferably indium tin oxide, and of course may also be other transparent conductive material.

[0042] At step 7, on the substrate 101 subjected to the above steps, a passivation layer 111 is formed. Here, material of the passivation layer 111 is generally silicon dioxide, silicon nitride, aluminum oxide, etc.

[0043] At step 8, on the substrate 101 subjected to the above steps, a pattern including a common electrode is formed through a patterning process. Here, material of the common electrode is preferably indium tin oxide, and of course may also be other transparent conductive material. Thus, the array substrate shown in Fig. 2 or 3 is formed.

[0044] It should be noted that, in the above, the pixel electrode is the first electrode layer 110 and the common electrode is the second electrode layer 112 shown in Fig. 2 or 3.

[0045] The drain 105 of the thin film transistor on the array substrate manufactured by using the method provided by the present embodiment is electrically connected to the pixel electrode 110 through the third electrode layer 113 extending onto the light filtering layer, without lengthening the length of the drain 105, and therefore, the aperture ratio of the array substrate will not be affected. In particular, as the third electrode layer 113 extends onto the light filtering layer, only a contacting via 109 that penetrates through the planarization layer 108 on a portion of the third electrode layer 113 on the light filtering layer needs to be formed. The contacting via 109, compared to the contacting via in the prior art, obviously has a shallower depth and a narrower opening width, and as a result, compared to an existing array substrate, the array substrate provided by the present embodiment has an apparently improved aperture ratio.

[0046] Those skilled in the art can understand that, after the array substrate is manufactured, a liquid crystal layer is formed by using a liquid crystal pouring (dropping) device, and then the array substrate is assembled with an opposite substrate (color filter substrate). Detailed description regarding these known operations is omitted herein.

Embodiment 3

[0047] The present embodiment provides a manufacturing method of an array substrate, this method and the method in Embodiment 2 are similar, and only differ in that a pattern including the common electrode is formed through a patterning process after sequentially forming a thin film transistor, a light filtering layer and a planarization layer 108 on the substrate. After the common electrode is formed, the method further includes steps as below.

[0048] A passivation layer 111 is formed on the common electrode, and a contacting via 109 penetrating through the passivation layer 111 and the planarization layer 108 are formed above a portion of the third electrode layer 113 on the light filtering layer. If the third electrode layer 113 extends onto the color filter 107, the contacting via 109 penetrating through the passivation layer 111 and the planarization layer 108 is formed above a portion of the third electrode layer 113 on the color filter 107 accordingly; if the third electrode layer 113 extends onto the black matrix 106, the contacting via 109 penetrating through the passivation layer 111 and the planarization layer 108 is formed above a portion of the third electrode layer 113 on the black matrix 106 accordingly.

[0049] On the substrate subjected to the above steps, a pattern including a pixel electrode is formed through a patterning process, wherein a portion of the third electrode layer 113 is exposed by the contacting via 109 formed in the above step, as shown in Fig. 4. In this case, the pixel electrode is the second electrode layer 112 and the common electrode is the first electrode layer 110.

Embodiment 4

[0050] The present embodiment provides a display device, which comprises the array substrate described in Embodiment 1.

[0051] The display device may be any product or component with a display function, such as a mobile phone, a tablet computer, a television, a display, a notebook computer, a digital photo frame, a navigator or the like.

[0052] The display device of the present embodiment comprises the array substrate in Embodiment 1, and

therefore has better aperture ratio and better visual effect.

[0053] Needless to say, the display device of the present embodiment may also comprise other conventional structures, such as backlight, power unit, display driving unit and the like, which are not elaborated herein.

[0054] It can be understood that, the above implementations are merely exemplary implementations for explaining the principle of the present invention, but the present invention is not limited thereto. For those skilled in the art, various variations and improvements may be made without departing from the scope of the present invention which is defined by the appended claims.

Claims

1. An array substrate comprising: a substrate (101) with a thin film transistor formed thereon; a light filtering layer (106, 107) formed on said substrate (101)and saidthin film transistor, a planarization layer (108) covering the light filtering layer (106, 107), and a pixel electrode layer comprising a pixel electrode (110) and provided above the planarization layer (108), **characterized in that** the array substrate further comprises: an electrode layer (113) connected to a drain (105) of the thin film transistor and extending onto the light filtering layer (106, 107); and
   a contacting via (109) penetrating through the planarization layer (108) and provided above the electrode layer (113), the pixel electrode (110) being connected to the electrode layer (113) through the contacting via (109).

2. The array substrate according to claim 1, wherein the light filtering layer comprises a color filter (107) and a black matrix (106), the pixel electrode (110) is positioned above the color filter (107), the black matrix (106) is at least positioned above the thin film transistor, the color filter (107) and the black matrix (106) are provided alternately on the substrate, and the electrode layer (113) extends onto the color filter (107), or
   the electrode layer (113) extends onto the black matrix (106) .

3. The array substrate according to claim 2, further comprising: a passivation layer (111) and a common electrode (112) sequentially provided on the pixel electrode (110).

4. The array substrate according to claim 2, further comprising: a passivation layer (111) and a common electrode (112) provided between the pixel electrode (110) and the planarization layer (108), wherein, the common electrode (112) and the passivation layer (111) are sequentially provided on the planarization layer (108) and the contacting via (109) penetrates through the planarization layer (108) and the passivation layer (111).

5. The array substrate according to claim 3 or 4, wherein, materials of the pixel electrode (110) and the common electrode (112) are indium tin oxide.

6. A manufacturing method of an array substrate, comprising a step of:

   forming, on a substrate with a thin film transistor formed thereon, a pattern including a light filtering layer through a patterning process;
   characterized in that, the manufacturing method further comprises steps of:

      forming, on the substrate subjected to the above step, a electrode layer (113) connected to a drain (105) of the thin film transistor and extending onto the light filtering layer through a patterning process;
      forming, on the substrate subjected to the above steps, a planarization layer (108), and forming a contacting via (109) penetrating through the planarization layer (108) above a portion of the electrode layer (113) on the light filtering layer; and
      forming, on the substrate subjected to the above steps, a pattern including a pixel electrode (110) through a patterning process, wherein the pixel electrode (110) is connected to the electrode layer (113) through the contacting via (109) penetrating through the planarization layer (108).

7. The manufacturing method of an array substrate according to claim 6, wherein the light filtering layer comprises a color filter (107) and a black matrix (106), the pixel electrode (110) is formed above the color filter (107), the black matrix (106) is at least formed above the thin film transistor, the color filter (107) and the black matrix (106) are provided alternately on the substrate, and
   the electrode layer (113) extends onto the color filter (107), or
   the electrode layer (113) extends onto the black matrix (106) .

8. The manufacturing method of an array substrate according to claim 7, further comprising steps of:

   forming a passivation layer (111) on the pixel electrode (110); and
   forming, on the passivation layer (111), a pattern including a common electrode (112) through a patterning process.

9. The manufacturing method of an array substrate ac-

cording to claim 7, wherein after forming the planarization layer (108) and before forming, above a portion of the electrode layer (113) on the light filtering layer, the contacting via (109) penetrating through the planarization layer (108), the manufacturing method further comprises steps of:

forming, on the planarization layer (108), a pattern including a common electrode (112) through a patterning process; and
forming a passivation layer (111) on the common electrode (112),
wherein the contacting via (109) penetrating through the planarization layer (108) and formed above a portion of the electrode layer (113) on the light filtering layer also penetrates through the passivation layer (111).

10. A display device, **characterized in that**, the display device comprises the array substrate according to any one of claims 1 to 5.

Patentansprüche

1. Arraysubstrat, umfassend: ein Substrat (101) mit einem darauf ausgebildeten Dünnfilmtransistor; eine Lichtfilterschicht (106, 107), die auf dem Substrat (101) und dem Dünnfilmtransistor ausgebildet ist, wobei eine Planarisierungsschicht (108) die Lichtfilterschicht (106, 107) bedeckt, und eine Pixelelektrodenschicht eine Pixelelektrode (110) umfasst und über der Planarisierungsschicht (108) bereitgestellt ist, **dadurch gekennzeichnet, dass** das Arraysubstrat ferner umfasst: eine Elektrodenschicht (113), die mit einem Drain (105) des Dünnfilmtransistors verbunden ist und sich auf die Lichtfilterschicht (106, 107) erstreckt; und
eine Durchkontaktierung (109), die die Planarisierungsschicht (108) durchdringt und über der Elektrodenschicht (113) bereitgestellt ist, wobei die Pixelelektrode (110) durch die Durchkontaktierung (109) mit der Elektrodenschicht (113) verbunden ist.

2. Arraysubstrat nach Anspruch 1, wobei die Lichtfilterschicht einen Farbfilter (107) und eine Schwarzmatrix (106) umfasst, wobei die Pixelelektrode (110) über dem Farbfilter (107) angeordnet ist, die Schwarzmatrix (106) mindestens über dem Dünnfilmtransistor angeordnet ist, der Farbfilter (107) und die Schwarzmatrix (106) abwechselnd auf dem Substrat bereitgestellt sind, und
die Elektrodenschicht (113) sich auf den Farbfilter (107) erstreckt, oder
die Elektrodenschicht (113) sich auf die Schwarzmatrix (106) erstreckt.

3. Arraysubstrat nach Anspruch 2, ferner umfassend:

eine Passivierungsschicht (111) und eine gemeinsame Elektrode (112), die auf der Pixelelektrode (110) sequenziell bereitgestellt sind.

4. Arraysubstrat nach Anspruch 2, ferner umfassend:

eine Passivierungsschicht (111) und eine gemeinsame Elektrode (112), die zwischen der Pixelelektrode (110) und der Planarisierungsschicht (108) bereitgestellt sind, wobei die gemeinsame Elektrode (112) und die Passivierungsschicht (111) sequenziell auf der Planarisierungsschicht (108) bereitgestellt sind und die Durchkontaktierung (109) die Planarisierungsschicht (108) und die Passivierungsschicht (111) durchdringt.

5. Arraysubstrat nach Anspruch 3 oder 4, wobei es sich bei den Materialien der Pixelelektrode (110) und der gemeinsamen Elektrode (112) um Indiumzinnoxid handelt.

6. Herstellungsverfahren für ein Arraysubstrat, das folgenden Schritt umfasst:

Ausbilden, auf einem Substrat mit einem darauf ausgebildeten Dünnfilmtransistor, einer Struktur, die eine Lichtfilterschicht beinhaltet, mittels eines Strukturierungsverfahrens;
dadurch gekennzeichnet, dass das Herstellungsverfahren ferner folgende Schritte umfasst:

Ausbilden, auf dem Substrat, das dem vorstehend genannten Schritt unterzogen wurde, einer Elektrodenschicht (113), die mit einem Drain (105) der Dünnfilmtransistors verbunden ist und sich auf die Lichtfilterschicht erstreckt, mittels eines Strukturierungsverfahrens;
Ausbilden, auf dem Substrat, das den vorstehend genannten Schritten unterzogen wurde, einer Planarisierungsschicht (108) und Ausbilden einer Durchkontaktierung (109), die die Planarisierungsschicht (108) durchdringt, über einen Abschnitt der Elektrodenschicht (113) auf der Lichtfilterschicht; und
Ausbilden, auf dem Substrat, das den vorstehend genannten Schritten unterzogen wurde, einer Struktur, die eine Pixelelektrode (110) beinhaltet, mittels eines Strukturierungsverfahrens, wobei die Pixelelektrode (110) durch die Durchkontaktierung (109), die die Planarisierungsschicht (108) durchdringt, mit der Elektrodenschicht (113) verbunden ist.

7. Herstellungsverfahren für ein Arraysubstrat nach Anspruch 6, wobei die Lichtfilterschicht einen Farbfilter (107) und eine Schwarzmatrix (106) umfasst, wobei die Pixelelektrode (110) über dem Farbfilter (107) ausgebildet ist, die Schwarzmatrix (106) mindestens über dem Dünnfilmtransistor ausgebildet ist, der Farbfilter (107) und die Schwarzmatrix (106) abwechselnd auf dem Substrat bereitgestellt sind, und
die Elektrodenschicht (113) sich auf den Farbfilter (107) erstreckt, oder
die Elektrodenschicht (113) sich auf die Schwarzmatrix (106) erstreckt.

8. Herstellungsverfahren für ein Arraysubstrat nach Anspruch 7, das ferner folgende Schritte umfasst:

Ausbilden einer Passivierungsschicht (111) auf der Pixelelektrode (110); und
Ausbilden, auf der Passivierungsschicht (111), einer Struktur, die eine gemeinsame Elektrode (112) beinhaltet, mittels eines Strukturierungsverfahrens.

9. Herstellungsverfahren für ein Arraysubstrat nach Anspruch 7, wobei das Herstellungsverfahren, nach Ausbilden der Planarisierungsschicht (108) und vor Ausbilden, über einem Abschnitt der Elektrodenschicht (113) auf der Lichtfilterschicht, der Durchkontaktierung (109), die die Planarisierungsschicht (108) durchdringt, ferner folgende Schritte umfasst:

Ausbilden, auf der Planarisierungsschicht (108), einer Struktur, die eine gemeinsame Elektrode (112) beinhaltet, mittels eines Strukturierungsverfahrens; und
Ausbilden einer Passivierungsschicht (111) auf der gemeinsamen Elektrode (112),
wobei die Durchkontaktierung (109) die Planarisierungsschicht (108) durchdringt und über einem Abschnitt der Elektrodenschicht (113) auf der Lichtfilterschicht ausgebildet ist, auch die Passivierungsschicht (111) durchdringt.

10. Anzeigevorrichtung, **dadurch gekennzeichnet, dass** die Anzeigevorrichtung das Arraysubstrat nach einem der Ansprüche 1 bis 5 umfasst.

Revendications

1. Substrat de réseau comprenant : un substrat (101) comportant un transistor à couches minces formé sur ledit substrat ; une couche de filtration de la lumière (101, 107) formée sur ledit substrat (101) et sur ledit transistor à couches minces, comprenant une couche de planarisation (108) couvrant la couche de filtration de la lumière (106, 107), et une couche d'électrode de pixel comprenant une électrode de pixel (110) et prévue au-dessus de la couche de planarisation (108),
caractérisé en ce que le support de réseau comprend en outre : une couche d'électrode (113) connectée à un drain (105) du transistor à couches minces et s'étendant sur la couche de filtration de la lumière (106, 107) ; et comprend un trou d'interconnexion (109) traversant la couche de planarisation (108) et prévu au-dessus de la couche d'électrode (113), l'électrode de pixel (110) étant connectée à la couche d'électrode (113) grâce au trou d'interconnexion (109).

2. Substrat de réseau selon la revendication 1, dans lequel la couche de filtration de la lumière comprend un filtre coloré (107) et une matrice noire (106), où l'électrode de pixel (110) est positionnée au-dessus du filtre coloré (107), où la matrice noire (106) est positionnée au moins au-dessus du film à couches minces, le filtre coloré (107) et la matrice noire (106) étant prévus de façon alternée sur le substrat, et la couche d'électrode (113) s'étend sur le filtre coloré (107), ou bien la couche d'électrode (113) s'étend sur la matrice noire (106).

3. Substrat de réseau selon la revendication 2, comprenant en outre : une couche de passivation (111) et une électrode commune (112) prévues successivement sur l'électrode de pixel (110).

4. Substrat de réseau selon la revendication 2, comprenant en outre : une couche de passivation (111) et une électrode commune (112) prévues entre l'électrode de pixel (110) et la couche de planarisation (108), où l'électrode commune (112) et la couche de passivation (111) sont prévues successivement sur la couche de planarisation (108), et le trou d'interconnexion (109) traverse la couche de planarisation (108) et traverse la couche de passivation (111).

5. Substrat de réseau selon la revendication 3 ou 4, dans lequel des matériaux de l'électrode de pixel (110) et de l'électrode commune (112) sont de l'oxyde d'étain et d'indium.

6. Procédé de fabrication d'un substrat de réseau, comprenant l'étape consistant :

à former, sur un substrat comprenant un transistor à couches minces formé sur ledit substrat, un motif comprenant une couche de filtration de la lumière, ladite couche étant réalisée grâce à un processus de formation des motifs ;
caractérisé en ce que le procédé de fabrication comprend en outre des étapes consistant :

à former, sur le substrat soumis à l'étape mentionnée précédemment, une couche d'électrode (113) connectée à un drain (105) du transistor à couches minces et s'étendant sur la couche de filtration de la lumière, ladite couche étant réalisée grâce à un processus de formation des motifs ;
à former, sur le substrat soumis aux étapes mentionnées précédemment, une couche de planarisation (108), et à former un trou d'interconnexion (109) traversant la couche de planarisation (108) située au-dessus d'une partie de la couche d'électrode (113) placée sur la couche de filtration de la lumière ; et
à former, sur le substrat soumis aux étapes mentionnées précédemment, un motif comprenant une électrode de pixel (110) réalisée grâce à un processus de formation des motifs, où l'électrode de pixel (110) est connectée à la couche d'électrode (113) grâce" au trou d'interconnexion (109) traversant la couche de planarisation (108).

7. Procédé de fabrication d'un substrat de réseau selon la revendication 6, dans lequel la couche de filtration de la lumière comprend un filtre coloré (107) et une matrice noire (106), où l'électrode de pixel (110) est formée au-dessus du filtre coloré (107), où la matrice noire (106) est au moins formée au-dessus du transistor à couches minces, le filtre coloré (107) et la matrice noire (106) étant prévus de manière alternée sur le substrat, et la couché d'électrode (113) s'étend sur le filtre coloré (107), ou bien la couche d'électrode (113) s'étend sur la matrice noire (106).

8. Procédé de fabrication d'un substrat de réseau selon la revendication 7, comprenant en outre les étapes consistant :

à former une couche de passivation (111) sur l'électrode de pixel (110) ; et
à former, sur la couche de passivation (111), un motif comprenant une électrode commune (112) réalisée grâce à un processus de formation des motifs.

9. Procédé de fabrication d'un substrat de réseau selon la revendication 7, dans lequel, après formation de la couche de planarisation (108), et avant formation, au-dessus d'une partie de la couche d'électrode (113) placée sur la couche de filtration de la lumière, du trou d'interconnexion (109) traversant la couche de planarisation (108), le procédé de fabrication comprend en outre des étapes consistant :

à former, sur la couche de planarisation (108), un motif comprenant une électrode commune (112) réalisée grâce à un processus de formation des motifs ; et
à former une couche de passivation (111) sur l'électrode commune (112),
procédé dans lequel le trou d'interconnexion (109), qui traverse la couche de planarisation (108) et est formé au-dessus d'une partie de la couche d'électrode (113) placée sur la couche de filtration de la lumière, traverse également la couche de passivation (111).

10. Dispositif de visualisation, **caractérisé en ce que** ledit dispositif de visualisation comprend le substrat de réseau selon l'une quelconque des revendications 1 à 5.

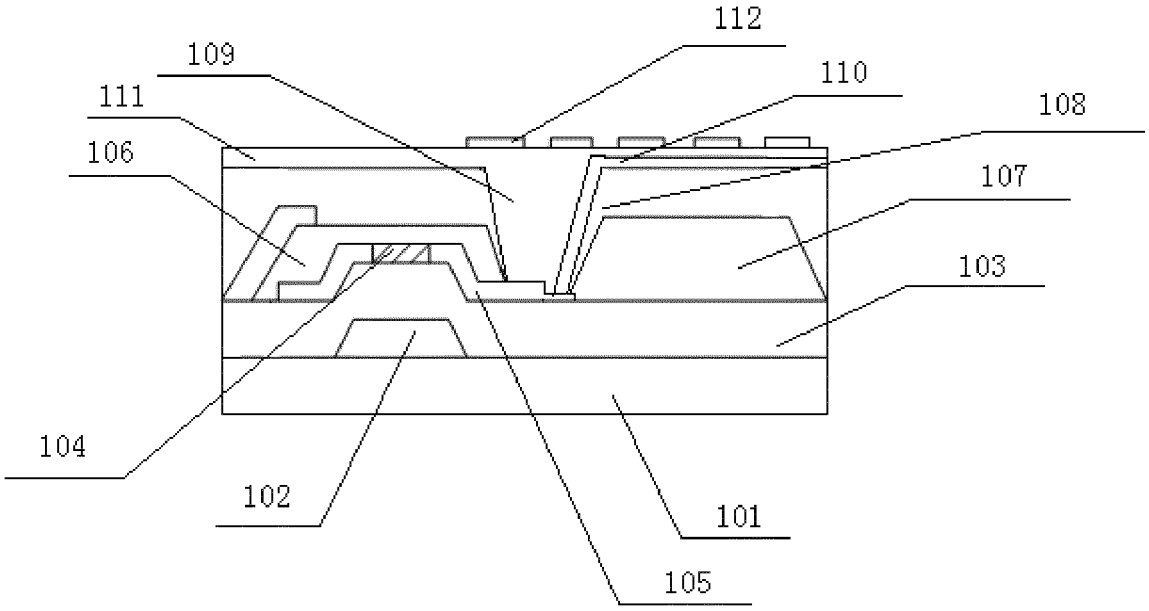
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Fig. 1

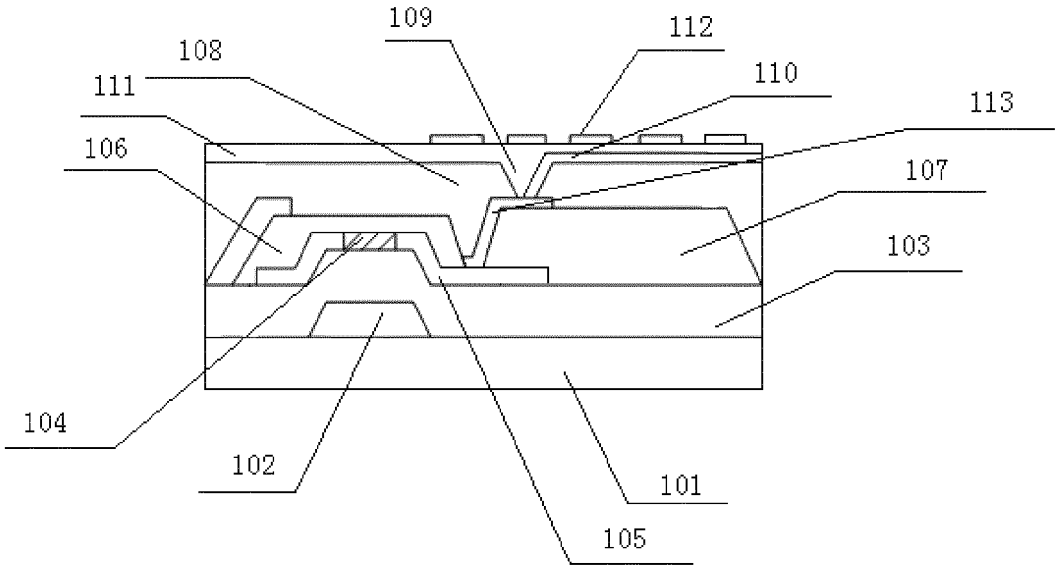
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Fig. 2

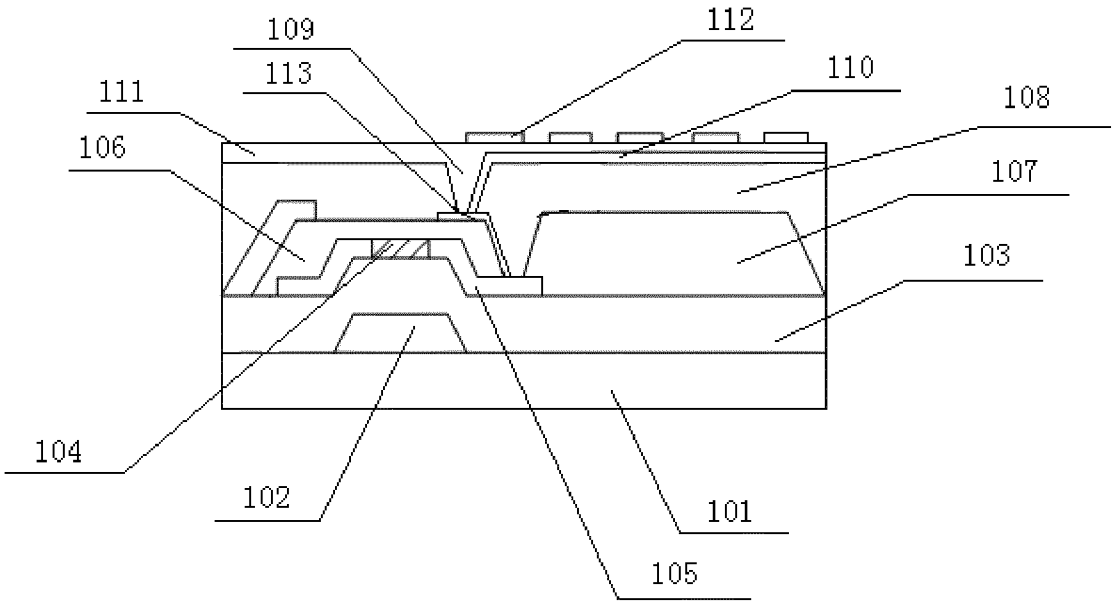
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Fig. 3

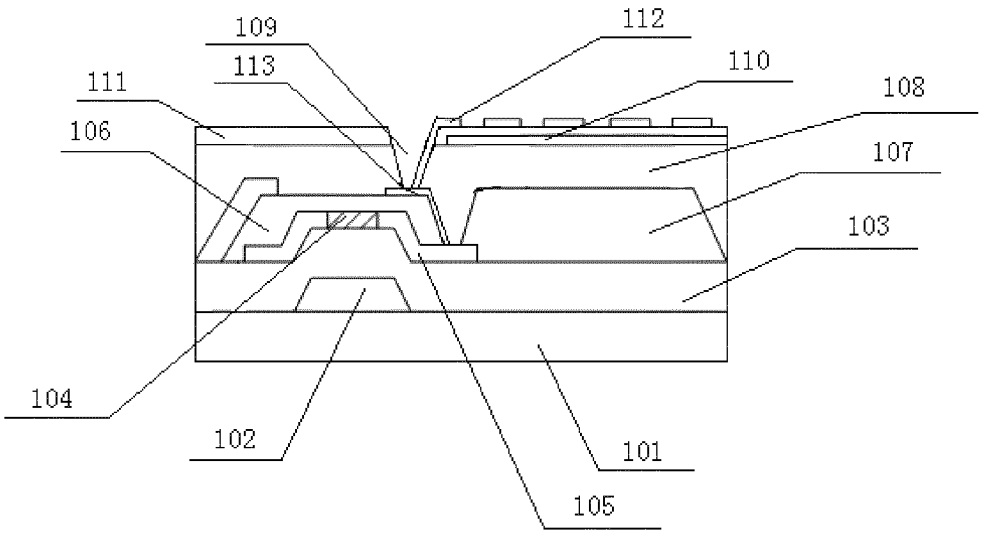
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Fig. 4

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- KR 20130054772 A **[0004]**
- CN 103309081 A **[0005]**

专利名称(译)	阵列基板，其制备方法和显示装置		
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代理机构(译)	COHAUSZ & FLORACK		
优先权	201310706543.0 2013-12-19 CN		
其他公开文献	EP2919266A4 EP2919266A1		
外部链接	Espacenet		

摘要(译)

本发明提供一种阵列基板及其制作方法和显示装置，涉及液晶显示技术领域，可以解决现有阵列基板的开口率低的问题。本发明的阵列基板包括：滤光层，设置在基板上，形成于其上的薄膜晶体管;覆盖所述滤光层的平坦化层;以及设置在所述平坦化层上方的像素电极，所述阵列基板还包括：a第三电极层连接到薄膜晶体管的漏极并延伸到滤光层上;接触通孔穿过平坦化层并设置在滤光层上的第三电极层的一部分上方，像素电极通过接触通孔连接到第三电极层。

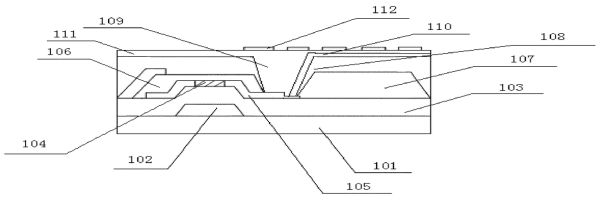

Fig. 1

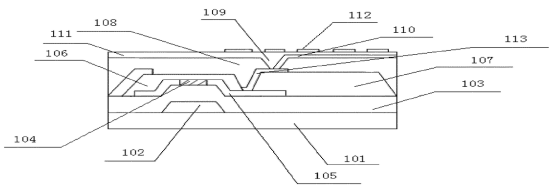

Fig. 2