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(54) ARRAY SUBSTRATE, LIQUID CRYSTAL DISPLAY AND DRIVING METHOD THEREOF

(57) An array substrate, a liquid crystal display and a control method thereof are disclosed according to the invention. The array substrate includes: multiple scanning lines; multiple data lines; multiple pixel units; multiple common lines, where each of the common lines is disposed along a row of pixel units; a common voltage supply line; multiple dual-channel selection switches, where an output terminal of each of the dual-channel selection switches is connected to a set of common lines, two input terminals are connected to a common voltage high level supply line and a common voltage low level supply line respectively, so as to selectively apply a high level or a low level to the common lines. The control method includes: supplying power to a common line corresponding to a scanning line before providing a scanning signal to the scanning line, and maintaining the potential of the common line unchanged during displaying a frame of picture; and inverting the potentials applied to the common line during scanning for a next frame. The embodiments of the invention avoid the problems of the delay of the common voltage Vcom and the Vcom drift during displaying, and improve the displaying effect for an image.

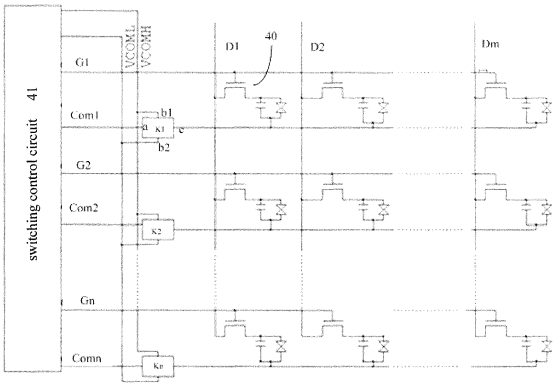

FIG. 4

EP 2 874 002 A1

Description

[0001] This application claims the priority of Chinese Patent Application No. 201210244083.X, entitled "ARRAY SUBSTRATE, LIQUID CRYSTAL DISPLAY AND CONTROL METHOD THEREOF", filed with State Intellectual Property Office of People's Republic of China on July 13, 2012, which is incorporated herein by reference in its entirety.

FIELD OF THE INVENTION

[0002] The invention relates to the field of liquid crystal display, and in particular to an array substrate, a liquid crystal display and a control method thereof.

BACKGROUND OF THE INVENTION

[0003] A Liquid Crystal Display (LCD) is a widely used flat-panel display. The LCD relatively widely applied in the prior art is the Thin Film Transistor Liquid Crystal Display (simply referred to as TFT-LCD). A Thin Film Transistor (TFT) includes an amorphous-Silicon Thin Film Transistor (a-Si TFT) and a Poly-Silicon Thin Film Transistor (Poly-Si TFT). Furthermore, the Poly-Silicon Thin Film Transistors includes Low Temperature Polysilicon (simply referred to as LTPS) TFT-LCDs and High Temperature Poly-silicon (simply referred to as HTPS) TFT-LCDs. Specifically, the so-called TFT-LCDs in the prior art refer to the a-Si TFT-LCDs. The circuit diagram of the internal structure of the TFT-LCD is shown in Figure 1, and the structure will be described as follows.

[0004] Multiple scanning lines S1 to Sm parallel to one another and multiple data lines D1 to Dn parallel to one another are disposed on the array substrate of the TFT-LCD. The scanning lines are arranged to intersect with the data lines and pixel units 110 are disposed at the intersections of the scanning lines and the data lines to form a pixel unit array. The pixel unit 110 includes a transistor 112 of which the gate is connected to a corresponding scanning line, the source of the transistor 112 is connected to a corresponding data line and the drain of the transistor 112 is coupled to a common voltage Vcom via a pixel element 114. Specifically, a storage capacitor 116 is generally also connected across the pixel element 114 to stabilize the voltage across the pixel element 114.

[0005] When an image is displayed by the TFT-LCD, a scanning signal is needed to be transmitted to the scanning lines so as to turn on a transistor connected to each of the scanning lines. Then a data signal is sequentially input to the pixel units 110, and the storage capacitor 116 will be charged upon the data signal is transmitted from the source to the drain of transistor 112. Meanwhile, the common voltage Vcom is applied to the other end of the pixel element 114, since Vcom is different from the voltage of the drain of the transistor, the voltage difference is formed between the two ends of the pixel element 114, and thus the pixel element 114 is lightened.

[0006] On the array substrate of the TFT-LCD, the common voltage is applied to the whole substrate, therefore, when one pixel unit is driven, it is needed to apply the common voltage to the whole substrate simultaneously. That is, the load driven by the common voltage Vcom may be all the pixel units on the array substrate, causing the problem that the driving ability of the common voltage Vcom is not sufficient.

[0007] In order to solve the problem, the solution according to the prior art is shown in Figure 2. One common line is disposed for each row of pixel units, and a common voltage is applied to the pixel units via the common line. The common line is connected to a corresponding scanning line via a transistor 21. Here, the gate of the transistor 21 is connected to the corresponding scanning line, and the drain of the transistor 21 is connected to the common line, and the sources of all the transistors 21 on the array substrate are all connected to a terminal from which the common voltage is supplied.

[0008] During displaying an image, transistors within a row of pixel units and the transistor 21 connected to the corresponding common line are turned on simultaneously by a scanning signal, thus the common voltage is applied to the pixel units row by row, the load for the common voltage is reduced and the driving ability of Vcom is improved.

[0009] However, adopting this design will affect the quality of displaying due to the excessively short charging time of the pixel far away from a common voltage signal inputting end which is caused by the RC delay; and since a common electrode line is electrified only when the row of scanning line is turned on, the common electrode line is in a dangling state at other times, it will be affected by any disturbance and thus the quality of displaying will be deteriorated.

SUMMARY OF THE INVENTION

[0010] In view of the above, the object of the present invention is to provide an array substrate, a liquid crystal display and a control method thereof. The problems of the delay of the common voltage Vcom and the Vcom drift during the displaying in the prior art are solved, and the displaying effect of an image is improved.

[0011] In order to achieve the above object, the following technical solutions are provided according to embodiments of the present invention.

[0012] An array substrate, including: a plurality of scanning lines parallel to each other in a first direction; a plurality of data lines parallel to each other in a second direction, where the first direction intersects with the second direction; a plurality of pixel units disposed at intersections of the scanning lines and the data lines; a plurality of common lines, each common line arranged along a row of pixel units and electrically connected thereto; a common voltage supply line having a common voltage high level supply line and a common voltage low level supply line; and a plurality of dual-channel selection

switches, each dual-channel selection switch comprising a control terminal, two input terminals and a output terminal, wherein the output terminal of each of the dual-channel selection switches is connected to a set of common lines, wherein the two input terminals of the dual-channel selection switch are connected to the common voltage high level supply line and the common voltage low level supply line respectively, wherein a high level or a low level is selectively applied to the common lines in response to a control signal of the control terminal of the dual-channel selection switch, and

wherein the number of the common lines comprised in the set of common lines is less than the number of the common lines comprised in the array substrate.

[0013] Preferably, the common voltage supply line includes a first common voltage supply line and a second common voltage supply line, each of which includes a first common voltage supply line and a second common voltage supply line, each of first and second common voltage supply lines comprising a common voltage high level supply line and a common voltage low level supply line; and the first common voltage supply line being connected to an end of the common line through a dual-channel selection switch, and the second common voltage supply line is connected to the other end the common line through a dual-channel selection switch.

[0014] Preferably, the control signal is a clock signal.

[0015] Preferably, the set of common lines includes only one common line.

[0016] According to the an embodiment of the present invention, it is disclosed a liquid crystal display, which includes: the array substrate described above, a color film substrate disposed opposite to the array substrate; a liquid crystal layer disposed between the array substrate and the color film substrate; a gate driving circuit connected to the scanning lines and configured to transmit scanning signals through the scanning lines; a source driving circuit connected to the data lines and configured to transmit image data through the data lines; a control circuit coupled to the gate driving circuit and the source driving circuit and configured to control a normal operation of the gate driving circuit and the source driving circuit; and a switching control circuit connected to control terminals of the dual-channel selection switches, and configured to control connecting lines of the dual-channel selection switches and selectively apply a high level or a low level to the common lines through outputting a control signal.

[0017] Preferably, the switching control circuit is integrated with the gate driving circuit, the source driving circuit, or the control circuit.

[0018] Preferably, the pixel unit may include: a transistor having a gate connected to the scanning line and a source connected to the data line; a pixel element having an end connected to the drain of the transistor and an opposite end connected to the common line; and a storage capacitor connected across the pixel element.

[0019] Preferably, the pixel unit may include: a first transistor having a gate connected to the scanning line and a source connected to the data line; a second transistor having a the gate coupled to the gate of the first transistor and a source coupled to the drain of the first transistor; a pixel element having an end connected to the drain of the second transistor and an opposite end connected to the common line; and a storage capacitor connected across the pixel element.

[0020] Preferably, the transistor is an amorphous-silicon thin film transistor, a low temperature poly-silicon thin film transistor, or a high temperature poly-silicon thin film transistor.

[0021] A control method is disclosed according to an embodiment of the invention, applied to the liquid crystal display described above and including: supplying power to a common line corresponding to a scanning line before providing a scanning signal to the scanning line, wherein the pixel units connected to the scanning line have a common potential in the case where a scanning signal is provided to the scanning line; maintaining a potential of the common line unchanged during display of a frame of picture; and inverting a potential applied to the common line during scanning for a next frame.

[0022] Preferably, the array substrate of the liquid crystal display is provided with n scanning lines and n common lines, and during display of a frame of picture, wherein a supplying power onset timing for an n-th common line is one of the supplying power onset timings for an (n-4)-th scanning line to the (n-1)-th scanning line.

[0023] Preferably, the n-th common line and the (n-1)-th scanning line are supplied with power concurrently.

[0024] Preferably, the potentials of two common lines adjacent to each other are opposite to each other during display of a frame of picture.

[0025] Preferably, the supplying power for the common lines includes: connecting the two ends of the common line to a same potential supply line of the first common voltage supply line and the second common voltage supply line through two dual-channel selection switches located at the two ends of the common line; and concurrently supplying a power of the first common supply line and the second common voltage supply line to the common line.

[0026] Compared with the prior art, the solutions according to an embodiment of the invention have the following advantages.

[0027] The array substrate and liquid crystal display according to the embodiments of the invention provide the structural basis for the control process of the liquid crystal display. The potentials of common lines can be controlled separately via a dual-channel selection switch, and during displaying, a common line corresponding to a scanning line is supplied with power in advance, such that pixel units connected to the scanning line already have a common potential when the scanning signal is provided to the scanning line. Therefore each pixel element of the row of pixel elements can form a potential difference across the pixel element immediately after a

corresponding transistor is turned on, such that the poor displaying effect due to the delay of the common potential is avoided.

[0028] Furthermore, since the potentials of each row of common lines are maintained unchanged during displaying a frame of picture, that is, during the displaying, each of the common lines is not in a floating state, thus the crosstalk among the common lines is avoided and the stability of the common voltage during the displaying is guaranteed. Meanwhile, since the potentials of the common lines are inverted with the refresh frequency of the pictures during the displaying, the problem of liquid crystal aging caused if the liquid crystal is controlled in the same potential for a long time is avoided, and the normal displaying of the display is further guaranteed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0029]

Figure 1 is an equivalent circuit diagram of a liquid crystal display in the prior art;

Figure 2 is an equivalent circuit diagram of another liquid crystal display in the prior art;

Figure 3 is an equivalent circuit diagram of a pixel unit in the prior art;

Figure 4 is an equivalent circuit diagram of a liquid crystal display according to an embodiment of the present invention;

Figure 5 is an equivalent circuit diagram of a liquid crystal display according to another embodiment of the present invention;

Figure 6 is an equivalent circuit diagram of a pixel unit in a liquid crystal display according to an embodiment of the present invention;

Figure 7 is an equivalent circuit diagram of a pixel unit in a liquid crystal display according to another embodiment of the present invention; and

Figure 8 and Figure 9 are schematic diagrams of power supply modes of the common line during the displaying of two adjacent frames in a control method for a liquid crystal display according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0030] In order to make objects, technical solutions and advantages of embodiments of the invention to be clearer, in the following the technical solutions according to the embodiments of the invention will be clearly and fully described in conjunction with the drawings. Apparently, the embodiments to be described are only some of the embodiments of the invention but not all the embodiments of the invention. Any other embodiments obtained by the skilled in the art based on the embodiments of the invention without inventive works fall within the protective scope of the invention.

[0031] As described in the background of the present invention, the displaying effect of the liquid crystal display (LCD) in the prior art is poor. The inventors research and find that the main reason is in that there exist delay and voltage drift during Vcom in the prior art driving a row of pixel units. It will be described further below in conjunction with Figure 2 and Figure 3, and Figure 3 is an internal circuit diagram of a pixel unit in Figure 2.

[0032] After a scanning signal is input to the (Gm-1)-th scanning line, the transistors 301 and 214 are turned on simultaneously, and a data signal is input to the transistor 301 via the data line D1. After the transistor 301 is turned on, a first potential is applied on one end of a pixel element 303 after a short signal transmission. After the transistor 214 is turned on, a common voltage is applied to the source of the transistor 214 from the Vcom providing terminal, and then the common voltage is transmitted to the other end of the pixel element 303 via a transmission line, thus a voltage difference is formed between the two ends of the pixel element 303. During the transmission of the signal, although both of the data signal and the common voltage need to pass through a transistor, the common voltage needs to be transmitted to the whole row of the common lines shown in Figure 2 as the common voltage passes the transistor 214, but the transistor 301 only needs to transmit the data signal to the inside of the pixel unit in which the transistor 301 is located. That is, the load driven by the transistor 214 is much larger than the transistor 301. Therefore the speed at which the signal is transmitted on the common line is inevitably slower than the speed at which the signal is transmitted inside the pixel unit, causing a delay of the signal on the common line and thus a delay in the displaying of the pixel unit 303.

[0033] In another aspect, since the turn-on and turn-off of the transistor 214 are also controlled by a scanning signal, that is, after a row of scanning signals are turned off, a corresponding common line will be in a floating state and easy to be disturbed by the external environment such as capacity coupling; or if a voltage is applied to other rows of scanning lines and the common lines, the common line in the floating state is easy to be affected, thus the displaying effect is affected.

[0034] Based on this, an array substrate is disclosed according to an embodiment of the present invention. The array substrate includes: multiple scanning lines parallel to one another in a first direction; multiple data lines parallel to one another in a second direction, where the first direction intersects with the second direction, generally, the first direction is substantially vertical to the second direction; multiple pixel units disposed at intersections of the scanning lines and the data lines; multiple

common lines, each of which is disposed along and electrically connected to a row of pixel units, that is, each of which is electrically connected to one corresponding row of pixel units; a common voltage supply line including a common voltage high level supply line and a common voltage low level supply line; multiple dual-channel selection switches, each of which includes one control terminal, two input terminals and one output terminal, where the output terminal of each of the dual-channel selection switches is connected to a set of common lines, the two input terminals of the dual-channel selection switch are connected to the common voltage high level supply line and the common voltage low level supply line respectively, such that a high level or a low level is selectively applied to a common line through a control signal input from the control terminal, and the number of the common lines included in the set of common lines is less than the number of the common lines included in the array substrate.

[0035] Based on this array substrate, a liquid crystal display with the array substrate described above is further disclosed according to an embodiment of the present invention. The display further includes: a color film substrate disposed opposite to the array substrate and a liquid crystal layer disposed between the array substrate and the color film substrate; a gate driving circuit which is connected to the multiple scanning lines and transmits multiple scanning signals through the multiple scanning lines; a source driving circuit which is connected to the multiple data lines and transmits multiple pieces of image data through the multiple data lines; a control circuit which is coupled to the gate driving circuit and the source driving circuit and controls the normal operations of the gate driving circuit and the source driving circuit; a switching control circuit which is connected to the control terminals of the multiple dual-channel selection switches, controls the connecting lines of the multiple dual-channel selection switches and selectively applies a high level or a low level to the common lines through outputting a control signal.

[0036] Based on the above-described structure, a control method for the above-described LCD is further disclosed according to an embodiment of the present invention. The method includes: supplying power to a common line corresponding to a scanning line before providing a scanning signal to the scanning line, such that the pixel units connected to the scanning line have a common potential if the scanning signal is provided to the scanning line, and maintaining the common potential unchanged during displaying a frame of picture; inverting the potential applied to the common line during scanning for a next frame.

[0037] According to an embodiment of the present invention, the common line corresponding to a scanning line is supplied with power before a scanning signal is provided to the scanning line, such that the pixel units connected to the scanning line already have a common potential if the scanning signal is provided to the scanning line. Therefore each pixel element in the row of pixel elements can form a potential difference across the pixel element immediately after a transistor corresponding to the pixel element is turned on, so as to avoid a poor displaying effect due to the delay of the common potential.

[0038] Furthermore, since the potentials of individual common lines are maintained unchanged during displaying a frame of picture, that is, each of the common lines is not in a floating state during the whole displaying, the crosstalk among the common lines is avoided and the stability of the common voltage during the displaying is guaranteed. Meanwhile, since the potentials of the common lines inverts with the refreshing frequency of the pictures during the displaying, the problem of liquid crystal aging caused if the liquid crystal is controlled in the same potential for a long time is avoided, and the normal displaying of the display is further guaranteed.

[0039] The above descriptions are core ideas of the present invention. In the following the technical solutions according to embodiments of the present invention will be clearly, fully described in conjunction with the appended drawings of the embodiments. Apparently, the described embodiments are only some of but not all the embodiments of the present invention. All other embodiments obtained by the skilled in the art based on the embodiments of the present invention without an inventive work fall within the protection scope of the present invention.

[0040] A circuit diagram of an array substrate disclosed according to an embodiment of the present invention is shown in Figure 4. In this embodiment, the circuit diagram of the array substrate according to the embodiment of the present invention will be explained by only taking an array substrate driven by a single gate as an example. The array substrate includes:

multiple scanning lines G1 to Gn parallel to one another in a first direction, multiple data lines D1 to Dm parallel to one another in a second direction, where the first direction is substantially vertical to the second direction; multiple pixel units 40 disposed at intersections of the scanning lines and the data lines; multiple common lines Com1 to Comn disposed along the pixel units, where one common line is disposed along a row of pixel units, and for the array substrate driven by a single gate, that is, one common line is disposed along one scanning line; a common voltage supply line including a common voltage high level supply line VcomH and a common voltage low level supply line VcomL, both of which supply a common voltage to the common lines of the entire substrate;

multiple dual-channel selection switches K1 to Kn, each of which includes one control terminal "a", two input terminals being "a" first input terminal "b1" and a second input terminal "b2" respectively, and one output terminal "c", where the output terminal "c" of each of dual-channel selection switches is connect-

ed to a set of common lines, and the two input terminals "b1" and "b2" being connected to the common voltage high level supply line VcomH and the common voltage low level supply line VcomL respectively, such that a high level or a low level is selectively input to the common line through a control signal input from the control terminal "a". The control signal is preferably a clock signal in this embodiment, and the common lines are connected to different lines at different time.

[0041] It is to be noted that a set of common lines connected to a same dual-channel selection switch includes at least one common line, and the number of the common lines in the set of common lines is less than the number of the common lines included in the array substrate. Specifically, if a set of common lines include only one common line, the connecting way in this case is shown in Figure 4; and if a set of common lines include at least two common lines, that is, at least two common lines are connected to a same dual-channel selection switch, on this case, the common lines connected to the same dual-channel selection switch may be multiple common lines adjacent to one another, may also be common lines that are not adjacent to one another, or may include common lines adjacent to one another and common lines alternate with each other.

[0042] Taking two common lines being connected to a same dual-channel selection switch K1 as an example. If the common lines adjacent to one another are connected to K1, the two common lines connected to K1 may be Com1 and Com2, else if the common lines that are alternate with each other and are connected to K1, the two common lines connected to K1 maybe Com1 and Com3.

[0043] Preferably, the common lines included in a set of common lines are not adjacent to one another in this embodiment. More preferably, the number of the common lines included in a set of common lines is not greater than 4. More preferably, a set of common lines includes only one common line. The following embodiments will be explained by only taking one common line being connected to one dual-channel selection switch as an example.

[0044] If one common line is connected to one dual-channel selection switch, the dual-channel selection switch K1 is taken as an example. The first input terminal "b"1 of K1 is connected to VcomH, the second input terminal "b2" of K1 is connected to VcomL, the output terminal "c" of K1 is connected to Com1, and the control terminal "a" of K1 is connected to the switching control circuit 41 which may transmit a clock signal. The switching control circuit may be integrated with the gate driving circuit, may also be integrated with the source driving circuit, or may be integrated with a control circuit of the entire array substrate which is generally manufactured on a control chip. In Figure 4, the explanation is performed by only taking the switching control circuit 41 being integrated with the gate driving circuit as an example.

[0045] As shown in Figure 5, according to other embodiments of the present invention, in order to further improve the driving capability of the common voltage, the common voltage supply lines are provided on both ends of a row of pixels, that is, the common voltage supply line includes a first common voltage supply lines 51 and a second common voltage supply lines 52 respectively, and each of them includes a common voltage high level supply line VcomH and a common voltage low level supply line VcomL. Herein, the first common voltage supply line 51 is connected to one end of the common line through a dual-channel selection switch and the second common voltage supply line 52 is connected to the other end of the common line through a dual-channel selection switch.

[0046] In other words, two dual-channel selection switches are disposed on each set of common lines, the two dual-channel selection switches are disposed on the two ends of the common line respectively, and every input terminal of each of the dual-channel selection switches is connected to a common voltage supply line. If the common voltage is applied to common lines, the common voltage is applied to a set of common lines by the two common voltage supply lines on the two ends of the set of common lines simultaneously, such that the capability of the common voltage for driving loads is improved. Herein, a set of common lines include at least one common line, and in Figure 4 and Figure 5, the explanation is performed by taking a set of common lines including one common line as an example.

[0047] It is to be noted that the voltages applied to a same common line by the two common voltage supply line on the two ends of the common line at the same time are the same, that is, the control signals applied to the two dual-channel selection switches respectively on the two ends of the common line must be the same. Preferably, the two dual-channel selection switches respectively on the two ends of the common line may be controlled by a same switching control circuit.

[0048] Based on the array substrates disclosed according to the above embodiments, a LCD is disclosed according to another embodiment of the present invention. The LCD includes:

[0049] the array substrate described in the above embodiments, a color film substrate disposed opposite to the array substrate and a liquid crystal layer disposed between the array substrate and the color film substrate; a gate driving circuit which is connected to the multiple scanning lines and transmits multiple scanning signals through the multiple scanning lines so as to control the turn-on and turn-off of a transistor in a corresponding pixel unit; a source driving circuit which is connected to the multiple data lines and transmits multiple pieces of image data through the multiple data lines; a control circuit which is coupled to the gate driving circuit and the source driving circuit and controls the normal operations of the gate driving circuit and the source driving circuit; a switching control circuit which is connected to the con-

trol terminals of the multiple dual-channel selection switches, controls the connecting lines of the multiple dual-channel selection switches and selectively inputs a high level or a low level to the common lines through outputting a control signal.

[0050] As described in the above embodiments, the switching control circuit may be integrated with the gate driving circuit in a same chip, may also be integrated with the source driving circuit in a same chip, or may be integrated with the control circuit in a same chip. Preferably, the switching control circuit may be integrated with the gate driving circuit in this embodiment.

[0051] The LCD in this embodiment may preferably be an LCD controlled by a single gate. As shown in Figure 6, taking a pixel unit formed at the intersection of G1 with D1 as an example, the pixel unit includes: a transistor 601 of which the gate is connected to the scanning line G1 and the source is connected to the data line D1; a pixel element 602 of which one end is connected to the drain of the transistor 601 and the other end is connected to a common line Com1; and a storage capacitor 603 connected across the pixel element 602.

[0052] In other embodiments, the LCD may also be an LCD controlled by a dual-gate. As shown in Figure 7, taking a pixel unit formed at the intersection of G1 with D1 as an example, the pixel unit includes: a first transistor 701 of which the gate is connected to the scanning line G1 and the source is connected to the data line D1; a second transistor 702, the gate of the second transistor 702 being coupled to the gate of the first transistor 701, that is, the gates of the first transistor 701 and the second transistor 702 being connected to the same scanning line G1, and the source of the second transistor 702 being connected to the drain of the first transistor 701; a pixel element 703 of which one end is connected to the drain of the second transistor 702 and the other end is connected to a common line Com1; and a storage capacitor 704 connected across the pixel element 703.

[0053] Herein, regardless of that an LCD is controlled by a single gate or a dual-gate, the transistors included in the pixel units, that is, the transistor 601 in Figure 6, the first transistor 701 and the second transistor 702 in Figure 7 may be an a-Si TFT (amorphous-silicon thin film transistor), or a LTPS (low temperature poly-Silicon thin film) transistor or a HTPS (high temperature poly-silicon thin film) transistor.

[0054] The above-described pixel element may include a pixel electrode in the pixel area and liquid crystal molecules in the control area of the corresponding pixel electrode. The LCD in this embodiment may preferably be a LCD of a flat panel electric field mode in which the common lines are manufactured on the array substrate, and may include LCDs of IPS, FFS and AFFS driving modes.

[0055] There are two formation modes of the storage capacitor in this embodiment. One mode is that a storage capacitor is formed by one of a row of pixel electrodes overlapping with a common line corresponding to the row of pixel electrodes, and the other mode is that a storage capacitor is formed by one of a row of the pixel electrodes overlapping with both of a scanning line corresponding to the last row of pixel electrodes and a common line corresponding to the current row of pixel electrodes.

[0056] Based on the above structure, a control method for an LCD is disclosed according to another embodiment of the present invention. The control method is applied to the LCD described in the above embodiments, and the control method includes:

> Step 1: supplying power to a common line corresponding to a scanning line before providing a scanning signal to the scanning line, such that the pixel units connected to the scanning line have a common potential if a scanning signal is provided to the scanning line, and maintaining the potential of the common line unchanged during displaying a frame of picture.

[0057] In other words, the common line connected to a pixel unit to be turned on is charged in advance to guarantee that the common voltage has been applied on one end of the pixel element when the transistor in the pixel unit is turned on. Therefore the row of pixel elements may form potential differences across the pixel elements immediately after the corresponding transistors are turned on, so as to avoid the delay of the common voltage.

[0058] Further, since the potential of each of the common lines is maintained unchanged during displaying one frame of pictures, that is, during the displaying, each of common lines is not in a floating state. In other words, during displaying a frame of picture, the potential of each common line is stable and the potential does not change, thus the crosstalk among the common lines of individual rows is avoided and the stability of the common voltage during the displaying is guaranteed.

[0059] Step 2: inverting the potentials applied to the common lines during scanning for the next frame.

[0060] Since the potentials of the common lines inverts with the refresh frequency of the pictures during the displaying, the problem of liquid crystal aging caused if the liquid crystal is controlled in the same potential for a long time is avoided, and the normal displaying of the display is further guaranteed.

[0061] Theoretically, in order to avoid the delay of the common voltage, it only needs to apply the common voltage to one end of each of the pixel elements before the transistors in each row of pixel units is turned on. In other words, all the common lines on the entire array substrate can be charged in advance and the potentials of the common lines can be absolutely the same. But in this embodiment, in order to avoid that the load on the common voltage supplying terminal is excessively large which may cause the charging time of the common lines to excessively long, it is preferred that only some of common lines may be charged at the same time. It is more preferred that 1 to 4 common lines may be charged simul-

taneously. It is more preferred that one dual-channel selection switch is connected to only one common line, that is, only one common line is charged at the same time, as shown in Figure 4 and Figure 5.

[0062] Furthermore, in order to avoid that the charging of a common line is not synchronized with the charging of a scanning line, that is, during the charging of a scanning line, it begins to charge a common line, which may cause the crosstalk among the lines. Therefore, in the embodiment, it is preferred that the charging onset timing of the common line is the same as the onset timing of supplying a scanning signal to a scanning line, that is, it begins to supply power to the common line and the scanning line simultaneously, herein, the common line is not in the row corresponding to the scanning line.

[0063] For example, in this embodiment, in the case where the number of the scanning lines is the same as number of the common lines, that is, there are n scanning lines and n common lines on the array substrate of the LCD. Preferably, during displaying a frame of picture, the supplying power onset timing for the n-th common line is the supplying power onset timing for the (n-4)-th to the (n-1)-th scanning lines. It is more preferred that the n-th common line and the (n-1)-th scanning line are supplied with power simultaneously. As shown in Figure 8 and Figure 9, the control signal received by the dual-channel selection switch K2 is synchronized with the scanning signal received by the scanning line G1, the control signal received by the dual-channel selection switch K3 is synchronized with the scanning signal received by the scanning line G2, and so on, thus the charging time of Com2 is the same as the charging time of the pixel unit connected to G1, the charging time of Com3 is the same as the charging time of the pixel unit connected to G2, and so on.

[0064] Theoretically, the potentials for charging all the common lines on the array substrate during displaying a frame of picture may be the same, and the potentials of the common lines are inverted during scanning for the next frame. In this embodiment, in order to further reduce the load of the common voltage supplying terminal, it is preferred that some of common lines are supplied with a high potential and other common lines are supplied with a low potential. In this embodiment, it is more preferred that the potentials of two adjacent common lines are contrary to each other during displaying a frame of picture as shown in Figure 8, and a potential contrary to that of the last frame is applied to the common lines during the scanning for the next frame as shown in Figure 9.

[0065] Another control method for an LCD is disclosed according to another embodiment of the present invention. The control method is applied to the LCD with two common voltage supply lines. In this embodiment, the specific way for supplying power to the common lines is: at the same time, the two ends of one common line are connected to a same potential supply line of the first common voltage supply line and the second common voltage supply line respectively via the two dual-channel selection switches located at the two ends of the common line, and the common line is supplied with power by the first common voltage supply line and the second common voltage supply line simultaneously, thus the capability of the common voltage supplying terminal for driving the common line is further improved and the driving time of the common line is further shortened.

[0066] According to the description for the disclosed embodiments, those skilled in the art may implement or use the invention. A number of modifications to those embodiments will be apparent to those skilled in the art, and the general principles defined herein may be realized in other embodiments without departing from the scope or spirit of the invention. Therefore, the invention is not limited to the embodiments shown herein, and is subject to the maximum range according to the principles and the novel characteristics.

Claims

1. An array substrate, comprising:

a plurality of scanning lines parallel to each other in a first direction;
a plurality of data lines parallel to each other in a second direction, wherein the first direction intersects with the second direction;
a plurality of pixel units disposed at intersections of the scanning lines and the data lines;
a plurality of common lines, each common line arranged along a row of pixel units and electrically connected thereto;
a common voltage supply line having a common voltage high level supply line and a common voltage low level supply line; and
a plurality of dual-channel selection switches, each dual-channel selection switch comprising a control terminal, two input terminals and an output terminal,
wherein the output terminal of each of the dual-channel selection switches is connected to a set of common lines,
wherein the two input terminals of the dual-channel selection switch are connected to the common voltage high level supply line and the common voltage low level supply line respectively,
wherein a high level or a low level is selectively applied to the common lines in response to a control signal of the control terminal of the dual-channel selection switch, and
wherein the number of the common lines comprised in the set of common lines is less than the number of the common lines comprised in the array substrate.

2. The array substrate according to claim 1, wherein the common voltage supply line comprises a first

common voltage supply line and a second common voltage supply line, each of first and second common voltage supply lines comprising a common voltage high level supply line and a common voltage low level supply line; and the first common voltage supply line being connected to an end of the common line through a dual-channel selection switch, and the second common voltage supply line is connected to the other end the common line through a dual-channel selection switch.

3. The array substrate according to claim 1, wherein the control signal is a clock signal.

4. The array substrate according to claim 2, wherein the control signal is a clock signal.

5. The array substrate according to claim 3, wherein the set of common lines comprises only one common line.

6. A liquid crystal display, comprising:

the array substrate according to claim 1;
a color film substrate disposed opposite to the array substrate;
a liquid crystal layer disposed between the array substrate and the color film substrate;
a gate driving circuit connected to the scanning lines and configured to transmit scanning signals through the scanning lines;
a source driving circuit connected to the data lines and configured to transmit image data through the data lines;
a control circuit coupled to the gate driving circuit and the source driving circuit and configured to control a normal operation of the gate driving circuit and the source driving circuit; and
a switching control circuit connected to control terminals of the dual-channel selection switches, and configured to control connecting lines of the dual-channel selection switches and selectively apply a high level or a low level to the common lines through outputting a control signal.

7. The liquid crystal display according to claim 6, wherein the switching control circuit is integrated with the gate driving circuit, the source driving circuit, or the control circuit.

8. The liquid crystal display according to claim 6, wherein the pixel unit comprises:

a transistor having a gate connected to the scanning line and a source connected to the data line;
a pixel element having an end connected to the drain of the transistor and an opposite end connected to the common line; and
a storage capacitor connected across the pixel element.

9. The liquid crystal display according to claim 6, wherein the pixel unit comprises:

a first transistor having a gate connected to the scanning line and a source connected to the data line;
a second transistor having a gate coupled to the gate of the first transistor and a source coupled to the drain of the first transistor;
a pixel element having an end connected to the drain of the second transistor and an opposite end connected to the common line; and
a storage capacitor connected across the pixel element.

10. The liquid crystal display according to claim 8, wherein the transistor is an amorphous-silicon thin film transistor, a low temperature poly-silicon thin film transistor, or a high temperature poly-silicon thin film transistor.

11. The liquid crystal display according to claim 9, wherein the transistor is an amorphous-silicon thin film transistor, a low temperature poly-silicon thin film transistor, or a high temperature poly-silicon thin film transistor.

12. A control method for a liquid crystal display, which is applied to the liquid crystal display according to claim 6, the control method comprising:

supplying power to a common line corresponding to a scanning line before providing a scanning signal to the scanning line, wherein the pixel units connected to the scanning line have a common potential in the case where a scanning signal is provided to the scanning line;
maintaining a potential of the common line unchanged during display of a frame of picture; and
inverting a potential applied to the common line during scanning for a next frame.

13. The control method according to claim 12, wherein the array substrate of the liquid crystal display is provided with n scanning lines and n common lines, and during display of a frame of picture, wherein a supplying power onset timing for an n-th common line is one of the supplying power onset timings for an (n-4)-th scanning line to the (n-1)-th scanning line.

14. The control method according to claim 13, wherein the n-th common line and the (n-1)-th scanning line are supplied with power concurrently.

15. The control method according to claim 14, wherein

the potentials of two common lines adjacent to each other are opposite to each other during display of a frame of picture.

16. The control method according to claim 12, wherein supplying power to a common line comprises:

connecting the two ends of the common line to a same potential supply line of the first common voltage supply line and the second common voltage supply line through two dual-channel selection switches located at the two ends of the common line; and
concurrently supplying a power of the first common supply line and the second common voltage supply line to the common line.

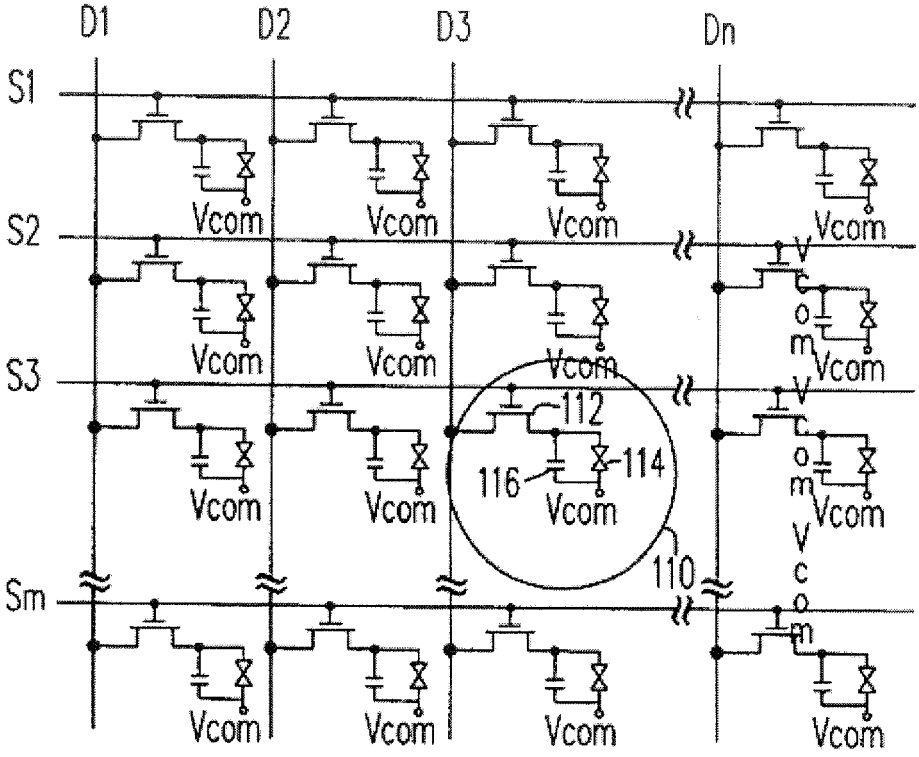

FIG. 1

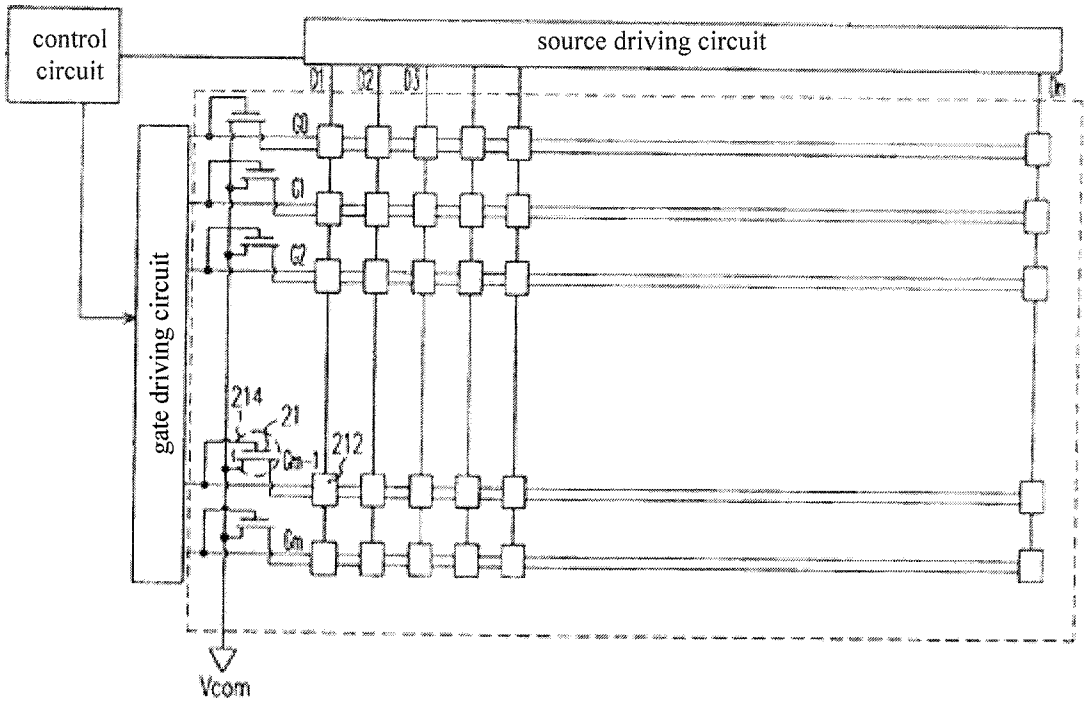
control circuit
source driving circuit
gate driving circuit
Vcom
214
21
212

FIG. 2

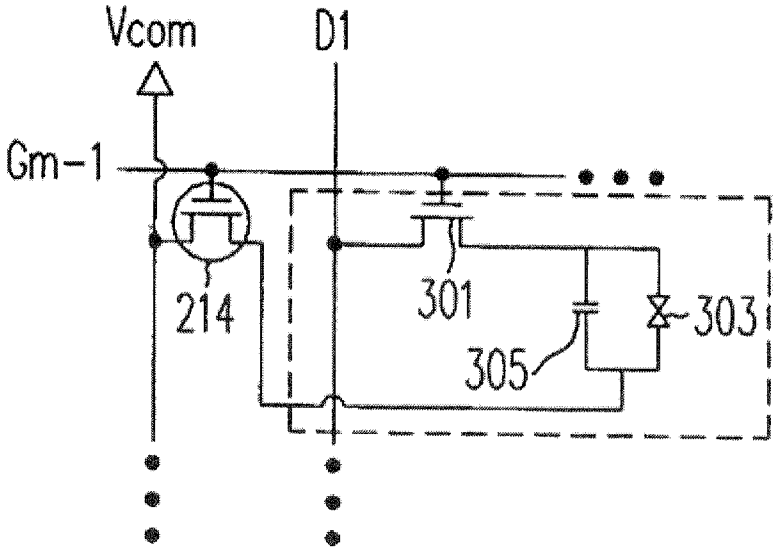
Vcom
D1
Gm-1
214
301
303
305

FIG. 3

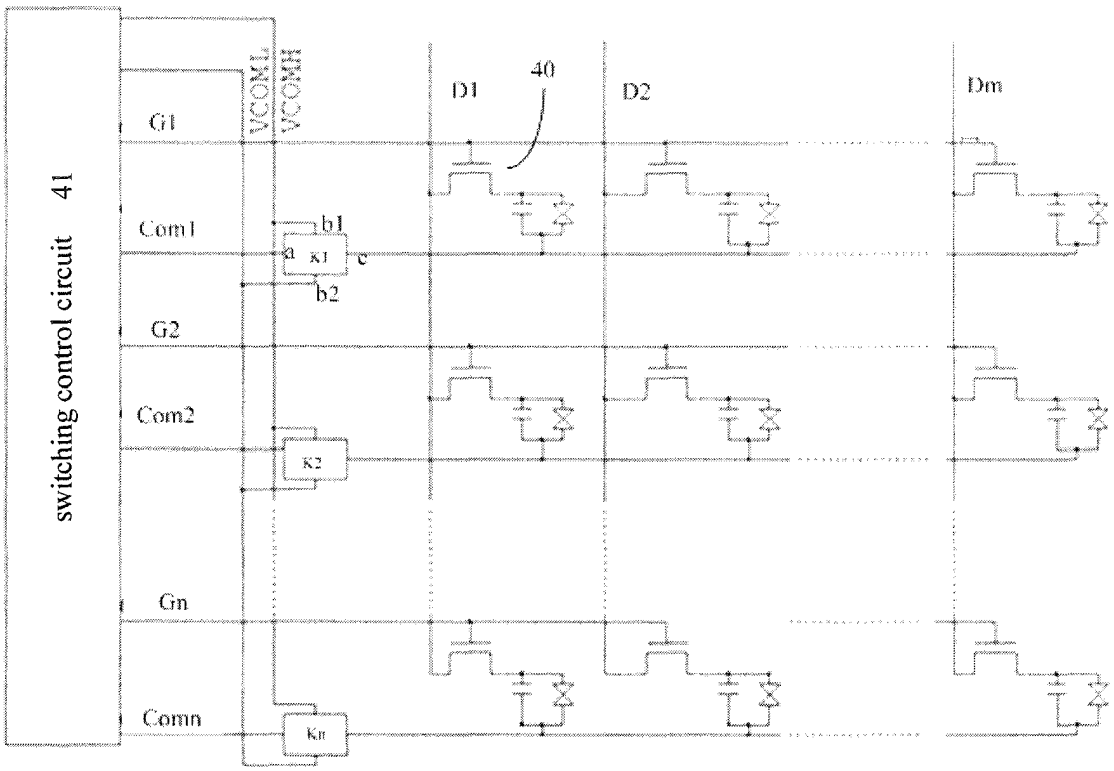
switching control circuit 41
G1
G2
Gn
Com1
Com2
Comn
VCOML
VCOMH
D1
D2
Dm
40
b1
a
K1
c
b2
K2
Kn

FIG. 4

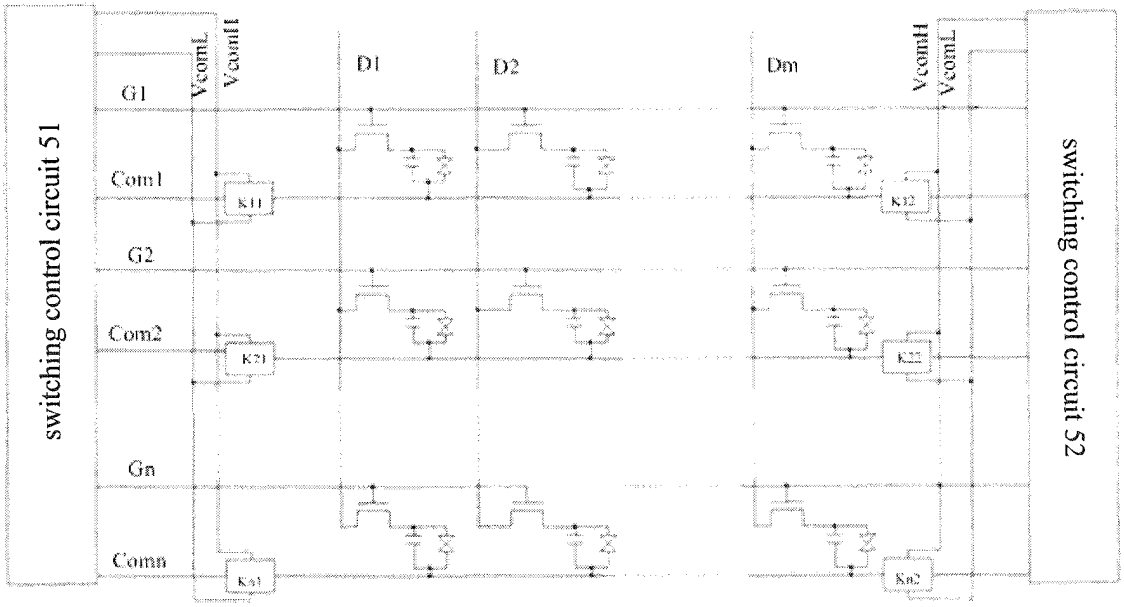
switching control circuit 51
switching control circuit 52
G1
G2
Gn
Com1
Com2
Comn
VcomL
VcomH
D1
D2
Dm
K11
K12
K21
K22
Kn1
Kn2

FIG. 5

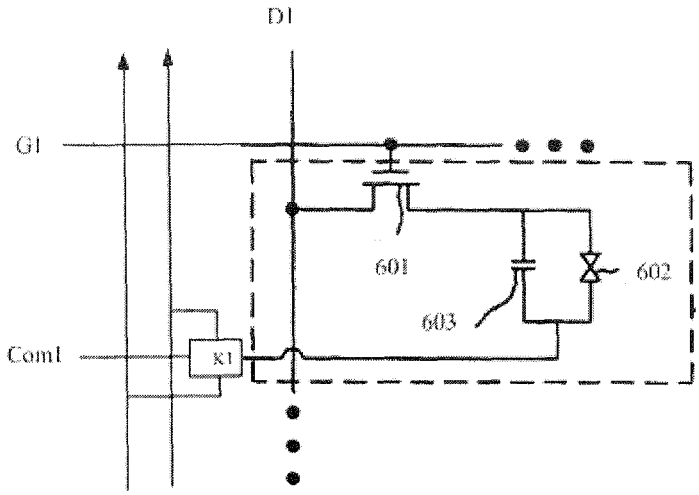

FIG. 6

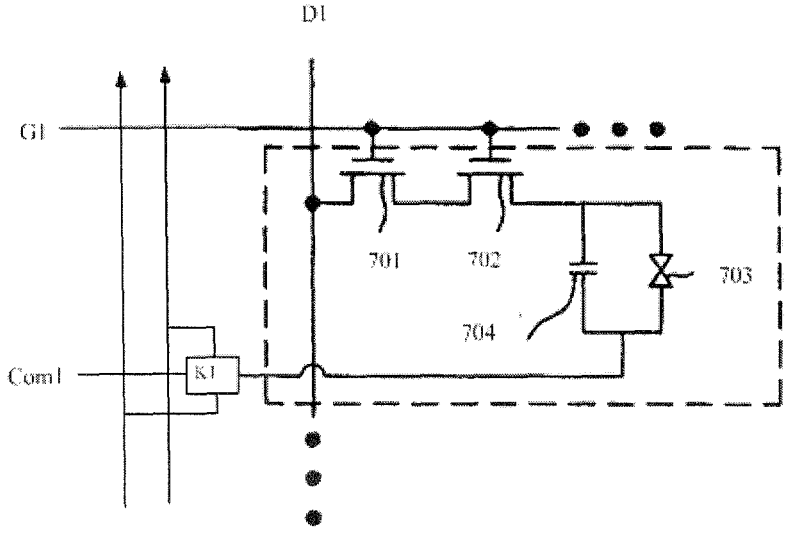

FIG. 7

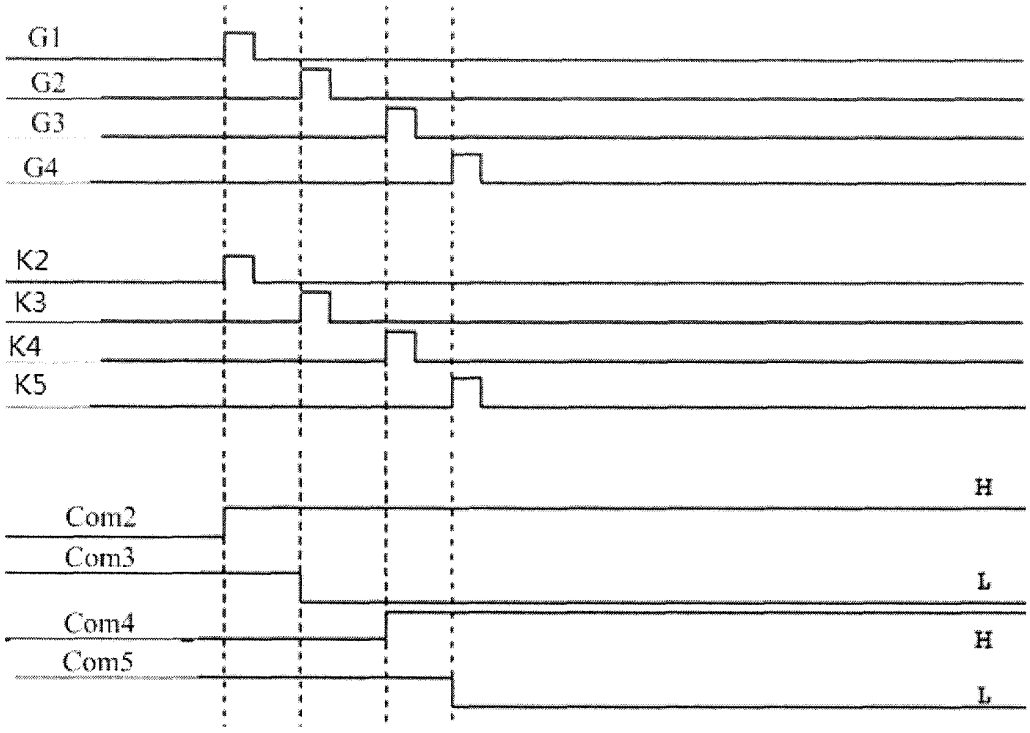
G1
G2
G3
G4
K2
K3
K4
K5
Com2
Com3
Com4
Com5
H
L
H
L

FIG. 8

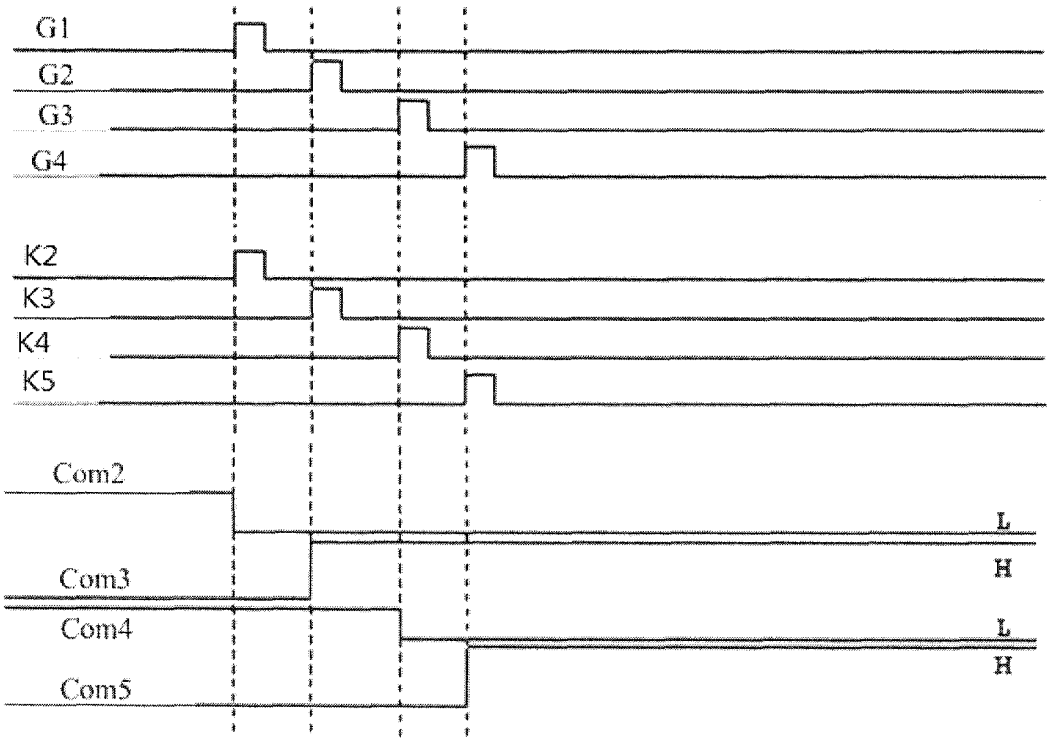
G1
G2
G3
G4
K2
K3
K4
K5
Com2
Com3
Com4
Com5
L
H
L
H

FIG. 9

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2012/085922

A. CLASSIFICATION OF SUBJECT MATTER

G02F 1/1368 (2006.01) i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: G02F, G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNABS, CNTXT: SHANGHAI TIANMA MICRO-ELECTRONICS CO., LTD., high, low, two-way selector switch, option switch, control end, high level, low level

USTXT, WOTXT, EPTXT, CATXT, VEN: VCOM, DRIFT, SWITCH, HIGH, LOW, COMMON, LINE, END, SIDE, SOURCE, VOLTAGE, THE SAME, ANOTHER, TWO

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	CN 101154004 A (EPSON IMAGING DEVICES CORP.), 02 April 2008 (02.04.2008), claims 6-7, description, page 11, line 2 to page 27, line 13, and figures 1, 6 and 9-10	1, 6-9, 12-15
Y	CN 101154004 A (EPSON IMAGING DEVICES CORP.), 02 April 2008 (02.04.2008), claims 6-7, description, page 11, line 2 to page 27, line 13, and page 48, lines 18-19, and figures 1, 6 and 9-10	2-5, 10-11, 16
Y	CN 1115535 A (SHARP KABUSHIKI KAISHA), 24 January 1996 (24.01.1996), description, page 26, line 14 to page 28, line 1, and figure 9	2-5, 10-11, 16
A	US 2006/0208985 A1 (LG DISPLAY CO., LTD.), 21 September 2006 (21.09.2006), the whole document	1-16

☒ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
02 April 2013 (02.04.2013)	**18 April 2013 (18.04.2013)**
Name and mailing address of the ISA/CN: State Intellectual Property Office of the P. R. China No. 6, Xitucheng Road, Jimenqiao Haidian District, Beijing 100088, China Facsimile No.: (86-10) 62019451	Authorized officer **XI, Wanhua** Telephone No.: (86-10) **62085833**

Form PCT/ISA/210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2012/085922

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2007/0057887 A1 (SONY CORP.), 15 March 2007 (15.03.2007), the whole document	1-16
A	US 2009/0128527 A1 (SONY CORP.), 21 May 2009 (21.05.2009), the whole document	1-16

Form PCT/ISA/210 (continuation of second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2012/085922

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Form PCT/ISA/210 (patent family annex) (July 2009)

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- CN 201210244083X **[0001]**

专利名称(译)	阵列基板，液晶显示器及其驱动方法		
公开(公告)号	EP2874002A1	公开(公告)日	2015-05-20
申请号	EP2012880905	申请日	2012-12-05
[标]申请(专利权)人(译)	上海天马微电子有限公司		
申请(专利权)人(译)	上海天马微电子有限公司.		
当前申请(专利权)人(译)	上海天马微电子有限公司.		
[标]发明人	ZHANG CHENGFENG LI YUAN YANG JINJIN		
发明人	ZHANG, CHENGFENG LI, YUAN YANG, JINJIN		
IPC分类号	G02F1/1368		
CPC分类号	G02F1/134363 G09G3/3648 G09G3/3655 G09G2300/0876 G09G2310/0218 G09G2310/08		
优先权	201210244083.X 2012-07-13 CN		
其他公开文献	EP2874002A4		
外部链接	Espacenet		

摘要(译)

根据本发明公开了一种阵列基板，液晶显示器及其控制方法。阵列基板包括：多条扫描线;多条数据线;多个像素单元;多条公共线，其中每条公共线沿着一行像素单元设置;公共电压供应线;多个双通道选择开关，其中每个双通道选择开关的输出端子连接到一组公共线，两个输入端子连接到公共电压高电平电源线和公共电压低电平电源线以便选择性地将高电平或低电平施加到公共线。该控制方法包括：在向扫描线提供扫描信号之前，向对应于扫描线的公共线提供电源，并且在显示图像帧期间保持公共线的电位不变;以及在扫描下一帧期间反转施加到公共线的电位。本发明实施例避免了显示期间公共电压Vcom的延迟和Vcom漂移的问题，提高了图像的显示效果。

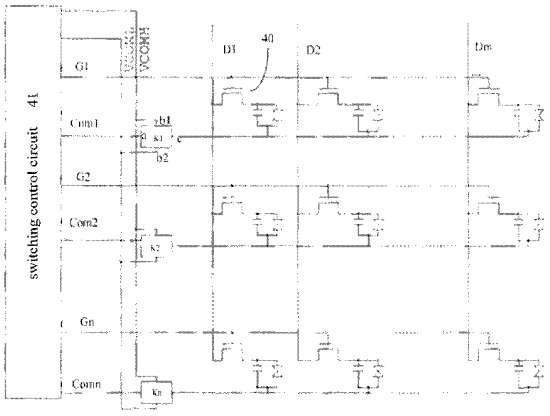

FIG. 4