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(72) Inventors:
• **ZHANG, Bin**
Beijing 100176 (CN)
• **ZHANG, Liang**
Beijing 100176 (CN)
• **HU, Weihao**
Beijing 100176 (CN)

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(71) Applicants:
• **BOE Technology Group Co., Ltd.**
Beijing 100015 (CN)
• **Beijing BOE Display Technology Co., Ltd.**
Beijing 100176 (CN)

(74) Representative: **Brötz, Helmut et al**
Rieder & Partner
Patentanwälte - Rechtsanwalt
Corneliusstrasse 45
42329 Wuppertal (DE)

(54) **THIN FILM TRANSISTOR ARRAY SUBSTRATE AS WELL AS DRIVING METHOD AND LIQUID CRYSTAL DISPLAY THEREOF**

(57) A thin film transistor array substrate as well as a driving method and a liquid crystal display thereof. The thin film transistor array substrate comprises at least one sub-pixel area formed by that one grid electrode line and a data line cross with each other. Each sub-pixel comprises: a first transistor (21), a grid electrode being connected to the grid electrode line, and a drain electrode being connected to the data line; a first storage capacitor (23), one end being connected to a source electrode of the first transistor (21), and the other end being connected to a reference voltage output end. At the same time, the sub-pixel further comprises: a second storage capacitor (24) and a second transistor (25). One end of the second storage capacitor (24) is connected to the source electrode of the first transistor (21), and the other end is connected to a drain electrode of the second transistor (25). A source electrode of the second transistor (25) is connected to the reference voltage output end, and a grid electrode of the second transistor is connected to an enable signal output end. Because each sub-pixel in the thin film transistor array substrate is respectively additionally provided with the second storage capacitor (24), capacitance of the storage capacitors displayed during static status display is increased, voltage conversion frequency during the static status display is lowered, and

an effect on lowering the system power consumption is achieved.

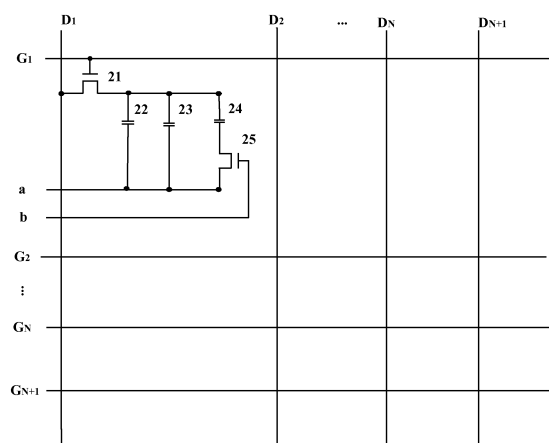


FIG. 2

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Description

TECHNICAL FIELD

[0001] The present invention relates to a thin film transistor (TFT) array substrate and a driving method therefor as well as a liquid crystal display (LCD).

BACKGROUND

[0002] With the continuing development of the LCD technology, the LCD with small size, low power consumption, no radiation and the like has gradually replaced the cathode ray tube (CRT) display, and becomes the mainstream product among display devices.

[0003] Nowadays, the LCD typically has a TFT array substrate structure as shown in FIG 1. The TFT array substrate includes at least one sub-pixel region formed with a gate line (G) and a data line (D) intersected with each other (taking the structure schematic diagram of the TFT array substrate shown in FIG 1 as an example, a sub-pixel region is formed when G_1 , G_2 , D_1 and D_2 are intersected with each other, and likewise, a sub-pixel region is formed as well when G_N , G_{N+1} , D_N and D_{N+1} are intersected with each other.) The sub-pixel corresponding to each sub-pixel region comprises a transistor 11, a liquid crystal capacitor 12, and a storage capacitor 13. The gate of the transistor 11 is connected with a gate line, and the drain of the transistor 11 is connected with a data line; one end of the liquid crystal capacitor 12 is connected with the source of the transistor 11, and the other end of the liquid crystal capacitor 12 is connected with the output (denoted as 'a') of a reference voltage (Vcom); and one end of the storage capacitor 13 is connected with the source of the transistor 11, and the other end of the storage capacitor 13 is connected with the output of the reference voltage.

[0004] The sub-pixel region on which the transistor 11 is placed is activated for display when a driving voltage is loaded onto the transistor 11 through the data line.

[0005] Currently, in order to ensure the image continuity of each sub-pixel of the LCDs during the dynamic image display, the LCDs mostly change the driving voltage once per 60 Hz (i.e., the voltage conversion frequency is 60Hz) to realize the AC drive of the sub-pixel. Even if each sub-pixel of the LCD is in the static image display, the voltage conversion frequency is fixed at 60Hz.

[0006] However, since the LCD power consumption generated during driving each sub-pixel of the LCD for image display is proportional to the driving voltage, the voltage conversion frequency of the driving voltage, and the parasitic capacitance on the LCD data line, the LCD will produce high static power consumption because of the high voltage conversion frequency when each sub-pixel of the LCD is in the static display mode.

SUMMARY

[0007] The embodiments of the invention provide a TFT array substrate and a driving method therefor as well as a liquid crystal display.

[0008] In one aspect of the present invention, it provides a TFT array substrate including at least one sub-pixel region formed by a gate line and a data line intersected with each other, wherein, a sub-pixel corresponding to each of at least one sub-pixel region comprises a first transistor of which the gate is connected with a gate line and the drain is connected with a data line and a first storage capacitor of which one end is connected with the source of the first transistor and the other end is connected with an output of a first reference voltage, the sub-pixel further comprises a second storage capacitor and a second transistor, wherein one end of the second storage capacitor is connected with the source of the first transistor, and the other end of the second storage capacitor is connected with the drain of the second transistor; the source of the second transistor is connected with an output of a second reference voltage, and the gate of the second transistor is connected with an output (denoted as 'b') of an Enable signal.

[0009] For example, the second transistor is a metal oxide semiconductor field effect transistor (MOSFET). For example, the first reference voltage and the second reference voltage are the same reference voltage, e.g., Vcom.

[0010] In another aspect of the present invention, it provides a LCD, wherein the LCD includes the above-mentioned TFT array substrate.

[0011] In still another aspect of the present invention, it provides a method for driving the above-mentioned TFT array substrate. The method includes: the output of the Enable signal inputs a first Enable signal to the gate of the second transistor for setting the second transistor into an open circuit state when the sub-pixel in the TFT array substrate performs dynamic image display; and the output of the Enable signal inputs a second Enable signal to the gate of the second transistor for setting the second transistor into a conducting state when the sub-pixel in the TFT array substrate performs static image display.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] In order to illustrate the technical solution of the embodiments of the invention more clearly, the drawings of the embodiments will be briefly described below; it is obvious that the drawings as described below are only related to some embodiments of the invention, and thus are not limitative of the invention.

FIG 1 is a schematic diagram of the TFT array substrate structure in the prior art;

FIG 2 is a schematic diagram of the TFT array substrate structure in an embodiment of the present invention;

FIG 3 is a schematic diagram of the signal drive of the TFT array substrate in an embodiment of the present invention.

DETAILED DESCRIPTION

[0013] The technical solutions of the embodiments of the present invention will be described in a clearly and fully understandable way in connection with the drawings related to the embodiments of the invention. It is obvious that the described embodiments are just a part but not all of the embodiments of the invention. According to the embodiments of the invention, all other embodiments obtained by those ordinary skilled in the art under the premise of without creative efforts are all intend to be within the scope of the invention.

[0014] Since the LCD power consumption generated during driving each sub-pixel of the TFT array substrate of the LCD for image display is proportional to the driving voltage, the voltage conversion frequency of the driving voltage, and the parasitic capacitance on the data line of the LCD, and the driving voltage and the parasitic capacitance on the data line of the LCD is determined by the characteristics of the liquid crystal of the LCD, which means that the driving voltage of the LCD and the parasitic capacitance on the data line of the LCD are determined when the LCD is determined, in order to decrease the static power consumption generated during each sub-pixel in the TFT array substrate of the LCD performing static image display, a new TFT array substrate is provided in the embodiments of the present invention, which achieves the effects of increasing the capacitance of the storage capacitor of each sub-pixel to decrease the voltage conversion frequency by providing an additional storage capacitor and a transistor for controlling the switching of the additional storage capacitor in each sub-pixel of the TFT array substrate.

[0015] A further description of the embodiments of the present invention will be made by reference to the accompanying drawings. However, the present invention is not limited to the following embodiments.

Embodiment 1:

[0016] As shown in FIG 2, it is the structure schematic diagram of the TFT array substrate in the embodiment 1 of the present invention. The TFT array substrate includes at least one sub-pixel region formed by a gate line and a data line intersected with each other (taking the structure schematic diagram of the TFT array substrate shown in FIG 2 as an example, a sub-pixel region is formed when G_1 , G_2 , D_1 and D_2 are intersected with each other, and likewise, a sub-pixel region is also formed when G_N , G_{N+1} , D_N and D_{N+1} are intersected with each other), wherein, the sub-pixel corresponding to each sub-pixel region includes a first transistor 21 of which the gate is connected with a gate line and the drain is connected with a data line, and a first storage capacitor 23 of which

one end is connected with the source of the first transistor and the other end is connected with an output (denoted as 'a') of a first reference voltage, and the sub-pixel further includes a second storage capacitor 24 and a second transistor 25, wherein:

one end of the second storage capacitor 24 is connected with the source of the first transistor 21, and the other end of the second storage capacitor is connected with the drain of the second transistor 25; the source of the second transistor 25 is connected with an output of a second reference voltage, and the gate of the second transistor 25 is connected with the output (denoted as 'b') of the Enable signal.

[0017] The first and the second reference voltages may be different reference voltages or the same reference voltage, e.g., V_{com} .

[0018] For example, the capacitance of the first storage capacitor 23 and the second storage capacitor 24 can be set according to the actual situation, but there is not any limitation to this in the embodiment of the invention. On the other hand, the first transistor 21 and the second transistor 25 can be switching tubes, such as, Metal Oxide Semiconductor Field Effect Transistor (MOSFET), including PMOSFET and NMOSFET, and Thin Film Transistors (TFT). For example, it may be NMOSFET.

[0019] For example, the second transistor 25 is used to control the switching of the second storage capacitor 24, and the second transistor 25 is a NMOSFET. The second transistor 25 is in a conducting state when the Enable signal outputted by the output of the Enable signal is at a high level. At this time, the second storage capacitor 24 and the first storage capacitor 23 are connected in parallel. Taking the TFT array substrate shown in Fig.2 as an example, the capacitance of the storage capacitors of the sub-pixel corresponding to the sub-pixel region formed by intersecting G_1 , G_2 , D_1 , and D_2 to each other would be the sum of the capacitance of the first storage capacitor 23 and that of the second storage capacitor 24. At this time, the voltage conversion frequency of the LCD driving voltage is decreased accordingly since the capacitance of the storage capacitors is increased. Taking the voltage conversion frequency of 60Hz in the prior art as an example, the decreased voltage conversion frequency can be of 6-10Hz. Further, the second transistor 25 is in an open circuit state when the Enable signal outputted by the output of the Enable signal is at a low level. At this time, still taking the TFT array substrate shown in Fig. 2 as an example, the capacitance of the storage capacitors of the sub-pixel corresponding to the sub-pixel region formed by intersecting G_1 , G_2 , D_1 and D_2 to each other would be only the capacitance of the first storage capacitor 23. Under this circumstance, the voltage conversion frequency of the LCD driving voltage would remain unchanged since the capacitance of the storage capacitors is the same as the capacitance of the storage capacitor of each sub-pixel in the TFT array substrate in

the prior art.

[0020] Further, the Enable signal outputted by the output of the enable signal is controlled by a timing controller (TCON).

[0021] Since the higher the capacitance of the storage capacitors, the lower the voltage conversion frequency of the LCD driving voltage, and the lower the voltage conversion frequency, the lower the LCD static power consumption. Therefore, in the embodiment 1 of the present invention, in order to decrease the static power consumption generated during performing the static image display by each sub-pixel in the TFT array substrate of the LCD, and to ensure the image continuity during performing the dynamic image display by each sub-pixel at the same time, it is required that the Enable signal outputted by the output of the Enable signal corresponding to the second transistor 25 of the sub-pixel is the first Enable signal which enables the second transistor 25 to be set in the open circuit state (for example, the first Enable signal can be at the low level when the second transistor is a NMOSFET) when the sub-pixel of the TFT array substrate performs dynamic image display, and moreover, the Enable signal outputted by the output of the Enable signal corresponding to the second transistor 25 of the sub-pixel is the second Enable signal which enables the second transistor 25 to be set in the conducting state (for example, the second Enable signal can be at the high level when the second transistor is a NMOSFET) when the sub-pixel performs static image display.

[0022] For example, the second transistor is a NMOSFET. Taking the signal driving schematic diagram of the TFT array substrate shown in Fig. 3 as an example, the Data signals on the data line between frames (such as, frame N-1, frame N, and frame N+1) are the same when the sub-pixel of the TFT array substrate performs static image display. At this time, in order to decrease the static power consumption generated during static image display performed by each sub-pixel, the Enable signals outputted by the output of the Enable signal are all at the high level. When the sub-pixel of the TFT array substrate performs dynamic image display, the data on the data line between frames (such as, between frame N+1 and frame N+2, or between frame N-2 and frame N-1) are different. At this time, in order to ensure the image continuity during dynamic image display performed by each sub-pixel, the Enable signal outputted by the output of the Enable signal is at the low level.

[0023] Further, the TFT array substrate also includes a liquid crystal capacitor 22 of which one end is connected with the drain of the first transistor 21 and the other end is connected with the output of Vcom. For example, the capacitance of the liquid crystal capacitor 22 is determined by the characteristics of the liquid crystal of the LCD, and the capacitance of the liquid crystal capacitor 22 is usually small.

[0024] It is needed to be explained that, in the TFT array substrate described in the embodiment 1, each

sub-pixel may comprise several branches, each of which is formed by the second storage capacitor 24 connected with the second transistor 25 in series and is connected with the first storage capacitor 23 in parallel. There is not any limitation for this in the embodiments of the invention. In addition, for any one branch which is formed by the second storage capacitor 24 connected with the second transistor 25 in series and is connected with the first storage capacitor 23 in parallel, the branch may also comprise several second storage capacitors 24 and/or second transistors 25. There is not any limitation for this in the embodiments of the invention.

[0025] A TFT array substrate is provided in the embodiment 1 of the present invention. In the TFT array substrate, each sub-pixel comprises a first transistor of which the gate is connected with a gate line and the drain is connected with the data line, and a first storage capacitor of which one end is connected with the source of the first transistor and the other end is connected with the output of Vcom. At the same time, each sub-pixel also comprises a second storage capacitor and a second transistor, wherein one end of the second storage capacitor is connected with the source of the first transistor and the other end of the second storage capacitor is connected with the drain of the second transistor; and the source of the second transistor is connected with the output of Vcom and the gate of the second transistor is connected with the output of the Enable signal. Since in the TFT array substrate of the embodiment 1 of the present invention, each sub-pixel is additionally provided with the second storage capacitor, the capacitance of the storage capacitors during static image display performed by each sub-pixel is increased, the voltage conversion frequency during static image display is decreased, and the effect of decreasing the system power consumption is achieved.

Embodiment 2

[0026] The embodiment 2 of the present invention provides a LCD. The LCD comprises the TFT array substrate described in the embodiment 1.

[0027] For example, in comparison to the existing LCD, in the TFT array substrate of the LCD described in the embodiment 2, each sub-pixel is additionally provided with both the second storage capacitor and the second transistor for controlling the switching of the second storage capacitor, wherein one end of the second storage capacitor is connected with the source of the first transistor in the TFT array substrate, the other end of the second storage capacitor is connected with the drain of the second transistor, and the source of the second transistor is connected with the output of Vcom and the gate of the second transistor is connected with the output of the Enable signal.

[0028] For example, when each sub-pixel in the TFT array substrate of the LCD of the embodiment 2 of the present invention performs dynamic image display, the Enable signal outputted by the output of the Enable signal

corresponding to the second transistor of the sub-pixel is the first Enable signal for setting the second transistor into the open circuit state (for example, when the second transistor is a NMOSFET, the first Enable signal can be at the low level), and when the sub-pixel performs static image display, the Enable signal outputted by the output of the Enable signal corresponding to the second transistor of the sub-pixel is the second Enable signal for setting the second transistor into the conducting state (for example, when the second transistor is a NMOSFET, the second Enable signal can be at the high level). Therefore, the capacitance of each sub-pixel in the TFT array substrate of the LCD during the static display is increased, the voltage conversion frequency during the static display is decreased, and the effect of decreasing the system power consumption is achieved.

[0029] It is needed to be explained that in comparison to the existing LCD, all structural components other than the TFT array substrate of the LCD may remain unchanged in the LCD described in the embodiment 2 of the present invention.

Embodiment 3

[0030] The embodiment 3 of the present invention provides a method for driving the TFT array substrate described in the embodiment 1, which comprises:

when the sub-pixel in the TFT array substrate performs dynamic image display, the output of the Enable signal inputs the first Enable signal to the gate of the second transistor for setting the second transistor into the open circuit state (for example, when the second transistor is a NMOSFET, the first Enable signal can be at the low level); when the sub-pixel in the TFT array substrate performs static image display, the output of the Enable signal inputs the second Enable signal to the gate of the second transistor for setting the second Enable signal into the conducting state (for example, when the second transistor is a NMOSFET, the second Enable signal can be at the high level).

[0031] For example, the second transistor is a NMOSFET. When the output of the Enable signal inputs the Enable signal with the low level to the gate of the second transistor, the second transistor is in the open circuit state. At this time, taking the TFT array substrate shown in Fig. 2 as an example, the capacitance of the storage capacitors of the sub-pixel corresponding to the sub-pixel region formed by intersecting G_1 , G_2 , D_1 and D_2 to each other is only the capacitance of the first storage capacitor 23. At this time, the voltage conversion frequency of the driving voltage remains unchanged (it is usually 60Hz in the prior art). Further, the second transistor 25 is in the conducting state when the Enable signal outputted by the output of the Enable signal to the gate of the second transistor is at the high level. At this time, the second

storage capacitor 24 and the first storage capacitor 23 are connected in parallel. In still an example of the TFT array substrate shown in Fig.2, the capacitance of the storage capacitors of the sub-pixel corresponding to the sub-pixel region formed by intersecting G_1 , G_2 , D_1 and D_2 to each other would be the sum of the capacitance of the first storage capacitor 23 and that of the second storage capacitor 24. At this time, since the capacitance of the storage capacitors is increased, the voltage conversion frequency of the LCD driving voltage is decreased accordingly. Taking the voltage conversion frequency of 60Hz in the prior art as an example, the decreased voltage conversion frequency can be of 6-10Hz.

[0032] For example, the Enable signal outputted by the output of the Enable signal can be controlled by a TCON. When the second transistor is a NMOSFET, taking the signal driving schematic diagram of the TFT array substrate shown in Fig.3 as an example, Data signals on the data line between frames (such as, frames N-1, N and N+1) are the same when the sub-pixel of the TFT array substrate performs static image display. At this time, in order to decrease the static power consumption generated by each sub-pixel during the static display, TCON may control all Enable signals outputted by the output of the Enable signal to be at the high level according to the state of frames N-1, N and N+1 of the data signals on the data line. When the sub-pixel of the TFT array substrate performs dynamic image display, the data on the data line between frames (such as, between frame N+1 and frame N+2, or between frame N-2 and N-1) are different. At this time, in order to ensure the image continuity of each sub-pixel during dynamic image display, TCON may control the Enable signal outputted by the output of the Enable signal to be at the low level according to the state of frames N+1 and N+2 or frames N-2 and N-1 of the data signals on the data line.

[0033] The disclosed technical solution provides at least the following advantages:

- (1) Since a second storage capacitor is additionally added to each sub-pixel, the capacitance of the storage capacitors during static display is increased;
- (2) The voltage conversion frequency during static display is decreased; and
- (3) The system power consumption during static image display is decreased.

[0034] The above description is only the exemplary embodiments of the present invention, but not used to limit the scope of the present invention, which should be determined by the attaching claims.

Claims

1. A thin film transistor array substrate, comprising at least a sub-pixel region formed by a gate line and a data line intersected with each other, wherein, a sub-

pixel corresponding to each sub-pixel region comprises a first transistor of which the gate is connected with a gate line and the drain is connected with a data line, and a first storage capacitor of which one end is connected with the source of the first transistor and the other end is connected with an output of a reference voltage, wherein the sub-pixel further comprises a second storage capacitor and a second transistor, wherein:

one end of the second storage capacitor is connected with the source of the first transistor, and the other end of the second storage capacitor is connected with the drain of the second transistor;
the source of the second transistor is connected with the output of the reference voltage, and the gate of the second transistor is connected with an output of an Enable signal.

2. The thin film transistor array substrate of claim 1, wherein the second transistor is a metal oxide semiconductor field effect transistor.
3. A liquid crystal display comprising the thin film transistor array substrate of claim 1 or 2.
4. A method for driving the thin film transistor array substrate of claim 1, comprising:

the output of the Enable signal inputting a first Enable signal to the gate of the second transistor which sets the second transistor in an open circuit state when the sub-pixel in the thin film transistor array substrate is in dynamic image display;

the output of the Enable signal inputting a second Enable signal to the gate of the second transistor which sets the second transistor in a conducting state when the sub-pixel in the thin film transistor array substrate is in static image display.
5. The method in claim 4, wherein the Enable signal outputted by the output of the Enable signal is controlled by a timing controller.
6. The method in claim 4, wherein the driving voltage conversion frequency of the sub-pixel is from 6 to 10 Hz when each sub-pixel of the thin film transistor array substrate performs static image display.

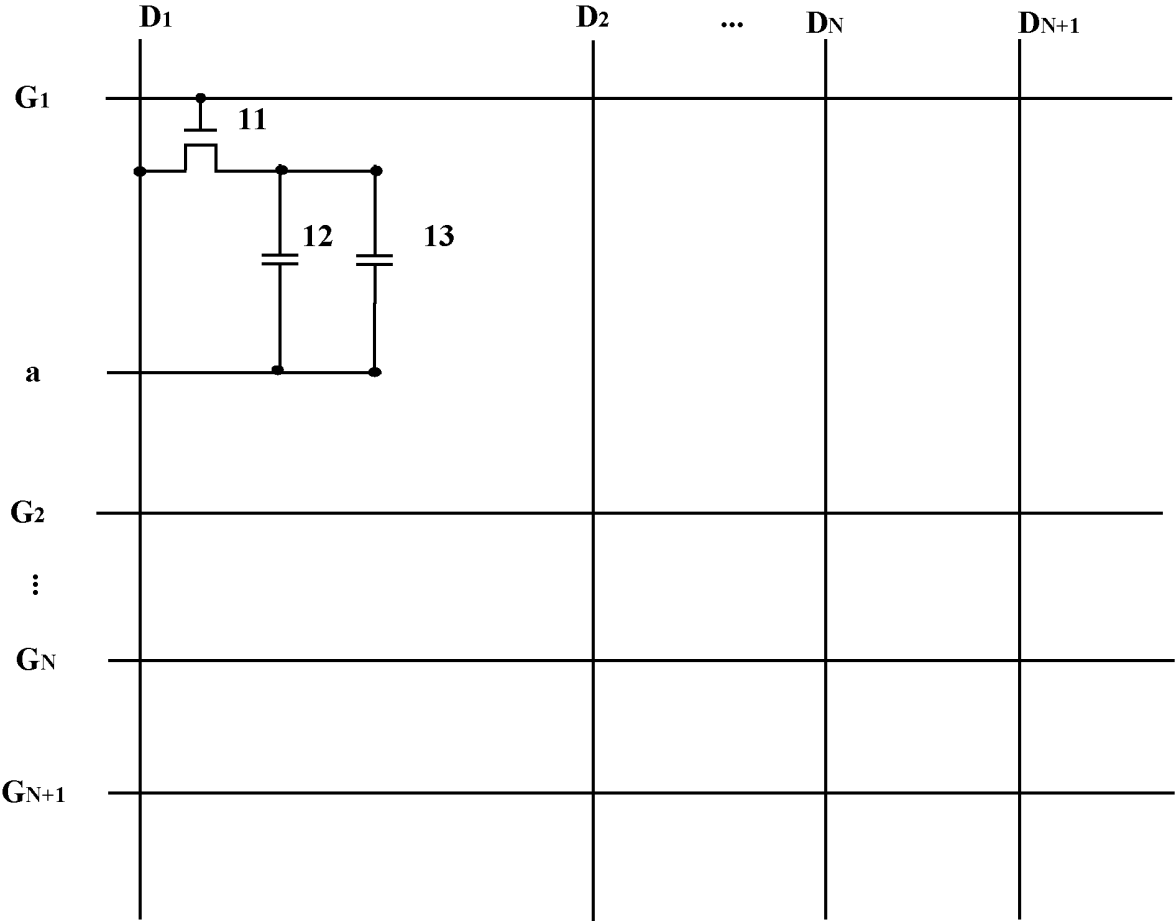


FIG. 1

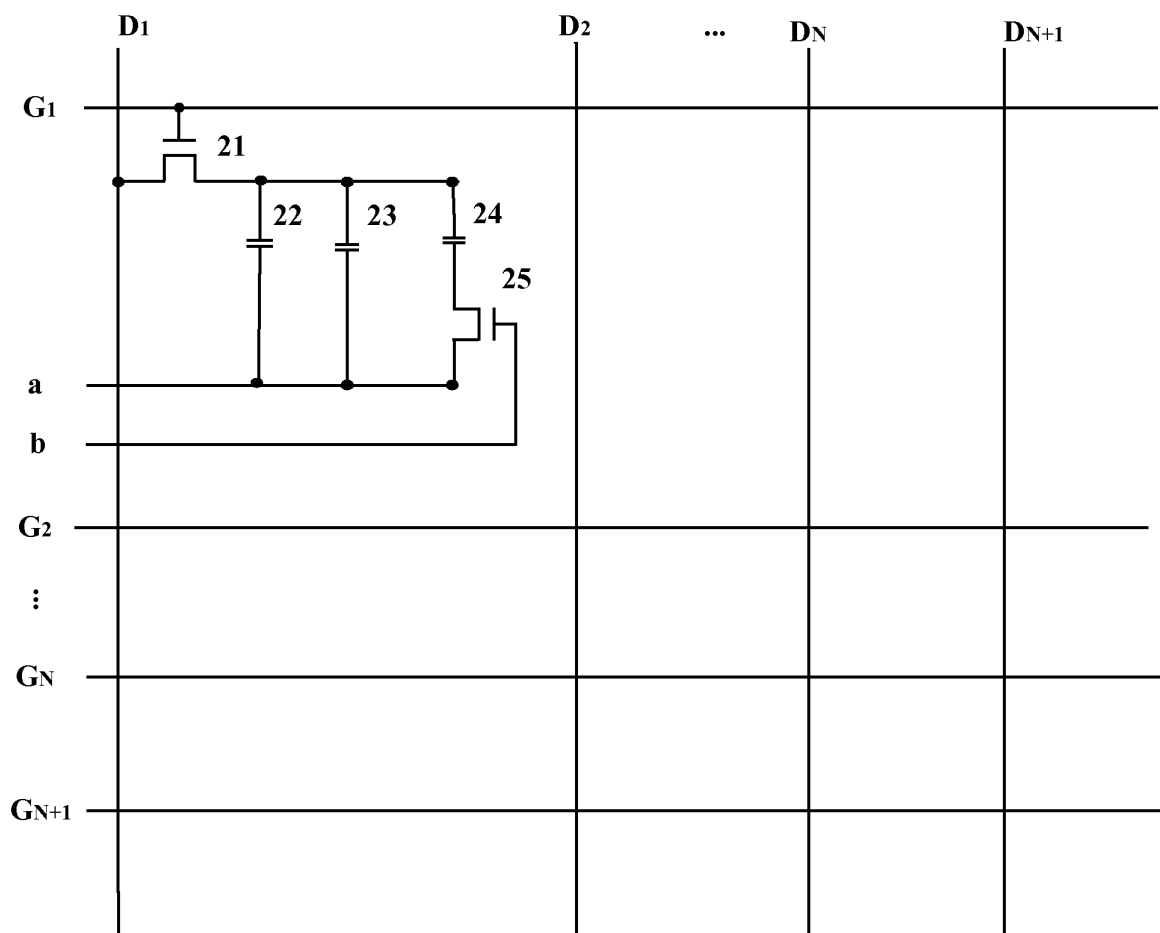


FIG. 2

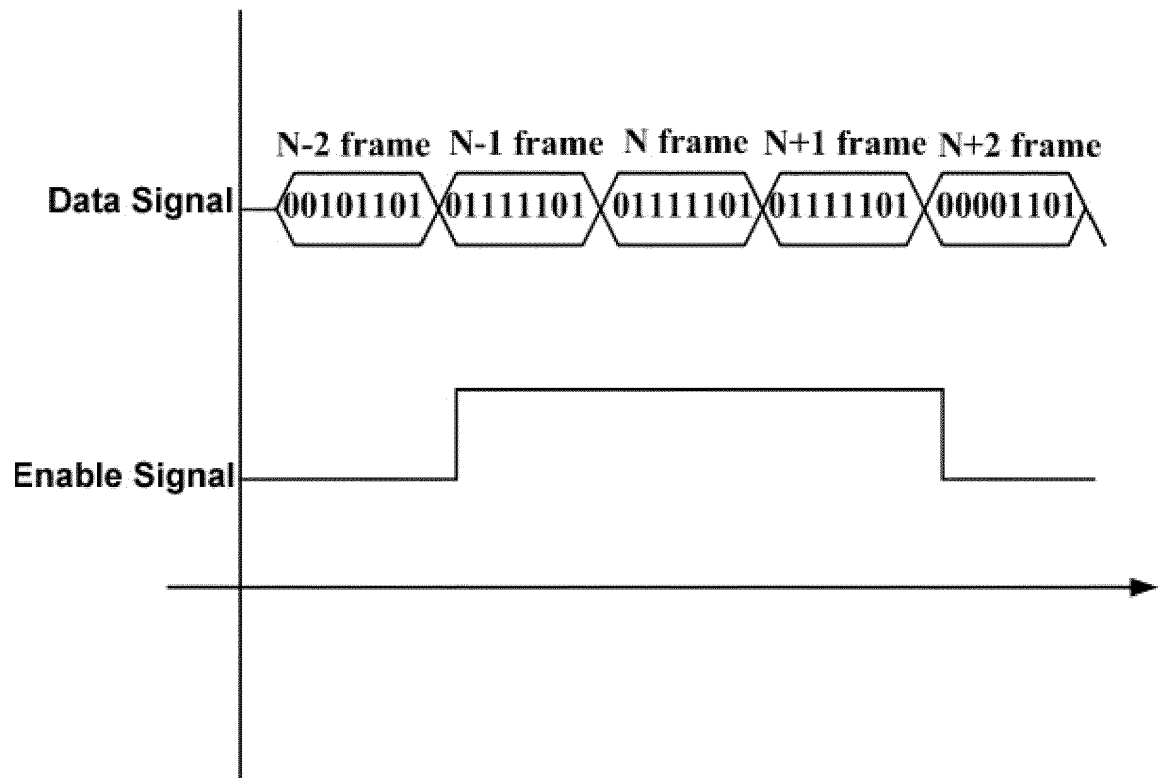


FIG. 3

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2012/085762

A. CLASSIFICATION OF SUBJECT MATTER

See the extra sheet
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: G02F; G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

VEN, CNABS, CNTXT, CNKI: pixel, array, substrate, capacitance, memory, storage, transistor, second, enable, liquid crystal, gate line, data line, reference voltage, enable signal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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A	CN 102184717 A (SHENZHEN HUAXING ELECTRIC TECH) 29 April 2011 (29.04.2011) description, pages 2 to 5 and figure 5	1-6
A	CN 101446721 A (KUNSHAN LONGTENG ACTINOELECTRICITY CO., LTD.) 03 June 2009 (03.06.2009) the whole document	1-6
A	CN 102135689 A (AU OPTRONICS CORP) 27 July 2011 (27.07.2011) the whole document	1-6
A	US 2011181563 A1 (CHUNGWA PICTURE TUBES LTD) 28 July 2011 (28.07.2011) the whole document	1-6

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A" document defining the general state of the art which is not considered to be of particular relevance	
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"O" document referring to an oral disclosure, use, exhibition or other means	
"P" document published prior to the international filing date but later than the priority date claimed	"&" document member of the same patent family

Date of the actual completion of the international search 27 March 2013 (27.03.2013)	Date of mailing of the international search report 11 April 2013 (11.04.2013)
Name and mailing address of the ISA State Intellectual Property Office of the P. R. China No. 6, Xitucheng Road, Jimenqiao Haidian District, Beijing 100088, China Facsimile No. (86-10) 62019451	Authorized officer YANG, Yan Telephone No. (86-10) 62085617

INTERNATIONAL SEARCH REPORT
 Information on patent family members

 International application No.
 PCT/CN2012/085762

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2012/085762

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A. CLASSIFICATION OF SUBJECT MATTER
G02F 1/1362 (2006.01) i
G09G 3/36 (2006.01) i
G02F 1/133 (2006.01) i
G02F 1/1368 (2006.01) i

专利名称(译)	薄膜晶体管阵列基板及其驱动方法和液晶显示器		
公开(公告)号	EP2871516A1	公开(公告)日	2015-05-13
申请号	EP2012880654	申请日	2012-12-03
[标]申请(专利权)人(译)	京东方科技集团股份有限公司 北京京东方显示技术有限公司		
申请(专利权)人(译)	京东方科技集团股份有限公司. 北京京东方显示技术有限公司.		
当前申请(专利权)人(译)	京东方科技集团股份有限公司. 北京京东方显示技术有限公司.		
[标]发明人	ZHANG BIN ZHANG LIANG HU WEIHAO		
发明人	ZHANG, BIN ZHANG, LIANG HU, WEIHAO		
IPC分类号	G02F1/1362 G09G3/36 G02F1/133 G02F1/1368		
CPC分类号	H01L27/1255 G02F1/136213 G09G3/3648 G09G3/3696 G09G2300/0852 G09G2320/10 G09G2330/021 G09G2340/0435		
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其他公开文献	EP2871516A4		
外部链接	Espacenet		

摘要(译)

薄膜晶体管阵列基板及其驱动方法和液晶显示器。薄膜晶体管阵列基板包括由该一条栅极线和数据线彼此交叉形成的至少一个子像素区域。每个子像素包括：第一晶体管（21），栅极连接到栅极线，漏极连接到数据线；第一存储电容器（23），一端连接到第一晶体管（21）的源极，另一端连接到参考电压输出端。同时，子像素还包括：第二存储电容器（24）和第二晶体管（25）。第二存储电容器（24）的一端连接到第一晶体管（21）的源极，另一端连接到第二晶体管（25）的漏极。第二晶体管（25）的源极连接到参考电压输出端，第二晶体管的栅极连接到使能信号输出端。由于薄膜晶体管阵列基板中的每个子像素分别另外设置有第二存储电容器（24），因此在静态状态显示期间显示的存储电容器的电容增加，静态状态显示期间的电压转换频率降低，并且实现了降低系统功耗的效果。

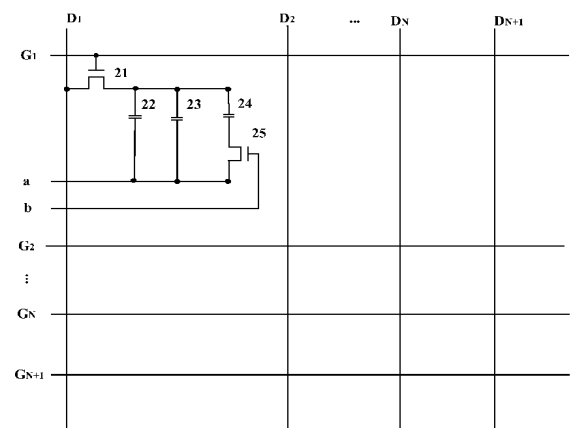


FIG 2