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(54) LIQUID CRYSTAL DISPLAY DEVICE AND DRIVE METHOD THEREFOR

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(73) Proprietor: **Shanghai Tianma Micro-Electronics
Co., Ltd.
201201 Shanghai (CN)**

(72) Inventors:
• **LV, Bojia
Shanghai 201201 (CN)**

- **QIAN, Dong
Shanghai 201201 (CN)**
- **KONG, Xiangzi
Shanghai 201201 (CN)**
- **GU, Hanyu
Beijing 100036 (CN)**

(74) Representative: **TBK
Bavariaring 4-6
80336 München (DE)**

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EP 2 818 916 B1

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Description

FIELD OF THE INVENTION

[0001] The present invention relates to flat panel display technologies, and in particular to a liquid crystal display device and a driving method of the liquid crystal display device.

BACKGROUND OF THE INVENTION

[0002] In a traditional liquid crystal display device, an electric field is used to control the rotation of liquid crystal molecules to display an image. As shown in Figure 1, the traditional liquid crystal display device 100 includes a liquid crystal panel 101, a plurality of data lines 102 formed on the liquid crystal panel 101, a plurality of gate lines 103, a plurality of common lines 104, a plurality of gate line trigger circuits (including a trigger circuit Gate 1, a trigger circuit Gate 2, a trigger circuit Gate 3, a trigger circuit Gate 4... a trigger circuit Gate n-1, and a trigger circuit Gate n), and a plurality of common line trigger circuits (including a trigger circuit COM 1, a trigger circuit COM 2, a trigger circuit COM 3, a trigger circuit COM 4... a trigger circuit COM n-1, and a trigger circuit COM n).

[0003] In Figure 1, a first direction is defined by the vertical direction, while a second direction is defined by the horizontal direction. The data lines 102 extend in the first direction, the gate lines 103 extend in the second direction and intersect with the data lines 102, and the common lines 104 are in parallel with the gate lines 103 and intersect with the data lines 102. The regions defined by the plurality of data lines 102 and the plurality of gate lines 103 are used as display regions. The liquid crystal panel 101 is provided with Thin-Film-Transistors (TFTs), each of which is used to drive a liquid crystal element C_{LC} located at the intersection. Furthermore, the liquid crystal panel 101 is equipped with storage capacitors C_{ST} for maintaining the voltages of the liquid crystal elements C_{LC} . The TFT is turned on if its gate is applied with a gate voltage by the gate line 103. At this time, if a drive voltage is provided to a pixel electrode 107 via the data line 102 and a common voltage is provided to a common electrode 108 via the common line 104, an electric field is generated on the liquid crystal element C_{LC} to change the arrangement of the liquid crystal molecules, so as to control the light transmittance of the liquid crystal element C_{LC} .

[0004] In the liquid crystal panel 101, one end of each of the gate lines 103 is connected to one gate line trigger circuit which is used to selectively provide a gate voltage to the gate line 103; and the other end of the gate line 103 is connected to a common line trigger circuit in the row of the gate line, and is used to trigger the common line trigger circuit and to selectively provide a common voltage to the common line 104 in the row. The gate line trigger circuit is located on one side of the display region and the common line trigger circuit is located on the other side of the display region. When a common voltage is

applied to the common electrode and a gate voltage is inputted to apply a data voltage to the pixel electrode 107, the charging of the storage capacitor C_{ST} is started, and the charging ends once the gate voltage is removed and the TFT is turned off. Here, the time for the charging of the storage capacitor C_{ST} is referred to as charging time. After the sufficient charging time, the voltage across the storage capacitors C_{ST} is equal to the difference between the data voltage and the common voltage. After the TFT is turned off, the storage capacitor C_{ST} maintains the rotation of the liquid crystal molecules with its voltage.

[0005] There exists latency for the gate voltage to be transferred from the leftmost pixel to the rightmost pixel. The gate voltage transferred to the rightmost pixel triggers the common line trigger circuit, and then the triggered common line trigger circuit provides the common voltage to the common line. Likewise, there exists latency for the common voltage to be transferred from the rightmost pixel to the leftmost pixel. All the above latency results in that, after a gate voltage is applied to the TFT, the common voltage is applied to the common electrode 108 after certain delay time. The above latency is an RC delay which is significantly impacted by resistance of the gate line and the common line as well as the related parasitic capacitance. Particularly, if the resistance is increased, the related parasitic capacitance is increased, and the latency is lengthened. The presence of the above latency shortens the charging time of the storage capacitors C_{ST} , as a result, the storage capacitors C_{ST} cannot be charged to a predetermined voltage value and hence the liquid crystal molecules cannot be rotated to predetermined positions to implement the intended display.

[0006] To maintain the polarities of the liquid crystal molecules, the liquid crystal display device may be driven by a driving approach with an unchanged common voltage and a driving approach with inverted common voltages. Figure 2 shows a time sequence for the driving approach with inverted common voltages. As shown in Figure 2, after each gate line is applied by a gate voltage, the applying of a common voltage to the common voltage line is later than the applying of the gate voltage because of the presence of the latency t , therefore the charging time T of the storage capacitors C_{ST} is shortened, such that the voltage of the storage capacitor C_{ST} cannot reach the difference between the data voltage and the common voltage, and hence the display effect is degraded.

[0007] With the increasing improved resolution of the liquid crystal display device, more and more gate lines and common lines are distributed on the liquid crystal panel, and the charging time for each storage capacitor C_{ST} under the same refresh frequency is increasingly shortened. Meanwhile, a high aperture ratio of the liquid crystal panel requires for thinner gate lines and common lines, which causes larger resistance and hence lengthened RC delay. Based on the above two reasons, the effective charging time for the storage capacitor C_{ST} is increasingly shortened, which has become a substantial problem degrading the resolution of the liquid crystal display device.

play device.

[0008] Therefore, it is necessary to develop a liquid crystal display device and a driving method of the liquid crystal display device, for reducing or eliminating the impact of the above latency to the storage capacitor C_{ST} . The document EP 1 796 073A2 discloses a display device including a plurality of gate lines transmitting gate signals wherein each gate signal has a gate-on voltage and a gate-off voltage, a plurality of data lines intersecting the gate lines and transmitting data voltages, a plurality of storage electrode lines extending in parallel to the gate lines and transmitting storage signals, a plurality of pixels arranged in a matrix wherein each pixel includes a switching element connected to a gate line and a data line, a liquid crystal capacitor connected to the switching element and a common voltage, a storage capacitor connected to the switching element and a storage electrode line, and a plurality of storage signal generators generating the storage signals based on the gate signals. The storage signal applied to each pixel has a changed voltage level immediately after the charging the data voltage into the liquid crystal capacitor and the storage capacitor is completed.

SUMMARY OF THE INVENTION

[0009] The present invention provides a liquid crystal display device and a driving method of the liquid crystal display device, for reducing or eliminating the impact of the above latency to the storage capacitor C_{ST} .

[0010] In order to solve the above technical problems, the present invention provides a liquid crystal display device, as defined in the claims.

[0011] In this invention, at least one dummy gate line is introduced, a gate line trigger circuit provides a gate voltage to a gate line corresponding to the gate line trigger circuit and triggers a succeeding gate line trigger circuit; meanwhile, the first common line trigger circuit is triggered by a signal transmitted via the dummy gate line, and each of remaining common line trigger circuits is triggered by one or more preceding gate line trigger circuits. That is, the common line trigger circuits are not triggered by the gate voltage of the same gate line, but triggered before the arrival of the gate voltage of this gate line. Therefore, the common voltage of the common line is applied to the common electrode before the gate voltage is applied, thereby ensuring that the charged capacitor is maintained in a charging state once the voltage of the pixel electrode is applied to the capacitor, such that the impact of the latency of the common voltage on the charging time is alleviated, and the display effect is improved.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012]

Figure 1 is a schematic view of a traditional liquid

crystal display device;

Figure 2 is a diagram showing a time sequence of a driving approach of the traditional liquid crystal display device;

Figure 3 is schematic view of a liquid crystal display device according to a first embodiment of the invention;

Figure 4 is a diagram showing a time sequence of a driving approach of the liquid crystal display device according to the first embodiment of the invention;

Figure 5 is a schematic view of a liquid crystal display device according to a second embodiment of the invention;

Figure 6 is a diagram showing a time sequence of a driving approach of the liquid crystal display device according to the second embodiment of the invention;

Figure 7 is a schematic view of a liquid crystal display device according to a third embodiment of the invention; and

Figure 8 is a diagram showing a time sequence of a driving approach of the liquid crystal display device according to the third embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0013] The concept of the present invention lies in adding at least one dummy gate line, one end of the last gate line is connected with the last gate line trigger circuit; one end of each of remaining gate lines is connected with a gate line trigger circuit corresponding to said each of remaining gate lines and the other end is connected with the succeeding gate line trigger circuit; and the first common line trigger circuit is connected with the dummy gate line, and each of remaining common line trigger circuits is connected with one or more preceding gate line trigger circuits. In this way, the gate line trigger circuit may provide a gate voltage to its corresponding gate line and trigger the gate line trigger circuit corresponding to the succeeding gate line; meanwhile, the first common line trigger circuit is triggered by a signal transmitted via the dummy gate line, and each of remaining common line trigger circuits is triggered by one or more preceding gate line trigger circuits. That is, the common line trigger circuits are not triggered by the gate voltage of the same gate line, but triggered before the arrival of the gate voltage of this gate line. Therefore, the common voltage of the common line is applied to the common electrode before the gate voltage is applied, thereby ensuring that the charged capacitor is maintained in a charging state once

the voltage of the pixel electrode is applied to the capacitor, such that the impact of the latency of the common voltage on the charging time is alleviated, and the display effect is improved.

[0014] In order for better understanding of the objects, solutions and advantages of the invention, the invention is further detailed in conjunction with Figures 3-8.

First Embodiment

[0015] Figure 3 is a schematic view showing a liquid crystal display device of the first embodiment of the invention. As shown in Figure 3, the liquid crystal display device 200 includes a liquid crystal panel 201, a plurality of data lines 202 formed on the liquid crystal panel 201, a plurality of gate lines 203, a plurality of common lines 204, a plurality of gate line trigger circuits (including a trigger circuit Gate 1, a trigger circuit Gate 2, a trigger circuit Gate 3, a trigger circuit Gate 4... a trigger circuit Gate m-1, and a trigger circuit Gate m), a plurality of common line trigger circuits (including a trigger circuit COM 1, a trigger circuit COM 2, a trigger circuit COM 3, a trigger circuit COM 4... a trigger circuit COM m-1, and a trigger circuit COM m), and a dummy gate line 207.

[0016] As shown in Figure 3, a first direction is defined by the vertical direction and a second direction is defined by the horizontal direction. The data lines 202 extend in the first direction, the gate lines 203 extend in the second direction and intersect with the data lines 202, and the dummy gate line 207 is in parallel with the gate lines 203. The liquid crystal panel 201 is provided with TFTs, each of which is configured to drive a liquid crystal element C_{LC} and a storage capacitor C_{ST} located at the intersection. The regions defined by the plurality of data lines 202 and the gate lines 203 are used as display regions. When a drive voltage is provided to a pixel electrode 208 via the data line 202 and a common voltage is provided to a common electrode 209 via the common line 204, an electric field is generated on the liquid crystal element C_{LC} to change the arrangement of the liquid crystal molecules, so as to control the light transmittance of the liquid crystal element C_{LC} .

[0017] One dummy gate line, m common lines, m gate lines, m common line trigger circuits, and m gate line trigger circuits are shown in Figure 3, wherein, m is an even number. Both gate line trigger circuits connected with even number gate lines and common line trigger circuits connected with odd number common lines are located on one side (e.g. the left side) of the display regions, and both gate line trigger circuits connected with odd number gate lines and common line trigger circuits connected with even number common lines are located on the other side (e.g. the right side) of the display regions.

[0018] Additionally, this embodiment is applicable to a liquid crystal display device in which a liquid crystal driving electric field is in parallel with the liquid crystal panel 201. Each common line trigger circuit is connected with

a first common voltage terminal 210 and a second common voltage terminal 211, which are used for providing a first common voltage V_{COMH} and a second common voltage V_{COML} to the common lines. For a liquid crystal display device adopting a driving approach with the inverted common voltages, the first common voltage and the second common voltage have the same magnitude but different polarities. For example, the first common voltage V_{COMH} is +5V and the second common voltage V_{COML} is -5V. Of course, in order to reduce power consumption, the first common voltage and the second common voltage may have different magnitudes, for example, the first common voltage V_{COMH} is +5V and the second common voltage V_{COML} is 0V, which is not limited in the invention.

[0019] As shown in Figure 3, one end of the dummy gate line 207 is connected to the first gate line trigger circuit, i.e. a trigger circuit Gate 1. One end of the trigger circuit Gate 1 which is connected to the first gate line is used to provide a gate voltage to the first gate line. Meanwhile, the other end of the dummy gate line 207 is connected to the first common line trigger circuit, i.e. a trigger circuit COM 1. The COM 1 trigger circuit is connected to the first common line to selectively provide a common electrode voltage to the first common line. The signal of the dummy gate line 207 is provided by the last gate line, and the first common line trigger circuit (i.e. the trigger circuit COM 1) is triggered by the gate voltage of the last gate line. The other end of the first gate line is connected to the second gate line trigger circuit, i.e. a trigger circuit Gate 2, and one end of the trigger circuit Gate 2 which is connected to the second gate line is used to selectively provide a gate voltage to the second gate line. Meanwhile, the first gate line trigger circuit is connected to the second common line trigger circuit, i.e. a trigger circuit COM 2, which is connected to the second common line to selectively provide a common electrode voltage to the second common line.

[0020] Likewise, the x th gate line trigger circuit is connected to one end of the x th gate line to selectively provide a gate voltage to the x th gate line, and the other end of the x th gate line is connected to the $(x+1)$ th gate line trigger circuit. The $(x+1)$ th gate line trigger circuit is meanwhile connected to the $(x+1)$ th gate line to selectively provide a gate voltage to the $(x+1)$ th gate line. Meanwhile, the x th gate line trigger circuit is connected to the $(x+1)$ th common line trigger circuit, and the $(x+1)$ th common line trigger circuit is connected to the $(x+1)$ th common line to selectively provide a common voltage to the $(x+1)$ th common line.

[0021] One end of the last gate line is connected to the last gate line trigger circuit, i.e. the trigger circuit Gate m, the other end of the last gate line is connected to the dummy gate line 207, to trigger the first gate line trigger circuit (i.e. the trigger circuit Gate 1) and the first common line trigger circuit (i.e. the trigger circuit COM 1).

[0022] Figure 4 is diagram showing a time sequence of a driving approach of the liquid crystal display device

according to the first embodiment of the invention. In the present embodiment, the liquid crystal display device is driven in the driving approach with the inverted common voltages. Particularly, Figure 4 is a diagram showing a driving time sequence of the liquid crystal display device of the present embodiment under the driving approach with the inverted common voltages. The driving approach of the liquid crystal display device of the present embodiment is described in detail in conjunction with Figures 3 and 4.

[0023] After the signal of the dummy gate line 207 is transferred to the first gate line trigger circuit (i.e. the trigger circuit Gate 1), the trigger circuit Gate 1 provides a gate voltage to the first gate line. Meanwhile, the signal of the dummy gate line 207 is also transferred to the first common line trigger circuit (i.e. the trigger circuit COM 1). After being triggered, the trigger circuit COM 1 selectively provides a common voltage to the first common line. That is, the trigger circuit Gate 1 and the trigger circuit COM 1 are triggered simultaneously without any trigger latency. When the gate voltage begins to be transferred along the first gate line, the common voltage is transferred along the first common line.

[0024] Next, the gate voltage begins to be transferred along the first gate line from left to right, and arrives at the rightmost end of the first gate line after latency t_1 . The other end of the first gate line is connected to the second gate line trigger circuit, i.e. the trigger circuit Gate 2. After being triggered, the trigger circuit Gate 2 provides a gate voltage to the second gate line. After being triggered, the trigger circuit Gate 1 also sends a trigger signal to the trigger circuit COM 2. After being triggered, the trigger circuit COM 2 in turn selectively provides a common voltage to the second common line. That is, after the trigger circuit COM 2 is triggered, the trigger circuit Gate 2 is not triggered until the latency t_1 elapses. That is, the trigger circuit COM 2 is triggered before the trigger circuit Gate 2 is triggered.

[0025] Likewise, after being triggered by the $(x-1)th$ gate line, the trigger circuit Gate x selectively provides a gate voltage to the xth gate line, and the gate voltage is transferred along the xth gate line and arrives at the other end of the xth gate line after the latency t_1 , to subsequently trigger the trigger circuit Gate $x+1$. Meanwhile, when the gate voltage begins to be transferred along the xth gate line, the trigger circuit Gate x triggers the trigger circuit Gate $x+1$ and the trigger circuit COM $x+1$ begins to selectively provide a common voltage to the $(x+1)th$ common line. That is, after the trigger circuit COM $x+1$ is triggered, the trigger circuit Gate $x+1$ is not triggered until the latency t_1 elapses. That is, the trigger circuit COM $x+1$ is triggered before the trigger circuit Gate $x+1$ is triggered.

[0026] At last, after the last gate line trigger circuit (i.e. the trigger circuit Gate m) is triggered, the trigger circuit Gate m also sends a trigger signal to the dummy gate line 207 as the trigger signal for both the trigger circuit Gate 1 and the trigger circuit COM 1. Subsequently, the

line-by-line triggering for the next period begins.

Second Embodiment

[0027] Figure 5 is schematic view of a liquid crystal display device of the second embodiment of the invention. As shown in Figure 5, the liquid crystal display device 300 includes a liquid crystal panel 301, a plurality of data lines 302 formed on the liquid crystal panel 301, a plurality of gate lines 303, a plurality of common lines 304, a plurality of gate line trigger circuits, a plurality of common line trigger circuits, and a plurality of dummy gate lines 307. In this embodiment, there are 5 dummy gate lines, i.e. dummy gate lines 307-1, 307-2, 307-3, 307-4, and 307-5; there are m gate lines, m common lines, $m+4$ gate line trigger circuits (i.e. a trigger circuit Gate -3, a trigger circuit Gate -2, a trigger circuit Gate -1, a trigger circuit Gate 0, a trigger circuit Gate 1, a trigger circuit Gate 2, a trigger circuit Gate 3, a trigger circuit Gate 4... and a trigger circuit Gate m), and m common line control circuits (including a trigger circuit COM 1, a trigger circuit COM 2, a trigger circuit COM 3, a trigger circuit COM 4, a trigger circuit COM 5... and a trigger circuit COM m).

[0028] Additionally, TFTs are provided on the liquid crystal panel 101 to drive liquid crystal elements C_{LC} and storage capacitors C_{ST} located at the intersections. When a drive voltage is provided to a pixel electrode 308 via the data line 302 and a common voltage is provided to the common electrode 309 via the common line 304, an electric field is generated on the liquid crystal element C_{LC} to change the arrangement of the liquid crystal molecules, so as to control the light transmittance of the liquid crystal element C_{LC} .

[0029] As shown in Figure 5, one end of the first dummy gate line 307-1 is connected to the first gate line trigger circuit, i.e. the trigger circuit Gate -3, which is connected to one end of the second dummy gate line 307-2. Meanwhile, the other end of the first dummy gate line 307-1 is connected to the first common line trigger circuit, i.e. the trigger circuit COM 1, which is connected to the first common line. The other end of the second dummy gate line 307-2 is connected to the second gate line trigger circuit, i.e. the trigger circuit Gate -2, which is also connected to one end of the third dummy gate line 307-3. The other end of the third dummy gate line 307-3 is connected to the third gate line trigger circuit, i.e. the trigger circuit Gate -1. In the same way, one end of each gate line or dummy gate line is connected to a gate line trigger circuit, and the other end of the gate line or dummy gate line is connected to the next gate line trigger circuit.

[0030] As shown in Figure 5, the first gate line trigger circuit (i.e. the trigger circuit Gate -3) is also connected to the second common line trigger circuit (i.e. the trigger circuit COM 2), and the second gate line trigger circuit (i.e. the trigger circuit Gate -2) is also connected to the third common line trigger circuit, i.e. the trigger circuit COM 3.

[0031] Likewise, each of the remaining common line

trigger circuits is connected with one or more preceding gate line trigger circuits. In this embodiment, each of the remaining common line trigger circuits is connected with one preceding gate line trigger circuit.

[0032] One end of the last gate line is connected with the last gate line trigger circuit (i.e. the trigger circuit Gate m), and the other end of the last gate line is connected with the first dummy gate line 307-1 to trigger the first gate line trigger circuit (i.e. the trigger circuit Gate -3) and the first common line trigger circuit (i.e. the trigger circuit COM 1).

[0033] In this embodiment, dummy gate lines 307 are formed above the display regions. In another embodiment, the dummy gate lines 307 are formed below the display regions.

[0034] Figure 6 is a diagram showing a time sequence of a driving approach of the liquid crystal display device according to the second embodiment of the invention. In this embodiment, the liquid crystal display device is driven in the driving approach with the inverted common voltages. Particularly, Figure 6 is a diagram showing a time sequence of the driving approach of the liquid crystal display device of the embodiment under the driving approach with the inverted common voltages.

[0035] The driving approach of the liquid crystal display device of the second embodiment is described in detail in conjunction with Figures 5 and 6.

[0036] After the signal of the first dummy gate line 307-1 is transferred to the first gate line trigger circuit (i.e. the trigger circuit Gate -3), the gate voltage of the trigger circuit Gate -3 triggers the second gate line trigger circuit (i.e. the trigger circuit Gate -2) through the second dummy gate line 307-2. In the same way, the gate voltage of the trigger circuit Gate 0 triggers the fifth gate line trigger circuit (i.e. the trigger circuit Gate 1) through the fifth dummy gate line 307-5. After being triggered, the trigger circuit Gate 1 provides a gate voltage to the first gate line, and the gate voltage begins to be transferred along the first gate line from left to right and arrives at the rightmost end of the first gate line after latency t_1 . The other end of the first gate line is connected to the trigger circuit Gate 2, which is triggered after certain charging time t_2 to provide a gate voltage to the second gate line. That is, the gate line trigger circuit (i.e. the trigger circuit Gate 1) connected with the first gate line will not be triggered until the gate voltage is transferred through 4 dummy gate lines, that is, the gate line trigger circuit connected with the first gate line will not be triggered until four multiples of the latency t_1 and the charging time t_2 elapses after the trigger circuit Gate -3 is triggered.

[0037] The signal of the first dummy gate line 307-1 triggers the first gate line trigger circuit (i.e. the trigger circuit Gate -3) and the first common line trigger circuit (i.e. the trigger circuit COM 1) simultaneously. Similarly, the Gate -3 trigger circuit, when providing the gate voltage to the second dummy gate line 307-2, simultaneously provides a trigger signal to the second common line trigger circuit (i.e. the trigger circuit COM 2), and the trigger

circuit COM 2 is triggered to provide a common voltage to the second common line. That is, the common line trigger circuit (i.e. the trigger circuit COM 1) connected with the first common line is triggered simultaneously while the trigger circuit Gate -3 is triggered.

[0038] In the same way, after the trigger circuit Gate x is triggered by the $(x-1)th$ gate line, the trigger circuit Gate x selectively provides a gate voltage to the xth gate line, and the gate voltage begins to be transferred along the xth gate line. The trigger circuit COM y is connected to and triggered by the trigger circuit Gate x. However, the trigger circuit COM y is triggered by the trigger signal of the trigger circuit Gate x that is delayed by n multiples of the latency. That is, the trigger circuit COM y is triggered earlier than the trigger circuit Gate y by the sum of n multiples of the latency t_1 and the charging time t_2 .

[0039] That is, the time when the common voltage of each common line is provided is earlier than the time when the gate voltage of the gate line corresponding to the common line by time of $n \cdot (t_1 + t_2)$. In this embodiment, $n=5$. Therefore, the time when the common voltage of each common line is provided is earlier than the time when the gate voltage of the gate line corresponding to the common line by time of $5 \cdot (t_1 + t_2)$.

[0040] In comparison with the first embodiment, the time when the common voltage of each common line is provided is much advanced with respect to the time when the gate voltage of the gate line is provided in the second embodiment, so as to ensure that the voltage of the common electrode 309 is always maintained at the common voltage during the time when the TFT is turned on. However, the time amount, by which the time when the common voltage is provided is earlier than the time when the gate voltage is provided, depends on the number of the dummy gate lines. That is, more dummy gate lines cause that the common line trigger circuit may be triggered much more earlier. However, the increased dummy gate lines occupy more space on the liquid crystal panel, and the area of the effective display regions is decreased accordingly. Therefore, the number of the dummy gate lines shall be selected to strike a balance between reducing the impact of the latency to the charging time and maintaining the area of the effective display regions as large as possible. Preferably, the number of the dummy gate lines is equal to or less than 5.

Third Embodiment

[0041] Figure 7 is a schematic view showing a liquid crystal display device of the third embodiment of the invention. As shown in Figure 7, the liquid crystal display device 400 includes a liquid crystal panel 401, a plurality of data lines 402 formed on the liquid crystal panel 401, a plurality of gate lines 403, a plurality of common lines 404, a plurality of gate line trigger circuits (including a trigger circuit Gate 1, a trigger circuit Gate 2, a trigger circuit Gate 3, a trigger circuit Gate 4... a trigger circuit Gate m-1, and a trigger circuit Gate m), a plurality of

common line trigger circuits (including a trigger circuit COM 1, a trigger circuit COM 2, a trigger circuit COM 3, a trigger circuit COM 4... a trigger circuit COM m-1, and a trigger circuit COMm), a dummy gate line 407 and a periodic pulse trigger circuit 412.

[0042] As shown in Figure 7, the data lines 402 extend in the first direction, the gate lines 403 extend in the second direction and intersect with the data lines 402, and the dummy gate line 407 is in parallel with the gate lines 403. TFTs are provided on the liquid crystal panel 401 to drive liquid crystal elements C_{LC} and storage capacitors C_{ST} located at the intersections. When a drive voltage is provided to a pixel electrode 408 via the data line 402 and a common voltage is provided to a common electrode 409 via the common line 404, an electric field is generated on the liquid crystal element C_{LC} to change the arrangement of the liquid crystal molecules, so as to control the light transmittance of the liquid crystal element C_{LC} .

[0043] As shown in Figure 7, the periodic pulse trigger circuit 412 is connected to one end of the dummy gate line 407, and the other end of the dummy gate line 407 is connected to the first common line trigger circuit, i.e. the trigger circuit COM 1, which is connected to the first common line to selectively provide a common electrode voltage to the first common line. Moreover, the periodic pulse trigger circuit 412 is connected to the first gate line trigger circuit, i.e. the trigger circuit Gate 1, which is connected to one end of the first gate line to provide a gate voltage to the first gate line. The periodic pulse trigger circuit 412 triggers both the first gate line trigger circuit (i.e. the trigger circuit Gate 1) and the first common line trigger circuit (i.e. the trigger circuit COM 1). The other end of the first gate line is connected to the second gate line trigger circuit, i.e. the trigger circuit Gate 2, which is connected to one end of the second gate line to selectively provide a gate voltage to the second gate line. Meanwhile, the first gate line trigger circuit is connected to the second common line trigger circuit, i.e. the trigger circuit COM 2, which is connected to the second common line to selectively provide a common electrode voltage to the second common line.

[0044] In the same way, the x th gate line trigger circuit is connected to one end of the x th gate line to selectively provide a gate voltage to the x th gate line, while the other end of the x th gate line is connected to the $(x+1)$ th gate line trigger circuit, which is meanwhile connected to the $(x+1)$ th gate line to selectively provide a gate voltage to the $(x+1)$ th gate line. Meanwhile, the x th gate line trigger circuit is connected to the $(x+1)$ th common line trigger circuit, and the $(x+1)$ th common line trigger circuit is connected to the $(x+1)$ th common line to selectively provide a common voltage to the $(x+1)$ th common line.

[0045] Finally, one end of the last gate line is connected to the last gate line trigger circuit, i.e. the trigger circuit Gate m.

[0046] In comparison with the first and second embodiments, both the first gate line trigger circuit and the first

common line trigger circuit are triggered by the periodic pulse trigger circuit 412 in the present embodiment. The time for scanning all the gate lines and the common lines for one time is equal to one period of the periodic pulse trigger circuit 412.

[0047] Figure 8 is a diagram showing a time sequence of a driving approach of the liquid crystal display device according to the third embodiment of the invention. The driving approach of the liquid crystal display device of this embodiment will be described in detail in conjunction with Figures 7 and 8.

[0048] After the signal of the periodic pulse trigger circuit 412 triggers the first gate line trigger circuit, i.e. the trigger circuit Gate 1, the trigger circuit Gate 1 in turn provides a gate voltage to the first gate line. Moreover, the signal of the periodic pulse trigger circuit 412 is transferred to the first common line trigger circuit (i.e. the trigger circuit COM 1) through the dummy gate line 407, and the triggered trigger circuit COM 1 selectively provides a common electrode voltage to the first common line.

[0049] Next, the gate voltage begins to be transferred along the first gate line from left to right, and arrives at the rightmost end of the first gate line. The other end of the first gate line is connected to the second gate line trigger circuit, i.e. the trigger circuit Gate 2, which provides a gate voltage to the second gate line after being triggered. After being triggered, the trigger circuit Gate 1 also sends a trigger signal to the trigger circuit COM 2, and the triggered trigger circuit COM 2 in turn selectively provides a common voltage to the second common line.

[0050] In the same way, after being triggered by the $(x-1)$ th gate line, the trigger circuit Gate x selectively provides a gate voltage to the x th gate line. The gate voltage is transferred along the x th gate line, and is transferred to the other end of the x th gate line, and then triggers the trigger circuit Gate $x+1$. Meanwhile, when the gate voltage begins to be transferred along the x th gate line, the trigger circuit Gate x triggers the trigger circuit COM $x+1$, which in turn begins to selectively provide a common voltage to the $(x+1)$ th common line.

[0051] At last, after being triggered, the last gate line trigger circuit (i.e. the trigger circuit Gate m) provides a gate voltage to the last gate line. Moreover, after being triggered, the last common line trigger circuit (i.e. the trigger circuit COMm) provides a common voltage to the last common line. One period of the periodic pulse trigger circuit 412 is finished once the scanning of both the last gate line and the last common line is completed.

[0052] Subsequently, the periodic pulse trigger circuit 412 proceeds to the next period, and the line-by-line triggering for the next period begins.

[0053] In this embodiment, the periodic pulse trigger circuit 412 is used for the triggering of both the first gate line trigger circuit and the first common line trigger circuit. Therefore, in comparison with the first and second embodiments, the pulse trigger circuit is used in the present embodiment for better control on products.

[0054] As can be seen, a plurality of dummy gate lines

are introduced in the present invention, a gate line trigger circuit is triggered by a dummy gate line or a gate line, and each gate line trigger circuit further triggers a certain succeeding common line trigger circuit. That is, the common line trigger circuit is not triggered by the gate voltage of the same gate line, but is triggered before the arrival of the gate voltage of the gate line. Therefore, the common voltage of the common line may be applied to the common line before the gate voltage is applied, thus ensuring that the charged capacitor is always maintained at a charged state after the pixel electrode voltage is applied, such that the impact of the latency of the common voltage to the charging time is reduced or eliminated.

[0055] It should be noted that, embodiments are described in a step-up way in the description, that is, differences of each embodiment from the previous embodiments are described, but reference is made to the previous embodiments for any identical or similar parts of said each embodiment with respect to the previous embodiments.

[0056] Obviously, various modifications and variations may be made by those skilled in the art without departing from the principle and scope of the invention. Thus, all these modifications and variations are intended to be included in this invention if they fall within the scope of the claims of the invention and their equivalents.

Claims

1. A liquid crystal display device (200, 300, 400), comprising:

a plurality of pixels in a two-dimensional arrangement in a first direction and a second direction, each pixel comprising a pixel electrode (208), a common electrode (209) and a TFT, wherein a first terminal of the TFT is connected to the pixel electrode;

a plurality of data lines (202, 302, 402) extending in the first direction, each data line being configured to provide a drive voltage via a second terminal of the TFT to the pixel electrode of pixels arranged in the first direction;

a plurality of gate lines (203, 303, 403) extending in the second direction and intersecting with the plurality of data lines, each gate line being configured to provide a gate voltage to a gate terminal of the TFT of pixels arranged in the second direction;

a plurality of common lines (204, 304, 404) extending in parallel with the plurality of gate lines and intersecting with the plurality of data lines, each common line being configured to provide a common voltage to the common electrodes of pixels arranged in the second direction;

at least one dummy gate line (207, 307, 407) extending in parallel with the gate lines;

a plurality of gate line trigger circuits for selectively providing a gate voltage to a corresponding gate line and the at least one dummy gate line; and

a plurality of common line trigger circuits for selectively providing a common voltage to a corresponding common line,

characterized in that

one end of the last gate line in the first direction is connected with a last gate line trigger circuit corresponding to the last gate line in the first direction, and the other end of the last gate line is connected with the first dummy gate line of the at least one dummy gate line,

one end of each of the remaining gate lines is connected with a gate line trigger circuit corresponding to a respective one of the remaining gate lines in the first direction, and the other end of each of the remaining gate lines is connected with the succeeding gate line trigger circuit corresponding to a succeeding one of the remaining gate lines in the first direction,

one end of the first dummy gate line of the at least one dummy gate line is connected with the last gate line in the first direction, and the other end of the first dummy gate line of the at least one dummy gate line is connected with a first gate line trigger circuit corresponding to the first gate line in the first direction and a first common line trigger circuit corresponding to the first common line in the first direction, and

each of the remaining common line trigger circuits is connected with one preceding gate line trigger circuit corresponding to a preceding gate line in the first direction,

wherein the last gate line trigger circuit is configured to provide a gate voltage, via the last gate line in the first direction, to the first dummy gate line to trigger the first gate line trigger circuit and the first common line trigger circuit, and wherein each of the remaining gate line trigger circuits is configured to trigger a succeeding common line trigger circuit corresponding to a succeeding common line in the first direction.

2. The liquid crystal display device of claim 1, wherein pixel regions defined by the plurality of data lines and the plurality of gate lines are display regions.

3. The liquid crystal display device of claim 2, wherein

both the gate line trigger circuits connected with even number gate lines and the common line trigger circuits connected with odd number common lines are located on one side of the display regions, or

both the gate line trigger circuits connected with odd number gate lines and the common line trig-

ger circuits connected with even number common lines are located on the other side of the display regions.

4. The liquid crystal display device of claim 1, wherein, if the at least one dummy gate line consists of one dummy gate line, the other end of the last gate line in the first direction is connected with the dummy gate line. 5
5. The liquid crystal display device of claim 1, wherein, if the at least one dummy gate line consists of a plurality of dummy gate lines, the other end of the last gate line in the first direction is connected with the first dummy gate line, and one end of each of remaining dummy gate lines in the first direction is connected with a gate line trigger circuit corresponding to said each of remaining dummy gate lines in the first direction, and the other end of said each of the remaining dummy gate lines is connected with the succeeding gate line trigger circuit corresponding to a succeeding one of the remaining gate lines in the first direction. 10
6. The liquid crystal display device of claim 1, wherein, if the at least one dummy gate line consists of one dummy gate line, said one dummy gate line is connected with a periodic pulse trigger circuit (412). 15
7. The liquid crystal display device of claim 1, wherein, if the at least one dummy gate line consists of a plurality of dummy gate lines, the first dummy gate line in the first direction is connected with a periodic pulse trigger circuit, one end of each of remaining dummy gate lines in the first direction is connected with a gate line trigger circuit corresponding to said each of remaining dummy gate lines in the first direction and the other end of said each of the remaining dummy gate lines in the first direction is connected with a succeeding gate line trigger circuit corresponding to a succeeding one of the remaining gate lines in the first direction. 20
8. The liquid crystal display device of claim 1, further comprising a first common voltage terminal (210, 410) and a second common voltage terminal (211, 411), which are connected with the common line trigger circuit and used for providing the common lines with a first common voltage and a second common voltage. 25
9. The liquid crystal display device of claim 8, wherein the first common voltage and the second common voltage have the same magnitude and different polarities, or the magnitude of the first common voltage or the second common voltage is zero. 30

10. A driving method of a liquid crystal display device of any one of claims 1 to 9, comprising:

providing, by a gate line trigger circuit, a gate voltage to a gate line corresponding to the gate line trigger circuit, and triggering a succeeding gate line trigger circuit corresponding to a succeeding one of the remaining gate lines in the first direction; and triggering the first common line trigger circuit in the first direction by a signal transmitted by a dummy gate line, wherein each of remaining common line trigger circuits in the first direction is triggered by one or more preceding gate line trigger circuits corresponding to preceding gate lines in the first direction. 35

11. The driving method of a liquid crystal display device of claim 10, wherein, if only one dummy gate line is present, the other end of the last gate line in the first direction is connected with the dummy gate line, and a gate voltage of the last gate line in the first direction is used to trigger the first common line trigger circuit in the first direction. 40

12. The driving method of a liquid crystal display device of claim 10, wherein, if a plurality of the dummy gate lines are present, the other end of the last gate line in the first direction is connected with the first dummy gate line in the first direction, and a gate voltage of the last gate line in the first direction is used to trigger the first common line trigger circuit in the first direction; and one end of each of remaining dummy gate lines in the first direction is connected with a gate line trigger circuit corresponding to said each of remaining dummy gate lines in the first direction, and the other end of said each of the remaining dummy gate lines in the first direction is connected with a succeeding gate line trigger circuit corresponding to a succeeding one of the remaining gate lines in the first direction, so that the succeeding gate line trigger circuit corresponding to the succeeding one of the remaining gate lines in the first direction is triggered by its preceding gate line trigger circuit corresponding to preceding gate lines in the first direction. 45

13. The driving method of a liquid crystal display device of claim 10, wherein, if only one dummy gate line is present, the dummy gate line is connected with a periodic pulse trigger circuit, which is used to trigger the first common line trigger circuit in the first direction. 50

14. The driving method of a liquid crystal display device of claim 10, wherein, if a plurality of the dummy gate lines are present, the first dummy gate line in the first direction is connected with a periodic pulse trigger circuit, which is used to trigger the first common line 55

trigger circuit in the first direction; and one end of each of remaining dummy gate lines in the first direction is connected with a gate line trigger circuit corresponding to said each of remaining dummy gate lines in the first direction, and the other end of said each of the remaining dummy gate lines in the first direction is connected with a succeeding gate line trigger circuit corresponding to a succeeding one of the remaining gate lines in the first direction, so that the succeeding gate line trigger circuit corresponding to a succeeding one of the remaining gate lines in the first direction is triggered by its preceding gate line trigger circuit corresponding to the preceding gate line in the first direction.

15. The driving method of a liquid crystal display device of claim 10, further comprising a first common voltage terminal and a second common voltage terminal, which are connected with the common line trigger circuit and used for selectively providing the common lines with a first common voltage and a second common voltage.

Patentansprüche

1. Flüssigkristallanzeigevorrichtung (200, 300, 400) mit:

einer Vielzahl von Pixel in einer zweidimensionalen Anordnung in einer ersten Richtung und einer zweiten Richtung, wobei jedes Pixel eine Pixelelektrode (208), eine gemeinsame Elektrode (209) und einen TFT aufweist, wobei ein erster Anschluss von dem TFT mit der Pixelelektrode verbunden ist;

einer Vielzahl von Datenleitungen (202, 302, 402), die sich in der ersten Richtung erstrecken, wobei jede Datenleitung konfiguriert ist zum Bereitstellen einer Ansteuerspannung, über einen zweiten Anschluss von dem TFT, an die Pixelelektrode von in der ersten Richtung angeordneten Pixel;

einer Vielzahl von Gateleitungen (203, 303, 403), die sich in der zweiten Richtung erstrecken und mit der Vielzahl von Datenleitungen überkreuzen, wobei jede Gateleitung konfiguriert ist zum Bereitstellen einer Gatespannung an einen Gateanschluss von dem TFT von in der zweiten Richtung angeordneten Pixel;

einer Vielzahl von gemeinsamen Leitungen (204, 304, 404), die sich parallel zu der Vielzahl von Gateleitungen erstrecken und mit der Vielzahl von Datenleitungen überkreuzen, wobei jede gemeinsame Leitung konfiguriert ist zum Bereitstellen einer gemeinsamen Spannung an die gemeinsamen Elektroden von in der zweiten Richtung angeordneten Pixel;

zumindest einer Dummygateleitung (207, 307, 407), die sie parallel zu den Gateleitungen erstreckt;

einer Vielzahl von Gateleitung-Triggerschaltungen zum selektiven Bereitstellen einer Gatespannung an eine korrespondierende Gateleitung und die zumindest eine Dummygateleitung; und

einer Vielzahl von Gemeinsame-Leitung-Triggerschaltungen zum selektiven Bereitstellen einer gemeinsamen Spannung an eine korrespondierende gemeinsame Leitung,

dadurch gekennzeichnet, dass

ein Ende der letzten Gateleitung in der ersten Richtung mit einer letzten Gateleitung-Triggerschaltung verbunden ist, die mit der letzten Gateleitung in der ersten Richtung korrespondiert, und das andere Ende der letzten Gateleitung mit der ersten Dummygateleitung von der zumindest einen Dummygateleitung verbunden ist,

ein Ende von jeder der übrigen Gateleitungen mit einer Gateleitung-Triggerschaltung verbunden ist, die mit einer jeweiligen der übrigen Gateleitungen in der ersten Richtung korrespondiert, und das andere Ende von jeder der übrigen Gateleitungen mit der nachfolgenden Gateleitung-Triggerschaltung verbunden ist, die mit einer nachfolgenden der übrigen Gateleitungen in der ersten Richtung korrespondiert,

ein Ende der ersten Dummygateleitung von der zumindest einen Dummygateleitung mit der letzten Gateleitung in der ersten Richtung verbunden ist, und das andere Ende der ersten Dummygateleitung von der zumindest einen Dummygateleitung mit einer ersten Gateleitung-Triggerschaltung, die mit der ersten Gateleitung in der ersten Richtung korrespondiert, und einer ersten Gemeinsame-Leitung-Triggerschaltung, die mit der ersten gemeinsamen Leitung in der ersten Richtung korrespondiert, verbunden ist, und

jede der übrigen Gemeinsame-Leitung-Triggerschaltungen mit einer vorhergehenden Gateleitung-Triggerschaltung verbunden ist, die mit einer vorhergehenden Gateleitung in der ersten Richtung korrespondiert,

wobei die letzte Gateleitung-Triggerschaltung konfiguriert ist zum Bereitstellen einer Gatespannung, über die letzte Gateleitung in der ersten Richtung, an die erste Dummygateleitung, um die erste Gateleitung-Triggerschaltung und die erste Gemeinsame-Leitung-Triggerschaltung zu triggern, und

wobei jede der übrigen Gateleitung-Triggerschaltungen konfiguriert ist, um eine nachfolgende Gemeinsame-Leitung-Triggerschaltung zu triggern, die mit einer nachfolgenden gemein-

samen Leitung in der ersten Richtung korrespondiert.

2. Flüssigkristallanzeigevorrichtung gemäß Anspruch 1, wobei Pixelbereiche, die durch die Vielzahl von Datenleitungen und die Vielzahl von Gateleitungen definiert sind, Anzeigebereiche sind. 5
3. Flüssigkristallanzeigevorrichtung gemäß Anspruch 2, wobei 10

sowohl die Gateleitung-Triggerschaltungen, die mit geradzahligem Gateleitungen verbunden sind, als auch die Gemeinsame-Leitung-Triggerschaltungen, die mit ungeradzahligem gemeinsamen Leitungen verbunden sind, auf einer Seite der Anzeigebereiche liegen, oder

sowohl die Gateleitung-Triggerschaltungen, die mit ungeradzahligem Gateleitungen verbunden sind, als auch die Gemeinsame-Leitung-Triggerschaltungen, die mit geradzahligem gemeinsamen Leitungen verbunden sind, auf der anderen Seite der Anzeigebereiche liegen. 15 20
4. Flüssigkristallanzeigevorrichtung gemäß Anspruch 1, wobei, wenn die zumindest eine Dummygateleitung aus einer Dummygateleitung besteht, das andere Ende der letzten Gateleitung in der ersten Richtung mit der Dummygateleitung verbunden ist. 25 30
5. Flüssigkristallanzeigevorrichtung gemäß Anspruch 1, wobei, wenn die zumindest eine Dummygateleitung aus einer Vielzahl von Dummygateleitungen besteht, das andere Ende der letzten Gateleitung in der ersten Richtung mit der ersten Dummygateleitung verbunden ist, und ein Ende von jeder von übrigen Dummygateleitungen in der ersten Richtung mit einer Gateleitung-Triggerschaltung verbunden ist, die mit der Besagten von jeder von übrigen Dummygateleitungen in der ersten Richtung korrespondiert, und das andere Ende der Besagten von jeder der übrigen Dummygateleitungen mit der nachfolgenden Gateleitung-Triggerschaltung verbunden ist, die mit einer nachfolgenden der übrigen Gateleitungen in der ersten Richtung korrespondiert. 35 40 45
6. Flüssigkristallanzeigevorrichtung gemäß Anspruch 1, wobei, wenn die zumindest eine Dummygateleitung aus einer Dummygateleitung besteht, die eine Dummygateleitung mit einer Periodenpuls-Triggerschaltung (412) verbunden ist. 50
7. Flüssigkristallanzeigevorrichtung gemäß Anspruch 1, wobei, wenn die zumindest eine Dummygateleitung aus einer Vielzahl von Dummygateleitungen besteht, die erste Dummygateleitung in der ersten Richtung mit einer Periodenpuls-Triggerschaltung verbunden ist, ein Ende von jeder von übrigen Dum-

mygateleitungen in der ersten Richtung mit einer Gateleitung-Triggerschaltung verbunden ist, die mit der Besagten von jeder von übrigen Dummygateleitungen in der ersten Richtung korrespondiert, und das andere Ende der Besagten von jeder der übrigen Dummygateleitungen in der ersten Richtung mit einer nachfolgenden Gateleitung-Triggerschaltung verbunden ist, die mit einer nachfolgenden der übrigen Gateleitungen in der ersten Richtung korrespondiert.

8. Flüssigkristallanzeigevorrichtung gemäß Anspruch 1, zusätzlich mit einem ersten Gemeinsame-Spannung-Anschluss (210, 410) und einem zweiten Gemeinsame-Spannung-Anschluss (211, 411), die mit der Gemeinsame-Leitung-Triggerschaltung verbunden sind, und die zum Versorgen der gemeinsamen Leitungen mit einer ersten gemeinsamen Spannung und einer zweiten gemeinsamen Spannung verwendet werden. 15 20
9. Flüssigkristallanzeigevorrichtung gemäß Anspruch 8, wobei

die erste gemeinsame Spannung und die zweite gemeinsame Spannung den gleichen Betrag und unterschiedliche Polaritäten aufweisen, oder

der Betrag der ersten gemeinsamen Spannung oder der zweiten gemeinsamen Spannung Null ist. 25
10. Ansteuerungsverfahren einer Flüssigkristallanzeigevorrichtung gemäß einem der Ansprüche 1 bis 9, mit

Bereitstellen, durch eine Gateleitung-Triggerschaltung, einer Gatespannung an eine Gateleitung, die mit der Gateleitung-Triggerschaltung korrespondiert, und Triggern einer nachfolgenden Gateleitung-Triggerschaltung, die mit einer nachfolgenden der übrigen Gateleitungen in der ersten Richtung korrespondiert; und

Triggern der ersten Gemeinsame-Leitung-Triggerschaltung in der ersten Richtung durch ein Signal, das durch eine Dummygateleitung übertragen wird, wobei jede von übrigen Gemeinsame-Leitung-Triggerschaltungen in der ersten Richtung durch ein oder mehr vorhergehende Gateleitung-Triggerschaltungen getriggert werden, die mit vorhergehenden Gateleitungen in der ersten Richtung korrespondieren. 30 35 40 45 50
11. Ansteuerungsverfahren einer Flüssigkristallanzeigevorrichtung gemäß Anspruch 10, wobei, wenn nur eine Dummygateleitung vorhanden ist, das andere Ende der letzten Gateleitung in der ersten Richtung mit der Dummygateleitung verbunden ist, und eine Gatespannung der letzten Gateleitung in der ersten

Richtung verwendet wird, um die erste Gemeinsame-Leitung-Triggerschaltung in der ersten Richtung zu triggern.

12. Ansteuerungsverfahren einer Flüssigkristallanzeigevorrichtung gemäß Anspruch 10, wobei, wenn eine Vielzahl der Dummygateleitungen vorhanden sind, das andere Ende der letzten Gateleitung in der ersten Richtung mit der ersten Dummygateleitung in der ersten Richtung verbunden ist, und eine Gatespannung der letzten Gateleitung in der ersten Richtung verwendet wird, um die erste Gemeinsame-Leitung-Triggerschaltung in der ersten Richtung zu triggern; und ein Ende von jeder von übrigen Dummygateleitungen in der ersten Richtung mit einer Gateleitung-Triggerschaltung verbunden ist, die mit der Besagten von jeder von übrigen Dummygateleitungen in der ersten Richtung korrespondiert, und das andere Ende der Besagten von jeder der übrigen Dummygateleitung in der ersten Richtung mit einer nachfolgenden Gateleitung-Triggerschaltung verbunden ist, die mit einer nachfolgenden der übrigen Gateleitungen in der ersten Richtung korrespondiert, so dass die nachfolgende Gateleitung-Triggerschaltung, die mit der nachfolgenden der übrigen Gateleitungen in der ersten Richtung korrespondiert, durch ihre vorhergehende Gateleitung-Triggerschaltung, die mit den vorhergehenden Gateleitungen in der ersten Richtung korrespondiert, getriggert wird.
13. Ansteuerungsverfahren einer Flüssigkristallanzeigevorrichtung gemäß Anspruch 10, wobei, wenn nur eine Dummygateleitung vorhanden ist, die Dummygateleitung mit einer Periodenpuls-Triggerschaltung verbunden ist, die verwendet wird, um die erste Gemeinsame-Leitung-Triggerschaltung in der ersten Richtung zu triggern.
14. Ansteuerungsverfahren einer Flüssigkristallanzeigevorrichtung gemäß Anspruch 10, wobei, wenn eine Vielzahl der Dummygateleitungen vorhanden sind, die erste Dummygateleitung in der ersten Richtung mit einer Periodenpuls-Triggerschaltung verbunden ist, die verwendet wird, um die erste Gemeinsame-Leitung-Triggerschaltung in der ersten Richtung zu triggern; und ein Ende von jeder von übrigen Dummygateleitungen in der ersten Richtung mit einer Gateleitung-Triggerschaltung verbunden ist, die mit der Besagten von jeder von übrigen Dummygateleitungen in der ersten Richtung korrespondiert, und das andere Ende der Besagten von jeder der übrigen Dummygateleitungen in der ersten Richtung mit einer nachfolgenden Gateleitung-Triggerschaltung verbunden ist, die mit einer nachfolgenden der übrigen Gateleitungen in der ersten Richtung korrespondiert, so dass die nachfolgende Gateleitung-Triggerschaltung, die mit einer nachfolgenden der

übrigen Gateleitungen in der ersten Richtung korrespondiert, durch ihre vorhergehende Gateleitung-Triggerschaltung, die mit der vorhergehenden Gateleitungen in der ersten Richtung korrespondiert, getriggert wird.

15. Ansteuerungsverfahren einer Flüssigkristallanzeigevorrichtung gemäß Anspruch 10, zusätzlich mit einem ersten Gemeinsame-Spannung-Anschluss und einem zweiten Gemeinsame-Spannung-Anschluss, die mit der Gemeinsame-Leitung-Triggerschaltung verbunden sind, und die zum selektiven Versorgen der gemeinsamen Leitungen mit einer ersten gemeinsamen Spannung und einer zweiten gemeinsamen Spannung verwendet werden.

Revendications

1. Dispositif d'affichage à cristaux liquides (200, 300, 400), comprenant :

une pluralité de pixels en un agencement bidimensionnel dans une première direction et une deuxième direction, chaque pixel comprenant une électrode de pixel (208), une électrode commune (209) et un TFT, dans lequel une première borne du TFT est connectée à l'électrode de pixel ;

une pluralité de lignes de données (202, 302, 402) s'étendant dans la première direction, chaque ligne de données étant configurée pour fournir une tension de commande par l'intermédiaire d'une deuxième borne du TFT à l'électrode de pixel des pixels agencés dans la première direction ;

une pluralité de lignes de grille (203, 303, 403) s'étendant dans la deuxième direction et croisant la pluralité de lignes de données, chaque ligne de grille étant configurée pour fournir une tension de grille à une borne de grille du TFT des pixels agencés dans la deuxième direction ; une pluralité de lignes communes (204, 304, 404) s'étendant parallèlement à la pluralité de lignes de grille et croisant la pluralité de lignes de données, chaque ligne commune étant configurée pour fournir une tension commune aux électrodes communes des pixels agencés dans la deuxième direction ;

au moins une ligne de grille fictive (207, 307, 407) s'étendant parallèlement aux lignes de grille ;

une pluralité de circuits de déclenchement de ligne de grille pour fournir de manière sélective une tension de grille à une ligne de grille correspondante et à ladite au moins une ligne de grille fictive ; et

une pluralité de circuits de déclenchement de

ligne commune pour fournir de manière sélective une tension commune à une ligne commune correspondante,

caractérisé en ce que

une extrémité de la dernière ligne de grille dans la première direction est connectée à un circuit de déclenchement de dernière ligne de grille correspondant à la dernière ligne de grille dans la première direction, et l'autre extrémité de la dernière ligne de grille est connectée à la première ligne de grille fictive de ladite au moins une ligne de grille fictive,

une extrémité de chacune des lignes de grille restantes est connectée à un circuit de déclenchement de ligne de grille correspondant à l'une respective des lignes de grille restantes dans la première direction, et l'autre extrémité de chacune des lignes de grille restantes est connectée au circuit de déclenchement de ligne de grille suivant correspondant à une ligne suivante parmi les lignes de grille restantes dans la première direction,

une extrémité de la première ligne de grille fictive de ladite au moins une ligne de grille fictive est connectée à la dernière ligne de grille dans la première direction, et l'autre extrémité de la première ligne de grille fictive de ladite au moins une ligne de grille fictive est connectée à un circuit de déclenchement de première ligne de grille correspondant à la première ligne de grille dans la première direction et à un circuit de déclenchement de première ligne commune correspondant à la première ligne commune dans la première direction, et

chacun des circuits de déclenchement de ligne commune restants est connecté à un circuit de déclenchement de ligne de grille précédente correspondant à une ligne de grille précédente dans la première direction,

dans lequel le circuit de déclenchement de dernière ligne de grille est configuré pour fournir une tension de grille, par l'intermédiaire de la dernière ligne de grille dans la première direction, à la première ligne de grille fictive pour déclencher le circuit de déclenchement de première ligne de grille et le circuit de déclenchement de première ligne commune, et

dans lequel chacun des circuits de déclenchement de ligne de grille restants est configuré pour déclencher un circuit de déclenchement de ligne commune suivant correspondant à une ligne commune suivante dans la première direction.

2. Dispositif d'affichage à cristaux liquides selon la revendication 1, dans lequel les régions de pixels définies par la pluralité de lignes de données et la pluralité de lignes de grille sont des régions d'affichage.

3. Dispositif d'affichage à cristaux liquides selon la revendication 2, dans lequel

les circuits de déclenchement de ligne de grille connectés à des lignes de grille de numéro pair et les circuits de déclenchement de ligne commune connectés aux lignes communes de numéro impair sont tous situés d'un côté des régions d'affichage, ou les circuits de déclenchement de ligne de grille connectés aux lignes de grille de numéro impair et les circuits de déclenchement de ligne commune connectés aux lignes communes de numéro pair sont tous situés de l'autre côté des régions d'affichage.

4. Dispositif d'affichage à cristaux liquides selon la revendication 1, dans lequel, si ladite au moins une ligne de grille fictive consiste en une ligne de grille fictive, l'autre extrémité de la dernière ligne de grille dans la première direction est connectée à la ligne de grille fictive.

5. Dispositif d'affichage à cristaux liquides selon la revendication 1, dans lequel, si ladite au moins une ligne de grille fictive consiste en une pluralité de lignes de grille fictives, l'autre extrémité de la dernière ligne de grille dans la première direction est connectée à la première ligne de grille fictive, et une extrémité de chacune des lignes de grille fictives restantes dans la première direction est connectée à un circuit de déclenchement de ligne de grille correspondant à chacune desdites lignes de grille fictives restantes dans la première direction, et l'autre extrémité de chacune desdites lignes de grille fictives restantes est connectée au circuit de déclenchement de ligne de grille suivant correspondant à une ligne suivante parmi les lignes de grille restantes dans la première direction.

6. Dispositif d'affichage à cristaux liquides selon la revendication 1, dans lequel, si ladite au moins une ligne de grille fictive consiste en une ligne de grille fictive, ladite une ligne de grille fictive est connectée à un circuit de déclenchement d'impulsions périodiques (412).

7. Dispositif d'affichage à cristaux liquides selon la revendication 1, dans lequel, si ladite au moins une ligne de grille fictive consiste en une pluralité de lignes de grille fictives, la première ligne de grille fictive dans la première direction est connectée à un circuit de déclenchement d'impulsions périodiques, une extrémité de chacune des lignes de grille fictives restantes dans la première direction est connectée à un circuit de déclenchement de ligne de grille correspondant à chacune desdites lignes de grille fictives restantes dans la première direction et l'autre extrémité de chacune desdites lignes de grille fictives restantes dans la première direction est connectée à un circuit de déclenchement de ligne de grille

suyant correspondant à une ligne suivante parmi les lignes de grille restantes dans la première direction.

8. Dispositif d'affichage à cristaux liquides selon la revendication 1, comprenant en outre une première borne de tension commune (210, 410) et une deuxième borne de tension commune (211, 411), qui sont connectées au circuit de déclenchement de ligne commune et utilisées pour fournir aux lignes communes une première tension commune et une deuxième tension commune. 5
9. Dispositif d'affichage à cristaux liquides selon la revendication 8, dans lequel la première tension commune et la deuxième tension commune ont la même amplitude et différentes polarités, ou l'amplitude de la première tension commune ou de la deuxième tension commune est nulle. 10 15 20
10. Procédé de commande d'un dispositif d'affichage à cristaux liquides selon l'une quelconque des revendications 1 à 9, comprenant : 25
la fourniture, par un circuit de déclenchement de ligne de grille, d'une tension de grille à une ligne de grille correspondant au circuit de déclenchement de ligne de grille, et le déclenchement d'un circuit de déclenchement de ligne de grille suivant correspondant à une ligne suivante parmi les lignes de grille restantes dans la première direction ; et 30
le déclenchement du circuit de déclenchement de première ligne commune dans la première direction par un signal transmis par une ligne de grille fictive, dans lequel chacun des circuits de déclenchement de ligne commune restants dans la première direction est déclenché par un ou plusieurs circuits de déclenchement de ligne de grille précédents correspondant à des lignes de grille précédentes dans la première direction. 35 40
11. Procédé de commande d'un dispositif d'affichage à cristaux liquides selon la revendication 10, dans lequel, si une seule ligne de grille fictive est présente, l'autre extrémité de la dernière ligne de grille dans la première direction est connectée à la ligne de grille fictive, et une tension de grille de la dernière ligne de grille dans la première direction est utilisée pour déclencher le circuit de déclenchement de première ligne commune dans la première direction. 45 50
12. Procédé de commande d'un dispositif d'affichage à cristaux liquides selon la revendication 10, dans lequel, si une pluralité des lignes de grille fictives sont présentes, l'autre extrémité de la dernière ligne de grille dans la première direction est connectée à la 55

première ligne de grille fictive dans la première direction, et une tension de grille de la dernière ligne de grille dans la première direction est utilisée pour déclencher le circuit de déclenchement de première ligne commune dans la première direction ; et une extrémité de chacune des lignes de grille fictives restantes dans la première direction est connectée à un circuit de déclenchement de ligne de grille correspondant à chacune desdites lignes de grille fictives restantes dans la première direction, et l'autre extrémité de chacune desdites lignes de grille fictives restantes dans la première direction est connectée à un circuit de déclenchement de ligne de grille suivant correspondant à une ligne suivante parmi les lignes de grille restantes dans la première direction, de sorte que le circuit de déclenchement de ligne de grille suivant correspondant à la ligne suivante parmi les lignes de grille restantes dans la première direction est déclenché par son circuit de déclenchement de ligne de grille précédent correspondant à la ligne de grille précédente dans la première direction.

13. Procédé de commande d'un dispositif d'affichage à cristaux liquides selon la revendication 10, dans lequel, si une seule ligne de grille fictive est présente, la ligne de grille fictive est connectée à un circuit de déclenchement d'impulsions périodiques, qui est utilisé pour déclencher le circuit de déclenchement de première ligne commune dans la première direction. 25
14. Procédé de commande d'un dispositif d'affichage à cristaux liquides selon la revendication 10, dans lequel, si une pluralité des lignes de grille fictives sont présentes, la première ligne de grille fictive dans la première direction est connectée à un circuit de déclenchement d'impulsions périodiques, qui est utilisé pour déclencher le circuit de déclenchement de première ligne commune dans la première direction ; et une extrémité de chacune des lignes de grille fictives restantes dans la première direction est connectée à un circuit de déclenchement de ligne de grille correspondant à chacune desdites lignes de grille fictives restantes dans la première direction, et l'autre extrémité de chacune desdites lignes de grille fictives restantes dans la première direction est connectée à un circuit de déclenchement de ligne de grille suivant correspondant à une ligne suivante parmi les lignes de grille restantes dans la première direction, de sorte que le circuit de déclenchement de ligne de grille suivant correspondant à une ligne suivante parmi les lignes de grille restantes dans la première direction est déclenché par son circuit de déclenchement de ligne de grille précédent correspondant à la ligne de grille précédente dans la première direction. 35 40 45 50 55
15. Procédé de commande d'un dispositif d'affichage à cristaux liquides selon la revendication 10, compre-

nant en outre une première borne de tension commune et une deuxième borne de tension commune, qui sont connectées au circuit de déclenchement de ligne commune et utilisées pour fournir de manière sélective aux lignes communes une première tension commune et une deuxième tension commune.

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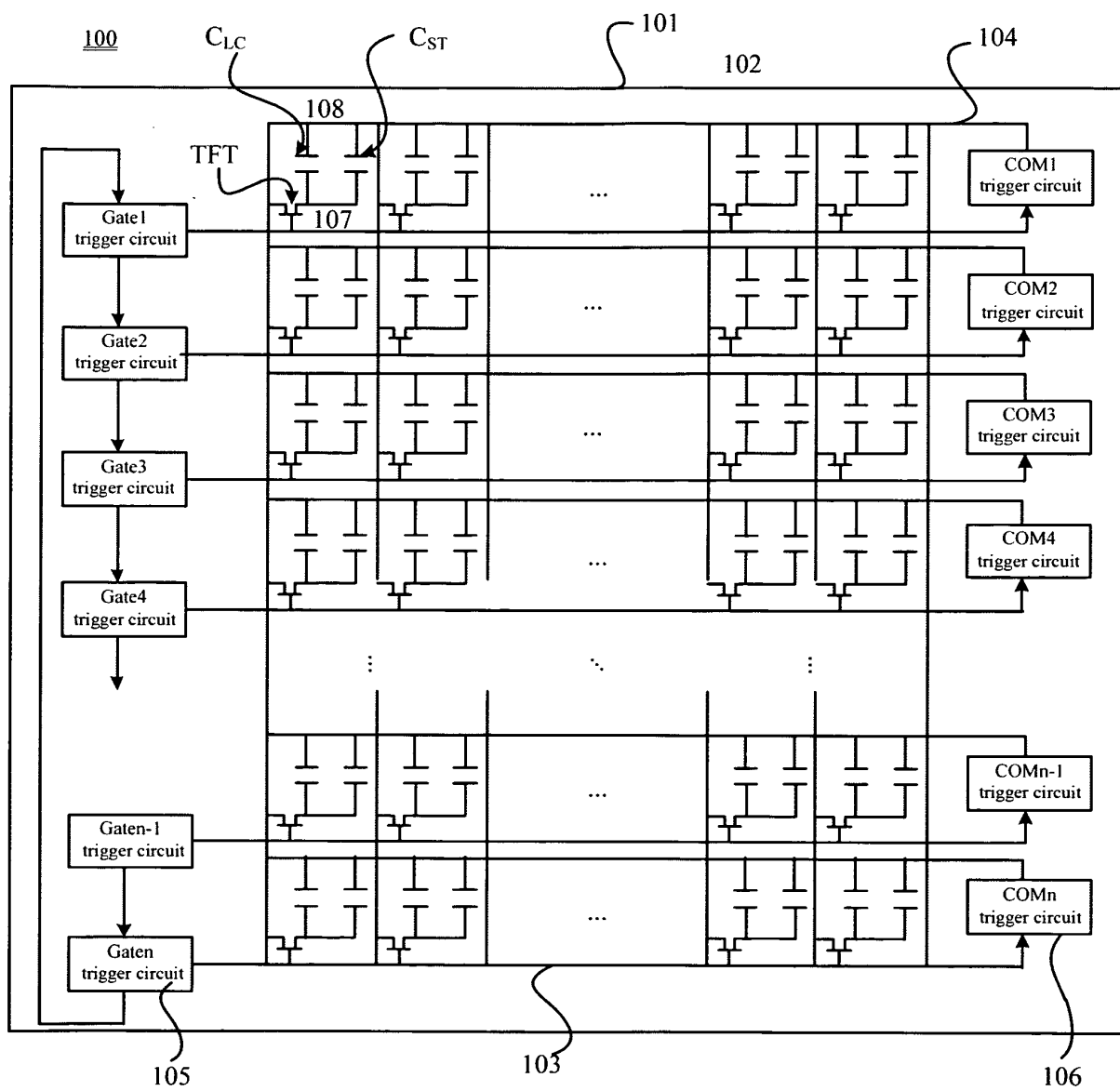


FIG. 1

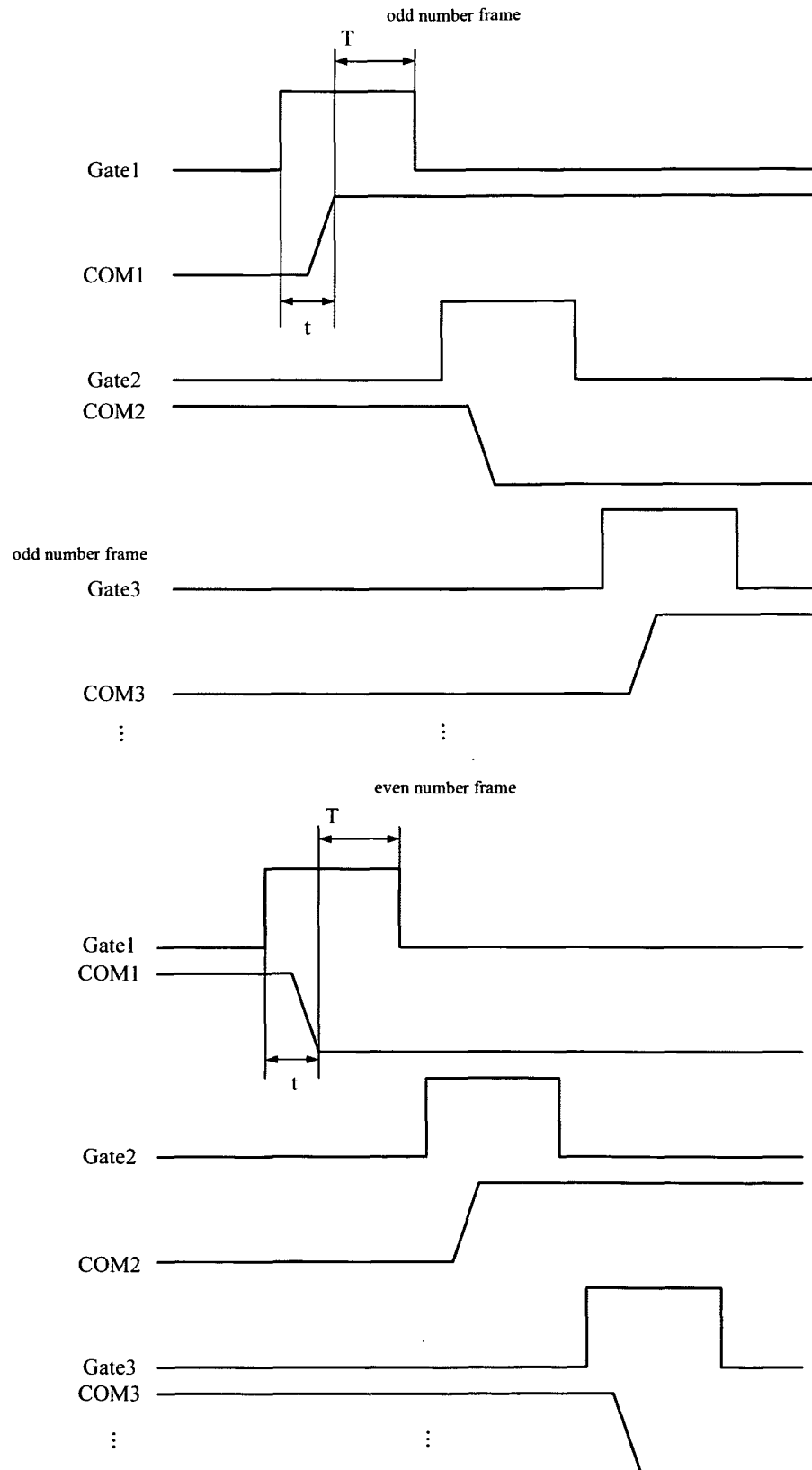


FIG.2

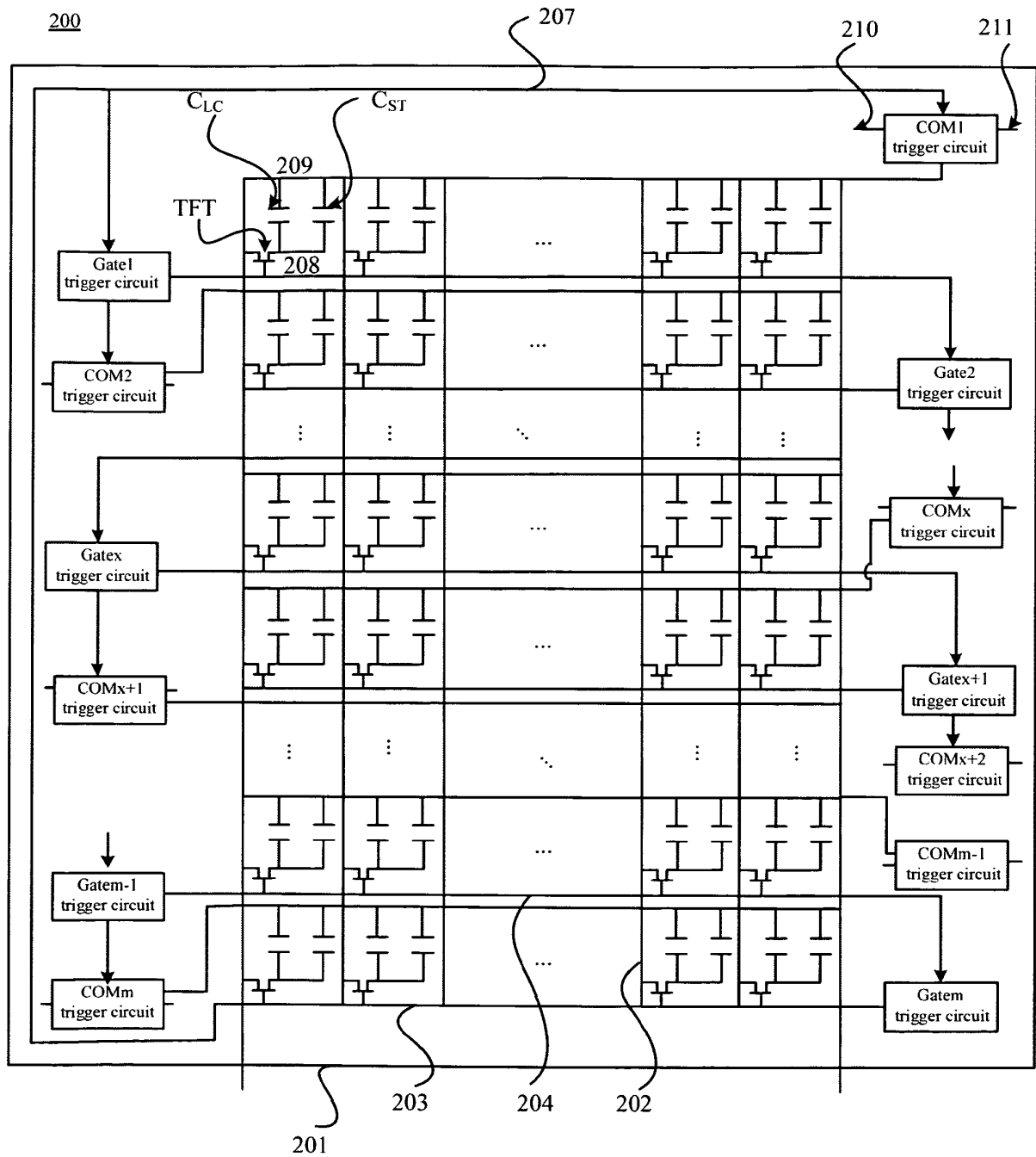


FIG.3

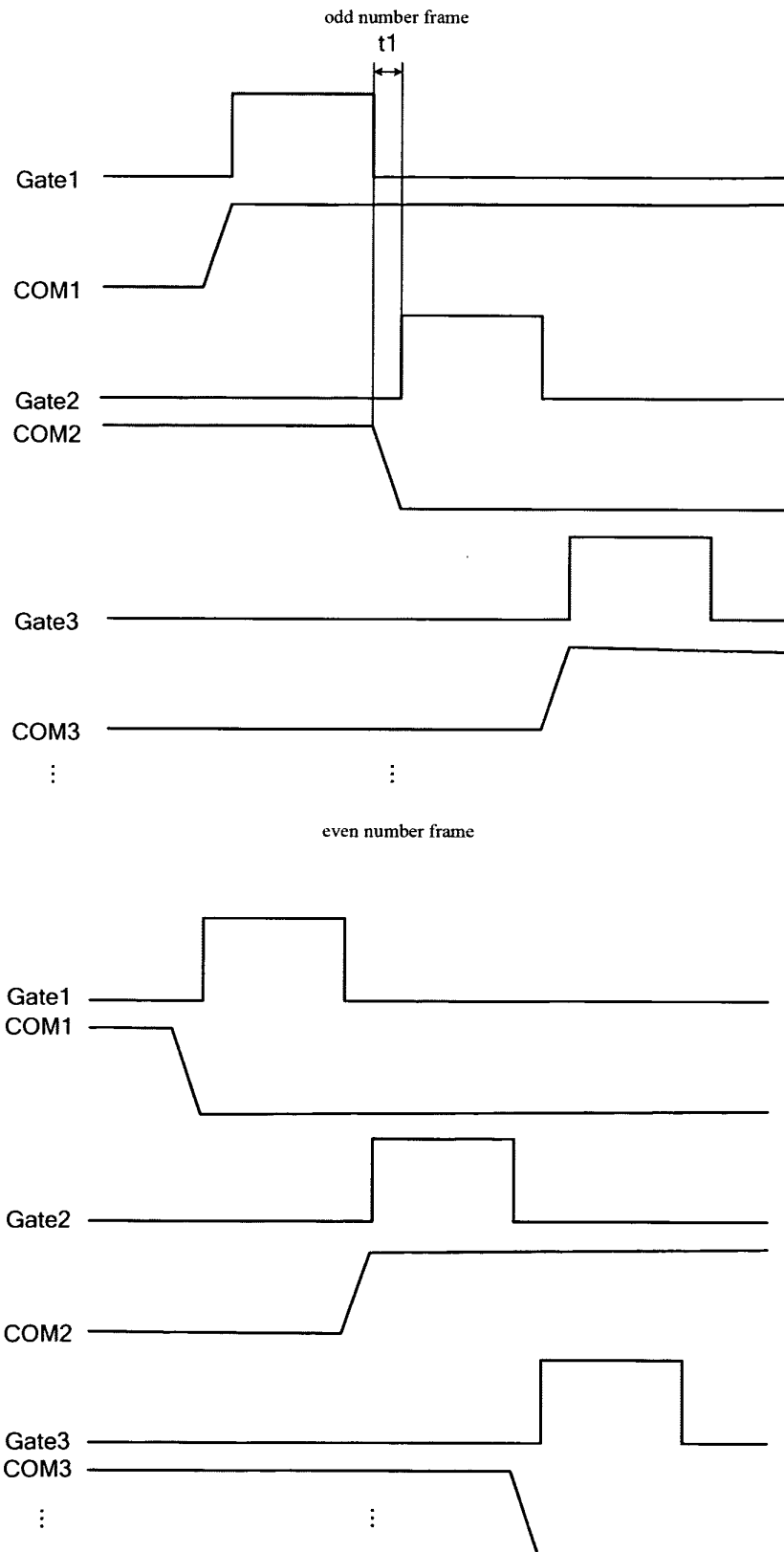


FIG.4

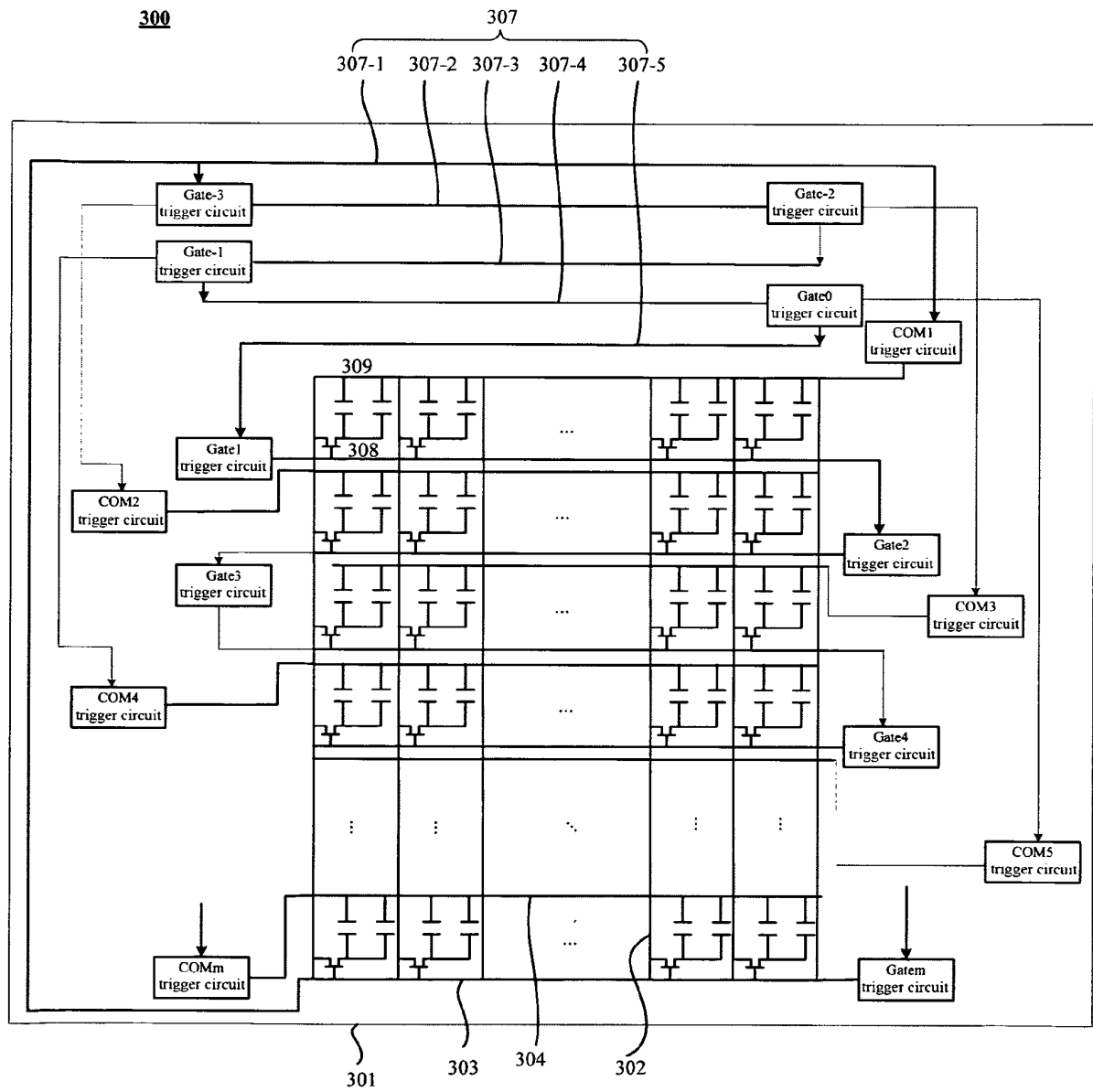


FIG.5

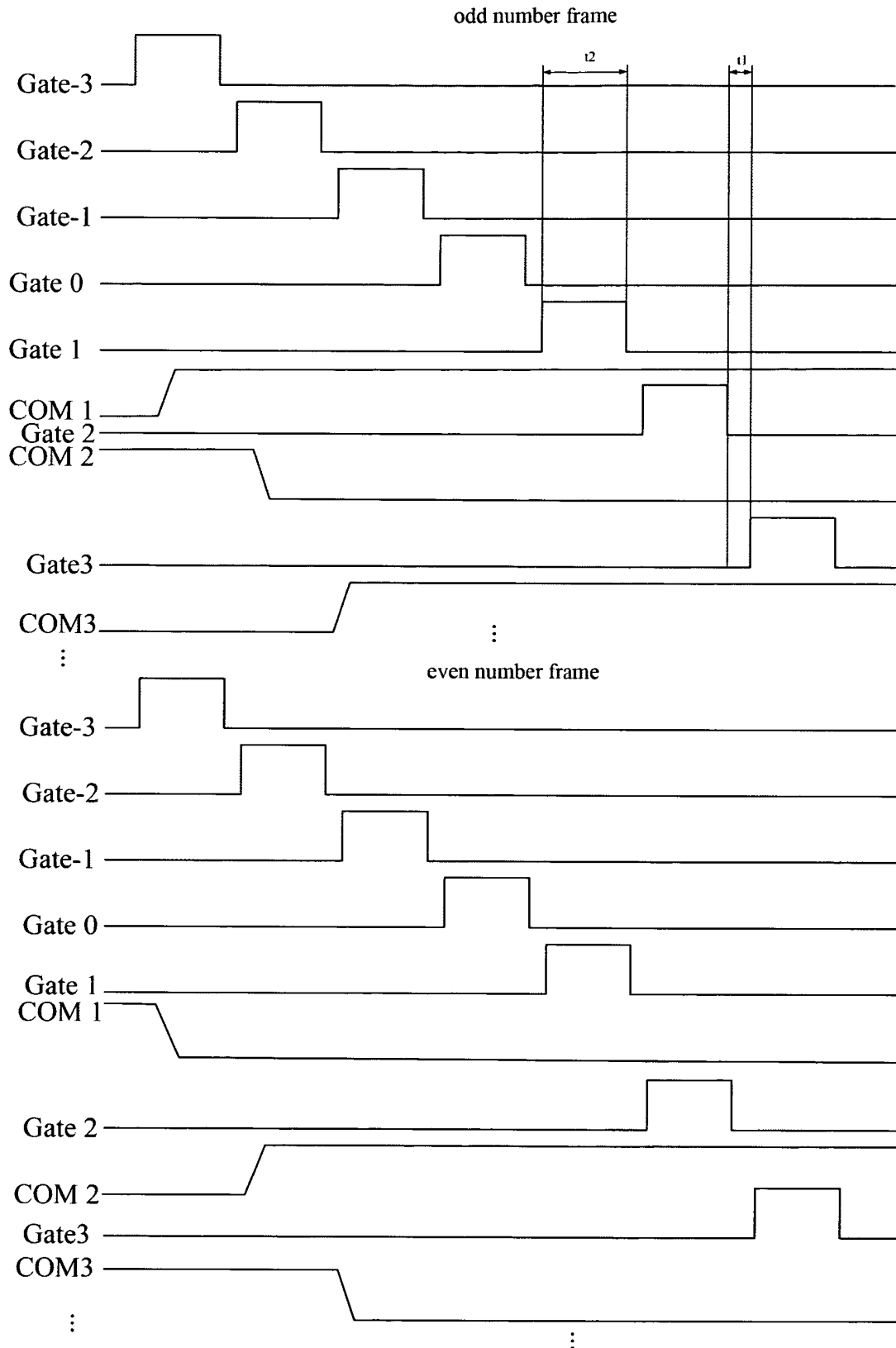


FIG.6

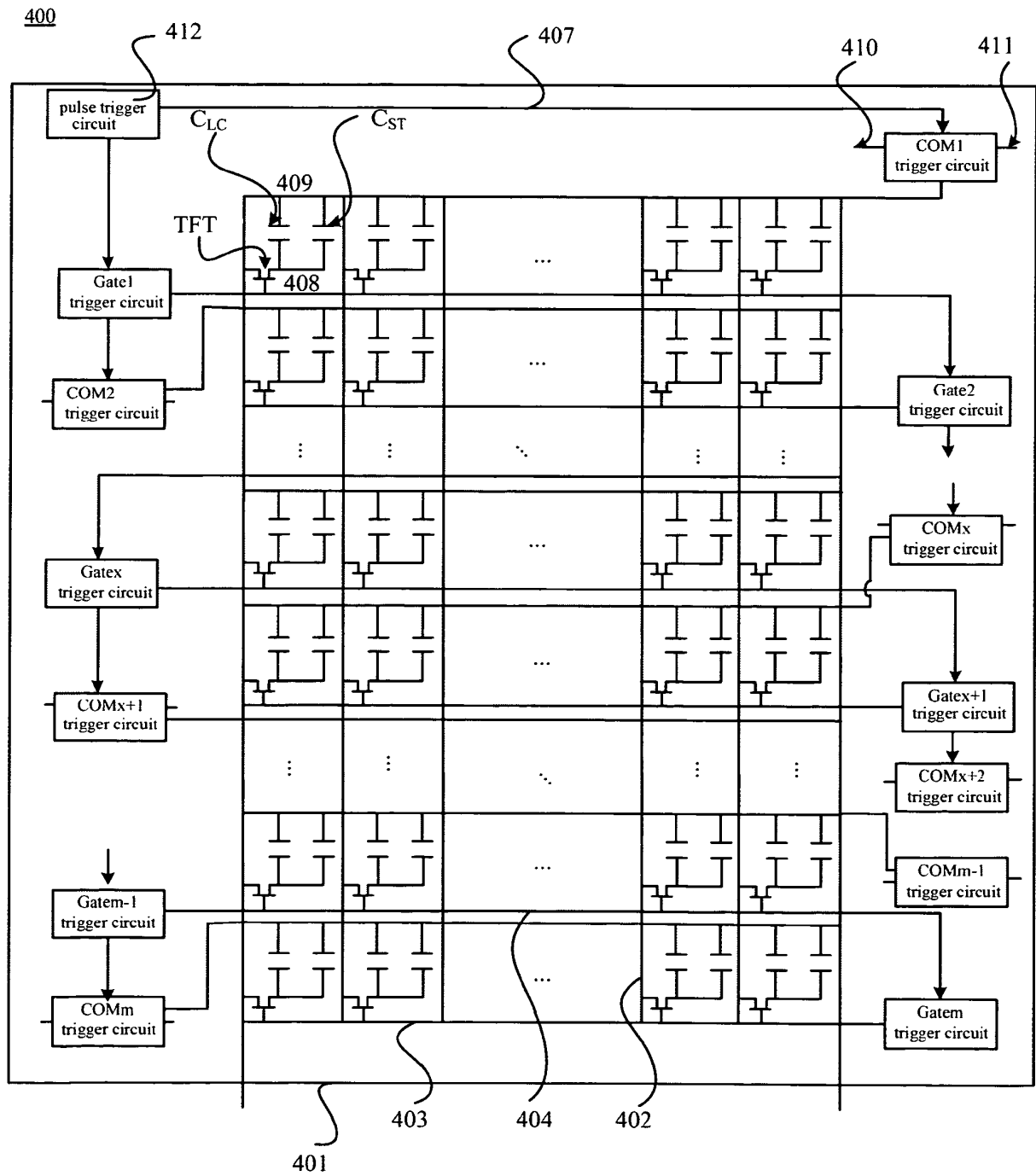


FIG.7

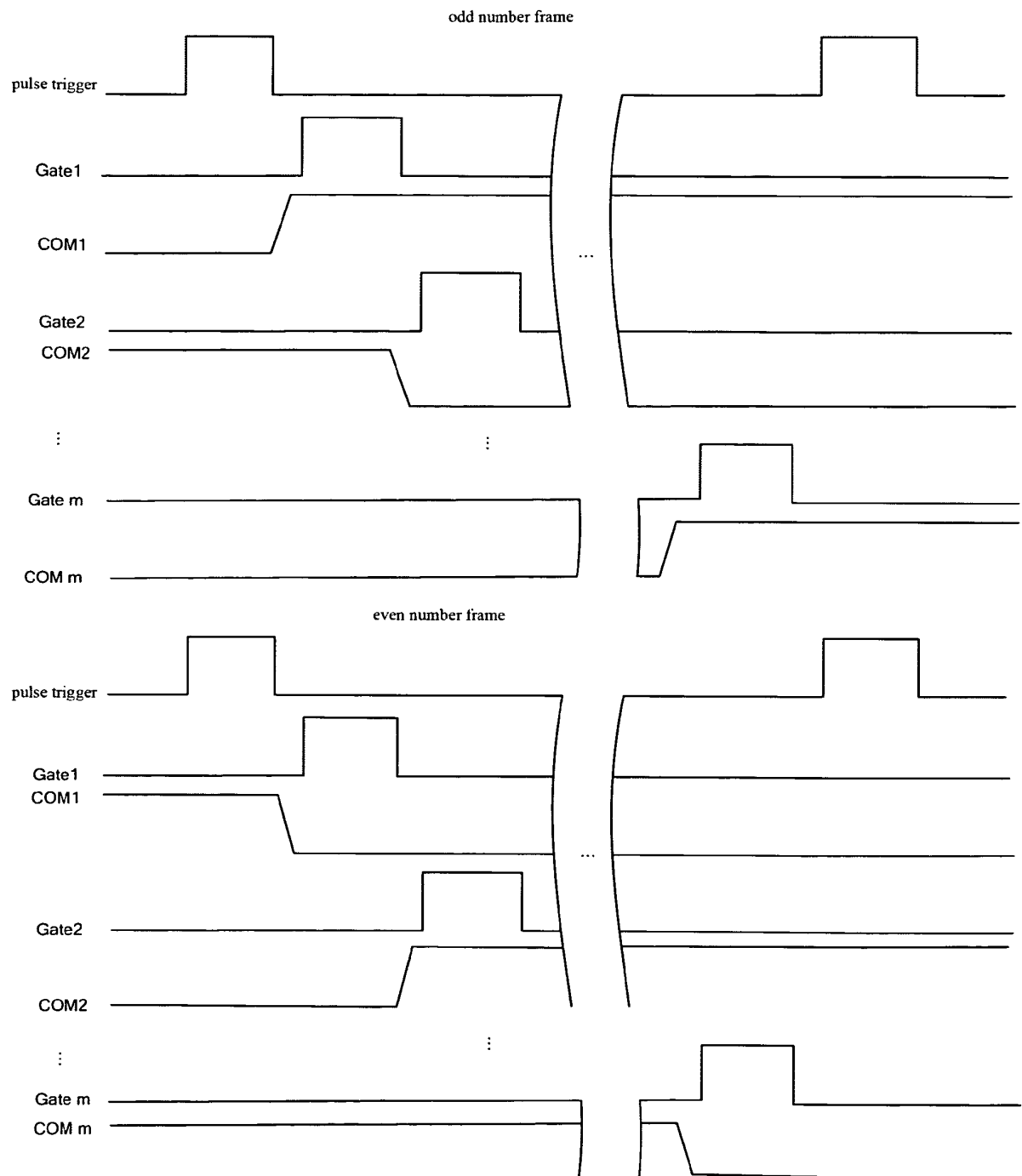


FIG.8

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- EP 1796073 A2 [0008]

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当前申请(专利权)人(译)	上海天马微电子有限公司.		
[标]发明人	LV BOJIA QIAN DONG KONG XIANGZI GU HANYU		
发明人	LV, BOJIA QIAN, DONG KONG, XIANGZI GU, HANYU		
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代理机构(译)	TBK		
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摘要(译)

本发明公开了一种液晶显示装置及其驱动方法，该装置包括多条数据线；多条栅极线；多条公共线；至少一条伪栅极线；多个栅极线触发电路；多个公共线触发电路；其中，最后一条栅极线的一端与最后一条栅极线触发电路连接；每个剩余栅极线的一端与对应于所述每个剩余栅极线的栅极线触发电路连接，并且所述每个剩余栅极线的另一端与后续栅极线触发电路连接；第一公共线触发电路与一条虚拟栅极线连接，其余每条公共线触发电路与一条或多条在线栅极线触发电路连接。利用本发明的液晶显示装置，有效地降低了等待时间对充电时间的影响。

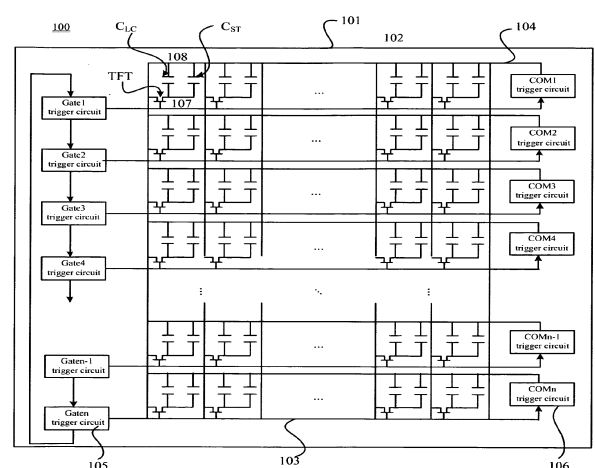


FIG. 1