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**(54) GATE INTEGRATED DRIVE CIRCUIT, SHIFT REGISTER AND DISPLAY SCREEN**

(57) The embodiment of the present disclosure relates to a technical field of liquid crystal display, and particularly, to a gate driver on array, a shifting register and a display screen. The gate driver on array comprises: a first TFT, a second TFT, a third TFT, a fourth TFT, a capacitor and a pulling-down module, the pulling-down module is connected among a first clock signal input terminal, a second clock signal input terminal, a first node and an output terminal, and is connected with a low volt-

age signal terminal, for maintaining the first node and the output terminal being in a low level during a non-operation period of the gate driver on array. Thus, the gate driver on array may achieve a bidirectional scan by designing the functions of the input terminal and the reset terminal in the gate driver on array as being implemented symmetrically, without changing a charging-discharging characteristic of nodes, which ensures a reliability and stabilization of the circuit.

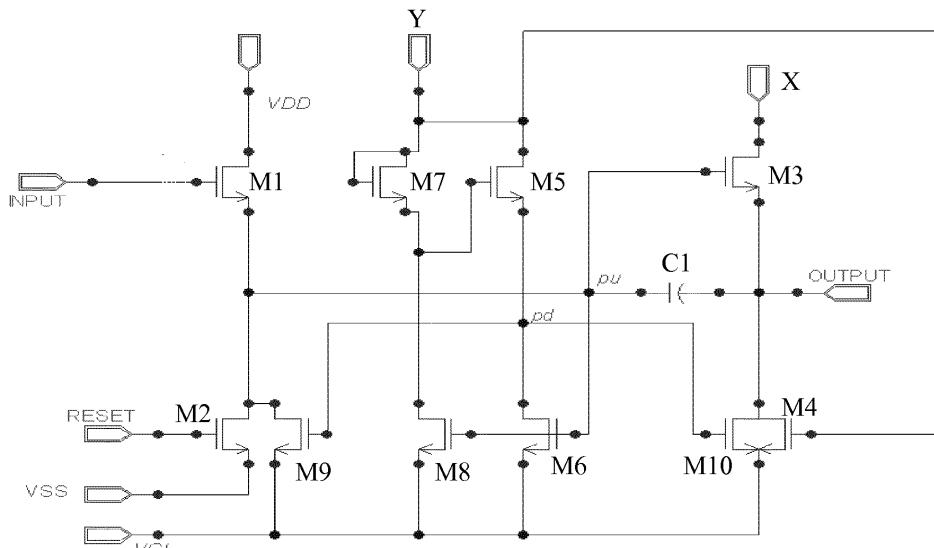


FIG. 4

## Description

### FIELD OF THE DISCLOSURE

**[0001]** The present disclosure relates to a technical field of liquid crystal display, and particularly, to a gate driver on array, a shifting register and a display screen.

### BACKGROUND

**[0002]** The Gate Drive on Array (GOA) refers to integrate a gate driver of a LCD (Liquid Crystal Display) panel on a glass substrate. Then the GOA is connected with gates of an array substrate to control gate signals as a shifting register. As compared with the traditional COF (Chip on Film) and COG (Chip on Glass) processes, the GOA technique saves cost.

**[0003]** However, a scan direction of the GOA panel in the prior art is only a single direction, for example, the scan is performed from up to down or performed from down to up. As shown in Fig.1, which illustrates a GOA circuit with an unidirectional scan in the prior art, the operation principle of the GOA circuit is as follows: when a signal at an input terminal INPUT is in a high level, a TFT (Thin Film Transistor) M1 is turned on so as to charge a PU node; when a clock signal CLK is in the high level, a M3 is turned on and an output terminal OUTPUT outputs pulse signal of the CLK; at the same time, the PU node is pulled-up by a bootstrapping effect of a capacitor C1; subsequently, a reset terminal RESET is in the high level, so that TFTs M2 and M4 are turned on so as to discharge the PU node and the OUTPUT; next, a PD node is controlled by a clock signal CLKB so as to discharge the PU node and the OUTPUT, thus it is ensured that no noise occurs in the GOA circuit in the non-operation period. When such panel is used along with usage of a system terminal, sometimes it needs to debug software again to reverse an image since ICs of different system terminals have differences (the IC is upward or downward), which brings many inconveniences.

### SUMMARY

**[0004]** A gate driver on array (GOA), a shifting register and a display screen according to embodiments of the present disclosure may achieve a bidirectional scan of the GOA and ensure a stabilization of the gate driver on array.

**[0005]** A gate driver on array according to the embodiments of the present disclosure comprises:

**[0006]** a first thin film field effect transistor TFT, a gate of which is connected with an input terminal of the gate driver on array circuit, a drain of which is connected with a power supply voltage terminal VDD, and a source of which is connected with a first node being a pulling-up node;

**[0007]** a second TFT, a gate of which is connected with a reset terminal of the gate driver on array, a source of

which is connected with a common connection voltage terminal VSS, and a drain of which is connected with the first node;

**[0008]** a third TFT, a gate of which is connected with the first node, a drain of which is connected with a first clock signal input terminal, and a source of which is connected with an output terminal;

**[0009]** a fourth TFT, a gate of which is connected with a second clock signal input terminal, a drain of which is connected with the output terminal, and a source of which is connected with a low voltage signal terminal;

**[0010]** a capacitor which is connected between the first node and the output terminal;

**[0011]** a pulling-down module, which is connected among the first clock signal input terminal, the second clock signal input terminal, the first node and the output terminal, and is connected with the low voltage signal terminal, for maintaining the first node and the output terminal being in the low level during a non-operation period of the gate driver on array.

**[0012]** The embodiments of the present disclosure provide a shifting register comprising a plurality of the above-described gate drivers on array, each of the gate driver on array is used to control a gate signal of respective row, wherein an input terminal of the gate driver on array for controlling the gate signal of the N<sup>th</sup> row is connected with an output terminal of the gate driver on array for controlling the gate signal of the (N-1)<sup>th</sup> row, an output terminal of the gate driver on array for controlling the gate signal of the N<sup>th</sup> row is connected with an input terminal of the gate driver on array for controlling the gate signal of the (N+1)<sup>th</sup> row, and a reset terminal of the gate driver on array for controlling the gate signal of the N<sup>th</sup> row is connected with the output terminal of the gate driver on array for controlling the gate signal of the (N+1)<sup>th</sup> row, wherein N is equal to or more than 2.

**[0013]** The embodiments of the present disclosure provide a display screen comprising: the above-described shifting register and an array substrate;

**[0014]** signal output terminals of the shifting register are connected with gate lines of the array substrate, respectively.

**[0015]** The gate driver on array, shifting register and display screen according to the embodiments of the present disclosure enable the gate driver on array to achieve a bidirectional scan by designing the functions of the input terminal and the reset terminal in the gate driver on array as being implemented symmetrically, without changing a charging-discharging characteristic of nodes, which ensures a reliability and stabilization of the circuit.

### BRIEF DESCRIPTION OF THE DRAWINGS

**[0016]**

Fig.1 is a schematic diagram of the GOA in the prior art;

Fig.2 is a schematic diagram illustrating a structure of the gate driver on array according to an embodiment of the present disclosure;

Fig.3 is a schematic diagram illustrating a structure of the shifting register according to another embodiment of the present disclosure;

Fig.4 is a schematic diagram illustrating a detailed structure of the gate driver on array according to the embodiments of the present disclosure;

Fig.5 is a timing sequence chart of voltages of respective terminals of the gate drivers on array for controlling the gate signal corresponding to an odd row during a forward scan according to the embodiments of the present disclosure;

Fig. 6 is a timing sequence chart of voltages of respective terminals of the gate drivers on array for controlling the gate signal corresponding to an even row during a forward scan according to the embodiments of the present disclosure;

Fig.7 is a timing sequence chart of voltages of respective terminals of the gate driver on array for controlling the gate signal corresponding to an odd row during a backward scan according to the embodiments of the present disclosure; and

Fig.8 is a timing sequence chart of voltages of respective terminals of the gate drivers on array for controlling the gate signal corresponding to an even row during a backward scan according to the embodiments of the present disclosure.

#### DETAILED DESCRIPTION

**[0017]** Below detailed implementations of the disclosure will be described in further details in connection with the accompanying drawings.

**[0018]** The embodiments of the present disclosure provide a gate driver on array, as shown in Fig.2, the gate driver on array comprises:

**[0019]** a first thin film field effect transistor TFT M1, a gate of which is connected with an input terminal INPUT of the gate driver on array, a drain of which is connected with a power supply voltage terminal VDD, and a source of which is connected with a first node PU being a pulling-up node;

**[0020]** a second TFT M2, a gate of which is connected with a reset terminal RESET of the gate driver on array, a source of which is connected with a common connection voltage terminal VSS, and a drain of which is connected with the first node PU;

**[0021]** a third TFT M3, a gate of which is connected with the first node PU, a drain of which is connected with a first clock signal input terminal X, and a source of which is connected with an output terminal OUTPUT;

**[0022]** a fourth TFT M4, a gate of which is connected with a second clock signal input terminal Y, a drain of which is connected with the output terminal OUTPUT, and a source of which is connected with a low voltage signal terminal VGL;

**[0023]** a capacitor C1 which is connected between the first node PU and the output terminal OUTPUT;

**[0024]** a pulling-down module 11, which is connected among the first clock signal input terminal X, the second clock signal input terminal Y, the first node PU and the output terminal OUTPUT, and is connected with the low voltage signal terminal VGL, for maintaining the first node PU and the output terminal OUTPUT being in the low level during a non-operation period of the gate driver on array.

**[0025]** Wherein the pulling-down module 11 comprises:

**[0026]** a fifth TFT, a drain of which is connected with the second clock signal input terminal, and a source of which is connected with a second node being a pulling-down node;

**[0027]** a sixth TFT, a drain of which is connected with the second node, a gate of which is connected with the first node, and a source of which is connected with the low voltage signal terminal;

**[0028]** a seventh TFT, gate and drain of which are connected with the second clock signal input terminal together, and a source of which is connected with a gate of the fifth TFT;

**[0029]** a eighth TFT, a drain of which is connected with the source of the seventh TFT, a gate of which is connected with the first node, and a source of which is connected with the low voltage signal terminal;

**[0030]** a ninth TFT, a drain of which is connected with the first node, a gate of which is connected with the second node, and a source of which is connected with the low voltage signal terminal;

**[0031]** a tenth TFT, a drain of which is connected with the output terminal, a gate of which is connected with the second node, and a source of which is connected with the low voltage signal terminal.

**[0032]** In an example, the first clock signal input terminal X of the gate driver on array is connected to a first clock signal line, such as CLK, and the second clock signal input terminal Y thereof is connected to a second clock signal line, such as CLKB, when the gate driver on array is used to control the gate signal corresponding to an odd row; the second clock signal input terminal Y of the gate driver on array is connected to the first clock signal line, and the first clock signal input terminal X thereof is connected to a second clock signal line, when the gate driver on array is used to control the gate signal corresponding to an even row.

**[0033]** A bidirectional scan can be performed by a cascade of a plurality of the above-described gate driver on array and comprises the following cases.

**[0034]** (1) In a forward scan, that is, the scan is performed from the first row to the last row, and the gate driver on array is used to control the gate signal corresponding to an odd row.

**[0035]** When the forward scan is initiated, the VDD provides a constant high level and the VSS provides a constant low level, a high level pulse signal is input to the

input terminal of the gate driver on array, and the first node is charged via the drain of the first TFT; the first clock signal input terminal receives a high level clock signal provided by the first clock signal line, the output terminal is controlled by the third TFT so as to output a high level; the sixth TFT is turned on and pulls down the voltage at the second node to the voltage at the low voltage signal terminal; the reset terminal connected to the gate of the second TFT is in the high level, and the first node is discharged; the second clock signal input terminal receives a high level clock signal provided by the second clock signal line, and the output terminal is discharged via the fourth TFT; the second node is charged through the fifth TFT, the ninth TFT is controlled to discharge the first node and the tenth TFT is controlled to discharge the output terminal.

**[0036]** (2) In the forward scan, that is, the scan is performed from the first row to the last row, and the gate driver on array is used to control the gate signal corresponding to an even row.

**[0037]** When the forward scan is initiated, the VDD provides a constant high level and the VSS provides a constant low level, a high level pulse signal is input to the input terminal of the gate driver on array, and the first node is charged via the drain of the first TFT; the first clock signal input terminal receives a high level clock signal provided by the second clock signal line, the output terminal is controlled by the third TFT so as to output the high level; the sixth TFT is turned on and pulls down the voltage at the second node to the voltage at the low voltage signal terminal; the reset terminal connected to the gate of the second TFT is in the high level, and the first node is discharged; the second clock signal input terminal receives a high level clock signal provided by the first clock signal line, and the output terminal is discharged via the fourth TFT; the second node is charged through the fifth TFT, the ninth TFT is controlled to discharge the first node and the tenth TFT is controlled to discharge the output terminal.

**[0038]** (3) In a backward scan, that is, the scan is performed from the last row to the first row, and the gate driver on array is used to control the gate signal corresponding to an odd row.

**[0039]** When the backward scan is initiated, the VDD provides a constant low level and the VSS provides a constant high level, a high level pulse signal is input to the reset terminal of the gate driver on array, the first node is charged via the source of the second TFT; the first clock signal input terminal receives a high level clock signal provided by the first clock signal line, the output terminal is controlled by the third TFT so as to output a high level; the sixth TFT is turned on and pulls down the voltage at the second node to the voltage at the low voltage signal terminal; the input terminal connected to the gate of the first TFT is in the high level, and the first node is discharged; the second clock signal input terminal receives a high level clock signal provided by the second clock signal line, and the output terminal is discharged

via the fourth TFT; the second node is charged through the fifth TFT, the ninth TFT is controlled to discharge the first node and the tenth TFT is controlled to discharge the output terminal.

**[0040]** (4) In the backward scan, that is, the scan is performed from the last row to the first row, and the gate driver on array is used to control the gate signal corresponding to an even row.

**[0041]** When the backward scan is initiated, the VDD provides a constant low level and the VSS provides a constant high level, a high level pulse signal is input to the reset terminal of the gate driver on array, the first node is charged via the source of the second TFT; the first clock signal input terminal receives a high level clock signal provided by the second clock signal line, the output terminal is controlled by the third TFT so as to output a high level; the sixth TFT is turned on and pulls down the voltage at the second node to the voltage at the low voltage signal terminal; the input terminal connected to the gate of the first TFT is in the high level, and the first node is discharged; the second clock signal input terminal receives a high level clock signal provided by the first clock signal line, and the output terminal is discharged via the fourth TFT; the second node is charged through the fifth TFT, the ninth TFT is controlled to discharge the first node and the tenth TFT is controlled to discharge the output terminal.

**[0042]** In an example, the low voltage signal terminal is used for providing the constant low level to the gate driver on array.

**[0043]** It can be seen from the above description that the gate driver on array according to the embodiments of the present disclosure enable the gate driver on array to achieve a bidirectional scan by designing the functions of the input terminal and the reset terminal in the gate driver on array as being implemented symmetrically, without changing a charging-discharging characteristic of nodes, which ensures a reliability and stabilization of the circuit.

**[0044]** Based on the same conception, the embodiments of the present disclosure provide a shifting register comprising a plurality of the above-described gate drivers on array, each of the gate driver on array is used to control a gate signal of respective row, as shown in Fig.3, an input terminal of the gate driver on array for controlling the gate signal of the  $N^{th}$  row is connected with an output terminal of the gate driver on array for controlling the gate signal of the  $(N-1)^{th}$  row, an output terminal of the gate driver on array for controlling the gate signal of the  $N^{th}$  row is connected with an input terminal of the gate driver on array for controlling the gate signal of the  $(N+1)^{th}$  row and a reset terminal of the gate driver on array for controlling the gate signal of the  $N^{th}$  row is connected with the output terminal of the gate driver on array for controlling the gate signal of the  $(N+1)^{th}$  row, wherein  $N$  is equal to or more than 2. Regarding the gate driver on array for controlling the gate signal corresponding to an odd row, its first clock signal input terminal X is connected to a first

clock signal line, such as CLK, and its second clock signal input terminal Y is connected to a second clock signal line, such as CLKB; regarding the gate driver on array for controlling the gate signal corresponding to an even row, its second clock signal input terminal Y is connected to a first clock signal line, and its first clock signal input terminal X is connected to a second clock signal line.

**[0045]** Below will describe the gate driver on array in the shifting register according to the present disclosure by means of specific embodiments. Making a 10T1C as an example, as shown in Fig.4, a first thin film field effect transistor TFT M1, a gate of which is connected with an input terminal INPUT of the gate driver on array, a drain of which is connected with a power supply voltage terminal VDD, and a source of which is connected with a first node PU being a pulling-up node; a second TFT M2, a gate of which is connected with a reset terminal RESET of the gate driver on array, a source of which is connected with a common connection voltage terminal VSS, and a drain of which is connected with the first node PU; a third TFT M3, a gate of which is connected with the first node PU, a source of which is connected with a first clock signal input terminal X, and a drain of which is connected with an output terminal OUTPUT; a fourth TFT M4, a gate of which is connected with a second clock signal input terminal Y, a drain of which is connected with the output terminal OUTPUT, and a source of which is connected with a low voltage signal terminal VGL; a capacitor C1 which is connected between the first node PU and the output terminal OUTPUT; a fifth TFT M5, a drain of which is connected with the second clock signal input terminal Y, and a source of which is connected with a second node PD being a pulling-down node; a sixth TFT M6, a drain of which is connected with the second node PD, a gate of which is connected with the first node PU, and a source of which is connected with the low voltage signal terminal VGL; a seventh TFT M7, a gate and a drain of which are connected with the second clock signal input terminal Y together, and a source of which is connected with the gate of the fifth TFT M5; a eighth TFT M8, a drain of which is connected with the source of the seventh TFT M7, a gate of which is connected with the first node PU, and a source of which is connected with the low voltage signal terminal VGL; a ninth TFT M9, a drain of which is connected with the first node PU, a gate of which is connected with the second node PD, and a source of which is connected with the low voltage signal terminal VGL; a tenth TFT M10, a drain of which is connected with the output terminal OUTPUT, a gate of which is connected with the second node PD, and a source of which is connected with the low voltage signal terminal VGL. Wherein the drain of the TFT M3 is the first clock signal input terminal X, and the drain of the TFT M5 is the second clock signal input terminal Y. When the current row is an odd row, the first clock signal input terminal X is connected to the first clock signal line CLK and the second clock signal input terminal Y is connected to the second clock signal line CLKB. When the current row is an even row,

the first clock signal input terminal X is connected to the second clock signal line CLKB and the second clock signal input terminal Y is connected to the first clock signal line CLK.

**[0046]** Fig.5 is a timing sequence chart of voltages of respective terminals of the gate driver on array for controlling the gate signal corresponding to an odd row during the forward scan. It can be seen that, when the forward scan (from the first row to the last row) is performed, the VDD provides a constant high voltage and the VSS provides a constant low voltage, a high level pulse signal is input to the input terminal INPUT, so that the M1 is turned on and a voltage control bus PU node is in turn charged; next, the first clock signal input terminal X inputs a high level clock signal provided by the first clock signal line CLK, so that the M3 is turned on and the output terminal OUTPUT is controlled output a high level, while charges stored in the capacitor C1 transfers to the PU node and thus the voltage at the PU node further increases. Meanwhile, the M6 is turned on by the increased voltage at the PU node, and in turn pulls down the voltage at the second node PD to the voltage at the low voltage signal terminal VGL. Next, the reset terminal RESET is in the high level, so that the MS is turned on and the PU node is discharged; at the same time, the second clock signal input terminal Y inputs a high level clock signal provided by the second clock signal line CLKB, so that the M4 is turned on and the output terminal OUTPUT is discharged; further, the M5 is turned on and the PD node is charged, then the pulling-down M9 is controlled to discharge the PU node and the pulling-down TFT M10 is controlled to discharge the output terminal OUTPUT.

**[0047]** Fig. 6 is a timing sequence chart of voltages of respective terminals of the gate driver on array for controlling the gate signal corresponding to an even row during a forward scan. It can be seen that, when the forward scan (from the first row to the last row) is performed, the VDD provides a constant high voltage and the VSS provides a constant low voltage, a high level pulse signal is input to the input terminal INPUT, so that the M1 is turned on and the PU node is in turn charged; next, the first clock signal input terminal X inputs a high level clock signal provided by the second clock signal line CLKB, so that the M3 is turned on and the output terminal OUTPUT outputs the high level, while charges stored in the capacitor C1 transfers to the PU node and the voltage at the PU node further increases. Meanwhile, the M6 is turned on due to the increased voltage at the PU node, and in turn pulls down the voltage at the second node PD to the voltage at the low voltage signal terminal VGL. Next, the reset terminal RESET is in the high level, so that the M2 is turned on and the PU node is discharged; at the same time, the second clock signal input terminal Y inputs a high level clock signal provided by the first clock signal line CLK, so that the M4 is turned on and the output terminal OUTPUT is discharged; further, the M5 is turned on and the PD node is charged, then the pulling-down M9 is controlled to discharge the PU node and the pulling-

down TFT M10 is controlled to discharge the output terminal OUTPUT.

**[0048]** Fig.7 is a timing sequence chart of voltages of respective terminals of the gate driver on array for controlling the gate signal corresponding to an odd row during a backward scan. It can be seen that, when the backward scan (from the last row to the first row) is performed, the VDD provides a constant low voltage and the VSS provides a constant high voltage, a high level pulse signal is input to the reset terminal RESET, so that the M2 is turned on and in turn the PU node is charged; next, the first clock signal input terminal X inputs a high level clock signal provided by the first clock signal line CLK, so that the M3 is turned on and the output terminal OUTPUT outputs the high level at this moment, while charges stored in the capacitor C1 transfers to the PU node and the voltage at the PU node further increases. Meanwhile, the M6 is turned on due to the increased voltage at the PU node, and in turn pulls down the voltage at the second node PD to the voltage at the low voltage signal terminal VGL. Next, the input terminal INPUT is in the high level, so that the M1 is turned on and the PU node is discharged; at the same time, the second clock signal input terminal Y inputs a high level clock signal provided by the second clock signal line CLKB, so that the M4 is turned on and the output terminal OUTPUT is discharged; further, the M5 is turned on and the PD node is charged, then the pulling-down M9 is controlled to discharge the PU node and the pulling-down TFT M10 is controlled to discharge the output terminal OUTPUT.

**[0049]** Fig.8 is a timing sequence chart of voltages of respective terminals of the gate driver on array for controlling the gate signal corresponding to an even row during a backward scan. It can be seen that, when the backward scan (from the last row to the first row) is performed, the VDD provides a constant low voltage and the VSS provides a constant high voltage, a high level pulse signal is input to the reset terminal RESET, so that the M2 is turned on and in turn the PU node is charged; next, the first clock signal input terminal X inputs a high level clock signal provided by the second clock signal line CLKB, so that the M3 is turned on and the output terminal OUTPUT outputs the high level, while charges stored in the capacitor C1 transfers to the PU node and the voltage at the PU node further increases. Meanwhile, the M6 is turned on due to the increased voltage at the PU node, and in turn pulls down the voltage at the second node PD to the voltage at the low voltage signal terminal VGL. Next, the input terminal INPUT is in the high level, so that the M1 is turned on and the PU node is discharged; at the same time, the second clock signal input terminal Y inputs a high level clock signal provided by the first clock signal line CLK, so that the M4 is turned on and the output terminal OUTPUT is discharged; further, the M5 is turned on and the PD node is charged, then the pulling-down M9 is controlled to discharge the PU node and the pulling-down TFT M10 is controlled to discharge the output terminal OUTPUT.

**[0050]** It can be seen from the above description that the gate driver on array according to the embodiments of the present disclosure enable the gate driver on array to achieve a bidirectional scan by designing the functions of the input terminal and the reset terminal in the gate driver on array as being implemented symmetrically, without changing a charging-discharging characteristic of nodes, which ensures a reliability and stabilization of the circuit.

**[0051]** Based on the same conception, the embodiments of the present disclosure provide a display screen comprising the above-described shifting register and an array substrate, a signal output terminal of each gate driver on array in the shifting register is connected with a gate line under the control of a gate signal output from the gate driver on array in the array substrate.

**[0052]** It can be seen from the above description that the gate driver on array, shifting register and display screen according to the embodiments of the present disclosure enable the gate driver on array to achieve a bidirectional scan by designing the functions of the input terminal and the reset terminal in the gate driver on array as being implemented symmetrically, without changing a charging-discharging characteristic of nodes, which ensures a reliability and stabilization of the circuit.

**[0053]** The above are only exemplary embodiments of the disclosed solution, but the scope sought for protection is not limited thereto. Instead, any or all modifications or replacements as would be obvious to those skilled in the art are intended to be included within the scope of the present invention. Therefore, the scope of the present invention is defined in the appended claims.

### 35 Claims

#### 1. A gate driver on array, comprising:

a first thin film field effect transistor TFT, a gate of which is connected with an input terminal of the gate driver on array, a drain of which is connected with a power supply voltage terminal VDD, and a source of which is connected with a first node being a pulling-up node; a second TFT, a gate of which is connected with a reset terminal of the gate driver on array, a source of which is connected with a common connection voltage terminal VSS, and a drain of which is connected with the first node; a third TFT, a gate of which is connected with the first node, a drain of which is connected with a first clock signal input terminal, and a source of which is connected with an output terminal; a fourth TFT, a gate of which is connected with a second clock signal input terminal, a drain of which is connected with the output terminal, and a source of which is connected with a low voltage signal terminal;

a capacitor which is connected between the first node and the output terminal; and a pulling-down module, which is connected among the first clock signal input terminal, the second clock signal input terminal, the first node and the output terminal, and is connected with the low voltage signal terminal, for maintaining the first node and the output terminal being in the low level during a non-operation period of the gate driver on array. 5

2. A gate driver on array as claimed in claim 1, wherein the pulling-down module comprises:

a fifth TFT, a drain of which is connected with the second clock signal input terminal, and a source of which is connected with a second node being a pulling-down node; 15  
 a sixth TFT, a drain of which is connected with the second node, a gate of which is connected with the first node, and a source of which is connected with the low voltage signal terminal; 20  
 a seventh TFT, a gate and a drain of which are connected with the second clock signal input terminal together, and a source of which is connected with a gate of the fifth TFT; 25  
 a eighth TFT, a drain of which is connected with the source of the seventh TFT, a gate of which is connected with the first node, and a source of which is connected with the low voltage signal terminal; 30  
 a ninth TFT, a drain of which is connected with the first node, a gate of which is connected with the second node, and a source of which is connected with the low voltage signal terminal; 35  
 a tenth TFT, a drain of which is connected with the output terminal, a gate of which is connected with the second node, and a source of which is connected with the low voltage signal terminal. 40

3. A gate driver on array as claimed in claim 1, wherein the first clock signal input terminal of the gate driver on array is connected to the first clock signal line, and the second clock signal input terminal of the gate driver on array is connected to the second clock signal line, when the gate driver on array is used to control the gate signal corresponding to an odd row; the second clock signal input terminal of the gate driver on array is connected to the first clock signal line, and the first clock signal input terminal of the gate driver on array is connected to the second clock signal line, when the gate driver on array is used to control the gate signal corresponding to an even row. 45

4. A shifting register, comprising:

a plurality of gate drivers on array, each of the gate drivers on array is used to control a gate

signal of respective row, wherein an input terminal of the gate driver on array for controlling the gate signal of the  $N^{th}$  row is connected with an output terminal of the gate driver on array for controlling the gate signal of the  $(N-1)^{th}$  row, an output terminal of the gate driver on array for controlling the gate signal of the  $N^{th}$  row is connected with an input terminal of the gate driver on array for controlling the gate signal of the  $(N+1)^{th}$  row and a reset terminal of the gate driver on array for controlling the gate signal of the  $N^{th}$  row is connected with the output terminal of the gate driver on array for controlling the gate signal of the  $(N+1)^{th}$  row, wherein  $N$  is equal to or more than 2, each of the gate drivers on array comprises:

a first thin film field effect transistor TFT, a gate of which is connected with an input terminal of the gate driver on array, a drain of which is connected with a power supply voltage terminal VDD, and a source of which is connected with a first node being a pulling-up node; 5  
 a second TFT, a gate of which is connected with a reset terminal of the gate driver on array, a source of which is connected with a common connection voltage terminal VSS, and a drain of which is connected with the first node; 10  
 a third TFT, a gate of which is connected with the first node, a drain of which is connected with a first clock signal input terminal, and a source of which is connected with an output terminal; 15  
 a fourth TFT, a gate of which is connected with a second clock signal input terminal, a drain of which is connected with the output terminal, and a source of which is connected with a low voltage signal terminal; 20  
 a capacitor which is connected between the first node and the output terminal; and a pulling-down module, which is connected among the first clock signal input terminal, the second clock signal input terminal, the first node and the output terminal, and is connected with the low voltage signal terminal, for maintaining the first node and the output terminal being in the low level during a non-operation period of the gate driver on array. 25

5. A shifting register as claimed in claim 4, wherein the pulling-down module comprises:

a fifth TFT, a drain of which is connected with the second clock signal input terminal, and a source of which is connected with a second node

being a pulling-down node; a sixth TFT, a drain of which is connected with the second node, a gate of which is connected with the first node, and a source of which is connected with the low voltage signal terminal; a seventh TFT, a gate and a drain of which are connected with the second clock signal input terminal together, and a source of which is connected with a gate of the fifth TFT; a eighth TFT, a drain of which is connected with the source of the seventh TFT, a gate of which is connected with the first node, and a source of which is connected with the low voltage signal terminal; a ninth TFT, a drain of which is connected with the first node, a gate of which is connected with the second node, and a source of which is connected with the low voltage signal terminal; and a tenth TFT, a drain of which is connected with the output terminal, a gate of which is connected with the second node, and a source of which is connected with the low voltage signal terminal.

6. A shifting register as claimed in claim 5, wherein the first clock signal input terminal of the gate driver on array is connected to the first clock signal line, and the second clock signal input terminal of the gate driver on array is connected to the second clock signal line, when the gate driver on array is used to control the gate signal corresponding to an odd row; the second clock signal input terminal of the gate driver on array is connected to the first clock signal line, and the first clock signal input terminal of the gate driver on array is connected to the second clock signal line, when the gate driver on array is used to control the gate signal corresponding to an even row.

7. A shifting register as claimed in claim 6, wherein, regarding the gate driver on array for controlling the gate signal corresponding to an odd row, the VDD provides a constant high level and the VSS provides a constant low level when a forward scan is initiated, a high level pulse signal is input to the input terminal of the gate driver on array, and the first node is charged via the drain of the first TFT; the first clock signal input terminal receives a high level clock signal provided by the first clock signal line, the output terminal is controlled by the third TFT so as to output a high level; the sixth TFT is turned on and pulls down the voltage at the second node to the voltage at the low voltage signal terminal; the reset terminal connected to the gate of the second TFT is in a high level, and the first node is discharged; the second clock signal input terminal receives a high level clock signal provided by the second clock signal line, and the output terminal is discharged via the fourth TFT; the second node is charged through the fifth TFT, the ninth TFT is controlled to discharge the first node and the tenth TFT is controlled to discharge the output terminal.

8. A shifting register as claimed in claim 6, wherein, regarding the gate driver on array for controlling the gate signal corresponding to an even row, the VDD provides a constant high level and the VSS provides a constant low level when a forward scan is initiated, a high level pulse signal is input to the input terminal of the gate driver on array, and the first node is charged via the drain of the first TFT; the first clock signal input terminal receives a high level clock signal provided by the second clock signal line, the output terminal is controlled by the third TFT so as to output a high level; the sixth TFT is turned on and pulls down the voltage at the second node to the voltage at the low voltage signal terminal; the reset terminal connected to the gate of the second TFT is in a high level, and the first node is discharged; the second clock signal input terminal receives a high level clock signal provided by the first clock signal line, and the output terminal is discharged via the fourth TFT; the second node is charged through the fifth TFT, the ninth TFT is controlled to discharge the first node and the tenth TFT is controlled to discharge the output terminal.

9. A shifting register as claimed in claim 6, wherein, regarding the gate driver on array for controlling the gate signal corresponding to an odd row, the VDD provides a constant low level and the VSS provides a constant high level when a backward scan is initiated, a high level pulse signal is input to the reset terminal of the gate driver on array, and the first node is discharged through the source of the second TFT; the first clock signal input terminal receives a high level clock signal provided by the first clock signal line, the output terminal is controlled by the third TFT so as to output a high level; the sixth TFT is turned on and pulls down the voltage at the second node to the voltage at the low voltage signal terminal; the input terminal connected to the gate of the first TFT is in a high level, and the first node is discharged; the second clock signal input terminal receives a high level clock signal provided by the second clock signal line, and the output terminal is discharged via the fourth TFT; the second node is charged through the fifth TFT, the ninth TFT is controlled to discharge the first node and the tenth TFT is controlled to discharge the output terminal.

10. A shifting register as claimed in claim 6, wherein, regarding the gate driver on array for controlling the gate signal corresponding to an even row, the VDD provides a constant low level and the VSS provides a constant high level when a backward scan is initiated, a high level pulse signal is input to the input terminal of the gate driver on array, and the first node is charged via the drain of the first TFT; the first clock signal input terminal receives a high level clock signal provided by the second clock signal line, the output terminal is controlled by the third TFT so as to output a high level; the sixth TFT is turned on and pulls down the voltage at the second node to the voltage at the low voltage signal terminal; the reset terminal connected to the gate of the second TFT is in a high level, and the first node is discharged; the second clock signal input terminal receives a high level clock signal provided by the first clock signal line, and the output terminal is discharged via the fourth TFT; the second node is charged through the fifth TFT, the ninth TFT is controlled to discharge the first node and the tenth TFT is controlled to discharge the output terminal.

gate signal corresponding to an even row,  
the VDD provides a constant low level and the VSS  
provides a constant high level when a backward scan  
is initiated,  
a high level pulse signal is input to the reset terminal 5  
of the gate driver on array, and the first node is dis-  
charged through the source of the second TFT;  
the first clock signal input terminal receives a high  
level clock signal provided by the second clock signal  
line, the output terminal is controlled by the third TFT 10  
so as to output a high level; the sixth TFT is turned  
on and pulls down the voltage at the second node  
to the voltage at the low voltage signal terminal;  
the input terminal connected to the gate of the first  
TFT is in a high level, and the first node is discharged; 15  
the second clock signal input terminal receives a high  
level clock signal provided by the first clock signal  
line, and the output terminal is discharged via the  
fourth TFT; the second node is charged through the  
fifth TFT, the ninth TFT is controlled to discharge the 20  
first node and the tenth TFT is controlled to discharge  
the output terminal.

11. A display screen, comprising: a shifting register as  
claimed in any one of claims 4-10, and an array sub- 25  
strate;  
a signal output terminal of the shifting register is con-  
nected with a gate line of the array substrate.

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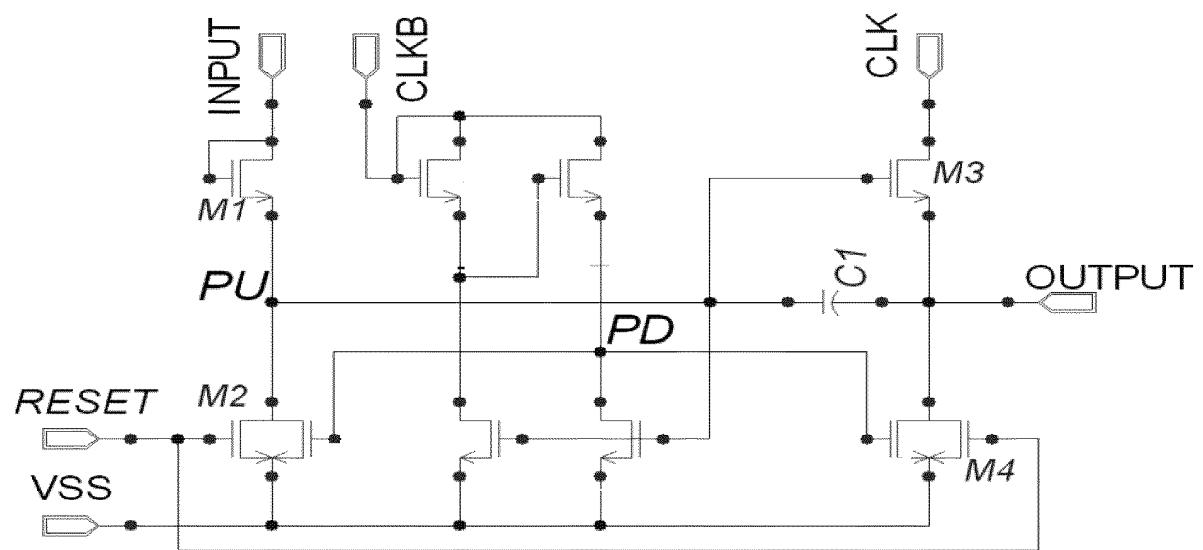


FIG. 1

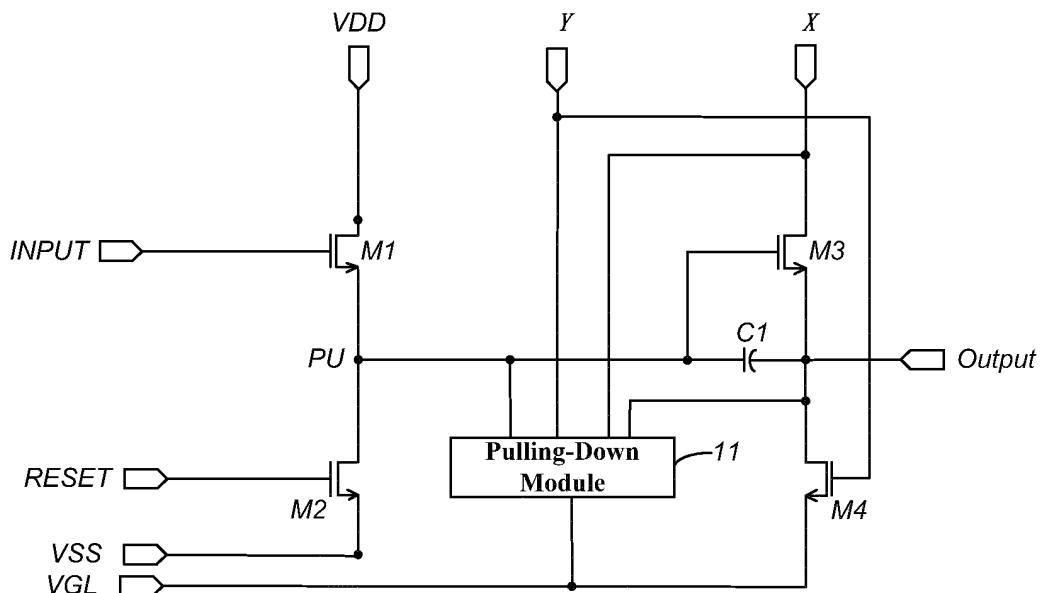


FIG. 2

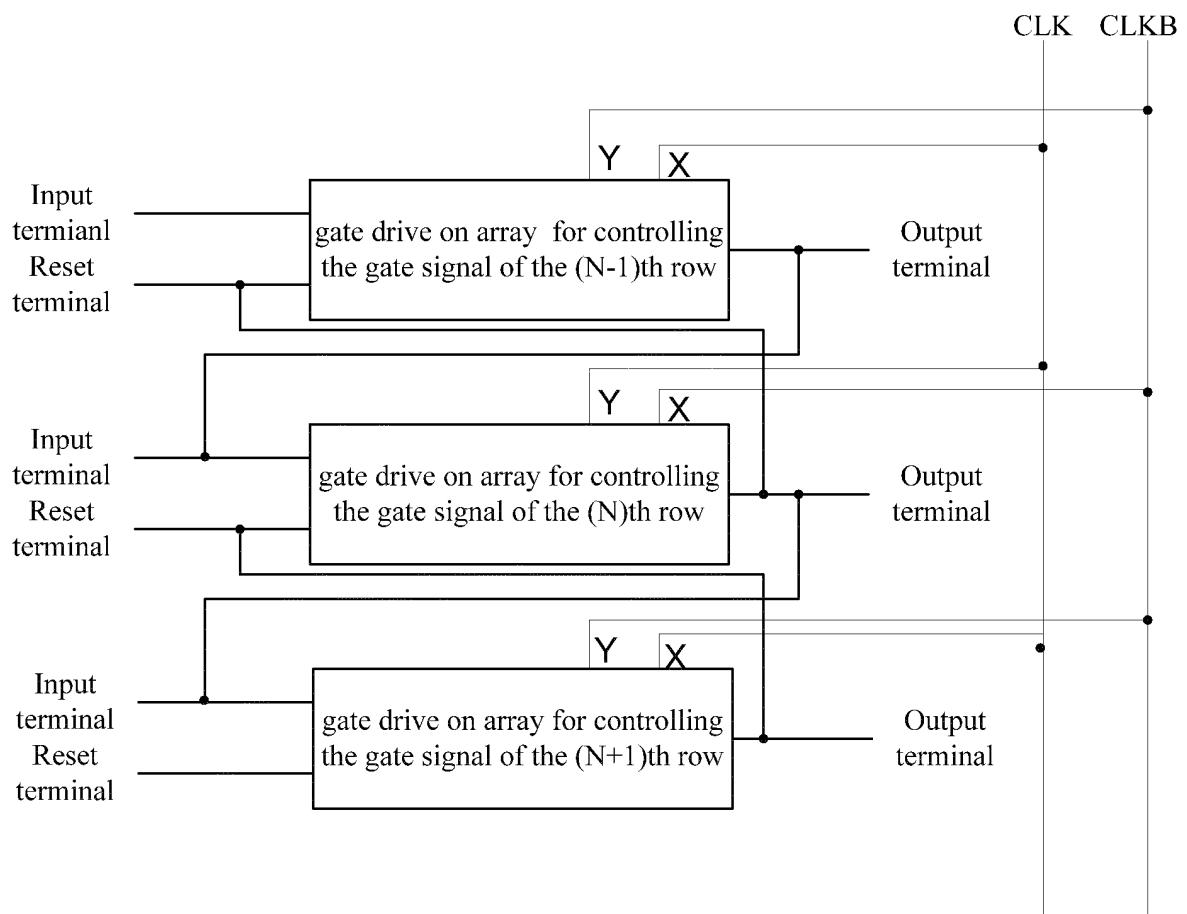


FIG. 3

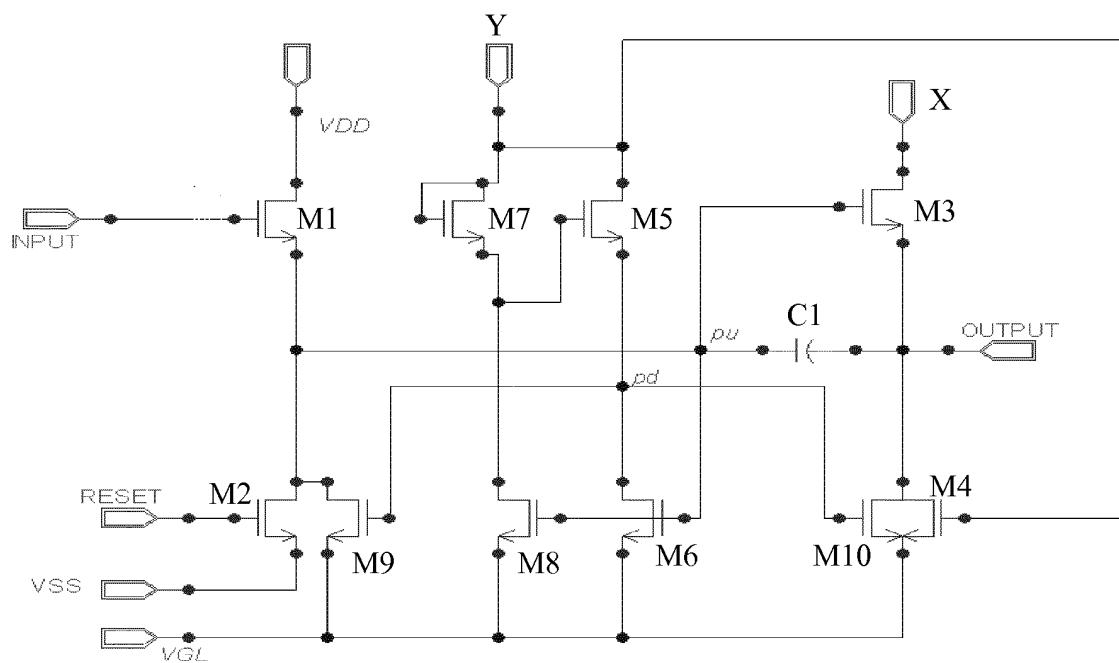


FIG. 4

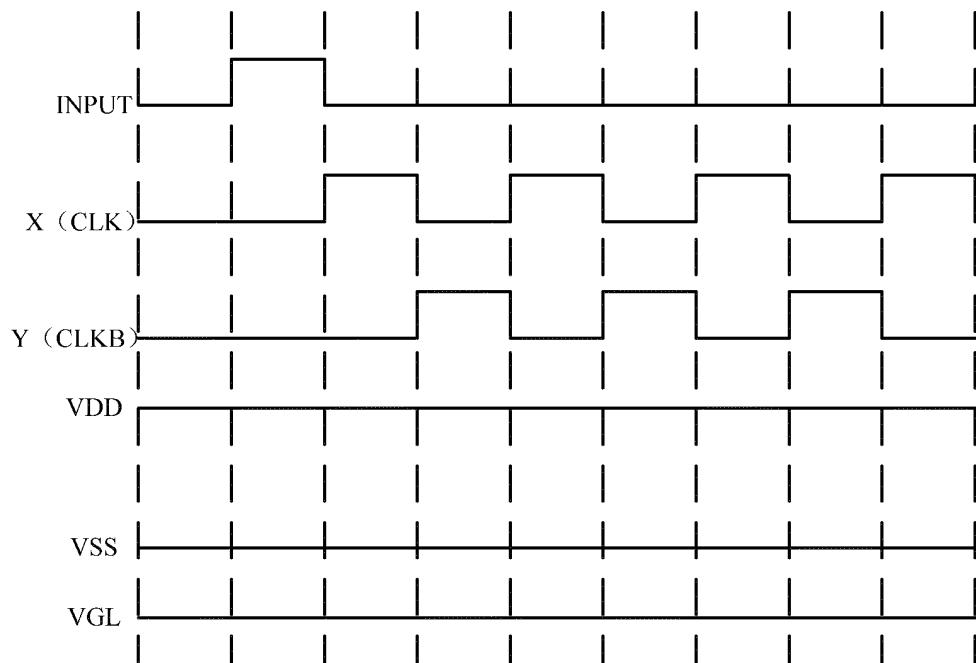


FIG. 5

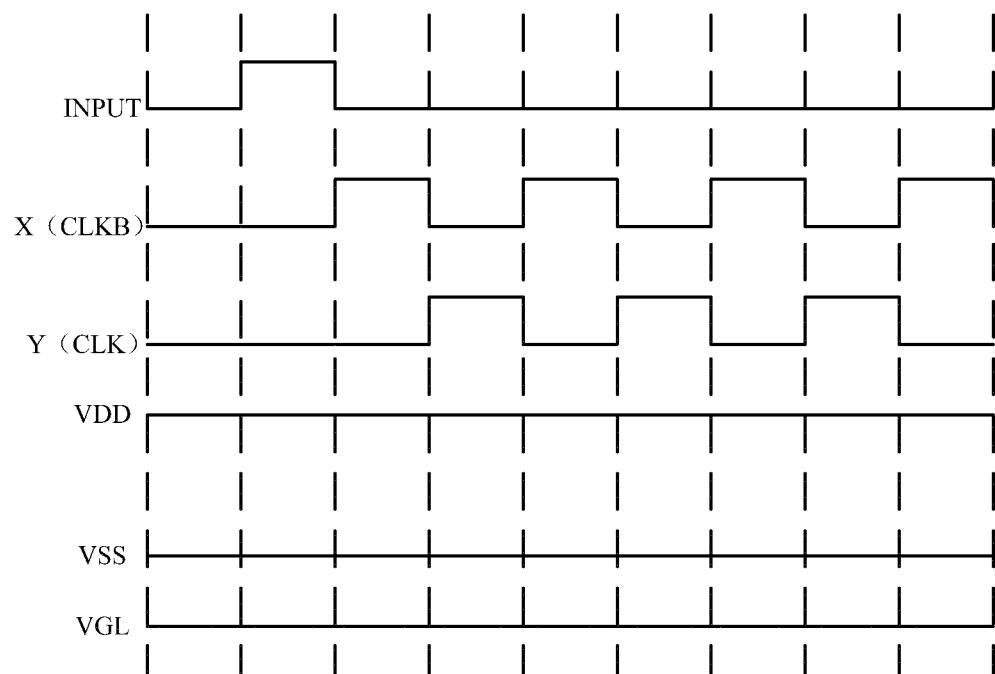


FIG. 6

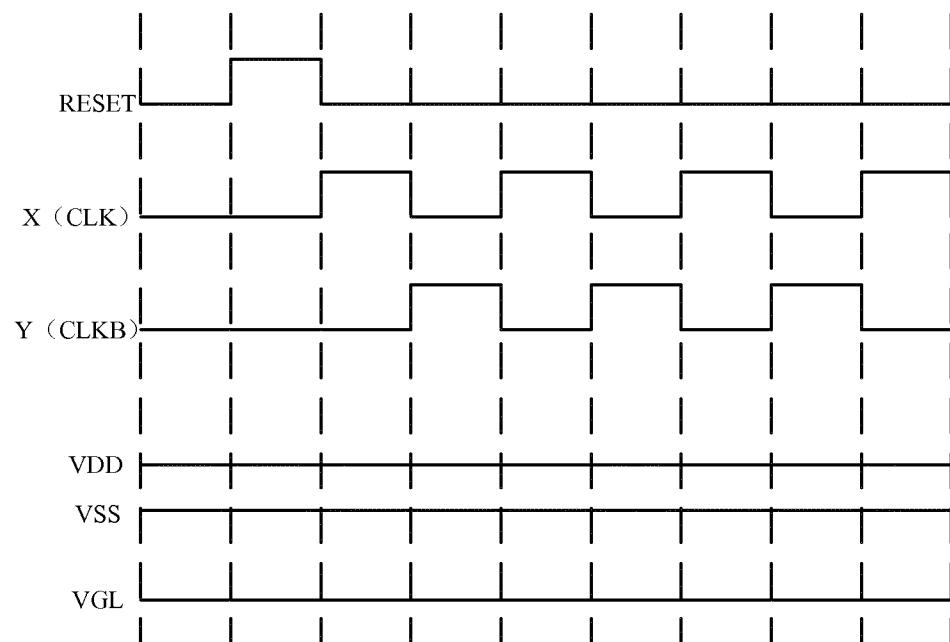


FIG. 7

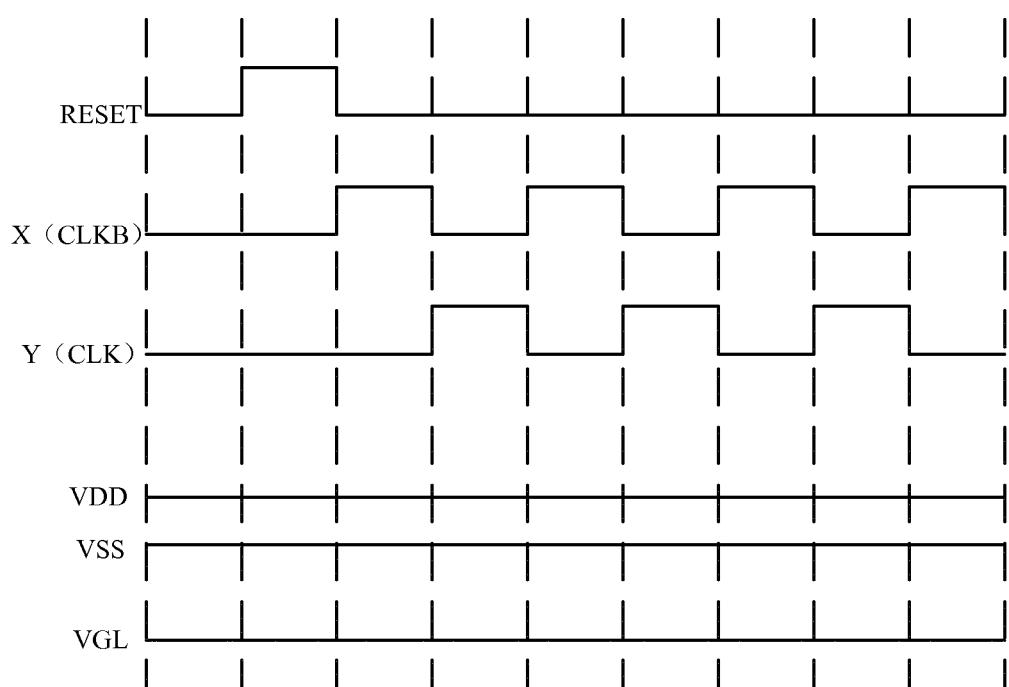


FIG. 8

5	<b>INTERNATIONAL SEARCH REPORT</b>																
10	International application No. PCT/CN2012/080420																
15	<b>A. CLASSIFICATION OF SUBJECT MATTER</b> see the extra sheet According to International Patent Classification (IPC) or to both national classification and IPC																
20	<b>B. FIELDS SEARCHED</b> Minimum documentation searched (classification system followed by classification symbols) IPC: G09G3, G02F1/13+																
25	Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) CNABS,CNTXT,CNKI,VEN:GOA, gate, grid, array, pull+ 1w up, pull+ 1w down, shift register?, TFT, transistor?, capacitor, bidirection, direction																
30	<b>C. DOCUMENTS CONSIDERED TO BE RELEVANT</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: left; padding: 2px;">Category*</th> <th style="text-align: left; padding: 2px;">Citation of document, with indication, where appropriate, of the relevant passages</th> <th style="text-align: left; padding: 2px;">Relevant to claim No.</th> </tr> </thead> <tbody> <tr> <td style="padding: 2px;">PX</td> <td style="padding: 2px;">CN102629444A (BOE TECHNOLOGY GROUP CO., LTD.) 08 Aug.2012(08.08.2012) the whole document</td> <td style="padding: 2px;">1-11</td> </tr> <tr> <td style="padding: 2px;">A</td> <td style="padding: 2px;">CN101093647A (SAMSUNG ELECTRONICS CO., LTD.) 26 Dec.2007 (26.12.2007) description, page 7, the last third line to page 16, line 11 and figures 1-4</td> <td style="padding: 2px;">1-11</td> </tr> <tr> <td style="padding: 2px;">A</td> <td style="padding: 2px;">CN101937718A (AU OPTRONICS CORP) 05 Jan.2011 (05.01.2011) the whole document</td> <td style="padding: 2px;">1-11</td> </tr> <tr> <td style="padding: 2px;">A</td> <td style="padding: 2px;">KR20070105001A (SAMSUNG ELECTRONICS CO., LTD.) 30 Oct.2007 (30.10.2007) the whole document</td> <td style="padding: 2px;">1-11</td> </tr> </tbody> </table>		Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.	PX	CN102629444A (BOE TECHNOLOGY GROUP CO., LTD.) 08 Aug.2012(08.08.2012) the whole document	1-11	A	CN101093647A (SAMSUNG ELECTRONICS CO., LTD.) 26 Dec.2007 (26.12.2007) description, page 7, the last third line to page 16, line 11 and figures 1-4	1-11	A	CN101937718A (AU OPTRONICS CORP) 05 Jan.2011 (05.01.2011) the whole document	1-11	A	KR20070105001A (SAMSUNG ELECTRONICS CO., LTD.) 30 Oct.2007 (30.10.2007) the whole document	1-11
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.															
PX	CN102629444A (BOE TECHNOLOGY GROUP CO., LTD.) 08 Aug.2012(08.08.2012) the whole document	1-11															
A	CN101093647A (SAMSUNG ELECTRONICS CO., LTD.) 26 Dec.2007 (26.12.2007) description, page 7, the last third line to page 16, line 11 and figures 1-4	1-11															
A	CN101937718A (AU OPTRONICS CORP) 05 Jan.2011 (05.01.2011) the whole document	1-11															
A	KR20070105001A (SAMSUNG ELECTRONICS CO., LTD.) 30 Oct.2007 (30.10.2007) the whole document	1-11															
35	<input type="checkbox"/> Further documents are listed in the continuation of Box C. <input checked="" type="checkbox"/> See patent family annex.																
40	* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed																
45	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family																
50	Date of the actual completion of the international search 14 Nov.2012 (14.11.2012)	Date of mailing of the international search report 29 Nov. 2012 (29.11.2012)															
55	Name and mailing address of the ISA State Intellectual Property Office of the P. R. China No. 6, Xitucheng Road, Jimenqiao Haidian District, Beijing 100088, China Facsimile No. (86-10) 62019451 Authorized officer YANG Xi Telephone No. (86-10) 62085797																

5 **INTERNATIONAL SEARCH REPORT**  
 Information on patent family members

International application No.  
 PCT/CN2012/080420

	Patent Documents referred in the Report	Publication Date	Patent Family	Publication Date
10	CN102629444A	08.08.2012	NONE	
	CN101093647A	26.12.2007	CN101093647B	04.01.2012
			EP1870877A2	26.12.2007
			EP1870877A3	07.10.2009
15			JP2008003602A	10.01.2008
			JP5005440B2	22.08.2012
			KR20070121071A	27.12.2007
			KR20080104726A	03.12.2008
20			US2007296662A1	27.12.2007
			US7936332B2	03.05.2011
	CN101937718A	05.01.2011	NONE	
	KR20070105001A	30.10.2007	NONE	
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55	Form PCT/ISA/210 (patent family annex) (July 2009)			

**INTERNATIONAL SEARCH REPORT**

International application No.

PCT/CN2012/080420

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Continuation of second sheet A. CLASSIFICATION OF SUBJECT MATTER

G09G3/20 (2006.01) i

G09G3/36 (2006.01) i

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Form PCT/ISA/210 (extra sheet) (July 2009)

专利名称(译)	门集成驱动电路，移位寄存器和显示屏		
公开(公告)号	<a href="#">EP2750122A1</a>	公开(公告)日	2014-07-02
申请号	EP2012790777	申请日	2012-08-21
[标]申请(专利权)人(译)	北京京东方光电科技有限公司		
申请(专利权)人(译)	北京京东方光电科技有限公司.LTD.		
当前申请(专利权)人(译)	北京京东方光电科技有限公司.LTD.		
[标]发明人	CHEN XI		
发明人	CHEN, XI		
IPC分类号	G09G3/20 G09G3/36		
CPC分类号	G09G3/3674 G09G2300/0408 G09G2310/0283 G09G2310/0286 G09G2310/08 G11C19/28 H03K5/153		
优先权	201110241400.8 2011-08-22 CN		
其他公开文献	<a href="#">EP2750122A4</a>		
外部链接	<a href="#">Espacenet</a>		

### 摘要(译)

本发明实施例涉及液晶显示技术领域，尤其涉及一种阵列上的栅极驱动器，移位寄存器和显示屏。阵列上的栅极驱动器包括：第一TFT，第二TFT，第三TFT，第四TFT，电容器和下拉模块，下拉模块连接在第一时钟信号输入端，第二时钟信号输入端，第一节点和输出端，与低压信号端连接，用于在阵列上的栅极驱动器的非工作期间保持第一节点和输出端处于低电平。因此，阵列上的栅极驱动器可以通过将阵列中的栅极驱动器中的输入端子和复位端子的功能设计为对称地实现而不改变节点的充电 - 放电特性来实现双向扫描，这确保了可靠性和稳定电路。

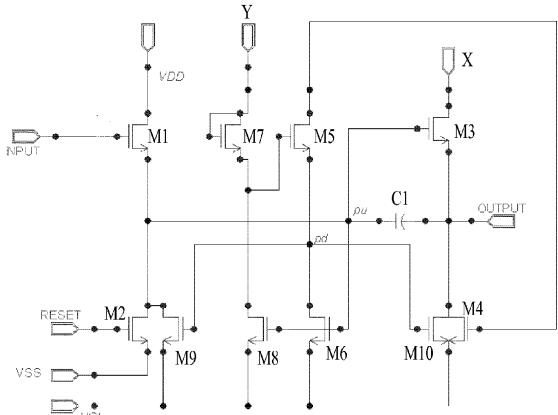


FIG. 4