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(54) **Display driving circuit, display driving method, array substrate and display apparatus**

Anzeigeansteuerungsschaltung, Anzeigeansteuerungsverfahren, Array-Substrat und
Anzeigevorrichtung

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Description

TECHNICAL FIELD OF THE DISCLOSURE

[0001] The present disclosure relates to a field of display technology, and particularly to a display driving circuit, a display driving method, an array substrate and a display apparatus.

BACKGROUND

[0002] In a conventional liquid crystal panel, gates of thin film transistors (TFTs) are scanned by a gate driver, and pixel electrodes are charged through data lines. Liquid crystal molecules are deflected under an effect of the pixel electrical field so as to generate optical rotations, which is a display principle for a liquid crystal display. In a case that a refresh frequency is higher and higher, a time period of a frame reduces and a charging time for the TFT reduces accordingly, wherein a response time of liquid crystal molecules is on the order of millisecond. Taking a refresh frequency 120Hz of a full high definition (FHD) resolution 1920×1080 as an example, a time period of each frame is 8.3ms, and a turning-on time of each row is $8.3/1080 = 7.68 \mu\text{s}$. A scanning backlight technology is usually adopted in a shutter glass 3D display mode, and in order to reduce a crosstalk phenomenon, the backlight is turned on only when the liquid crystal molecules deflect to desired corresponding grayscales.

[0003] JP 2011 203742 A discloses a panel display apparatus in which power consumption is reduced in a driving circuit of a structure only with transistors whose polarities are same and also operation of which is stabilized. US 20070296682A1 discloses a liquid crystal display with improved response speed of the liquid crystals, in which when a first gate driving circuit supplies a gate ON voltage to the N th gate line, where N is a natural number, a second gate driving circuit supplies a pre-charge voltage to the $(N+4n)$ th gate lines, wherein n is a natural number.

[0004] A high refresh frequency will cause that the charging time for the TFT becomes shorter, and the time required for deflecting from one grayscale to another grayscale of the liquid crystal molecules, that is, the response time of the liquid crystal molecules is too long, both of which will cause that the crosstalk phenomenon becomes more severe.

SUMMARY

Technical Problem To Be Solved

[0005] A technical problem to be solved in the present disclosure is how to shorten the response time of the liquid crystal molecules to accommodate the higher refresh frequency.

Technical Solution

[0006] The problem is solved by the features of the respective independent claims. Further embodiments and developments are defined in the respective dependent claims.

Benefit Effect

[0007] The display driving circuit according to the embodiments of the present invention inserts black levels to pixels in a region according to a region division before charging the pixels, that is, supplies a pre-charging voltage to TFTs in the region according to the region division, the liquid crystal molecule will be deflected at first under such pre-charging voltage, so that the time required for deflecting to an accurate position corresponding to a desired grayscale of the liquid crystal molecule will be reduced when the voltage to be charged is supplied on the liquid crystal molecule, thereby may accommodate a higher refresh frequency.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008]

Fig.1 is a schematic structure diagram of a display driving circuit according to an embodiment of the present disclosure;

Fig.2 is a timing chart of signals as driving to display; Fig.3 is a schematic structure diagram of connection between the display driving circuit as shown in Fig. 1 and gate lines on an array substrate; and

Fig.4 is a flowchart of a display driving method according to an embodiment of the present disclosure.

DETAILED DESCRIPTION

[0009] Particular implementations of the present disclosure will be described below in detail in combination with the accompanying drawings and the embodiments of the present disclosure, which are only illustrative and give no limitation to the scope of the present disclosure.

[0010] As shown in Fig.1, a display driving circuit according to an embodiment of the present disclosure comprises N gate driving units 100 connected to N gate lines on an array substrate, respectively, and further comprises a timing control unit 200, n pre-charging units 300 and n scanning control units 400. The N gate driving units 100, the n pre-charging units 300 and the n scanning control units 400 are all connected to the timing control unit 200, wherein n represents a number of groups into which the N gate lines on the array substrate are divided in advance and is an integer greater than or equal to 2. That is to say, the N gate lines on the array substrate are divided into n groups, for example, taking a television with 120Hz and a FHD resolution as an example, both the numbers of the gate driving units 100 and the number

of the gate lines are 1080, then the 1080 gate lines are divided into four groups, each of which comprises 270 gate lines.

[0011] The n pre-charging units 300 are connected to the n gate line groups divided in advance on the array substrate, respectively, the timing control unit 200 is used to control the gate driving units 100 to input scanning signals to the gate lines; the timing control unit 200 is further used to control an i^{th} pre-charging unit 300 to insert a pre-charging signal to an i^{th} gate line group before the scanning signals are input to the gate lines in the i^{th} gate line group, and control an i^{th} scanning control unit 400 to pause the input of scanning signals at the same time. The pre-charging signal is used to turn on thin film transistors connected to the gate lines in the gate line group on the array substrate, thus the timing control unit controls the data lines to pre-charge pixel units connected to the thin film transistors, such that liquid crystal molecules are deflected at first under an effect of a pre-charging voltage corresponding to the pre-charging signal. The controlling of the timing control unit on the data lines may be implemented by controlling driving units of the data lines.

[0012] After the insertion of the pre-charging signal is completed, the i^{th} scanning control unit 400 triggers the gate driving units 100 corresponding to the i^{th} gate line group to input scanning signals to the gate lines in the i^{th} gate line group, respectively, wherein $i = 1, 2, \dots, n$.

[0013] The display driving circuit according to the embodiments of the present disclosure inserts black levels to pixels in a region according to a region division before charging the pixels, that is, supplies a pre-charging voltage to TFTs in the region according to the region division, the driving timing is as illustrated in Fig.2. The liquid crystal molecules will be deflected at first under such pre-charging voltage, and then an actual charging voltage is applied to the liquid crystal molecule in order to make the liquid crystal molecule deflect to an accurate position corresponding to a desired grayscale, so that a response time of the liquid crystal molecule is reduced, thereby may accommodate a higher refresh frequency.

[0014] Since the gate driving unit 100 is usually a shift register and is connected to the gate line together with the pre-charging unit 300, the pre-charging process performed by the pre-charging unit 300 will affect an operation of the shift register. Therefore, in an example, the display driving circuit according to the embodiment of the present disclosure further comprises: N first switches 500 connected to the timing control unit 200 and connected to the N gate driving units 100, respectively, the N first switches 500 are used to connect the N gate driving units 100 to the N gate lines respectively. The timing control unit 200 is further used to turn off all of the first switches 500 when the i^{th} pre-charging unit 300 inserts the pre-charging signal into the i^{th} gate line group and turn on all of the first switches 500 when the gate driving units 100 input the scanning signals.

[0015] The first switches 500 may be MOS transistors,

each of the MOS transistor has a gate connected to the timing control unit 200, and a source and a drain thereof are connected to a corresponding gate driving unit 100 and a corresponding gate line, respectively.

[0016] In an example, the pre-charging unit 300 may be a controller with a one-way structure and also may be a shift register. If the pre-charging unit 300 is a shift register, the display driving circuit according to the embodiment of the present disclosure may further comprise: n second switches (not shown) connected to the timing control unit 200 and connected to the n pre-charging units 300, respectively, the n second switches are used to connect the n pre-charging units 300 to the n gate line groups, respectively. That is, the n second switches are connected between the n pre-charging units 300 and the n gate line groups, respectively, and are used to control connections or disconnections between the pre-charging units 300 and the respective gate line groups under the control of the timing control unit 200. The timing control unit 200 is further used to turn off the second switches when the gate driving units 100 input the scanning signals and turn on the second switches when the pre-charging units 300 input the pre-charging signals.

[0017] The second switches may be MOS transistors, each of the MOS transistors has a gate connected to the timing control unit 200, a source and a drain thereof are connected to a corresponding pre-charging unit 300 and a corresponding gate line on the array substrate respectively.

[0018] For a shutter 3D display, in an example, the display driving circuit according to the embodiment of the present disclosure may further comprise a backlight driving unit 600 connected to the timing control unit 200. The timing control unit is further used to control the backlight driving unit to drive an i^{th} backlight source to emit light after the scanning of the gate lines in the i^{th} gate line group is completed, a $((i \bmod n) + 1)^{\text{th}}$ pre-charging unit is turned on after the i^{th} backlight source emits light.

[0019] Since the backlight source is turned on after the response of the liquid crystal molecules are completed, for a same refresh period, shorter the response time of the liquid crystal molecules is, longer the turn-on period of the backlight source is and higher the luminance of the displayed picture may be. In addition, shorter the response period of the liquid crystal molecules is, smaller the crosstalk phenomenon is correspondingly.

[0020] The display driving circuit according to the present disclosure may be manufactured on the array substrate by a Gate Drive on Array (GOA) technology. As shown in Fig.3, the array substrate comprises N gate lines 700 being divided into n groups, as well as the above described display driving circuit. The N gate driving units 100 are connected to the N gate lines 700 respectively, and the n pre-charging units 300 are connected to the n gate line groups respectively.

[0021] In order to make the luminance of displayed pictures more even, numbers of the gate lines in each of the n gate line groups may be same.

[0022] A display driving method of the above display driving circuit is shown in Fig.4 and comprises steps of:

At step S401: pre-charging pixel units controlled by gate lines in an i^{th} gate line group and stopping inputting scanning signals to the gate lines at the same time;

At step S402: scanning the gate lines in the i^{th} gate line group sequentially after the pre-charging to the i^{th} gate line group is completed;

At step S403: setting i to $((i \bmod n) + 1)$ after the scanning of the gate lines in the i^{th} gate line group is completed. When $(i \bmod n) = 0$, that is, a frame has been completely scanned, the scanning of a next frame may be started.

[0023] Steps of S401 to S403 are repeatedly performed to display a picture.

[0024] For a shutter 3D display, in the step S403, after the scanning of the gate lines in the i^{th} gate line group is completed, the backlight source corresponding to the i^{th} gate line group is turned on, and i is set to $((i \bmod n) + 1)$ after the backlight source is turned on.

[0025] In the embodiments of the present disclosure, there is further provided a display apparatus comprising the above display driving circuit or the above array substrate. The display apparatus may be a liquid crystal display (LCD) panel, a liquid crystal display television (LCD TV), a liquid crystal display (LCD) monitor, a digital photo frame, a mobile phone, a tablet PC and other product or part having a display function.

[0026] The above descriptions are only for illustrating the embodiments of the present disclosure, and in no way limit the scope of the present disclosure. It will be obvious that those skilled in the art may make modifications, variations and equivalences to the above embodiments without departing the scope of the present disclosure as defined by the following claims. Such variations and modifications are intended to be comprised within the scope of the present disclosure.

Claims

1. A display driving circuit for driving a liquid crystal display panel, said display driving circuit comprising N gate driving units (100) connectable to N gate lines (700) on an array substrate of said liquid crystal display panel, respectively, a timing control unit (200), n pre-charging units (300) and n scanning control units (400), wherein N gate driving units (100), the n pre-charging units (300) and the n scanning control units (400) are all connected to the timing control unit (200), wherein n represents a number of groups into which the N gate lines (700) on the array substrate are divided and is an integer greater than or equal to 2, wherein the n pre-charging units (300) are connectable to the n gate line groups, respec-

tively, and wherein the timing control unit (200) is configured to control the gate driving units (100) to apply scanning signals to the gate lines (700) and to control the pre-charging units (300) to apply pre-charging signals into the gate lines (700), group by group; the timing control unit (200) being configured, for an i^{th} gate line group,

1) to control an i^{th} pre-charging unit to simultaneously apply a pre-charging signal to all gate lines of said i^{th} gate line group while a pre-charging voltage corresponding to a black level is applied to data lines, the pre-charging signal being configured to turn-on thin film transistors within pixel units controlled by the gate lines in the i -th gate line group, and

2) after completion of the pre-charging to the i -th gate line group to control an i^{th} scanning control unit to control the gate driving units corresponding to the i^{th} gate line group to sequentially output scanning signals to the gate lines in the i^{th} gate line group while charging voltages corresponding to desired greyscales are applied to the data lines, wherein $i = 1, 2, \dots, n$.

2. The display driving circuit of claim 1, **characterized in that** the display driving circuit further comprises N first switches (500) connected to the timing control unit (200) and connected to the N gate driving units (100), respectively, the N first switches (500) being configured to connect the N gate driving units (100) to the N gate lines (700), respectively, and the timing control unit (200) being further configured to turn off the first switches (500) when the i^{th} pre-charging unit outputs the pre-charging signal into the i^{th} gate line group and to turn on the first switches (500) when the gate driving units output the scanning signals.

3. The display driving circuit of claim 2, **characterized in that** the first switches (500) are MOS transistors, each of the MOS transistor having a gate connected to the timing control unit (200), a source and a drain thereof being connected to a corresponding gate driving unit (100) and a corresponding gate line (700), respectively.

4. The display driving circuit of any one of claims 1-3, **characterized in that** the display driving circuit further comprises n second switches connected to the timing control unit (200) and connected to the n pre-charging units (300), respectively, the n second switches being configured to connect the n pre-charging units (300) to the n gate line groups, respectively, the timing control unit (200) being further configured to turn off the second switches when the gate driving units (100) output the scanning signals and turn on the second switches when the pre-charging units (300) output the pre-charging signals.

5. The display driving circuit of claim 4, **characterized in that** the second switches are MOS transistors, each of the MOS transistors having a gate connected to the timing control unit (200), a source and a drain thereof being connected to a corresponding pre-charging unit (300) and a corresponding gate line (700), respectively 5
6. The display driving circuit of any one of claims 1-5, **characterized in that** the display driving circuit further comprises a backlight driving unit (600) connected to the timing control unit (200), and the timing control unit (200) is further configured to control the backlight driving unit (600) to drive an i^{th} backlight source to emit light after the scanning of the gate lines of the i^{th} gate line group is completed, and to turn on $((i \bmod n) + 1)^{\text{th}}$ pre-charging unit after the i^{th} backlight source emits light. 10
7. A liquid crystal display apparatus, **characterized in that** the display apparatus comprises the display driving circuit of any one of claims 1-6. 15
8. An array substrate of a liquid crystal display apparatus, wherein the array substrate comprises N gate lines being divided into n groups, **characterized in that** the array substrate further comprises the display driving circuit of any one of claims 1-6, the N gate driving units (100) being connected to the N gate lines (700), respectively, and the n pre-charging units (300) being connected to the n gate line groups, respectively, wherein n is an integer greater than or equal to 2. 20
9. The array substrate of claim 8, **characterized in that** the number of the gate lines (700) in each of the n gate line groups is identical. 25
10. A liquid crystal display apparatus, **characterized in that** the display apparatus comprises the array substrate of any one of claims 8-9. 30
11. A display driving method for a liquid crystal display panel comprising N gate lines on an array substrate divided in n groups, n being an integer greater than or equal to 2, **characterized in that** the display driving method comprises the steps of: 35

S1: simultaneously pre-charging pixel units controlled by gate lines in an i^{th} gate line group by applying a pre-charging signal into the gate lines of said i^{th} gate line group while applying a pre-charging voltage corresponding to a black level to data lines, the pre-charging signals being configured to turn on thin film transistors within said pixel units controlled by the gate lines in said i^{th} gate line group; 40

S2: after completion of the pre-charging to the 45

i^{th} gate line group, sequentially outputting scanning signals to the gate lines of the i^{th} gate line group, and applying charging voltages corresponding to desired grayscales on the data lines;

S3: setting i to $((i \bmod n) + 1)$ after the scanning of the gate lines in the i^{th} gate line group is completed, wherein n is the number of the gate line groups;

performing the steps of S1 to S3 repeatedly to display a pictures.

12. The display driving method of claim 11, wherein in the step S3, after the completion of the scanning of the gate lines in the i^{th} gate line group, the backlight corresponding to the i^{th} gate line group is turned on, and i is set to $((i \bmod n) + 1)$ after the backlight is turned on. 50

Patentansprüche

1. Anzeigeansteuerschaltung zum Ansteuern eines Flüssigkristallanzeige-Panels, wobei die Anzeigeansteuerschaltung aufweist N Gate-Ansteuereinheiten (100), die jeweils mit N Gate-Leitungen (700) auf einem Array-Substrat des Flüssigkristallanzeige-Panels verbindbar sind, eine Zeitsteuerungseinheit (200), n Vorladeeinheiten (300) und n Abtaststeuereinheiten (400), wobei die N Gate-Ansteuereinheiten (100), die n Vorladeeinheiten (300) und die n Abtaststeuereinheiten (400) alle mit der Zeitsteuerungseinheit (200) verbunden sind, wobei n für eine Anzahl von Gruppen steht, in welche die N Gate-Leitungen (700) auf dem Array-Substrat unterteilt sind, und eine ganze Zahl größer als oder gleich 2 ist, wobei die n Vorladeeinheiten (300) jeweils mit den n Gate-Leitungsgruppen verbindbar sind, und wobei die Zeitsteuerungseinheit (200) konfiguriert ist, die Gate-Ansteuereinheiten (100) zu steuern, Abtastsignale an die Gate-Leitungen (700) anzulegen, und die Vorladeeinheiten (300) zu steuern, Vorladesignale in die Gate-Leitungen (700) einzuspeisen, Gruppe für Gruppe; 55

1) eine i -te Vorladeeinheit zu steuern, gleichzeitig ein Vorladesignal an alle Gate-Leitungen der i -te Gate-Leitungsgruppe anzulegen, während eine Vorladespannung, die einem Schwarzpegel entspricht, an Daten-Leitungen angelegt ist, wobei das Vorladesignal konfiguriert ist, Dünnschichttransistoren in Pixeleinheiten, die durch die Gate-Leitungen in der i -te Gate-Leitungsgruppe gesteuert werden, einzuschalten, und 2) Nach Abschluss des Vorladens der i -te Gate-

- Leitungsgruppe eine i-te Abtaststeuereinheit zu steuern, die Gate-Ansteuereinheiten, die der i-te Gate-Leitungsgruppe entsprechen, zu steuern, sequentiell Abtastsignale auszugeben an die Gate-Leitungen in der i-te Gate-Leitungsgruppe auszugeben, während Ladespannungen, die gewünschten Graustufen entsprechen, an die Datenleitungen angelegt sind, wobei $i=1, 2, \dots, n$ ist.
2. Anzeigeansteuerschaltung gemäß Anspruch 1, **dadurch gekennzeichnet, dass** die Anzeigesteuerschaltung weiter aufweist N erste Schalter (500), die mit der Ansteuereinheit (200) verbunden sind und jeweils mit den N Gate-Ansteuereinheiten (100) verbunden sind, wobei die N ersten Schalter (500) konfiguriert sind, die N Gate-Ansteuereinheiten (100) jeweils mit den N Gate-Leitungen (700) zu verbinden, und die Zeitsteuereinheit (200) weiter konfiguriert ist, die ersten Schalter (500) auszuschalten, wenn die i-te Vorladeeinheit das Vorladesignal in die i-te Gate-Leitungsgruppe einspeist, und den ersten Schalter (500) einzuschalten, wenn die Gate-Ansteuereinheiten die Abtastsignale ausgeben.
 3. Anzeigeansteuerschaltung gemäß Anspruch 2, **dadurch gekennzeichnet, dass** die ersten Schalter (500) MOS-Transistoren sind, wobei jeder der MOS-Transistoren ein Gate aufweist, das mit der Zeitsteuereinheit (200) verbunden ist, wobei eine Source und einen Drain davon jeweils mit einer zugehörigen Gate-Ansteuereinheit (100) bzw. einer zugehörigen Gate-Leitung (700) verbunden sind.
 4. Anzeigeansteuerschaltung gemäß einem der Ansprüche 1 bis 3, **dadurch gekennzeichnet, dass** die Anzeigeansteuerschaltung weiter aufweist n zweite Schalter, die mit der Zeitsteuereinheit (200) verbunden sind und jeweils mit den n Vorladeeinheiten (300) verbunden sind, wobei die n zweiten Schalter konfiguriert sind, die n Vorladeeinheiten (300) jeweils mit den n Gate-Leitungsgruppen zu verbinden, wobei die Zeitsteuereinheit (200) weiter konfiguriert ist, die zweiten Schalter auszuschalten, wenn die Gate-Ansteuereinheiten (100) die Abtastsignale ausgeben und die zweiten Schalter einzuschalten, wenn die Vorladeeinheiten (300) die Vorladesignale ausgeben.
 5. Anzeigeansteuerschaltung gemäß Anspruch 4, **dadurch gekennzeichnet, dass** die zweiten Schalter MOS-Transistoren sind, wobei jeder der MOS-Transistoren ein Gate aufweist, das mit der Zeitsteuereinheit (200) verbunden ist, wobei eine Source und einen Drain davon mit einer zugehörigen Vorladeeinheit (300) bzw. einer zugehörigen Gate-Leitung (700) verbunden sind.
 6. Anzeigeansteuerschaltung gemäß einem der Ansprüche 1 bis 5, **dadurch gekennzeichnet, dass** die Anzeigeansteuerschaltung weiter aufweist eine Hintergrundbeleuchtungsansteuereinheit (600), die mit der Zeitsteuereinheit (200) verbunden ist, und wobei die Steuereinheit (200) weiter konfiguriert ist, die Hintergrundbeleuchtungsansteuereinheit (600) anzusteuern, eine i-te Hintergrundbeleuchtungsquelle anzusteuern, Licht abzustrahlen, nachdem das Abtasten der Gate-Leitungen der i-te Gate-Leitungsgruppe abgeschlossen ist, und eine $((i \bmod n) + 1)$ -te Vorladeeinheit einzuschalten, nachdem die i-te Hintergrundbeleuchtungsquelle Licht abstrahlt.
 7. Flüssigkristallanzeigevorrichtung, **dadurch gekennzeichnet, dass** die Anzeigevorrichtung die Anzeigeansteuerschaltung gemäß einem der Ansprüche 1 bis 6 aufweist.
 8. Array-Substrat einer Flüssigkristallanzeigevorrichtung, wobei das Array-Substrat aufweist N Gate-Leitungen, die in n Gruppen unterteilt sind, **dadurch gekennzeichnet, dass** das Array-Substrat weiter die Anzeigeansteuerschaltung gemäß einem der Ansprüche 1 bis 6 aufweist, wobei die N Gate-Ansteuereinheiten (100) jeweils mit den N Gate-Leitungen (700) verbunden sind und die n Vorladeeinheiten (300) jeweils mit den n Gate-Leitungsgruppen verbunden sind, wobei n eine ganze Zahl größer als oder gleich 2 ist.
 9. Array-Substrat gemäß Anspruch 8, **dadurch gekennzeichnet, dass** die Anzahl der Gate-Leitungen (700) in jeder der n Gate-Leitungsgruppen gleich ist.
 10. Flüssigkristallanzeigevorrichtung, **dadurch gekennzeichnet, dass** die Anzeigevorrichtung das Array-Substrat gemäß einem der Ansprüche 8 bis 9 aufweist.
 11. Anzeigeansteuerungsverfahren für ein Flüssigkristallanzeigepanel, welches aufweist N Gate-Leitungen auf einem Array-Substrat, die in n Gruppen unterteilt sind, wobei n eine ganze Zahl größer oder gleich 2 ist, **dadurch gekennzeichnet, dass** das Anzeigeansteuerungsverfahren die Schritte aufweist des:

S1: gleichzeitiges Vorladen von Pixeleinheiten, die durch Gate-Leitungen in einer i-te Gate-Leitungsgruppe gesteuert werden, durch Anlegen eines Vorladesignals an die Gate-Leitungen der i-te Gate-Leitungsgruppe, während Anlegens einer Vorladespannung, die einem Schwarzpegel entspricht, an Daten-Leitungen, wobei das Vorladesignal konfiguriert ist, Dünnschichttransistoren in den Pixeleinheiten, die durch die Gate-Leitungen in der i-te Gate-Leitungsgruppe

gesteuert werden, einzuschalten;

S2: nach Abschluss des Vorladens der i-te Gate-Leitungsgruppe sequentielles Ausgeben von Abtastsignalen an die Gate-Leitungen der i-te Gate-Leitungsgruppe und Anlegen von Vorladespannungen, die gewünschten Graustufen entsprechen, an die Datenleitungen;

S3: Einstellen i auf $((i \bmod n) + 1)$ nachdem das Abtasten der Gate-Leitungen in der i-te Gate-Leitungsgruppe abgeschlossen wurde, wobei n die Anzahl der Gate-Leitungsgruppen ist;

Durchführen der Schritte S1 bis S3 wiederholt, um Bilder anzuzeigen.

12. Anzeigeansteuerungsverfahren gemäß Anspruch 11, wobei in dem Schritt S3, nach dem Abschluss des Abtastens der Gate-Leitungen in der i-te Gate-Leitungsgruppe, die Hintergrundbeleuchtung entsprechend der i-te Gate-Leitungsgruppe eingeschaltet wird, und i eingestellt wird auf $((i \bmod n) + 1)$, nachdem die Hintergrundbeleuchtung eingeschaltet wurde.

Revendications

1. Circuit de pilotage d'affichage destiné à piloter un panneau d'affichage à cristaux liquides, ledit circuit de pilotage d'affichage comprenant N unités de pilotage de grille (100) pouvant être connectées respectivement à N lignes de grille (700) sur un substrat de réseau dudit panneau d'affichage à cristaux liquides, une unité de commande de temporisation (200), n unités de précharge (300) et n unités de pilotage de balayage (400), dans lequel les N unités de pilotage de grille (100), les n unités de précharge (300) et les n unités de commande de balayage (400) sont toutes connectées à l'unité de commande de temporisation (200), où n représente un nombre de groupes par lequel les N lignes de grille (700) sur le substrat de réseau sont divisées et est un entier supérieur ou égal à 2, dans lequel les n unités de précharge (300) peuvent être connectées respectivement aux n groupes de lignes de grille, et dans lequel l'unité de commande de temporisation (200) est configurée pour commander les unités de pilotage de grille (100) afin d'appliquer des signaux de balayage aux lignes de grille (700), et pour commander les unités de précharge (300) afin d'appliquer des signaux de précharge dans les lignes de grille (700), groupe par groupe, l'unité de commande de temporisation (200) étant configurée, pour un $j^{\text{ème}}$ groupe de lignes de grille pour :

- 1) commander une $j^{\text{ème}}$ unité de précharge et appliquer simultanément un signal de précharge à toutes les lignes de grille dudit $j^{\text{ème}}$ groupe de

lignes de grille tandis qu'une tension de précharge correspondant à un niveau de noir est appliquée aux lignes de données, le signal de précharge étant configuré pour rendre passants des transistors à couches minces dans des unités de pixel commandées par les lignes de grille dans le $j^{\text{ème}}$ groupe de lignes de grille, et 2) au terme du précharge vers le $j^{\text{ème}}$ groupe de lignes de grille, pour commander une $j^{\text{ème}}$ unité de commande de balayage pour commander les unités de commande de grille correspondant au $j^{\text{ème}}$ groupe de lignes de grille afin de produire de manière séquentielle des signaux de balayage vers les lignes de grille dans le $j^{\text{ème}}$ groupe de lignes de grille tandis que des tensions de charge correspondant aux échelles de gris souhaitées sont appliquées aux lignes de données, où $i = 1, 2, \dots, n$.

2. Circuit de pilotage d'affichage selon la revendication 1, **caractérisé en ce que** le circuit de pilotage d'affichage comprend en outre N premiers commutateurs (500) connectés à l'unité de commande de temporisation (200) et connectés respectivement aux N unités de pilotage de grille (100), les N premiers commutateurs (500) étant configurés pour connecter les N unités de pilotage de grille (100) respectivement aux N lignes de grille (700), et l'unité de commande de temporisation (200) étant en outre configurée pour rendre bloquants les premiers commutateurs (500) lorsque la $j^{\text{ème}}$ unité de précharge produit le signal de précharge dans le $j^{\text{ème}}$ groupe de lignes de grille et rendre passants les premiers commutateurs (500) lorsque les unités de pilotage de grille produisent les signaux de balayage.
3. Circuit de pilotage d'affichage selon la revendication 2, **caractérisé en ce que** les premiers commutateurs (500) sont des transistors MOS, chacun des transistors MOS présentant une grille connectée à l'unité de commande de temporisation (200), dont une source et un drain sont connectés respectivement à une unité de pilotage de grille correspondante (100) et une ligne de grille correspondante (700).
4. Circuit de pilotage d'affichage selon l'une quelconque des revendications 1 à 3, **caractérisé en ce que** le circuit de pilotage d'affichage comprend en outre n seconds commutateurs connectés respectivement à l'unité de commande de temporisation (200) et connectés aux unités de précharge (300), les n seconds commutateurs étant configurés pour connecter respectivement les n unités de précharge (300) aux n groupes de lignes de grille, l'unité de commande de temporisation (200) étant en outre configurée pour rendre bloquants les seconds commutateurs lorsque les unités de pilotage de grille (100) produisent les signaux de balayage et rendre passants les

seconds commutateurs lorsque les unités de précharge (300) produisent les signaux de précharge.

5. Circuit de pilotage d'affichage selon la revendication 4, **caractérisé en ce que** les seconds commutateurs sont des transistors MOS, chacun des transistors MOS présentant une grille connectée à l'unité de commande de temporisation (200), dont une source et un drain sont connectés respectivement à une unité de précharge (300) et à une ligne de grille correspondante (700). 5 10
6. Circuit de pilotage d'affichage selon l'une quelconque des revendications 1 à 5, **caractérisé en ce que** le circuit de pilotage d'affichage comprend en outre une unité de pilotage de rétroéclairage (600) connectée à l'unité de commande de temporisation (200), et l'unité de commande de temporisation (200) est en outre configurée pour commander l'unité de pilotage de rétroéclairage (600) pour piloter une $i^{\text{ème}}$ source de rétroéclairage afin d'émettre une lumière au terme du balayage des lignes de grille du $i^{\text{ème}}$ groupe de lignes de grille, et pour rendre passante la $((i \bmod n) + 1)^{\text{ème}}$ unité de précharge après émission de lumière par la $i^{\text{ème}}$ source de rétroéclairage. 15 20 25
7. Appareil d'affichage à cristaux liquides, **caractérisé en ce que** l'appareil d'affichage comprend le circuit de pilotage d'affichage selon l'une quelconque des revendications 1 à 6. 30
8. Substrat de réseau pour appareil d'affichage à cristaux liquides, dans lequel le substrat de réseau comprend N lignes de grilles divisées en n groupes, **caractérisé en ce que** le substrat de réseau comprend en outre le circuit de pilotage d'affichage selon l'une quelconque des revendications 1 à 6, les N unités de pilotage de grille (100) étant connectées respectivement aux N lignes de grille (700), et les n unités de précharge (300) étant respectivement connectées aux n groupes de lignes de grille, où n est un entier supérieur ou égal à 2. 35 40
9. Substrat de réseau selon la revendication 8, **caractérisé en ce que** le nombre des lignes de grille (700) dans chacun des n groupes de lignes de grille est identique. 45
10. Appareil d'affichage à cristaux liquides, **caractérisé en ce que** l'appareil d'affichage comprend le substrat de réseau selon l'une quelconque des revendications 8 à 9. 50
11. Procédé de pilotage d'affichage destiné à un panneau d'affichage à cristaux liquides, comprenant N lignes de grille sur un substrat de réseau divisées en n groupes, n étant un entier supérieur ou égal à 2, **caractérisé en ce que** le procédé de pilotage d'affichage comprend les étapes pour : 55

fichage comprend les étapes pour :

S1 : précharger simultanément des unités de pixel commandées par des lignes de grille dans un $i^{\text{ème}}$ groupe de lignes de grille, en appliquant un signal de précharge dans les lignes de grille dudit $i^{\text{ème}}$ groupe de lignes de grille tout en appliquant une tension de précharge correspondant à un niveau de noir aux lignes de données, le signal de précharge étant configuré pour rendre passants des transistors à couches minces dans des unités de pixel commandées par les lignes de grille dans ledit $i^{\text{ème}}$ groupe de lignes de grille ;
 S2 : au terme du précharge vers le $i^{\text{ème}}$ groupe de lignes de grille, produire de manière séquentielle des signaux de balayage vers les lignes de grille du $i^{\text{ème}}$ groupe de lignes de grille, et appliquer des tensions de charge correspondant aux échelles de gris souhaitées aux lignes de données ;
 S3 : régler i sur $((i \bmod n) + 1)$ au terme du balayage des lignes de grille dans le $i^{\text{ème}}$ groupe de lignes de grille, où n est le nombre de groupes de lignes de grille, et

exécuter les étapes S1 à S3 de manière répétée pour afficher une image.

12. Procédé de pilotage d'affichage selon la revendication 11, dans lequel lors de l'étape S3, au terme du balayage des lignes de grille dans le $i^{\text{ème}}$ groupe de lignes de grille, le rétroéclairage correspondant au $i^{\text{ème}}$ groupe de lignes de grille est rendu passant, et i est réglé sur $((i \bmod n) + 1)$ après passage du rétroéclairage sur l'état passant.

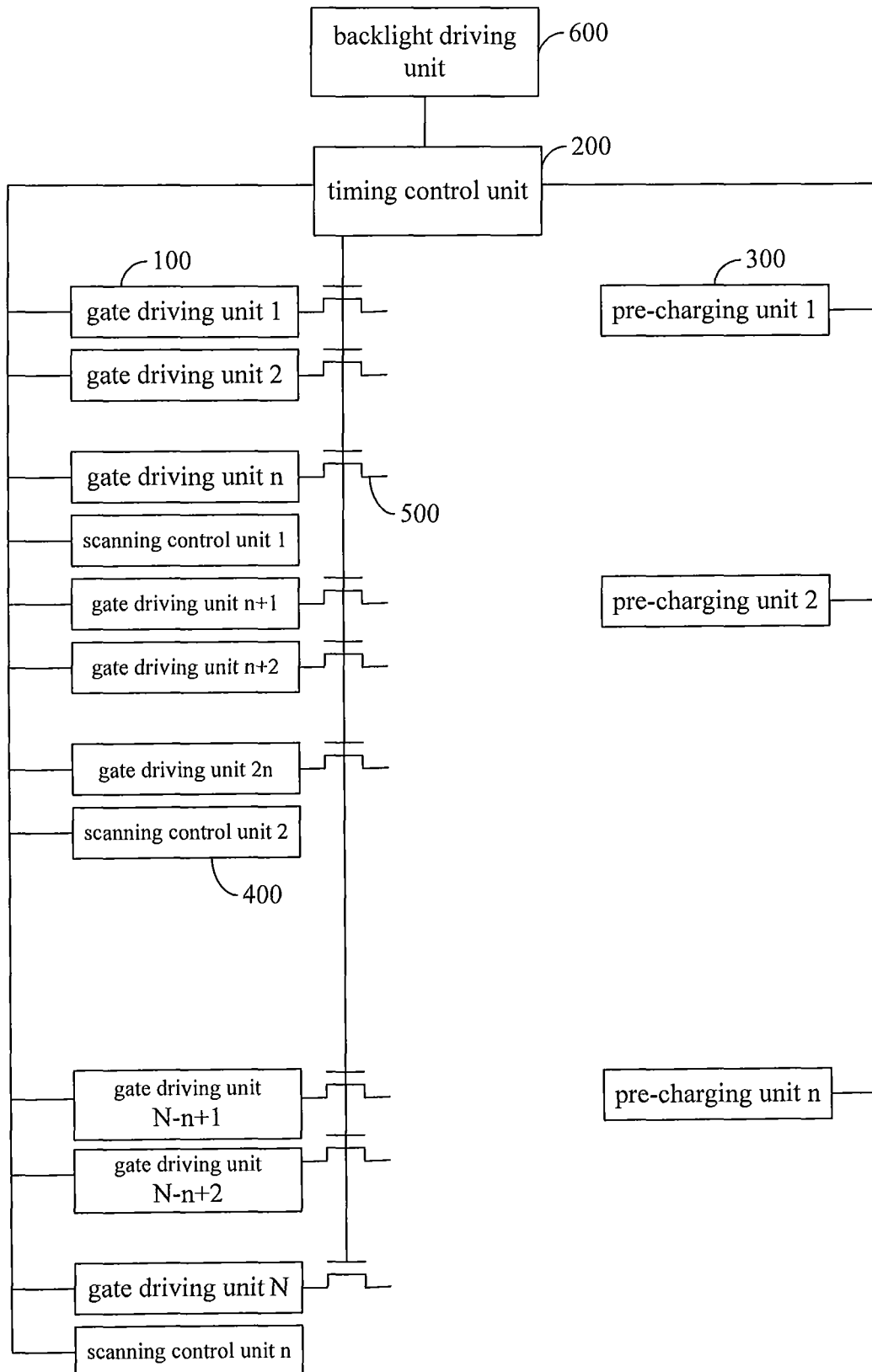


Fig.1

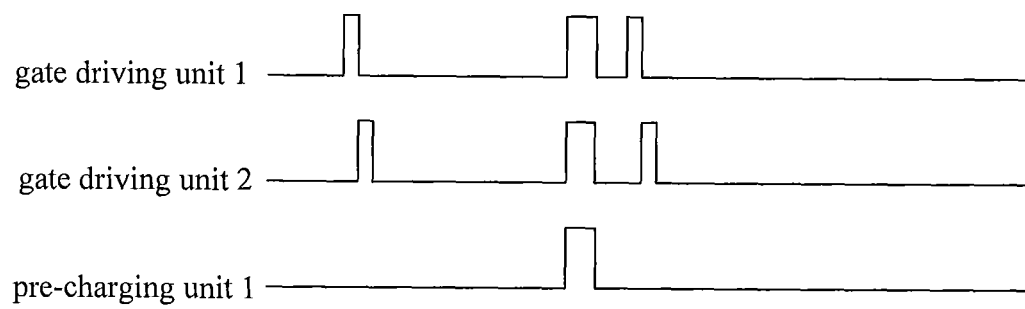


Fig.2

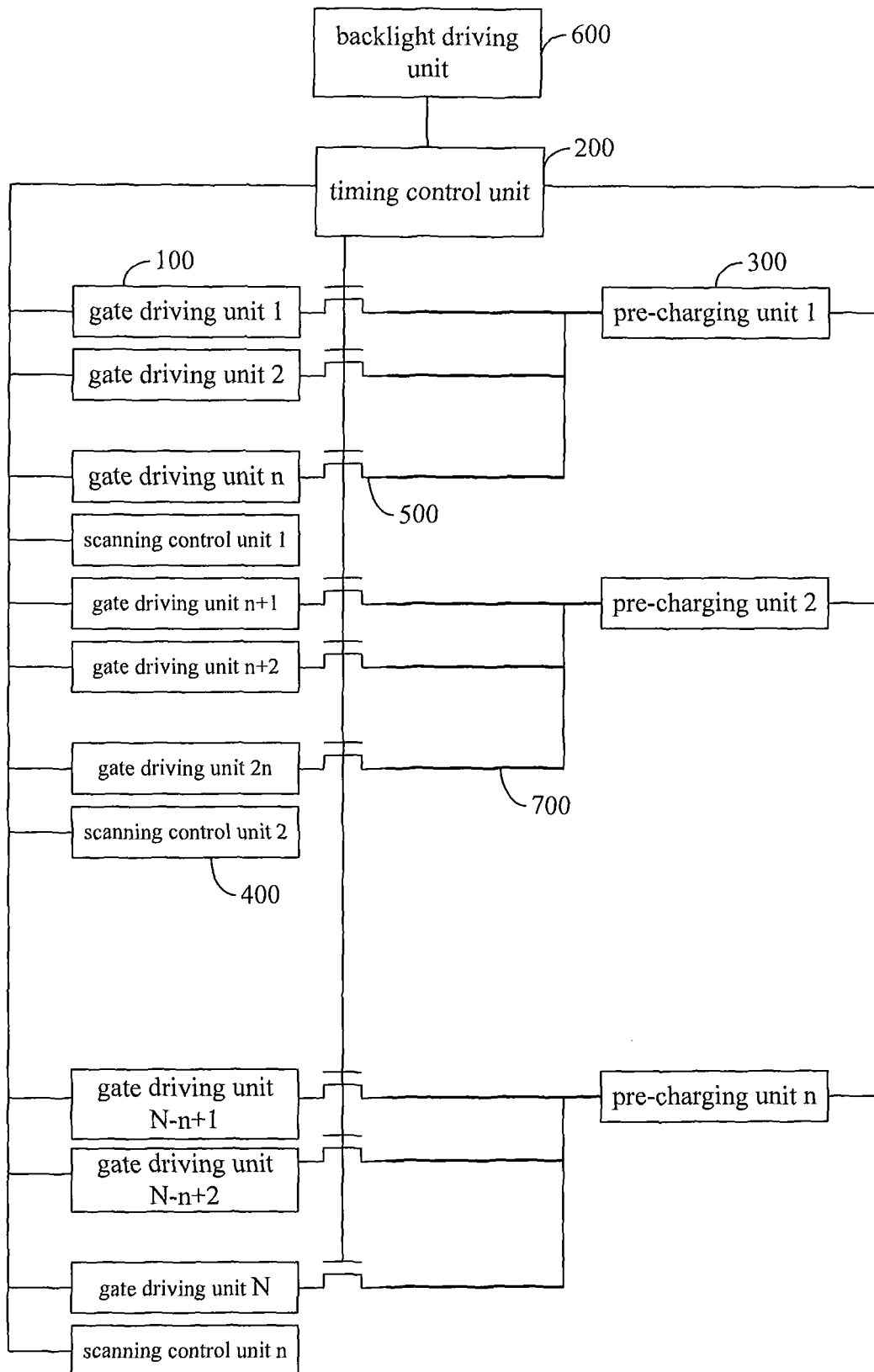


Fig.3

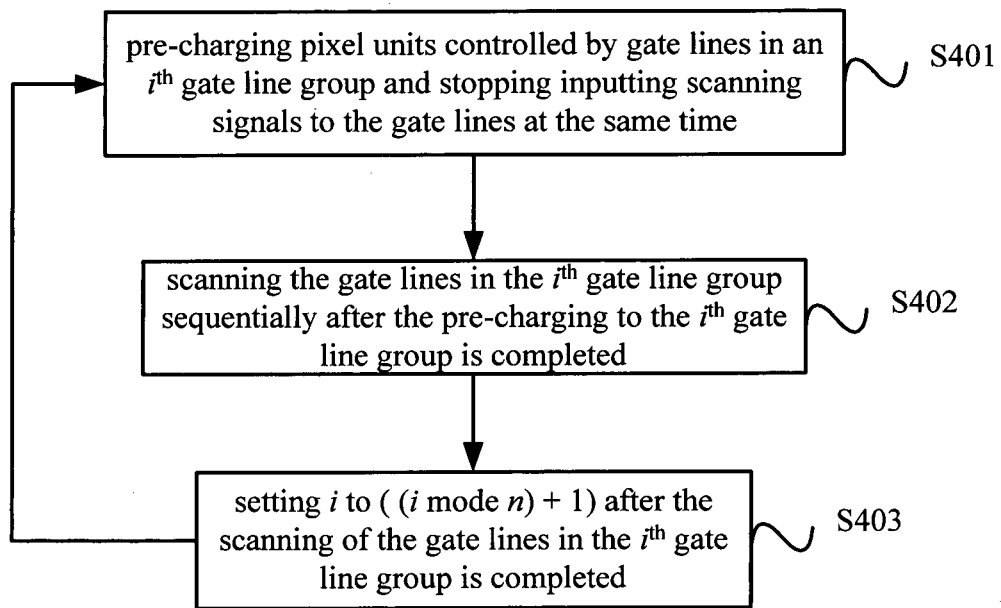


Fig. 4

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- JP 2011203742 A [0003]
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专利名称(译)	显示驱动电路，显示驱动方法，阵列基板和显示装置		
公开(公告)号	EP2743911B1	公开(公告)日	2018-01-03
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优先权	201210537327.3 2012-12-12 CN		
其他公开文献	EP2743911A1		
外部链接	Espacenet		

摘要(译)

提供一种显示驱动电路，包括分别连接到阵列基板上的N条栅极线的N个栅极驱动单元，以及定时控制单元，n个预充电单元和n个扫描控制单元，N个栅极驱动单元，n个预充电单元和n个扫描控制单元都连接到定时控制单元。还提供了一种显示驱动方法，阵列基板和显示装置。根据本公开的实施例，当在液晶分子上提供要充电的电压时，将减小液晶分子偏转到对应于期望灰度的精确位置的时间段，从而适应更高的刷新频率。

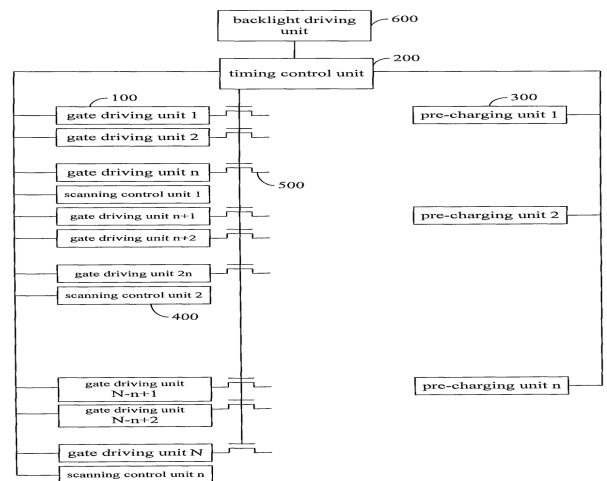


Fig. 1