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(54) **Liquid crystal display device having an integrated gate drive circuit and a reduced bezel width**

Flüssigkristallanzeigevorrichtung mit integrierter Gatetreiberschaltung und reduzierter Rahmenbreite

Dispositif d'affichage à cristaux liquides comportant un circuit de commande de grille intégré et un encadrement à largeur réduite

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Description

1. Field of the Invention

[0001] The present invention relates to a liquid crystal display device in which a bezel is minimized by overlapping circuit lines with an insulating layer interposed therebetween in an outer edge region.

2. Description of the Related Art

[0002] In general, a liquid crystal display (LCD) device displays an image by adjusting light transmittance of liquid crystal having dielectric anisotropy by using an electric field. To this end, the LCD device includes a liquid crystal panel on which pixel regions are arranged in a matrix form and a driving circuit for driving the liquid crystal panel.

[0003] The liquid crystal panel is formed by attaching a first substrate and a second substrate and forming a liquid crystal layer therebetween. A plurality of gate lines and a plurality of data les are arranged to cross vertically to define the pixel regions on the first substrate. Pixel electrodes are formed in each pixel region, and a thin film transistor (TFT) is formed in each crossing of each of the gate lines and data lines. The TFT is turned on according to a scan signal of each gate line to apply a data signal of each data line to each pixel electrode to drive the liquid crystal layer.

[0004] Also, black matrices for blocking light transmission in a portion excluding the pixel region and a color filter layers formed in the respective pixel regions to implementing actual colors are disposed on the second substrate.

[0005] The driving circuit includes a gate driver for driving the plurality of gate lines, a data driver for driving a plurality of data lines, a timing controller for supplying control signals for controlling the gate driver and the data driver, data signals, and the like.

[0006] The gate driver includes a shift register for sequentially outputting scan pulses to the respective gate lines. The shift register includes a plurality of stages which are dependently connected to each other. The plurality of stages sequentially output scan pulses to sequentially scan the gate lines of the liquid crystal panel.

[0007] In detail, a first stage, among the plurality of stages, receives a start signal as a trigger signal from the timing controller, and the other remaining stages excluding the first stage receives an output signal as a trigger signal from the previous stage. In addition, each of the plurality of stages receives at least one clock pulse among a plurality of clock pulses each having a mutually sequential phase difference. Thus, the first to the final stages sequentially output scan pulses.

[0008] In the related art, a gate driver integrated circuit (IC) including the shift register is used the gate driver and the gate driver iC is connected to a gate line pad of a liquid crystal panel by using a TCP (Taped Carrier Package) process, or the like.

[0009] However, recently, as the data driver, a data driver integrate circuit has been used, but in case of the gate driver, a gate in panel (GIP) technique for forming a shift register on a liquid crystal display panel is used to reduce material cost and the number of processes and shorten a processing time.

[0010] The related art LCD device having a GIP structure will be described.

[0011] FIG. 1 is a plan view of the related art LCD device having a GIP structure and FIG. 2 is an enlarged plan view of a region 'A' in FIG. 1.

[0012] As illustrated in FIG. 1, in the related art LCD device having a GIP structure, a first substrate 1 and a second substrate 2 are attached by a sealant 10 with a predetermined space therebetween. Here, the first substrate 1 is formed to be larger than the second substrate 2 and has a non-display region in which a data driver, or the like, is mounted, a display region is formed in the inner side of the sealant 10 in the first substrate 1 and the second substrate 2.

[0013] The display region of the attached first substrate 1 and the second substrate 2 is divided in to an active region A/A and a dummy region D. A gate line, a data line, a pixel electrode, and a TFT are formed in the active region A/A of the first substrate 1, and a black matrix layer and a color filter layer are formed in the active region A/A of the second substrate 2.

[0014] The GIP gate driver 3, a GIP dummy gate driver 4, a ground 11, control signal lines 12 for applying various signals such as a clock signal, an enable signal, a start signal, a common voltage, and the like, output from the timing controller to the GIP gate driver 3 and the GIP dummy gate driver 4, a GIP circuit 13 configured as a shift register, and a common line 15 are formed in the dummy region D of the first substrate 1. Black matrices (not shown) are formed in the dummy region D of the second substrate 2 in order to block light transmission to the region.

[0015] However, the LCD device having the foregoing structure has the following problems.

[0016] Recently, research into minimizing a size of a bezel including a dummy region has been continuously conducted in order to reduce a size of a display device and obtain a fine outer appearance thereof while maintaining the same size of screen.

[0017] However, as shown in FIG. 2, since the ground 11, the control signal lines 12, the shift GIP circuit 13, the common line 15, and the like are disposed in the dummy region D of the related art LCD device having a GIP structure, a width d1 of the dummy region D should be maintained to have a certain size or greater. Thus, there is a limitation in reducing the area of the dummy region D, resulting in a limitation in reducing a bezel, and thus, it is impossible to fabricate an LCD device having a small bezel.

[0018] EP 1176457 A2 describes a wiring and sealing scheme for a liquid crystal display device. Wiring lines

run in a sealing member to be connected to a gate signal line driving circuit and a source signal line driving circuit surrounded by the sealing member. The width of each of the wiring lines is set to a width that allows the sealing member on the wiring lines sufficient exposure to ultraviolet rays when the sealing member is irradiated with ultraviolet rays through the wiring lines.

[0019] US 2009219457 A1 describes a display substrate includes a source pad part, a plurality of storage wirings and a first voltage wiring. The source pad part includes a first voltage input pad receiving a storage common voltage. The storage wirings transmit the storage common voltage to a plurality of pixels. In particular, a first connecting wiring part includes a first voltage wiring that is connected to first end portions of storage wirings to transmit a common voltage to storage electrodes in the pixels of the display area.

[0020] US 2009296038 A1 describes a gate-in-panel type liquid crystal display device that includes first and second substrates spaced apart from and facing each other, the first and second substrates including a display area and a non-display area; gate lines, data lines, thin film transistors and pixel electrodes in the display area on the first substrate, the gate lines and the data lines crossing each other to define pixel regions, the thin film transistors connected to the gate lines and the data lines, the pixel electrodes connected to the thin film transistors.

[0021] US 2006061711 A1 describes a display substrate that comprises a base substrate divided into a display region and a peripheral region surrounding the display region, wherein an image is displayed in the display region, a pixel part formed in the display region of the base substrate, a first color filter layer formed on the base substrate including the pixel part, wherein the first color filter layer is formed in the display region, and a second color filter layer formed in the peripheral region of the base substrate.

[0022] US 2003094615 A1 describes a light-emitting device constituted by a combination of a TFT and a light-emitting element. In an outer circumferential part of a display area formed by the light-emitting element, a shield pattern surrounding the display area is formed by metal wiring on a second insulating layer, and a first substrate and a second substrate are fixed to each other with an adhesive resin formed in contact with the shield pattern.

SUMMARY OF THE INVENTION

[0023] An aspect of the present invention provides a liquid crystal display (LCD) device having a minimized bezel by disposing lines in a dummy region such that some of the lines overlap a gate in panel circuit (GIP) with an insulating layer interposed therebetween.

[0024] The object is solved by the features of appended independent claim 1.

[0025] Preferred embodiments of the present invention are defined in the appended dependent claims.

[0026] According to an embodiment of the present invention, portions of the control circuit line, the ground, and the common line are formed with the insulating layer interposed therebetween in an upper side of the GIP circuit in a GIP circuit region, whereby a region in which a line is formed is reduced relative to the related art LCD device, and thus, a width of the dummy region can be reduced and, as a result, an LCD device having a minimized bezel can be fabricated.

[0027] The foregoing and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0028]

FIG. 1 is a plan view illustrating a structure of a related art liquid crystal display (LCD) device.

FIG. 2 is an enlarged partial plan view of a portion 'A' in FIG. 1.

FIG. 3 is a plan view illustrating a structure of a liquid crystal display (LCD) device according to an embodiment of the present invention.

FIG. 4A is an enlarged partial plan view of a portion 'B' in FIG. 3.

FIG. 4B is a schematic sectional view of the portion 'B' in FIG. 3.

FIG. 5 is a cross-sectional view specifically illustrating a structure of an LCD device according to a first embodiment of the present invention.

FIG. 6 is a cross-sectional view specifically illustrating a structure of an LCD device not according to the present invention.

FIGS. 7A to 7D are views illustrating a method for fabricating an LCD device according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0029] Hereinafter, a liquid crystal display device according to an embodiment of the present invention.

[0030] FIG. 3 is a plan view illustrating a liquid crystal display (LCD) device having a gate in panel (GIP) structure according to an embodiment of the present invention.

[0031] As illustrated in FIG. 3, the LCD device having a GIP structure according to an embodiment of the present invention is formed by attaching a first substrate 101 and a second substrate 102 made of a transparent material such as glass or plastic with a sealant 110. Here, the first substrate 101 is formed to be larger than the second substrate 102 to include a non-display region on which a data driver, or the like, is mounted, and a display region is formed in the interior of the first substrate 101 and the second substrate 102 attached by the sealant

110.

[0032] Also, the display region of the attached first substrate 10 and the second substrate 102 is divided into an active region A/A and a dummy region D.

[0033] The active region A/A is a region on which an image is actually implemented. Although not shown, the active region A/A includes a plurality of pixel regions defined by a plurality of gate lines and data lines disposed on the first substrate 101, TFTs as switching elements formed in the respective pixel regions and driven upon receiving a signal applied thereto to apply an image signal to an image region, a pixel electrode and a common electrode formed in the pixel region and driving liquid crystal molecules of a liquid crystal layer upon receiving the image signal according to an operation of the TFTs to control transmittance of light transmitted through the liquid crystal layer to thus implement an image, a black matrix formed on the second substrate 102 to block light transmission to a region other than a region in which an image is implemented, and a color filter layer including R, G, and B color filters to implement actual colors.

[0034] A GIP gate driver 103, a GIP dummy gate driver 104, a ground 111, control signal lines 112 for applying various signals such as a clock signal, an enable signal, a start signal, a common voltage, and the like, output from the timing controller to the GIP gate driver 103 and the GIP dummy gate driver 104, a GIP circuit 113 configured as a shift register, and a common line 114 are formed in the dummy region D of the first substrate 101. Black matrices (not shown) are formed in the dummy region D of the second substrate 102 in order to block light transmission to the region.

[0035] The control signal lines 112 include a clock signal line, an enable signal line, a start signal line, and the like.

[0036] FIGS. 4A and 4B are partially enlarged views of a region 'B' in FIG. 3, in which FIG. 4A is a plan view illustrating a disposition of lines in the dummy region D, and FIG. 4B is a cross-sectional view schematically illustrating a layer structure.

[0037] As illustrated in FIG. 4A, a common line 115, a GIP circuit 113, a control signal line 112, and a ground 111 are sequentially disposed from a boundary of the active region A/A to an end portion of the first substrate 101 in the dummy region D. Here, it is illustrated that a particular number of common lines 114 and control signal lines 112 are formed, but this is for the description purpose and the lines of the present invention are not limited to a particular number. Substantially, a number of lines may be determined by a size of a fabricated liquid crystal panel, a number of pixels, a number of GIP gate drivers 103 mounted on the liquid crystal panel, and the like.

[0038] As illustrated in FIGS. 4A and 4B, the GIP circuit 113 is disposed on the first substrate 101, and the ground 111 and the common line 114 are disposed in both sides of the GIP circuit 113. The control signal line 112 is disposed on the GIP circuit 113. Here, the control signal line 112 is formed to completely overlap the GIP circuit 113, and the ground 111 and the common line 114 are formed such that portions thereof are formed on the first substrate 101 and other portions are formed on the GIP circuit 113 to overlap with the GIP circuit 113.

[0039] In this manner, the control signal line 112 is formed on the GIP circuit 113, and portions of the ground 111 and the common line 114 are formed on the GIP circuit 113, a width of the dummy region can be reduced relative to the related art LCD device.

[0040] As for the structure of related art LCD device illustrated in FIG. 2 and that of the LCD device according to an embodiment of the present invention illustrated in FIG. 4A, in the related art, the ground 111, the GIP circuit 113, the control signal 112, and the common line 114 are disposed on the first substrate 101 having widths of a1, a2, a3, and a4. In comparison, in an embodiment of the present invention, the ground 111, the GIP circuit 113, and the common line 114 are disposed on the first substrate 101 having the widths of a1', a2', and a4'.

[0041] Since the control signal line 112 is formed on the GIP circuit 113, it does not occupy any region of the first substrate 101. Also, since a portion of the ground 111 overlaps with the GIP circuit 113, a1' is smaller than a1 (a1'<a1), and since a portion of the common line 114 overlaps with the GIP circuit, a4' is smaller than a4 (a4'<a4). Here, 50 to 100% of the ground 111 of the entire area overlaps with the GIP circuit 113, and 50 5o 100% of the common line 114 of the entire area overlaps with the GIP circuit 113. As a result, in an embodiment of the present invention, the width of the dummy region may be reduced by a3+(a1-a1')+(a4-a4') (i.e., d1 >d2) in comparison to the related art.

[0042] An embodiment of the present invention will be described in detail with reference to the accompanying drawings.

[0043] FIG. 5 shows a structure of an LCD device according to a first embodiment of the present invention, in which only the dummy region is illustrated.

[0044] As shown in FIG. 5, the dummy region D of the first substrate 101 includes a ground region, a GIP circuit region, and a common line region. A first ground 111a, a gate electrode 113a of a TFT for a shift register forming a GIP circuit, and a first common line 114a are formed in the ground region, the GIP circuit region, and the common line region of the first substrate 101.

[0045] The first ground 111 a, the gate electrode 113a of the TFT for a shift register, and the first common line 114a may be formed with different metals through different processes, but preferably, they are formed with the same metal through the same process. Here, first ground 111 a, the gate electrode 113a of the TFT for a shift register, and the first common line 114a may be formed as a single layer made of a metal having excellent conductivity such as aluminum (Al) or an Al alloy, respectively. Also, the first ground 111 a, the gate electrode 113a of the TFT for a shift register, and the first common line 114a may be formed as a plurality of layers such as AlNd/Mo.

[0046] A gate insulating layer 142 made of an inorganic insulating material such as SiOx or SiNx is formed on the first substrate 101 with the first ground 111 a, the gate electrode 113a of the TFT for a shift register, and the first common line 114a formed thereon.

[0047] A semiconductor layer 113b is formed on the gate insulating layer 142 in the GIP circuit region. The semiconductor layer 113b may be largely made of amorphous silicon (a-Si), but a crystalline silicon or an oxide semiconductor may also be used.

[0048] A source electrode 113c and a drain electrode 113d are formed on the semiconductor layer 113b, completing a TFT for a shift register. Here, the source electrode 113c and the drain electrode 113d may be made of a metal having excellent conductivity such as aluminum (Al), an Al alloy, molybdenum (Mo), or the like. Although not shown, various lines, as well as the TFT for a shift register, may be formed in the GIP circuit region.

[0049] A passivation layerpassivation layer 144 is formed on the first substrate 101 with the TFT for a shift register formed thereon. The passivation layerpassivation layer 144 may be made of an organic material such as photoacryl or may be made of an inorganic material such as SiOx or SiNx. Also, the passivation layerpassivation layer 144 may be formed as a dual layer including an inorganic passivation layerpassivation layer and an organic passivation layerpassivation layer.

[0050] A first contact hole 119a, a second contact hole 119b, and a third contact hole 119c are formed in the GIP circuit region and the common line region. Here, the second contact hole 119b is formed only in the passivation layerpassivation layer 144 to allow the TFT for a shift register to be exposed therthrough. The first contact hole 119a and the third contact hole 119c are formed in the gate insulating layer 142 and the passivation layerpassivation layer 144 to allow the first ground 111 a and the first common line 114a to be exposed therethrough, respectively.

[0051] A second ground 111b is formed in the ground region above the passivation layerpassivation layer 144, a control circuit line 112 is formed in the GIP circuit region, and a second common line 114b is formed in the common line region. The second ground 111b is electrically connected to the first ground 111 a through the first contact hole 119a, the control circuit line 112 is electrically connected to the drain electrode 113d of the TFT for a shift register, i.e., a GIP circuit, through the second contact hole 119d, and the second common line 114b is electrically connected to the first common line 119a through the third contact hole 119c.

[0052] Here, although not illustrated in FIG.5, a portion of the second ground 111b and a portion of the second common line 114b extend into the GIP circuit region. Thus, since the portion of the second ground 111b and the portion of the second common line 114b, as well as the control circuit line 112, are formed in the GIP circuit region, the GIP circuit (i.e., the shift register), overlaps with the control circuit line 112 and portions of the second ground 111b and the second common line 114b with the insulating layer (gate insulating layer) 142 and/or the passivation layerpassivation layer 144 interposed therebetween.

[0053] In this manner, in the first embodiment of the present invention, since the control circuit line 112 and the portions of the second ground 111 b and the second common line 114 are formed in an upper side of the GIP circuit with the insulating layer interposed therebetween in the GIP circuit region, the width of the dummy region can be reduced relative to the related art LCD device.

[0054] Here, it is illustrated in the drawing that portions of the second ground 111b and the second common line 114b overlap with the GIP circuit, but only the control circuit line 112 may be formed to overlap with the GIP circuit and the second ground 111b and the second common line 114b do not overlap with the GIP circuit or a portion of only one of the second ground 111b and the second common line 114b may overlap with the GIP circuit.

[0055] In other words, an embodiment of the present invention includes any structure in which the control circuit line 112 and the entirety or portions of the second ground 111b and the second common line 114 are overlap with the GIP circuit with the insulating layer interposed therebetween.

[0056] FIG. 6 is a view illustrating a structure of an LCD device not according to the present invention.

[0057] As illustrated in FIG. 6, the dummy region D includes a ground region, a GIP circuit region, and a common line region. The first ground 111a and the first common line 114a are formed in the ground region and the common line region of the first substrate 101. Also, a GIP circuit including a TFT for a shift register comprised of the gate electrode 113a, the semiconductor layer 113b, the source electrode 113c, and the drain electrode 114 is formed in the GIP circuit region.

[0058] Here, the gate insulating layer 142 is formed on first ground 111 a, the firs common line 114a, and the gate electrode 113a of the TFT for a shift register.

[0059] The passivation layerpassivation layer 144 formed of an inorganic layer, an organic layer, or an organic layer/inorganic layer is formed on the first substrate 101 with the TFT for a shift register formed thereon.

[0060] A color filter layer 146 is formed on the passivation layerpassivation layer 144. Namely, the LCD device having the foregoing structure is an LCD device having a color filter on TFT (COT) structure in which the color filter layer 146 is formed on the first substrate 101. In this structure, the color filter layer 146 is formed on the first substrate, in comparison to the structure of the LCD device illustrated in FIG. 4 in which the color filter layer is formed on the second substrate (i.e., the upper substrate).

[0061] In the LCD device having the COT structure, the R, G, and B color filters are formed directly on the corresponding pixel, there is no need to consider a defect due to misalignment of the first substrate and the second

substrate generated when the color filter layer is formed on the second substrate or an attachment margin.

[0062] Although not shown, the color filter layer 146 may be a single layer of one color among an R-color filter layer, a G-color filter layer, and a B-color filter layer, or may be formed as a triple-layer by stacking the R-color filter layer, the G-color filter layer, and the B-color filter layer, or may be formed as a dual-layer including two different colors.

[0063] The first contact hole 119a, the second contact hole 119b, and the third contact hole 119c are respectively formed in the ground region, the GIP circuit region and the common line region. Here, the second contact hole 119b is formed only in the passivation layerpassivation layer 144 and the color filter layer 146 to allow the TFT for a shift register to be exposed therthrough. The first contact hole 119a and the third contact hole 119c are formed in the gate insulating layer 142, the passivation layerpassivation layer 144, and the color filter layer to allow the first ground 111 a and the first common line 114a to be exposed therethrough, respectively.

[0064] A second ground 111 b is formed in the ground region above the color filter layer 146, a control circuit line 112 is formed in the GIP circuit region, and a second common line 114b is formed in the common line region. The second ground 111b is electrically connected to the first ground 111a through the first contact hole 119a, the control circuit line 112 is electrically connected to the drain electrode 113d of the TFT for a shift register, i.e., a GIP circuit, through the second contact hole 119d, and the second common line 114b is electrically connected to the first common line 119a through the third contact hole 119c.

[0065] Although not shown, a buffer layer made of an inorganic insulating material or an organic insulating material may be formed on the color filter layer 146. The buffer layer serves to improve interface characteristics with the color filter layer 146 when the second ground 111 b and the second common line 114b are formed. Of course, in this structure, the first contact hole 119a, the second contact hole 119b, and the third contact hole 119c are formed on the buffer layer.

[0066] Although not shown, a black matrix may be formed in the dummy region of the second substrate to block a light transmission thereto, thus preventing light from being transmitted to degrade picture quality.

[0067] Hereinafter, a method for fabricating the LCD device having the foregoing structure will be described. Here, a method for fabricating the LCD device having the structure illustrated in FIG. 5 is described, but the LCD device having the structure illustrated in FIG. 6 may also be fabricated by the same method.

[0068] Also, hereinafter, a method for fabricating the LCD device having a particular pixel structure is described, but the present invention is not limited only to the particular pixel structure. The present invention may be applicable to LCD devices of various modes such as an in plane switching (IPS) mode LCD device, a twisted nematic (TN) mode LCD device, a vertical alignment (VA) mode LCD device, and the like. Also, in the following description, various electrodes and insulating layers have a particular structure, but the present invention is not limited thereto. The present invention may be applied to LCD devices having any structure as long as a line of a dummy region is formed in an overlapping manner.

[0069] FIGS. 7A to 7D are views illustrating a method for fabricating an LCD device according to an embodiment of the present invention.

[0070] First, as illustrated in FIG. 7A, AINd and Mo are successively stacked on the first substrate 101 made of transparent glass of plastic and including the dummy region D and the active region A/A through a sputtering method and subsequently etched through photolithography to form the first ground 111a, the gate electrode 113a for a shift register of a GIP circuit, and the second common line 112 in the dummy region D and the gate electrode 151 of a TFT for switching of a pixel in the active region A/A. Next, an inorganic insulating material such as SiOx or SiNx is stacked on the entirety of the first substrate through chemical vapor deposition (CVD) to form the gate insulating layer 142.

[0071] Subsequently, as illustrated in FIG. 7B, an amorphous semiconductor material such as an amorphous silicon is stacked on the first substrate 101 and etched to form the semiconductor layer 113b for a shift register on the gate insulating layer 142 above the gate electrode 113a for a shift register and the semiconductor layer 152 of the TFT for switching on the gate insulating layer 142 above the gate electrode 151 of the TFT for switching.

[0072] Thereafter, a metal such as molybdenum (Mo), or the like, is stacked through a sputtering method and etched through photolithography to form the source electrode 113c and the drain electrode 113d for a shift register and the source electrode 153 and the drain electrode 154 of a TFT for switching on the semiconductor layers 113b and 152, respectively, to form a GIP circuit line including a shift register in the dummy region and a TFT for switching in each pixel region of the active region A/A.

[0073] Subsequently, an organic material such as photoacryl or an inorganic material such as SiOx or SiNx is stacked on the first substrate 101 with the TFT formed thereon to form the passivation layerpassivation layer 114. Here, the passivation layerpassivation layer 144 formed as a dual-layer may be formed by successively stacking an inorganic material and an organic material.

[0074] Thereafter, as illustrated in FIG. 7C, a portion of the passivation layerpassivation layer is etched to form the first contact hole 119a, the second contact hole 119b, and the third contact hole 119c in the dummy region D to allow the first ground 111a, the drain electrode 113d for a shift register, and the first common line 114 to be exposed therethrough and to form the fourth contact hole 119d in the active region A/A to allow the drain electrode 154 of the TFT for switching to be exposed.

[0075] Subsequently, as illustrated in FIG. 7D, a trans-

parent conductive material such as indium tin oxide (ITO) is stacked on the passivation layerpassivation layer 144 and etched to form at least a pair of common electrode 156 and pixel electrode 158 in the active region A/A. Here, the common electrode 156 and the pixel electrode 158 have a band-like shape having a predetermined width and are arranged to be parallel to each other. The pixel electrode 158 is electrically connected to the drain electrode 154 of the TFT for switching through the fourth contact hole 119d and an image signal is applied from the outside through the TFT for switching.

[0076] Subsequently, molybdenum (Mo), aluminum (Al), and molybdenum (Mo) are successively stacked on the passivation layerpassivation layer 144 and etched to form the second ground 111 b, the control signal line 112, and the second common line 114b in the dummy region D. The second ground 111 b is electrically connected to the first ground 111 b through the first contact hole 119a, the control signal line 112 is connected to the GIP circuit (i.e., the drain electrode 113d for a shift register) through the second contact hole 119b, and the second common line 114b is electrically connected to the first common line 114a through the third contact hole 119c.

[0077] Here, the second ground 111 b, the control signal line 112, and the second common line 114b may be formed with the same metal layer (e.g., Mo/Al/Mo) through the same process, or may be formed with different metals through different processes.

[0078] Although not clearly shown, a portion of the second ground 111 b formed on the passivation layerpassivation layer 144 overlaps with the GIP circuit. Also, a portion of the second common line 114b overlaps with the GIP circuit.

[0079] Thereafter, although not shown, after the color filter layer and the black matrix are formed on the second substrate, the first substrate and the second substrate may be attached by a sealant and a liquid crystal layer is formed between the first substrate and the second substrate, thus completing an LCD device.

[0080] As described above, in an embodiment of the present invention, by overlapping some lines formed in the dummy region with a GIP circuit with an insulating layer interposed therebetween, the area of the dummy region can be minimized, and as a result, a bezel area of the LCD device can be minimized to thus reduce a size of the LCD device and obtain a fine outer appearance.

[0081] Meanwhile, the LCD device having a particular structure has been described, but it is only for the description purpose and the present invention is not limited thereto.

[0082] The present invention may be applied to LCD devices having any structures as long as at least portions of various lines overlap a GIP circuit with an insulating layer interposed therebetwen in a dummy region to reduce an area of the dummy region.

[0083] The present invention may be embodied in several forms without departing from the scope of the invention as defined in the appended claims, and therefore all changes and modifications that fall within the metes and bounds of the claims are therefore intended to be embraced by the present invention.

Claims

1. A liquid crystal display device comprising:

a first substrate (101) including an active display region (A/A) and a dummy region (D) formed at an outer side of the active display region (A/A);
a plurality of gate lines and data lines formed in the active display region to define a plurality of pixel regions arranged to display an image;
a thin film transistor (151, 153, 154) provided in each pixel region for switching the pixel associated with each pixel region;
a common electrode (156) and a pixel electrode (158) provided in each pixel region;
a passivation layer (144) on the first substrate (101); and
a gate in panel, GIP, circuit (113) in the dummy region (D) configured as a shift register connected to the gate lines, a control signal line (112) in the dummy region (D) connected to the GIP circuit (113) for supplying a control signal to the GIP circuit (113), a ground (111) and a common line (114) in the dummy region (D),
wherein the GIP circuit (113) is overlapped with the control signal line (112), at least a portion of the ground (111), and at least a portion of the common line (114) with the passivation layer (144) interposed therebetween.

2. The device of claim 1, wherein the control signal line (112) includes a clock signal line, an enable signal line, and a start signal line.

3. The device of claim 1, wherein the passivation layer (144) is made of photoacryl.

4. The device of claim 1, wherein the passivation layer (144) is made of an inorganic insulating material.

5. The device of claim 1, wherein the passivation layer (144) comprises:

an inorganic passivation layer; and
an organic passivation layer formed on the inorganic passivation layer.

6. The device of claim 1, wherein the TFT in each pixel region for switching the corresponding pixel comprises:

a gate electrode (151) formed on the first sub-

strate (101);
a gate insulating layer (142) formed on the first substrate (101) and covering the gate electrode (151);
a semiconductor layer (152) formed on the gate insulating layer (142); and
a source electrode (153) and a drain electrode (154) formed on the semiconductor layer (152).

7. The device of claim 6, wherein the ground (111) comprises:

a first ground (111a) formed on the first substrate (101); and
a second ground (111b) formed on the passivation layer (144) and electrically connected to the first ground (111a) through a first contact hole (119a) formed in the passivation layer (144).

8. The device of claim 6, wherein the common line (114) comprises:

a first common line (114a) formed on the first substrate (101); and
a second common line (114b) formed on the passivation layer (144) and electrically connected to the first common line (114a) through a second contact hole (119c) formed in the passivation layer (144).

9. The device of claim 6, wherein the control signal line (112) is formed on the passivation layer (144) and electrically connected to the GIP circuit (113) through a third contact hole (119b) formed in the passivation layer (144).

10. The device of claim 1, further comprising:

a color filter layer formed on the passivation layer (144).

11. The device of claim 10, wherein the control signal line (112), the second ground (111b), and the second common line (114b) are formed on the color filter layer.

12. The device of claim 1, further comprising:

a second substrate (102) attached to the first substrate (101);
a black matrix formed on the second substrate (102); and
a liquid crystal layer formed between the first substrate (101) and the second substrate (102).

Patentansprüche

1. Flüssigkristallanzeigevorrichtung, die Folgendes umfasst:

ein erstes Substrat (101), das ein aktives Anzeigegebiet (A/A) und ein Dummy-Gebiet (D), das auf einer äußeren Seite des aktiven Anzeigegebiets (A/A) gebildet ist, enthält;
mehrere Gate-Leitungen und Datenleitungen, die in dem aktiven Anzeigegebiet gebildet sind, um mehrere Pixelgebiete zu definieren, die angeordnet sind, um ein Bild anzuzeigen;
ein Dünnschichttransistor (151, 153, 154), der in jedem Pixelgebiet vorgesehen ist, um das Pixel zu schalten, das jedem Pixelgebiet zugeordnet ist;
eine gemeinsame Elektrode (156) und eine Pixelelektrode (158), die in jedem Pixelgebiet vorgesehen sind;
eine Passivierungsschicht (144) auf dem ersten Substrat (101) und
eine Gate-in-Panel-Schaltung, GIP-Schaltung, (113) in dem Dummy-Gebiet (D), die als ein Schieberegister konfiguriert ist, das mit den Gate-Leitungen verbunden ist, eine Steuersignalleitung (112) in dem Dummy-Gebiet (D), die mit der GIP-Schaltung (113) zum Zuführen eines Steuersignals an die GIP-Schaltung (113) verbunden ist, eine Masse (111) und eine gemeinsame Leitung (114) in dem Dummy-Gebiet (D),
wobei die GIP-Schaltung (113) durch die Steuersignalleitung (112), mindestens einen Abschnitt der Masse (111) und mindestens einen Abschnitt der gemeinsamen Leitung (114) mit der Passivierungsschicht (144) dazwischen eingeschoben überlappt wird.

2. Vorrichtung nach Anspruch 1, wobei die Steuersignalleitung (112) eine Taktsignalleitung, eine Freigabesignalleitung und eine Startsignalleitung enthält.

3. Vorrichtung nach Anspruch 1, wobei die Passivierungsschicht (144) aus Photoacryl hergestellt ist.

4. Vorrichtung nach Anspruch 1, wobei die Passivierungsschicht (144) aus einem anorganischen Isoliermaterial hergestellt ist.

5. Vorrichtung nach Anspruch 1, wobei die Passivierungsschicht (144) Folgendes umfasst:

eine anorganische Passivierungsschicht und
eine organische Passivierungsschicht, die auf der anorganischen Passivierungsschicht gebildet ist.

6. Vorrichtung nach Anspruch 1, wobei der TFT in jedem Pixelgebiet zum Schalten des entsprechenden Pixels Folgendes umfasst:

eine Gate-Elektrode (151), die auf dem ersten Substrat (101) gebildet ist;
eine Gate-Isolierelektrode (142), die auf dem ersten Substrat (101) gebildet ist und die Gate-Elektrode (151) abdeckt;
eine Halbleiterschicht (152), die auf der Gate-Isolierschicht (142) gebildet ist, und
eine Source-Elektrode (153) und eine Drain-Elektrode (154), die auf der Halbleiterschicht (152) gebildet sind.

7. Vorrichtung nach Anspruch 6, wobei die Masse (111) Folgendes umfasst:

eine erste Masse (111a), die auf dem ersten Substrat (101) gebildet ist, und
eine zweite Masse (111b), die auf der Passivierungsschicht (144) gebildet ist und mit der ersten Masse (111a) durch ein erstes Kontaktloch (119a), das in der Passivierungsschicht (144) gebildet ist, elektrisch verbunden ist.

8. Vorrichtung nach Anspruch 6, wobei die gemeinsame Leitung (114) Folgendes umfasst:

eine erste gemeinsame Leitung (114a), die auf dem ersten Substrat (101) gebildet ist, und
eine zweite gemeinsame Leitung (114b), die auf der Passivierungsschicht (144) gebildet ist und mit der ersten gemeinsamen Leitung (114a) durch ein zweites Kontaktloch (119c), das in der Passivierungsschicht (144) gebildet ist, elektrisch verbunden ist.

9. Vorrichtung nach Anspruch 6, wobei die Steuersignalleitung (112) auf der Passivierungsschicht (144) gebildet ist und mit der GIP-Schaltung (113) durch ein drittes Kontaktloch (119b), das in der Passivierungsschicht (144) gebildet ist, elektrisch verbunden ist.

10. Vorrichtung nach Anspruch 1, die ferner Folgendes umfasst:

eine Farbfilterschicht, die auf der Passivierungsschicht (144) gebildet ist.

11. Vorrichtung nach Anspruch 10, wobei die Steuersignalleitung (112), die zweite Masse (111b) und die zweite gemeinsame Leitung (114b) auf der Farbfilterschicht gebildet sind.

12. Vorrichtung nach Anspruch 1, die ferner Folgendes umfasst:

ein zweites Substrat (102), das an dem ersten Substrat (101) angebracht ist;
eine schwarze Matrix, die auf dem zweiten Substrat (102) gebildet ist, und
eine Flüssigkristallschicht, die zwischen dem ersten Substrat (101) und dem zweiten Substrat (102) gebildet ist.

Revendications

1. Dispositif d'affichage à cristaux liquides comprenant :

un premier substrat (101) comprenant une région d'affichage active (A/A) et une région factice (D) formée à un côté extérieur de la région d'affichage active (A/A) ;
une pluralité de lignes de grille et de lignes de données formées dans la région d'affichage active pour définir une pluralité de régions de pixels agencées pour afficher une image ;
un transistor à film mince (151, 153, 154) fourni dans chaque région de pixel pour commuter le pixel associé à chaque région de pixel ;
une électrode commune (156) et une électrode de pixel (158) fournies dans chaque région de pixel ;
une couche de passivation (144) sur le premier substrat (101) ; et
un circuit de grille dans panneau, GIP, (113) dans la région factice (D) configuré en tant que registre à décalage relié aux lignes de grille,
une ligne de signal de commande (112) dans la région factice (D) reliée au circuit GIP (113) pour fournir un signal de commande au circuit GIP (113), une masse (111) et une ligne commune (114) dans la région factice (D),
dans lequel le circuit GIP (113) est chevauché par la ligne de signal de commande (112), au moins une portion de la masse (111) et au moins une portion de la ligne commune (114) avec la couche de passivation (144) interposée entre elles.

2. Dispositif selon la revendication 1, dans lequel la ligne de signal de commande (112) comprend une ligne de signal d'horloge, une ligne de signal d'activation et une ligne de signal de début.

3. Dispositif selon la revendication 1, dans lequel la couche de passivation (144) est constituée de photoacryl.

4. Dispositif selon la revendication 1, dans lequel la couche de passivation (144) est constituée d'un matériau isolant inorganique.

5. Dispositif selon la revendication 1, dans lequel la couche de passivation (144) comprend :

une couche de passivation inorganique ; et
une couche de passivation organique formée sur la couche de passivation inorganique.

6. Dispositif selon la revendication 1, dans lequel le TFT dans chaque région de pixel pour commuter le pixel correspondant comprend :

une électrode de grille (151) formée sur le premier substrat (101) ;
une couche d'isolation de grille (142) formée sur le premier substrat (101) et recouvrant l'électrode de grille (151) ;
une couche de semi-conducteur (152) formée sur la couche d'isolation de grille (142) ; et
une électrode de source (153) et une électrode de drain (154) formées sur la couche de semiconducteur (152).

7. Dispositif selon la revendication 6, dans lequel la masse (111) comprend :

une première masse (111a) formée sur le premier substrat (101) ; et
une deuxième masse (111b) formée sur la couche de passivation (144) et électriquement reliée à la première masse (111a) à travers un premier trou de contact (119a) formé dans la couche de passivation (144).

8. Dispositif selon la revendication 6, dans lequel la ligne commune (114) comprend :

une première ligne commune (114a) formée sur le premier substrat (101) ; et
une deuxième ligne commune (114b) formée sur la couche de passivation (144) et électriquement reliée à la première ligne commune (114a) à travers un deuxième trou de contact (119c) formé dans la couche de passivation (144).

9. Dispositif selon la revendication 6, dans lequel la ligne de signal de commande (112) est formée sur la couche de passivation (144) et est électriquement reliée au circuit GIP (113) à travers un troisième trou de contact (119b) formé dans la couche de passivation (144).

10. Dispositif selon la revendication 1, comprenant en outre :

une couche de filtre de couleur formée sur la couche de passivation (144).

11. Dispositif selon la revendication 10, dans lequel la ligne de signal de commande (112), la deuxième masse (111b) et la deuxième ligne commune (114b) sont formées sur la couche de filtre de couleur.

12. Dispositif selon la revendication 1, comprenant en outre :

un deuxième substrat (102) attaché au premier substrat (101) ;
une matrice noire formée sur le deuxième substrat (102) ; et
une couche de cristaux liquides formée entre le premier substrat (101) et le deuxième substrat (102).

FIG. 1

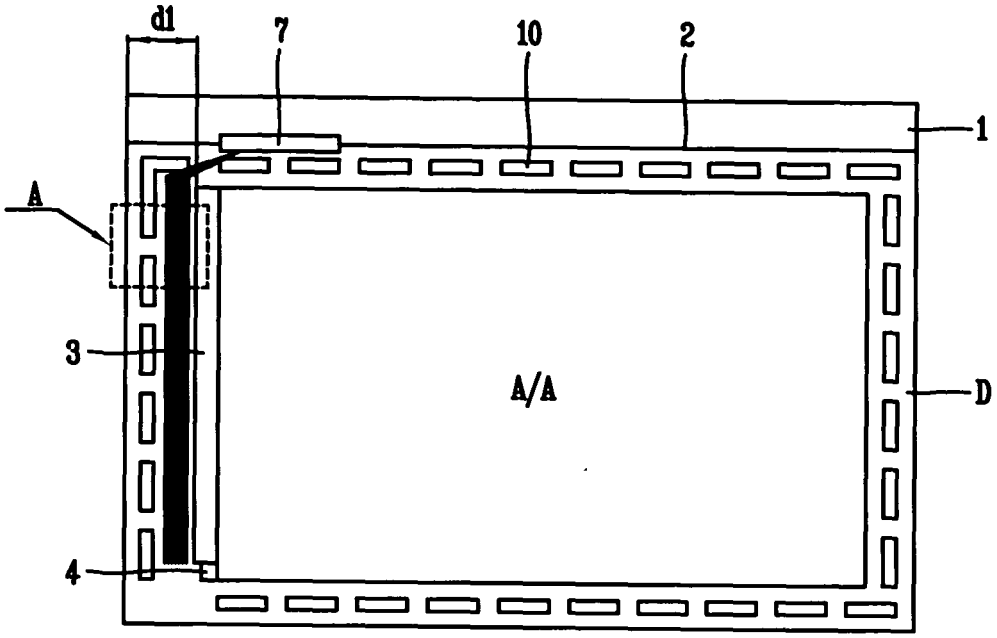


FIG. 2

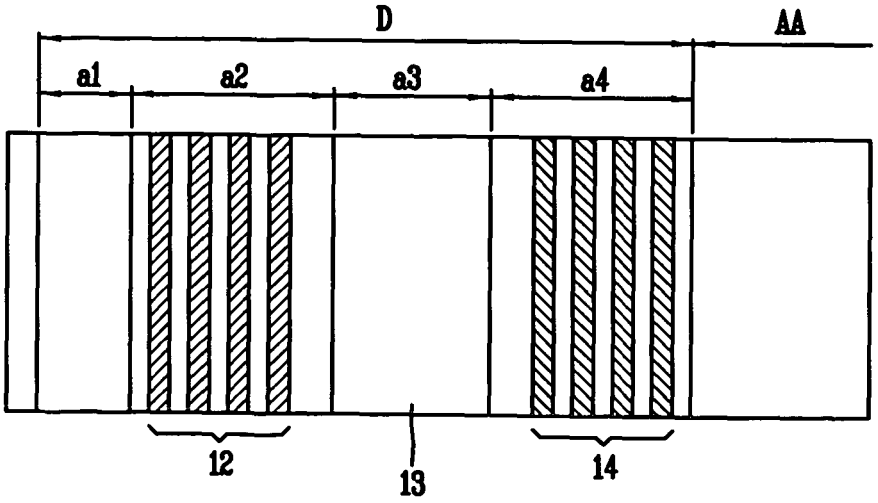


FIG. 3

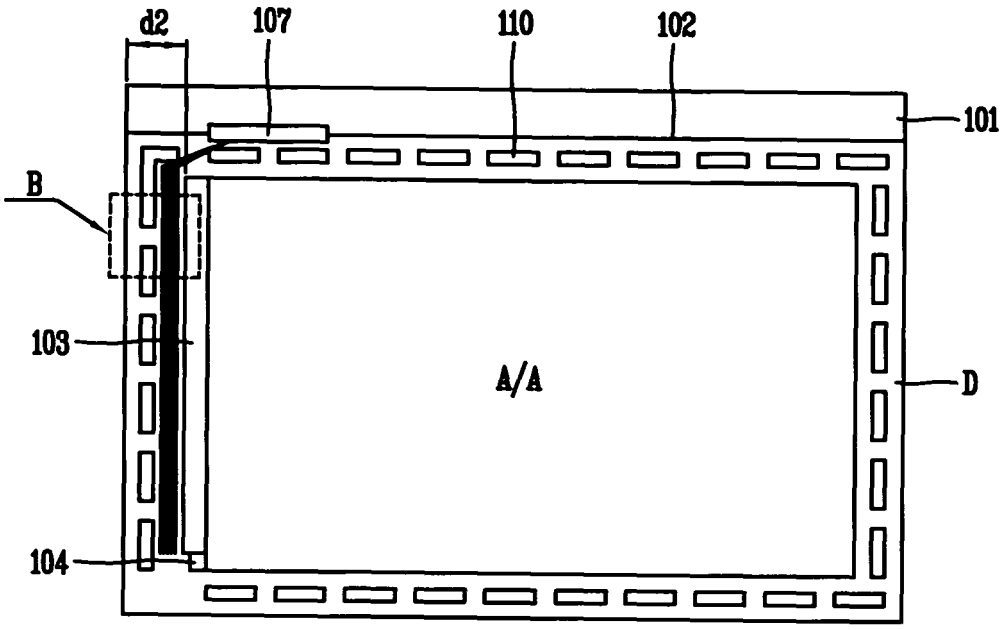


FIG. 4A

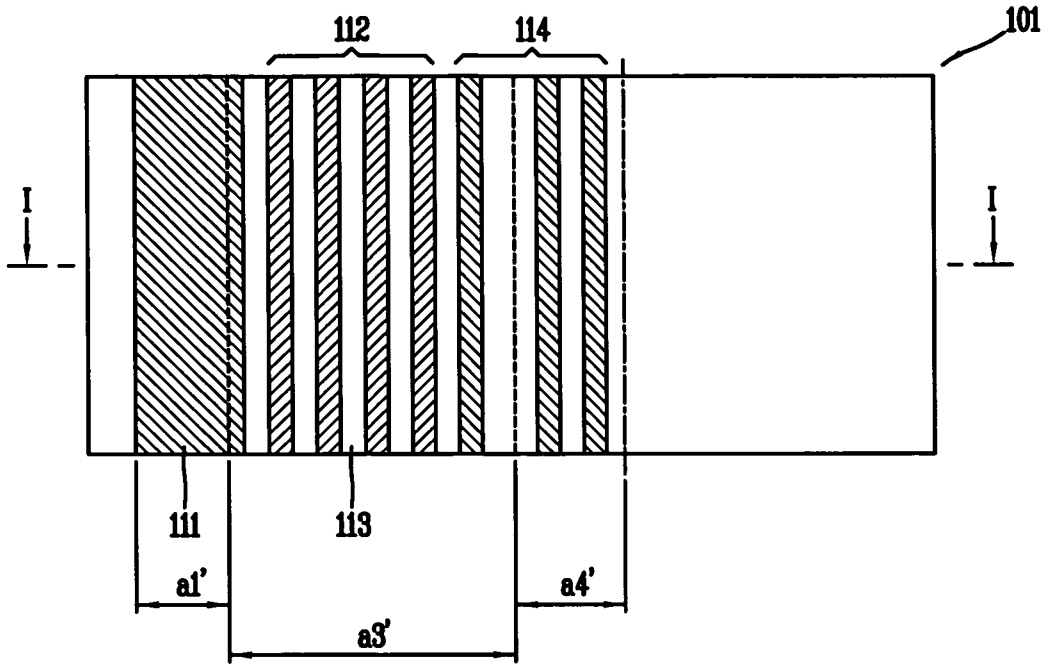


FIG. 4B

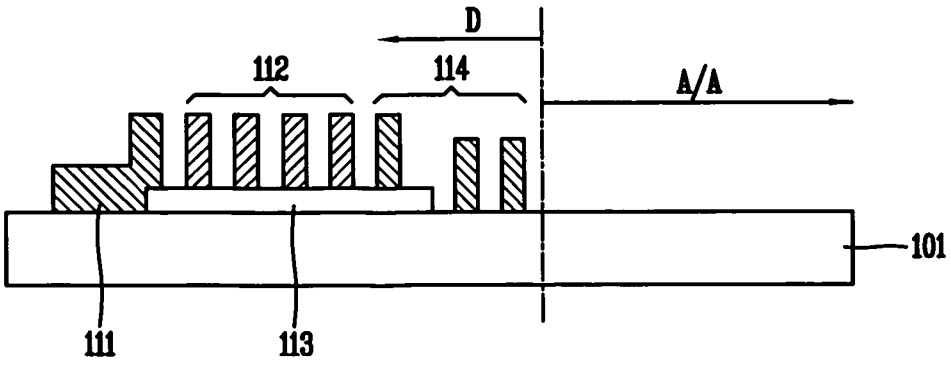


FIG. 5

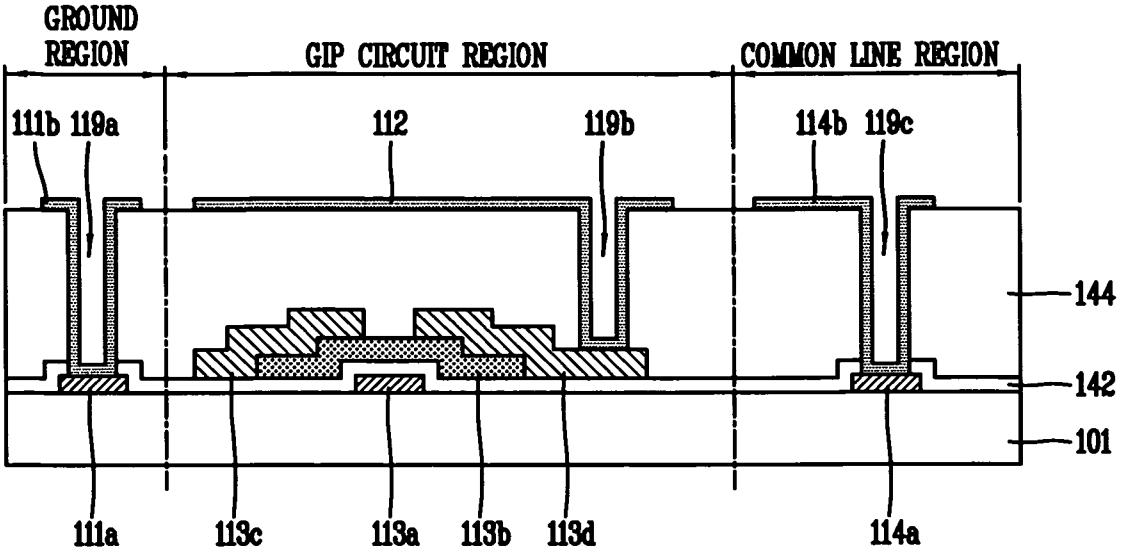

GROUND REGION
GIP CIRCUIT REGION
COMMON LINE REGION
111b
119a
112
119b
114b
119c
144
142
101
111a
113c
113a
113b
113d
114a

FIG. 6

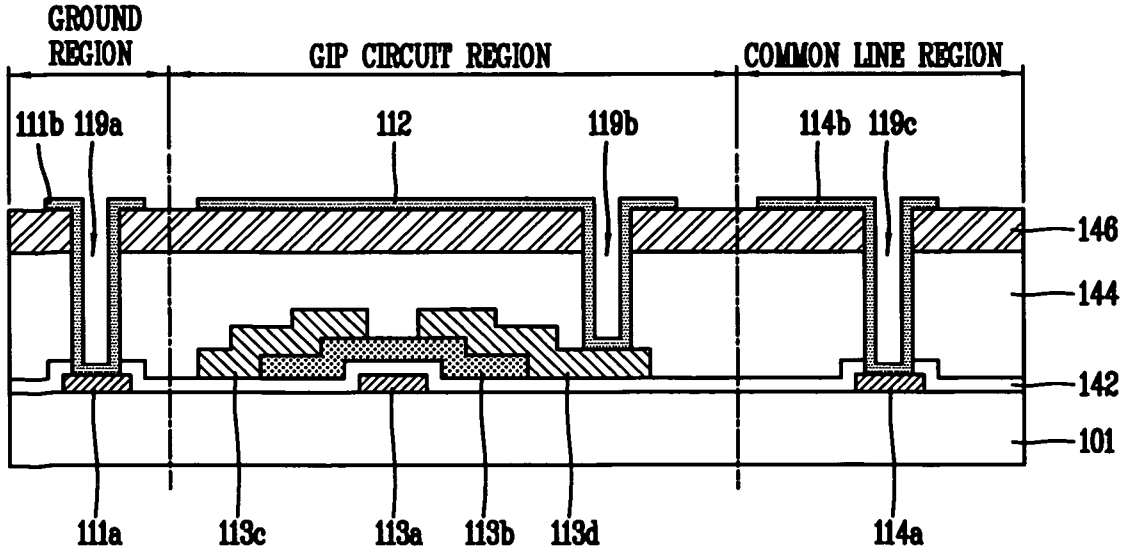

GROUND REGION
GIP CIRCUIT REGION
COMMON LINE REGION
111b
119a
112
119b
114b
119c
146
144
142
101
111a
113c
113a
113b
113d
114a

FIG. 7A

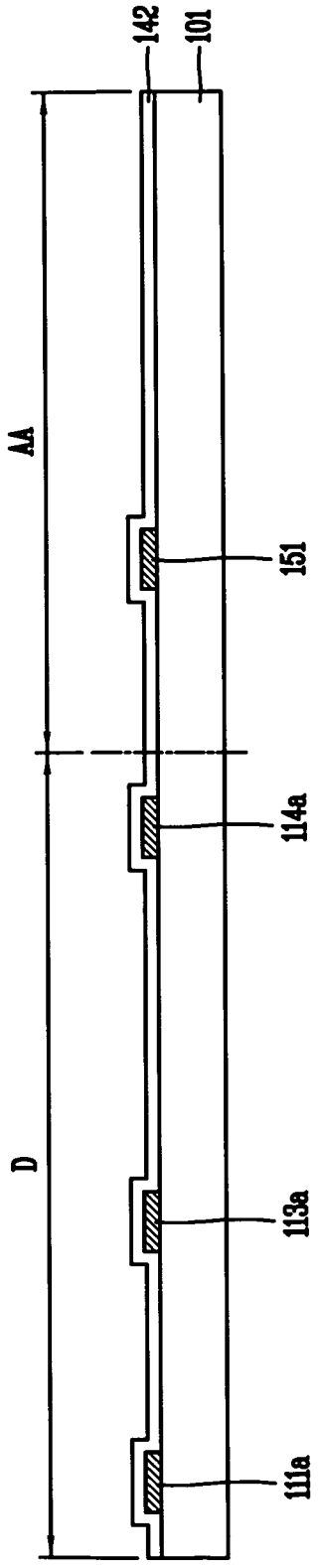

142
101
AA
151
114a
D
113a
111a

FIG. 7B

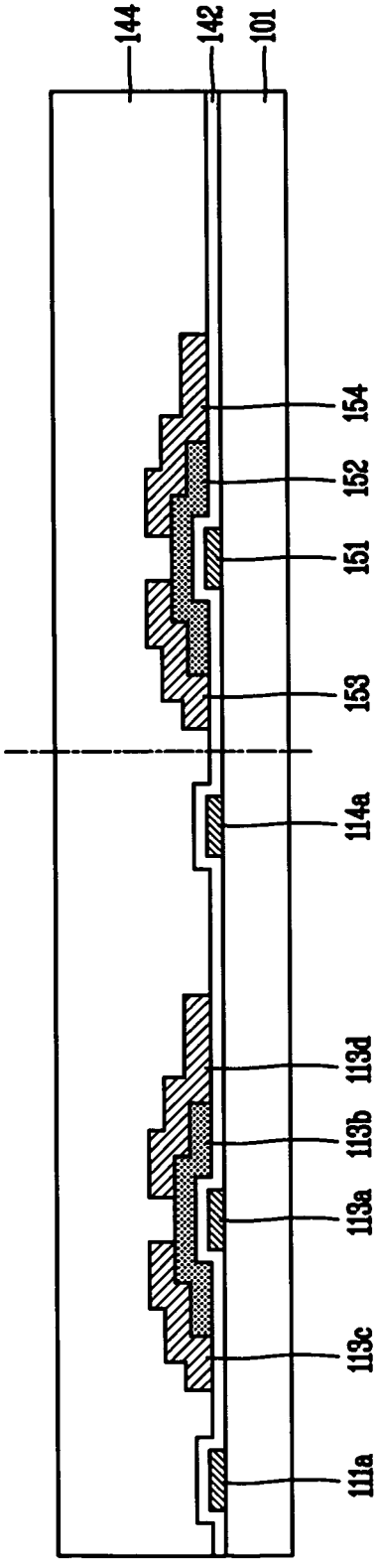

144
142
101
154
152
151
153
114a
113d
113b
113a
113c
111a

FIG. 7C

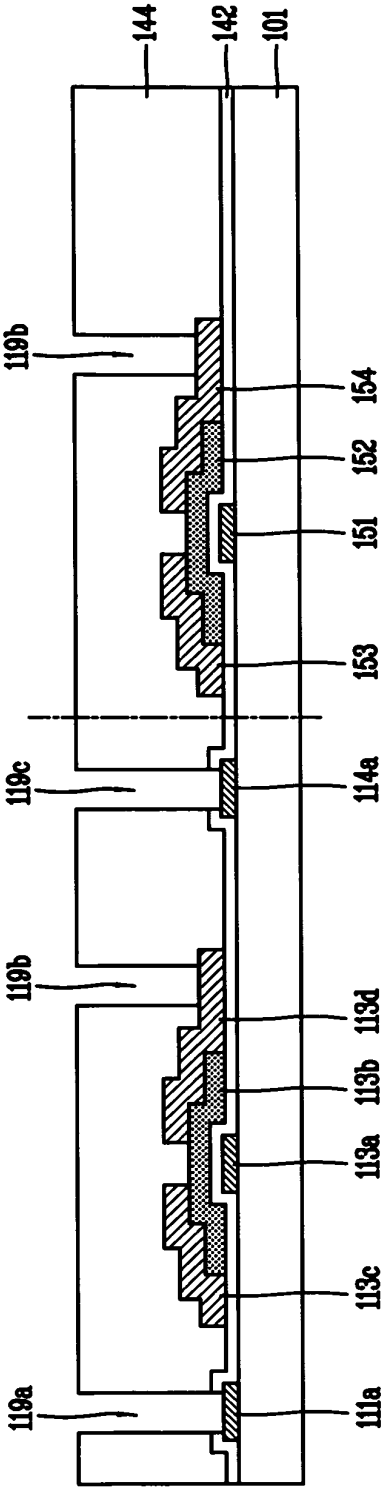
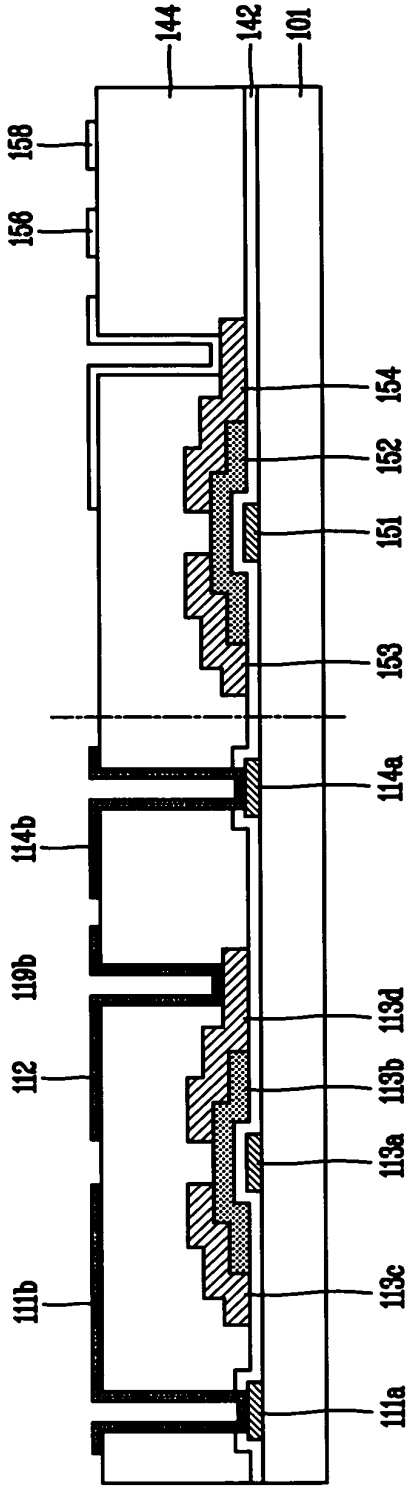

144
142
101
119b
154
152
151
153
119c
114a
119b
113d
113b
113a
113c
119a
111a

FIG. 7D


144
142
101
158
156
154
152
151
153
114a
114b
119b
113d
112
113b
113a
113c
111b
111a

REFERENCES CITED IN THE DESCRIPTION

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- US 2003094615 A1 **[0022]**

专利名称(译)	液晶显示装置具有集成的栅极驱动电路和减小的边框宽度		
公开(公告)号	EP2720082B1	公开(公告)日	2015-09-23
申请号	EP2012008576	申请日	2012-12-21
[标]申请(专利权)人(译)	乐金显示有限公司		
申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
当前申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
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发明人	LEE, YOUNG JANG JEONG, HO YOUNG LEE, BOK YOUNG		
IPC分类号	G02F1/1345 G02F1/1333		
CPC分类号	G02F1/13306 G02F1/133345 G02F1/13452 G02F1/13454 G02F2001/136222 G02F2201/42		
优先权	1020120113804 2012-10-12 KR		
其他公开文献	EP2720082A1		
外部链接	Espacenet		

摘要(译)

一种液晶显示（LCD）装置，包括：虚设区域（D），其上安装有栅极驱动器（113）;包括多个像素区域的有源区域（A / A）以实现实际图像;第一线（111a，114a）和第二线（111b，114b）设置在虚设区域（D）中，其中第一线（111a，114a）形成在基板（101）和第二线（111b，114b）上在绝缘层（144,146）上形成第一和第二线（111a，114a; 111b，114b）的部分与插入其间的绝缘层（144,146）重叠。

FIG. 1

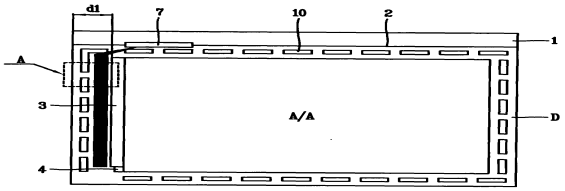

FIG. 2