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(54) **Array substrate, liquid crystal panel and liquid crystal display device**

Arraysubstrat, Flüssigkristallanzeigetafel und Flüssigkristallanzeigevorrichtung

Substrat matriciel, panneau à cristaux liquides et dispositif d'affichage à cristaux liquides

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Description

FIELD OF THE INVENTION

[0001] Embodiments of the present invention relate to an array substrate, a liquid crystal display panel and a liquid crystal display device. According to the generic part of claim 1 the invention relates to an array substrate, comprising a plurality of array substrate units, each of which comprising: gate lines and data lines extending along a first direction and a second direction crossing with each other, respectively, in a plane of a substrate, wherein, each array substrate unit comprises four array substrate sub-units which are arranged in the first direction and the second direction to form sub-unit rows and sub-unit columns, and each of sub-unit rows and sub-unit columns has two array substrate sub-units, each array substrate sub-unit comprises three pixels, and one data line and three gate lines which are electrically connected to the three pixels, the three gate lines comprising a first gate line, a second gate line and a third gate line; and the three gate lines are shared by two array substrate sub-units in each sub-unit row, and the one data line and one of the gate lines are shared by two array substrate sub-units in each sub-unit column, within each array substrate sub-unit, the three pixels are arranged in the first direction,
within each array substrate sub-unit, each pixel is electrically connected to a corresponding gate line and a corresponding data line (36, 37), respectively, through a switch,
wherein the switch is a thin-film transistor (TFT).

BACKGROUND

[0002] A liquid crystal display device is a flat panel display device in which arrangement of liquid crystal molecules is controlled by an electric field formed between a pixel electrode and a common electrode within the panel so that a refractive index of the liquid crystal molecules to light is controlled and an image is displayed. A panel of the liquid crystal display device is constituted by an array substrate and a color filter substrate. The array substrate includes a gate line extending in a horizontal direction and a data line extending in a vertical direction, and a switch is provided in each of intersections between the gate line and the data line so as to control each pixel.

[0003] Typically, the array substrate is constituted by a number of array substrate units. In the prior art, many design solutions on the array substrate units have been proposed.

[0004] Figure 1 is a schematic structural diagram of an array substrate unit. The array substrate unit illustrated in Figure 1 adopts a Dual Gate driving mode, and its specific structure is: the array substrate unit is provided with a first gate line G1, a second gate line G2, a third gate line G3 and a fourth gate lines G4 which extend in the horizontal direction, and a first data line D1, a second data line D2 and a third data line D3 which extend in the vertical direction. A pixel R1, a pixel G1, a pixel B1, a pixel R2, a pixel G2 and a pixel B2 are provided between the first gate line G1 and the second gate line G2, and the respective pixels are arranged in the horizontal direction between the first gate line G1 and the second gate line G2. A pixel R3, a pixel G3, a pixel B3, a pixel R4, a pixel G4 and a pixel B4 are provided between the third gate line G3 and the fourth gate line G4, the respective pixels are arranged in the horizontal direction between the third gate line G3 and the fourth gate lines G4. The pixel R1, the pixel G1 and the pixel B1 and the gate lines and the data line connected
thereto constitute a first array substrate sub-unit; the pixel R2, the pixel G2, and the pixel B2, and the gate lines and the data line connected thereto constitute a second array substrate sub-unit; the pixel R3, the pixel G3 and the pixel B3, and the gate lines and the data line connected thereto constitute a third array substrate sub-unit; the pixel R4, the pixel G4, the pixel B4, and the gate lines and the data lines connected thereto constitute a fourth array substrate sub-unit. In each array substrate sub-unit, each pixel is connected to the gate lines and data line in a similar manner, except being connected to different gate lines and data line. The following description is made by taking the first array substrate sub-unit as an example. The pixel R1 is electrically connected to the first gate line G1 and the first data line D1 though a switch, respectively; the pixel G1 is electrically connected to the second gate line G2 and the first data line D1 though a switch, respectively; the pixel B1 is electrically connected to the second gate line G2 and the second data line D2 though a switch, respectively.

[0005] Figure 2 is a schematic structural diagram of another array substrate unit. The array substrate unit illustrated in Figure 2 adopts a Triple Gate driving mode, and its specific structure is: the array substrate unit is provided with a first gate line G1, a second gate line G2, a third gate line G3, a fourth gate lines G4, a fifth gate line G5 and a sixth grid line G6 which extend in the horizontal direction, and a first data line D1 and a second data line D2 which extend in the vertical direction. Different from the pixel structure in Figure 1, the long side of each pixel is in the horizontal direction, and the short side in the vertical direction in Figure 2. The pixel R1 and the pixel R2 are arranged horizontally above the first gate line G1, the pixel R1 is electrically connected to the first gate line G1 and the first data line D1, the pixel R2 is electrically connected to the first gate line G1 and the second data line D2; the pixel G1 and the pixel G2 are arranged horizontally between the first gate line G1 and the second gate line G2, the pixel G1 is electrically connected to the second gate line G2 and the first data line D1, and the pixel G2 is electrically connected to the second gate line G2 and the second data line D2; the pixel B1 and the pixel B2 are arranged horizontally between the second gate line G2 and the third gate line G3, the pixel B1 is electrically connected to the third gate line G3

and the first data line D1, and the pixel B2 is electrically connected to the third gate line G3 and the second data line D2; the pixel R3 and the pixel R4 are arranged horizontally between the third gate line G3 and the fourth gate line G4, the pixel R3 is electrically connected to the fourth gate line G4 and the first data line D1, and the pixel R4 is electrically connected to the fourth gate line G4 and the second data line D2; the pixel G3 and the pixel G4 are arranged horizontally between the fourth gate line G4 and the fifth gate line G5, the pixel G3 is electrically connected to the fifth gate line G5 and the first data line D1, and the pixel G4 is electrically connected to the fifth gate line G5 and the second data line D2; the pixel B3 and the pixel B4 are arranged horizontally between the fifth gate line G5 and the sixth gate line G6, the pixel B3 is electrically connected to the sixth gate line G6 and the first data line D1, and the pixel B4 is electrically connected to the sixth gate line G6 and the second data line D2.

[0006] During the array substrate, which is constituted by array substrate units, is incorporated into a panel, Chip On Film (COF) is required. The number of COF is relative to the number of the gate lines and data lines. The more gate lines and data lines, the more COF is required, which means more product cost. Therefore, how to design a array substrate unit to reduce the number of the gate lines and the data lines and further reduce the COF quantity in the liquid crystal manufacturing process has become a technical problem in the prior art to be solved.US2003/0189559 A1 discloses a display apparatus including a first scan line; a first data line perpendicular to the first scan line; a first pixel, a second pixel, and a third pixel which are adjacent and coupled to the same data line respectively; and a first switching device, a second switching device, and a third switching device set in the first, second, and third pixels respectively. The data signals can be selectively input into the corresponding pixels from the first data line by enabling/disabling the corresponding scan lines.

SUMMARY

[0007] Embodiments of the invention provide an array substrate unit, an array substrate, a liquid crystal display panel and a liquid crystal display device, so as to reduce the number of COF used in the manufacturing process of the liquid crystal panel.

[0008] According to the characterizing portion of claim 1 an array substrate according to the invention is characterized in that: within each array substrate sub-unit, the first gate line, the three pixels, the second gate line and the third gate line are arranged sequentially in the second direction; within each array substrate unit, the first sub-unit row and the second sub-unit row are arranged sequentially in the second direction, the third gate line for the first sub-unit row and the first gate line for the second sub-unit row are the same gate line, the three pixels are a first pixel, a second pixel and a third pixel, respectively;

within each array substrate sub-unit, the first pixel is electrically connected to the first gate line, the third gate line and the data line through a first TFT and a second TFT, respectively, a gate electrode of the first TFT is connected to the third gate line, a drain electrode of the first TFT is connected to the first gate line, a source electrode of the first TFT is connected to a gate electrode of the second TFT, a drain electrode of the second TFT is connected to the data line, a source electrode of the second TFT is connected to the first pixel;

the second pixel is electrically connected to the second gate line, the third gate line and the data line through a third TFT and a fourth TFT, respectively, a gate electrode of the third TFT is connected to the third gate line, a drain electrode of the third TFT is connected to the second gate line, a source electrode of the third TFT is connected to a gate electrode of the fourth TFT, a drain electrode of the fourth TFT is connected to the data line, a source electrode of the fourth TFT is connected to the second pixel; and

the third pixel is electrically connected to the first gate line and the data line through a fifth TFT, a gate electrode of the fifth TFT is connected to the first gate line, a drain electrode of the fifth TFT is connected to the data line, and a source electrode of the fifth TFT is connected to the third pixel.

[0009] Preferred embodiments of an array substrate are provided according to the subject matter of dependent claims 2 - 4.

[0010] Another embodiment of the present invention provides a liquid crystal display panel, comprising a color filter substrate, the above array substrate and liquid crystal interposed between the color filter substrate and the array substrate.

[0011] Still another embodiment of the present invention provides a liquid crystal display device comprising a backlight, a liquid crystal panel, and an integrated circuit board that provides control signals to the liquid crystal panel, the liquid crystal display panel comprising a color filter substrate, the above array substrate and liquid crystal interposed between the color filter substrate and the array substrate.

[0012] The array substrate unit according to the embodiments of the present invention includes five gate lines and two data lines, which is reduced by one data line when comparing with the array substrate unit in the Dual Gate driving mode, and reduced by one gate line when comparing with the array substrate unit in the Triple Gate driving mode. Since each liquid crystal panel includes several hundreds of array substrate units, the number of COF used in the manufacturing process of the liquid crystal panel is reduced effectively.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] In order to clearly illustrate the technical solution of the embodiments of the invention, the drawings of the embodiments will be briefly described in the following; it

is obvious that the described drawings are only related to some embodiments of the invention and thus are not limitative of the invention.

Figure 1 is structural diagram of an array substrate unit in a Dual Gate driving mode in the prior art;

Figure 2 is structural diagram of an array substrate unit in a Triple Gate driving mode in the prior art;

Figure 3a is a structural diagram of an array substrate sub-unit according to an embodiment of the invention;

Figure 3b is a structural diagram of an array substrate unit according to an embodiment of the invention;

Figure 4 is a waveform of a driving signal supplied by each gate line according to an embodiment of the invention.

DETAILED DESCRIPTION

[0014] In order to make objects, technical details and advantages of the embodiments of the invention apparent, the technical solutions of the embodiment will be described in a clearly and fully understandable way in connection with the drawings related to the embodiments of the invention. It is obvious that the described embodiments are just a part but not all of the embodiments of the invention. Based on the described embodiments herein, those skilled in the art can obtain other embodiment(s), without any inventive work, which should be within the scope of the invention.

[0015] In order to reduce the COF number required in the liquid crystal panel manufacturing process, embodiments of the invention provide an array substrate unit, an array substrate, a liquid crystal panel and a liquid crystal display device.

[0016] According to an embodiment of the present invention, an array substrate unit includes four array substrate sub-units, and these array substrate sub-units are symmetric in pair-wise manner in a horizontal direction and a vertical direction. Each array substrate sub-unit includes three pixels, respectively, a pixel R, a pixel G, and a pixel B, and one data line and three gate lines electrically connected to the three pixels. The three gate lines are a gate line G1, a gate line G2 and a gate line G3. Two array substrate sub-units arranged in the horizontal direction share the three gate lines, and two array substrate sub-units arranged in the vertical direction share the one data base line and one of the gate lines.

[0017] For example, the four array substrate sub-units are arranged in the horizontal direction and the vertical direction to form sub-unit rows and sub-unit columns, and each sub-unit row and each sub-unit column includes two array substrate sub-units.

[0018] For example, each array substrate sub-unit includes three pixels, and one data line and three gate lines which are electrically connected to the three pixels, and the three gate lines includes a first gate line, a second gate line and a third gate line. The three gate lines are shared by two array substrate sub-units in each sub-unit row, and the one data line and one of the gate lines are shared by two array substrate sub-units in each sub-unit column.

[0019] In one example, within each array substrate sub-unit, the first gate line, the three pixels, the second gate line and the third gate line are arranged sequentially in the second direction; within each array substrate unit, the first sub-unit row and the second sub-unit row are arranged sequentially in the second direction, the third gate line for the first sub-unit row and the first gate line for the second sub-unit row are the same gate line. For example, in each array substrate sub-unit, the three pixels are arranged in the first direction.

[0020] For example, Figure 3a is a structural diagram of an array substrate sub-unit. In each array substrate sub-unit, a pixel R is electrically connected to a gate line G1, a gate line G3 and a data line through a first TFT 38 and a second TFT 39. For example, the gate electrode of the first TFT 38 is connected to the gate line G3, the drain electrode of the first TFT 38 is connected to the gate line G1, the source electrode of the first TFT 38 is connected to the gate electrode of the second TFT 39, the drain electrode of the second TFT 39 is connected to the data line, the source electrode of the second TFT 39 is connected to the pixel R. A pixel G is electrically connected to the gate line G2, the gate line G3 and the data line through a third TFT 310 and a fourth TFT 311. For example, the gate electrode of the third TFT 310 is connected to the gate line G3, the drain electrode of the third TFT 310 is connected to the gate line G2, the source electrode of the third TFT 310 is connected to the gate electrode of the fourth TFT 311, the drain electrode of the fourth TFT 311 is connected to the data line, the source electrode of the fourth TFT 311 is connected to the pixel G. A pixel B is electrically connected to the gate line G1 and the data line through a fifth TFT 312. For example, the gate electrode of the fifth TFT 312 is connected to the gate line G1, and the drain electrode of the fifth TFT 312 is connected to the data line, and the source electrode of the fifth TFT 312 is connected to the pixel B.

[0021] As for an array substrate unit constituted by four array substrate sub-units, the two array substrate sub-units sequentially arranged in the horizontal direction share three gate lines, and the two array substrate sub-units arranged in the vertical direction share a single data line. In the vertical direction, the first gate line in a lower array substrate sub-unit and the last gate line in the upper array substrate sub-unit are the same gate line. For convenience of description, the three gate lines connected to the two array substrate sub-units (in the upper side in Figure 3b) sequentially arranged in the horizontal direction are represented as a first gate line 31, a second gate line 32, a third gate line 33; the three gate lines connected to the other two array substrate sub-units (in the lower side in Figure 3b) sequentially arranged in the horizontal direction are represented as the third gate line 33, a fourth gate line 34, a fifth gate line 35. That is to say, the two

array substrate sub-units (in the upper side in Figure 3b) sequentially arranged in the horizontal direction share the first gate line, the second gate line, and the third gate line; the other two array substrate sub-units (in the lower side in Figure 3b) sequentially arranged in the horizontal direction share the third gate line, the fourth gate line, and the fifth gate line, as illustrated in Figure 3b.

[0022] The array substrate unit includes the first gate line 31, the second gate line 32, a third gate line 33, the fourth gate line 34 and the fifth gate lines 35 which extend in the horizontal direction, and a first data line 36 and a second data line 37 which extend in the vertical direction; a pixel R1, a pixel G1, a pixel B1, a pixel R2, a pixel G2, a pixel B2 provided between the first gate line 31 and the second gate line 32 in this order; a pixel R3, a pixel G3, a pixel B3, a pixel R4, a pixel G4, a pixel B4 provided between the third gate line 33 and the fourth gate line 34. Each gate line is used to supply driving signals, and each data line is used to supply voltage signals the polarities of which are reversed continuously.

[0023] For example, the pixel R1 is electrically connected to the first gate line 31, the third gate line 33 and the first data line 36; the pixel G1 is electrically connected to the second gate line 32, the third gate line 33 and the first data line 36; the pixel B1 is electrically connected to the first gate line 31 and the first data line 36; the pixel R2 is electrically connected to the first gate line 31, the third gate line 33 and the second data line 37; the pixel G2 is electrically connected to the second a gate line 32, the third gate line 33 and the second data line 37; the pixel B2 is electrically connected to the first gate line 31 and the second data line 37; the pixel R3 is electrically connected to the third gate line 33, the fifth gate line 35 and the first data line 36; the pixel G3 is electrically connected to the fourth gate line 34, the fifth gate line 35 and the first data line 36; the pixel B3 is electrically connected to the third gate line 33 and the first data line 36; the pixel R4 is electrically connected to the third gate line 33, the fifth gate line 35 and the second data line 37; the pixel G4 is electrically connected to the fourth gate line 34, the fifth gate line 35 and the second data line 37; the pixel B4 is electrically connected to the third pixel gate line 33 and the second data line 37.

[0024] The pixel R1, the pixel G1, the pixel B1, and the gate lines and the data line connected to each pixel constitute a first array substrate sub-unit, i.e. the pixel R1, the pixel G1, the pixel B1, the first gate line 31, the second gate line 32, the third gate line 33 and the first data line 36 constitute the first array substrate sub-unit, the pixel R2, the pixel G2, the pixel B2, and the gate lines and the data line connected to each pixel constitute a second array substrate sub-unit, i.e., the pixel R2 , the pixel G2, the pixel B2, and the first gate line pixel 31, the second gate line 32, the third gate line 33 and the second data line 37 constitute the second array substrate sub-unit. The second array substrate sub-unit and the first array substrate sub-unit share the three gate lines, i.e., the first gate line 31, the second gate line 32 and the third gate line 33. The pixel R3, the pixel G3, the pixel B3 and the gate lines and the data line connected to each pixel constitute a third array substrate sub-unit, i.e., the pixels R3, the pixel G3, the pixel B3, the third gate line 33, the fourth gate line 34, the fifth gate line 35 and the first data line 36 constitute the third array substrate sub-unit. The third array substrate sub-unit and the first array substrate sub-unit share the first data line 36 and the third gate line 33. The pixel R4, the pixel G4, the pixel B4 pixel and the gate lines and the data line connected to each pixel constitute a fourth array substrate sub-unit, i.e., the pixel R4, the pixel G4, the pixel B4, the third gate line 33, the fourth gate line 34, the fifth gate line 35 and the second data line 37 constitute the fourth array substrate sub-unit. The fourth array substrate sub-unit and the third array substrate sub-unit share three gate lines, i.e., the third gate line 33, the fourth gate line 34 and the fifth gate line 35; the fourth array substrate sub-unit and the second array substrate sub-unit share the second data line 37 and the third gate line 33. In each array substrate sub-unit, each pixel is electrically connected to the corresponding gate line and data line through switches and the switches include but not limited to thin film transistor (TFT).

[0025] In one example, if each pixel is connected to the corresponding gate line and data line through the TFT, as illustrated in Figure 3, the specific structure can be as follows: in the first array substrate sub-unit, the pixel R1 is electrically connected to the first gate line 31, the third gate line 33 and the first data line 36 through the first TFT 38 and the second TFT 39. For example, the gate electrode of the first TFT 38 is connected to the third gate line 33, the drain electrode of the first TFT 38 is connected to the first gate line 31, the source electrode of the first TFT 38 is connected to the gate electrode of the second TFT 39, the drain electrode of the second TFT 39 is connected to the first data line, the source electrode of the second TFT 39 is connected to the pixel R1. The pixel G1 is electrically connected to the second gate line 32, the third gate line 33 and the first data line 36 through the third TFT 310 and the fourth TFT 311. For example, the gate electrode of the third TFT 310 is connected to the third gate line 33, the drain electrode of the third TFT 310 is connected to the second gate line 32, a source electrode of the third TFT 310 is connected to a gate electrode of the fourth TFT 311, the drain electrode of the fourth TFT 311 is connected to the first data line, the source electrode of the fourth TFT 311 is connected to the pixel G1. The pixel B1 is electrically connected to the first gate line 31 and the first data line through a fifth TFT 312. For example, the gate electrode of the fifth TFT 312 is connected to the first gate line 31, the drain electrode of the fifth TFT 312 is connected to the first data line, and the source electrode of the fifth TFT 312 is connected to the pixel B1.

[0026] In the second array substrate sub-unit, the pixel R2 is electrically connected to the first gate line 31, the third gate line 33 and the second data line through the first TFT 38 and the second TFT 39. For example, the

gate electrode of the first TFT 38 is connected to the third gate line 33, the drain electrode of the first TFT 38 is connected to the first gate line 31, the source electrode of the first TFT 38 is connected to the gate electrode of the second TFT 39, the drain electrode of the second TFT 39 is connected to the second data line, and the source electrode of the second TFT 39 is connected to the pixel R2. The pixel G2 is electrically connected to the second gate line 32, the third gate line 33 and the second data line through the third TFT 310 and the fourth TFT 311. For example, the gate electrode of the third TFT 310 is connected to the third gate line 33, the drain electrode of the third TFT 310 is connected to the second gate line 32, the source electrode of the third TFT 310 is connected to the gate electrode of the fourth TFT 311, the drain electrode of the fourth TFT 311 is connected to the second data line, the source electrode of the fourth TFT 311 is connected to the pixel G2. The pixel B2 is electrically connected to the first gate line 31 and the second data line through a fifth TFT 312. For example, the gate electrode of the fifth TFT 312 is connected to the first gate line 31, the drain electrode of the fifth TFT 312 is connected to the second data line, and the source electrode of the fifth TFT 312 is connected to the pixel B2.

[0027] In the third array substrate sub-unit, the pixel R3 is electrically connected to the third gate line 31, the fifth gate line 35 and the first data line through the first TFT 38 and the second TFT 39. For example, the gate electrode of the first TFT 38 is connected to the fifth gate line 35, the drain electrode of the first TFT 38 is connected to the third gate line 33, the source electrode of the first TFT 38 is connected to a gate electrode of the second TFT 39, the drain electrode of the second TFT 39 is connected to the first data line, and the source electrode of the second TFT 39 is connected to the pixel R3. The pixel G3 is electrically connected to the fourth gate line 34, the fifth gate line 35 and the first data line 36 through the third TFT 310 and the fourth TFT 311. For example, the gate electrode of the third TFT 310 is connected to the fifth gate line 35, the drain electrode of the third TFT 310 is connected to the fourth gate line 34, the source electrode of the third TFT 310 is connected to the gate electrode of the fourth TFT 311, the drain electrode of the fourth TFT 311 is connected to the first data line 36, and the source electrode of the fourth TFT 311 is connected to the pixel G3. The pixel B3 is electrically connected to the third gate line 33 and the first data line 36 through a fifth TFT 312. For example, the gate electrode of the fifth TFT 312 is connected to the third gate line 33, the drain electrode of the fifth TFT 312 is connected to the first data line 36, and the source electrode of the fifth TFT 312 is connected to the pixel B3.

[0028] In the fourth array substrate sub-unit, the pixel R4 is electrically connected to the third gate line 31, the fifth gate line 35 and the second data line 37 through the first TFT 38 and the second TFT 39. For example, the gate electrode of the first TFT 38 is connected to the fifth gate line 35, the drain electrode of the first TFT 38 is connected to the third gate line 33, the source electrode of the first TFT 38 is connected to a gate electrode of the second TFT 39, the drain electrode of the second TFT 39 is connected to the second data line 37, and the source electrode of the second TFT 39 is connected to the pixel R4. The pixel G4 is electrically connected to the fourth gate line 34, the fifth gate line 35 and the second data line 37 through the third TFT 310 and the fourth TFT 311. For example, the gate electrode of the third TFT 310 is connected to the fifth gate line 35, the drain electrode of the third TFT 310 is connected to the fourth gate line 34, the source electrode of the third TFT 310 is connected to the gate electrode of the fourth TFT 311, the drain electrode of the fourth TFT 311 is connected to the second data line 37, and the source electrode of the fourth TFT 311 is connected to the pixel G4. The pixel B4 is electrically connected to the third gate line 33 and the second data line 37 through a fifth TFT 312. For example, the gate electrode of the fifth TFT 312 is connected to the third gate line 33, the drain electrode of the fifth TFT 312 is connected to the second data line 37, and the source electrode of the fifth TFT 312 is connected to the pixel B4.

[0029] Figure 4 illustrates a waveform of driving signals supplied by various gate lines according to an embodiment of the invention. Upon the time 1 being reached, the first gate line 31 and the third gate line 33 are in a high level, the rest of the gate lines are in a low level, so that the first data line 36 charges the pixel R1 and the pixel B1, and the second data line 37 charges the pixel R2 and the pixel B2. Assuming a voltage required by the pixel R1 is 8V, and a voltage required by the pixel B1 is 16V, at the time 1, charging on the pixel B1 is a pre-charge, and for the next time of charging on the pixel B1, it can be started from 8V. Similarly, at the time 1, charging on the pixel B2 is a pre-charge, and for the next time of charging on the pixel B2, it can be started from 8V. At the time 2, the second gate line 32 and the third gate line 33 is in a high level, the first data line 36 charges the pixel G1, the second data line 37 charges the pixel G2. At time 3, the first gate line 31 is in a high level, the first data line 36 charges the pixel B1, the second data line 37 charges the pixel B2, and so on. The gate lines control the data lines according to the received driving signals to charge each pixel at the time 4, the time 5, the time 6, the time 7 and the time 8.

[0030] The structure of the array substrate unit is described with the first gate line, the second gate line, the third gate line, the fourth gate line and the fifth gate line as above. However, the structure for each array substrate sub-unit in the array substrate unit is the same. Actually, each array substrate sub-unit includes three gate lines, and the third gate line and the first gate line between two sub-unit rows adjacent in the vertical direction are the same gate line (shared). That is, the above first to fifth gate lines may be referred as the first gate line for the first sub-unit row, the second gate line for the first sub-unit row, the third gate line for the first sub-unit row (or

the first gate line for the second sub-unit row), the second gate line for the second sub-unit row and the third gate line for the second sub-unit row.

[0031] The above horizontal direction and the vertical direction are two directions perpendicular to each other in a plane of the array substrate, respectively. However, the array substrate according to the present embodiment is not limited to two directions perpendicular to each other, but may be crossing with each other in any other angles.

[0032] For example, a predetermined number of array substrate units according to the embodiments of the invention can constitute an array substrate, and the array substrate can be used to constitute a liquid crystal panel in which liquid crystal is interposed between the array substrate and a color filter substrate. Further, the liquid crystal panel, together with a backlight and an integrated circuit board for supplying control signals to the liquid crystal panel, can be used to constitute a liquid crystal display device. In the above devices, except that the array substrate adopts the array substrate according to the embodiments of the invention, other structures can be the same as those in the prior art, which will not be described in detail herein.

[0033] Further, a plurality of array substrate units according to the embodiments of the present invention can be arranged in a matrix in an array substrate. In the vertical direction, the last third gate line in the previous array substrate unit and the foremost first gate line in the next array substrate unit can be the same gate line.

[0034] Embodiments of the present invention provide an array substrate unit, an array substrate, a liquid crystal display panel and a liquid crystal display device. Each array substrate unit includes four array substrate sub-units, and these array substrate sub-units are symmetric in pair-wise manner in a horizontal direction and a vertical direction. Each array substrate sub-unit includes three pixels, and one data lines and three gate lines electrically connected to the three pixels. Two array substrate sub-units arranged in the horizontal direction share the three gate lines, and two array substrate sub-units arranged in the vertical direction share the one data base line and one of the gate lines. Therefore, the array substrate unit according to the embodiments of the present invention includes five gate lines and two data lines, which is reduced by one data line when comparing with the array substrate unit in the Dual Gate driving mode, and reduced by one gate line when comparing with the array substrate unit in the Triple Gate driving mode. Since each liquid crystal panel includes several hundreds of array substrate units, the number of COF used in the manufacturing process of the liquid crystal panel can be reduced effectively.

[0035] The foregoing are merely exemplary embodiments of the invention, but are not used to limit the protection scope of the invention. The protection scope of the invention shall be defined by the attached claims.

Claims

1. An array substrate, comprising a plurality of array substrate units, each of which comprising: gate lines (G1, G2, G3; 31, 32, 33, 34, 35) and data lines (36, 37) extending along a first direction and a second direction crossing with each other, respectively, in a plane of a substrate, wherein,

each array substrate unit comprises four array substrate sub-units which are arranged in the first direction and the second direction to form sub-unit rows and sub-unit columns, and each of sub-unit rows and sub-unit columns has two array substrate sub-units,

each array substrate sub-unit comprises three pixels (R, G, B; R1, G1, B1, R2, G2, B2, R3, G3, B3, R4, G4, B4), and one data line (36, 37) and three gate lines (G1, G2, G3; 31, 32, 33, 34, 35) which are electrically connected to the three pixels (R, G, B; R1, G1, B1, R2, G2, B2, R3, G3, B3, R4, G4, B4), the three gate lines (G1, G2, G3; 31, 32, 33, 34, 35) comprising a first gate line (G1; 31, 33), a second gate line (G2; 32, 34) and a third gate line (G3; 33, 35); and

the three gate lines (G1, G2, G3; 31, 32, 33, 34, 35) are shared by two array substrate sub-units in each sub-unit row, and the one data line (36, 37) and one of the gate lines (G1, G2, G3; 31, 32, 33, 34, 35) are shared by two array substrate sub-units in each sub-unit column,

within each array substrate sub-unit, the three pixels (R, G, B; R1, G1, B1, R2, G2, B2, R3, G3, B3, R4, G4, B4) are arranged in the first direction,

within each array substrate sub-unit, each pixel (R, G, B; R1, G1, B1, R2, G2, B2, R3, G3, B3, R4, G4, B4) is electrically connected to a corresponding gate line (G1, G2, G3; 31, 32, 33, 34, 35) and a corresponding data line (36, 37), respectively, through a switch (38, 39, 310, 311, 312),

wherein the switch (38, 39, 310, 311, 312) is a thin-film transistor (TFT),

characterized in that:

within each array substrate sub-unit, the first gate line (G1; 31, 33), the three pixels (R, G, B; R1, G1, B1, R2, G2, B2, R3, G3, B3, R4, G4, B4), the second gate line (G2; 32, 34) and the third gate line (G3; 33, 35) are arranged sequentially in the second direction;

within each array substrate unit, the first sub-unit row and the second sub-unit row are arranged sequentially in the second direction, the third gate line (33) for the first sub-unit row and the first gate line (33) for the second sub-unit row are the same gate line;

the three pixels (R, G, B; R1, G1, B1, R2, G2, B2, R3, G3, B3, R4, G4, B4) are a first pixel (R; R1, R2, R3, R4), a second pixel (G; G1, G2, G3, G4) and a third pixel (B; B1, B2, B3, B4), respec-

tively;
within each array substrate sub-unit, the first pixel (R; R1, R2, R3, R4) is electrically connected to the first gate line (G1; 31, 33), the third gate line (G3; 33, 35) and the data line (36, 37) through a first TFT (38) and a second TFT (39), respectively, a gate electrode of the first TFT (38) is connected to the third gate line (G3; 33, 35), a drain electrode of the first TFT (38) is connected to the first gate line (G1; 31, 33), a source electrode of the first TFT (38) is connected to a gate electrode of the second TFT (39), a drain electrode of the second TFT (39) is connected to the data line (36, 37), a source electrode of the second TFT (39) is connected to the first pixel (R; R1, R2, R3, R4);
the second pixel (G; G1, G2, G3, G4) is electrically connected to the second gate line (G2; 32, 34), the third gate line (G3; 33, 35) and the data line (36, 37) through a third TFT (310) and a fourth TFT (311), respectively, a gate electrode of the third TFT (310) is connected to the third gate line (G3; 33, 35), a drain electrode of the third TFT (310) is connected to the second gate line (G2; 32, 34), a source electrode of the third TFT (310) is connected to a gate electrode of the fourth TFT (311), a drain electrode of the fourth TFT (311) is connected to the data line (36, 37), a source electrode of the fourth TFT (311) is connected to the second pixel (G; G1, G2, G3, G4); and
the third pixel (B; B1, B2, B3, B4) is electrically connected to the first gate line (G1; 31, 33) and the data line (36, 37) through a fifth TFT (312), a gate electrode of the fifth TFT (312) is connected to the first gate line (G1; 31, 33), a drain electrode of the fifth TFT (312) is connected to the data line (36, 37), and a source electrode of the fifth TFT (312) is connected to the third pixel (B; B1, B2, B3, B4).

2. The array substrate according to any one of claims 1, wherein a plurality of the array substrate units are arranged in a matrix, and in the second direction, the last third gate line (33) in a previous array substrate unit and the foremost first gate line (33) in a next array substrate unit are the same gate line.

3. The array substrate according to claims 1 or 2, wherein the first direction and the second direction are perpendicular to each other.

4. The array substrate according to any one of claims 1-3, wherein the gate lines (G1, G2, G3; 31, 32, 33, 34, 35) are configured to supply driving signals, and the data line (36, 37) is configured to supply voltage signals, polarities of which are reversed continuously.

5. A liquid crystal display panel, comprising a color filter substrate, an array substrate and liquid crystal interposed between the color filter substrate and the array substrate, wherein the array substrate is an array substrate according to any one of claims 1-3.

6. A liquid crystal display device, comprising a backlight, a liquid crystal panel, and a integrated circuit board that provides control signals to the liquid crystal panel, the liquid crystal display panel comprising a color filter substrate, an array substrate and liquid crystal interposed between the color filter substrate and the array substrate, wherein the array substrate is an array substrate according to any one of claims 1-3.

Patentansprüche

1. Array-Substrat, umfassend eine Mehrzahl von Array-Substrateinheiten, von denen jede umfasst: Gate-Leitungen (G1, G2, G3; 31, 32, 33, 34, 35) und Datenleitungen (36, 37), die sich entlang einer ersten Richtung und einer zweiten Richtung, die sich gegenseitig kreuzen, in einer Ebene eines Substrates erstrecken, wobei
jede Array-Substrateinheit vier Array-Substratuntereinheiten umfasst, die in der ersten Richtung und in der zweiten Richtung angeordnet sind, um Untereinheitreihen und Untereinheitspalten zu bilden, und wobei jede der Untereinheitreihen und Untereinheitspalten zwei Substratuntereinheiten aufweist,
wobei jede Array-Substratuntereinheit drei Pixel (R, G, B; R1, G1, B1, R2, G2, B2, R3, G3, B3, R4, G4, B4) und eine Datenleitung (36, 37) und drei Gate-Leitungen (G1, G2, G3; 31, 32, 33, 34, 35), die elektrisch mit den drei Pixeln (R, G, B; R1, G1, B1, R2, G2, B2, R3, G3, B3, R4, G4, B4) verbunden sind, aufweist, wobei die drei Gate-Leitungen (G1, G2, G3; 31, 32, 33, 34, 35) eine erste Gate-Leitung (G1; 31, 33), eine zweite Gate-Leitung (G2; 32, 34) und eine dritte Gate-Leitung (G3; 33, 35)umfassen; und
wobei die drei Gate-Leitungen (G1, G2, G3; 31, 32, 33, 34, 35) gemeinsam genutzt werden mittels zwei Array-Substratuntereinheiten in jeder Untereinheitreihe, und wobei die eine Datenleitung (36, 37) und eine der Gate-Leitungen (G1, G2, G3; 31, 32, 33, 34, 35) gemeinsam genutzt werden mittels zwei Array-Substratuntereinheiten in jeder Untereinheitspalte,
wobei innerhalb von jeder Array-Substratuntereinheit die drei Pixel (R, G, B; R1, G1, B1, R2, G2, B2, R3, G3, B3, R4, G4, B4) in der ersten Richtung angeordnet sind,
wobei innerhalb jeder Array-Substratuntereinheit jedes Pixel (R, G, B; R1, G1, B1, R2, G2, B2, R3, G3, B3, R4, G4, B4) elektrisch verbunden ist mit einer korrespondierenden Gate-Leitung (G1, G2, G3; 31,

32, 33, 34, 35) und mit einer korrespondierenden Datenleitung (36, 37),
durch einen Schalter (38, 39, 310, 311, 312),
wobei der Schalter (38, 39, 310, 311, 312) ein Dünnschichttransistor (TFT) ist,
dadurch gekennzeichnet:

dass innerhalb jeder Array-Substratuntereinheit die erste Gate-Leitung (G1; 31, 33), die drei Pixel (R, G, B; R1, G1, B1, R2, G2, B2, R3, G3, B3, R4, G4, B4), die zweite Gate-Leitung (G2; 32, 34) und die dritte Gate-Leitung (G3; 33, 35) fortlaufend in der zweiten Richtung angeordnet sind;
dass innerhalb jeder Array-Substrateinheit die erste Untereinheitreihe und die Untereinheitreihe fortlaufend in der zweiten Richtung angeordnet sind, wobei die dritte Gate-Leitung (33) für die erste Untereinheitreihe und die erste Gate-Leitung (33) für die zweite Untereinheitreihe die gleiche Gate-Leitung sind;
dass die drei Pixel (R, G, B; R1, G1, B1, R2, G2, B2, R3, G3, B3, R4, G4, B4) ein erstes Pixel (R; R1, R2, R3, R4), ein zweites Pixel (G; G1, G2, G3, G4) und ein drittes Pixel (B; B1, B2, B3, B4) sind,
dass innerhalb jeder Array-Substratuntereinheit das erste Pixel (R; R1, R2, R3, R4) elektrisch verbunden ist mit der ersten Gate-Leitung (G1; 31, 33), der dritten Gate-Leitung (G3; 33, 35) und der Datenleitung (36, 37) mittels eines ersten TFT (38) und eines zweiten TFT (39), wobei eine Gate-Elektrode des ersten TFT (38) verbunden ist mit der dritten Gate-Leitung (G3; 33, 35), wobei eine Drain-Elektrode des ersten TFT (38) verbunden ist mit der ersten Gate-Leitung (G1; 31, 33), wobei eine Source-Elektrode des ersten TFT (38) verbunden ist mit einer Gate-Elektrode des zweiten TFT (39), wobei eine Drain-Elektrode des zweiten TFT (39) verbunden ist mit der Datenleitung (36, 37), wobei eine Source-Elektrode des zweiten TFT (39) verbunden ist mit dem ersten Pixel (R, R1, R2, R3, R4);
dass das zweite Pixel (G; G1, G2, G3, G4) elektrisch verbunden ist mit der zweiten Gate-Leitung (G2; 32, 34), der dritten Gate-Leitung (G3; 33, 35) und der Datenleitung (36, 37) durch einen dritten TFT (310) und einen vierten TFT (311), wobei eine Gate-Elektrode des dritten TFT (310) verbunden ist mit der dritten Gate-Leitung (G3; 33, 35), wobei eine Drain-Elektrode des dritten TFT (310) verbunden ist mit der zweiten Gate-Leitung (G2; 32, 34), wobei eine Source-Elektrode des dritten TFT (310) verbunden ist mit einer Gate-Elektrode des vierten TFT (311), wobei eine Drain-Elektrode des vierten TFT (311) verbunden ist mit der Datenleitung 36, 37), wobei eine Source-Elektrode des vierten TFT (311) verbunden ist mit dem zweiten Pixel (G; G1, G2, G3, G4); und
dass das dritte Pixel (B; B1, B2, B3, B4) elektrisch verbunden ist mit der ersten Gate-Leitung (G1; 31, 33) und der Datenleitung (36, 37) durch einen fünften TFT (312), wobei eine Gate-Elektrode des fünften TFT (312) verbunden ist mit der ersten Gate-Leitung (G1; 31, 33), wobei eine Drain-Elektrode des fünften TFT (312) verbunden ist mit der Datenleitung (36, 37) und wobei eine Source-Elektrode des fünften TFT (312) verbunden ist mit dem dritten Pixel (B; B1, B2, B3, B4).

2. Array-Substrat gemäß Anspruch 1, wobei eine Mehrzahl der Array-Substrateinheiten in einer Matrix angeordnet ist, und wobei in der zweiten Richtung die letzte dritte Gate-Leitung (33) in einer früheren Array-Substrateinheit und die vorderste erste Gate-Leitung (33) in einer nächsten Array-Substrateinheit die gleiche Gate-Leitung sind.

3. Array-Substrat gemäß Anspruch 1 oder 2, wobei die erste Richtung und die zweite Richtung senkrecht zueinander sind.

4. Array-Substrat gemäß einem der Ansprüche 1-3, wobei die Gate-Leitungen (G1, G2, G3; 31, 32, 33, 34, 35) konfiguriert sind, um Treibersignale zu übertragen, und wobei die Datenleitung (36, 37) konfiguriert ist, um Spannungssignale zu übertragen, deren Polaritäten kontinuierlich umgekehrt werden.

5. Flüssigkristallanzeigetafel, umfassend ein Farbfiltersubstrat, ein Array-Substrat und Flüssigkristall, das zwischen dem Farbfiltersubstrat und dem Array-Substrat angeordnet ist, wobei das Array-Substrat ein Array-Substrat gemäß einem der Ansprüche 1-3 ist.

6. Flüssigkristallanzeigevorrichtung, umfassend ein Hintergrundlicht, eine Flüssigkristalltafel und ein integriertes Schaltungs-Board, das Steuersignale an die Flüssigkristalltafel liefert, wobei die Flüssigkristallanzeigetafel ein Farbfiltersubstrat, ein Array-Substrat und Flüssigkristall, das zwischen dem Farbfiltersubstrat und dem Array-Substrat angeordnet ist, umfasst, wobei das Array-Substrat ein Array-Substrat gemäß einem der Ansprüche 1-3 ist.

Revendications

1. Un substrat de réseau, comprenant une pluralité d'unités de substrat de réseau dont chacune comprend : des lignes de grille (G1, G2, G3 ; 31, 32, 33, 34, 35) et des lignes de données (36, 37) s'étendant le long d'une première direction et d'une secon-

de direction se croisant l'une l'autre, respectivement, dans un plan d'un substrat, dans lequel,
chaque unité de substrat de réseau comprend quatre sous-unités de substrat de réseau qui sont agencées dans la première direction et la seconde direction pour former des rangées de sous-unités et des colonnes de sous-unités, et chacune des rangées de sous-unités et des colonnes de sous-unité comporte deux sous-unités de substrat de réseau,
chaque sous-unité de substrat de réseau comprend trois pixels (R, G, B ; R1, G1, B1, R2, G2, B2, R3, G3, B3, R4, G4, B4) et une ligne de données (36, 37) et trois lignes de grille (G1, G2, G3 ; 31, 32, 33, 34, 35) qui sont connectées électriquement aux trois pixels (R, G, B ; R1, G1, B1, R2, G2, B2, R3, G3, B3, R4, G4, B4), les trois lignes de grille (G1, G2, G3 ; 31, 32, 33, 34, 35) comprenant une première ligne de grille (G1 ; 31, 33), une seconde ligne de grille (G2 ; 32, 34) et une troisième ligne de grille (G3; 33, 35) ; et
les trois lignes de grille (G1, G2, G3 ; 31, 32, 33, 34, 35) sont partagées par deux sous-unités de substrat de réseau dans chaque rangée de sous-unités, et la une ligne de données (36, 37) et une des lignes de grille (G1, G2, G3 ; 31, 32, 33, 34, 35) sont partagées par deux sous-unités de substrat de réseau dans chaque colonne de sous-unités,
dans chaque sous-unité de substrat de réseau, les trois pixels (R, G, B ; R1, G1, B1, R2, G2, B2, R3, G3, B3, R4, G4, B4) sont disposés dans la première direction,
dans chaque sous-unité de substrat de réseau, chaque pixel (R, G, B ; R1, G1, B1, R2, G2, B2, R3, G3, B3, R4, G4, B4) est connecté électriquement à une ligne de grille correspondante (G1, G2, G3 ; 31, 32, 33, 34, 35) et à une ligne de données correspondante (36, 37), respectivement, par le biais d'un commutateur (38, 39, 310, 311, 312),
dans lequel le commutateur (38, 39, 310, 311, 312) est un transistor à film mince (TFT), caractérisé en ce qui :

dans chaque sous-unité de substrat de réseau, la première ligne de grille (G1 ; 31, 33), les trois pixels (R, G, B ; R1, G1, B1, R2, G2, B2, R3, G3, B3, R4, G4, B4), la deuxième ligne de grille (G2 ; 32, 34) et la troisième ligne de grille (G3 ; 33, 35) sont disposées séquentiellement dans la seconde direction;
dans chaque unité de substrat de réseau, la première rangée de sous-unités et la deuxième rangée de sous-unités sont disposées séquentiellement dans la seconde direction, la troisième ligne de grille (33) pour la première rangée de sous-unités et la première ligne de grille (33) pour la deuxième rangée de sous-unités sont la même ligne de grille ;
les trois pixels (R, G, B ; R1, G1, B1, R2, G2, B2, R3, G3, B3, R4, G4, B4) sont respectivement un premier pixel (R ; R1, R2, R3, R4), un deuxième pixel (G ; G1, G2, G3, G4) et un troisième pixel (B ; B1, B2, B3, B4) ;
dans chaque sous-unité de substrat de réseau, le premier pixel (R ; R1, R2, R3, R4) est connecté électriquement à la première ligne de grille (G1 ; 31, 22), à la troisième ligne de grille (G3 ; 33, 35) et à la ligne de données (36, 37) par le biais d'un premier TFT (38) et un second TFT (39), respectivement, une électrode de grille du premier TFT (38) est connectée à la troisième ligne de grille (G3 ; 33, 35), une électrode de drain du premier TFT (38) est connectée à la première ligne de grille (G1 ; 31, 33), une électrode de source du premier TFT (38) est connectée à une électrode de grille du second TFT (39), une électrode de drain du second TFT (39) est connectée à la ligne de données (36, 37), une électrode de source du deuxième TFT (39) est connectée au premier pixel (R ; R1, R2, R3, R4) ;
le deuxième pixel (G ; G1, G2, G3, G4) est connecté électriquement à la deuxième ligne de grille (G2 ; 32, 34), à la troisième ligne de grille (G3 ; 33, 35) et à la ligne de données (36, 37) par le biais d'un troisième TFT (310) et d'un quatrième TFT (311), respectivement, une électrode de grille du troisième TFT (310) est connectée à la troisième ligne de grille (G3 ; 33, 35), une électrode de drain du troisième TFT (310) est connectée à la deuxième ligne de grille (G2 ; 32, 34), une électrode de source du troisième TFT (310) est connectée à une électrode de grille du quatrième TFT (311), une électrode de drain du quatrième TFT (311) est connectée à la ligne de données (36, 37), une électrode de source du quatrième TFT (311) est connectée au second pixel (G ; G1, G2, G3, G4) ; et
le troisième pixel (B ; B1, B2, B3, B4) est connecté électriquement à la première ligne de grille (G1 ; 31, 33) et à la ligne de données (36, 37) par le biais d'un cinquième TFT (312), une électrode de grille du cinquième TFT (312) est connectée à la première ligne de grille (G1 ; 31, 33), une électrode de drain du cinquième TFT (312) est connectée à la ligne de données (36, 37) et une électrode source du cinquième TFT (312) est connectée au troisième pixel (B ; B1, B2, B3, B4).

2. Le substrat de réseau selon la revendicationl, dans lequel une pluralité des unités de substrat de réseau sont disposées dans une matrice, et dans la seconde direction, la dernière troisième ligne de grille (33) dans une unité de substrat de réseau précédente et la première ligne de grille venant en premier dans une unité de substrat de réseau suivante sont la mê-

me ligne de grille.

3. Le substrat de réseau selon la revendication 1 ou 2, dans lequel la première direction et la seconde direction sont perpendiculaires l'une à l'autre.

4. Le substrat de réseau selon l'une quelconque des revendications 1 à 3, dans lequel les lignes de grille (G1, G2, G3 ; 31, 32, 33, 34, 35) sont configurées pour fournir des signaux d'attaque, et la ligne de données (36, 37) est configurée pour fournir des signaux de tension dont les polarités sont inversées en continu.

5. Un panneau d'affichage à cristal liquide, comprenant un substrat de filtre de couleur, un substrat de réseau et un cristal liquide interposé entre le substrat de filtre de couleur et le substrat de réseau, dans lequel le substrat de réseau est un substrat de réseau selon l'une quelconque des revendications 1 à 3.

6. Un dispositif d'affichage à cristal liquide, comprenant un rétro-éclairage, un panneau à cristal liquide et une carte de circuit intégré qui fournit des signaux de commande au panneau à cristal liquide, le panneau d'affichage à cristal liquide comprenant un substrat de filtre de couleur, un substrat de réseau et un cristal liquide interposé entre le substrat de filtre de couleur et le substrat de réseau, dans lequel le substrat de réseau est un substrat de réseau selon l'une quelconque des revendications 1 à 3.

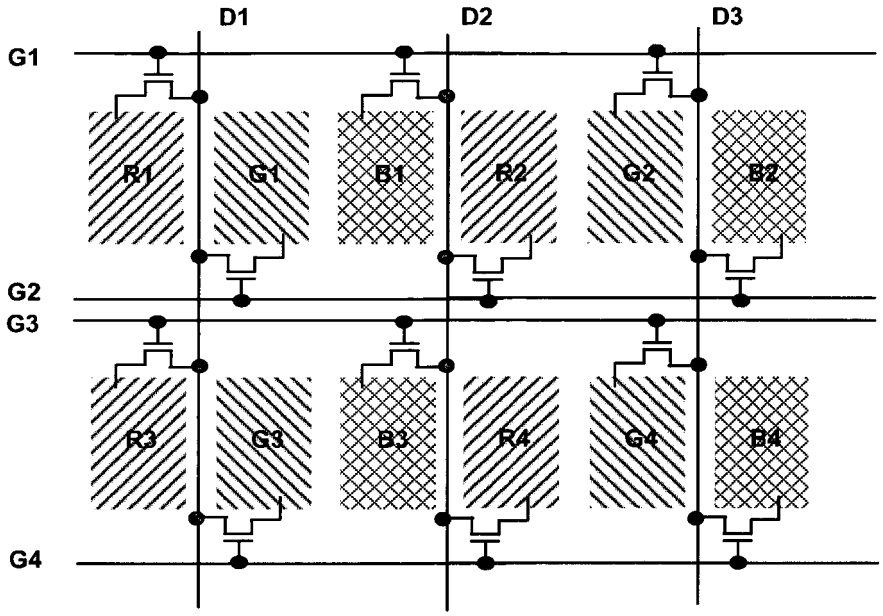

Figure 1

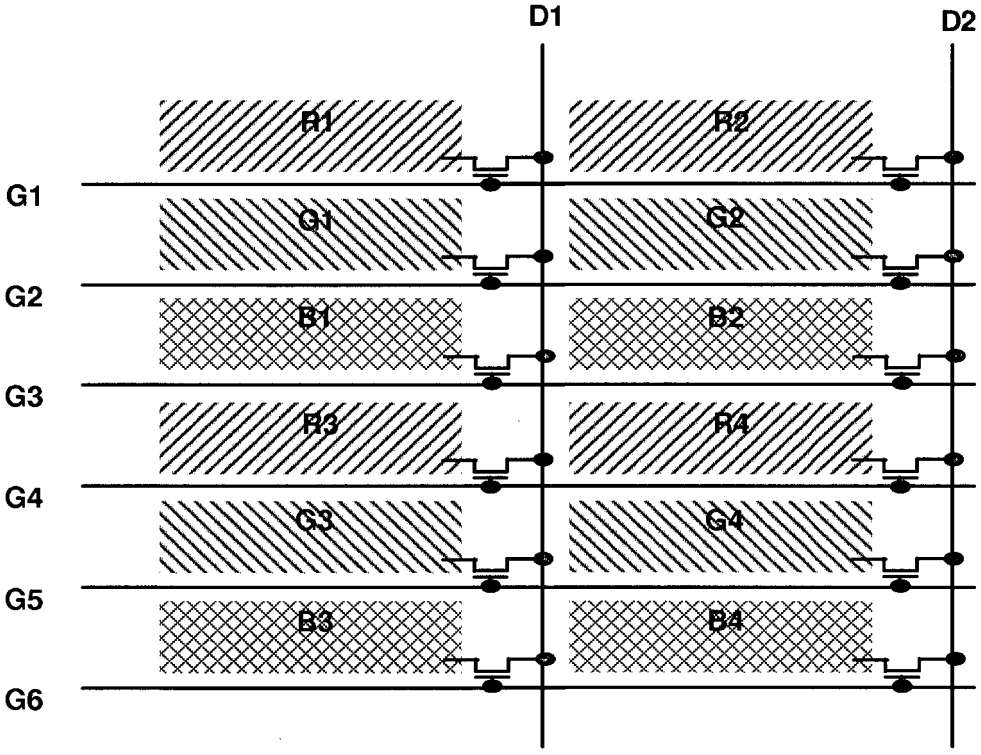

Figure 2

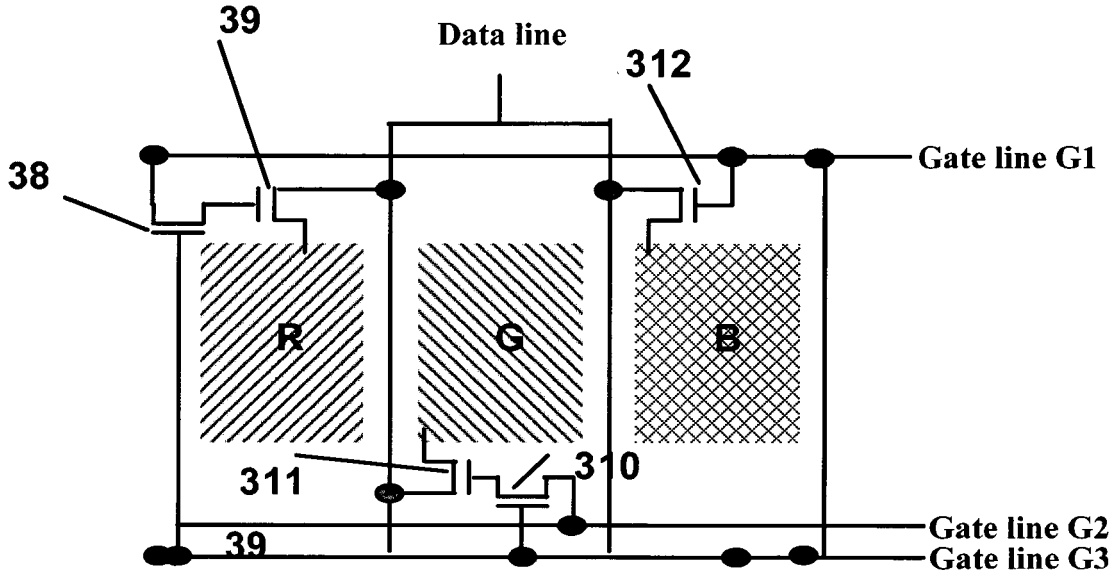

Figure 3a

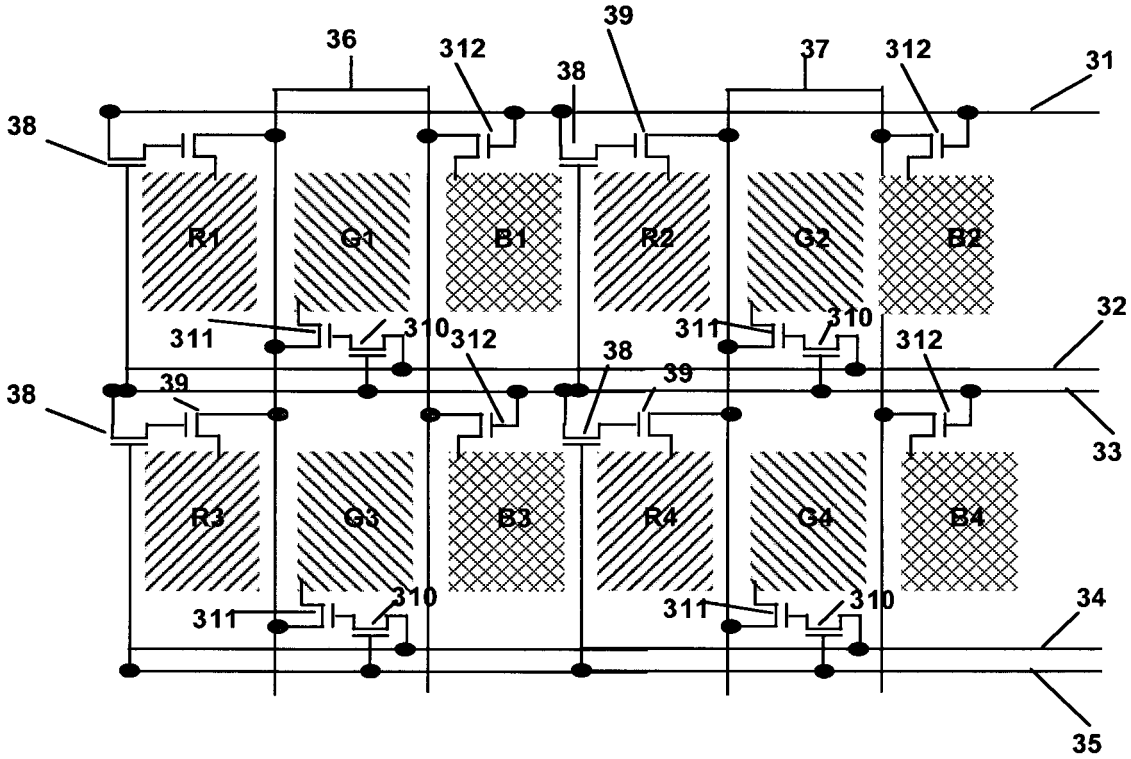

Figure 3b

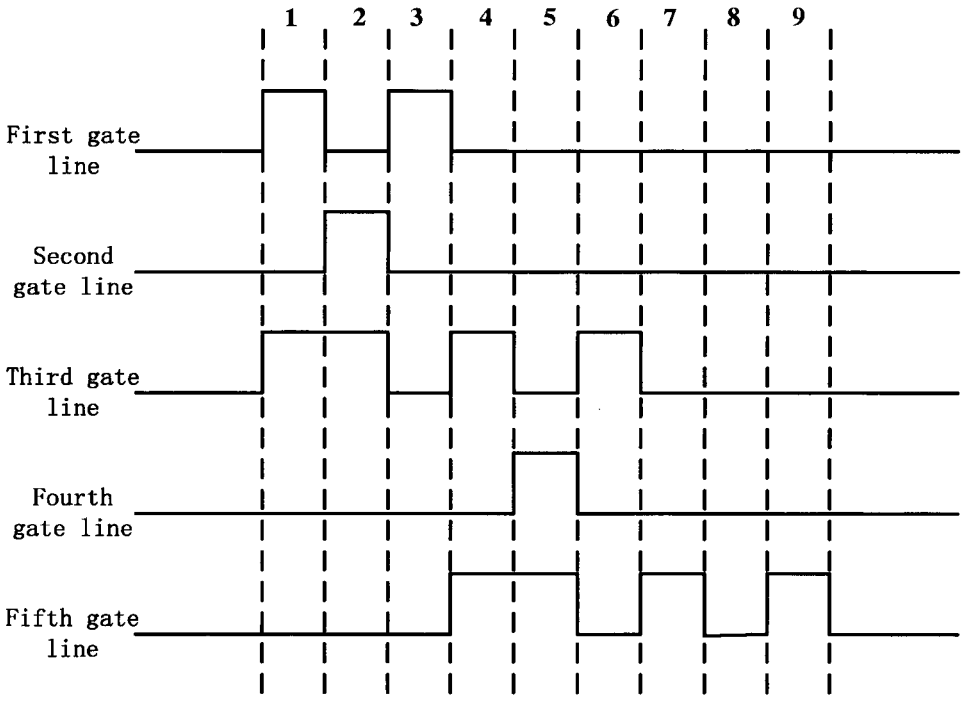
1
2
3
4
5
6
7
8
9
First gate line
Second gate line
Third gate line
Fourth gate line
Fifth gate line

Figure 4

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- US 20030189559 A1 **[0006]**

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外部链接	Espacenet		

摘要(译)

本发明实施例提供一种阵列基板，液晶显示面板和液晶显示装置。阵列基板包括多个阵列基板单元，每个阵列基板单元包括：栅极线和数据线，它们分别沿基板平面中的第一方向和第二方向彼此交叉延伸。每个阵列基板单元包括四个阵列基板子单元，所述四个阵列基板子单元沿第一方向和第二方向排列，形成子单元行和子单元列，子单元行和子单元列各有两个阵列基板子单元。三条栅极线由每个子单元行中的两个阵列基板子单元共享，并且一条数据线和一条栅极线由每个子单元列中的两个阵列基板子单元共享。

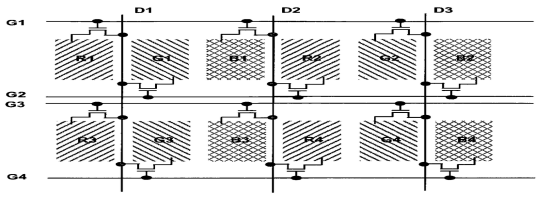

Figure 1

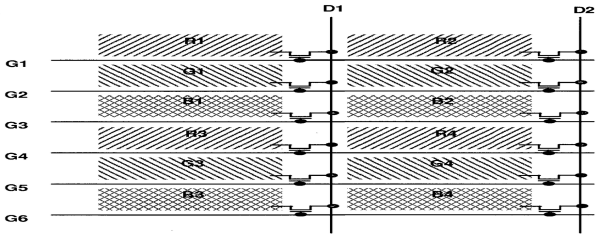

Figure 2