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(54) **Array substrate for fringe field switching mode liquid crystal display device**

Arraysubstrat für eine Flüssigkristallanzeigevorrichtung mit Fringe-Field-Switching-Modus

Substrat de réseau pour dispositif d'affichage à cristaux liquides en mode de commutation de champ de franges

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EP 2 637 060 B1

Description

[0001] The present application claims the priority benefit of Korean Patent Application No. 10-2012-0022501 filed in Republic of Korea on March 5, 2012.

BACKGROUND

FIELD OF THE DISCLOSURE

[0002] The present disclosure relates to an array substrate for a fringe field switching mode liquid crystal display device, which enables measurement of the properties of thin film transistors included in a display area of the display device.

DISCUSSION OF THE RELATED ART

[0003] In general, a liquid crystal display (LCD) device is driven using optical anisotropy and polarization of liquid crystal molecules. Since liquid crystal molecules have a thin, long molecular structure, an arrangement of the liquid crystal molecules has directivity. Thus, when an electric field is applied to the liquid crystals, the molecular arrangement direction of the liquid crystals is changed.

[0004] Accordingly, by arbitrarily adjusting the molecular arrangement direction of the liquid crystals, the molecular arrangement of the liquid crystals is changed, and light is refracted in the molecular arrangement direction of the liquid crystals to thereby display image information.

[0005] An active matrix LCD (AM-LCD, hereinafter simply referred to as an LCD) in which thin film transistors and pixel electrodes connected to the thin film transistors are arranged in a matrix form has been attracting attention due to its high resolution and excellent quality of fast moving images.

[0006] The LCD generally includes a color filter substrate in which a common electrode is formed, an array substrate in which pixel electrodes are formed, and liquid crystals filled between the color filter substrate and the array substrate. The common electrodes and the pixel electrodes drive liquid crystals by an electric field applied in an up-down direction therebetween. The LCD has an excellent light transmission rate and aperture ratio.

[0007] However, in the general LCD, liquid crystal driving by an electric field applied in the up-down direction becomes a factor for deteriorating a viewing angle property. In order to overcome this disadvantage, an in-plane switching mode LCD having an excellent viewing angle has been proposed.

[0008] JP 2009 216963 A describes a liquid crystal display device which can conduct characteristic inspection of a switching element using a test pixel, wherein at least one pixel region located in the outer edge of a plurality of pixel regions surrounded by the scanning line and the signal line constitutes the test pixel. The features of the pre-characterising portion of claim 1 are known from this document.

[0009] JP 10-339887 A describes a row or a column of test pixels having a constitution which is different from that of pixels of the display part at the outer side of the display area, which is constituted of the display elements which are two-dimensionally arranged on the active element substrate, wherein switching elements of the test pixels, which are arranged at the outer side of the display area, in this way are evaluated and analyzed as substitutive characteristics.

[0010] Hereinafter, a general in-plane switching mode LCD will be described in detail with reference to FIG. 1.

[0011] FIG. 1 is a cross-sectional view of the general in-plane switching mode LCD.

[0012] As shown in FIG. 1, an upper substrate 9 which is a color substrate is spaced apart from a lower substrate 10 which is an array substrate, and faces the lower substrate 10. A liquid crystal layer 11 is inserted between the upper and lower substrates 9 and 10.

[0013] On the lower substrate 10, a common electrode 17 and a pixel electrode 30 are formed on the same surface, and the liquid crystal layer 11 is driven by a horizontal electric field L formed by the common electrode 17 and the pixel electrode 30.

[0014] FIGS. 2A and 2B are views for explaining operations when the in-plane switching mode LCD of FIG. 1 is turned on and off, respectively.

[0015] First, referring to FIG. 2A showing an arrangement of liquid crystal molecules when a voltage is applied to the in-plane switching mode LCD, the arrangement of liquid crystal molecules 11 a positioned at locations corresponding to or directly above the common electrode 17 and the pixel electrode 30 does not change, whereas liquid crystal molecules 11b positioned between the common electrode 17 and the pixel electrode 30 are arranged by a horizontal electric field L formed by the common electrode 17 and the pixel electrode 30 in the direction of the horizontal electric field L. In other words, the in-plane switching mode LCD can achieve a wide viewing angle since the liquid crystals are moved by the horizontal electric field.

[0016] Therefore, images can be viewed even at angles of about 80° to 89° with respect to the front of the in-plane switching mode LCD, without causing image inversions.

[0017] Then, referring to FIG. 2B showing an arrangement of liquid crystal molecules when no voltage is applied to the in-plane switching mode LCD so that the in-plane switching mode LCD is turned off, since no horizontal electric field is formed between the common electrode 17 and the pixel electrode 30, the arrangement of the liquid crystal molecules 11 does not change.

[0018] The in-plane switching mode LCD, however, has a low transmission rate and aperture ratio although it can provide an improved viewing angle. In order to overcome these disadvantages of the in-plane switching mode LCD, a fringe field switching mode LCD in which liquid crystals are driven by a fringe field has been proposed.

[0019] FIG. 3 is a cross-sectional view of an array substrate 41 for a fringe field switching mode LCD according to a related art, cut along a line crossing the center portion of a pixel area of the LCD.

[0020] As shown in FIG. 3, the array substrate 41 for the fringe field switching mode LCD includes a plurality of pixel areas P, a gate line (not shown), and a data line 47, wherein the plurality of pixel areas P are defined by intersections of the upper parts and the lower parts with a gate insulating film 45 therebetween. In each pixel area, a thin film transistor Tr connected to the gate line and the data line 47 is formed. Also, in each pixel area on the gate insulating film 45, a plate-shaped pixel electrode 55 is formed to contact the drain electrode 51 of the thin film transistor Tr. The pixel electrode 55 is formed on the same layer as the data line 47, that is, on the gate insulating film 45, and is spaced a predetermined distance from the data line 47 in order to prevent a short with the data line 47.

[0021] Also, a protection layer 60 is formed on the data line 47 and the pixel electrode 55 throughout the entire display area, and a common electrode 65 is formed on the entire surface of the protection layer 60. The common electrode 65 has a plurality of bar-shaped openings oa, which are spaced a predetermined distance from each other in correspondence with the individual pixel areas.

[0022] The array substrate 41 for the fringe field switching mode LCD, as described above, should be tested to determine if each thin film transistor Tr has any defect and to check the properties of the thin film transistor Tr. However, since the common electrodes 65 are formed throughout the entire display area, it is not possible to check the properties of the thin film transistor Tr included in the pixel areas configuring the display area of the LCD. Further, it is not possible to check whether or not a corresponding gate or data line connected to a plurality of the thin film transistors Tr's is properly functioning or formed.

[0023] More specifically, in order to check the properties of the thin film transistor Tr included in each pixel area of the array substrate 41, a gate signal voltage and a data signal voltage need to be supplied to the gate electrode 43 and the source electrode 49, respectively, to drive the thin film transistor Tr, and also a signal voltage or current changing according to a data signal voltage supplied through the drain electrode 51 needs to be output.

[0024] However, in the array substrate 41 for the fringe field switching mode LCD according to the related art, as described above, since the drain electrode 51 of the thin film transistor Tr is connected to the pixel electrode 55 and the pixel electrode 55 is covered by the protection layer 60 and the common electrode 65, it is not possible to make a contact with the drain electrode 51 or with the pixel electrode 55 contacting the drain electrode 51 even when the data signal and the gate signal are respectively applied through the data line 47 and the gate line connected to the thin film transistor Tr. As a result, it is not possible to measure outputs from the thin film transistor TR formed in each pixel area P included in the display area of the LCD.

[0025] Accordingly, in the case of the array substrate 41 for the fringe field switching mode LCD according to the related art, a test for checking the properties of the thin film transistor Tr is not possible due to the structural configuration of the LCD.

SUMMARY OF THE INVENTION

[0026] Accordingly, the present invention is directed to a display device that substantially obviates one or more of the problems due to limitations and disadvantages of the related art.

[0027] An object of the present disclosure is to provide an array substrate for a fringe field switching mode liquid crystal display (LCD), which enables measurement of the properties of each thin film transistor included in a display area of the LCD.

[0028] Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0029] To achieve these and other advantages in accordance with the purpose of the present invention, as embodied and broadly described herein, provided is an array substrate for a fringe field switching mode liquid crystal display according to claim 1. Further embodiments are described in the dependent claims.

[0030] In a comparative example, an array substrate for a fringe field switching mode liquid crystal display is provided, the array substrate comprising: a display area including a plurality of pixel areas for displaying images, the pixel areas including a plurality of switch thin film transistors; and at least one non-display area surrounding in part the display area, the at least one non-display area including a row or column of test pixel areas, each of the test pixel areas including a test thin film transistor and a test electrode connected to the test thin film transistor, wherein a testing of the test pixel areas is used to detect a defect in the switch thin film transistors.

[0031] In another comparative example, a fringe field switching mode liquid crystal display is provided, comprising: an array substrate including a display area for displaying images; a color filter substrate including a color filter layer and a black matrix layer; and a liquid crystal layer between the array substrate and the color filter substrate, wherein the array substrate includes: the display area including a plurality of pixel areas for displaying the images, the pixel areas including a plurality of switch thin film transistors; and at least one non-display area surrounding in part the display area, the at least one non-display area including a row or column of test pixel

areas, each of the test pixel areas including a test thin film transistor and a test electrode connected to the test thin film transistor, and wherein a testing of the test pixel areas is used to detect a defect in the switch thin film transistors.

[0032] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0033] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention. In the drawings:

FIG. 1 is a cross-sectional view of a general in-plane switching mode liquid crystal display (LCD);

FIGS. 2A and 2B are views for explaining operations when the in-plane switching mode LCD of FIG. 1 is turned on and off, respectively;

FIG. 3 is a cross-sectional view of an array substrate for a fringe field switching mode LCD according to a related art, cut along a line crossing the center portion of a pixel area of the LCD.

FIG. 4 is a plane view of an array substrate for a fringe field switching mode LCD according to an embodiment of the present invention;

FIG. 5 is an enlarged view of an area A of FIG. 4 according to an embodiment of the present invention;

FIG. 6 is an enlarged view of an area B of FIG. 4 according to an embodiment of the present invention;

FIG. 7 is a cross-sectional view of a pixel area in a display area in the array substrate for the fringe field switching mode LCD shown in FIG. 4, cut along a line VI-VI of FIG 5;

FIG. 8 is a cross-sectional view of a pixel area for a test in the array substrate for the fringe field switching mode LCD shown in FIG. 4, cut along a line VIII-VIII of FIG 6;

FIG. 9 is a cross-sectional view of the fringe field switching mode LCD according to the embodiment of the present invention; and

FIG. 10 is a schematic view of the array substrate of the fringe field switching mode LCD including dummy pixel areas according to the embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0034] Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

[0035] FIG. 4 is a plane view of an array substrate 101 for a fringe field switching mode LCD according to an embodiment of the present invention. In FIG. 4, a display area AA for displaying images and non-display areas NA1-NA4 surrounding the display area AA are shown together. FIGS. 5 and 6 are enlarged views of an area A and an area B of FIG. 4, respectively. For convenience of description, an area in which a thin film transistor Tr, which is a switching device in each pixel area P, is formed is defined as a switching area TrA, and the non-display areas are defined as first through fourth non-display areas NA1 through NA4, wherein the first and third non-display areas NA1 and NA3 are adjacent to the left and right edges of the display area AA and the second and fourth non-display areas NA2 and NA4 are adjacent to the top and bottom edges of the display area AA of the LCD.

[0036] As shown in the drawings, the display area AA of the array substrate 101 for the fringe field switching mode LCD includes a plurality of gate lines 105 and a plurality of data lines 130. The gate lines 105 are spaced apart from each other at certain intervals and extend parallel to each other. The data lines 130 are spaced apart from each other at certain intervals and extend parallel to each other. The gate lines 105 extend in a first direction and are made of a low-resistance metal material, for example, at least one material selected among aluminum (Al), an aluminum alloy such as aluminum-neodymium (AlNd), copper (Cu), a copper alloy, molybdenum (Mo), and molybdenum titanium (MoTi). The data lines 130 are made of a low-resistance material, extend in a second direction generally or substantially perpendicular to the first direction, and cross the gate lines 105 to define a plurality of pixel areas P. For instance, the gate and data lines 105 and 130 cross each other perpendicularly to each other to form a matrix configuration in which the pixel areas P are provided.

[0037] The gate lines 105 and the data lines 130 extend to the non-display areas NA1 through NA4. One ends of the gate lines 105 are connected to a plurality of gate pad electrodes GP, respectively, and one ends of the data lines 130 are connected to a plurality of data pad electrodes DP, respectively. The gate pad electrodes GP and the data pad electrodes DP are connected to driving circuit ICs (D-ICs).

[0038] As part of an advantageous configuration of the array substrate 101 for the fringe field switching mode LCD, the first and third non-display areas NA1 and NA3 include data lines for a test, that is, first and second test data lines IDL1 and IDL2, respectively. The first and second test data lines IDL1 and IDL2 are formed parallel to the data lines 130. Also, the second and fourth non-display areas NA2 and NA4 include gate lines for a test, that is, first and second test gate lines IGLI and IGL2, respectively. Likewise, the first and second test gate lines IGLI and IGL2 are formed parallel to the gate lines 105.

[0039] The first and second test gate lines IGL1 and

IGL2 are connected to first and second test pad electrodes IP1 and IP2, respectively, and the first and second test data lines IDL1 and IDL2 are connected to third and fourth test pad electrodes IP3 and IP4, respectively.

[0040] Meanwhile, each pixel area P in the display area AA includes semiconductor layers and a switching thin film transistor STr, wherein the semiconductor layers are connected to a corresponding gate line 105 and a corresponding data line 130. The switching thin film transistor STr includes a gate electrode 107, a gate insulating film, an active layer 120a made of pure amorphous silicon, and an ohmic contact layer made of impure amorphous silicon. The switching thin film transistor STr further includes source and drain electrodes 133 and 136a spaced apart from each other. That is, at each intersection of the gate and data lines 105 and 130, the switching thin film transistor STr is provided such that a plurality of the switching thin film transistors STr are provided in parallel rows and columns in the display area AA.

[0041] Also, each pixel area P includes a plate-shaped pixel electrode 125 contacting the drain electrode 136 of the switching thin film transistor STr.

[0042] As part of the advantageous configuration of the array substrate 101 for the fringe field switching mode LCD, the non-display areas NA1, NA2, NA3, and NA4 include a plurality of test thin film transistors ITr1, ITr2, ITr3, and ITr4 formed at intersections of the first and second test gate lines IGL1 and IGL2 and the data lines 130 and at intersections of the first and second test data lines IDL1 and IDL2 and the gate lines 105. The test thin film transistors ITr1, ITr2, ITr3, and ITr4 each have the same configuration as the switching thin film transistor STr included in each pixel area P.

[0043] Particularly, a plurality of (or a column of) the test thin film transistor ITr1, ITr1, ITr1,... are provided at the intersections of the first test data line IDL1 and each of the gate lines 105. Similarly, a plurality of (or a column of) the test thin film transistors ITr3, ITr3, ITr3,... are provided at the intersections of the second test data line IDL2 and each of the gate lines 105. Further, a plurality of (or a row of) the test thin film transistors ITr2, ITr2, ITr2,... are provided at the intersections of the first test gate line IGL1 and each of the data lines 130. Similarly, a plurality of (or a row of) the test thin film transistors ITr4, ITr4, ITr4,... are provided at the intersections of the second test gate line IGL2 and each of the data lines 130. As a result, the gate electrodes of the first and third test thin film transistors ITr1 and ITr3 included in the first and third non-display areas NA1 and NA3 are respectively connected to the plurality of gate lines 105 included in the display area. The source electrodes of the second and fourth test thin film transistors ITr2 and ITr4 included in the second and fourth non-display areas NA2 and NA4 are respectively connected to the plurality of data lines 130 included in the display area.

[0044] Accordingly, in the array substrate 101 for the fringe field switching mode LCD according to the present invention, the plurality of test thin film transistors ITr each connected to a gate line 105 and a data line 130 are formed in such a manner to surround the display area AA.

[0045] That is, groups of the test thin film transistors ITr are formed at the left side of the leftmost pixel area P of each gate line 105, at the right side of the rightmost pixel area P of each gate line 105, above the top pixel area P of each data line 130, and below the bottom pixel area P of each data line 130, respectively.

[0046] All the test thin film transistors included in the first non-display area NA1 (hereinafter referred to as first test thin film transistors ITr1) are connected to the first test data line IDL1 and the third test pad electrode IP3 connected to the first test data line IDL1. All the test thin film transistors included in the second non-display area NA2 (hereinafter referred to as second test thin film transistors ITr2) are connected to the first test gate line IGL1 and the first test pad electrode IP1 connected to the first test gate line IGL1. All the test thin film transistors included in the third non-display area NA3 (hereinafter referred to as third test thin film transistors ITr3) are connected to the second test data line IDL2 and the fourth test pad electrode IP4 connected to the second test data line IDL2. All the test thin film transistors included in the fourth non-display area NA4 (hereinafter referred to as fourth test thin film transistors ITr4) are connected to the second test gate line IGL2 and the second test pad electrode IP2 connected to the second test gate line IGL2.

[0047] Meanwhile, in each pixel area P of the display area AA, a plate-shaped transparent common electrode 170, which has a plurality of bar-shaped openings op in correspondence with the pixel electrode 125, faces the pixel electrode 125 with a protection layer interposed between the pixel electrode 125 and the common electrode 170. The protection layer can be made of an insulating material.

[0048] The common electrode 170 is formed in correspondence with the pixel areas P of the display area AA, and no common electrode is formed in the non-display areas NA1 through NA4 including the test thin film transistors ITr1 through ITr4.

[0049] In the non-display areas NA1 through NA4 as shown in FIG. 6, test electrodes 175 are formed on the protection layer in correspondence with the test thin film transistors ITr1 through ITr4, and respectively connected to the drain electrodes 136b of the test thin film transistors ITr1 through ITr4. The test electrodes 175 are made of the same material as the transparent common electrode 170 and each test electrode 175 preferably has the same shape as the pixel electrode 125 included in each pixel area P.

[0050] Referring to FIG. 6, each test pixel area IPA having a test electrode 175 may have the same size and dimensions as each pixel area P included in the display area AA, and the distance between two immediately neighboring test pixel areas IPA can be the same as the distance between two immediately neighboring pixel areas p in the display area AA. Also, in the first and third non-display areas NA1 and NA3, the distance between

two immediately neighboring test pixel areas IPA (disposed in a column shape) may be the same as the distance between two immediately neighboring gate lines 105. Similarly, in the second and fourth display areas NA2 and NA4, the distance between two immediately neighboring test pixel areas IPA (disposed in a row shape) may be the same as the distance between two immediately neighboring data lines 130. As a variation, a width in a gate line direction of each test pixel area included in the first and third non-display areas can be equal to or narrower than a width in the same gate line direction of each pixel area included in the display area. Further, a width in a data line direction of the test pixel area included in the second and fourth non-display areas can be equal to or narrower than the width in the same data line direction of the pixel area included in the display area.

[0051] Meanwhile, the protective layer 160 is formed between the drain electrodes 136b of the test thin film transistors ITr1 through ITr4 and the test electrodes 175, and the drain electrode 136b of each of the test thin film transistors ITr1 through ITr4 contacts the corresponding test electrode 175 through its drain contact hole 165 exposing the corresponding drain electrode 136b.

[0052] Accordingly, due to the above-described configuration of the array substrate 101 for the fringe field switching mode LCD, all of the first test thin film transistors ITr1 included in the first non-display area NA1 are turned on by a data signal voltage supplied through the third test pad electrode IP3 and a gate signal voltage supplied through each of the gate lines 105. By contacting a probe pin to the test electrode 175 connected to the first test thin film transistor ITr1, the properties of the first test thin film transistor ITr1 and thus its test pixel area can be output and checked. Checking one test electrode 175 of the first test thin film transistor ITr1 as discussed above indicates whether or not the corresponding gate line is properly formed/functioning.

[0053] Also, all of the second test thin film transistors ITr2 included in the second non-display area NA2 are turned on by a gate signal voltage supplied through the first test pad electrode IP1 and a data signal voltage supplied through each of the data lines 130. By contacting a probe pin to a test electrode 175 connected to a second test thin film transistor ITr2, the properties of the second test thin film transistor ITr2 and thus its test pixel area can be output and checked. Checking one test electrode 175 of the second test thin film transistor ITr2 as discussed above indicates whether or not the corresponding data line is properly formed/functioning.

[0054] Likewise, all of the third and fourth test thin film transistors ITr3 and ITr4 included in the third and fourth non-display areas NA3 and NA4, respectively, are turned on by signal voltages supplied through the fourth test pad electrode IP4 and each of the gate lines 105, and through the second test pad electrode IP2 and each of the data lines 130, respectively. By contacting a probe pin to the test electrode 175 connected to the third or fourth test thin film transistor ITr3 or ITr4, the properties of the third or fourth test thin film transistor ITr3 or ITr4 and thus its test pixel area can be output and checked. Checking one test electrode 175 of the third or fourth test thin film transistor ITr3 or ITr4 as discussed above indicates whether or not the corresponding gate line or data line is properly formed/functioning.

[0055] Therefore, in the array substrate 101 for the fringe field switching mode LCD, it is possible to determine if a row or column of switching thin film transistors STrs included in the display area AA has any defect and measure the properties of the switching thin film transistors STrs when the common electrode 170 has been completely formed.

[0056] Furthermore, in the array substrate 101 for the fringe field switching mode LCD, since a plurality of test pixel areas that are used to measure and output the properties of the thin film transistors are formed adjacent to the beginning and end pixels of horizontal and vertical pixel lines connected to the gate lines 105 and the data lines 130, it is possible to check differences and distribution in pixels' output properties of the upper, lower, left, and right portions of the display area AA. Also, the results of this checking can be reflected and applied to the manufacturing process of other LCDs, which contributes to the quality improvement of the array substrate 101.

[0057] According to the present invention, referring to FIG. 10, a plurality of dummy pixel areas DPA having the same components as the pixel areas P are formed between the test pixel areas IPA and the display area AA to surround the display area AA. For instance, a dummy pixel area DPA having a certain width may be provided between each of the test pixel areas IPA and the display area AA. Such dummy pixel areas DPA include no common electrode, or only a part of the dummy pixel areas DPA includes the common electrode 170.

[0058] One reason for forming the dummy pixel areas DPA between the test pixel areas IPA and the pixel areas P is to prevent a short between the common electrode 170 and the test electrodes 175 both formed on the same layer (e.g., the protective layer 160), through the dummy pixel areas DPA. That is, by including dummy pixel areas DPA having a width greater than a predetermined fabrication tolerance range of a dummy pixel area DPA, it is possible to prevent the test electrodes 175 from contacting the common electrode 170, thereby avoiding an electric short between the test electrodes 175 and the common electrode 170 and avoiding a fabrication error. For instance, the dummy pixel area DPA can have a width of one pixel area of the display area.

[0059] Hereinafter, a cross-sectional structure of the array substrate 101 for the fringe field switching mode LCD according to an embodiment will be described.

[0060] FIG. 7 is a cross-sectional view of a pixel area in the display area AA in the array substrate 101 for the fringe field switching mode LCD shown in FIG. 4, cut along a line VI-VI of FIG 5, and FIG. 8 is a cross-sectional view of a pixel area for a test in the array substrate 101

for the fringe field switching mode LCD shown in FIG. 4, cut along a line VIII-VIII of FIG 6. For convenience of description, areas in which the switching thin film transistors STr and the test thin film transistors ITr are formed in the pixel areas P and the test pixel areas IPA, respectively, are referred to as switching areas TrA. Since each test thin film transistor ITr included in the switching areas TrA of the test pixel areas IPA has substantially the same components as each switching thin film transistor STr included in the switching areas TrA of the pixel areas P, the components of the switching thin film transistor STr and the test thin film transistor ITr are allocated the same reference numbers except for their drain electrodes. The drain electrode of the switching thin film transistor STr is denoted by 136a, and the drain electrode of the test thin film transistor ITr is denoted by 136b.

[0061] As shown in the drawings, the gate electrode 107 is formed in each switching area TrA on the transparent insulating substrate 101. The gate lines (105 of FIG. 4) in the pixel areas P and the gate electrodes 107 included in the first and third test pixel areas IPA are formed respectively in the display area AA and the first and third non-display areas (NA1 and NA3 of FIG. 4). The first and second test gate lines (IGL1 and IGL2 of FIG. 4) connected to the gate electrodes 107 included in the second and fourth test pixel areas IPA are formed in the second and fourth non-display areas (NA2 and NA4 of FIG. 4)

[0062] In an example, the gate lines (105 of FIG. 4), the first and second test gate lines (IGL1 test IGL2 of FIG. 4), and the gate electrodes 107 have a single layer structure made of a metal material having a low resistance, for example, a metal material selected from among aluminum (Al), an aluminum alloy such as aluminum-neodymium (AlNd), copper (Cu), a copper alloy, molybdenum (Mo), and molybdenum titanium (MoTi), or have a multi-layer structure made of two or more materials selected from among the above-mentioned materials. In the drawings, an example of a single layer structure is shown for the sake of brevity.

[0063] Then, the gate insulating film 110 made of a nonorganic insulating material, e.g., silicon oxide (SiO_2) or silicon nitride (SiN_x) is formed on the gate lines (105 of FIG. 4), the first and second test gate lines (IGL1 and IGL2 of FIG. 4), and the gate electrodes 107 throughout the entire area of the substrate 101.

[0064] Also, the plate-shaped pixel electrodes 125 are formed in correspondence with the pixel areas P (in correspondence with the pixel areas P and the dummy pixel areas (DPA of FIG. 10) in the case of the modified embodiment) included in the display area AA, on the gate insulating film 110. The test pixel areas IPA include no pixel electrode 125 since they include the test electrodes 175.

[0065] Then, in each switching area TrA on the gate insulating film 110, semiconductor layers 120 composed of an active layer 120a made of pure amorphous silicon and ohmic contact layers 120b made of impure amorphous silicon are formed in correspondence with each gate electrode 107. The ohmic contact layers 120b are formed on the active layer 120a and spaced apart from each other to expose the center part of the active layer 120a.

[0066] Also, in the switching area TrA, a source electrode 133 and either a drain electrode 136a or 136b are formed on the semiconductor layers 120, specifically, on the ohmic contact layers 120b spaced apart from each other, in a manner to expose the center part of the active layer 120a. In each pixel area P included in the display area AA and in each dummy pixel area of the modified example discussed above, the drain electrode 136a is formed in the corresponding switching area TrA and extends to contact the pixel electrodes 125 included in the pixel area P and the dummy pixel area.

[0067] Since no pixel electrode 125 is formed in any of the test pixel areas IPA included in the non-display areas NA1 through NA4 and since the drain electrodes 136b are provided in the test pixel areas IPA, the drain electrodes 136b of the test pixel areas IPA contact no pixel electrode 125. In the case of the drain electrode 136b included in each test pixel area IPA, a drain contact hole 165 is formed in or through the protection layer 160 covering the drain electrode 136, and the drain electrode 136b has a larger area than the drain electrode 136a included in each pixel electrode P so that the drain electrode 136b extends near the center part of the test pixel area IPA. That is, since the test pixel area IPA does not need to form images, the wide area of the drain electrode 136b does not influence an aperture ratio, etc. As shown in FIG. 8, the drain contact hole 165 for each of the test thin film transistors is formed through the protective layer 160 covering the drain electrode 136b, and exposes a portion of the drain electrode 136b. The test electrode 175 formed directly on the protective layer 160 is in contact with the drain electrode 136b through the drain contact hole 165.

[0068] Also, in the display area AA and the second and fourth non-display areas (NA2 and NA4 of FIG. 4) on the gate insulating film 110, the data lines 130 connected to the source electrodes 133 included in the pixel areas P and the second and fourth test pixel areas IPA are formed. In the first and third non-display areas (NA1 and NA3 of FIG. 4), the first and second test data lines IDL1 and IDL2 connected to the source electrodes 133 included in the first and second test pixel areas IPA are formed.

[0069] Meanwhile, in each switching area TrA, the gate electrode 107, the gate insulating film 110, the semiconductor layers 120, the source electrode 133, and the drain electrode 136a or 136b spaced apart from the source electrode 133, which have been sequentially or otherwise applied, form the thin film transistors STr and ITr.

[0070] Then, the protection layer 160 is formed on the thin film transistors STr and ITr and the pixel electrodes 125, in correspondence with the entire display area AA and the test pixel areas IPA of the non-display areas (NA1 through NA4 of FIG. 4). The protection layer 160 is made

of a nonorganic insulating material, for example, silicon oxide (SiO_2) or silicon nitride (SiN_x), or an organic insulating material, for example, benzocyclobutene (BCB) or photo acryl. The protection layer 160 may be formed as a double layer structure made of a nonorganic insulating material and an organic insulating material.

[0071] In the drawings, an example in which the protection layer 160 has a single layer structure made of an organic insulating material to form a flat surface is shown for the sake of brevity.

[0072] As part of the advantageous configuration of the array substrate 101 for the fringe field switching mode LCD according to the present invention, the drain contact hole 165 is formed in the protection layer 160, in correspondence with each test pixel area IPA, to expose the drain electrode 136b of the test thin film transistor ITr.

[0073] Then, the transparent common electrode 170 is formed in a plate form on the protection layer 160, in correspondence with the entire area of the display area AA. The common electrode 170 can be made of a transparent conductive material, for example, indium-tin-oxide (ITO) or indium-zinc-oxide (IZO). The common electrode 170 has a plurality of bar-shaped openings op in correspondence with each pixel area P included in the display area AA, and more specifically, in correspondence with each pixel electrode 125.

[0074] Also, in the non-display areas (NA1 through NA4 of FIG. 4) surrounding the display area AA, the test electrode 175 is formed on the protection layer 160 in correspondence with each test pixel area IPA. The test electrodes 175 are preferably made of the same material as the common electrode 170, and are spaced apart from the common electrode 170. Each test electrode 175 contacts the drain electrode 136b of the corresponding test thin film transistor ITr through the drain contact hole 165 formed above the drain electrode 136b. The test electrode 175 of each test pixel area IPA is electrically isolated from the test electrodes 175 of other test pixel areas IPA.

[0075] As described above, by forming the test electrodes 175 connected to the test thin film transistors ITr at the edge parts of the array substrate 101 for the fringe field switching mode LCD and applying signal voltages to the thin film transistors ITr through the test electrodes 175, signals including the properties of the thin film transistors ITr can be output and checked, thereby testing the thin film transistors ITr. The testing of all the test electrodes 175 can be performed simultaneously, selectively, independently, sequentially, in groups, or in any other manner.

[0076] Also, by forming the plurality of test pixel areas IPA that surround the display area AA, adjacent to the beginning and end parts of each of the horizontal and vertical pixel lines, it is possible to check the property distribution of the display area AA. The results of these checkings can be reflected back to the LCD manufacturing process, which then contributes to the quality improvement of the array substrate 101 according to the present invention.

[0077] The array substrate as above is attached to an opposing substrate, for example, a color filter substrate with a liquid crystal layer therebetween, so that the fringe field switching mode LCD can be manufactured. Referring to FIG. 9, a color filter substrate 201 is located over the array substrate 101 with a liquid crystal layer 250 therebetween. A black matrix layer 210 is formed on an inner surface of the color filter substrate 201 and along a peripheral portion of a pixel region P. A color filter layer is formed corresponding to the pixel area P. A planarization layer 230 may be formed on the black matrix layer 210 and the color filter layer 220.

[0078] It will be apparent to those skilled in the art that various modifications and variations can be made in a display device of the present disclosure without departing from the scope of the invention. Thus, it is intended that the present invention covers the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

Claims

1. An array substrate (101) for a fringe field switching mode liquid crystal display, the array substrate comprising:

a display area (AA) including a plurality of pixel areas (P) defined by a plurality of gate lines (105) and a plurality of data lines (130) crossing the plurality of gate lines, each pixel area including a switching thin film transistor (STr) and a plate-shaped pixel electrode (125) connected to the switching thin film transistor,
the display area of the array substrate further including a common electrode (170) having a plurality of bar-shaped openings (op) in correspondence with the pixel electrodes, the common electrode being formed over the pixel electrodes throughout an entire area of the display area; and
first through fourth non-display areas (NA1-NA4) surrounding the display area,
wherein the first through fourth non-display areas include a plurality of test pixel areas (IPA) surrounding the display area,
wherein each test pixel area includes a test thin film transistor (ITr) and a test electrode (175) connected to the corresponding test thin film transistor, **characterised in that**
each test electrode is formed on a same layer as the common electrode, is made of a same material as the common electrode, and is spaced apart from the common electrode, and
in that the array substrate further comprises dummy pixel areas (DPA) formed between each test pixel area and an adjacent pixel area located

at an edge portion of the display area, the dummy pixel area including a switching thin film transistor and a pixel electrode, wherein the dummy pixel areas include no common electrode, or only a part of the dummy pixel areas includes the common electrode.

2. The array substrate of claim 1, wherein the first through fourth non-display areas further include at least one of first and second test gate lines (IGL1, IGL2) formed parallel to the gate lines, and first and second test data lines (IDL1, IDL2) formed parallel to the data lines.

3. The array substrate of claim 2, wherein the first and third non-display areas are positioned at opposite sides of the display area and include the first and second test data lines, and
the first and second test data lines are connected to source electrodes of the plurality of test thin film transistors included in the first and third non-display areas, respectively,
wherein preferably gate electrodes of the plurality of test thin film transistors included in the first and third non-display areas are respectively connected to the plurality of gate lines included in the display area.

4. The array substrate of claim 2 or 3, wherein the second and fourth non-display areas are positioned at opposite sides of the display area, and include the first and second test gate lines, and
the first and second test gate lines are connected to gate electrodes of the plurality of test thin film transistors included in the second and fourth non-display areas, respectively,
wherein preferably source electrodes of the plurality of test thin film transistors included in the second and fourth non-display areas are respectively connected to the plurality of data lines included in the display area.

5. The array substrate of any one of claims 1 to 4, further comprising:

a plurality of test gate pad electrodes (IP1, IP2) formed in one of the first through fourth non-display areas and connected respectively to one end of the first and second test gate lines; and
a plurality of test data pad electrodes (IP3, IP4) formed in another of the first through fourth non-display areas and connected respectively to one end of the first and second test data lines.

6. The array substrate of any one of claims 1 to 5, wherein each test pixel area further includes a protection layer (160) formed on a drain electrode (136b) of the test thin film transistor included in each test pixel area,
the protection layer having a drain contact hole (165) for exposing said drain electrode of the test thin film transistor.

7. The array substrate of claim 6, wherein the test electrode in each test pixel area contacts the drain electrode of the test thin film transistor included in each test pixel area through the corresponding drain contact hole.

8. The array substrate of any one of claims 1 to 7, wherein each of the switching thin film transistors and the test thin film transistors includes a gate electrode (107), a gate insulating film (110), semiconductor layers (120), and a source electrode (133) and a drain electrode (136b) spaced apart from each other.

9. The array substrate of claim 8, wherein the pixel electrode included in the pixel area is formed on the gate insulating film, and the drain electrode of the switching thin film transistor extends to an upper surface of one end of the pixel electrode.

10. The array substrate of any one of claims 1 to 9, further comprising:

a gate pad electrode (GP) and a data pad electrode (DP) formed at one end of each gate line and each data line, respectively;
a first driving integrated circuit (D-IC) contacting the gate pad electrodes; and
a second driving integrated circuit (D-IC) contacting the data pad electrodes.

11. A fringe field switching mode liquid crystal display, comprising:

an array substrate according to any one of claims 1 to 10;
a color filter substrate (201) including a color filter layer (220) and a black matrix layer (210); and
a liquid crystal layer (250) between the array substrate and the color filter substrate.

Patentansprüche

1. Ein Matrixsubstrat (101) für eine Streufeldschalt-Modus-Flüssigkristallanzeige, das Matrixsubstrat aufweisend:

einen Anzeigebereich (AA), der eine Mehrzahl von Pixelbereichen (P) aufweist, die mittels einer Mehrzahl von Gate-Leitungen (105) und einer Mehrzahl von Datenleitungen (130), die die Mehrzahl von Gate-Leitungen überkreuzen, definiert sind, wobei jeder Pixelbereich einen

Schalt-Dünnschichttransistor (STr) und eine plattenförmige Pixelelektrode (125), die mit dem Schalt-Dünnschichttransistor verbunden ist, aufweist,
der Anzeigebereich des Matrixsubstrats ferner aufweisend eine gemeinsame Elektrode (170), die eine Mehrzahl von streifenförmigen Öffnungen (op) in Übereinstimmung mit den Pixelelektroden aufweist, wobei die gemeinsame Elektrode über eine gesamte Fläche des Anzeigebereichs hinweg über den Pixelelektroden gebildet ist; und
einen ersten Nicht-Anzeigebereich (NA1) bis vierten Nicht-Anzeigebereich (NA4), die den Anzeigebereich umgeben, wobei der erste Nicht-Anzeigebereich bis vierte Nicht-Anzeigebereich eine Mehrzahl von den Anzeigebereich umgebenden Test-Pixelbereichen (IPA) aufweist,
wobei jeder Test-Pixelbereich einen Test-Dünnschichttransistor (ITr) und eine mit dem entsprechenden Test-Dünnschichttransistor verbundene Testelektrode (175) aufweist, **dadurch gekennzeichnet, dass**
jede Testelektrode auf derselben Schicht wie die gemeinsame Elektrode gebildet ist, aus demselben Material wie die gemeinsame Elektrode gebildet ist, und von der gemeinsamen Elektrode entfernt angeordnet ist, und dass
das Matrixsubstrat ferner aufweist
Dummy-Pixelbereiche (DPA), die zwischen jedem Test-Pixelbereich und einem benachbarten Pixelbereich, der an einem Randbereich des Anzeigebereichs angeordnet ist, gebildet ist, wobei der Dummy-Pixelbereich einen Schalt-Dünnschichttransistor und eine Pixelelektrode aufweist, wobei die Dummy-Pixelbereiche keine gemeinsame Elektrode aufweisen oder nur ein Teil der Dummy-Pixelbereiche die gemeinsame Elektrode aufweist.

2. Matrixsubstrat gemäß Anspruch 1, wobei der erste Nicht-Anzeigebereich bis vierte Nicht-Anzeigebereich ferner mindestens eines von einer ersten Test-Gate-Leitung (IGL1) und einer zweiten Test-Gate-Leitung (IGL2), die parallel zu den Gate-Leitungen gebildet sind, und einer ersten Test-Datenleitung (IDL1) und einer zweiten Test-Datenleitung (IDL2), die parallel zu den Datenleitungen gebildet sind, aufweist.

3. Matrixsubstrat gemäß Anspruch 2, wobei der erste Nicht-Anzeigebereich und der dritte Nicht-Anzeigebereich auf einander gegenüberliegenden Seiten des Anzeigebereichs angeordnet sind und die erste Test-Datenleitung und zweite Test-Datenleitung aufweisen, und
die erste Test-Datenleitung und zweite Test-Datenleitung mit den Source-Elektroden der Mehrzahl von Test-Dünnschichttransistoren, die in dem ersten Nicht-Anzeigebereich bzw. dem dritten Nicht-Anzeigebereich angeordnet sind, verbunden sind,
wobei vorzugsweise Gate-Elektroden der Mehrzahl von Test-Dünnschichttransistoren, die in dem ersten Nicht-Anzeigebereich und dem dritten Nicht-Anzeigebereich enthalten sind, jeweils mit der Mehrzahl von in dem Anzeigebereich angeordneten Gate-Leitungen verbunden sind.

4. Matrixsubstrat gemäß Anspruch 2 oder 3, wobei der zweite Nicht-Anzeigebereich und der vierte Nicht-Anzeigebereich auf einander gegenüberliegenden Seiten des Anzeigebereichs angeordnet sind und die erste Test-Gate-Leitung und zweite Test-Gate-Leitung aufweisen, und
die erste Test-Gate-Leitung und zweite Test-Gate-Leitung mit den Gate-Elektroden der Mehrzahl von Test-Dünnschichttransistoren, die in dem zweiten Nicht-Anzeigebereich bzw. dem vierten Nicht-Anzeigebereich angeordnet sind, verbunden sind,
wobei vorzugsweise Source-Elektroden der Mehrzahl von Test-Dünnschichttransistoren, die in dem zweiten Nicht-Anzeigebereich und dem vierten Nicht-Anzeigebereich enthalten sind, jeweils mit der Mehrzahl von in dem Anzeigebereich angeordneten Datenleitungen verbunden sind.

5. Matrixsubstrat gemäß einem der Ansprüche 1 bis 4, ferner aufweisend:

eine Mehrzahl von Test-Gate-Pad-Elektroden (IP1, IP2), die in einem von dem ersten Nicht-Anzeigebereich bis vierten Nicht-Anzeigebereich gebildet sind und jeweils mit einem Ende der ersten Test-Gate-Leitung und der zweiten Test-Gate-Leitung verbunden sind; und
eine Mehrzahl von Test-Daten-Pad-Elektroden (IP3, IP4), die in einem anderen von dem ersten Nicht-Anzeigebereich bis vierten Nicht-Anzeigebereich gebildet sind und jeweils mit einem Ende der ersten Test-Datenleitung und der zweiten Test-Datenleitung verbunden sind.

6. Matrixsubstrat gemäß einem der Ansprüche 1 bis 5, wobei jeder Test-Pixelbereich ferner eine Schutzschicht (160) aufweist, die auf einer Drain-Elektrode (136b) des in jedem Test-Pixelbereich enthaltenen Test-Dünnschichttransistors gebildet ist,
wobei die Schutzschicht ein Drain-Kontaktloch (165) zum Freilegen der genannten Drain-Elektrode des Test-Dünnschichttransistors aufweist.

7. Matrixsubstrat gemäß Anspruch 6, wobei die Test-Elektrode in jedem Test-Pixelbereich die Drain-Elektrode des in jedem Test-Pixelbereich angeordneten Test-Dünnschichttransistors durch das entsprechende Drain-Kontaktloch hindurch kontaktiert.

8. Matrixsubstrat gemäß einem der Ansprüche 1 bis 7, wobei jeder der Schalt-Dünnschichttransistoren und der Test-Dünnschichttransistoren eine Gate-Elektrode (107), eine Gateisolierende Schicht (110), Halbleiterschichten (120) und eine Source-Elektrode (133) und eine Drain-Elektrode (136b), die voneinander beabstandet sind, aufweist.

9. Matrixsubstrat gemäß Anspruch 8, wobei die in dem Pixelbereich angeordnete Pixelelektrode auf der Gateisolierenden Schicht gebildet ist, und die Drain-Elektrode des Schalt-Dünnschichttransistors sich zu einer oberen Oberfläche eines Endes der Pixelelektrode erstreckt.

10. Matrixsubstrat gemäß einem der Ansprüche 1 bis 9, ferner aufweisend:

eine Gate-Pad-Elektrode (GP) und eine Daten-Pad-Elektrode (DP), die an einem Ende jeder Gate-Leitung bzw. jeder Datenleitung gebildet sind;
ein erster Steuerungs-Integrierter-Schaltkreis (D-IC), der die Gate-Pad-Elektroden kontaktiert; und
ein zweiter Steuerungs-Integrierter Schaltkreis (D-IC), der die Daten-Pad-Elektroden kontaktiert.

11. Eine Streufeldschalt-Modus-Flüssigkristallanzeige, aufweisend:

ein Matrixsubstrat gemäß einem der Ansprüche 1 bis 10;
ein Farbfiltersubtrat (201), das eine Farbfilterschicht (220) und eine Schwarzmatrix-Schicht (210) aufweist; und
eine Flüssigkristallschicht (250) zwischen dem Matrixsubstrat und dem Farbfiltersubstrat.

Revendications

1. Substrat de réseau (101) pour un afficheur à cristaux liquides à mode de commutation de champ de franges, le substrat de réseau comprenant :

une zone d'affichage (AA) comprenant une pluralité de zones de pixel (P) définies par une pluralité de lignes de grille (105) et une pluralité de lignes de données (130) croisant la pluralité de lignes de grille, chaque zone de pixel comprenant un transistor à couches minces de commutation (STr) et une électrode de pixel en forme de plaque (125) connectée au transistor à couches minces de commutation,
la zone d'affichage du substrat de réseau comprenant en outre une électrode commune (170) comportant une pluralité d'ouvertures en forme de barre (op) en correspondance avec les électrodes de pixel, l'électrode commune étant formée sur les électrodes de pixel dans une zone entière de la zone d'affichage ; et
des première à quatrième zones de non affichage (NA1 à NA4) entourant la zone d'affichage,
dans lequel les première à quatrième zones de non affichage comprennent une pluralité de zones de pixel de test (IPA) entourant la zone d'affichage,
dans lequel chaque zone de pixel de test comprend un transistor à couches minces de test (ITr) et une électrode de test (175) connectée au transistor à couches minces de test correspondant, **caractérisé en ce que**
chaque électrode de test est formée sur une même couche que l'électrode commune, est réalisée en un même matériau que l'électrode commune, et est espacée de l'électrode commune, et
en ce que le substrat de réseau comprend en outre des zones de pixel fictif (DPA) formées entre chaque zone de pixel de test et une zone de pixel adjacente située au niveau d'une partie de bord de la zone d'affichage, la zone de pixel fictif comprenant un transistor à couches minces de commutation et une électrode de pixel, dans lequel les zones de pixel fictif ne comprennent pas d'électrode commune, ou seulement une partie des zones de pixel fictif comprennent l'électrode commune.

2. Substrat de réseau selon la revendication 1, dans lequel les première à quatrième zones de non affichage comprennent en outre au moins l'une de première et deuxième lignes de grille de test (IGL1, IGL2) formée parallèlement aux lignes de grille, et des première et deuxième lignes de données de test (IDL1, IDL2) formées parallèlement aux lignes de données.

3. Substrat de réseau selon la revendication 2, dans lequel les première et troisième zones de non affichage sont positionnées sur des côtés opposés de la zone d'affichage et comprennent les première et deuxième lignes de données de test, et
les première et deuxième lignes de données de test sont connectées aux électrodes de source de la pluralité de transistors à couches minces de test inclus dans les première et troisième zones de non affichage, respectivement,
dans lequel, de préférence, les électrodes de grille de la pluralité de transistors à couches minces de test inclus dans les première et troisième zones de non affichage sont respectivement connectées à la pluralité de lignes de grille incluses dans la zone d'affichage.

4. Substrat de réseau selon la revendication 2 ou 3, dans lequel les deuxième et quatrième zones de non affichage sont positionnées sur des côtés opposés de la zone d'affichage, et comprennent les première et deuxième lignes de grille de test, et
les première et deuxième lignes de grille de test sont connectées aux électrodes de grille de la pluralité de transistors à couches minces de test inclus dans les deuxième et quatrième zones de non affichage, respectivement,
dans lequel, de préférence, les électrodes de source de la pluralité de transistors à couches minces de test inclus dans les deuxième et quatrième zones de non affichage sont respectivement connectées à la pluralité de lignes de données incluses dans la zone d'affichage.

5. Substrat de réseau selon l'une quelconque des revendications 1 à 4, comprenant en outre :

une pluralité d'électrodes de pastilles de grille de test (IP1, IP2) formées dans l'une des première à quatrième zones de non affichage et respectivement connectées à une extrémité des première et deuxième lignes de grille de test ;
une pluralité d'électrodes de pastilles de données de test (IP3, IP4) formées dans une autre des première à quatrième zones de non affichage et respectivement connectées à une extrémité des première et deuxième lignes de données de test.

6. Substrat de réseau selon l'une quelconque des revendications 1 à 5, dans lequel chaque zone de pixel de test comprend en outre une couche de protection (160) formée sur une électrode de drain (136b) du transistor à couches minces de test inclus dans chaque zone de pixel de test,
la couche de protection comportant un trou de contact de drain (165) pour exposer ladite électrode de drain du transistor à couches minces de test.

7. Substrat de réseau selon la revendication 6, dans lequel l'électrode de test dans chaque zone de pixel de test est en contact avec l'électrode de drain du transistor à couches minces de test inclus dans chaque zone de pixel de test à travers le trou de contact de drain correspondant.

8. Substrat de réseau selon l'une quelconque des revendications 1 à 7, dans lequel chacun des transistors à couches minces de commutation et des transistors à couches minces de test comprend une électrode de grille (107), un film isolant de grille (110), des couches semi-conductrices (120) et une électrode de source (133) et une électrode de drain (136b) espacées l'une de l'autre.

9. Substrat de réseau selon la revendication 8, dans lequel l'électrode de pixel incluse dans la zone de pixel est formée sur le film isolant de grille, et l'électrode de drain du transistor à couches minces de commutation s'étend vers une surface supérieure d'une extrémité de l'électrode de pixel.

10. Substrat de réseau selon l'une quelconque des revendications 1 à 9, comprenant en outre :

une électrode de pastille de grille (GP) et une électrode de pastille de données (DP) formées à une extrémité de chaque ligne de grille et de chaque ligne de données, respectivement ;
un premier circuit intégré de commande (D-IC) en contact avec les électrodes de pastilles de grille ; et
un deuxième circuit intégré de commande (D-IC) en contact avec les électrodes de pastilles de données.

11. Afficheur à cristaux liquides à mode de commutation de champ de franges, comprenant :

un substrat de réseau selon l'une quelconque des revendications 1 à 10 ;
un substrat de filtre coloré (201) comprenant une couche de filtre coloré (220) et une couche de matrice noire (210) ; et
une couche de cristal liquide (250) entre le substrat de réseau et le substrat de filtre coloré.

FIG. 1
Related Art

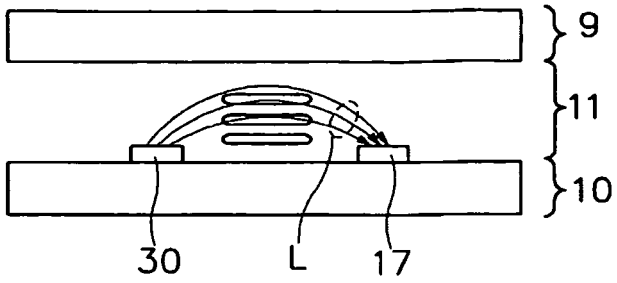


FIG. 2A
Related Art

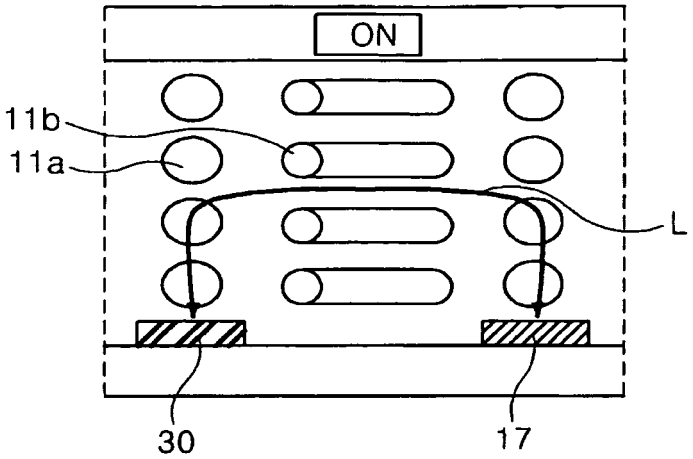


FIG. 2B
Related Art

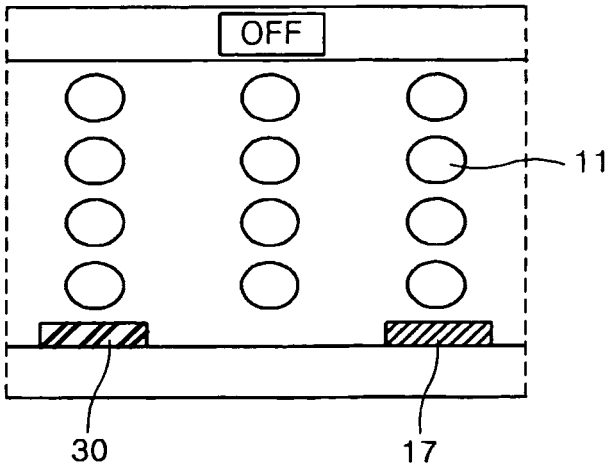


FIG. 3
Related Art

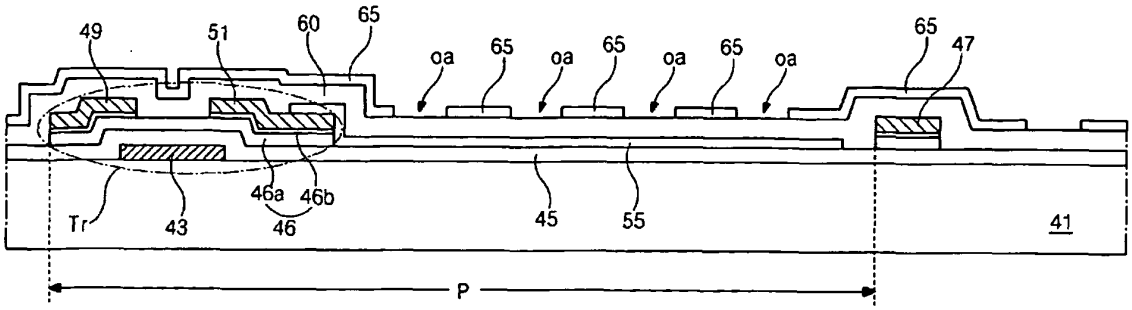


FIG. 4

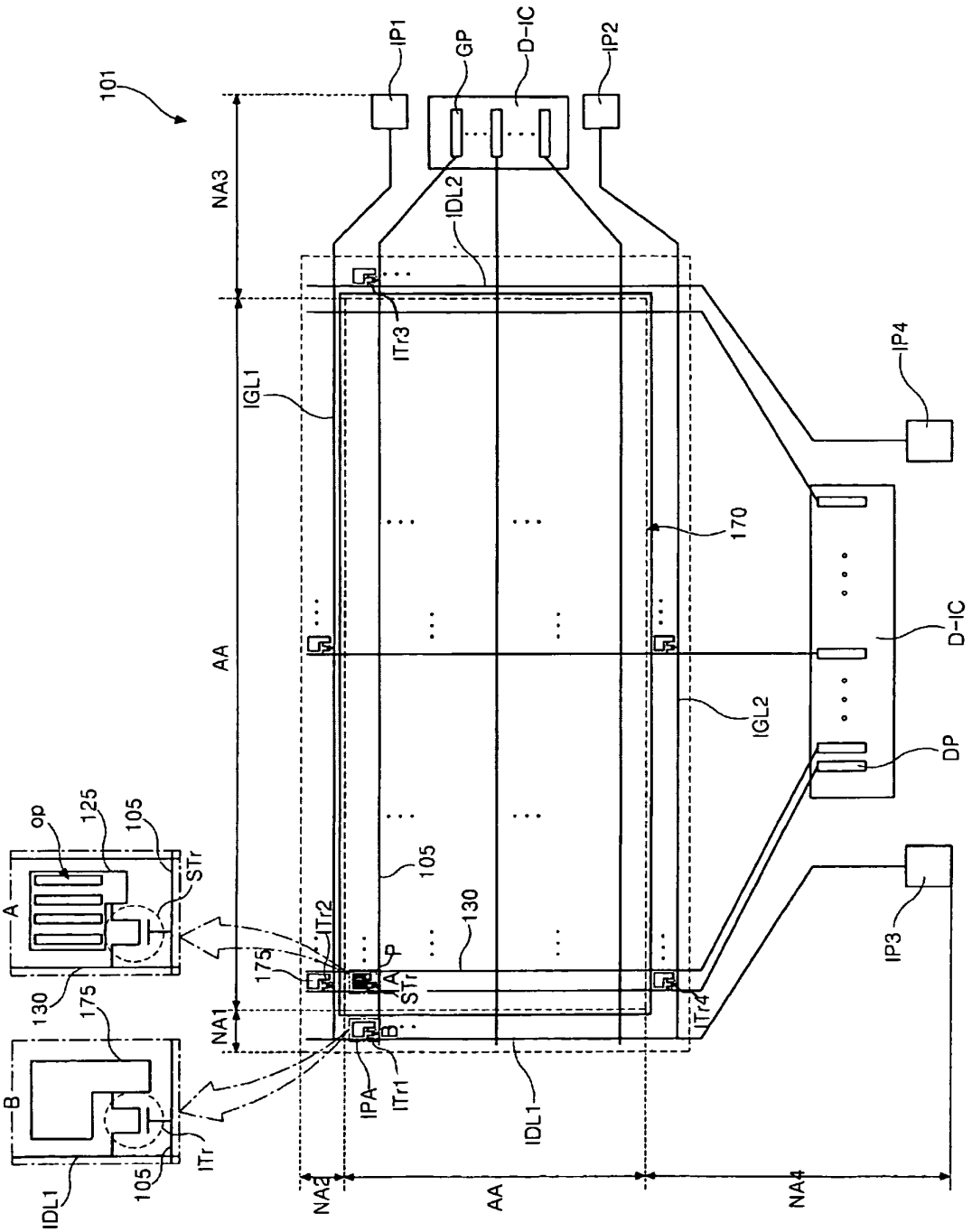

101
IP1
GP
D-IC
IP2
NA3
IDL2
ITr3
IGL1
IP4
170
AA
D-IC
IGL2
DP
op
125
105
STr
A
ITr2
105
130
175
P
A
STr
130
175
NA1
B
ITr4
IP3
B
IPA
ITr1
IDL1
ITr
105
IDL1
NA2
AA
NA4

FIG. 5

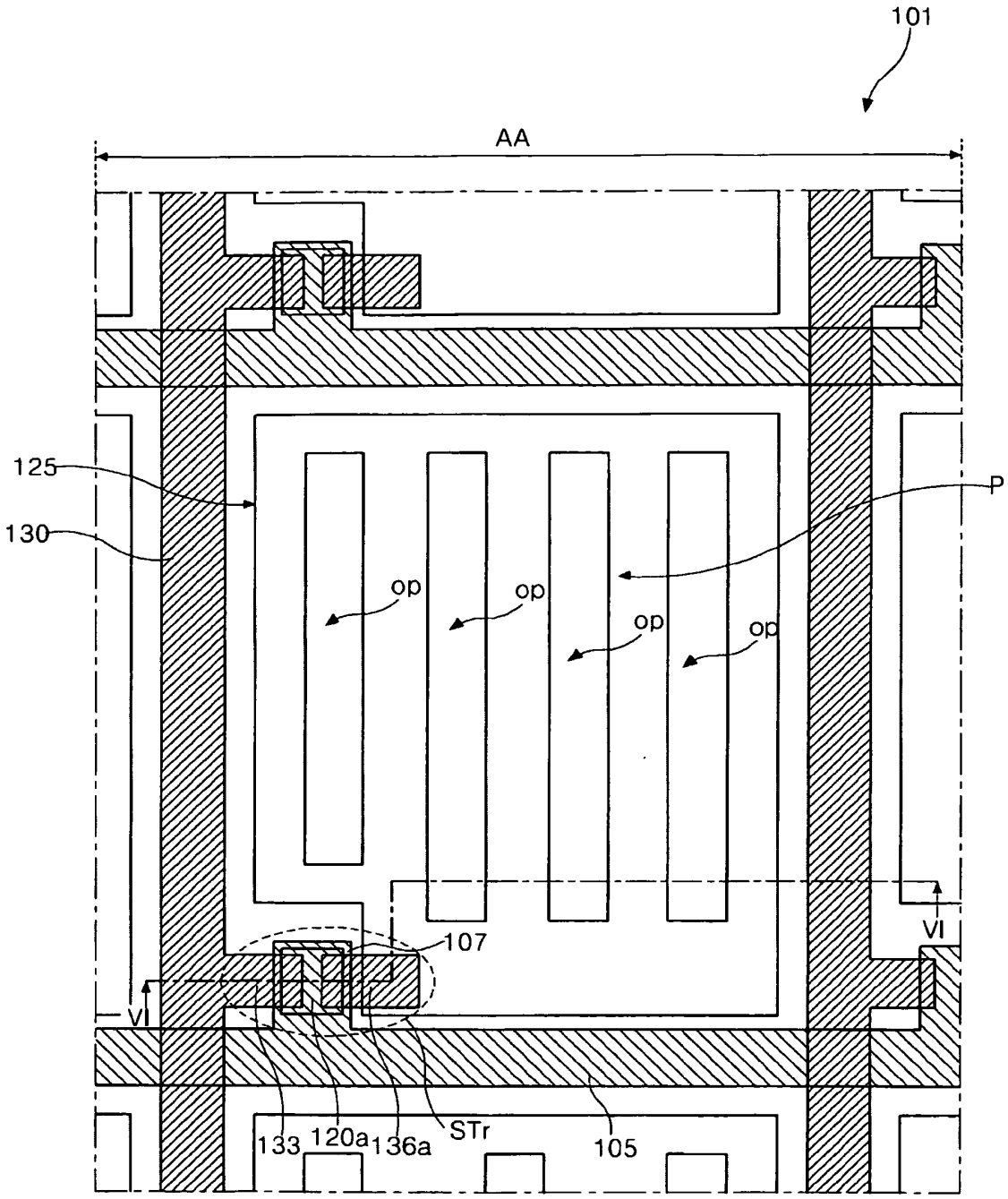


FIG. 6

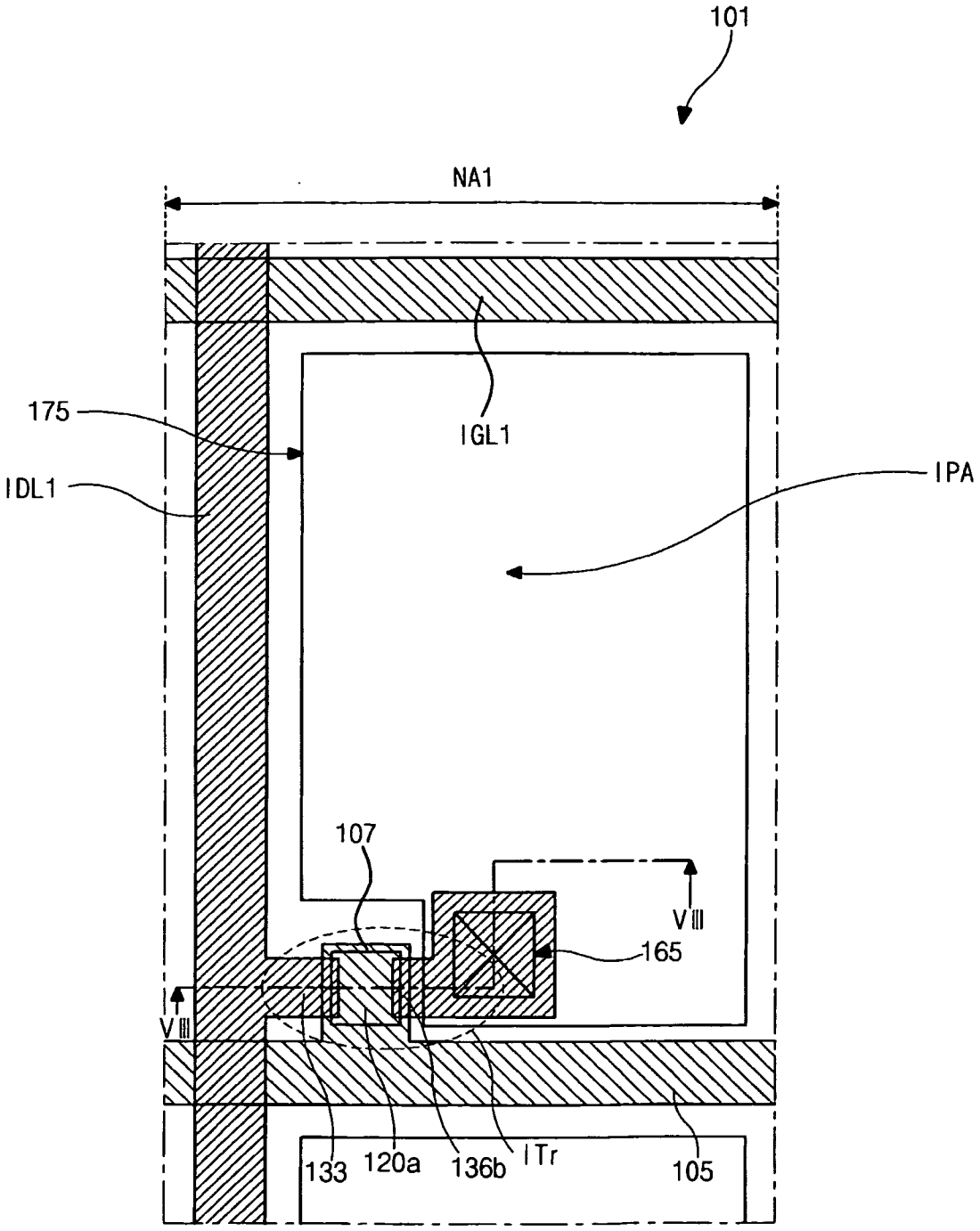

101
NA1
175
IGL1
IDL1
IPA
107
VIII
165
VIII
133
120a
136b
ITr
105

FIG. 7

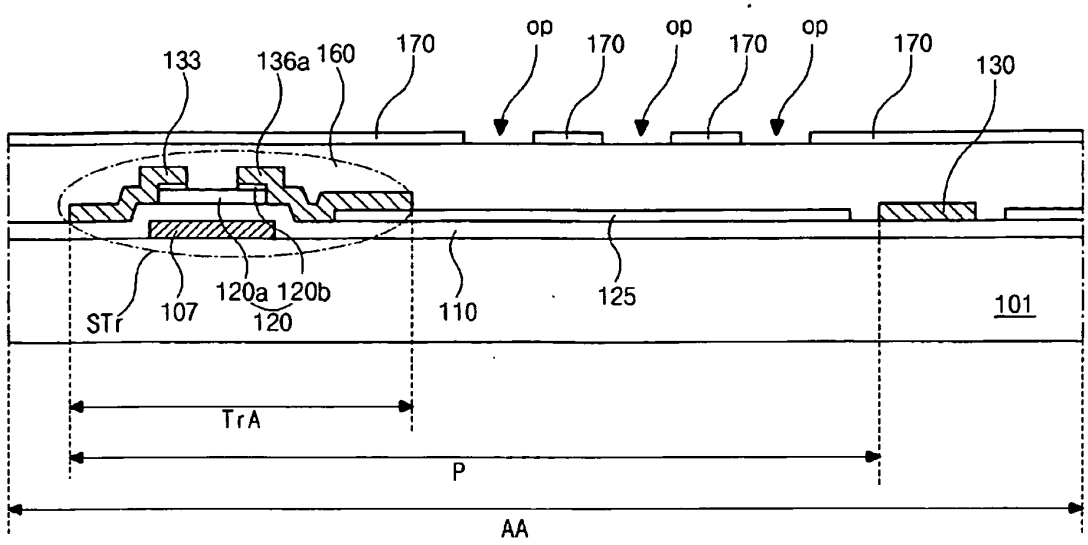

133
136a
160
170
op
170
op
170
op
170
130
STr
107
120a
120b
120
110
125
101
TrA
P
AA

FIG. 8

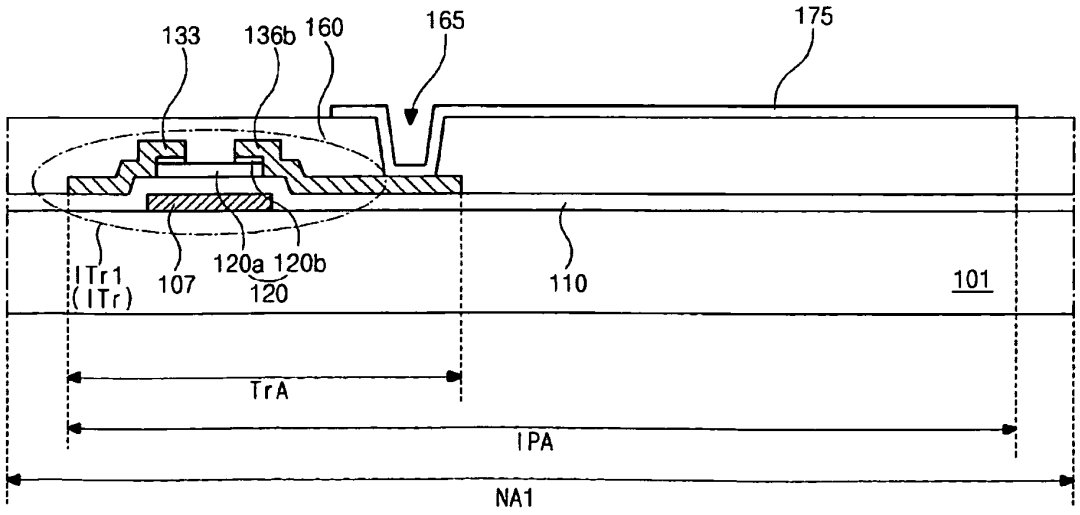

133
136b
160
165
175
ITr1
(ITr)
107
120a
120b
120
110
101
TrA
IPA
NA1

FIG. 9

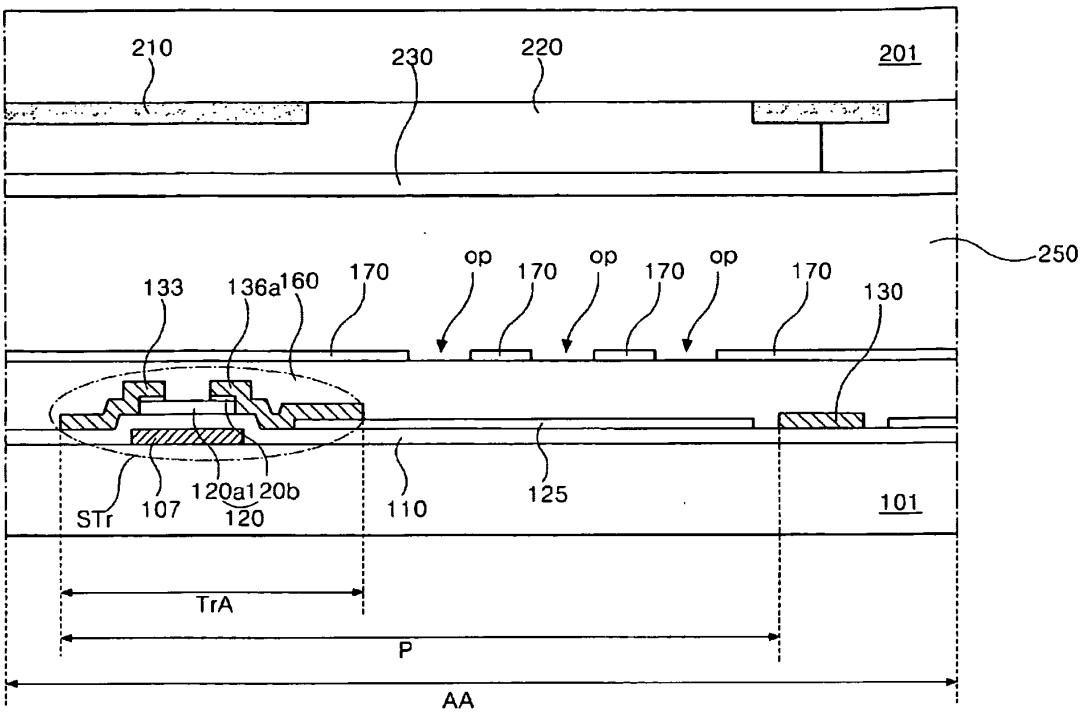
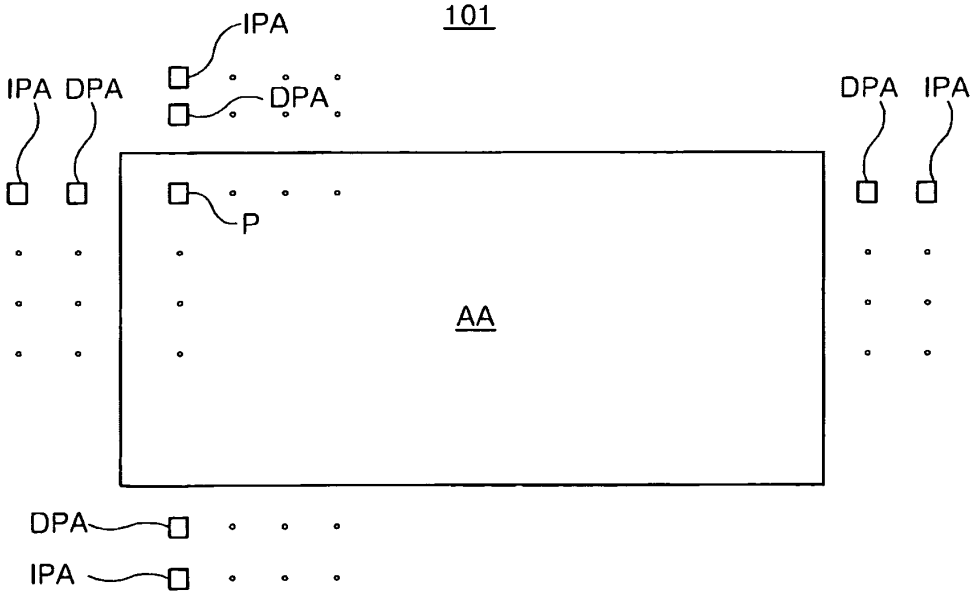

210
230
220
201
250
133
136a
160
170
op
170
op
170
op
170
130
STr
107
120a
120b
120
110
125
101
TrA
P
AA

FIG. 10


101
IPA
IPA
DPA
DPA
DPA
IPA
P
AA
DPA
IPA

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- KR 1020120022501 **[0001]**
- JP 2009216963 A **[0008]**
- JP 10339887 A **[0009]**

专利名称(译)	用于边缘场切换模式液晶显示装置的阵列基板		
公开(公告)号	EP2637060B1	公开(公告)日	2015-09-16
申请号	EP2012199324	申请日	2012-12-24
[标]申请(专利权)人(译)	乐金显示有限公司		
申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
当前申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
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发明人	WON, DAE-HYUN SHIN, CHANG-YEOP SHIN, AE-KYUNG LEE, RU-DA		
IPC分类号	G02F1/1368 G02F1/1343		
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优先权	1020120022501 2012-03-05 KR		
其他公开文献	EP2637060A1		
外部链接	Espacenet		

摘要(译)

公开了一种用于边缘场切换模式液晶显示器的阵列基板和显示器。阵列基板（101）包括显示区域（AA），其包括由栅极线和与栅极线交叉的数据线限定的像素区域（P），每个像素区域（P）包括开关薄膜晶体管（STr）和板 - 形状像素电极（125）连接到开关薄膜晶体管（STr），显示器的显示区域还包括公共电极（170），公共电极（170）具有与像素电极（125）对应的多个条形开口（op）。 ），在显示区域（AA）的整个区域上，在像素电极（125）上形成公共电极（170）;第一至第四非显示区域（NA1-NA4）围绕显示区域并包括显示区域周围的测试像素区域（IPA），其中每个测试像素区域（IPA）包括测试薄膜晶体管（ITr）和测试电极（175）由与公共电极（170）相同的层形成并连接到相应的测试薄膜晶体管（ITr）。