(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 2 482 125 B1

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
20.11.2013 Bulletin 2013/47

(21) Application number: **11183643.3**

(22) Date of filing: **30.09.2011**

(51) Int Cl.:
G02F 1/1343 *(2006.01)* ***G02F 1/139*** *(2006.01)*

(54) **Liquid crystal display**

Flüssigkristallanzeige

Écran à cristaux liquides

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR

(30) Priority: **28.01.2011 KR 20110008627**

(43) Date of publication of application:
01.08.2012 Bulletin 2012/31

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EP 2 482 125 B1

Printed by Jouve, 75001 PARIS (FR)

Description

BACKGROUND OF THE INVENTION

(a) Field of the Invention

[0001] Exemplary embodiments of the present invention relate to a liquid crystal display.

(b) Description of the Related Art

[0002] A liquid crystal display (hereinafter referred to as an "LCD") is one of the most widely used type of flat panel displays. The LCD includes two display panels provided with electric field generating electrodes, such as pixel electrodes and a common electrode, respectively, and a liquid crystal layer interposed between the two display panels. In the LCD, voltages are applied to the electric field generating electrodes to generate an electric field in the liquid crystal layer. Due to the generated electric field, liquid crystal molecules of the liquid crystal layer are aligned and polarization of incident light is controlled, thereby displaying images.

[0003] In general, it may be necessary to realize a liquid crystal display having a high contrast ratio, excellent viewing angle, and fast response speed to improve the display quality of the liquid crystal display.

[0004] Also, when the pixel electrode and the signal line overlap each other to increase the aperture ratio of the liquid crystal display, a parasitic capacitance between the signal line and the pixel electrode increases such that display quality may be deteriorated by crosstalk.

[0005] Liquid crystal displays having pixels with two switching elements, receiving first and second data voltages are known from US 2009/0310047 A1 and US 2007/0182902 A1.

BRIEF SUMMARY OF THE INVENTION

[0006] Exemplary embodiments of the present invention provide a liquid crystal display with a high contrast ratio and a wide viewing angle of the liquid crystal display, with increased response speed of liquid crystal molecules, and which prevents crosstalk caused by an parasitic capacitance between a signal line and a pixel electrode while having a high aperture ratio, thereby improving display characteristics.

[0007] According to exemplary embodiments, a liquid crystal display includes the features of appended claim 1.

[0008] In an exemplary embodiment, the first stem of the first pixel electrode and the fourth stem of the second pixel electrode may together cover at least two thirds of the area of the voltage transmitting line.

[0009] In an exemplary embodiment, the liquid crystal display may further include a plurality of pixels, where each of the plurality of pixels includes the first pixel electrode and the second pixel electrode, and the voltage transmitting line is arranged to supply the second voltage to three of the plurality of pixels.

[0010] In an exemplary embodiment, the liquid crystal display may further include a first region where the branches of the first pixel electrode and adjacent branches of the second pixel electrode are separated by a first interval, and a second region where the branches of the first pixel electrode and the adjacent branches of the second pixel electrode are separated by a second interval, where the first interval is greater than the second interval, and the first region includes a region where the stems of the first pixel electrode and the second pixel electrode are not disposed at an edge of a pixel area.

[0011] In an exemplary embodiment, the liquid crystal layer may be vertically aligned.

[0012] In an exemplary embodiment, the first pixel electrode and the second pixel electrode may be applied with voltages having different polarities.

[0013] In an exemplary embodiment, the liquid crystal display may further include a third region where the branches of the first pixel electrode and the adjacent branches of the second pixel electrode are separated by a third interval, where the third interval is greater than the first interval.

[0014] According to exemplary embodiments of the present invention, a high contrast ratio and a wide viewing angle of the liquid crystal display may be simultaneously ensured, the response speed of the liquid crystal molecule and the aperture ratio may be improved, and simultaneously crosstalk due to an increase of the parasitic capacitance between the signal line and the pixel electrode may be effectively prevented, and display characteristics is thereby substantially improved.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] The above and other aspects, advantages and features of the invention will become more apparent by describing in further detail exemplary embodiments thereof with reference to the accompanying drawings, in which:

FIG. 1 is a block diagram showing an exemplary embodiment of a liquid crystal display according to the present invention;

FIG. 2 is an equivalent circuit diagram showing a structure of an exemplary embodiment of the liquid crystal display and one pixel according to the present invention;

FIG. 3 is an equivalent circuit diagram showing a plurality of adjacent pixels of an exemplary embodiment of a liquid crystal display according to the present invention;

FIG. 4 is a cross-sectional view of an exemplary embodiment of the liquid crystal display according to the present invention;

FIG. 5 is a signal timing diagram of signals applied to a pixel of the liquid crystal display shown in FIG. 3;

FIG. 6 is a top plan view of an exemplary embodiment

of a liquid crystal display according to the present invention;

FIG. 7 is a cross-sectional view of an exemplary embodiment of the liquid crystal panel assembly of FIG. 6 taken along line VII-VII;

FIG. 8A to FIG. 8C are partial top plan views of an exemplary embodiment of a liquid crystal display according to the present invention;

FIG. 9 is a graph of grayscale measurement results showing display quality of an exemplary embodiment of the liquid crystal display; and

FIG. 10 is a graph of grayscale measurement results showing display quality of an exemplary embodiment of the liquid crystal display.

DETAILED DESCRIPTION OF THE INVENTION

[0016] The invention will be described more fully hereinafter with reference to the accompanying drawings, in which exemplary embodiments of the invention are shown. As those skilled in the art would realize, the described embodiments may be modified in various different ways, all without departing from the spirit or scope of the invention.

[0017] In the drawings, the thickness of layers, films, panels, regions, etc., are exaggerated for clarity. Like reference numerals designate like elements throughout the specification. It will be understood that when an element such as a layer, film, region, or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements present.

[0018] Hereinafter, an exemplary embodiment of a liquid crystal display the present invention will be described in detail with reference to the accompanying drawings.

[0019] Firstly, an exemplary embodiment of a liquid crystal display according to the present invention will be described with reference to FIGS. 1 to 3. FIG. 1 is a block diagram showing an exemplary embodiment of the liquid crystal display according to the present invention, FIG. 2 is an equivalent circuit diagram showing a structure of an exemplary embodiment of a liquid crystal display and one pixel according to the present invention, and FIG. 3 is an equivalent circuit diagram showing a plurality of adjacent pixels of an exemplary embodiment of the liquid crystal display according to the present invention.

[0020] Referring to FIG. 1, a liquid crystal display includes a liquid crystal panel assembly 300, a gate driver 400, a data driver 500, a gray voltage generator 800 and a signal controller 600. In an exemplary embodiment, the signal controller 600 may receive data signals R, G and B, a vertically synchronized signal Vsync, a horizontally synchronized signal Hsync, a main clock signal MCLK and a data enable signal DE from an external device. The gate driver 400 may receive a first control signal CONT1 from the signal controller 600, a gate-on voltage Von and a gate-off voltage Voff, and the data driver 500 may receive a second control signal CONT2 and an image signal DAT from the signal controller 600.

[0021] Referring to FIG. 2, the liquid crystal panel assembly 300 includes a lower panel 100 and an upper panel 200 disposed opposite to, e.g., facing, each other, and a liquid crystal layer 3 interposed therebetween.

[0022] The liquid crystal capacitor Clc adopts a first pixel electrode PEa and a second pixel electrode PEb of the lower panel 100 as two terminals, and the liquid crystal layer 3 between the first and second pixel electrodes PEa and PEb serves as a dielectric material. The first pixel electrode PEa is connected to the first switching element (not shown) and the second pixel electrode PEb is connected to the second switching element (not shown).

[0023] The liquid crystal layer 3 has dielectric anisotropy, and liquid crystal molecules 31 of the liquid crystal layer 3 may be arranged such that their long axes are aligned perpendicular to surfaces of the two panels 100 and 200 when an electric field is not applied.

[0024] The first pixel electrode PEa and the second pixel electrode PEb may be formed on different layers or on the same layer. First and second storage capacitors (not shown) serving as assistants of the liquid crystal capacitor Clc may be formed by further including separate electrodes (not shown) provided on the lower panel 100 and interposed between the first and second pixel electrodes PEa and PEb, and insulators. Although not shown, an alternative exemplary embodiment of the liquid crystal display may include an additional electrode on the upper panel 200 and applied with a predetermined voltage of a constant magnitude, and the additional electrode may be transparent.

[0025] In an exemplary embodiment, each pixel PX uniquely displays one of primary colors (spatial division), or each pixel PX temporally and alternately displays primary colors (temporal division), to realize color display. Then, the primary colors are spatially or temporally synthesized, and thus a desired color is recognized. An exemplary embodiment of the primary colors may include three primary colors of red, green and blue. Also, each pixel may display a white color as well as three primary colors of red, green and blue. One exemplary of the spatial division is represented in FIG. 2, where each pixel PX is provide with a color filter CF indicating one of the primary colors on the region of the upper panel 200 and corresponding to the first and second pixel electrodes PEa and PEb. In an alternative exemplary embodiment, unlike FIG. 2, the color filter CF may be disposed on or below the first and second pixel electrodes PEa and PEb of the lower panel 100.

[0026] Referring to FIGS. 1 and 3, in a view of an equivalent circuit, the liquid crystal panel assembly 300 includes a plurality of signal lines Gi, C1, C2, Dj, Dj+1, Dj+2, Dj+3, Dj+4, and Dj+5, and a plurality of pixels PX connected thereto and arranged substantially in a matrix format. In the structure shown in FIG. 2, the liquid crystal

panel assembly 300 includes the lower panel 100 and the upper panel 200 facing each other, and the liquid crystal layer 3 interposed therebetween.

[0027] The signal lines Gi, C1, C2 Dj, Dj+1, and Dj+2 include a plurality of gate lines, e.g., an i-th gate line Gi, that transmits gate signals (also referred to as "scanning signals"), a plurality of data lines, e.g., a j-th data line Dj, a (j+1)-th data line Dj+1, a (j+2)-th data line Dj+2, a (j+3)-th data line Dj+3, a (j+4)-th data line Dj+4, and a (j+5)-th data line Dj+5, that transmits data voltages, a first voltage transmitting line C1 that transmits a first voltage, and a second voltage transmitting line C2 that transmits a second voltage. The gate lines Gi extend substantially in a row direction and substantially parallel to each other, and the data lines Dj, Dj+1, Dj+2, Dj+3, Dj+4, and Dj+5, the first voltage transmitting line C1, and the second voltage transmitting line C2 extend substantially in a column direction and substantially parallel to each other.

[0028] A plurality of pixels PX include a first pixel PX1, a second pixel PX2, a third pixel PX3, a fourth pixel PX4, a fifth pixel PX5 and a sixth pixel PX6 that are sequentially disposed in a row direction of the pixel.

[0029] Among three neighboring pixels, e.g., the first, second and third pixels PX1, PX2, and PX3, the first pixel PX1 includes a first switching element Qa and a second switching element Qb connected to the signal lines, e.g., the i-th gate line Gi, the first voltage transmitting line C1, and the j-th data line Dj, and the liquid crystal capacitor Clc connected thereto, the second pixel PX2 includes a first switching element Qa and a second switching element Qb connected to the signal lines, e.g., the i-th gate line Gi, the first voltage transmitting line C1, and the (j+1)-th data line Dj+1, and the liquid crystal capacitor Clc connected thereto, and the third pixel PX3 includes a first switching element Qa and a second switching element Qb connected to the signal lines, e.g., the i-th gate line Gi, the first voltage transmitting line C1, and the (j+2)-th data line Dj+2, and the liquid crystal capacitor Clc connected thereto.

[0030] The first switching element Qa and the second switching element Qb of three neighboring pixels PX1, PX2, and PX3 as three terminal elements such as a thin film transistors provided in the lower panel 100 and including a control terminal connected to the gate line Gi, an input terminal connected to the first voltage transmitting line C1 or the corresponding data lines Dj, Dj+1, and Dj+2, and an output terminal connected to the liquid crystal capacitor Clc.

[0031] Among three neighboring pixels, e.g., the fourth pixel PX4, the fifth pixel PX5, and the sixth pixel PX6, the fourth pixel PX4 includes a first switching element Qa and a second switching element Qb connected to the signal lines, e.g., the i-th gate line Gi, the second voltage transmitting line C2, and the (j+3)-th data line Dj+3, and the liquid crystal capacitor Clc connected thereto, the fifth pixel PX5 includes a first switching element Qa and a second switching element Qb connected to the signal lines, e.g., the i-th gate line Gi, the second voltage transmitting line C2, and the (j+4)-th data line Dj+4, and the liquid crystal capacitor Clc connected thereto, and the sixth pixel PX6 includes a first switching element Qa and a second switching element Qb connected to the signal lines, e.g., the i-th gate line Gi, the second voltage transmitting line C2, and the (j+5)-th data line Dj+5, and the liquid crystal capacitor Clc connected thereto.

[0032] The first switching element Qa and the second switching element Qb of the three neighboring pixels pixel PX4, PX5, and PX6 as three terminal elements such as thin film transistors provided in the lower panel 100 and including a control terminal connected to the gate line Gi, an input terminal connected to the second voltage transmitting line C2 or the corresponding data lines Dj+3, Dj+4, and Dj+5, and an output terminal connected to the liquid crystal capacitor Clc.

[0033] Hereinafter, an exemplary embodiment of a driving method of a liquid crystal display according to the present invention will be described with reference to FIGS. 2, 3 and 4.

[0034] FIG. 4 is a cross-sectional view of an exemplary embodiment of a liquid crystal display according the present invention.

[0035] Referring to FIGS. 2 and 3, when the first voltage transmitting line C1 is applied with the first voltage and the data lines Dj, Dj+1, and Dj+2 are applied with the data voltage, the data voltage is applied to the corresponding pixels PX1, PX2, and PX3 via the turned-on first and second switching elements Qa and Qb. In detail, the first pixel electrode PEa of the first pixel PX1 is applied with the first voltage through the first voltage transmitting line C1 via the first switching element Qa thereof, and the second pixel electrode PEb is applied with the data voltage through the first data line Dj via the second switching element Qb thereof. Also, the first pixel electrode PEa of the second pixel PX2 is applied with the data voltage through the second data line Dj+1 via the first switching element Qa thereof, and the second pixel electrode PEb is applied with the first voltage through the first voltage transmitting line C1 via the second switching element Qb thereof. Also, the first pixel electrode PEa of the third pixel PX3 is applied with the first voltage through the first voltage transmitting line Cj via the first switching element Qa thereof, and the second pixel electrode PEb is applied with the data voltage through the third data line Dj+2 via the second switching element Qb thereof.

[0036] Also, when the second voltage transmitting line C2 is applied with the second voltage and the data lines Dj+3, Dj+4, and Dj+5 are applied with the data voltage, the data voltage is applied to the corresponding pixels PX4, PX5, and PX6 via the turned-on first and second switching elements Qa and Qb. In detail, the first pixel electrode PEa of the fourth pixel PX4 is applied with the second voltage through the second voltage transmitting line C2 via the first switching element Qa thereof, and the second pixel electrode PEb is applied with the data voltage through the fourth data line Dj+3 via the second switching element Qb thereof. Also, the first pixel elec-

trode PEa of the fifth pixel PX5 is applied with the data voltage through the fifth data line Dj+4 via the first switching element Qa thereof, and the second pixel electrode PEb is applied with the second voltage through the second voltage transmitting line C2 via the second switching element Qb thereof. Further, the first pixel electrode PEa of the sixth pixel PX6 is applied with the second voltage through the second voltage transmitting line C2 via the first switching element Qa thereof, and the second pixel electrode PEb is applied with the data voltage through the sixth data line Dj+5 via the second switching element Qb thereof.

[0037] In an exemplary embodiment, the voltage applied to the first pixel electrode PEa and the second pixel electrode PEb of the pixels PX1, PX2, PX3, PX4, PX5, and PX6 are corresponding to luminance displayed by the pixel PX.

[0038] The first voltage transmitted through the first voltage transmitting line C1 and the second voltage transmitted through the second voltage transmitting line C2 may have opposite polarities with respect to a reference voltage. In one exemplary embodiment, for example, when a minimum voltage of the liquid crystal display is about zero (0) volt (V) and a maximum voltage is about 14 V, the reference voltage may be about 7 V, the voltage transmitted through the first voltage line C1 may be about 0 V or about 14 V, and the voltage transmitted through the second voltage line C2 may be about 14 V or about 0 V. Also, the polarities of the first voltage transmitted through the first voltage line C1 and the second voltage transmitted through the second voltage line C2 may be changed per frame.

[0039] The difference between the two data voltages applied to the first and second pixels PXa and PXb corresponds to a charged voltage of the liquid crystal capacitors Clc, i.e., a pixel voltage. When a potential difference is generated between the two terminals of the liquid crystal capacitor Clc, as shown in FIG. 4, an electric field substantially parallel to the surface of the display panel 100 and 200 is generated in the liquid crystal layer 3 between the first and second pixel electrodes PEa and PEb. When the liquid crystal molecules 31 have positive dielectric anisotropy, the liquid crystal molecules 31 are arranged such that the longitudinal axes thereof are aligned substantially parallel to the direction of the electric field, and the degree of inclination of the longitudinal axes is changed according to the magnitude of the pixel voltage. This liquid crystal layer 3 is referred to as an electrically-induced optical compensation ("EOC") mode liquid crystal layer. Also, the change degree of the polarization of light passing through the liquid crystal layer 3 is changed according to the inclination degree of the liquid crystal molecules 31. The change of the polarization appears as a change of transmittance of the light by the polarizer, and the pixel PX thereby displays a predetermined luminance.

[0040] Hereinafter, an exemplary embodiment of a driving method of a liquid crystal display according to the present invention will be described with reference to FIGS. 3 and 5. FIG. 5 is a signal timing diagram of signals applied to a pixel of the liquid crystal display shown in FIG. 3.

[0041] Firstly, a driving method during the first frame (1st Frame) will be described. When the gate lines Gi is sequentially applied with the gate-on voltage, the first pixel electrode PEa of the first pixel PX1 is applied with the first voltage through the first voltage transmitting line C1 via the turned-on first switching element Qa thereof, the second pixel electrode PEb of the first pixel PX1 is applied with the data voltage through the first data line Dj via the turned-on second switching element Qb thereof, the first pixel electrode PEa of the second pixel PX2 is applied with the data voltage through the second data line Dj+1 via the turned-on first switching element Qa thereof, and the second pixel electrode PEb of the second pixel PX2 is applied with the first voltage through the first voltage transmitting line C1 via the turned-on second switching element Qb thereof. Also, the first pixel electrode PEa of the third pixel PX3 is applied with the first voltage through the first voltage transmitting line Cj via the turned-on first switching element Qa thereof, and the second pixel electrode PEb of the third pixel PX3 is applied with the data voltage through the third data line Dj+2 via the turned-on second switching element Qb thereof. Similarly, the first pixel electrode PEa of the fourth pixel PX4 is applied with the second voltage through the second voltage transmitting line C2 via the turned-on first switching element Qa thereof, and the second pixel electrode PEb of the fourth pixel PX4 is applied with the data voltage through the fourth data line Dj+3 via the turned-on second switching element Qb thereof. Also, the first pixel electrode PEa of the fifth pixel PX5 is applied with the data voltage through the fifth data line Dj+4 via the turned-on first switching element Qa thereof, and the second pixel electrode PEb of the fifth pixel PX5 is applied with the second voltage through the second voltage transmitting line C2 via the turned-on second switching element Qb thereof. Further, the first pixel electrode PEa of the sixth pixel PX6 is applied with the second voltage through the second voltage transmitting line C2 via the turned-on first switching element Qa thereof, and the second pixel electrode PEb of the sixth pixel PX6 is applied with the data voltage through the sixth data line Dj+5 via the turned-on second switching element Qb thereof.

[0042] In an exemplary embodiment, the polarity of the first voltage transmitted through the first voltage transmitting line C1 may be positive (+), and the polarity of the second voltage transmitted through the second voltage transmitting line C2 may be negative (-). Accordingly, during the first frame, the polarities of the first pixel PX, the second pixel PX2 and the third pixel PX3 are positive (+), and the polarities of the fourth pixel PX4, the fifth pixel PX5, and the sixth pixel PX6 are negative (-).

[0043] However, in an alternative exemplary embodiment of the present invention, the polarity of the first volt-

age applied to the first voltage transmitting line C1 may be negative (-), and the polarity of the second voltage applied to the second voltage line C2 may be positive (+).

[0044] The steps described above are repeated for the pixel row connected to the gate lines, and thereby the first frame (1 st Frame) is completed. When the first frame (1 st Frame) is completed, the second frame (2nd Frame) is started.

[0045] When the second frame (2nd Frame) is started, the gate-on voltage is sequentially applied to the gate lines Gi, and the signal is applied to each pixel similarly to the signals applied in the first frame. However, during the second frame, the polarities of the first voltage transmitted through the first voltage transmitting line C1 and the second voltage transmitted through the second voltage transmitting line C2 are opposite to that of the first frame. Accordingly, the polarity of a pixel PX in the second frame is opposite to the polarity of the pixel in the first frame. In detail, during the second frame, the polarities of the first pixel PX, the second pixel PX2 and the third pixel PX3 are negative (-), and the polarities of the fourth pixel PX4, the fifth pixel PX5 and the sixth pixel PX6 are positive (+).

[0046] However, in an alternative exemplary embodiment of the present invention, the polarity of the first voltage applied to the first voltage transmitting line C1 during the second frame may be positive (+), and the polarity of the second voltage applied to the second voltage line C2 may be negative (-).

[0047] The first frame and the second frame are repeated such that the desired pixel voltage is applied to each pixel during the desired frame.

[0048] In general, one pixel may be connected to one gate line and two different data lines to charge a desired voltage to the liquid crystal capacitor Clc by dividing one pixel into two pixel electrodes and applying the different voltages to the two pixel electrodes via the different switching elements. More particularly, the first and second switching elements connected to the first and second pixel electrodes of each pixel may be connected to the same gate line and the different data lines, thereby receiving the data voltage through the different data lines.

[0049] In an exemplary embodiment, one pixel of the liquid crystal display is connected to two gate lines, one data line, and a first voltage transmitting line and a second voltage transmitting line. Accordingly, the number of data lines is substantially reduced, and thereby the cost of the driver of the liquid crystal display is substantially reduced. According to the arrangement of the signal lines and the pixels of an exemplary embodiment of the liquid crystal display, two voltage lines are added compared with a typical arrangement of the signal lines and the pixels. However, the voltage lines are applied with the voltage that has the constant value during one frame and has the polarity that is changed per frame such that a driver having a simplified structure may be realized to apply the voltage having the constant value and the polarity that is changed per frame, and the driving method is thereby substantially simplified and the manufacturing cost is substantially reduced.

[0050] Next, an exemplary embodiment of the above-described liquid crystal display will be described with reference to FIGS. 6 and 7. FIG. 6 is a top plan view of an exemplary embodiment of the liquid crystal display according to the present invention, and FIG. 7 is a cross-sectional view of the liquid crystal panel assembly in FIG. 6 taken along line VII-VII.

[0051] Referring to FIGS. 6 and 7, a liquid crystal panel assembly according to an exemplary embodiment of the present invention includes a lower panel 100 and an upper panel 200 disposed substantially opposite to each other, and a liquid crystal layer 3 interposed between the lower and upper display panels 100 and 200.

[0052] Firstly, the lower panel 100 will be described.

[0053] A plurality of gate conductors including a plurality of gate lines 121, a plurality of storage electrode lines 131, and first to third connection conductors 135a, 135b and 135c are disposed on a first insulation substrate 110.

[0054] The gate lines 121 transmit gate signals and longitudinally extend in a transverse direction, and each gate line 121 includes a plurality of pairs of a first gate electrode 124a and a second gate electrode 124b protruding upward from a main portion of the gate line 121 and in a longitudinal direction.

[0055] The storage electrode lines 131 are applied with a predetermined voltage and mainly extend in the transverse direction. Each storage electrode line 131 is positioned between two neighboring gate lines 121 and is close to the lower of the neighboring gate lines 121 in the top plan view. Each storage electrode line 131 includes a plurality of first storage electrodes 133a and second storage electrodes 133b protruding upward from the main portion of the storage electrode line 131 and in the longitudinal direction. The connection conductors 135a, 135b and 135c are disposed at an edge and a center of the pixel area.

[0056] The gate conductor may have a single layer or a multilayer structure.

[0057] A gate insulating layer 140 including silicon nitride (SiNx) or silicon oxide (SiOx) is disposed on the gate conductor.

[0058] A plurality of pairs of a first semiconductor 154a and a second semiconductor 154b including hydrogenated amorphous silicon or polysilicon are formed on the gate insulating layer 140. The first semiconductor 154a and the second semiconductor 154b are positioned overlapping the first gate electrode 124a and the second gate electrode 124b, respectively.

[0059] A pair of ohmic contacts (not shown) are disposed overlapping each of the first semiconductors 154a, and a pair of ohmic contacts 163b and 165b are disposed overlapping each the second semiconductors 154b. The ohmic contact may include a material such as n+ hydrogenated amorphous silicon, which is highly doped with an n-type impurity such as phosphorous (P), or of silicide.

In an alternative exemplary embodiment, the ohmic contacts may be omitted. In detail, when at least one of the first semiconductor 154a and the second semiconductor 154b include an oxide semiconductor, the ohmic contacts may be omitted.

[0060] A data conductor including a plurality of data lines, e.g., a first data line 171 a, a second data line 171 b and a third data line 171 c and voltage transmitting lines 172, and a plurality of pairs of a first drain electrode 175a and a second drain electrode 175b is disposed on the ohmic contacts 163a and 165a and the gate insulating layer 140.

[0061] The data lines 171 a, 171 b and 171 c, which transmit data signals, mainly extend in the longitudinal direction and intersect the gate lines 121 and the storage electrode lines 131. The voltage transmitting line 172 transmits a voltage of a constant magnitude, and extends substantially parallel to the data lines 171 a, 171b, and 171c thereby intersecting the gate lines 121 and the storage electrode lines 131. The voltage transmitting line 172 includes a first source electrode 173b that extends from a main portion of the voltage transmitting line 172 and is curved with a U-like shape toward the first gate electrode 124b in the top plan view.

[0062] Each of the data lines 171 a, 171 b, and 171c include a second source electrode 173b that is curved with a U-like shape toward the second gate electrode 124b.

[0063] The voltage transmitted by the voltage transmitting line 172 may have a constant magnitude, and the polarity thereof may be changed per frame. The first source electrodes 173a of the second pixel PX2 and the third pixel PX3 are connected to the first source electrode 173a of the first pixel PX1 connected to the voltage transmitting line 172 via a contact hole 186c and a connection member 196, thereby receiving the same signal. The voltage transmitting line 172 transmits the voltage to three pixels PX1, PX2 and PX3.

[0064] Each of the first drain electrode 175a and the second drain electrode 175b includes a bar-shaped first end and a second end having a wide area in the top plan view. The bar-shape first ends of the first drain electrode 175a and the second drain electrode 175b are opposite to the first source electrode 173a and the second source electrode 173b with respect to the first gate electrode 124a and the second gate electrode 124b, and are partially enclosed by the curved first source electrode 173a and second source electrode 173b, respectively. The second ends of the first drain electrode 175a and the second drain electrode 175b are electrically connected to a first pixel electrode 191 a and a second pixel electrode 191 b via a first contact hole 185a and a second contact hole 185b, which will be described in greater detail later.

[0065] The first gate electrode 124a, the first source electrode 173a, and the first drain electrode 175a collectively define a first thin film transistor ("TFT") along with the first semiconductor 154a, and a channel of the first TFT is formed on the first semiconductor 154a between the first source electrode 173a and the first drain electrode 175a.

[0066] The second gate electrode 124b, the second source electrode 173b and the second drain electrode 175b collectively define a second TFT along with the second semiconductor 154b, and a channel of the second TFT is formed on the second semiconductor 154b between the second source electrode 173b and the second drain electrode 175b.

[0067] The data conductors 171, 172, 175a and 175b may have a single layer or multilayer structure.

[0068] The ohmic contacts are interposed only between the underlying semiconductors 154a and 154b and the overlying data conductors 171, 172, 175a, and 175b thereon, respectively, and reduce contact resistance therebetween. The semiconductors 154a and 154b include exposed portions that are not covered by the data conductors 171, 172, 175a, and 175b, and portions that are disposed between the source electrodes 173a and 173b and the drain electrodes 175a and 175b.

[0069] A passivation layer 180 including an inorganic insulator or organic insulator is disposed on the data conductors 171, 172, 175a, and 175b and the exposed portions of the semiconductors 154a and 154b.

[0070] The passivation layer 180 has a plurality of the first and second contact holes 185a and 185b at the wide second ends of the first drain electrode 175a and the second drain electrode 175b. The passivation layer 180 and the gate insulating layer 140 have a plurality of contact holes 186a, 186b, 187a and 187b exposing portions of the first to third connection conductors 135a, 135b, and 135c.

[0071] A plurality of pixel electrodes 191 including a transparent conductive material such as indium tin oxide ("ITO") or indium zinc oxide ("IZO") or a reflective metal such as aluminum, silver, chromium, or alloys thereof are disposed on the passivation layer 180. The pixel electrodes 191 include a plurality of pairs of the first and second pixel electrode 191 a and 191 b.

[0072] As shown in FIG. 6, an entire outer shape of one pixel electrode 191 is a quadrangle, and the first pixel electrode 191 a and the second pixel electrode 191 b are engaged with each other. That is, portions of the first pixel electrode 191 a and the second pixel electrode 191 b alternate with each other in the longitudinal and transverse directions. The first pixel electrode 191 a and the second pixel electrode 191b are disposed substantially symmetrically with respect to an imaginary transverse central line, and are respectively divided into two sub-regions, e.g., an upper sub-region and a lower sub-region.

[0073] The first pixel electrode 191 a includes a lower stem 191 a1 and an upper stem 191a3, and a plurality of first branches 191a2 and a plurality of second branches 191a4 extending from the lower stem 191a1 and the upper stem 191a3, respectively. The second pixel electrode 191 b includes a lower stem 191 b1 and an upper stem

191 b3, and a plurality of the third branches 191 b2 and a plurality of fourth branches 191 b4 extending from the lower stem 191 b1 and the upper stem 191 b3, respectively.

[0074] The lower stem 191a1 and the upper stem 191a3 of the first pixel electrode 191 a are disposed on the left side and the right side of one pixel electrode, respectively, and the lower stem 191 b1 and the upper stem 191 b3 of the second pixel electrode 191 b are disposed on the right side and the left side of one pixel electrode, respectively.

[0075] The angle of the plurality of branches 191 a2, 191 a4, 191 b2 and 191 b4 of the first pixel electrode 191 a and the second pixel electrode 191 b, with respect to the transverse center line, may be about 45 degrees.

[0076] The branches 191 a2, 191 a4, 191 b2 and 191 b4 of the first pixel electrode 191 a and the second pixel electrode 191b engage with each other with a predetermined interval therebetween and are alternately disposed, thereby forming a pectinated pattern. In an exemplary embodiment, the interval between the branches 191a2, 191a4, 191b2 and 191b4 of the first pixel electrode 191 a and the second pixel electrode 191 b less than or equal to about 30 micrometers (μm). The interval between adjacent branches 191a2, 191a4, 191 b2 and 191 b4 may be taken perpendicular to a longitudinal direction of the branches 191 a2, 191 a4, 191 b2 and 191 b4.

[0077] The branches 191 a2, 191 a4, 191 b2 and 191 b4 of the first pixel electrode 191 a and the second pixel electrode 191 b engage with each other and are alternately disposed, thereby forming a pectinated pattern. A pixel region includes a low gray region, in which the interval between the neighboring branches is wide, and a high gray region, in which the interval between the neighboring branches is narrow, and the high gray region is disposed substantially at the center of the pixel area and is enclosed by the low gray region. In an exemplary embodiment, in the case of the low gray region, in which the interval between the branches of the first pixel electrode 191 a and the branches of the second pixel electrode 191 b that are alternately disposed, is wide, the intensity of the electric field applied to the liquid crystal layer 3 between the branches of the first pixel electrode 191 a and the branches of the second pixel electrode 191 b is decreased such that a relative low gray is displayed although the same voltage is applied compared with the high gray region in which the interval between the neighboring branches is narrow. In the case of the high gray region, in which the interval between the branches of the first pixel electrode 191 a and the branches of the second pixel electrode 191 b that are alternately disposed, is narrow, the intensity of the electric field applied to the liquid crystal layer 3 between the branches of the first pixel electrode 191 a and the branches of the second pixel electrode 191 b is increased such that a relative high gray is displayed although the same voltage is applied compared with the low gray region in which the interval between the neighboring branches is wide. In an alternative exemplary embodiment, the inclination angle of the liquid crystal molecules 31 of the liquid crystal layer 3 may vary and different luminance with respect to one image information set may be displayed by varying the interval between the first pixel electrode 191 a and the second pixel electrode 191 b in one pixel. Further, an image viewed from a side of the liquid crystal display may be substantially similar to an image viewed from a front of the liquid crystal display by properly adjusting the interval between the branches of the first pixel electrode 191 a and the second pixel electrode 191 b. Therefore, in exemplary embodiment, side visibility is substantially improved and transmittance is substantially enhanced.

[0078] In the exemplary embodiment , a ratio of a total planar area of the low gray region and a total planar area of the high gray region may be in a range of about 4:1 to about 30:1. Also, the interval between the branches of the first pixel electrode 191 a and the second pixel electrode 191 b may be about 10 μm to about 20 μm, and more specifically about 10 μm to about 17 μm in the low gray region, and the interval between the branches of the first pixel electrode 191 a and the second pixel electrode 191 b may be about 3 μm to about 9 μm, and more specifically about 3 μm to about 7 μm in the high gray region.

[0079] A portion of the low gray region is disposed in a portion that is not enclosed by the stems 191a1, 191a3, 191b1, and 191b3 of the first pixel electrode 191 a and the second pixel electrode 191 b among the pixel outer portion of the liquid crystal display according to the exemplary embodiment illustrated in FIGS. 6 and 7 such that the portion of low gray region is disposed at the region where the magnitude of the horizontal electric field between the first pixel electrode 191 a and the second pixel electrode 191 b is relatively weak. Accordingly, a display quality deterioration that may be generated by the asymmetry of the direction of the horizontal electric field between the first pixel electrode 191 a and the second pixel electrode 191 b such as texture may be substantially reduced.

[0080] In an exemplary embodiment, the liquid crystal display may have an extension region, in which the intervals between the branches 191 a2 and 191 a4 of the first pixel electrode 191 a and the branches 191b2 and 191b4 of the second pixel electrode 191b are extended. The intervals between the branches 191a2 and 191a4 of the first pixel electrode 191 a and the branches 191b2 and 191b4 of the second pixel electrode 191 b in the extension region may be about 20 μm to about 28 μm. In an exemplary embodiment, the extension region is disposed at the position where the liquid crystal molecules are irregularly moved in the pixel area such as a portion near the portion that is not enclosed by the stems 191a1, 191a3, 191b1 and 191b3 of the first pixel electrode 191 a and the second pixel electrode 191 b among the pixel outer part of the liquid crystal display or the gate line 121.

[0081] In such an embodiment, the liquid crystal molecules 31 disposed at the extension region are less influenced by the horizontal electric field generated between the branches 191a2 and 191a4 of the first pixel electrode 191 a and the branches 191b2 and 191b4 of the second pixel electrode 191 b. Accordingly, the liquid crystal molecules 31 disposed at the extension region are less influenced by the asymmetrical horizontal electric field, and the liquid crystal molecules 31 have a tendency to be in an initial vertical alignment state, such that the liquid crystal molecules may be effectively prevented from being irregularly slanted by external pressure. Accordingly, irregular movement of the liquid crystal molecules is effectively prevented from being diffused from the outer part of the pixel area to the inner part of the pixel area, and a singular point limited in the extension region is thereby prevented from being formed such that the quality deterioration of a large-sized display from the outer part of the pixel area to the inner part of the pixel area is effectively prevented.

[0082] However, the shape of the first pixel electrode 191 a and the second pixel electrode 191b in one pixel of the liquid crystal display according to an exemplary embodiment of the present invention is not limited thereto, and all shapes of which at least portions of the first pixel electrode 191 a and the second pixel electrode 191b are the same and are alternately disposed may be applied.

[0083] The first pixel electrode 191 a of the first pixel PX1 is physically and electrically connected to the first drain electrode 175a via the contact hole 185a, thereby receiving a voltage transmitted through the voltage transmitting line 172 from the first drain electrode 175a. Also, the second pixel electrode 191 b of the first pixel PX1 is physical and electrically connected to the second drain electrode 175b via the contact hole 185b, thereby receiving the first data voltage flowing in the first data line 171 a. The first sub-pixel electrode 191 a and the second sub-pixel electrode 191 b form the liquid crystal capacitor Clc along with the liquid crystal layer 3 interposed therebetween to maintain the applied voltage after the first TFT and the second TFT are turned off.

[0084] The first pixel electrode 191 a of the second pixel PX2 is connected to the second drain electrode 175b via the first contact hole 185a, thereby receiving the data voltage through the second data line 171b, and the second pixel electrode 191 b of the second pixel PX2 is connected to the first drain electrode 175a via the second contact hole 185b, thereby receiving the voltage through the voltage transmitting line 172.

[0085] The first pixel electrode 191 a of the third pixel PX3 is electrically connected to the first drain electrode 175a via the contact hole 185a, thereby receiving the voltage through the voltage transmitting line 172 from the first drain electrode 175a, and the second pixel electrode 191 b of the third pixel PX3 is electrically connected to the second drain electrode 175b via the contact hole 185b, thereby receiving the third data voltage through the third data line 171 c.

[0086] The wide second ends of the first drain electrode 175a and the second drain electrode 175b connected to the first sub-pixel electrode 191 a and the second sub-pixel electrode 191 b overlap the storage electrodes 133a and 133b via the gate insulating layer 140, thereby collectively defining the storage capacitor that reinforces the voltage maintaining capacity of the liquid crystal capacitor Clc.

[0087] In the first pixel PX1, the lower stem 191a1 of the first pixel electrode 191 a is connected to the first connection conductor 135a via the contact hole 186a, and the upper stem 191 a3 of the first pixel electrode 191 a is connected to the first connection conductor 135a via the contact hole 186b, thereby receiving the voltage from the first drain electrode 175a.

[0088] In the first pixel PX1, the lower stem 191 b1 of the second pixel electrode 191 b is connected to the second connection conductor 135a via the contact hole 187a, and the upper stem 191b3 of the second pixel electrode 191b is connected to the second connection conductor 135a via the contact hole 187b, thereby receiving the voltage from the second drain electrode 175b. In an exemplary embodiment, the stems 191a1, 191a3, 191b1 and 191b3 of the second pixel PX2 and the third pixel PX3 receive the voltage through a connection substantially the same as the connection described with respect to the first pixel PX1.

[0089] A lower alignment layer (not shown) may be disposed on an inner surface of the display panel 100, and the lower alignment layer may be a vertical alignment layer. Although not shown, a polymer layer may be disposed on the lower alignment layer, and the polymer layer may include a polymer branch that is formed according to an initial alignment direction of the liquid crystal molecules 31. In an exemplary embodiment, the polymer layer may be formed by exposing and polymerizing a prepolymer such as a monomer, that is hardened by polymerization with light such as ultraviolet rays, and the alignment force of the liquid crystal molecules may be controlled according to the polymer branch.

[0090] Next, the upper panel 200 will be described.

[0091] A light blocking member 220 is disposed on a second insulation substrate 210 including transparent glass or plastic. The light blocking member 220 prevents light leakage between the pixel electrodes 191 and defines an opening region that faces the pixel electrodes 191.

[0092] A plurality of color filters 230 are disposed on the second substrate 210 and the light blocking member 220. The color filters 230 mostly exist within the area surrounded by the light blocking member 220, and may longitudinally extend along the columns of the pixel electrodes 191 in the longitudinal direction. The respective color filters 230 may express one of three primary colors of red, green and blue, or the primary colors of yellow, cyan, and magenta. Also, each pixel may represent a mixture color of the primary colors or white as well as the

primary colors.

[0093] An overcoat 250 is disposed on the color filters 230 and the light blocking member 220. The overcoat 250 may include an inorganic or organic insulator, and reduce or effectively prevents exposure of the color filters 230 and provides a planarized surface. In an alternative exemplary embodiment, the overcoat 250 may be omitted.

[0094] An upper alignment layer (not shown) is disposed on the inner surface of the display panel 200, and the upper alignment layer may be a vertical alignment layer. Although not shown, a polymer layer may also be disposed on the upper alignment layer. In an exemplary embodiment, the polymer layer may be formed by exposing a prepolymer such as a monomer, that is hardened by polymerization with light such as ultraviolet rays, such that the alignment force of the liquid crystal molecules may be controlled. The polymer layer may include a polymer branch that is formed according to the initial alignment direction of the liquid crystal molecule.

[0095] At least one polarizer (not shown) may be provided on the outer surface of the display panels 100 and 200.

[0096] The liquid crystal layer 3 is disposed between the lower display panel 100 and the upper display panel 200, and includes liquid crystal molecules 31 that have positive dielectric anisotropicity, and the liquid crystal molecules 31 may be aligned such that longitudinal axes thereof are substantially perpendicular to the surfaces of two display panels 100 and 200 in a state in which there is no electric field.

[0097] When the first pixel electrode 191 a and the second pixel electrode 191 b are applied with different voltages, an electric field substantially parallel to the surfaces of the display panels 100 and 200 is generated. Thus, the liquid crystal molecules of the liquid crystal layer 3 that are initially aligned perpendicular to the surfaces of the display panels 100 and 200 are rearranged in response to the electric field such that the longitudinal axes thereof are declined parallel to the direction of the electric field, and the change degree of the polarization of the light incident to the liquid crystal layer 3 is different according to the declination degree of the liquid crystal molecules. The change of the polarization appears as a change of the transmittance by the polarizer, and thereby the liquid crystal display displays the images.

[0098] As described above, the liquid crystal molecules 31 that are vertically aligned are used such that the contrast ratio of the liquid crystal display may be improved and the wide viewing angle may be realized. Furthermore, when the liquid crystal molecules 31 that are aligned perpendicular to the display panel 100 and 200 are used, the contrast ratio of the liquid crystal display may be improved and the wide viewing angle may be realized. In an exemplary embodiment, the liquid crystal molecules 31 that have positive dielectric anisotropicity have greater dielectric anisotropicity and a lower rotation viscosity as compared to the liquid crystal molecules 31 that have negative dielectric anisotropicity, and a response speed is thereby substantially increased.

[0099] Also, in an exemplary embodiment of the liquid crystal display, the branches of the first pixel electrode 191 a and the second pixel electrode 191 b engage with each other and are alternately disposed, thereby forming a pectinated pattern. A low gray region is formed where the interval between the neighboring branches is wide, and a high gray region is formed where the interval between the neighboring branches is narrow, and the high gray region is disposed at the center of the pixel area and is enclosed by the low gray region. Accordingly, the inclination angle of the liquid crystal molecules 31 of the liquid crystal layer 3 may vary and different luminance with respect to one image information set may be displayed by varying the interval between the first pixel electrode 191 a and the second pixel electrode 191 b in one pixel. Further, an image viewed from the side of the liquid crystal display may be substantially similar to an image viewed from the front of the liquid crystal display by properly adjusting the interval between the branches of the first pixel electrode 191 a and the second pixel electrode 191 b. Therefore, in an exemplary embodiment, side visibility is substantially improved and transmittance is substantially enhanced.

[0100] The low gray region is disposed in a portion that is not enclosed by the stems 191 a1, 191 a3, 191 b1 and 191 b3 of the first pixel electrode 191 a and the second pixel electrode 191 b among the pixel outer portion of the liquid crystal display in FIGS. 6 and 7 such that the region where the magnitude of the horizontal electric field between the first pixel electrode 191 a and the second pixel electrode 191 b is relatively weak is disposed. Accordingly, the display quality deterioration that can be generated by the asymmetry of the direction of the horizontal electric field between the first pixel electrode 191 a and the second pixel electrode 191 b such as texture may be reduced.

[0101] In an exemplary embodiment, the liquid crystal display has the extension region where the interval between portions of the branches 191a2 and 191a4 of the first pixel electrode 191 a, and between portions of the branches 191b2 and 191 b4 of the second pixel electrode 191 b are extended. The interval between the portions of the branches 191a2 and 191a4 of the first pixel electrode 191 a and the interval between the portions of the branches 191b2 and 191b4 of the second pixel electrode 191 b in the extension region may be about 20 μm to about 28 μm. In an exemplary embodiment, the extension region is disposed at the position where the liquid crystal molecules are irregularly moved in the pixel area such as a portion near the portion that is not enclosed by the stems 191 a1, 191a3, 191b1 and 191b3 of the first pixel electrode 191 a and the second pixel electrode 191 b among the pixel outer part of the liquid crystal display or near the gate line 121.

[0102] In such an embodiment, the liquid crystal molecules 31 disposed at the extension region are less in-

fluenced by the horizontal electric field generated between the branches 191a2 and 191a4 of the first pixel electrode 191 a and the branches 191b2 and 191b4 of the second pixel electrode 191 b. Accordingly, the liquid crystal molecules 31 disposed at the extension region are less influenced by the asymmetry horizontal electric field, and the liquid crystal molecules 31 have a tendency to be in the initial vertical alignment state, such that the liquid crystal molecules may be prevented from being irregularly slanted by external pressure. Accordingly, the irregular movement of the liquid crystal molecules is prevented from being diffused from the outer part of the pixel area to the inner of the pixel area, and the singular point limited in the extension region is prevented from being formed such that the large-sized display quality deterioration from the outer part of the pixel area to the inner part of the pixel area may be prevented.

[0103] In such an embodiment, the voltage transmitting line 172 is covered by the stem of the pixel electrodes 191. In addition to, the stems of the pixel electrodes 191 applied with the data voltages through the data lines are disposed opposite to each other with respect to the first data line 171 a and the second data line 171 b and the stems of the pixel electrodes applied with the voltage through the voltage transmitting line are disposed opposite to each other with respect to the first data line 171 a and the second data line 171 b. This will be described with reference to FIGS. 8A to 8C. FIGS. 8A to 8C are partial top plan views of an exemplary embodiment of a liquid crystal display according to the present invention.

[0104] Referring to FIG. 8A, at least a portion of the voltage transmitting line 172 of the liquid crystal display is covered by the stems 191a1 and 191 b3 of the pixel electrodes 191 a and 191 b in the top plan view. In an exemplary embodiment, the stems 191 a1 and 191 b3 of the pixel electrodes 191 a and 191 b covering the voltage transmitting line 172 may cover at least about two third of the voltage transmitting line 172.

[0105] As described above, the voltage transmitting line 172 that transmits the voltage having the constant magnitude is covered by the pixel electrodes 191 a and 191 b such that the electric field may not be generated between the voltage transmitting line 172 and the pixel electrodes 191 a and 191 b, and the voltage distortion of the pixel electrodes 191 a and 191 b and the signal delay of the voltage transmitted by the voltage transmitting line 172 is thereby effectively prevented. Also, the capacitance caused by the overlapping of the pixel electrodes 191 a and 191 b and the voltage transmitting line 172 functions as a storage capacitor such that the storage capacitance of the liquid crystal display is substantially increased. Therefore, any electric fields caused by the signal of the voltage transmitting line 172 may be prevented and storage capacitors may be increased.

[0106] Next, referring to FIGS. 8B and 8C, the stems of the pixel electrodes applied with the data voltage through the data lines are disposed opposite to each other at the right and left sides of the data line 171 b and 171 b of the liquid crystal display, and the stems of the pixel electrodes applied with the voltage through the voltage transmitting line are disposed opposite to each other. Referring to FIG. 8B, the stem 191b1 of the second pixel electrode 191 b of the first pixel PX1 applied with the data voltage and the stem 191a1 of the first pixel electrode 191 a of the second pixel PX2 applied with the data voltage are disposed to opposite to each other at the right and left sides of the first data line 171 a, which is disposed therebetween, and the stem 191a3 of the first pixel electrode 191 a of the first pixel PX1 applied with the voltage from the voltage transmitting line 172 and the stem 191b3 of the second pixel electrode 191 b of the second pixel PX2 applied with the voltage from the voltage transmitting line 172 are disposed opposite to each other. Also, referring to FIG. 8C, the stems of the pixel electrodes applied with the data voltage through the data lines connected to the second and third pixels PX2 and PX3 are disposed opposite to each other with respect to the second data line 171b, which is disposed therebetween, and the stems of the pixel electrodes applied with the voltage through the voltage transmitting line are disposed opposite to each other, at the right and left sides of the second data line 171 b.

[0107] In such an embodiment, the stems of the pixel electrodes applied with the data voltage through the data line are disposed opposite to, e.g., facing, each other and the stems of the pixel electrodes applied with the voltage through the voltage transmitting line are disposed opposite to each other at left and right sides of the data lines 171 a and 171 b such that crosstalk that may be generated by the deviation of the parasitic capacitance due to the data lines 171 a and 171 b is effectively prevented from being generated.

[0108] Next, display quality of an exemplary embodiment of a liquid crystal display of the present invention will be described with reference to FIGS. 9 and 10. FIG. 9 is a graph of grayscale measuring results showing display quality of an exemplary embodiment of the liquid crystal display, and FIG. 10 is a graph grayscale measuring results showing display quality of an exemplary embodiment of the liquid crystal display.

[0109] In an exemplary experiment, grayscales of case 1 and case 2 were measured. In the exemplary experiment, case 1 is a conventional liquid crystal display, in which the voltage transmitting line 172 is not covered by the stems of the pixel electrodes, and the branches of the pixel electrodes applied with the data voltage and the branches of the pixel electrodes applied with the voltage from the voltage transmitting line are disposed to be symmetrical at both side of the data lines 171 a and 171 b, and case 2 is an exemplary embodiment of the liquid crystal display, in which the voltage transmitting line 172 is covered by the stems of the pixel electrodes, and the stems of the pixel electrodes applied with the data voltage through the data lines and the stems of the pixel electrodes applied with the voltage through the voltage transmitting line are disposed to be symmetrical with respect

to the data lines disposed therebetween, e.g., to face each other at both sides of the data lines 171 a and 171 b. Also, for case 1 and case 2, in the low gray region where an interval between the neighboring branches of the first pixel electrode 191 a and the second pixel electrode 191 b is relatively wide and the high gray region where an interval between the neighboring branches is relatively narrow. In the exemplary experiment, the intervals between the branches of the first pixel electrode 191 a and the second pixel electrode 191 b are set to be about 11.5 μm and 5 μm, respectively, or the intervals between the branches of the first pixel electrode 191 a and the second pixel electrode 191 b are set to be about 11.5 μm and about 6.5 μm, respectively. The remaining conditions are substantially the same.

[0110] In the exemplary experiment, the liquid crystal displays prepare according to case 1 and case 2 is pressed with a predetermined pressure and it is determined whether stains due to the pressure are recognized for each grayscale, and the results thereof are shown in the graph of FIG. 9. Also, the liquid crystal display is hit using an apparatus having a constant weight and then it is determined whether stains caused by the pressure for each grayscale are recognized, and the results thereof are shown in FIG. 10.

[0111] In FIG. 9, lines x1 and x2 are curves showing the grayscales when the stains due to the pressure are recognized, and lines x1' and x2' are curves showing the grayscales when the stains due to the pressure disappear in case 1. Also, lines y1 and y2 are curves showing the grayscales when the stains due to the pressure are recognized, and lines y1' and y2' are curves showing the grayscales when the stains due to the pressure disappear in case 2.

[0112] Referring to FIG. 9, when comparing the lines x1 and x2 and the lines y1 and y2 and the lines x1' and x2' and the lines y1' and y2' by comparing grayscale values corresponding to a same X-axis, it is confirmed that the stain by the pressure is recognized at a lower grayscale in case 2 than in case 1. As shown in FIG. 9, since the stains caused by the same pressure are recognized at a lower grayscale in case 2 of an exemplary embodiment of the liquid crystal display, compared with case 1 of the conventional liquid crystal display, a user may recognize substantially less stains in an exemplary embodiment according to the present invention.

[0113] Also, in case 1 of the conventional liquid crystal display, compared with case 2 of an exemplary embodiment of the liquid crystal display, it is confirmed that the stains caused by the pressure are more continuously recognized at a low grayscale value. In one exemplary embodiment, for example, the stains caused by the pressure are recognized at a grayscale of less than 160 in case 1, while the stains caused by the pressure are not recognized at a grayscale of less than 160 in case 2. By this, it may be confirmed that the stains due to the pressure are not generated in the low grayscale in case 2 of the liquid crystal display according to the exemplary embodiment of the present invention compared with case 1 of the conventional liquid crystal display.

[0114] Also, when comparing the lines x1' and x2' and the lines y1' and y2', by comparing grayscale values corresponding to a same X-axis, it is confirmed that the stains caused by the pressure disappear in the upper grayscales in case 2. Accordingly, it is confirmed that the stains caused by the pressure more quickly disappear in case 2 compared with case 1 of the conventional liquid crystal display.

[0115] In FIG. 10, the lines xx1 and xx2 are curves showing grayscales when the stains caused by an impact, e.g., by being hit, are recognized in case 1 of the conventional liquid crystal display, and the lines yy1 and yy2 are curves showing grayscales when the stains caused by the impact are recognized in case 2 of an exemplary embodiment of the liquid crystal display.

[0116] Referring to FIG. 10, it is confirmed that the stains caused by the impact appear as a lower grayscale in case 2 than in case 1. Accordingly, it is confirmed that the stains caused by the impact are less generated at low grayscales in case 2 compared with case 1.

[0117] As described above, in an exemplary embodiment of the liquid crystal display, when compared with a conventional liquid crystal display, it is confirmed that the deterioration of the display quality due to external pressure is substantially decreased, and thereby display quality thereof is substantially improved.

[0118] The arrangements of signal lines and the pixels and the driving methods thereof of the liquid crystal displays according to the above-described exemplary embodiments may be applied to a pixel of all shapes including a first pixel electrode and a second pixel electrode of which at least portions are disposed in a same layer and are alternately disposed.

[0119] While this invention has been described in connection with what is presently considered to be practical exemplary embodiments, it is to be understood that the invention is not limited to the exemplary embodiments described herein, but, on the contrary, is intended to include various modifications within the scope of the appended claims.

Claims

1. A liquid crystal display comprising:

a first substrate (110);
a second substrate (210) disposed opposite to the first substrate;
a liquid crystal layer (300) interposed between the first substrate and the second substrate and including liquid crystal molecules (31);
a gate line (121) disposed on the first substrate, wherein the gate line is arranged to transmit a gate signal;
a plurality of data lines (171a, 171b, 171c) dis-

posed on the first substrate, wherein each data line is arranged to transmit a first voltage;
a voltage transmitting line (172) disposed on the first substrate, wherein the voltage transmitting line is arranged to transmit a second voltage;
a plurality of pixels (PX1, PX2, PX3) each comprising a first pixel electrode (191a) disposed on the first substrate (110), and a second pixel electrode (191b) disposed on the first substrate (110), the second pixel electrode (191b) being engaged with and spaced apart from the first pixel electrode (191a),
wherein one of the first pixel electrode (191a) and the second pixel electrode (191b) is arranged to be applied with the first voltage through one of the plurality of data lines (171a, 171b, 171c), the other of the first pixel electrode (191a) and the second pixel electrode (191b) is arranged to be applied with a second voltage through the voltage transmitting line (172),
wherein each of the first pixel electrode (191a) and the second pixel electrode (191b) includes stems (191a1, 191a3, 191b1, 191b3) and a plurality of branches (191a2, 191a4, 191b2, 191b4) extending from the stems (191a1, 191a3, 191b1, 191b3), and the branches (191a2, 191a4) of the first pixel electrode (191a) and the branches (191b2, 191b4) of the second pixel electrode (191b) are alternately disposed, and
the plurality of pixels (PX1, PX2, PX3) includes a first pixel (PX1) and a second pixel (PX2) neighboring each other in the gate line direction,
a data line (171a) of the plurality of data lines (171a, 171b, 171c) is disposed between the first pixel (PX1) and the second pixel (PX2),
a first stem (191a1) of the first pixel electrode (191a) of the second pixel (PX2) and a second stem (191b1) of the second pixel electrode (191b) of the first pixel (PX1) are arranged to be applied with the first voltage, overlap the data line (171a) disposed between the first pixel (PX1) and the second pixel (PX2), and are disposed opposite to each other with respect to the data line (171 a) disposed between the first pixel (PX1) and the second pixel (PX2),
a third stem (191a3) of the first pixel electrode (191a) of the first pixel (PX1) and a fourth stem (191b3) of the second pixel electrode (191b) of the second pixel (PX2) are arranged to be applied with the second voltage, overlap the data line (171a) disposed between the first pixel (PX1) and the second pixel (PX2), and are disposed opposite to each other with respect to the data line (171a) disposed between the first pixel (PX1) and the second pixel (PX2).

2. The liquid crystal display of claim 1, wherein
wherein the first stem (191a1) of the first pixel electrode (191a) and the fourth stem (191b3) of the second pixel electrode (191b) of the first pixel (PX1) overlap at least a portion of the voltage transmitting line (172).

3. The liquid crystal display of claim 2, wherein
the first stem (191a1) of the first pixel electrode (191a) and the fourth stem (191b3) of the second pixel electrode (191b) of the first pixel (PX1) together cover at least two thirds of the voltage transmitting line (172).

4. The liquid crystal display of claim 3,
wherein the voltage transmitting line (172) is arranged to supply the second voltage to three of the plurality of pixels (PX1, PX2, PX3).

5. The liquid crystal display of claim 1 or claim 4, wherein each of the pixels (PX1, PX2, PX3) comprises
a first region where the branches (191a2, 191a4) of the first pixel electrode (191a) and adjacent branches (191b2, 191b4) of the second pixel electrode (191b) are separated by a first interval; and
a second region where the branches (191a2, 191a4) of the first pixel electrode (191a) and the adjacent branches (191b2, 191b4) of the second pixel electrode (191b) are separated by a second interval,
wherein the first interval is greater than the second interval.

6. The liquid crystal display of claim 5, wherein
the liquid crystal molecules (31) of the liquid crystal layer (300) are vertically aligned when no electric field is applied to the liquid crystal layer.

7. The liquid crystal display of claim 6, wherein
the first pixel electrode (191 a) and the second pixel electrode (191b) are arranged to be applied with voltages having different polarities.

8. The liquid crystal display of claim 7, further comprising:

an third region where the branches (191a2, 191a4) of the first pixel electrode (191a) and the adjacent branches (191b2, 191b4) of the second pixel electrode (191b) are separated a thir interval, wherein the third interval is greater than the first interval.

9. The liquid crystal display of claim 1, wherein
the liquid crystal molecules (31) of the liquid crystal layer (300) are vertically aligned when no electric field is applied to the liquid crystal layer.

10. The liquid crystal display of claim 9, wherein
the first pixel electrode (191a) and the second pixel electrode (191b) are each arranged to be applied

with voltages having different polarities.

11. The liquid crystal display of claim 1, wherein the voltage transmitting line is arranged to supply the second voltage with a polarity that is changed per driving frame.

12. The liquid crystal display of claim 1,
wherein the third pixel (PX3) is disposed adjacent to the second pixel (PX2) along the gate line direction,
wherein each of the first pixel (PX1), the second pixel (PX2), and the third pixel (PX3) comprises a first thin film transistor and a second thin film transistor and has a first contact hole (185a) and a second contact hole (185b),
wherein the first pixel electrodes (191a) of the first pixel (PX1), the second pixel (PX2), and the third pixel (PX3) are connected to the first thin film transistors through the first contact holes (185a), and
wherein the first contact hole (185a) is disposed on a first side of the first thin film transistor in the first pixel (PX1) and the third pixel (PX2) and the first contact hole (185c) is disposed on a second side opposite to the first side of the first thin film transistor in the second pixel (PX2).

13. The liquid crystal display of claim 12,
wherein the second pixel electrodes (191b) of the first pixel (PX1), the second pixel (PX2), and the third pixel (PX3) are connected to the second thin film transistors through the second contact holes (185b), and
wherein the second contact hole (185b) is disposed on one side of the second thin film transistor in the first pixel (PX1) and the third pixel (PX3) and the second contact hole (185b) is disposed on the opposite side of the second thin film transistor in the second pixel (PX2).

14. The liquid crystal display of claim 13,
wherein the first contact hole (185a) is disposed on a first drain electrode (175a) of the first thin film transistor.

15. The liquid crystal display of claim 14,
wherein the second contact hole (185b) is disposed on a second drain electrode (175b) of the second thin film transistor.

16. The liquid crystal display of claim 15,
wherein at least one of the first drain electrode (175a) and the second drain electrode (175b) form a storage capacitor by overlapping a storage electrode (133a, 133b).

Patentansprüche

1. Flüssigkristallanzeige, umfassend:

ein erstes Substrat (110);
ein zweites Substrat (210), das gegenüber von dem ersten Substrat angeordnet ist;
eine Flüssigkristallschicht (300), die zwischen dem ersten Substrat und dem zweiten Substrat angeordnet ist und Flüssigkristallmoleküle (31) umfasst;
eine Gate-Leitung (121), die auf dem ersten Substrat angeordnet ist, wobei die Gate-Leitung dafür ausgelegt ist, ein Gate-Signal zu übertragen;
eine Vielzahl von Datenleitungen (171a, 171b, 171c), die auf dem ersten Substrat angeordnet sind, wobei jede Datenleitung dafür ausgelegt ist, eine erste Spannung zu übertragen;
eine Spannungsübertragungsleitung (172), die auf dem ersten Substrat angeordnet ist, wobei die Spannungsübertragungsleitung dafür ausgelegt ist, eine zweite Spannung zu übertragen;
eine Vielzahl von Pixeln (PX1, PX2, PX3), die jeweils Folgendes umfassen:

eine erste Pixelelektrode (191a), die auf dem ersten Substrat (110) angeordnet ist, und eine zweite Pixelelektrode (191b), die auf dem ersten Substrat (110) angeordnet ist, wobei die zweite Pixelelektrode (191b) in Eingriff mit der ersten Pixelelektrode (191a) ist und von dieser beabstandet ist;
wobei eine von der ersten Pixelelektrode (191a) und der zweiten Pixelelektrode (191b) dafür ausgelegt ist, durch eine der Vielzahl von Datenleitungen (171a, 171b, 171c) mit der ersten Spannung versorgt zu werden, wobei die andere von der ersten Pixelelektrode (191a) und der zweiten Pixelelektrode (191b) dafür ausgelegt ist, durch die Spannungsübertragungsleitung (172) mit einer zweiten Spannung versorgt zu werden;
wobei jede von der ersten Pixelelektrode (191a) und der zweiten Pixelelektrode (191b) Stämme (191a1, 191a3, 191b1, 191b3) und eine Vielzahl von Ästen (191a2, 191a4, 191b2, 191b4) umfasst, die sich ausgehend von den Stämmen (191a1, 191a3, 191b1, 191b3) erstrecken, und wobei die Äste (191a2, 191a4) der ersten Pixelelektrode (191a) und die Äste (191b2, 191b4) der zweiten Pixelelektrode (191b) alternierend angeordnet sind, und
wobei die Vielzahl von Pixeln (PX1, PX2, PX3) ein erstes Pixel (PX1) und ein zweites Pixel (PX2) umfasst, die in Richtung der Ga-

te-Leitung benachbart angeordnet sind;
wobei eine Datenleitung (171a) der Vielzahl von Datenleitungen (171a, 171b, 171c) zwischen dem ersten Pixel (PX1) und dem zweiten Pixel (PX2) angeordnet ist;
wobei ein erster Stamm (191a1) der ersten Pixelelektrode (191a) des zweiten Pixels (PX2) und ein zweiter Stamm (191b1) der zweiten Pixelelektrode (191b) des ersten Pixels (PX1) dafür ausgelegt sind, mit der ersten Spannung versorgt zu werden, die Datenleitung (171a) überlappen, die zwischen dem ersten Pixel (PX1) und dem zweiten Pixel (PX2) angeordnet ist, und in Bezug auf die Datenleitung (171a), die zwischen dem ersten Pixel (PX1) und dem zweiten Pixel (PX2) angeordnet ist, einander gegenüberliegend angeordnet sind;
wobei ein dritter Stamm (191a3) der ersten Pixelelektrode (191a) des ersten Pixels (PX1) und ein vierter Stamm (191b3) der zweiten Pixelelektrode (191b) des zweiten Pixels (PX2) dafür ausgelegt sind, mit der zweiten Spannung versorgt zu werden, die Datenleitung (171a) überlappen, die zwischen dem ersten Pixel (PX1) und dem zweiten Pixel (PX2) angeordnet ist, und in Bezug auf die Datenleitung (171a), die zwischen dem ersten Pixel (PX1) und dem zweiten Pixel (PX2) angeordnet ist, einander gegenüberliegend angeordnet sind.

2. Flüssigkristallanzeige nach Anspruch 1, wobei der erste Stamm (191a1) der ersten Pixelelektrode (191a) und der vierte Stamm (191b3) der zweiten Pixelelektrode (191b) des ersten Pixels (PX1) wenigstens einen Teil der Spannungsübertragungsleitung (172) überlappen.

3. Flüssigkristallanzeige nach Anspruch 2, wobei der erste Stamm (191a1) der ersten Pixelelektrode (191a) und der vierte Stamm (191b3) der zweiten Pixelelektrode (191b) des ersten Pixels (PX1) zusammen wenigstens zwei Drittel der Spannungsübertragungsleitung (172) überlappen.

4. Flüssigkristallanzeige nach Anspruch 3, wobei die Spannungsübertragungsleitung (172) dafür ausgelegt ist, die zweite Spannung zu drei der Vielzahl von Pixeln (PX1, PX2, PX3) zu liefern.

5. Flüssigkristallanzeige nach Anspruch 1 oder Anspruch 4, wobei jedes der Pixel (PX1, PX2, PX3) Folgendes umfasst:

einen ersten Bereich, wo die Äste (191a2, 191a4) der ersten Pixelelektrode (191a) und benachbarte Äste (191b2, 191b4) der zweiten Pixelelektrode (191b) durch einen ersten Zwischenraum getrennt sind; und
einen zweiten Bereich, wo die Äste (191a2, 191a4) der ersten Pixelelektrode (191a) und die benachbarten Äste (191b2, 191b4) der zweiten Pixelelektrode (191b) durch einen zweiten Zwischenraum getrennt sind;
wobei der erste Zwischenraum größer als der zweite Zwischenraum ist.

6. Flüssigkristallanzeige nach Anspruch 5, wobei die Flüssigkristallmoleküle (31) der Flüssigkristallschicht (300) vertikal ausgerichtet sind, wenn kein elektrisches Feld an die Flüssigkristallschicht angelegt wird.

7. Flüssigkristallanzeige nach Anspruch 6, wobei die erste Pixelelektrode (191a) und die zweite Pixelelektrode (191b) dafür ausgelegt sind, mit Spannungen versorgt zu werden, die unterschiedliche Polaritäten aufweisen.

8. Flüssigkristallanzeige nach Anspruch 7, ferner umfassend:

einen dritten Bereich, wo die Äste (191a2, 191a4) der ersten Pixelelektrode (191a) und die benachbarten Äste (191b2, 191b4) der zweiten Pixelelektrode (191b) durch einen dritten Zwischenraum getrennt sind, wobei der dritte Zwischenraum größer als der erste Zwischenraum ist.

9. Flüssigkristallanzeige nach Anspruch 1, wobei die Flüssigkristallmoleküle (31) der Flüssigkristallschicht (300) vertikal ausgerichtet sind, wenn kein elektrisches Feld an die Flüssigkristallschicht angelegt wird.

10. Flüssigkristallanzeige nach Anspruch 9, wobei die erste Pixelelektrode (191a) und die zweite Pixelelektrode (191b) jeweils dafür ausgelegt sind, mit Spannungen versorgt zu werden, die unterschiedliche Polaritäten aufweisen.

11. Flüssigkristallanzeige nach Anspruch 1, wobei die Spannungsübertragungsleitung dafür ausgelegt ist, die zweite Spannung mit einer Polarität zu liefern, die pro Treiberrahmen geändert wird.

12. Flüssigkristallanzeige nach Anspruch 1, wobei das dritte Pixel (PX3) entlang der Richtung der Gateleitung angrenzend an das zweite Pixel (PX2) angeordnet ist, wobei das erste Pixel (PX1), das zweite Pixel (PX2) und das dritte Pixel (PX3) jeweils einen ersten Dünnschichttransistor und einen zweiten Dünnschichttransistor umfassen und ein erstes Kontaktloch (185a) und ein zweites Kon-

taktloch (185b) aufweisen;
wobei die ersten Pixelelektroden (191a) des ersten Pixels (PX1), des zweiten Pixels (PX2) und des dritten Pixels (PX3) durch die ersten Kontaktlöcher (185a) mit den ersten Dünnschichttransistoren verbunden sind; und
wobei das erste Kontaktloch (185a) an einer ersten Seite des ersten Dünnschichttransistors in dem ersten Pixel (PX1) und dem dritten Pixel (PX2) angeordnet ist und wobei das erste Kontaktloch (185c) an einer zweiten Seite angeordnet ist, die der ersten Seite des ersten Dünnschichttransistors in dem zweiten Pixel (PX2) entgegengesetzt ist.

13. Flüssigkristallanzeige nach Anspruch 12,
wobei die zweiten Pixelelektroden (191b) des ersten Pixels (PX1), des zweiten Pixels (PX2) und des dritten Pixels (PX3) durch die zweiten Kontaktlöcher (185b) mit den zweiten Dünnschichttransistoren verbunden sind; und
wobei das zweite Kontaktloch (185b) an einer Seite des zweiten Dünnschichttransistors in dem ersten Pixel (PX1) und dem dritten Pixel (PX3) angeordnet ist und wobei das zweite Kontaktloch (185b) an der entgegengesetzten Seite des zweiten Dünnschichttransistors in dem zweiten Pixel (PX2) angeordnet ist.

14. Flüssigkristallanzeige nach Anspruch 13,
wobei das erste Kontaktloch (185a) an einer ersten Drain-Elektrode (175a) des ersten Dünnschichttransistors angeordnet ist.

15. Flüssigkristallanzeige nach Anspruch 14,
wobei das zweite Kontaktloch (185b) an einer zweiten Drain-Elektrode (175b) des zweiten Dünnschichttransistors angeordnet ist.

16. Flüssigkristallanzeige nach Anspruch 15,
wobei mindestens eine von der einer ersten Drain-Elektrode (175a) und der zweiten Drain-Elektrode (175b) einen Speicherkondensator bildet, indem sie eine Speicherelektrode (133a, 133b) überlappt.

Revendications

1. Afficheur à cristaux liquides comprenant :

un premier substrat (110) ;
un deuxième substrat (210) disposé face au premier substrat ;
une couche de cristaux liquides (300) interposée entre le premier substrat et le deuxième substrat et contenant des molécules de cristaux liquides (31) ;
une ligne de grille (121) disposée sur le premier substrat, laquelle ligne de grille est conçue pour transmettre un signal de grille ;
une pluralité de lignes de données (171a, 171b, 171c) disposées sur le premier substrat, chacune des lignes de données étant conçue pour transmettre une première tension ;
une ligne de transmission de tension (172) disposée sur le premier substrat, laquelle ligne de transmission de tension est conçue pour transmettre une deuxième tension ;
une pluralité de pixels (PX1, PX2, PX3) comprenant chacun une première électrode de pixel (191a) disposée sur le premier substrat (110) et une deuxième électrode de pixel (191b) disposée sur le premier substrat (110), la deuxième électrode de pixel (191b) étant en prise avec et espacée de la première électrode de pixel (191a),
dans lequel la première électrode de pixel (191a) ou la deuxième électrode de pixel (191b) est conçue pour recevoir la première tension via l'une de la pluralité de lignes de données (171a, 171b, 171c), l'autre des première (191a) et deuxième (191b) électrodes de pixel étant conçue pour recevoir une deuxième tension via la ligne de transmission de tension (172),
dans lequel la première électrode de pixel (191a) et la deuxième électrode de pixel (191b) comprennent chacune des troncs (191a1, 191a3, 191b1, 191b3) et une pluralité de branches (191a2, 191a4, 191b2, 191b4) s'étendant à partir des troncs (191a1, 191a3, 191b1, 191b3), et les branches (191a2, 191a4) de la première électrode de pixel (191a) et les branches (191b2, 191b4) de la deuxième électrode de pixel (191b) sont disposées alternativement, et
la pluralité de pixels (PX1, PX2, PX3) comprend un premier pixel (PX1) et un deuxième pixel (PX2) voisins l'un de l'autre dans la direction de la ligne de grille,
une ligne de données (171a) de la pluralité de lignes de donnés (171a, 171b, 171c) est disposée entre le premier pixel (PX1) et le deuxième pixel (PX2),
un premier tronc (191a1) de la première électrode de pixel (191a) du deuxième pixel (PX2) et un deuxième tronc (191b1) de la deuxième électrode de pixel (191b) du premier pixel (PX1) sont conçus pour recevoir la première tension, chevauchent la ligne de données (171a) disposée entre le premier pixel (PX1) et le deuxième pixel (PX2), et sont disposés l'un en face de l'autre par rapport à la ligne de données (171a) disposée entre le premier pixel (PX1) et le deuxième pixel (PX2),
un troisième tronc (191a3) de la première électrode de pixel (191a) du premier pixel (PX1) et un quatrième tronc (191b3) de la deuxième élec-

trode de pixel (191b) du deuxième pixel (PX2) sont conçus pour recevoir la deuxième tension, chevauchent la ligne de données (171a) disposée entre le premier pixel (PX1) et le deuxième pixel (PX2), et sont disposés l'un en face de l'autre par rapport à la ligne de données (171a) disposée entre le premier pixel (PX1) et le deuxième pixel (PX2).

2. Afficheur à cristaux liquides selon la revendication 1, dans lequel le premier tronc (191a1) de la première électrode de pixel (191a) et le quatrième tronc (191b3) de la deuxième électrode de pixel (191b) du premier pixel (PX1) chevauchent au moins une partie de la ligne de transmission de tension (172).

3. Afficheur à cristaux liquides selon la revendication 2, dans lequel le premier tronc (191a1) de la première électrode de pixel (191a) et le quatrième tronc (191b3) de la deuxième pixel (191b) du premier pixel (PX1) couvrent ensemble au moins les deux tiers de la ligne de transmission de tension (172).

4. Afficheur à cristaux liquides selon la revendication 3, dans lequel la ligne de transmission de tension (172) est conçue pour fournir la deuxième tension à trois des pixels de la pluralité de pixels (PX1, PX2, PX3).

5. Afficheur à cristaux liquides selon la revendication 1 ou 4, dans lequel chacun des pixels (PX1, PX2, PX3) comprend
une première région dans laquelle les branches (191a2, 191a4) de la première électrode de pixel (191a) et les branches (191b2, 191b4) adjacentes de la deuxième électrode de pixel (191b) sont séparées par un premier intervalle et
une deuxième région dans laquelle les branches (191a2, 191a4) de la première électrode de pixel (191a) et les branches (191b2, 191b4) adjacentes de la deuxième électrode de pixel (191b) sont séparées par un deuxième intervalle,
le premier intervalle étant plus grand que le deuxième intervalle.

6. Afficheur à cristaux liquides selon la revendication 5, dans lequel les molécules de cristaux liquides (31) de la couche de cristaux liquides (300) sont alignés verticalement quand aucun champ électrique n'est appliqué à la couche de cristaux liquides.

7. Afficheur à cristaux liquides selon la revendication 6, dans lequel la première électrode de pixel (191a) et la deuxième électrode de pixel (191b) sont conçues pour recevoir des tensions de polarité différente.

8. Afficheur à cristaux liquides selon la revendication 7, comprenant en outre une troisième région dans laquelle les branches (191a2, 191a4) de la première électrode de pixel (191a) et les branches (191b2, 191b4) adjacentes de la deuxième électrode de pixel (191b) sont séparées par un troisième intervalle, le troisième intervalle étant plus grand que le premier intervalle.

9. Afficheur à cristaux liquides selon la revendication 1, dans lequel les molécules de cristaux liquides (31) de la couche de cristaux liquides (300) sont alignées verticalement quand aucun champ électrique n'est appliqué à la couche de cristaux liquides.

10. Afficheur à cristaux liquides selon la revendication 9, dans lequel la première électrode de pixel (191a) et la deuxième électrode de pixel (191b) sont conçues chacune pour recevoir des tensions de polarité différente.

11. Afficheur à cristaux liquides selon la revendication 1, dans lequel la ligne de transmission de tension est conçue pour fournir la deuxième tension sous une polarité qui change à chaque trame d'excitation.

12. Afficheur à cristaux liquides selon la revendication 1, dans lequel le troisième pixel (PX3) est adjacent au deuxième pixel (PX2) dans la direction de la ligne de grille, le premier pixel (PX1), le deuxième pixel (PX2) et le troisième pixel (PX3) comprenant chacun un premier transistor à couches minces et un deuxième transistor à couches minces et possédant un premier trou de contact (185a) et un deuxième trou de contact (185b),
dans lequel les premières électrodes de pixel (191a) du premier pixel (PX1), du deuxième pixel (PX2) et du troisième pixel (PX3) sont connectées aux premiers transistors à couches minces via les premiers trous de contact (185a), et
dans lequel le premier trou de contact (185a) est disposé sur un premier côté du premier transistor à couches minces dans le premier pixel (PX1) et le troisième pixel (PX2) et le premier trou de contact (185c) est disposé sur un deuxième côté opposé au premier côté du transistor à couches minces dans le deuxième pixel (PX2).

13. Afficheur à cristaux liquides selon la revendication 12,
dans lequel les deuxièmes électrodes de pixel (191b) du premier pixel (PX1), du deuxième pixel (PX2) et du troisième pixel (PX3) sont connectées aux deuxièmes transistors à couche mince via les deuxièmes trous de contact (185b), et
dans lequel le deuxième trou de contact (185b) est disposé sur un côté du deuxième transistor à couches minces dans le premier pixel (PX1) et le troisième pixel (PX3) et le deuxième trou de contact

(185b) est disposé sur le côté opposé du deuxième transistor à couches minces dans le deuxième pixel (PX2).

14. Afficheur à cristaux liquides selon la revendication 13, dans lequel le premier trou de contact (185a) est disposé sur une première électrode de drain (175a) du premier transistor à couches minces.

15. Afficheur à cristaux liquides selon la revendication 14, dans lequel le deuxième trou de contact (185b) est disposé sur une deuxième électrode de drain (175b) du deuxième transistor à couches minces.

16. Afficheur à cristaux liquides selon la revendication 15, dans lequel au moins une des première (175a) et deuxième (175b) électrodes de drain forme une capacité de stockage en chevauchant une électrode de stockage (133a, 133b).

FIG. 1

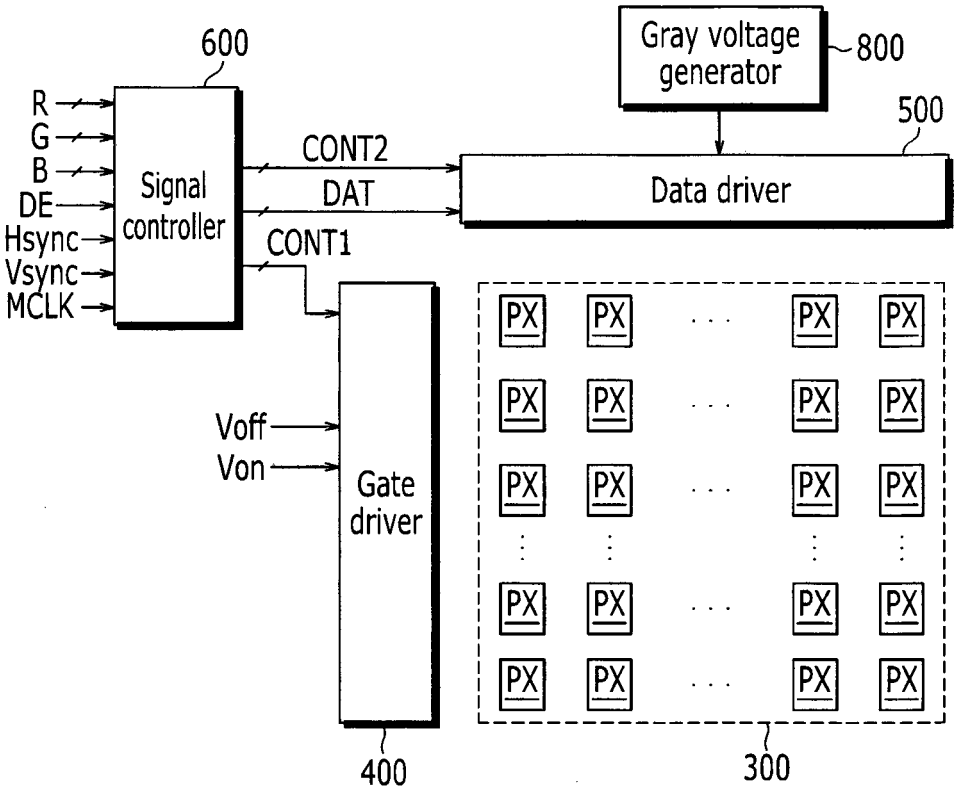

600
Gray voltage generator
800
500
R
G
B
DE
Hsync
Vsync
MCLK
Signal controller
CONT2
DAT
Data driver
CONT1
Voff
Von
Gate driver
PX
400
300

FIG. 2

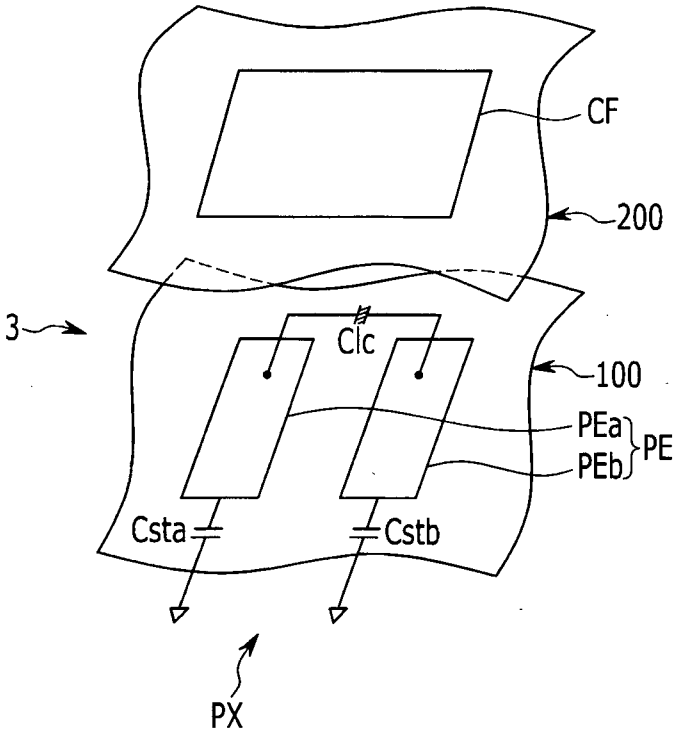


FIG. 3

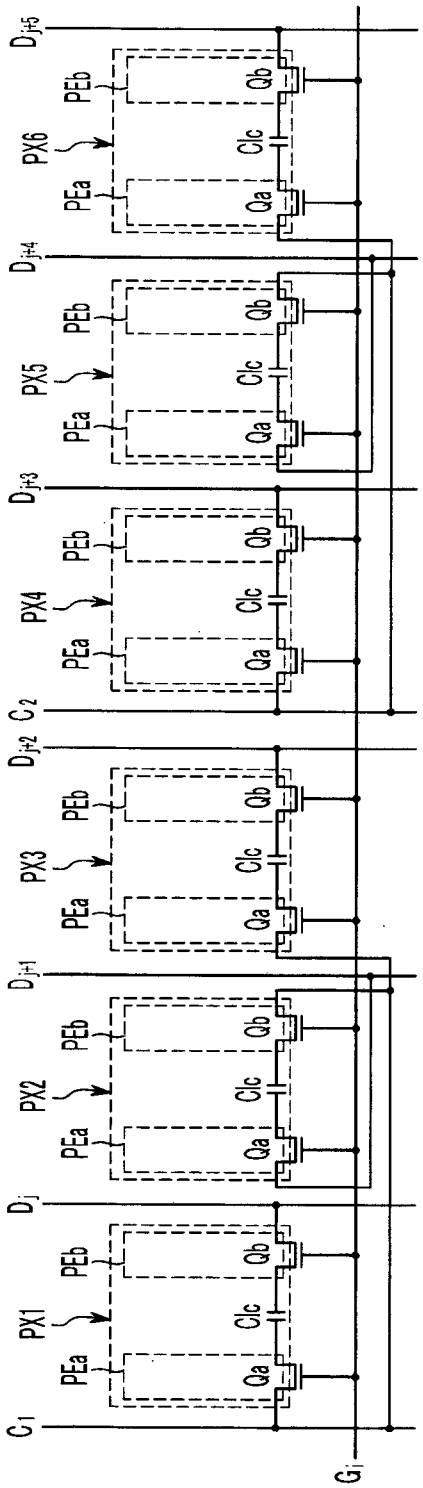

D_{j+5}
D_{j+4}
D_{j+3}
D_{j+2}
D_{j+1}
D_j
C_1
C_2
G_i
PX1
PX2
PX3
PX4
PX5
PX6
PEa
PEb
Qa
Qb
Clc

FIG. 4

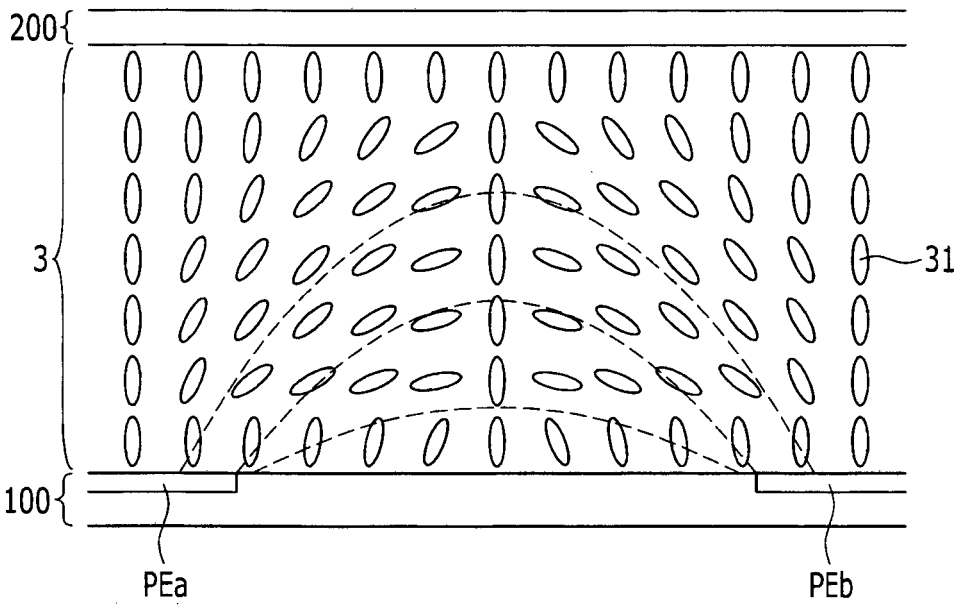


FIG. 5

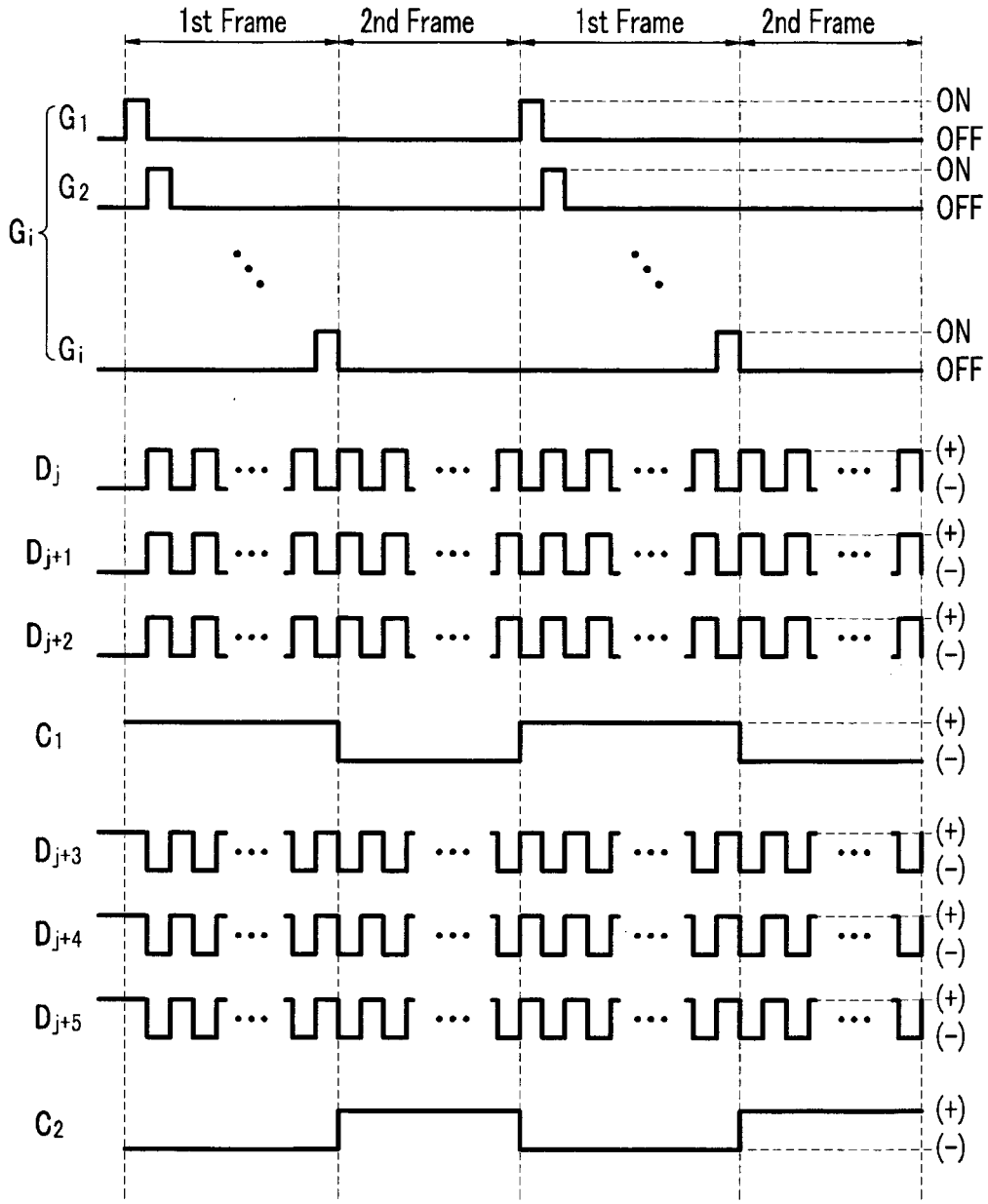

1st Frame
2nd Frame
1st Frame
2nd Frame
G1
G2
Gi
Gi
ON
OFF
ON
OFF
ON
OFF
Dj
Dj+1
Dj+2
C1
Dj+3
Dj+4
Dj+5
C2
(+)
(-)

FIG. 6

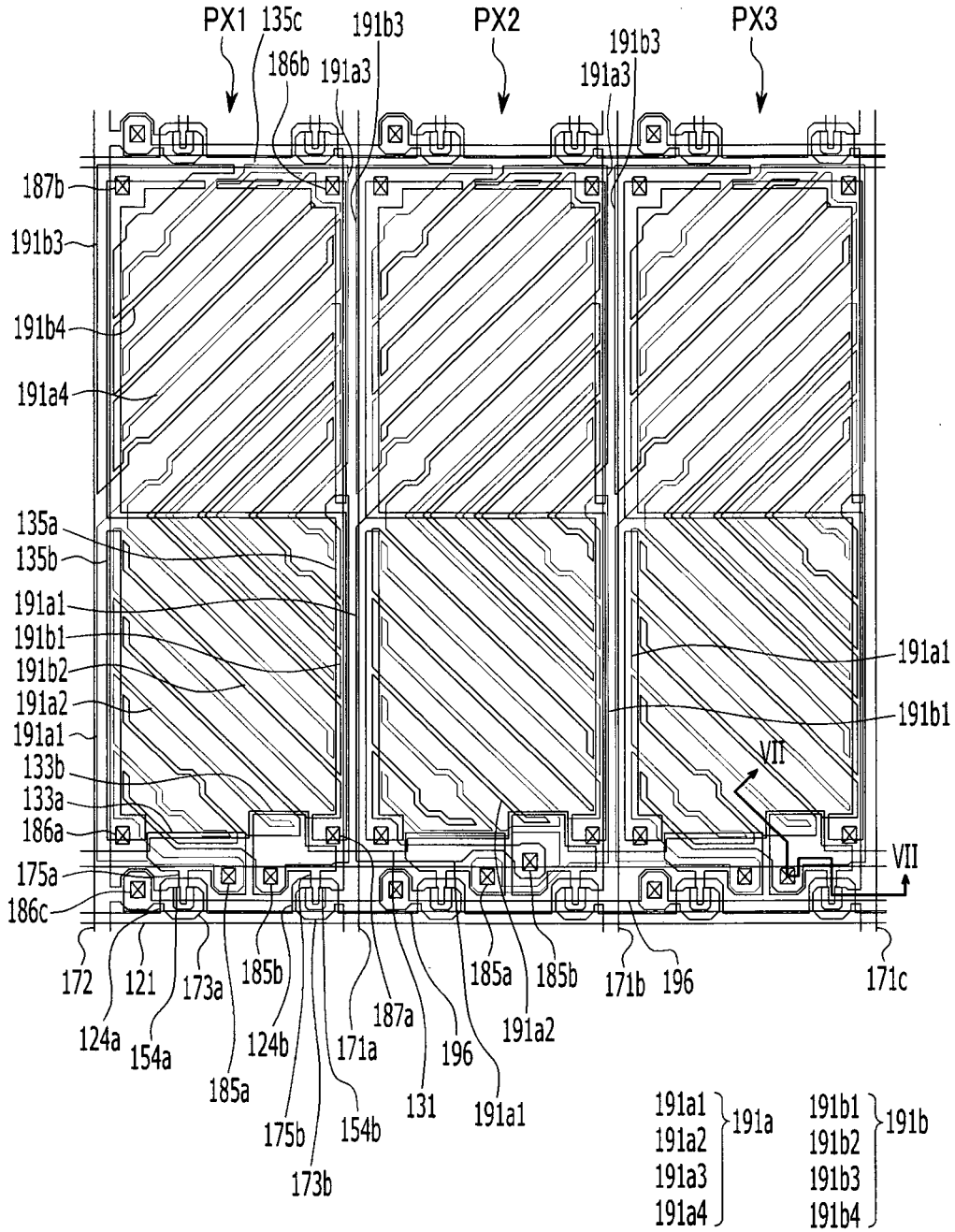

PX1
135c
191b3
186b
191a3
PX2
191b3
191a3
PX3
187b
191b3
191b4
191a4
135a
135b
191a1
191b1
191b2
191a2
191a1
133b
133a
186a
175a
186c
191a1
191b1
VII
VII
172
121
173a
185b
185a
185b
171b
196
171c
124a
154a
185a
124b
171a
187a
196
191a2
175b
154b
131
191a1
173b
191a1
191a2
191a3
191a4
191a
191b1
191b2
191b3
191b4
191b

FIG. 7

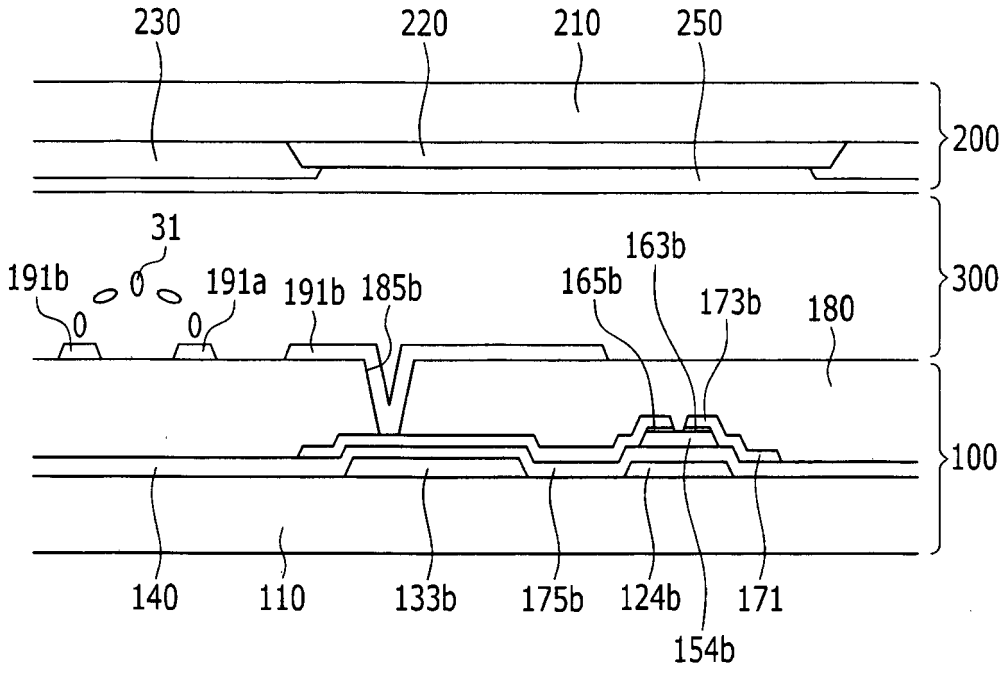

230
220
210
250
200
31
191b
191a
191b
185b
163b
165b
173b
180
300
100
140
110
133b
175b
124b
171
154b

FIG. 8A

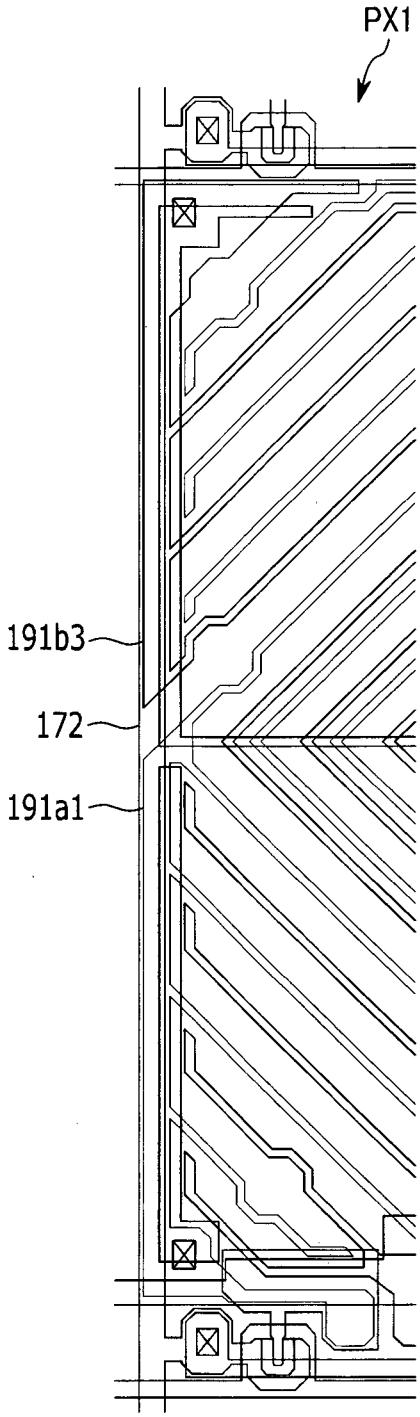


FIG. 8B

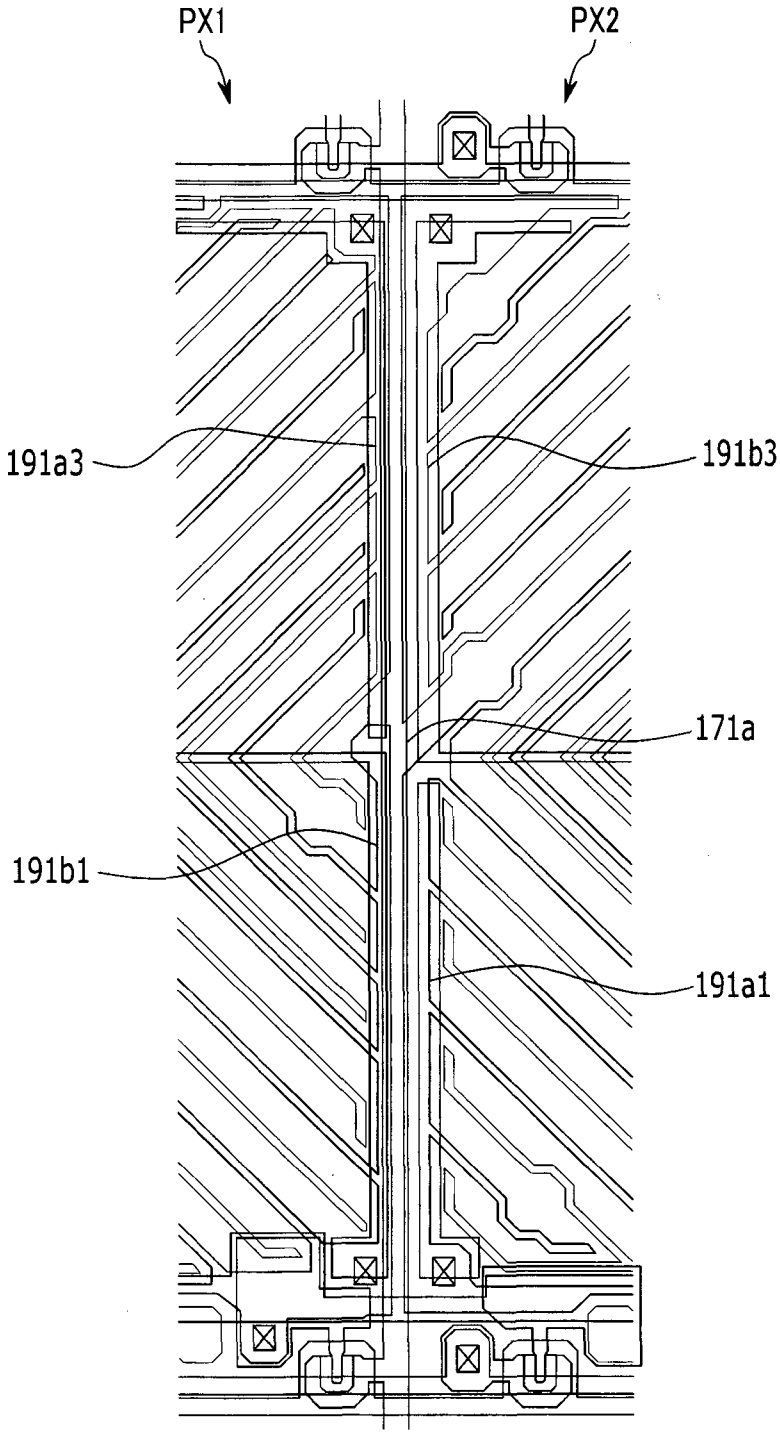


FIG. 8C

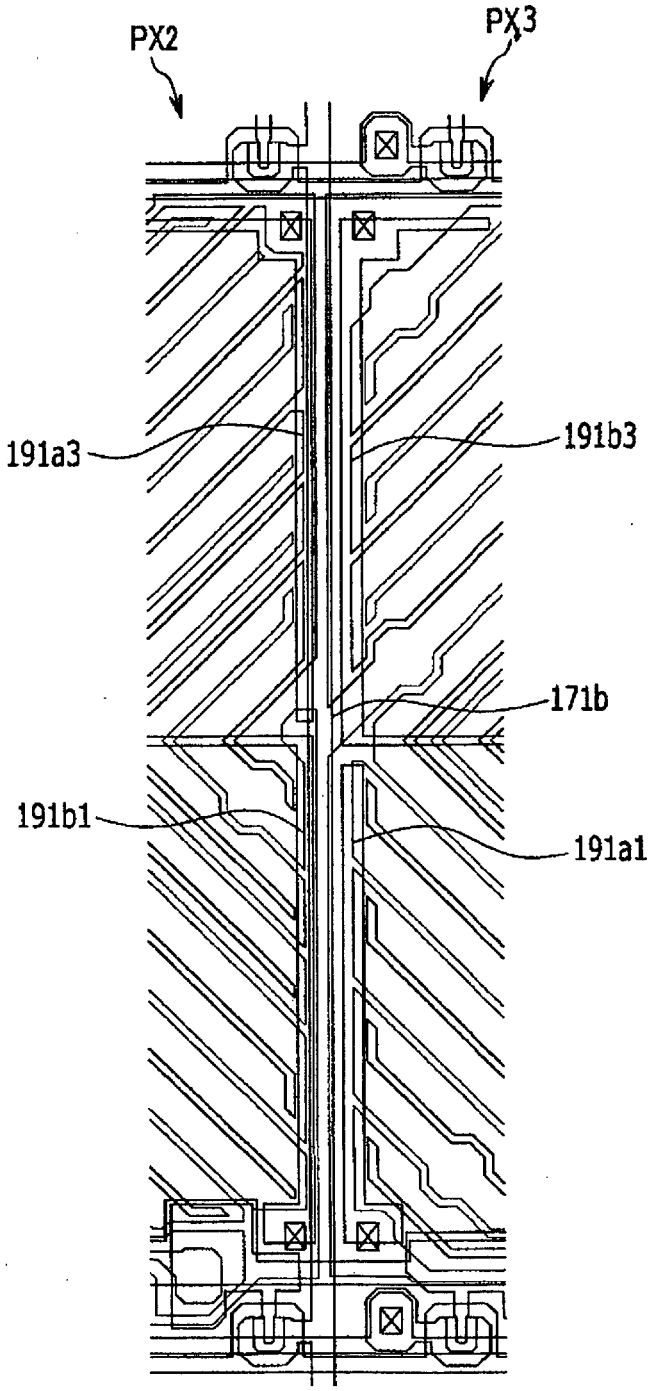
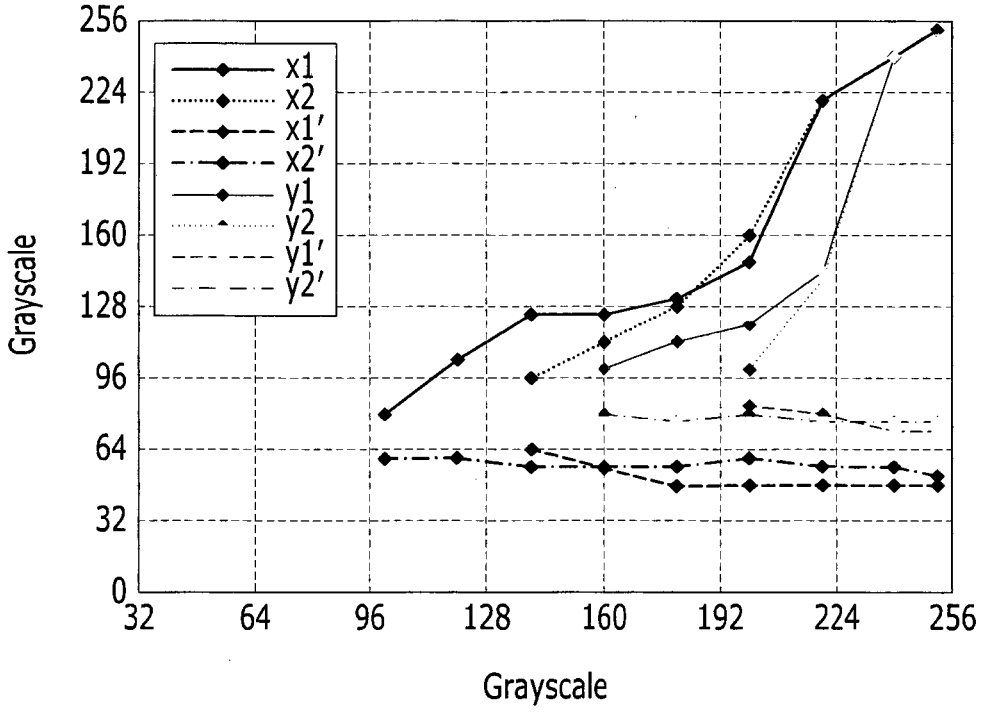


FIG. 9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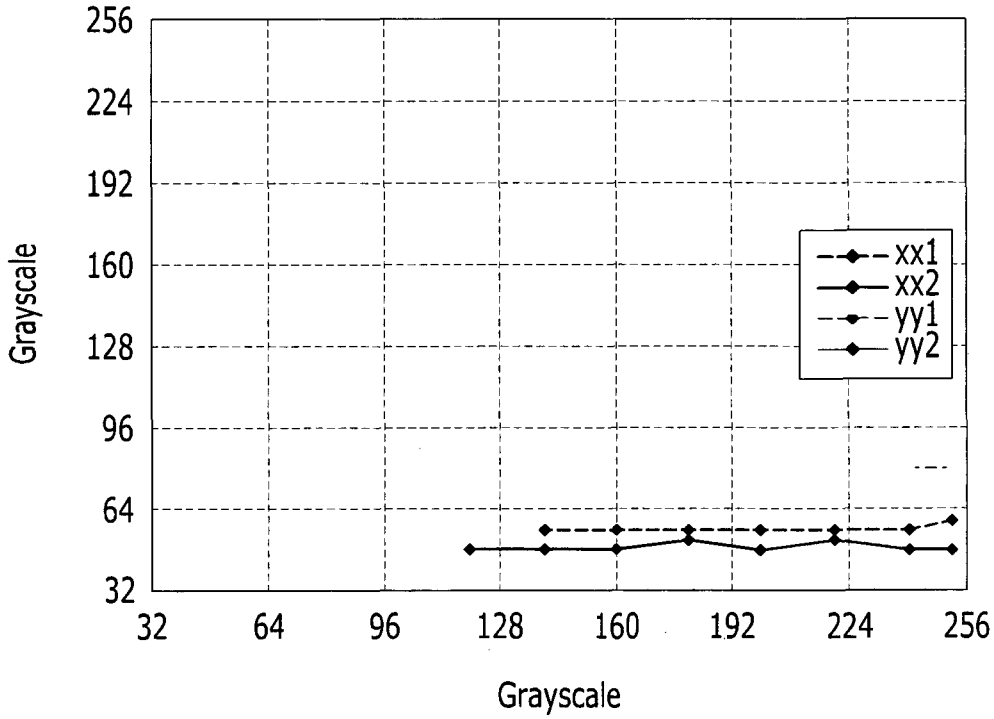
192
160
128
96
64
32
0
Grayscale
x1
x2
x1'
x2'
y1
y2
y1'
y2'
32
64
96
128
160
192
224
256
Grayscale

FIG. 10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32
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96
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224
256
Grayscale
xx1
xx2
yy1
yy2

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- US 20090310047 A1 **[0005]**
- US 20070182902 A1 **[0005]**

专利名称(译)	液晶显示器		
公开(公告)号	EP2482125B1	公开(公告)日	2013-11-20
申请号	EP2011183643	申请日	2011-09-30
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IPC分类号	G02F1/1343 G02F1/139		
CPC分类号	G02F1/134363 G02F1/13624 G02F1/1395 G02F2001/13606 G02F2201/40		
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优先权	1020110008627 2011-01-28 KR		
其他公开文献	EP2482125A1		
外部链接	Espacenet		

摘要(译)

液晶显示器包括：彼此相对的第一和第二基板（110,210）;传输第一电压的第一基板上的数据线（171a-c）;第一基板上的电压传输线（172），其传输第二电压;第一和第二像素电极（191a，191b）在第一基板上并彼此间隔开，其中第一和第二像素电极中的一个通过数据线施加第一电压，第一和第二像素中的另一个通过电压传输线向第二电压施加电极，第一和第二像素电极中的每一个包括从杆延伸的杆（191a1, 191a3; 191b1,191b3）和分支（191a2,191a4; 191b2,191b4），第一像素电极的分支和第二像素电极的分支交替设置，并且施加有第一电压的第一像素（PX1）和相邻的第二像素（PX1）的第一和第二像素电极的主干被设置相对于设置在第一像素和第二像素之间的数据线（171a）彼此相对。

FIG. 1