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(54) **Liquid crystal display device**

Flüssigkristallanzeigevorrichtung

Dispositif d'affichage à cristaux liquides

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EP 2 466 365 B1

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Description

FIELD OF THE INVENTION

[0001] The present invention relates to a display device, and more particularly, to a liquid crystal display device designed to prevent peeling of a film formed on an organic passivation film. A liquid crystal display device as described in the preamble portions of claims 1, 2, and 4 has been known from JP 2009-271103 A.

BACKGROUND OF THE INVENTION

[0002] A liquid crystal display device includes a TFT substrate in which pixels each having a pixel electrode, a thin film transistor (TFT), and the like are arranged in a matrix form. Further, a counter substrate is disposed opposite to the TFT substrate, in which color filters and the like are formed at positions corresponding to the pixel electrodes of the TFT substrate. A liquid crystal is interposed between the TFT substrate and the counter substrate. Then, the light transmittance is controlled by liquid crystal molecules in each pixel to form an image.

[0003] The use of liquid crystal display devices is growing in various fields due to its flatness and lightweight. Small-sized liquid crystal display devices are widely used in mobile phones and digital still cameras (DSCs). In the liquid crystal display device, the viewing angle characteristics are a problem. The viewing angle is a phenomenon in which the brightness changes or the color changes between when the display is viewed from the front and when the display is viewed from an oblique direction. The viewing angle characteristics are excellent in the inplane switching (IPS) mode for driving liquid crystal molecules by the electric field in the horizontal direction.

[0004] There are many different types of IPS modes. For example, a common electrode is formed in a planar shape, on which a pixel electrode having a slit is provided with an insulating film interposed therebetween, to rotate liquid crystal molecules by the electric field generated between the pixel electrode and the common electrode. This type can increase the light transmittance, and is now a mainstream IPS mode. An organic passivation film is used for flattening the base on which the common electrode is formed. However, the organic passivation film is highly hygroscopic and absorbs water from the air when it is left outside. Then, in the film formation, the water absorbed by the organic passivation film is released during heat treatment. This affects the film formed on the organic passivation film, causing it to peel off.

[0005] As a method to solve such a problem, JP 2009-271103 A describes a configuration in which an interlayer insulating film is formed on an organic passivation film on an image signal line, and a through hole is formed along the image signal line in the interlayer insulating film to allow gas present in the organic passivation film to be released from the through hole. Further, in JP 2009-271103 A, the through hole is covered by a transparent electrode that is electrically connected to the common electrode.

[0006] More concretely, JP 2009-271103 A discloses a liquid crystal display device comprising a pixel electrode in an area surrounded by scan lines extending in a first direction and arranged in a second direction and by image signal lines extending in the second direction and arranged in the first direction, wherein the pixel electrode is supplied with an image signal from the image signal line through a TFT, wherein the TFT includes a semiconductor layer having a channel portion, a drain portion formed on the side of the image signal line, and a source portion formed on the side of the pixel electrode, wherein a gate insulating film is formed so as to cover the semiconductor layer, wherein a gate electrode is formed on the gate insulating film above the channel portion, and wherein a first interlayer insulating film is formed so as to cover the gate electrode.

[0007] In order to describe the problem in the related art, first the cross-sectional structure of an IPS liquid crystal display device will be described. Fig. 9 is a cross-sectional view showing the structure of a pixel portion of a display area 10 of the liquid crystal display device. Note that the cross-sectional view of Fig. 9 is an example of the basic structure, and does not correspond one-to-one to the figures such as Fig. 2 which is a top view of an embodiment of the present invention described below. As shown in Fig. 9, the liquid crystal display device to which the present invention is applied is a top-gate TFT using poly-Si for a semiconductor layer 103. In Fig. 9, a first, base film 101 of SiN and a second base film 102 of SiO_2 are formed on a glass substrate 100 by chemical vapor deposition (CVD). The role of the first base film 101 and the second base film 102 is to prevent the semiconductor layer 103 from being contaminated with impurities from the glass substrate 100.

[0008] The semiconductor layer 103 is formed on the second base film 102. In order to form the semiconductor layer 103, a-Si film is formed on the second base film 102 by CVD, which is then converted into poly-Si film by laser annealing. Then, the poly-Si film is patterned by photolithography.

[0009] A gate insulating film 104 is formed on the semiconductor film. The gate insulating film 104 is SiO_2 film derived from tetraethyl orthosilicate (TEOS). This film is also formed by CVD. Then, a gate electrode 105 is formed on the gate insulating film 104. The gate electrode 105 is formed on the same layer as a scan signal 30 at the same time. For example, the gate electrode 105 is formed from MoW film. When it is necessary to reduce the resistance of the scan line 30, Al alloy is used.

[0010] The gate electrode 105 is patterned by photolithography. At the time of patterning, impurities such as phosphor or boron are doped in the poly-Si layer to form a source S or drain D in the poly-Si layer. Further, a lightly doped drain (LDD) layer is formed between a channel layer of the poly-Si layer, and the source S or drain D by using the photoresist in patterning the gate electrode 105.

[0011] Then, a first interlayer insulating film 106 is formed of SiO_2 so as to cover the gate electrode 105. The role of the first interlayer insulating film 106 is to provide electrical insulation between the gate line 105 and a source electrode 107. The source electrode 107 is formed on the first interlayer insulating film 106. The source electrode 107 is connected to the pixel electrode 112 through a contact hole 130. In Fig. 9, the source electrode 107 is made wide enough to cover the TFT. The drain D of the TFT is connected to the image signal line at a point not shown.

[0012] The source electrode 107 is formed on the same layer as the image signal line at the same time. In order to reduce the resistance, AlSi alloy is used for the source electrode 107 or the image signal line. In the AlSi alloy, hillock formation occurs or Al diffuses into other layers. In order to prevent such a phenomenon, AlSi is sandwiched by a barrier layer of MoW and a cap layer. Alternatively, Mow or MoCr may be used instead of using Al.

[0013] The source electrode 107 and the source S of the TFT are connected to each other through the contact hole 130 formed in the gate insulating film 104 and the first interlayer insulating film 106. An inorganic passivation film 108 is formed and covers the source electrode 107 so as to protect the entire TFT. Similarly to the first base film 101, the inorganic passivation film 108 is formed by CVD.

[0014] An organic passivation film 109 is formed so as to cover the inorganic passivation film 108. The organic passivation film 109 is formed of a photosensitive acrylic resin. Examples of the material of the organic passivation film, in addition to the acrylic resin, are a silicone resin, epoxy resin, and polyimide resin. The organic passivation film 109, which has a role of a flattening film, is made thick. The thickness of the organic passivation film 109 is 1 to 4 μm, and in most cases, about 2 μm.

[0015] The contact hole 130 is formed in the inorganic passivation film 108 and in the organic passivation film 109 to provide electrical continuity between a pixel electrode 110 and the source electrode 107. The photosensitive resin used as the organic passivation film 109 is applied and then exposed. In this way, only the portion exposed by light is dissolved with a specific developer. In other words, when the photosensitive resin is used, the formation of photoresist can be omitted. After the contact hole is formed in the organic passivation film 109, the organic passivation film 109 is annealed at about 230 °C. Thus, the organic passivation film 109 is completed.

[0016] The organic passivation film 109 is dry etched using the resist as a mask, in order to form the contact hole in the inorganic passivation film 108. In this way, the contact hole 130 is formed to provide electrical continuity between the source electrode 107 and the pixel electrode 110.

[0017] The top surface of the organic passivation film 109 formed as described above is flat. Amorphous indium-tin-oxide (ITO) is deposited by sputtering on the top of the organic passivation film 109, and then patterned using photoresist. Then, the ITO is etched by sulfuric acid to pattern the common electrode 110. The common electrode 110 is formed in a planner shape, avoiding the contact hole 130. Then, the ITO is polycrystallized by annealing at 230 °C in order to reduce the electrical resistance. The common electrode 110 is formed of ITO which is a transparent electrode. The thickness of the common electrode 110 is, for example, 77 μm.

[0018] Then, a second interlayer insulating film 111 is formed by CVD so as to cover the common electrode 110. At this time, the temperature condition of CVD is about 230 °C, which is called low temperature CVD. Then, the second interlayer insulating film 111 is patterned by photolithography process. In Fig. 9, the second interlayer insulating film 111 does not cover the side wall of the contact hole 130. However, it is also possible that the second interlayer insulating film 111 covers the side wall of the contact hole 130.

[0019] The other films, such as the first base film 101 and the inorganic passivation film 108 are formed by CVD at a temperature of 300 °C or more. In general, the higher the temperature at which a CVD film and the like is formed the greater the adhesion to the base film. However, the organic passivation film 109 has been formed below the second interlayer insulating film 111. Thus, the characteristics of the organic passivation film 109 may be changed when the temperature is 230 °C or higher. For this reason, the second interlayer insulting film 111 is formed by low temperature CVD. When the second interlayer insulating film 111 is formed by low temperature CVD, there is a problem with the adhesion of the organic passivation film 109 to the other film, in particular to the common electrode 110 or the second interlayer insulating film 111.

[0020] The pixel electrode 112 having a slit 115 is formed by sputtering the amorphous ITO on the second interlayer insulating film 111 through a photolithography process. The pixel electrode 112 is connected to the source electrode 107 through the contact hole 130. When a signal voltage is applied to the pixel electrode 112, electric field lines are generated between the common electrode 110 and the pixel electrode 112 through the slit 115. The electric field rotates the liquid crystal molecules, thereby controlling the transmittance of light from a backlight for each pixel to form an image. The pixel electrode 112 is formed of ITO which is a transparent conductive film. The thickness of the pixel electrode 112 is, for example, in the range of 40 nm to 70 nm. An oriented film 113 is formed so as to cover the pixel electrode 112.

[0021] A counter substrate 200 is provided with a liquid crystal layer 300 interposed between the TFT substrate 100 and the counter substrate 200. A color filter 201 is formed within the counter substrate 200. The color filter 201 includes color filters of red, green, and blue in each pixel to form a color image. A black matrix 202 is formed between the color filters 201 to increase the contrast of the image. Note that the black matrix 202 also has a role as a light shielding film of the TFT to prevent the photo-

current from flowing into the TFT.

[0022] An overcoat film 203 is formed so as to cover the color filters 201 and the black matrix 202. The surface of the color filters 201 and the black matrix 202 is rough. Thus, the surface is flattened by the overcoat film 203. The oriented film 113 is formed on the overcoat film 203 for the initial orientation of the liquid crystal molecules. Note that Fig. 2 shows the case of the IPS, so that a counter electrode is formed on the side of the TFT substrate 100 but not on the side of the counter substrate.

[0023] As shown in Fig. 9, in the case of the IPS, the conductive film is not formed inside the counter substrate 200. As a result, the potential of the counter substrate 200 becomes unstable. In addition, external electromagnetic noise enters the liquid crystal layer 300 and affects the image. These problems eliminate by forming an external conductive film 210 on the outside of the counter substrate 200. The external conductive film 210 is formed by sputtering the ITO which is the transparent conductive film.

[0024] As described above, the second interlayer insulating film formed on the organic passivation film is deposited by low temperature CVD at about 230 °C. Thus, the adhesion of the second interlayer insulating film to the base film is low. The organic passivation film, which is formed below the second interlayer insulating film, absorbs water from the air when it is left outside. Then, when the organic passivation film is annealed to form various films on the organic passivation film, the water absorbed by the organic passivation film is released. At this time, the second interlayer insulating film peels off due to its low adhesion.

[0025] In order to solve the above problem, JP 2009-271103 A describes a configuration in which a thin through hole is formed in the second interlayer insulating film and along the image signal line, so that the water absorbed by the organic passivation film is let out from the through hole. Further, in JP 2009-271103 A, the through hole is covered by the ITO film. The ITO film is electrically connected to the common electrode so as to have the shielding effect.

[0026] However, JP 2009- 271103 A has the following problem. That is, the second interlayer insulating film is formed by low temperature CVD, so that the film structure is less precise than the film structure formed by high temperature CVD. Thus, when the contact hole is formed along the image signal by etching, the width of the though hole is not stabilized because of the unstable etching rate. As a result, the through hole is very likely to reach the pixel electrode. When the through hole reaches the pixel electrode, the disturbance of the electric field occurs in this portion of the pixel electrode, in which the liquid crystal molecules may not be controlled adequately. As a result, light leakage or other failure occurs. In addition, when the through hole is covered by the ITO film electrically connected to the common electrode, the pixel electrode and the common electrode are electrically connected to each other. As a result, the pixel is faulty.

[0027] Another problem of JP 2009-271103 A is that when the through hole is formed in the second interlayer insulating film, its effect is reduced by covering the through hole formed along the image signal line by the ITO. In other words, also when the pixel electrode of ITO is formed on the second interlayer insulating film, the ITO film is annealed at 230 °C to reduce the resistance of the ITO. At the same time, the oriented film is also annealed to be imidized. Thus, the water absorbed by the organic passivation film is released when the ITO and oriented films are formed. For this reason, it is necessary to effectively release the water from the through hole formed in the second interlayer insulating film.

SUMMARY OF THE INVENTION

[0028] It is the object of the present invention to solve the above problems, and to prevent the second insulating film from peeling off, without reducing the process latitude and without degrading the image quality.

[0029] According to the present invention these objects are accomplished with a liquid crystal display device according to claims 1, 3, 5 and 6.

[0030] Dependent claims are directed on features of preferred embodiments of the invention.

[0031] According to the present invention, it is possible to prevent the interlayer insulating film from peeling off. As a result, the production yield of the liquid crystal display device can be improved.

BRIEF DESCRIPTION OF THE DRAWINGS

[0032]

Fig. 1 is a top view of a liquid crystal display device;
Fig. 2 is a top view of a pixel portion according to a first embodiment of the present invention;
Fig. 3 is a cross-sectional view taken along line A-A in Fig. 2;
Fig. 4 is a cross-sectional view according to a comparative embodiment;
Fig. 5 is a top view showing an example in which the present invention is applied to the TEG pattern portion;
Fig. 6 is a cross-sectional view taken along line B-B in Fig. 5;
Fig. 7 is a top view showing an example in which the present invention is applied to the alignment mark portion;
Fig. 8 is a cross-sectional view taken along line C-C in Fig. 7; and
Fig. 9 is a cross-sectional view of the display area of the liquid crystal display device having a top-gate type TFT.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0033] Hereinafter, the present invention will be described in detail with reference to embodiments.

First Embodiment of the invention

[0034] Fig. 1 is a top view of a small liquid crystal display device used for portable electronic devices such as mobile phones, which is an example of the product to which the present invention is applied. In Fig. 1, a counter substrate 200 is provided on a TFT substrate 100. Although not shown, there is a liquid crystal layer interposed between the TFT substrate 100 and the counter substrate 200. The TFT substrate 100 and the counter substrate 200 are bonded together by a sealing material 20 formed around the frame. In Fig. 1, liquid crystal is injected between the substrates by a dropping method, so that no injection hole is formed.

[0035] The TFT substrate 100 is formed larger than the counter substrate 200. In a portion of the TFT substrate 100 extending beyond the counter substrate 200, a terminal portion 150 is formed to supply power, image signals, scan signals, and the like, to a liquid crystal cell 1. Further, on the outside of the terminal portion 150, there is formed a testing element group (TEG) used in the test of the circuit characteristics, or an alignment mark used in the alignment of the upper and lower boards in the production process.

[0036] Fig. 2 is a top view of the structure of a part of the pixel portion in the display area 10 shown in Fig. 1. In Fig. 2, the pixel electrode 112 having the slit 115 is formed in an area surrounded by an image signal line 40 and a scan line 30. A common electrode, not shown, is formed below the pixel electrode 112 through a second interlayer insulating film not shown. An image signal is supplied to the pixel electrode 112 from the image signal line 40 through TFT.

[0037] In Fig. 2, a first TFT and a second TFT are arranged in series from the image signal line 40 to the pixel electrode 112. In Fig. 2, a contact hole 130 is formed in a wide portion of the image signal line 40 to connect the semiconductor layer 103 with the image signal line 40. The semiconductor layer 103 extends beyond the scan line 30, and is folded across the scan line 30 once again to connect to the pixel electrode 112.

[0038] The semiconductor layer 103 includes a channel portion below the scan line 30 having a role as a gate electrode, in which a drain portion or a source portion is formed on either of the two sides of the scan line 30. In Fig. 2, for convenience, the side near the image signal line 40 is called the drain portion and the side near the pixel electrode 112 is called the source portion in each TFT. In other words, in the first TFT, the side connected to the image signal line 40 is the drain portion, and the side connected to the second TFT is the source portion, while in the second TFT, the side connected to the first TFT is the drain portion, and the side connected to the pixel electrode 112 is the source portion.

[0039] In Fig. 2, the scan line 30 also functions as the gate electrode. The channel portion of the semiconductor layer 103 is formed below the scan line 30. Thus, in Fig. 2, two TFTs are present between the image signal line 40 and the pixel electrode 112. In Fig. 2, a through hole 140 is also formed in the contact portion of the image signal line 40 and the semiconductor layer 103. The area of the through hole is greater than the area of the contact hole 130. The through hole 140 is used to release gas from an organic passivation film 109 not shown in Fig. 2.

[0040] In the counter substrate 200, there is formed a black matrix in the area shown in Fig. 2. The black matrix covers the image signal line 40, the scan line 30, the through hole 140, the contact hole 130, the channel portion of the TFT, and the like, formed on the TFT substrate 100 as described above.

[0041] Fig. 3 is a cross-sectional view taken along line A-A in Fig. 2. The semiconductor layer 103 is formed on the first base film and on the second base film. A gate insulating film 104 and a first interlayer insulating film 106 are formed so as to cover the semiconductor layer 103, on which the image signal line 40 is formed. The image signal line 40 is connected to the semiconductor layer 103 through the contact hole 130 that is formed in the gate insulating film 104 and in the first interlayer insulating film 106. The inorganic passivation film 108 is formed so as to cover the image signal line 40 or the first interlayer insulating film 106. Then, the organic passivation film 109 is formed on the inorganic passivation film 108.

[0042] A common electrode 110 is formed on the organic passivation film 109. Then, a second interlayer insulating film 111 is formed on the common electrode 110. The second interlayer insulating film 111 provides electrical insulation between the common electrode 110 and the pixel electrode 112. However, the pixel electrode 112 is not present on the image signal line 40. In the present invention, the through hole 140 is formed in this area of the second interlayer insulating film 111 to be able to easily release water and the like absorbed by the organic passivation film 109. Note that the oriented film is omitted in Fig. 3.

[0043] As shown in Figs. 2 and 3, the diameter of the through hole 140 is greater than the diameter of the contact hole 130. This is in order to effectively release the gas absorbed by the organic passivation film 109. The portion in which the contact hole 130 is formed has a concave shape, so that peeling of the second interlayer insulating film 111 is more likely to occur. For this reason, it is effective to form the through hole 140 for gas release in this area.

[0044] As shown in Fig. 2, the portion in which the through hole 140 for gas release is formed is the wide portion of the image signal line 40, which also functions as a light shielding electrode 135. Thus, if a disturbance in the orientation of the liquid crystal molecules occurs due to the influence of the through hole 140 for gas re-

lease, light leakage will not occur in this portion.

[0045] The through hole 140 for gas release is formed by etching. The second interlayer insulating film 111 is formed by low temperature CVD, so that the dimension control in etching is more difficult than the case of the film formed by high temperature CVD. However, as shown in Fig. 2, the light shielding electrode 135 having a large area is formed below the through hole 140 for gas release. Thus, light leakage will not occur if the dimension of the through hole 140 for gas release varies.

[0046] Further, in Fig. 2, the through hole 140 for gas release is formed very close to the scan line 30. In the counter substrate 200, the black matrix 202 is formed in the portion corresponding to the scan line 30. Thus, even if light leakage occurs due to the influence of the through hole 140 for gas release, the light can also be blocked by the black matrix 202.

[0047] As described above, according to the present invention, the through hole 140 for gas release is formed in the vicinity of the scan line 30 and in the wide portion of the image signal line 40. Thus, it is possible to prevent peeling of the second interlayer insulating film 111. Further, the wide portion of the image signal line 40 also functions as the light shielding electrode 135, preventing side effects such as light leakage due to the formation of the through hole 140 for gas release.

[0048] Note that in the present invention, the through hole 140 for gas release formed in the second interlayer insulating film 111 is not covered by ITO. As a result, it is possible to release gas from the organic passivation film to the outside more effectively.

Comparative Embodiment

[0049] In an upper wiring circuit 160 corresponding to the shaded part above the display area 10 shown in Fig. 1, a portion of protective wiring circuits or drive circuits is formed. These protective circuits have a TFT. The inorganic passivation film 108 and the organic passivation film 109 are formed so as to cover the TFT, on which the common electrode 110 is formed. Then, the second interlayer insulating film 111 is formed so as to cover the common electrode 110. There is also a problem with the adhesion of the second interlayer insulating film 111, similar to the case of the display area 10 described in the first embodiment of the invention.

[0050] Fig. 4 is a cross-sectional view in the area in which the protective circuit and the like are formed. Fig. 4 is a view of the cross section including TFT. Fig. 4 is the same as that described with reference to Fig. 9, and so the details will be omitted here. In Fig. 4, the source electrode 107 or drain electrode is connected through the contact hole 130 formed in the gate insulating film 104 and in the first interlayer insulating film 106, both of which cover the semiconductor layer 103. The source electrode 107 or drain electrode is the line formed in the same layer as the image signal line 40. The inorganic passivation film 108 is formed so as to cover the source electrode 107 or drain electrode. Then, the organic passivation film 109 is formed on the inorganic passivation film 108.

[0051] On the inorganic passivation film 108, there is an electrode of ITO formed at the same time as the common electrode 110. This electrode is electrically connected to the common electrode 110, and will also be referred to as the common electrode 110. This common electrode 110 does not drive the liquid crystal molecules as in the case of Fig. 9, which serves as a simple connection line or a shield electrode. The second interlayer insulating film 111 is formed so as to cover the common electrode 110. The contact hole 130 is formed in the vicinity of the TFT, in which the adhesion of the second interlayer insulating film 111 is particularly low. Thus, the through hole 140 is formed in the corresponding portion of the second interlayer insulating film 111 to release gas from the organic passivation film 109.

[0052] In Fig. 4, the through hole 140 for gas release is formed on the outside of the display area 10, so that light leakage or other problems will not occur if the dimension of the through hole 140 for gas release somewhat varies. Thus, a relatively larger through hole can be made on the outside of the display area 10 than inside. As a result, it is possible to prevent peeling of the second interlayer insulating film 111 more surely. Note that also in this comparative embodiment, the through hole 140 for gas release formed in the second interlayer insulating film 111 is not covered by ITO. Thus, it is possible to release gas from the organic passivation film to the outside more effectively.

Second Embodiment of the invention

[0053] In the liquid crystal display device to which the present invention is applied, the TFT is formed of poly-Si, in which a drive circuit can be mounted within the liquid crystal display panel. When the drive circuit is formed within the liquid crystal display panel, it is necessary to check the change in the circuit characteristics during the process. For this reason, as shown in Fig. 1, a testing element group (TEG) 170 is formed on the outside of the terminal portion 150. The characteristics of the TFT and the like are checked by the TEG 170. Thus, the TEG 170 should also have the same structure as the display area 10 or the drive circuit portion.

[0054] Also in the TEG 170, the common electrode 110 of ITO is formed on the organic passivation film 109. Then, the second interlayer insulating film 111 is present on the common electrode 110. This is the same as in the display area 10 and the like. Fig. 5 is an example of the TEG 170, in which a long resistance is formed between terminals 1501 and 1502 to measure the resistance formed by the common electrode 110. Although not shown, the second interlayer insulating film 111 is formed on this long resistance. The common electrode 110 is formed on the organic passivation film 109. When the water is released from the organic passivation film 109,

the second interlayer insulating film 111 peels off, and it is no longer able to function as the TEG 170. In this embodiment, as shown in Fig. 5, a large number of rectangular through holes 140 for gas release are formed to allow gas to be easily released from the organic passivation film 109. In this way, the second insulating film 111 is prevented from peeling off.

[0055] Fig. 6 is a cross-sectional view taken along line B-B in Fig. 5. The first and second base films are omitted in Fig. 6. Fig. 6 shows that the semiconductor layer 103, the gate insulating film 104, the first interlayer insulating film 106, the inorganic passivation film 108, and the organic passivation film 109 are laminated in this order from the bottom. Then, the common electrode 110 is formed on the organic passivation film 109. The second interlayer insulating film 111 is formed on the common electrode 110. The through holes 140 for gas release are formed in the second interlayer insulating film 111, in order that the water and the like can be easily released from the organic passivation film 109. As a result, the second interlayer insulating film 111 is prevented from peeling off.

[0056] The manufacturing process of liquid crystal display devices is as follows. A mother board is formed by bonding a mother TFT board in which a large number of the TFT substrates 100 are formed, to a mother counter board in which a large number of the counter substrates 200 are formed. Then, individual liquid crystal display panels are cut out of the mother board by scribing or other method. When the mother TFT substrate and the mother counter substrate are bonded together by a sealing material, it is necessary to use the alignment mark 180.

[0057] Fig. 7 is an example of an alignment mark 180. In Fig. 7, the alignment mark 180 is formed by combining square units. The rectangular through holes 140 for gas release are present in some of the units of the alignment mark 180. The through holes 140 are formed in the second interlayer insulating film 111. The through holes 140 for gas release allow the water and the like absorbed by the organic passivation film 109 to be easily released. As a result, the second interlayer insulating film 111 is prevented from peeling off.

[0058] Fig. 8 is a cross-sectional view taken along line C-C in Fig. 7. The configuration of Fig. 8 is the same as that described with reference to Fig. 6, except that the semiconductor layer 103 is not present. Thus, the description thereof will be omitted. Note that Fig. 6 or Fig. 8 is an example of the cross section. It does not necessarily mean that the semiconductor layer 103 is typically present in Fig. 6, and that the semiconductor layer 103 is typically not present in Fig. 8.

[0059] As described above, when the organic passivation film 109 and the second interlayer insulating film 111 are also formed in the area other than the area in which the liquid crystal is injected in the liquid crystal display panel, the through holes 140 for gas release are also formed in this area of the second interlayer insulating film 111, to be able to function as the TEG 170 or the alignment mark 180 without fail. However, the TEG 170 or the alignment mark 180 shown in Fig. 1 is not used after the liquid crystal display device is completed. Thus, the portion of the TEG 170 or the alignment mark 180 is often removed in the scribing process. Note that also in this embodiment, the through hole 140 for gas release formed in the second interlayer insulating film is not covered by ITO. Thus, it is possible to release gas from the organic passivation film to the outside more effectively.

[0060] In the above examples, the IPS is the type in which the common electrode 110 is formed on the organic passivation film 109, on which the pixel electrode 112 having the slit 115 is formed through the second interlayer insulating film 111. However, the present invention can also be applied in the same way to the other types of IPS in which the pixel electrode 112 is formed on the organic passivation film 109, on which the common electrode having the slit 115 is provided through the interlayer insulating film 111.

Claims

1. A liquid crystal display device comprising a TFT substrate (100) and a counter substrate (200), scan lines (30), image signal lines (40), and a pixel electrode (112), all formed on said TFT substrate (100), said pixel electrode (112) formed in an area surrounded by a pair said scan lines (30) extending in a first direction and arranged parallel to each other along a second direction perpendicular to said first direction, and by a pair of said image signal lines (40) extending in said second direction and arranged parallel to each other along said first direction,
wherein said pixel electrode (112) is supplied with an image signal from one of said pair of image signal lines (40) through a TFT on said TFT substrate (100),
wherein said TFT includes a semiconductor layer (103) on said TFT substrate (100), said TFT having a channel portion, a drain portion formed on the side of said one image signal line (40), and a source portion formed on the side of said pixel electrode (112),
wherein a gate insulating film (104) is formed so as to cover said semiconductor layer (103),
wherein a gate electrode (105) is formed on said gate insulating film (104) above said channel portion,
wherein a first interlayer insulating film (106) is formed so as to cover said gate electrode (105),
characterized in that
said one image signal line (40) is provided on said first interlayer insulating film (106),
wherein an inorganic passivation film (108) and an organic passivation film (109) are formed in this order so as to cover said one image signal line (40),
wherein a common electrode (110) is formed on said organic passivation film (109),
wherein a second interlayer insulating film (111) is formed on said common electrode (110),

wherein said pixel electrode (112) has a slit and is formed on said second interlayer insulating film,
wherein the portion of said one image signal line (40) connected to said drain portion of said TFT is made wider than the rest of said one image signal line (40),
wherein said pixel electrode (112) is not formed over said wider portion of said one image signal line (40),
wherein said one image signal line (40) is connected in said wider portion to said drain portion through a contact hole (130),
wherein a through hole (140) is formed in said second interlayer insulating film (111) in said wider portion of said one image signal line (40), and
wherein the diameter of said through hole (140) is greater than the diameter of said contact hole (130).

2. A liquid crystal display device comprising a TFT substrate (100) and a counter substrate (200), scan lines (30), image signal lines (40), and a pixel electrode (112), all formed on said TFT substrate (100), said pixel electrode (112) formed in an area surrounded by a pair of said scan lines (30) extending in a first direction and arranged parallel to each other along a second direction perpendicular to said first direction, and by a pair of said image signal lines (40) extending in said second direction and arranged parallel to each other along said first direction
wherein said pixel electrode (112) is supplied with an image signal from one of said pair of image signal lines (40) through a TFT on said TFT substrate (100),
wherein said TFT includes a semiconductor layer (103) on said TFT substrate (100), said TFT having a channel portion, a drain portion formed on the side of said one image signal line (40), and a source portion formed on the side of said pixel electrode (112),
wherein a gate insulating film (104) is formed so as to cover said semiconductor layer (103),
wherein a gate electrode (105) is formed on said gate insulating film (104) above said channel portion,
wherein a first interlayer insulating film (106) is formed so as to cover said gate electrode (105),
characterized in that
said one image signal line (40) is provided on said first interlayer insulating film (106),
wherein an inorganic passivation film (108) and an organic passivation film (109) are formed in this order so as to cover said one image signal line (40),
wherein said pixel electrode (112) is formed on said organic passivation film (109),
wherein a second interlayer insulating film (111) is formed on said pixel electrode (112),
wherein a common electrode (110) having a slit is formed on said second interlayer insulating film (111),
wherein the portion of said one image signal line (40) connected to said drain portion of said TFT is made wider than the rest of said one image signal line (40),
wherein said common electrode (110) is not formed over said wider portion of said one image signal line (40),
wherein said one image signal line (40) is connected in said wider portion to said drain portion through a contact hole (130),
wherein a through hole (140) is formed in said second interlayer insulating film (111) in said wider portion of said one image signal line (40), and
wherein the diameter of said through hole (140) is greater than the diameter of said contact hole (130).

3. The liquid crystal display device according to claim 1 or claim 2,
wherein said TFT includes a first TFT and a second TFT,
wherein said first TFT has a drain portion connected to said one image signal line (40),
wherein said second TFT is connected to said first TFT and has a source portion connected to said pixel electrode (112), and
wherein one of said pair of scan lines (30) also functions as said gate electrodes of said first TFT and said second TFT.

4. A liquid crystal display device comprising a TFT substrate (100) and a counter substrate (200), scan lines (30), image signal lines (40), and a pixel electrode (112), all formed on said TFT substrate (100),
wherein said TFT substrate (100) and said counter substrate (200) are bonded face-to-face with a liquid crystal layer formed inside,
wherein said pixel electrode (112) is supplied with an image signal from one of said image signal lines (40) through a TFT,
wherein said TFT includes a semiconductor layer (103) having a channel portion, a drain portion formed on the side of said one image signal line (40), and a source portion formed on the side of said pixel electrode (112),
wherein a gate insulating film (104) is formed so as to cover said semiconductor layer (103),
wherein a gate electrode (105) is formed on said gate insulating film (104) above said channel portion,
wherein a first interlayer insulating film (106) is formed so as to cover said gate electrode (105),
characterized in that
a terminal portion (150) and a testing element group (170), or a terminal portion (150) and an alignment mark (180), are formed in a portion of said TFT substrate (100) not facing said counter substrate (200),
wherein said testing element group (170) or said alignment mark (180) is configured such that an inorganic passivation film (108) and an organic passivation film (109) are laminated in this order on the laminated stack of said semiconductor layer (103), said gate insulating films (104), and said first interlayer insulating film (106) on said TFT substrate,
wherein an electrode is formed of ITO on said organic

passivation film (109),
wherein a second interlayer insulating film (111) is formed on said ITO electrode, and
wherein a through hole (140) is formed in said second interlayer insulating film (111) in an area in which said testing element group (170) or said aligment mark (108) is formed.

5. The liquid crystal display device according to claim 4, wherein said through hole (140) formed in said second interlayer insulating film (111) is not covered by ITO.

Patentansprüche

1. Flüssigkristallanzeigevorrichtung mit einem TFT-Substrat (100) und einem Gegensubstrat (200), Abtastzeilen (30), Bildsignalleitungen (40) und einer Pixelelektrode (112), die alle auf dem TFT-Substrat (100) ausgeformt sind, wobei die Pixelelektrode (112) in einem Bereich ausgebildet ist, der von einem Paar der Abtastzeilen (30) umgeben ist, die sich in einer ersten Richtung erstrecken und parallel zueinander entlang einer zweiten Richtung, die senkrecht zu der ersten Richtung verläuft, angeordnet sind, und von einem Paar der Bildsignalleitungen (40) umgeben ist, die sich in der zweiten Richtung erstrecken und parallel zueinander entlang der ersten Richtung angeordnet sind,
wobei die Pixelelektrode (112) mit einem Bildsignal von einer des Paares von Bildsignalleitungen (40) durch einen TFT auf dem TFT-Substrat (100) gespeist wird,
wobei der TFT eine Halbleiterschicht (103) auf dem TFT-Substrat (100) aufweist und wobei der TFT einen Kanal-Bereich, einen Drain-Bereich, der auf der Seite der einen Bildsignalleitung (40) ausgebildet ist, und einen Source-Bereich, der auf der Seite der Pixelelektrode (112) ausgebildet ist, aufweist,
wobei ein isolierender Gate-Film (104) so ausgebildet ist, dass er die Halbleiterschicht (103) bedeckt,
wobei eine Gate-Elektrode (105) auf dem isolierenden Gate-Film (104) oberhalb des Kanal-Bereichs ausgebildet ist,
wobei ein erster isolierender Zwischenfilm (106) so ausgeformt ist, dass er die Gate-Elektrode (105) bedeckt,
dadurch gekennzeichnet, dass
die eine Bildsignalleitung (40) auf dem ersten isolierenden Zwischenfilm (106) angeordnet ist,
wobei ein anorganischer Passivierungsfilm (108) und ein organischer Passivierungsfilm (109) in dieser Reihenfolge ausgebildet sind, um die eine Bildsignalleitung (40) abzudecken,
wobei eine gemeinsame Elektrode (110) auf dem organischen Passivierungsfilm (109) ausgebildet ist,
wobei ein zweiter isolierender Zwischenfilm (111) auf der gemeinsamen Elektrode (110) ausgebildet ist,
wobei die Pixelelektrode (112) einen Schlitz aufweist, und auf dem zweiten isolierenden Zwischenfilm ausgebildet ist,
wobei der Bereich der einen Bildsignalleitung (40), der mit dem Drain-Bereich des TFT verbunden ist, breiter ausgeführt ist als der Rest der einen Bildsignalleitung (40),
wobei die Pixelelektrode (112) nicht über den breiteren Bereich der einen Bildsignalleitung (40) ausgebildet ist,
wobei die eine Bildsignalleitung (40) in dem breiteren Bereich mit dem Drain-Bereich durch ein Kontaktloch (130) verbunden ist,
wobei ein durchgehendes Loch (140) in dem zweiten isolierenden Zwischenfilm (111) in dem breiteren Bereich der einen Bildsignalleitung (40) ausgeformt ist, und
wobei der Durchmesser des durchgehenden Lochs (140) größer ist als der Durchmesser des Kontaktlochs (130).

2. Flüssigkristallanzeigevorrichtung mit einem TFT-Substrat (100) und einem Gegensubstrat (200), Abtastzeilen (30), Bildsignalleitungen (40) und einer Pixelelektrode (112), die alle auf dem TFT-Substrat (100) ausgeformt sind, wobei die Pixelelektrode (112) in einem Bereich ausgebildet ist, der von einem Paar der Abtastzeilen (30) umgeben ist, die sich in einer ersten Richtung erstrecken und parallel zueinander entlang einer zweiten Richtung, die senkrecht zu der ersten Richtung verläuft, angeordnet sind, und von einem Paar der Bildsignalleitungen (40) umgeben ist, die sich in der zweiten Richtung erstrecken und parallel zueinander entlang der ersten Richtung angeordnet sind,
wobei die Pixelelektrode (112) mit einem Bildsignal von einer des Paares von Bildsignalleitungen (40) durch einen TFT auf dem TFT-Substrat (100) gespeist wird,
wobei der TFT eine Halbleiterschicht (103) auf dem TFT-Substrat (100) aufweist und wobei der TFT einen Kanal-Bereich, einen Drain-Bereich, der auf der Seite der einen Bildsignalleitung (40) ausgebildet ist, und einen Source-Bereich, der auf der Seite der Pixelelektrode (112) ausgebildet ist, aufweist,
wobei ein isolierender Gate-Film (104) so ausgebildet ist, dass er die Halbleiterschicht (103) bedeckt,
wobei eine Gate-Elektrode (105) auf dem isolierenden Gate-Film (104) oberhalb des Kanal-Bereichs ausgebildet ist,
wobei ein erster isolierender Zwischenfilm (106) so ausgeformt ist, dass er die Gate-Elektrode (105) bedeckt,
dadurch gekennzeichnet, dass
die eine Bildsignalleitung (40) auf dem ersten isolierenden Zwischenfilm (106) angeordnet ist,

wobei ein anorganischer Passivierungsfilm (108) und ein organischer Passivierungsfilm (109) in dieser Reihenfolge ausgebildet sind, um die eine Bildsignalleitung (40) abzudecken,
wobei die Pixelelektrode (112) auf dem organischen Passivierungsfilm (109) ausgebildet ist,
wobei ein zweiter isolierender Zwischenfilm (111) auf der Pixel-elektrode (112) ausgebildet ist,
wobei eine gemeinsame Elektrode (110), die einen Schlitz aufweist, auf dem zweiten isolierenden Zwischenfilm (111) ausgeformt ist,
wobei der Bereich der einen Bildsignalleitung (40), der mit dem Drain-Bereich des TFT verbunden ist, breiter als der Rest der einen Bildsignalleitung (40) ausgebildet ist,
wobei die gemeinsame Elektrode (110) nicht über den breiteren Bereich der einen Bildsignalleitung (40) ausgeformt ist,
wobei die eine Bildsignalleitung (40) in dem breiteren Bereich mit dem Drain-Bereich durch ein Kontaktloch (130) verbunden ist,
wobei ein durchgehendes Loch (140) in dem zweiten isolierenden Zwischenfilm (111) in dem breiteren Bereich der einen Bildsignalleitung (40) ausgeformt ist, und
wobei der Durchmesser des durchgehenden Lochs (140) größer ist als der Durchmesser des Kontaktlochs (130).

3. Flüssigkristallanzeigevorrichtung nach Anspruch 1 oder Anspruch 2,
wobei der TFT einen ersten TFT und einen zweiten TFT aufweist, wobei der erste TFT einen Drain-Bereich aufweist, der mit der einen Bildsignalleitung (40) verbunden ist,
wobei der zweite TFT mit dem ersten TFT verbunden ist, und dessen Source-Bereich mit der Pixelelektrode (112) verbunden ist, und
wobei eine des Paares von Abtastzeilen (30) ebenso funktioniert als Gate-Elektroden des ersten TFT und des zweiten TFT.

4. Flüssigkristallanzeigevorrichtung mit einem TFT-Substrat (100) und einem Gegensubstrat (200), Abtastzeilen (30), Bildsignalleitungen (40) und einer Pixelelektrode (112), die alle auf dem TFT-Substrat (100) ausgeformt sind,
wobei das TFT-Substrat (100) und das Gegensubstrat (200) Seite auf Seite mit einer dazwischen ausgeformten Flüssigkristallschicht miteinander verbunden sind,
wobei die Pixelelektrode (112) mit einem Bildsignal von einer der Bildsignalleitungen (40) durch einen TFT gespeist wird,
wobei der TFT eine Halbleiterschicht (103) aufweist mit einem Kanal-Bereich, einem Drain-Bereich, der auf der Seite der einen Bildsignalleitung (40) ausgebildet ist, und einem Source-Bereich, der auf der Seite der Pixel-Elektrode (112) ausgebildet ist,
wobei ein isolierender Gate-Film (104) so ausgebildet ist, dass er die Halbleiterschicht (103) bedeckt,
wobei eine Gate-Elektrode (105) auf dem isolierenden Gate-Film (104) oberhalb des Kanal-Bereichs ausgebildet ist,
wobei ein erster isolierender Zwischenfilm (106) so ausgebildet ist, dass er die Gate-Elektrode (105) bedeckt,
dadurch gekennzeichnet, dass
ein Anschlussbereich (150) und eine Testelementgruppe (170) oder ein Anschlussbereich (150) und eine Ausrichtungsmarkierung (180) in einem Bereich des TFT-Substrats (100) ausgebildet sind, der nicht dem Gegensubstrat (200) gegenüberliegt,
wobei die Testelementgruppe (170) oder die Ausrichtungsmarkierung (180) so angeordnet sind, dass ein anorganischer Passivierungsfilm (108) und ein organischer Passivierungsfilm (109) in dieser Reihenfolge auf dem laminierten Stapel aus der Halbleiterschicht (103), dem isolierenden Gate-Film (104) und dem ersten isolierenden Zwischenfilm (106) auf dem TFT-Substrat geschichtet sind,
wobei eine Elektrode aus ITO auf dem organischen Passivierungsfilm (109) ausgeformt ist,
wobei ein zweiter isolierender Zwischenfilm (111) auf der ITO-Elektrode ausgebildet ist, und
wobei ein durchgehendes Loch (140) in dem zweiten isolierenden Zwischenfilm (111) in einem Bereich ausgebildet ist, in dem die Testelementgruppe (170) oder die Ausrichtungsmarkierung (180) ausgeformt sind.

5. Flüssigkristallanzeigevorrichtung nach Anspruch 4, wobei das durchgehende Loch (140), welches in dem zweiten isolierenden Zwischenfilm (111) ausgeformt ist, nicht durch das ITO bedeckt ist.

Revendications

1. Dispositif d'affichage à cristaux liquides comprenant un substrat TFT (100) et un contre-substrat (200), des lignes (30) de balayage, des lignes (40) de signal d'image, et une électrode (112) de pixel, tous formés sur ledit substrat TFT (100), ladite électrode (112) de pixel formée dans une zone entourée par une paire desdites lignes (30) de balayage s'étendant dans un premier sens et agencées parallèles l'une à l'autre sur un deuxième sens perpendiculaire audit premier sens et par une paire desdites lignes (40) de signal d'image s'étendant dans ledit deuxième sens et agencées parallèles l'une à l'autre sur ledit premier sens,
dans lequel ladite électrode (112) de pixel reçoit un signal d'image provenant d'une de ladite paire de lignes (40) de signal d'image par l'intermédiaire d'un TFT sur ledit substrat TFT (100),

dans lequel ledit TFT inclut une couche semi-conductrice (103) sur ledit substrat TFT (100), ledit TFT ayant une partie de canal, une partie de drain formée sur le côté de ladite une ligne (40) de signal d'image, et une partie de source formée sur le côté de ladite électrode (112) de pixel,
dans lequel un film d'isolation de grille (104) est formé de manière à recouvrir ladite couche semi-conductrice (103),
dans lequel une électrode de grille (105) est formée sur ledit film d'isolation de grille (104) au-dessus de ladite partie de canal,
dans lequel un premier film d'isolation inter-couches (106) est formé de manière à recouvrir ladite électrode de grille (105),
caractérisé en ce que
ladite une ligne (40) de signal d'image est prévue sur ledit premier film d'isolation inter-couches (106),
dans lequel un film de passivation inorganique (108) et un film de passivation organique (109) sont formés dans cet ordre de manière à recouvrir ladite une ligne (40) de signal d'image,
dans lequel une électrode commune (110) est formée sur ledit film de passivation organique (109),
dans lequel un deuxième film d'isolation inter-couches (111) est formé sur ladite électrode commune (110),
dans lequel ladite électrode (112) de pixel a une fente et est formée sur ledit deuxième film d'isolation inter-couches,
dans lequel la partie de ladite une ligne (40) de signal d'image connectée à ladite partie de drain dudit TFT est constituée plus large que le reste de ladite une ligne (40) de signal d'image,
dans lequel ladite électrode (112) de pixel n'est pas formée sur ladite partie plus large de ladite une ligne (40) de signal d'image,
dans lequel ladite une ligne (40) de signal d'image est connectée dans ladite partie plus large à ladite partie de drain par l'intermédiaire d'un trou de contact (130),
dans lequel un trou traversant (140) est formé dans ledit deuxième film d'isolation inter-couches (111) dans ladite partie plus large de ladite une ligne (40) de signal d'image, et
dans lequel le diamètre dudit trou traversant (140) est plus grand que le diamètre dudit trou de contact (130).

2. Dispositif d'affichage à cristaux liquides comprenant un substrat TFT (100) et un contre-substrat (200), des lignes (30) de balayage, des lignes (40) de signal d'image, et une électrode (112) de pixel, tous formés sur ledit substrat TFT (100), ladite électrode (112) de pixel formée dans une zone entourée par une paire desdites lignes (30) de balayage s'étendant dans un premier sens et agencées parallèles l'une à l'autre sur un deuxième sens perpendiculaire audit premier sens et par une paire desdites lignes (40) de signal d'image s'étendant dans ledit deuxième sens et agencées parallèles l'une à l'autre sur ledit premier sens,
dans lequel ladite électrode (112) de pixel reçoit un signal d'image provenant d'une de ladite paire de lignes (40) de signal d'image par l'intermédiaire d'un TFT sur ledit substrat TFT (100),
dans lequel ledit TFT inclut une couche semi-conductrice (103) sur ledit substrat TFT (100), ledit TFT ayant une partie de canal, une partie de drain formée sur le côté de ladite une ligne (40) de signal d'image, et une partie de source formée sur le côté de ladite électrode (112) de pixel,
dans lequel un film d'isolation de grille (104) est formé de manière à recouvrir ladite couche semi-conductrice (103),
dans lequel une électrode de grille (105) est formée sur ledit film d'isolation de grille (104) au-dessus de ladite partie de canal,
dans lequel un premier film d'isolation inter-couches (106) est formé de manière à recouvrir ladite électrode de grille (105),
caractérisé en ce que
ladite une ligne (40) de signal d'image est prévue sur ledit premier film d'isolation inter-couches (106),
dans lequel un film de passivation inorganique (108) et un film de passivation organique (109) sont formés dans cet ordre de manière à recouvrir ladite une ligne (40) de signal d'image,
dans lequel ladite électrode (112) de pixel est formée sur ledit film de passivation organique (109),
dans lequel un deuxième film d'isolation inter-couches (111) est formé sur ladite électrode (112) de pixel,
dans lequel une électrode commune (110) ayant une fente est formée sur le deuxième film d'isolation inter-couches (111),
dans lequel la partie de ladite une ligne (40) de signal d'image connectée à ladite partie de drain dudit TFT est constituée plus large que le reste de ladite une ligne (40) de signal d'image,
dans lequel ladite électrode commune (110) n'est pas formée sur ladite partie plus large de ladite une ligne (40) de signal d'image,
dans lequel ladite une ligne (40) de signal d'image est connectée dans ladite partie plus large à ladite partie de drain par l'intermédiaire d'un trou de contact (130),
dans lequel un trou traversant (140) est formé dans ledit deuxième film d'isolation inter-couches (111) dans ladite partie plus large de ladite une ligne (40) de signal d'image, et
dans lequel le diamètre dudit trou traversant (140) est plus grand que le diamètre dudit trou de contact (130).

3. Dispositif d'affichage à cristaux liquides selon la re-

vendication 1 ou la revendication 2,
dans lequel ledit TFT inclut un premier TFT et un deuxième TFT,
dans lequel ledit premier TFT a une partie de drain connectée à ladite une ligne (40) de signal d'image,
dans lequel ledit deuxième TFT est connecté audit premier TFT et a une partie de source connectée à ladite électrode (112) de pixel, et
dans lequel une de ladite paire de lignes (30) de balayage fonctionne également comme lesdites électrodes de grille dudit premier TFT et dudit deuxième TFT.

4. Dispositif d'affichage à cristaux liquides comprenant un substrat TFT (100) et un contre-substrat (200), des lignes (30) de balayage, des lignes (40) de signal d'image, et une électrode (112) de pixel, tous formés sur ledit substrat TFT (100),
dans lequel ledit substrat TFT (100) et ledit contre-substrat (200) sont liés face à face avec une couche de cristaux liquides formée à l'intérieur,
dans lequel ladite électrode (112) de pixel reçoit un signal d'image provenant d'une desdites lignes (40) de signal d'image par l'intermédiaire d'un TFT,
dans lequel ledit TFT inclut une couche semi-conductrice (103) ayant une partie de canal, une partie de drain formée sur le côté de ladite une ligne (40) de signal d'image, et une partie de source formée sur le côté de ladite électrode (112) de pixel,
dans lequel un film d'isolation de grille (104) est formé de manière à recouvrir ladite couche semi-conductrice (103),
dans lequel une électrode de grille (105) est formée sur ledit film d'isolation de grille (104) au-dessus de ladite partie de canal,
dans lequel un premier film d'isolation inter-couches (106) est formé de manière à recouvrir ladite électrode de grille (105),
caractérisé en ce que
une partie terminale (150) et un groupe d'éléments de test (170) ou une partie terminale (150) et une marque d'alignement (180) sont formé(e)s dans une partie dudit substrat TFT (100) ne faisant pas face audit contre-substrat (200),
dans lequel ledit groupe d'éléments de test (170) ou ladite marque d'alignement (180) est configuré(e) de telle manière qu'un film de passivation inorganique (108) et un film de passivation organique (109) sont stratifiés dans cet ordre sur la pile stratifiée de ladite couche semi-conductrice (103), dudit film d'isolation de grille (104) et dudit premier film d'isolation inter-couches (106) sur ledit substrat TFT,
dans lequel une électrode est constituée d'ITO sur ledit film de passivation organique (109),
dans lequel un deuxième film d'isolation inter-couches (111) est formé sur ladite électrode d'ITO, et
dans lequel un trou traversant (140) est formé dans ledit deuxième film d'isolation inter-couches (111) dans une zone dans laquelle ledit groupe d'éléments de test (170) ou ladite marque d'alignement (180) est formé(e).

5. Dispositif d'affichage à cristaux liquides selon la revendication 4, dans lequel ledit trou traversant (140) formé dans ledit deuxième mm d'isolation inter-couches (111) n'est pas recouvert d'ITO.

FIG. 1

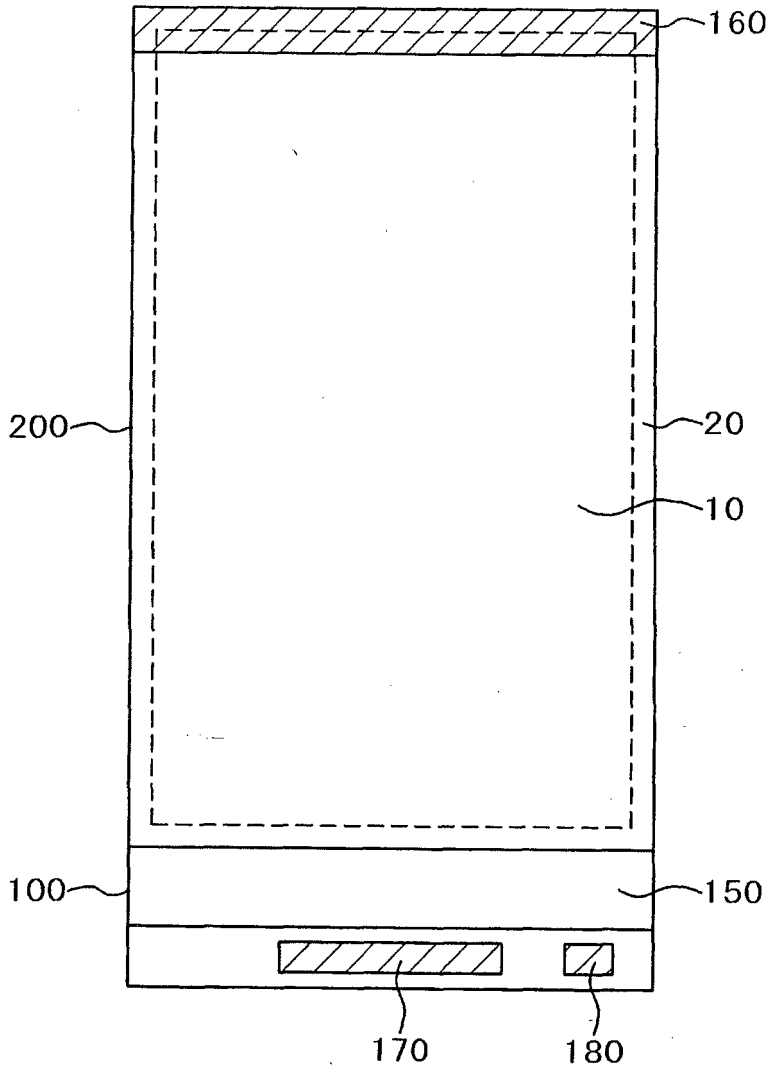


FIG. 2

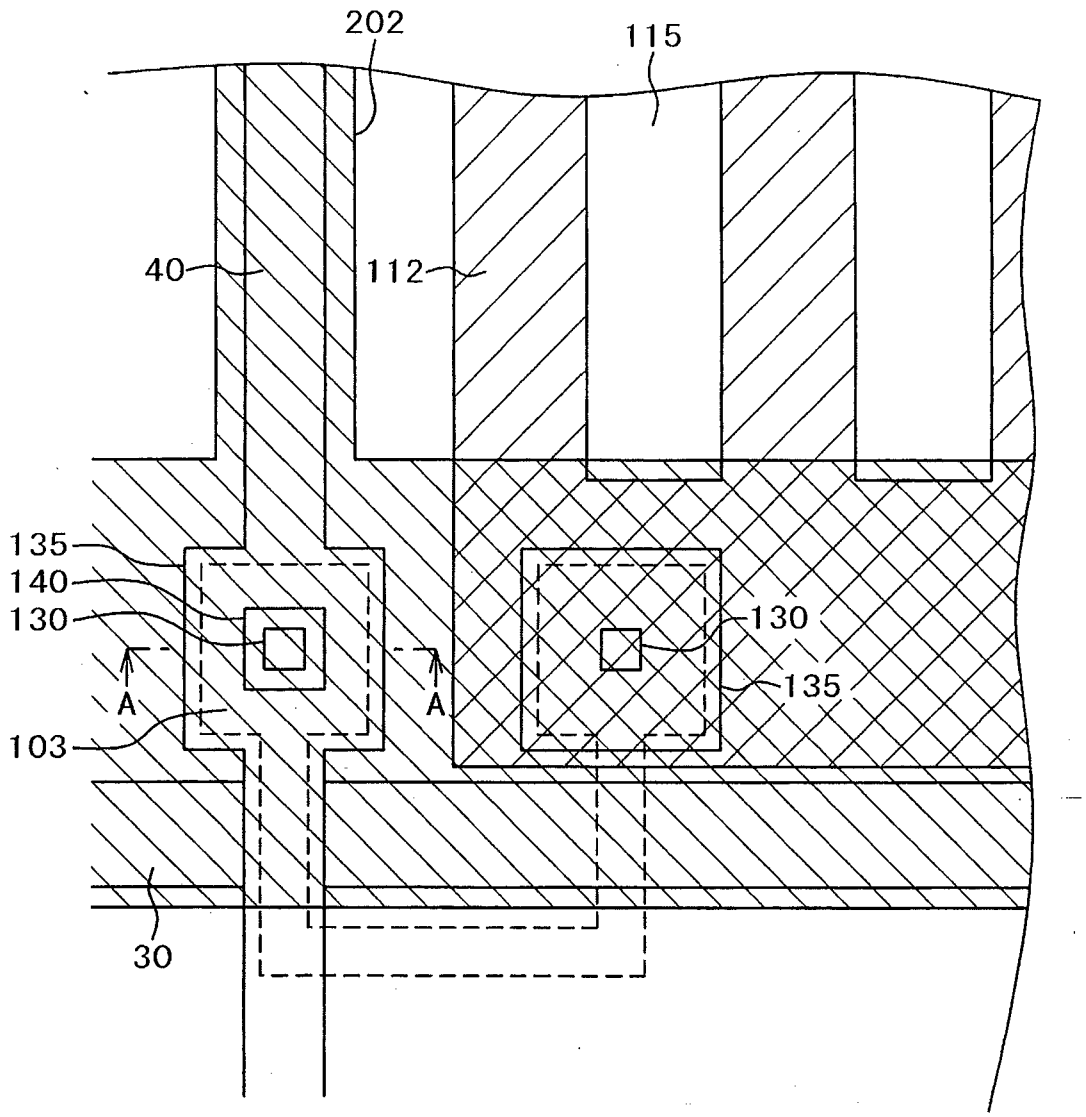


FIG. 3

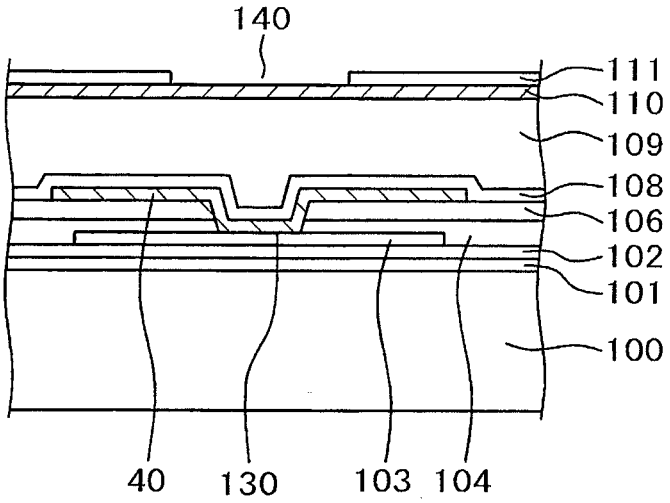

140
111
110
109
108
106
102
101
100
40
130
103
104

FIG. 4

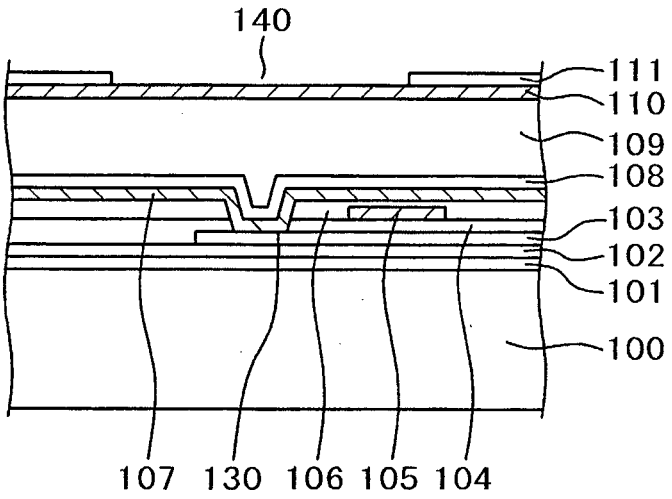

140
111
110
109
108
103
102
101
100
107
130
106
105
104

FIG. 5

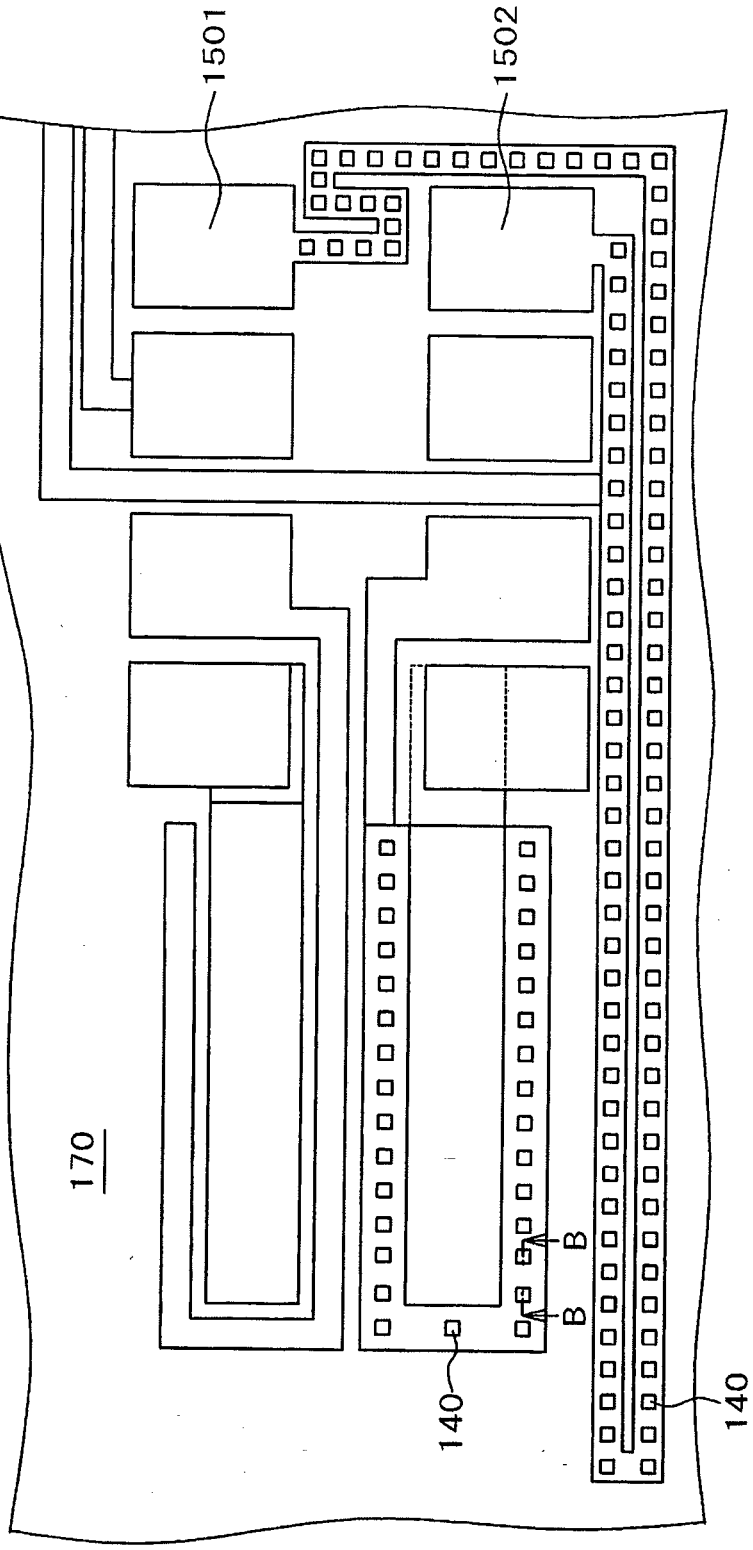


FIG. 6

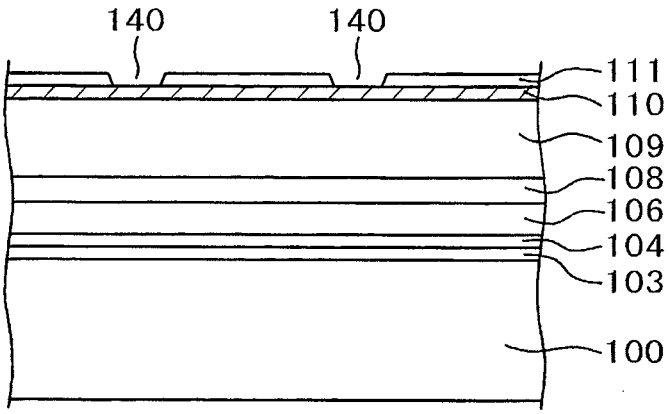


FIG. 7

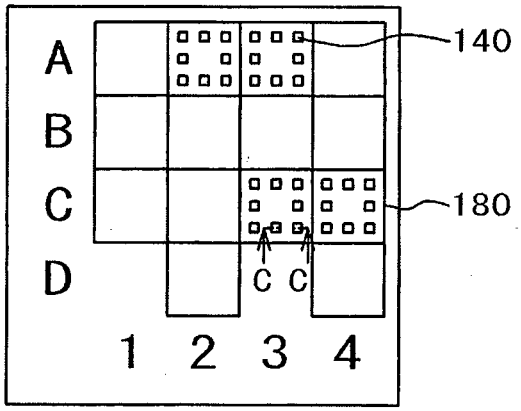


FIG. 8

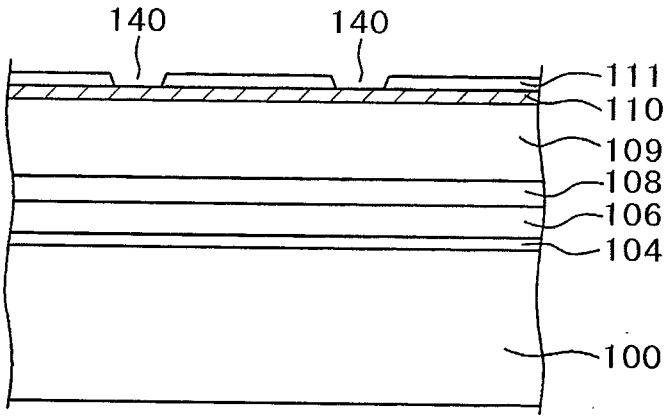
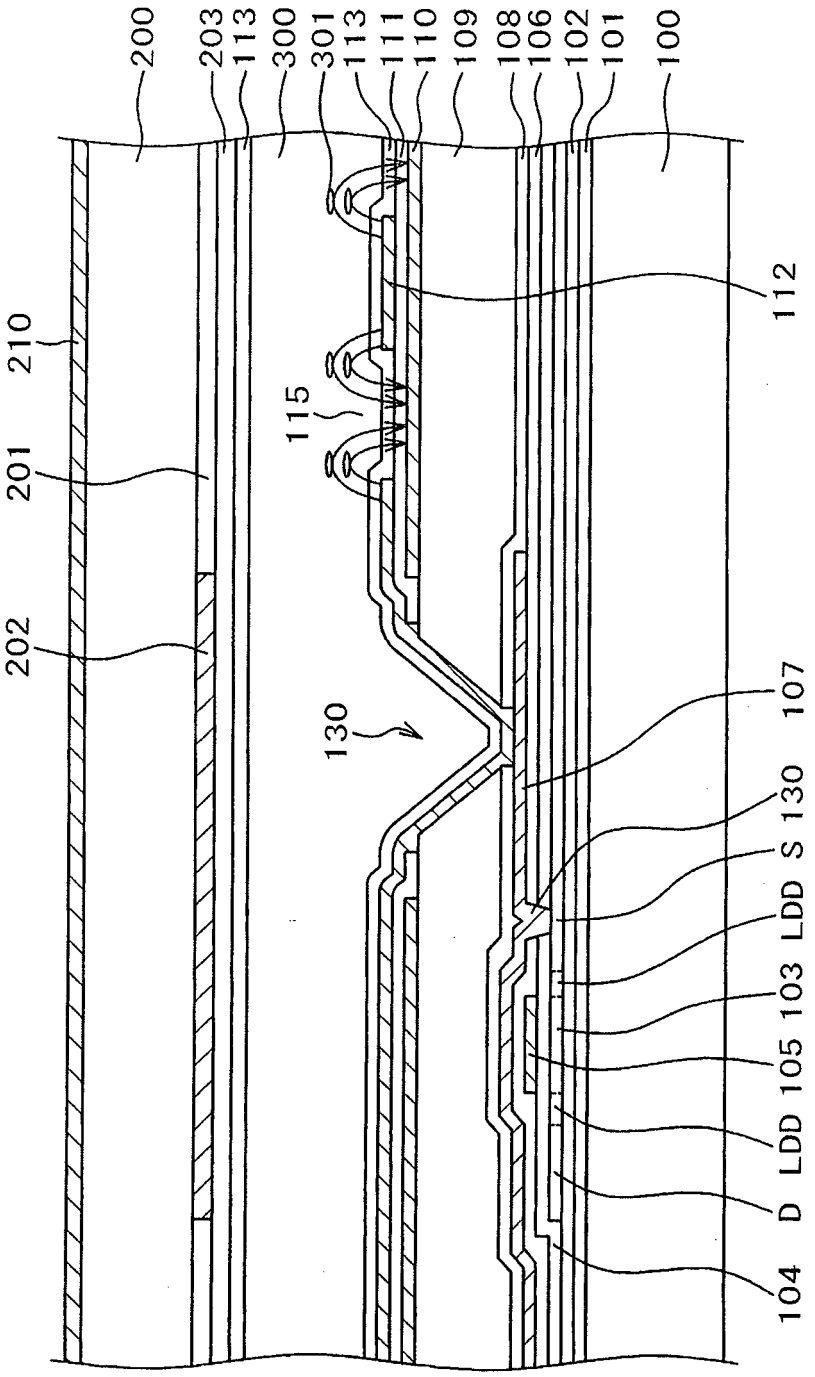


FIG. 9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D
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REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- JP 2009271103 A **[0001] [0005] [0006] [0025] [0026] [0027]**

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摘要(译)

在使用顶栅TFT的液晶显示装置中，形成接触孔（130）以连接到图像信号线（40）。依次形成无机钝化膜（108）和有机钝化膜（109）以覆盖其上形成有公共电极的TFT。然后，在公共电极上形成层间绝缘膜（106）。在层间绝缘膜（106）中形成用于释放气体的通孔（140）。通孔（140）的直径大于接触孔（130）的直径，以便能够容易地从有机钝化膜（109）释放气体，并且防止层间绝缘膜（106）从剥落。

FIG. 1