



(11) **EP 2 447 771 B1**

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention
of the grant of the patent:
11.05.2016 Bulletin 2016/19

(51) Int Cl.:
G02F 1/1343 ^(2006.01) **G02F 1/1362** ^(2006.01)

(21) Application number: **11008282.3**

(22) Date of filing: **13.10.2011**

(54) **High light transmittance in-plane switching liquid crystal display device**

Hohe Lichtübertragung in einer flachen Schaltungsflüssigkristallanzeigevorrichtung

Dispositif d'affichage à cristaux liquides à commutation dans le plan de forte transmission lumineuse

(84) Designated Contracting States:
**AL AT BE BG CH CY CZ DE DK EE ES FI FR GB
GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO
PL PT RO RS SE SI SK SM TR**

(30) Priority: **26.10.2010 KR 20100104590**

(43) Date of publication of application:
02.05.2012 Bulletin 2012/18

(73) Proprietor: **LG Display Co., Ltd.
Seoul 150-721 (KR)**

(72) Inventors:
• **Park, Seungryul
Goyang-si
Gyeonggi-do
411-734 (KR)**

• **Noh, Soyoung
Gwanak-gu
Seoul, 151-761 (KR)**

(74) Representative: **Ter Meer Steinmeister & Partner
Patentanwälte mbB
Nymphenburger Straße 4
80335 München (DE)**

(56) References cited:
**JP-A- 2003 149 664 US-A1- 2006 227 273
US-A1- 2009 174 854**

Note: Within nine months of the publication of the mention of the grant of the European patent in the European Patent Bulletin, any person may give notice to the European Patent Office of opposition to that patent, in accordance with the Implementing Regulations. Notice of opposition shall not be deemed to have been filed until the opposition fee has been paid. (Art. 99(1) European Patent Convention).

Description

[0001] This application claims the benefit of Korea Patent Application No. 10-2010-0104590 filed on October 26, 2010.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present disclosure relates to a high light transmittance in-plane switching liquid crystal display device. Especially, the present disclosure relates to a high light transmittance in-plane switching liquid crystal display device in which all problems shown in the horizontal electric field type liquid crystal display device, in which the pixel electrode and the common electrode are disposed in the same level plane, and the fringe field type liquid crystal display device, in which the pixel electrode and the common electrode are overlapped, are solved.

Discussion of the Related Art

[0003] The liquid crystal display device (or "LCD") represents video data by controlling the light transmittance of the liquid crystal layer using the electric fields driven by thin film transistor (or "TFT"). According to the direction of the electric field, the LCD can be classified in the two major types; one is vertical electric field type and the other is the horizontal electric field type.

[0004] For the vertical electric field type LCD, the common electrode formed on the upper substrate and the pixel electrode formed on the lower substrate are facing with each other for forming the electric field of which direction is perpendicular to the substrate face. The twisted nematic (TN) liquid crystal layer disposed between the upper substrate and the lower substrate is driven the vertical electric field. The vertical electric field type LCD has merit of higher aperture ratio, while it has demerit of narrower view angle about 90 degree.

[0005] For the horizontal electric field type LCD, the common electrode and the pixel electrode are formed on the same substrate in parallel. The liquid crystal layer disposed between the upper substrate and the lower substrate is driven in In-Plane-Switching (IPS) mode by the electric field parallel to the substrate face. The horizontal electric field type LCD has a merit of wider view angle over 170 degrees and faster response speed than the vertical electric field type LCD.

[0006] However, for the case of the horizontal electric field type LCD in which the pixel electrode and the common electrode are disposed on the same level plane, even though the horizontal electric field is formed between the pixel electrode and the common electrode, there is no electric field just over the pixel electrode and the common electrode. Therefore, the area occupied by the pixel electrode and the common electrode is to be the non-transmittance area at which the liquid crystal is

not driven. Consequently, even the pixel electrode and the common electrode is made of a transparent material, they cannot contribute the transmittance area and then the aperture ratio will be reduced by their area.

[0007] In order to above mentioned problem, the fringe field type LCD is suggested in which the common electrode corresponding to most of all portions of the pixel area is formed at under layer, and the pixel electrode is formed upper layer by overlapping with the common electrode. In the fringe field type LCD, as the horizontal electric field is formed over the pixel electrode, the high aperture ratio can be ensured. However, the fringe field type LCD can ensure high aperture ratio at only small area LCDs. When the LCD size is larger, the parasitic capacitance formed between the common electrode and the pixel electrode is also increased. To solve this problem, the size of the transistor should be getting larger and the gap between the pixel electrodes will be narrower, so that the transmittance will be lowered.

[0008] JP 2003 149664 A describes a liquid crystal display device. Within one pixel, a first pixel electrode and a second pixel electrode are provided. Each pixel electrode has a comb-like structure, wherein the pixel electrodes are engaged with each other. Further, a rectangular, sheet-like common electrode is provided. This document discloses the features of the preamble of claim 1.

[0009] US 2006/0227273 A1 describes a liquid crystal display apparatus. The liquid crystal display apparatus operated in horizontal electric field switching mode may include, within each pixel, first and second pixel electrodes.

SUMMARY OF THE INVENTION

[0010] In order to overcome the above mentioned drawbacks, the object of the present disclosure is to suggest a high light transmittance in-plane switching liquid crystal display device in which the horizontal electric field is formed at the space between the common electrode and the pixel electrode and the space over the pixel electrode and the common electrode. Another object of the present disclosure is to suggest a high light transmittance in-plane switching liquid crystal display device in which the parasitic capacitance formed between the common electrode and the pixel electrode is reduced when the horizontal electric field is formed by the fringe electric field type LCD.

[0011] The objects are solved by the features of claim 1.

[0012] In order to accomplish the above purpose, the present disclosure suggests a horizontal electric field type liquid crystal display device preferably comprising: a substrate; a plurality of gate lines disposed in horizontal direction on the substrate; a plurality of data lines disposed in vertical direction on the substrate; a plurality of pixel area defined by the cross-ing the plurality of the gate lines and the plurality of the data lines; a first pixel electrode having a plurality of segments arraying with a

predetermined distance within the pixel area; a second pixel electrode having a plurality of segments arraying in parallel with the first pixel electrode within the pixel area; and a common electrode overlapping with the first pixel electrode and the second pixel electrode within the pixel area.

[0013] The first pixel electrode and the second pixel electrode are formed on the same level layer, and the common electrode is overlapping with the first pixel electrode and the second pixel electrode with having an insulating layer therebetween.

[0014] The common electrode has a width which is 2 ~ 3 times wider than any one width of the first pixel electrode and the second pixel electrode.

[0015] The first pixel electrode and the second pixel electrode are alternately disposed and being apart from each other with distance of 8 μ m ~ 10 μ m.

[0016] The common electrode configured to be supplied with a voltage of which level is half of a maximum voltage difference between the pixel electrode and the second pixel electrode.

[0017] The first pixel electrode and the second pixel electrode are configured to have a voltage level difference having one value from 0V to 5V therebetween to form a horizontal electric field; and the common electrode, the first pixel electrode and the second pixel electrode are configured to have a voltage level difference having one value from 0V to 2.5V between the common electrode and the first pixel electrode and between the common electrode and the second pixel electrode to form a fringe field horizontal electric field.

[0018] The device further comprises a first thin film transistor formed at one corner of the pixel area and connected to the first pixel electrode; and a second thin film transistor formed at another corner of the pixel area and connected to the second pixel electrode.

[0019] The first thin film transistor is connected to a gate line disposed at one horizontal side of the pixel area and a first data line disposed at a first vertical side of the pixel area; and the second thin film transistor is connected to the gate line and a second data line disposed at a second vertical side of the pixel area.

[0020] The first thin film transistor includes a first gate electrode branched from the gate line, a first source electrode branched from the first data line, and a first drain electrode facing with the first source electrode; and the second thin film transistor includes a second gate electrode branched from the gate line, a second source electrode branched from the second data line, and a second drain electrode facing with the second source electrode.

[0021] The first thin film transistor is connected to a first gate line disposed at a first horizontal side of the pixel area, and a first data line disposed at a first vertical side of the pixel area; and the second thin film transistor is connected to a second gate line disposed at a second side of the pixel area, and a second data line disposed at a second vertical side of the pixel area.

[0022] The first thin film transistor includes a first gate

electrode branched from the first gate line, a first source electrode branched from the first data line, and a first drain electrode facing with the first source electrode; and the second thin film transistor includes a second gate electrode branched from the second gate line, a second source electrode branched from the second data line, and a second drain electrode facing with the second source electrode.

[0023] The horizontal electric field type LCD according to the present disclosure includes a first pixel electrode and a second pixel electrode which are formed on the same level plane to form a first horizontal electric field between them, and a common electrode formed under the first and second pixel electrodes to form a second electric field between the pixel electrode and the common electrode. As the horizontal electric field is formed over the pixel electrode, the electrode area can be used as the liquid crystal driving area so high light transmittance is ensured. Furthermore, as the overlapping area of the common electrode and the pixel electrode to form the horizontal electric field over the pixel electrode can be minimized and the gap between the pixel electrodes is ensured to minimize the amount of the parasitic capacitance. That is, as the in-plane switching type LCD according to the present disclosure has the merits of the horizontal electric field type LCD and the fringe field type LCD and overcomes the demerits of them, the present disclosure can suggest a high light transmittance LCD having lower driving power consumption.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention.

[0025] In the drawings:

FIG. 1 is the plane view illustrating the structure of the high light transmittance in-plane switching liquid crystal display device according to the first embodiment of the present disclosure.

FIG. 2 is the cross-sectional view illustrating the structure of the high light transmittance in-plane switching liquid crystal display device according to the first embodiment by cutting along the line I-I'.

FIG. 3 is the plane view illustrating the structure of the high light transmittance in-plane switching liquid crystal display device according to the second embodiment of the present disclosure.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

[0026] Hereinafter, referring to attached figures 1 to 3, we will explain preferred embodiments of the present dis-

closure. FIG. 1 is the plane view illustrating the structure of the high light transmittance in-plane switching liquid crystal display device according to the first embodiment of the present disclosure. FIG. 2 is the cross-sectional view illustrating the structure of the high light transmittance in-plane switching liquid crystal display device according to the first embodiment by cutting along the line I-I'.

[0027] Referring to Figs. 1 and 2, high light transmittance in-plane switching LCD includes a plurality of pixel areas defined by a plurality of gate lines running to the horizontal direction over a transparent substrate SUB and a plurality of data lines running to the vertical direction over the transparent substrate SUB which are crossing each other. A first thin film transistor T1 is disposed at one corner of each pixel area, and a second thin film transistor T2 is disposed the other corner of each pixel area. The first thin film transistor T1 is connected to a first pixel electrode PXL1 formed in the comb shape in which a plurality of segments are disposed with a first predetermined gap within the pixel area. The second thin film transistor T2 is also connected to a second pixel electrode PXL2 formed in the comb shape in which a plurality of segments are disposed with a second predetermined gap within the pixel area.

[0028] The first TFT T1 and the second TFT T2 are connected to the first gate electrode G1 and the second gate electrode G2 which are branched from the same gate line GL, respectively. The first source electrode S1 branched from the first data line DL1 is overlapped with one side of the first gate electrode G1. The first drain electrode D1 facing with the first source electrode S1 and being apart from the first source electrode S1 with a predetermined distance is overlapped with the other side of the first gate electrode G1. The first drain electrode D1 is connected to the first pixel electrode PXL1. Even though it is not shown in figures, the first semiconductor layer is disposed between the first gate electrode G1 and the first source-drain electrodes S1-D1 to play role of channel layer.

[0029] Furthermore, the second source electrode S2 branched from the second data line DL2 is overlapped with one side of the second gate electrode G2. The second drain electrode D2 facing with the second source electrode S2 and being apart from the second source electrode S2 with a predetermined distance is overlapped with the other side of the second gate electrode G2. The second drain electrode D2 is connected to the second pixel electrode PXL2. Even though it is not shown in figures, the second semiconductor layer is disposed between the second gate electrode G2 and the second source-drain electrodes S2-D2 to play role of channel layer.

[0030] The first pixel electrode PXL1 and the second pixel electrode PXL2 have a comb shape in which a plurality of segments are disposed with a predetermined distance between them. Furthermore, each segments of the first pixel electrode PXL1 and the second pixel electrode

PXL2 are alternately disposed each other. That is, one segment of the first pixel electrode PXL1 and one segment of the second pixel electrode PXL2 are closely disposed on the same level plane to form a horizontal electric field therebetween.

[0031] When a scan signal is supplied to a gate line GL, the first TFT T1 and the second TFT T2 turn on at the same time, and then the pixel signal is supplied to the first pixel electrode PXL1 and the second pixel electrode PXL2 at the same time. In order to form a horizontal electric field between the first pixel electrode PXL1 and the second pixel electrode PXL2, they should have different voltage levels. For example, the first pixel electrode PXL1 preferably has the voltage range changing from 0V to 5V, while the second pixel electrode PXL2 preferably has the voltage range changing from 5V to 0V, so that the voltage level different can be any one of from 0V to 5V. Consequently, it is possible to drive the liquid crystal molecules with the horizontal electric field formed between the first pixel electrode PXL1 and the second pixel electrode PXL2, and to represent the video data.

[0032] With this structure, especially when the distance between the first pixel electrode PXL1 and the second pixel electrode PXL2 is almost three times of the width of the pixel electrodes themselves PXL1 and PXL2, the horizontal electric field is formed at the space between the pixel electrodes PXL1 and PXL2, but there is no horizontal electric field just over the pixel electrodes themselves PXL1 and PXL2. Therefore, the liquid crystal molecules disposed over the pixel electrodes PXL1 and PXL2 cannot be driven. It is more preferable to make that the horizontal electric field is formed over the pixel electrodes themselves PXL1 and PXL2.

[0033] To do so, in the first embodiment of the present disclosure, a common electrode COM is further included which is disposed under the pixel electrodes PXL1 and PXL2 to be overlapped with them and has a wider width than the pixel electrodes PXL1 and PXL2. For example, the common electrode COM can be formed on the same level layer with the gate line GL and the gate electrodes G1 and G2, and made of a transparent conductive material. Furthermore, a common line CL can be disposed parallel with the gate line GL for supplying the common voltage to the common electrode COM. The common electrode COM and the pixel electrodes PXL1 and PXL2 are overlapped each other with having the gate insulating layer GI and the passivation layer PAS therebetween.

[0034] Referring to FIG. 2 again, more detailed structure is explained hereinafter. In order that the horizontal electric field is formed over the pixel electrodes themselves PXL1 and PXL2, it is preferable that the common electrode COM has wider width than those of pixel electrodes PXL1 and PXL2. As a result, a fringe field is formed between the surfaces of the pixel electrodes PXL1 and PXL2 and the edge of the common electrode COM. Due to this fringe field, the horizontal electric field can be formed over the pixel electrodes PXL1 and PXL2. The

width of the common electrode COM is preferably 2-3 times of the width of the pixel electrodes PXL1 and PXL2. In other words, the edge of the common electrode COM is preferably protruded from the edges of the pixel electrodes PXL1 and PXL2 with a length which is $1/2 \sim 3/4$ times of the width of the pixel electrodes PXL1 and PXL2. That is, it is preferable that the overlapped gap G of the common electrode COM and the pixel electrode PXL1 and PXL2 is $1/2 \sim 3/4$ times of the width of the pixel electrodes PXL1 and PXL2.

[0035] In addition, when the horizontal electric field due to the fringe field is formed between the common electrode COM and the pixel electrodes PXL1 and PXL2, the strength of the fringe field can be decided by considering the horizontal electric field formed between the first pixel electrode PXL1 and the second pixel electrode PXL2. For example, the common electrode COM can be supplied with the 2.5V level which is the middle level of the maximum difference voltage level between the first pixel electrode PXL1 and the second pixel electrode PXL2.

[0036] The strength of the horizontal electric field formed between the first pixel electrode PXL1 and the second pixel electrode PXL2 is defined by the voltage difference between the voltage level of the first pixel electrode PXL1 and the voltage level of the second pixel electrode PXL2. That is, the voltage difference between the first pixel electrode PXL1 and the second pixel electrode PXL2 is any one value from 0V to 5V. As the common electrode has the constant voltage level of 2.5V, the fringe field having the voltage difference of any one from 0V to 2.5V is formed between the common electrode COM and the pixel electrodes PXL1 and PXL2.

[0037] Consequently, in the liquid crystal display device according to the first embodiment of the present disclosure, the horizontal electric field is formed overall of the pixel area. Therefore, it is possible for the present disclosure to suggest a high light transmittance in-plane switching liquid crystal display device in which most of all area of the pixel region can be used as the light transmittance area.

[0038] Hereinafter, referring to FIG. 3, the second embodiment of the present disclosure will be explained. FIG. 3 is the plane view illustrating the structure of the high light transmittance in-plane switching liquid crystal display device according to the second embodiment of the present disclosure. The cross sectional structure of the horizontal electric field type LCD according to the second embodiment is very similar with that of the first embodiment. The difference is just on the arraying of the first TFT T1 and the second TFT T2.

[0039] Referring to FIG. 3, the high light transmittance in-plane switching liquid crystal display device according to the second embodiment comprises a plurality of pixel area defined by the crossing structure of a plurality of gate lines running to the horizontal direction on a transparent substrate SUB and a plurality of data lines running to the vertical direction on the transparent substrate SUB. A first TFT T1 is disposed at one corner of the pixel area,

and a second TFT T2 is disposed at another corner of the pixel area. The first TFT T1 is connected to a first pixel electrode PXL1 formed as a comb shape in the pixel area. The second TFT T2 is connected to a second pixel electrode PXL2 formed as a comb shape in the pixel area.

[0040] The first TFT T1 is connected to a first gate electrode G1 branched from a first gate line GL1, and the second TFT T2 is connected to a second gate electrode G2 branched from a second gate line GL2. In addition, a first source electrode S1 branched from a first data line DL1 is overlapped with one side of the first gate electrode G1. A first drain electrode D1 facing with the first source electrode S1 and being apart from the first source electrode S1 with a predetermined distance is overlapped with the other side of the first gate electrode G1. The first drain electrode D1 is connected to the first pixel electrode PXL1. Even though it is not shown in figures, a first semiconductor layer is disposed between the first gate electrode G1 and the first source-drain electrodes S1-D1, to play a role of channel.

[0041] Furthermore, the second source electrode S2 branched from the second data line DL2 is overlapped with one side of the second gate electrode G2. The second drain electrode D2 facing with the second source electrode S2 and being apart from the second source electrode S2 with a predetermined distance is overlapped with the other side of the second gate electrode G2. The second drain electrode D2 is connected to the second pixel electrode PXL2. Even though it is not shown in figures, the second semiconductor layer is disposed between the second gate electrode G2 and the second source-drain electrodes S2-D2 to play role of channel layer.

[0042] The first pixel electrode PXL1 and the second pixel electrode PXL2 have a comb shape in which a plurality of segments are disposed with a predetermined distance between them. Furthermore, each segments of the first pixel electrode PXL1 and the second pixel electrode PXL2 are alternately disposed each other. That is, one segment of the first pixel electrode PXL1 and one segment of the second pixel electrode PXL2 are closely disposed on the same level plane to form a horizontal electric field therebetween.

[0043] In the second embodiment, the first TFT T1 turns on when the first gate line GL1 is selected, and the second TFT T2 turns on when the second gate line GL2 is selected previously on the first gate line GL1. Therefore, there is time delay between when the first pixel electrode PXL1 is charged and when the second pixel electrode PXL2 is charged. However, during one picture frame is represented, the charged voltages to each pixel electrodes PXL1 and PXL2 are maintained, so that a horizontal electric field between the pixel electrodes PXL1 and PXL2 is formed.

[0044] As explained above, the difference between the first embodiment and the second embodiment is on the arraying structure of the thin film transistors T1 and T2 for forming the horizontal electric field between the pixel

electrodes PXL1 and PXL2, but there is no difference on the arraying structure of the common electrode COM and the pixel electrodes PXL1 and PXL2. In the present disclosure, the main electric field for driving the liquid crystal molecules is the horizontal electric field formed between the first pixel electrode PXL1 and the second pixel electrode PXL2. The horizontal electric field due to the fringe field formed between the common electrode COM and the pixel electrodes PXL1 and PXL2 contributes to drive the liquid crystal molecules disposed over the pixel electrodes themselves PXL1 and PXL2. Consequently, according to the present disclosure, the horizontal electric field is formed overall pixel area including the space just over the pixel electrodes PXL1 and PXL2.

[0045] Furthermore, the horizontal electric field due to the fringe field does make effect on the common electrode COM disposed just under its pixel electrode not on the neighboring common electrode COM. Therefore, there is a merit that it is possible to reduce the parasitic capacitance between the pixel electrode and the common electrode.

[0046] In addition, in the pixel area, as two pixel electrodes are driving using two thin film transistors, it is possible to make the driving voltage be lower. In other words, with the same driving voltage, it is possible to design the pixel electrodes to be disposed with longer distance. For example, the gap (A) between the pixel electrodes PXL1 and PXL2 can be 8~10μm which is longer than 7μm used in conventional one. Actually, when the widths of the first pixel electrode PXL1 and the second pixel electrode PXL2 would be 2μm, the gap between the pixel electrodes PXL1 and PXL2 would be 10μm, the width of the common electrode COM would be 4μm, and the gap between the common electrodes COM would be 8μm, the light transmittance can be increased at least 20%. Here, the gap (B) between the common electrodes COM is defined by the gap (A) between the pixel electrodes PXL1 and PXL2 and the overlapped area (G) between the common electrode COM and the pixel electrodes PXL1 and PXL2.

[0047] While the embodiment of the present invention has been described in detail with reference to the drawings, it will be understood by those skilled in the art that the invention can be implemented in other specific forms without changing the essential features of the invention. Therefore, it should be noted that the foregoing embodiments are merely illustrative in all aspects and are not to be construed as limiting the invention. The scope of the invention is defined by the appended claims rather than the detailed description of the invention. All changes or modifications or their equivalents made within the meanings and scope of the claims should be construed as falling within the scope of the invention.

Claims

1. A horizontal electric field type liquid crystal display

device comprising:

a substrate (SUB);
a plurality of gate lines (GL1, GL2) disposed in horizontal direction on the substrate (SUB);
a plurality of data lines (DL1, DL2) disposed in vertical direction on the substrate (SUB);
a plurality of pixel areas defined by the crossing the plurality of the gate lines (GL1, GL2) and the plurality of the data lines (DL1, DL2); each pixel area comprising
a first pixel electrode (PXL1) having a plurality of segments separated by a predetermined distance from each other within the pixel area;
a second pixel electrode (PXL2) having a plurality of segments arranged in parallel to and interdigitated with the segments of the first pixel electrode (PXL1) within the pixel area; and

characterized by

a common electrode (COM) comprising segments corresponding to the segments of the first pixel electrode (PXL1) and the second pixel electrode (PXL2), which segments overlap with the respective segments of the first pixel electrode (PXL1) and the second pixel electrode (PXL2) within each pixel area, wherein the segments of the common electrode have a width wider than the width of the segments of the first pixel electrode (PXL1) and the second pixel electrode (PXL2).

2. The device according to the claim 1, wherein the first pixel electrode (PXL1) and the second pixel electrode (PXL2) are formed on the same level layer, and the common electrode (COM) is overlapping with the first pixel electrode (PXL1) and the second pixel electrode (PXL2) with having an insulating layer (GI) therebetween.
3. The device according to the claim 1, wherein the width of the segments of the common electrode (COM) is 2 ~ 3 times wider than any one width of the segments of the first pixel electrode (PXL1) and the second pixel electrode (PXL2).
4. The device according to the claim 1, wherein the first pixel electrode (PXL1) and the second pixel electrode (PXL2) are alternately disposed and being apart from each other with distance of 8μm ~ 10μm.
5. The device according to the claim 1, wherein the common electrode (COM) configured to be supplied with a voltage of which level is half of a maximum voltage difference between the first pixel electrode (PXL1) and the second pixel electrode (PXL2).

6. The device according to the claim 5, wherein the first pixel electrode (PXL1) and the second pixel electrode (PXL2) are configured to have a voltage level difference having one value from 0V to 5V therebetween to form a horizontal electric field; and wherein the common electrode (COM), the first pixel electrode (PXL1) and the second pixel electrode (PXL2) are configured to have a voltage level difference having one value from 0V to 2.5V between the common electrode (COM) and the first pixel electrode (PXL1) and between the common electrode (COM) and the second pixel electrode (PXL2) to form a fringe field horizontal electric field.

7. The device according to the claim 1, further comprising:

a first thin film transistor (T1) formed at one corner of the pixel area and connected to the first pixel electrode (PXL1); and
a second thin film transistor (T2) formed at another corner of the pixel area and connected to the second pixel electrode (PXL2).

8. The device according to the claim 7, wherein the first thin film transistor (T1) is connected to a gate line (GL) disposed at one horizontal side of the pixel area and a first data line (DL1) disposed at a first vertical side of the pixel area; and wherein the second thin film transistor (T2) is connected to the gate line (GL) and a second data line (DL2) disposed at a second vertical side of the pixel area.

9. The device according to the claim 8, wherein the first thin film transistor (T1) includes a first gate electrode (G1) branched from the gate line (GL), a first source electrode (S1) branched from the first data line (DL1), and a first drain electrode (D1) facing with the first source electrode (S1); and wherein the second thin film transistor (T2) includes a second gate electrode (G2) branched from the gate line (GL), a second source electrode (S2) branched from the second data line (DL2), and a second drain electrode (D2) facing with the second source electrode (S2).

10. The device according to the claim 7, wherein the first thin film transistor (T1) is connected to a first gate line (GL1) disposed at a first horizontal side of the pixel area, and a first data line (DL1) disposed at a first vertical side of the pixel area; and wherein the second thin film transistor (T2) is connected to a second gate line (GL2) disposed at a second side of the pixel area, and a second data line (DL2) disposed at a second vertical side of the pixel area.

11. The device according to the claim 10, wherein the first thin film transistor (T1) includes a first gate electrode (G1) branched from the first gate line (GL1), a first source electrode (S1) branched from the first data line (DL1), and a first drain electrode (D1) facing with the first source electrode (S1); and wherein the second thin film transistor (T2) includes a second gate electrode (G2) branched from the second gate line (GL2), a second source electrode (S2) branched from the second data line (DL2), and a second drain electrode (D2) facing with the second source electrode (S2).

Patentansprüche

1. Flüssigkristallanzeigevorrichtung des Typs mit horizontalem elektrischem Feld, wobei die Vorrichtung Folgendes umfasst:

ein Substrat (SUB);
mehrere Gate-Leitungen (GL1, GL2), die in horizontaler Richtung auf dem Substrat (SUB) angeordnet sind;
mehrere Datenleitungen (DL1, DL2), die in vertikaler Richtung auf dem Substrat (SUB) angeordnet sind;
mehrere Pixelbereiche, die durch die Kreuzung der mehreren Gate-Leitungen (GL1, GL2) und der mehreren Datenleitungen (DL1, DL2) definiert sind; wobei jeder Pixelbereich Folgendes umfasst:

eine erste Pixelelektrode (PXL1), die mehrere Abschnitte besitzt, die innerhalb des Pixelbereichs durch einen vorgegebenen Abstand voneinander getrennt sind;
eine zweite Pixelelektrode (PXL2), die mehrere Abschnitte besitzt, die innerhalb des Pixelbereichs zu den Abschnitten der ersten Pixelelektrode (PXL1) parallel angeordnet sind und mit diesen interdigital sind; und

dadurch gekennzeichnet, dass

eine gemeinsame Elektrode (COM), die Abschnitte umfasst, die den Abschnitten der ersten Pixelelektrode (PXL1) und der zweiten Pixelelektrode (PXL2) entsprechen, wobei jene Abschnitte mit den jeweiligen Abschnitten der ersten Pixelelektrode (PXL1) und der zweiten Pixelelektrode (PXL2) innerhalb jedes Pixelbereichs überlappen, wobei die Abschnitte der gemeinsamen Elektrode eine Breite besitzen, die breiter als die Breite der Abschnitte der ersten Pixelelektrode (PXL1) und der zweiten Pixelelektrode (PXL2) ist.

2. Vorrichtung nach Anspruch 1, wobei die erste Pixelelektrode (PXL1) und die zweite Pixelelektrode (PXL2) auf der Schicht gleicher Ebene gebildet sind und die gemeinsame Elektrode (COM) mit der ersten Pixelelektrode (PXL1) und der zweiten Pixelelektrode (PXL2) überlappt und dazwischen eine isolierende Schicht (GI) besitzt. 5
3. Vorrichtung nach Anspruch 1, wobei die Breite der Abschnitte der gemeinsamen Elektrode (COM) 2 bis 3 mal breiter als eine Breite des Abschnitts der ersten Pixelelektrode (PXL1) oder der zweiten Pixelelektrode (PXL2) ist. 10
4. Vorrichtung nach Anspruch 1, wobei die erste Pixelelektrode (PXL1) und die zweite Pixelelektrode (PXL2) abwechselnd angeordnet sind und einen Abstand von 8 μm bis 10 μm voneinander besitzen. 15
5. Vorrichtung nach Anspruch 1, wobei die gemeinsame Elektrode (COM) konfiguriert ist, eine Spannung zugeführt zu bekommen, deren Pegel die Hälfte einer maximalen Spannungsdifferenz zwischen der ersten Pixelelektrode (PXL1) und der zweiten Pixelelektrode (PXL2) beträgt. 20
6. Vorrichtung nach Anspruch 5, wobei die erste Pixelelektrode (PXL1) und die zweite Pixelelektrode (PXL2) so konfiguriert sind, dass sie eine Spannungspegeldifferenz besitzen, die einen Wert im Bereich von 0V bis 5V besitzt, um ein horizontales elektrisches Feld zu erzeugen; und wobei die gemeinsame Elektrode (COM), die erste Pixelelektrode (PXL1) und die zweite Pixelelektrode (PXL2) so konfiguriert sind, dass sie eine Spannungspegeldifferenz besitzen, die zwischen der gemeinsamen Elektrode (COM) und der ersten Pixelelektrode (PXL1) und zwischen der gemeinsamen Elektrode (COM) und der zweiten Pixelelektrode (PXL2) einen Wert im Bereich von 0V bis 2,5 V besitzt, um ein Fransenfeld des horizontalen elektrischen Feldes zu bilden. 30 35 40
7. Vorrichtung nach Anspruch 1, die ferner Folgendes umfasst: 45
 - einen ersten Dünnschichttransistor (T1), der an einer Ecke des Pixelbereichs gebildet ist und mit der ersten Pixelelektrode (PXL1) verbunden ist; und
 - einen zweiten Dünnschichttransistor (T2), der an einer anderen Ecke des Pixelbereichs gebildet ist und mit der zweiten Pixelelektrode (PXL2) verbunden ist. 50
8. Vorrichtung nach Anspruch 7, wobei der erste Dünnschichttransistor (T1) mit einer Gate-Leitung (GL), die bei einer horizontalen Seite des Pixelbereichs 5
 - angeordnet ist, und einer ersten Datenleitung (DL1), die bei einer ersten vertikalen Seite des Pixelbereichs angeordnet ist, verbunden ist; und
 - wobei der zweite Dünnschichttransistor (T2) mit der Gate-Leitung (GL) und einer zweiten Datenleitung (DL2), die bei einer zweiten vertikalen Seite des Pixelbereichs angeordnet ist, verbunden ist.
9. Vorrichtung nach Anspruch 8, wobei der erste Dünnschichttransistor (T1) eine erste Gate-Elektrode (G1), die von der Gate-Leitung (GL) abzweigt, eine erste Source-Elektrode (S1), die von der ersten Datenleitung (DL1) abzweigt, und eine erste Drain-Elektrode (D1), die der ersten Source-Elektrode (S1) zugewandt ist, umfasst; und wobei der zweite Dünnschichttransistor (T2) eine zweite Gate-Elektrode (G2), die von der Gate-Leitung (GL) abzweigt, eine zweite Source-Elektrode (S2), die von der zweiten Datenleitung (DL2) abzweigt, und eine zweite Drain-Elektrode (D2), die der zweiten Source-Elektrode (S2) zugewandt ist, umfasst. 10 15 20 25
10. Vorrichtung nach Anspruch 7, wobei der erste Dünnschichttransistor (T1) mit einer ersten Gate-Leitung (GL1), die bei einer ersten horizontalen Seite des Pixelbereichs angeordnet ist, und einer ersten Datenleitung (DL1), die bei einer ersten vertikalen Seite des Pixelbereichs angeordnet ist, verbunden ist; und wobei der zweite Dünnschichttransistor (T2) mit einer zweiten Gate-Leitung (GL2), die bei einer zweiten Seite des Pixelbereichs angeordnet ist, und einer zweiten Datenleitung (DL2), die bei einer zweiten vertikalen Seite des Pixelbereichs angeordnet ist, verbunden ist. 30 35 40
11. Vorrichtung nach Anspruch 10, wobei der erste Dünnschichttransistor (T1) eine erste Gate-Elektrode (G1), die von der ersten Gate-Leitung (GL1) abzweigt, eine erste Source-Elektrode (S1), die von der ersten Datenleitung (DL1) abzweigt, und eine erste Drain-Elektrode (D1), die der ersten Source-Elektrode (S1) zugewandt ist, umfasst; und wobei der zweite Dünnschichttransistor (T2) eine zweite Gate-Elektrode (G2), die von der zweiten Gate-Leitung (GL2) abzweigt, eine zweite Source-Elektrode (S2), die von der zweiten Datenleitung (DL2) abzweigt, und eine zweite Drain-Elektrode (D2), die der zweiten Source-Elektrode (S2) zugewandt ist, umfasst. 45 50

Revendications

1. Dispositif d'affichage à cristaux liquides de type à champ électrique horizontal comprenant :
 - un substrat (SUB) ;

une pluralité de lignes de grille (GL1, GL2) disposées dans un sens horizontal sur le substrat (SUB) ;
 une pluralité de lignes de données (DL1, DL2) disposées dans un sens vertical sur le substrat (SUB) ;
 une pluralité de zones de pixels définies par l'intersection de la pluralité de lignes de grille (GL1, GL2) et de la pluralité de lignes de données (DL1, DL2) ;
 chaque zone de pixels comprenant :

une première électrode de pixel (PXL1) comprenant une pluralité de segments séparés d'une distance prédéterminée l'un de l'autre à l'intérieur de la zone de pixels ;
 une deuxième électrode de pixel (PXL2) comprenant une pluralité de segments agencés en parallèle aux segments de la première électrode de pixel (PXL1) à l'intérieur de la zone de pixels et entrecroisés avec ceux-ci ; et

caractérisé par

une électrode commune (COM) comprenant des segments correspondant aux segments de la première électrode de pixel (PXL1) et de la deuxième électrode de pixel (PXL2), les segments de l'électrode commune chevauchant les segments respectifs de la première électrode de pixel (PXL1) et de la deuxième électrode de pixel (PXL2) dans chaque zone de pixels, dans lequel les segments de l'électrode commune ont une largeur supérieure à la largeur des segments de la première électrode de pixel (PXL1) et de la deuxième électrode de pixel (PXL2).

2. Dispositif selon la revendication 1, dans lequel la première électrode de pixel (PXL1) et la deuxième électrode de pixel (PXL2) sont formées sur la couche de même niveau, et l'électrode commune (COM) chevauche la première électrode de pixel (PXL1) et la deuxième électrode de pixel (PXL2) ayant une couche d'isolation (GI) entre elles.
3. Dispositif selon la revendication 1, dans lequel la largeur des segments de l'électrode commune (COM) est 2 à 3 fois supérieure à l'une quelconque des largeurs des segments de la première électrode de pixel (PXL1) et de la deuxième électrode de pixel (PXL2).
4. Dispositif selon la revendication 1, dans lequel la première électrode de pixel (PXL1) et la deuxième électrode de pixel (PXL2) sont disposées en alternance en étant séparées l'une de l'autre d'une distance de 8 μm à 10 μm .

5. Dispositif selon la revendication 1, dans lequel l'électrode commune (COM) est configurée pour être alimentée avec une tension dont le niveau est égal à la moitié d'une différence de tension maximale entre la première électrode de pixel (PXL1) et la deuxième électrode de pixel (PXL2).
6. Dispositif selon la revendication 5, dans lequel la première électrode de pixel (PXL1) et la deuxième électrode de pixel (PXL2) sont configurées pour avoir une différence de niveau de tension d'une valeur de 0 V à 5 V entre elles afin de former un champ électrique horizontal ; et
 dans lequel l'électrode commune (COM), la première électrode de pixel (PXL1) et la deuxième électrode de pixel (PXL2) sont configurées pour avoir une différence de niveau de tension d'une valeur de 0 V à 2,5 V entre l'électrode commune (COM) et la première électrode de pixel (PXL1) et entre l'électrode commune (COM) et la deuxième électrode de pixel (PXL2) afin de former un champ électrique horizontal de champ de dispersion.
7. Dispositif selon la revendication 1, comprenant en outre :
 un premier transistor à film mince (T1) formé à un coin de la zone de pixels et relié à la première électrode de pixel (PXL1) ; et
 un deuxième transistor à film mince (T2) formé à un autre coin de la zone de pixels et relié à la deuxième électrode de pixel (PXL2).
8. Dispositif selon la revendication 7, dans lequel le premier transistor à film mince (T1) est relié à une ligne de grille (GL) disposée à un côté horizontal de la zone de pixels et une première ligne de données (DL1) disposée à un premier côté vertical de la zone de pixels ; et
 dans lequel le deuxième transistor à film mince (T2) est relié à la ligne de grille (GL) et à une deuxième ligne de données (DL2) disposée à un deuxième côté vertical de la zone de pixels.
9. Dispositif selon la revendication 8, dans lequel le premier transistor à film mince (T1) comprend une première électrode de grille (G1) ramifiée de la ligne de grille (GL), une première électrode de source (S1) ramifiée de la première ligne de données (DL1), et une première électrode de drain (D1) faisant face à la première électrode de source (S1) ; et
 dans lequel le deuxième transistor à film mince (T2) comprend une deuxième électrode de grille (G2) ramifiée de la ligne de grille (GL), une deuxième électrode de source (S2) ramifiée de la deuxième ligne de données (DL2), et une deuxième électrode de drain (D2) faisant face à la deuxième électrode de source (S2).

10. Dispositif selon la revendication 7, dans lequel le premier transistor à film mince (T1) est relié à une première ligne de grille (GL1) disposée à un premier côté horizontal de la zone de pixels, et une première ligne de données (DL1) disposée à un premier côté vertical de la zone de pixels ; et
dans lequel le deuxième transistor à film mince (T2) est relié à une deuxième ligne de grille (GL2) disposée à un deuxième côté de la zone de pixels, et une deuxième ligne de données (DL2) disposée à un deuxième côté vertical de la zone de pixels.
11. Dispositif selon la revendication 10, dans lequel le premier transistor à film mince (T1) comprend une première électrode de grille (G1) ramifiée de la première ligne de grille (GL1), une première électrode de source (S1) ramifiée de la première ligne de données (DL1), et une première électrode de drain (D1) faisant face à la première électrode de source (S1) ;
et
dans lequel le deuxième transistor à film mince (T2) comprend une deuxième électrode de grille (G2) ramifiée de la deuxième ligne de grille (GL2), une deuxième électrode de source (S2) ramifiée de la deuxième ligne de données (DL2), et une deuxième électrode de drain (D2) faisant face à la deuxième électrode de source (S2).

5

10

15

20

25

30

35

40

45

50

55

FIG. 1

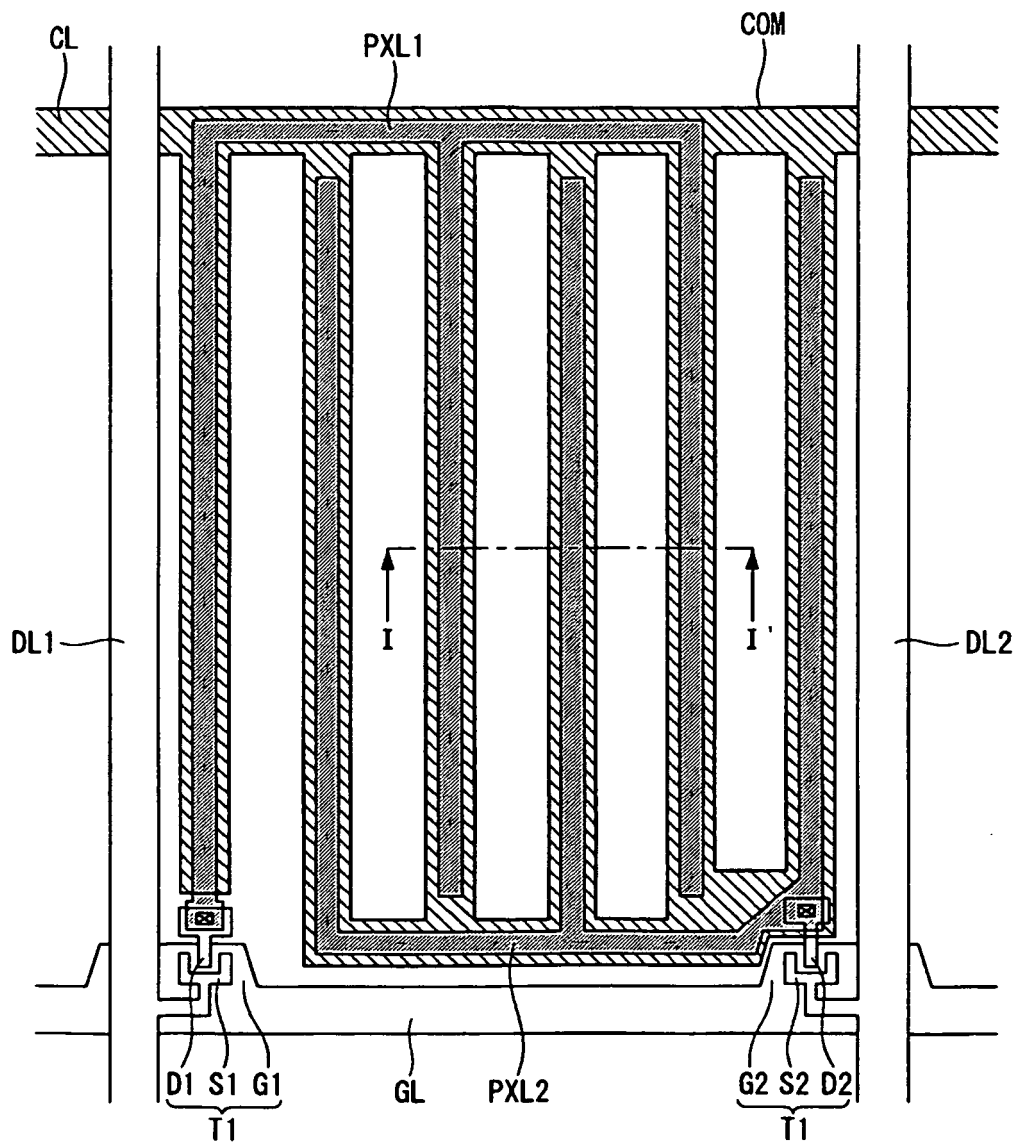


FIG. 2

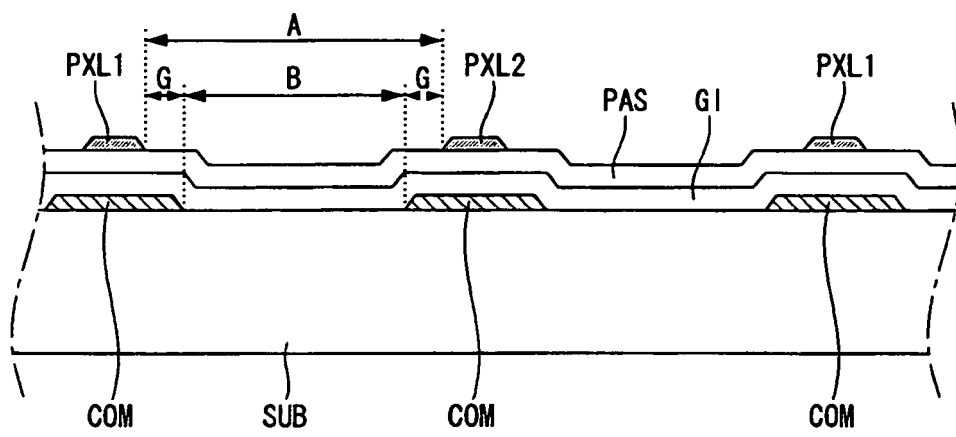
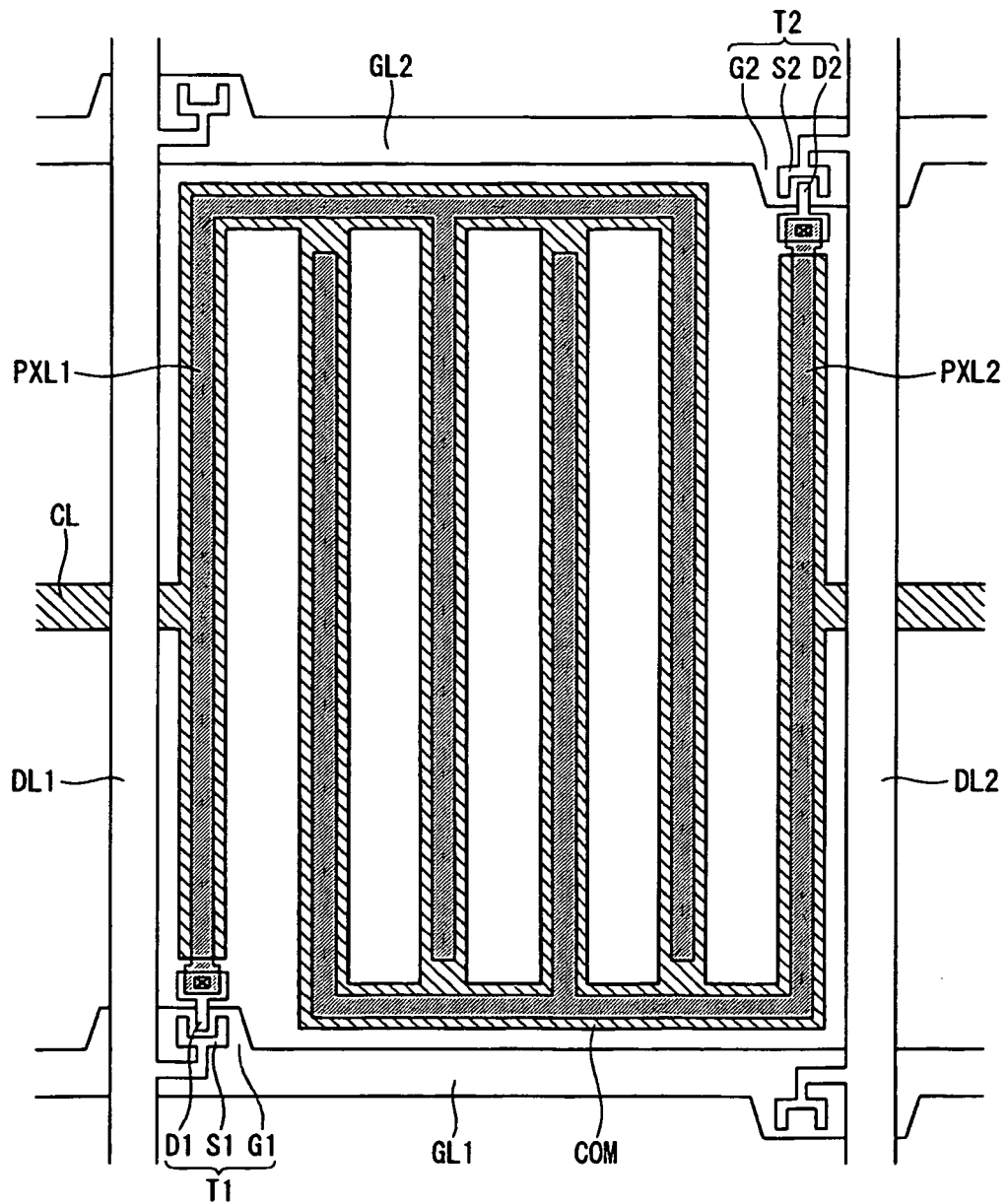


FIG. 3



REFERENCES CITED IN THE DESCRIPTION

This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

Patent documents cited in the description

- KR 1020100104590 [0001]
- JP 2003149664 A [0008]
- US 20060227273 A1 [0009]

专利名称(译)	高透光率面内切换液晶显示装置		
公开(公告)号	EP2447771B1	公开(公告)日	2016-05-11
申请号	EP2011008282	申请日	2011-10-13
[标]申请(专利权)人(译)	乐金显示有限公司		
申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
当前申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
[标]发明人	PARK SEUNGRYUL NOH SOYOUNG		
发明人	PARK, SEUNGRYUL NOH, SOYOUNG		
IPC分类号	G02F1/1343 G02F1/1362		
CPC分类号	G02F1/13624 G02F1/134309 G02F2001/134372 G02F2201/121 G02F2201/124		
优先权	1020100104590 2010-10-26 KR		
其他公开文献	EP2447771A1		
外部链接	Espacenet		

摘要(译)

本发明涉及一种高透光率面内切换液晶显示装置。本发明提出一种水平电场型液晶显示装置，包括：基板（SUB）；多个栅极线（G）设置在基板上的水平方向上；多个数据线（DL）沿垂直方向设置在基板上；多个像素区域，由多条栅极线和多条数据线交叉限定；第一像素电极（PXL1），具有在像素区域内以预定距离排列的多个区段；第二像素电极（PXL2），具有与像素区域内的第一像素电极（PXL1）平行排列的多个区段；公共电极（COM）与像素区域内的第一像素电极（PXL1）和第二像素电极（PXL2）重叠。

FIG. 1

