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(54) DISPLAY APPARATUS, LIQUID CRYSTAL DISPLAY APPARATUS, DRIVE METHOD FOR DISPLAY APPARATUS, AND TELEVISION RECEIVER

ANZEIGEVORRICHTUNG, FLÜSSIGKRISTALLANZEIGEVORRICHTUNG, ANTRIEBSVERFAHREN FÜR DIE ANZEIGEVORRICHTUNG UND FERNSEHEMPFÄNGER

APPAREIL D'AFFICHAGE, APPAREIL D'AFFICHAGE À CRISTAUX LIQUIDES, PROCÉDÉ DE COMMANDE POUR APPAREIL D'AFFICHAGE ET RÉCEPTEUR DE TÉLÉVISION

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Description

Technical Field

[0001] The present invention relates to a liquid crystal display apparatus in which data signals whose polarities are reversed per set period are supplied to data signal lines.

Background Art

[0002] With liquid crystal display apparatuses, source signals (shape of potential of data signal lines) round due to generation of parasitic resistance, parasitic capacitors and the like in the data signal lines. Particularly, when driving a large-sized liquid crystal panel, in a case where two temporally adjacent gate pulses are provided successively without having an interval therebetween, a rounded part of a source signal that corresponds to a preceding stage is written into a beginning of a horizontal scanning period. In view of this, JP 2008/009368 A discloses a method of providing a set interval between one and another of two temporally adjacent gate pulses (see Fig. 35).

[0003] A general data signal line drive method is a method which supplies data signals whose polarities are reversed per horizontal scanning period (1H) (1H reversal driving). However with this method, as a size of the liquid crystal panel increases and as speed is increased for high-speed driving, the rounding of the data signal increases in degree. As a result, problems arise such as that a pixel charging rate decreases and that electricity consumption increases. Accordingly, alternative drive methods are starting to be employed, such as (i) a method which supplies, to data signal lines, data signals in which their polarities are reversed per vertical scanning period or per a plurality of vertical scanning periods, while in one horizontal scanning period, supplies a data signal having a polarity to one of two data signal lines and outputting another data signal having another polarity to the other of the two data signal lines, which two data signal lines are arranged adjacent to each other (1V reversal driving or nV reversal driving), or (ii) a method which supplies, to data signal lines, data signals in which their polarities are reversed per plurality of horizontal scanning periods, while in one horizontal scanning period, supplies a data signal having a polarity to one of two data signal lines and outputting another data signal having another polarity to the other of the two data signal lines, which two data signal lines are arranged adjacent to each other (nH reversal driving). In the following description, the 1V reversal driving, the nV reversal driving, and the nH reversal driving are together referred to as long-term (LT) reversal driving.

[0004] US 2006/0044292 A1 shows a liquid crystal display driving device of matrix structure type and a driving method. The driving device consists of a group of thin film transistors with matrix array, a plurality of gate lines and a plurality of data lines. The object of increasing response speed can be accomplished by the different arrangement of gate lines and data lines and the different connection between each thin film transistor and the gate and data lines. The driving method for the said driving device includes: each pair of gate lines in the display panel are simultaneously and orderly turned on at different time of driving transistor, and the different driving voltages are orderly applied to the thin film transistors connected to the gate lines.; The structure and method can suit for picture treating of various displays such as liquid crystal display, organic light-emitting diode (OLED) display or plasma display panel (PDP).

[0005] US 2006/0208984 A1 shows a display device. The display device has a pixel including a first subpixel and a second subpixel; a first signal line connected to the first subpixel and transmitting a first signal; a second signal line connected to the second subpixel and transmitting a second signal; a third signal line intersecting the first and the second signal lines, connected to at least one of the first and the second subpixels, and transmitting a third signal; and a fourth signal line intersecting the first and the second signal lines and transmitting a fourth signal, wherein the first subpixel and the second subpixel are supplied with data voltages having different magnitude, and the data voltages applied to the first and the second subpixels are originated from a single image information.

Summary of Invention

Technical Problem

[0006] The inventors of the present invention found that the following problem occurs in the LT reversal driving if a set interval is provided between one and the other of two temporally adjacent gate pulses as illustrated in Fig. 35.

[0007] Namely, a ripple (wavelike variation) generates in an electric potential of the data signal line at a time of rise (at a start of a scanning period) and fall (at a termination of the scanning period) of the gate pulse, caused by the parasitic capacitor generated at an intersection of the data signal line and the scanning signal line. Further, as the distance increases from the supply source of the data signal (as the parasitic resistance of the data signal lines increases), the ripple increases in size, as illustrated in Fig. 36. This causes the display quality to decrease, for example causes a color change in a lower part of the screen, which part is away from
the source driver. It is considered that this is caused due to the LT reversal driving (i) supplying data signals of a single

polarity for a long period of time to the same data signal lines, and (ii) actualizing a parasitic capacitor between the data signal lines conjointly with the high definition of the liquid crystal panel, since an electric potential of any one of the data signal lines and a data signal line disposed adjacent to that any one of the data signal lines on one of its sides always are of reversed polarities. Moreover, such a deterioration in display quality is remarkable in a case where two scanning signal lines are selected simultaneously.

[0008] An object of the present invention is to improve display quality of a liquid crystal display apparatus that carries out LT reverse driving.

Solution to Problem

[0009] The invention is defined by the subject matter of the independent claims. Advantageous embodiments are subject to the dependent claims.

[0010] According to the invention, at a timing at which a set of N lines of the scanning signal lines is deactivated, another set of N lines of the scanning signal lines is activated; hence, an effect (e.g., fall of electric potential) received by the data signal lines due to the deactivation of the set of N lines of scanning signal lines (e.g., fall of N scanning pulses) is basically canceled by the effect (e.g., rise of electric potential) received by the data signal lines due to activating the set of N lines of scanning signal lines (e.g., rise of N scanning pulses). This allows for reducing the ripple (wavelike variation) generating in the electric potential of the data signal lines also in the LT reversal driving, which allows for preventing a phenomenon that the size of the ripple increases as the supply source of the data signal becomes more distant (see Fig. 36), thereby improving display quality.

Advantageous Effects of Invention

[0011] As described above, according to the present display apparatus, it is possible to reduce the ripple (wavelike variation) generated in the electric potential of the data signal line in the LT reversal driving, which allows for preventing a phenomenon that the size of the ripple increases as the supply source of the data signals becomes more distant, thereby improving the display quality.

Brief Description of Drawings

[0012]

Fig. 1 is a timing chart illustrating a driving method of a liquid crystal display apparatus according to Embodiment 1.
Fig. 2 is an equivalent circuit diagram illustrating a configuration of a liquid crystal panel according to Embodiment 1.
Fig. 3 is a schematic view illustrating a display state of a liquid crystal display apparatus which is driven by the driving method of Fig. 1.
Fig. 4 is a timing chart illustrating another driving method of a liquid crystal display apparatus according to an implementation example.
Fig. 5
Fig. 5 is a plan view illustrating a specific example of the liquid crystal panel of Fig. 2.
Fig. 6 is a cross sectional view of the liquid crystal panel of Fig. 5.
Fig. 7 is a plan view illustrating another specific example of the liquid crystal panel illustrated in Fig. 2.
Fig. 8 is a cross sectional view of the liquid crystal panel of Fig. 7.
Fig. 9 is a schematic view illustrating how to repair a disconnection of a data signal line in a liquid crystal panel according to Embodiment 1.
Fig. 10 is an equivalent circuit diagram of another configuration of the liquid crystal panel according to Embodiment 1.
Fig. 11 is a timing chart illustrating a driving method of a liquid crystal display apparatus including the liquid crystal panel of Fig. 10.
Fig. 12 is a schematic view illustrating a display state of a liquid crystal display apparatus which is driven by the driving method of Fig. 11.
Fig. 13 is an equivalent circuit diagram illustrating a configuration of a liquid crystal panel according to Embodiment 2.
Fig. 14 is a timing chart illustrating a driving method of a liquid crystal display apparatus according to Embodiment 2.
Fig. 15 is a schematic view illustrating a display state of a liquid crystal display apparatus which is driven by the driving method of Fig. 14.
Fig. 16 is a timing chart illustrating another driving method of a liquid crystal display apparatus according to another implementation example.
Fig. 17 is a plan view illustrating a specific example of the liquid crystal panel of Fig. 13.
Fig. 18 is a cross sectional view illustrating the liquid crystal panel of Fig. 17.

Fig. 19 is an equivalent circuit diagram illustrating a configuration of a liquid crystal panel according to Embodiment 3.
Fig. 20 is a timing chart illustrating a driving method of a liquid crystal display apparatus according to Embodiment 3.
Fig. 21 is a schematic view illustrating a display state of a liquid crystal display apparatus which is driven by the driving method of Fig. 20.
Fig. 22 is an equivalent circuit diagram illustrating a configuration of a liquid crystal panel according to Embodiment 4.
Fig. 23 is a timing chart illustrating a driving method of a liquid crystal display apparatus according to Embodiment 4.
Fig. 24 is a schematic view illustrating a display state of a liquid crystal display apparatus which is driven by the driving method of Fig. 23.
Fig. 25 is an equivalent circuit diagram illustrating a configuration of a liquid crystal panel according to an implementation example.
Fig. 26 is a timing chart illustrating a driving method of a liquid crystal display apparatus according to an implementation example.
Fig. 27 is a schematic view illustrating a display state of a liquid crystal display apparatus which is driven by the driving method of Fig. 26.
Fig. 28 is an equivalent circuit diagram illustrating a configuration of a liquid crystal panel according to another implementation example.
Fig. 29 is a timing chart illustrating a driving method of a liquid crystal display apparatus according to another implementation example.
Fig. 30 is a timing chart illustrating another driving method of a liquid crystal display apparatus according to an implementation example.
Fig. 31 is a block diagram describing an entire configuration of the present liquid crystal display apparatus.
Fig. 32 is a block diagram describing functions of the present liquid crystal display apparatus.
Fig. 33 is a block diagram describing functions of the present television receiver.
Fig. 34 is an exploded perspective view illustrating a configuration of the present television receiver.
Fig. 35 is a timing chart illustrating a conventional driving method of a liquid crystal display apparatus.
Fig. 36 is a schematic view describing problems in using the driving method of Fig. 35 in LT reversal driving.

Description of Embodiments

[0013] Different embodiments and implementation examples are described below, with reference to Figs. 1 to 34. For convenience in description, a row direction hereafter denotes an extending direction of scanning signal lines. However, it is needless to say that the scanning signal lines may be extended in a sideways direction or an up-down direction in a used (viewed) state of a liquid crystal display apparatus including the present liquid crystal panel (or an active matrix substrate used in the present liquid crystal panel). Note that alignment control structures have been omitted from the drawings which illustrate the liquid crystal panel, as appropriate.

Embodiment 1

[0014] Fig. 2 is an equivalent circuit diagram illustrating a portion of a liquid crystal panel according to Embodiment 1. As illustrated in Fig. 2, in the present liquid crystal panel, data signal lines 15x, 15y, 15X, and 15Y are arranged in this order, and scanning signal lines 16i, 16j, 16m, 16n, 16w, and
16u, each of which extend in the row direction (left-right direction of Fig. 2) are arranged in this order. A pixel 101 is provided between intersections where the scanning signal line 16i intersects with the data signal lines 15x and 15y, a pixel 102 is provided between intersections where the scanning signal line 16j intersects with the data signal lines 15x and 15y, a pixel 103 is provided between intersections where the scanning signal line 16m intersects with the data signal lines 15x and 15y, a pixel 104 is provided between intersections where the scanning signal line 16n intersects with the data signal lines 15x and 15y, a pixel 105 is provided between intersections where the scanning signal line 16i intersects with the data signal lines 15X and 15Y, a pixel 106 is provided between intersections where the scanning signal line 16j intersects with the data signal lines 15X and 15Y, a pixel 107 is provided between intersections where the scanning signal line 16m intersects with the data signal lines 15X and 15Y, and a pixel 108 is provided between intersections where the scanning signal line 16n intersects with the data signal lines 15X and 15Y. A storage capacitor wire 18p is provided associated with the pixels 101 and 105, a storage capacitor wire 18q is provided associated with the pixels 102 and 106, a storage capacitor wire 18r is provided associated with the pixels 103 and 107, and a storage capacitor wire 18s is provided associated with the pixels 104 and 108.

[0015] Adjacent to a pixel column α which includes the pixels 101 to 104 is disposed a pixel column β which includes the pixels 105 to 108; the data signal lines 15x and 15y are provided associated with the pixel column α, and the data signal lines 15X and 15Y are provided associated with the pixel column β.

[0016] Furthermore, one pixel electrode is disposed per pixel; a pixel electrode 17i of the pixel 101 is connected to

the data signal line 15x via a transistor 12i that is connected to the scanning signal line 16i, a pixel electrode 17j of the pixel 102 is connected to the data signal line 15y via a transistor 12j that is connected to the scanning signal line 16j; a pixel electrode 17m of the pixel 103 is connected to the data signal line 15x via a transistor 12m that is connected to the scanning signal line 16m, a pixel electrode 17n of the pixel 104 is connected to the data signal line 15y via a transistor 12n that is connected to the scanning signal line 16n, a pixel electrode 17I of the pixel 105 is connected to the data signal line 15Y via a transistor 12I that is connected to the scanning signal line 16i, a pixel electrode 17J of the pixel 106 is connected to the data signal line 15X via a transistor 12J that is connected to the scanning signal line 16j, a pixel electrode 17M of the pixel 107 is connected to the data signal line 15Y via a transistor 12M that is connected to the scanning signal line 16m, and a pixel electrode 17N of the pixel 108 is connected to the data signal line 15X via a transistor 12N that is connected to the scanning signal line 16n.

[0017] The scanning signal line 16i connected to the pixel electrode 17i of the pixel 101 and connected to the pixel electrode 17I of the pixel 105, and the scanning signal line 16j connected to the pixel electrode 17j of the pixel 102 and connected to the pixel electrode 17J of pixel 106, are selected simultaneously (later described). Moreover, the scanning signal line 16m connected to the pixel electrode 17m of the pixel 103 and connected to the pixel electrode 17M of the pixel 107, and the scanning signal line 16n connected to the pixel electrode 17n of the pixel 104 and connected to the pixel electrode 17N of the pixel 108 are selected simultaneously (later described).

[0018] Moreover, respective storage capacitors are formed between the storage capacitor wire 18p and each of the pixel electrodes 17i and 17I, respective storage capacitors are formed between the storage capacitor wire 18q and each of the pixel electrodes 17j and 17J, respective storage capacitors are formed between the storage capacitor wire 18r and each of the pixel electrodes 17m and 17M, respective storage capacitors are formed between the storage capacitor wire 18s and each of the pixel electrodes 17n and 17N, and respective liquid crystal capacitors are formed between each of the pixel electrodes and a common electrode com.

[0019] Fig. 1 is a timing chart showing a driving method of the present liquid crystal display apparatus which includes the liquid crystal panel (normally black mode) of Fig. 2. Sx, Sy, SX, SY represent data signals (data signals) that are supplied to the data signal lines 15x, 15y, 15X, 15Y, respectively, and GPi, GPj, GPm, GPn, GPw, GPu represent gate pulse signals which are supplied to the scanning signal lines 16i, 16j, 16m, 16n, 16w, 16u, respectively. Moreover, (a) of Fig. 3 is a schematic view of a portion of Fig. 2, and (b) to (d) of Fig. 3 are schematic views illustrating a write state of the portion illustrated in (a) of Fig. 3, from a kth horizontal scanning period to a (k+2)th horizontal scanning period in Fig. 1.

[0020] As illustrated in Fig. 1, in the present driving method, two scanning signal lines are selected simultaneously, and data signals whose polarities are reversed per vertical scanning period (1V) are supplied to the data signal lines. In one vertical scanning period, data signals (signal potentials) respectively supplied to two data signal lines which are associated to one pixel column are made to have different polarities, and data signals that are respectively supplied to two adjacent data signal lines which each are associated to different pixel columns are made to have different polarities. At a timing in which two scanning pulses fall, two scanning pulses rise; simultaneously with a start of a horizontal scanning period corresponding to a current stage, a scanning pulse of the current stage rises, and simultaneously with a start of a horizontal scanning period corresponding to a subsequent stage (termination of the horizontal scanning period corresponding to the current stage), the scanning pulse of the current stage falls.

[0021] More specifically, in consecutive frames F1 and F2, F1 is driven by the following driving method. First, in F1, the data signal lines 15x and 15X receive data signals of a positive polarity, and the data signal lines 15y and 15Y receive data signals of a negative polarity.

[0022] Simultaneously with a start of a kth horizontal scanning period (i.e. switchover to a data signal corresponding to the kth horizontal scanning period), a pulse Pi of the gate pulse signal GPi and a pulse Pj of the gate pulse signal GPj rise, and simultaneously with a start of the (k+1)th horizontal scanning period (termination of the kth horizontal scanning period), the pulse Pi and the pulse Pj fall.

[0023] As a result, data signals of the positive polarity are written into the pixel electrode 17i of the pixel 101, data signals of the negative polarity are written into the pixel electrode 17j of the pixel 102, data signals of the negative polarity are written into the pixel electrode 17I of the pixel 105, and data signals of the positive polarity are written into the pixel electrode 17J of the pixel 106, as illustrated in (a) and (b) of Fig. 3.

[0024] Moreover, simultaneously with the start of the (k+1)th horizontal scanning period, a pulse Pm of the gate pulse signal GPm and a pulse Pn of the gate pulse signal GPn rise, and simultaneously with a start of a (k+2)th horizontal scanning period, the pulse Pm and the pulse Pn fall.

[0025] As a result, data signals of the positive polarity are written into the pixel electrode 17m of the pixel 103, data signals of the negative polarity are written into the pixel electrode 17n of the pixel 104, data signals of the negative polarity are written into the pixel electrode 17M of the pixel 107, and data signals of the positive polarity are written into the pixel electrode 17N of the pixel 108, as illustrated in (a) and (c) of Fig. 3.

[0026] Furthermore, simultaneously with the start of the (k+2)th horizontal scanning period, a pulse Pw of the gate pulse signal GPw and a pulse Pu of the gate pulse signal GPu rise, and simultaneously with a start of a (k+3)th horizontal scanning period, the pulse Pw and the pulse Pu fall. As a result, data signals having a polarity as illustrated in (d) of Fig.

3 are written into a pixel electrode connected to the scanning signal line 16w and into a pixel electrode connected to the scanning signal line 16u.

[0027] The above thus allows for achieving a dot-reversal polarity distribution of data signals written into the pixels, in F1.

[0028] On the other hand, the following drive method is performed in F2. First, in F2, the data signal lines 15x and 15X receive data signals of a negative polarity, and the data signal lines 15y and 15Y receive data signals of a positive polarity.

[0029] Simultaneously with a start of the kth horizontal scanning period (i.e. a switchover of data signals corresponding to the kth horizontal scanning period), the pulse Pi of the gate pulse signal Gpi and the pulse Pj of the gate pulse signal GPj rise, and simultaneously with the start of the (k+1)th horizontal scanning period (termination of the kth horizontal scanning period), the pulse Pi and the pulse Pj fall.

[0030] As a result, data signals of the negative polarity are written into the pixel electrode 17i of the pixel 101, data signals of the positive polarity are written into the pixel electrode 17j of the pixel 102, data signals of the positive polarity are written into the pixel electrode 17l of the pixel 105, and data signals of the negative polarity are written into the pixel electrode 17J of the pixel 106.

[0031] Moreover, simultaneously with the start of the (k+1)th horizontal scanning period, the pulse Pm of the gate pulse signal GPm and the pulse Pn of the gate pulse signal GPn rise, and simultaneously with the start of the (k+2)th horizontal scanning period, the pulse Pm and the pulse Pn fall.

[0032] As a result, data signals of the negative polarity are written into the pixel electrode 17m of the pixel 103, data signals of the positive polarity are written into the pixel electrode 17n of the pixel 104, data signals of the positive polarity are written into the pixel electrode 17M of the pixel 107, and data signals of the negative polarity are written into the pixel electrode 17N of the pixel 108.

[0033] Furthermore, simultaneously with the start of the (k+2)th horizontal scanning period, the pulse Pw of the gate pulse signal GPw and the pulse Pu of the gate pulse signal GPu rise, and simultaneously with the start of the (k+3)th horizontal scanning period, the pulse Pw and the pulse Pu fall.

[0034] The above thus allows for achieving a dot-reversal polarity distribution of the data signals written into each of the pixels, in F2 also.

[0035] In the present liquid crystal display apparatus, two scanning pulses rise at a timing in which two scanning pulses fall. Hence, an effect (fall of electric potential) received by the data signal lines due to the fall of the two scanning pulses are canceled out by an effect (rise of electric potential) received by the data signal lines due to the rise of the two scanning pulses. As a result, a ripple (wavelike variation) generated in the electric potential of the data signal line can be reduced even in the 1V reversal driving. This allows for preventing the phenomenon that the size of the ripple increases as a supply source of the data signal becomes more distant (see Fig. 36), thereby improving display quality.

[0036] Moreover, since it is possible to simultaneously select two scanning signal lines in the present liquid crystal display apparatus, it is possible to reduce a write time into the screen by half while causing no change to a write time of the pixels. Namely, the present liquid crystal display apparatus is suitable for high-speed driving such as double-speed driving (120 Hz drive) and the like.

[0037] Moreover, the present liquid crystal display apparatus is a configuration which accomplishes dot reversal driving while supplying data signals of an identical polarity to the data signal lines during a single vertical scanning period. Accordingly, the present liquid crystal display apparatus can also be said as suitable for achieving a large size and for achieving high-speed driving, as well as for achieving low power consumption.

[0038] In the drive method of Fig. 1, a scanning pulse of the current stage rises simultaneously with a start of a horizontal scanning period corresponding to the current stage, and the scanning pulse of the current stage falls simultaneously with the start of a horizontal scanning period corresponding to a subsequent stage (termination of the horizontal scanning period corresponding to the current stage). However, the driving method is not limited to this example. For instance, the method may be as illustrated in Fig. 4, in which the scanning pulse of the current stage rises simultaneously with the start of the horizontal scanning period corresponding to a preceding stage, and the scanning pulse of the current stage falls simultaneously with the start of the horizontal scanning period corresponding to a subsequent stage (termination of the horizontal scanning period of the current stage). In this case, the scanning pulse has a width of 2H.

[0039] More specifically, the pulse Pi and pulse Pj rise simultaneously with the start of (k-1)th horizontal scanning period, and the pulse Pm and pulse Pn rise simultaneously with the start of the kth horizontal scanning period; thereafter, simultaneously with the start of (k+1)th horizontal scanning period (termination of the kth horizontal scanning period), the pulse Pi and pulse Pj fall, whereas the pulse Pw and pulse Pu rise.

[0040] The driving method of Fig. 4 allows for precharging during a first half (1H) of the pulse and for carrying out a main charge during the second half (1H) of the pulse. This allows for improving the pixel charging rate. Of course in this case also, two scanning pulses rise at the timing in which two scanning pulses fall. This allows for preventing the phenomenon that the size of the ripple increases as the supply source of the data signal becomes more distant (see Fig. 36), thereby improving the display quality.

[0041] A specific example of the liquid crystal panel (portion including pixels 101, 102, 105, and 106) of Fig. 2 is

illustrated as a plan view in Fig. 5 and as a cross sectional view in Fig. 6. In an active matrix substrate of the present liquid crystal panel, the scanning signal lines 16i and 16j which extend in a row direction and the storage capacitor wires 18p and 18q which extend in the row direction are provided on a transparent substrate 31. A gate insulating film 43 is provided so as to cover these members, and on the gate insulating film 43, a metal layer is formed, which metal layer includes the data signal lines 15x, 15y, 15X, and 15Y each extending in the column direction, semiconductor layers (i layer and n+ layer) and source electrodes and drain electrodes for each of transistors 12i, 12j, 12I, and 12J, drain draw-out electrodes 27, capacitor electrodes 37, and extension wires 47. Moreover, an inorganic interlayer insulating film 25 is provided so as to cover the metal layer, and an organic interlayer insulating film 26 which is thicker than the inorganic interlayer insulating film 25 is formed on an upper layer of the inorganic interlayer insulating film 25. Furthermore, pixel electrodes 17i, 17j, 17I, and 17J are formed on the organic interlayer insulating film 26, and an alignment film 9 is formed so as to cover these pixel electrodes. The inorganic interlayer insulating film 25 and the organic interlayer insulating film 26 are hollowed through at a section in which contact holes 11 are opened; this allows for the pixel electrodes to be in contact with respective capacitor electrodes 37. Meanwhile, a color filter substrate 30 has a black matrix 13 and a colored layer (color filter layers) 14 formed on a glass substrate 32, and a common electrode (com) 28 is formed on an upper layer of these layers. Further, an alignment film 19 is provided so as to cover the common electrode 28.

[0042] In the present liquid crystal panel, for instance, an edge of the pixel electrode 17j on an upstream side in the scanning direction overlaps an edge of the scanning signal line 16i on a downstream side in the scanning direction, whereas an edge of the pixel electrode 17j on the downstream side in the scanning direction overlaps an edge of the scanning signal line 16j on the upstream side in the scanning direction. From a plan view perspective, two edges of the pixel electrode 17j which run along the column direction of the pixel electrode 17j cover the data signal line 15x and data signal line 15y, respectively. Moreover, a storage capacitor is formed in a part on which the capacitor electrode overlaps the storage capacitor wire in such a manner that a gate insulating film is sandwiched between the capacitor electrode and the storage capacitor wire.

[0043] Another specific example of the liquid crystal panel (portion including pixels 101, 102, 105, and 106) illustrated in Fig. 2 is illustrated in Fig. 7 as a plan view and in Fig. 8 as a cross sectional view thereof. In an active matrix substrate of the present liquid crystal panel, the scanning signal lines 16i and 16j which extend in a row direction and the storage capacitor wires 18p and 18q which extend in the row direction are provided on the transparent substrate 31. The gate insulating film 43 is provided so as to cover these members, and on the gate insulating film 43, a metal layer is formed, which metal layer includes: the data signal lines 15x, 15y, 15X, 15Y each extending in the column direction; semiconductor layers (i layer and n+ layer) and source electrode and drain electrode for each of transistors 12i, 12j, 12I, 12J; capacitor electrodes 37; and a common electrode com. Moreover, an inorganic interlayer insulating film 25 is provided so as to cover the metal layer. On the inorganic interlayer insulating film 25, comb-shaped pixel electrodes 17i, 17j, 17I, 17J are formed, and an alignment film 9 is formed so as to cover these pixel electrodes. The inorganic interlayer insulating film 25 is hollowed through at a section in which the contact hole 11 is formed; this allows for the pixel electrodes to be in contact with the capacitor electrode 37. Moreover, at where the contact hole 111 is formed, the gate insulating film 43 is hollowed through, whereby allowing for the common electrode com to be in contact with the storage capacitor wire. On the other hand, the color filter substrate 30 has a black matrix 13 and a colored layer (color filter layer) 14 formed on the glass substrate 32, and an alignment film 19 is formed thereon so as to cover these members.

[0044] In the present liquid crystal panel, a transmittance of liquid crystal is controlled by an oblique electric field generated between the comb-shaped pixel electrode and the common electrode com. Hence, it is possible to improve the viewing angle characteristics.

[0045] As illustrated in (a) of Fig. 9, it is preferable to provide a spare wire PW for correcting a disconnection of the data signal line in the present liquid crystal display apparatus. The spare wire PW is drawn around a display region, and for example in a case where the data signal line 15x becomes disconnected as illustrated in (b) of Fig. 9, the vicinity of an input end (closest part to the source driver) of the data signal line 15x and the vicinity of an output end (most distant part from the source driver) of the data signal line 15x are connected to each other via the spare wire PW (see (c) of Fig. 9). This allows for transmitting data signals to parts downstream of the disconnected part (part from the disconnected part to the output end) via the spare wire PW, and as a result can repair the disconnection of the data signal line 15x.

[0046] If there is the phenomenon that the size of the ripple increases as the supply source of the data signal becomes more distant (see Fig. 36), providing a spare wire would leave a repair mark since the size of the ripple in the part downstream of the disconnected part (particularly in the vicinity of the output end) becomes different from its surroundings. However, the present liquid crystal display apparatus allows for preventing such a phenomenon; hence, it is advantageous in a point that no repair mark is caused.

[0047] The present liquid crystal panel may be configured as illustrated in Fig. 10. Namely, one pixel electrode is disposed per pixel; the pixel electrode 17i of pixel 101 is connected to the data signal line 15x via the transistor 12i that is connected to the scanning signal line 16i, the pixel electrode 17j of the pixel 102 is connected to the data signal line 15y via the transistor 12j that is connected to the scanning signal line 16j, the pixel electrode 17m of the pixel 103 is connected to the data signal line 15x via the transistor 12m that is connected to the scanning signal line 16m, the pixel

electrode 17n of the pixel 104 is connected to the data signal line 15y via the transistor 12n that is connected to the scanning signal line 16n, the pixel electrode 17I of the pixel 105 is connected to the data signal line 15X via the transistor 12I that is connected to the scanning signal line 16i, the pixel electrode 17J of the pixel 106 is connected to the data signal line 15Y via the transistor 12J of the scanning signal line 16j, the pixel electrode 17M of the pixel 107 is connected to the data signal line 15X via the transistor 12M that is connected to the scanning signal line 16m, and the pixel electrode 17N of the pixel 108 is connected to the data signal line 15Y via the transistor 12N of the scanning signal line 16n.

[0048] In a case where a liquid crystal display apparatus including the liquid crystal panel of Fig. 10 is driven, a dot-reversal polarity distribution of data signals written into the pixels can be achieved in F1, as illustrated in (a) to (d) of Fig. 12, by supplying, in F1, data signals of the positive polarity to the data signal lines 15x and 15Y and supplying data signals of the negative polarity in the data signal lines 15y and 15X, as illustrated in Fig. 11. Moreover, the dot reversal polarity distribution of data signals to be written into the pixels can also be achieved in F2, by supplying, in F2, data signals of the negative polarity to the data signal lines 15x and 15Y and supplying the data signals of the positive polarity to the data signal lines 15y and 15X.

Embodiment 2

[0049] Fig. 13 is an equivalent circuit diagram illustrating a portion of a liquid crystal panel according to Embodiment 2. As illustrated in Fig. 13, in the present liquid crystal panel, the data signal lines 15x, 15y, 15X, and 15Y are arranged in this order, and the scanning signal lines 16i, 16j, 16m, and 16n, each of which extend in the row direction (left-right direction of Fig. 13) are arranged in this order. The pixel 101 is provided between intersections where the scanning signal line 16i intersects with the data signal lines 15x and 15y, the pixel 102 is provided between intersections where the scanning signal line 16j intersects with the data signal lines 15x and 15y, the pixel 103 is provided between intersections where the scanning signal line 16m intersects with the data signal lines 15x and 15y, the pixel 104 is provided between intersections where the scanning signal line 16n intersects with the data signal lines 15x and 15y, the pixel 105 is provided between intersections where the scanning signal line 16i intersects with the data signal lines 15X and 15Y, the pixel 106 is provided between intersections where the scanning signal line 16j intersects with the data signal lines 15X and 15Y, the pixel 107 is provided between intersections where the scanning signal line 16m intersects with the data signal lines 15X and 15Y, and the pixel 108 is provided between intersections where the scanning signal line 16n intersects with the data signal lines 15X and 15Y. A storage capacitor wire 18k is provided associated with the pixels 101 and 105, the storage capacitor wire 18p is provided associated with the pixels 101, 105, 102, 106, the storage capacitor wire 18q is provided associated with the pixels 102, 106, 103, 107, the storage capacitor wire 18r is provided associated with the pixels 103, 107, 104, 108, and the storage capacitor wire 18s is provided associated with the pixels 104, 108.

[0050] Adjacent to a pixel column α which includes the pixels 101 to 104 is disposed a pixel column β which includes the pixels 105 to 108; the data signal lines 15x and 15y are provided associated with the pixel column α, and the data signal lines 15X and 15Y are provided associated with the pixel column β.

[0051] Furthermore, two pixel electrodes are provided per pixel: a pixel electrode 17ia of the pixel 101 is connected to the data signal line 15x via a transistor 12ia that is connected to the scanning signal line 16i, and a pixel electrode 17ib of the pixel 101 is connected to the data signal line 15x via a transistor 12ib that is connected to the scanning signal line 16i; a pixel electrode 17ja of the pixel 102 is connected to the data signal line 15y via a transistor 12ja that is connected to the scanning signal line 16j, and a pixel electrode 17jb of the pixel 102 is connected to the data signal line 15y via a transistor 12jb that is connected to the scanning signal line 16j; a pixel electrode 17ma of the pixel 103 is connected to the data signal line 15x via a transistor 12ma that is connected to the scanning signal line 16m, and the pixel electrode 17mb of the pixel 103 is connected to the data signal line 15x via a transistor 12mb that is connected to the scanning signal line 16m; a pixel electrode 17na of the pixel 104 is connected to the data signal line 15y via a transistor 12na that is connected to the scanning signal line 16n, and a pixel electrode 17nb of the pixel 104 is connected to the data signal line 15y via a transistor 12nb that is connected to the scanning signal line 16n; a pixel electrode 17IA of the pixel 105 is connected to the data signal line 15Y via a transistor 12IA that is connected to the scanning signal line 16i, and a pixel electrode 17IB of the pixel 105 is connected to the data signal line 15Y via a transistor 12IB that is connected to the scanning signal line 16i; and a pixel electrode 17JA of the pixel 106 is connected to the data signal line 15X via a transistor 12JA that is connected to the scanning signal line 16j, and a pixel electrode 17JB of the pixel 106 is connected to the data signal line 15X via a transistor 12JB that is connected to the scanning signal line 16j.

[0052] Note that the scanning signal line 16i and the scanning signal line 16i are selected simultaneously, and the scanning signal line 16m and the scanning signal line 16n are selected simultaneously (later described).

[0053] Moreover, respective storage capacitors are formed between the storage capacitor wire 18k and each of the pixel electrodes 17ia and 17IA, respective storage capacitors are formed between the storage capacitor wire 18p and each of the pixel electrodes 17ib, 17IB, 17ja, and 17JA, respective storage capacitors are formed between the storage capacitor wire 18q and each of the pixel electrodes 17jb, 17JB, 17ma, and 17MA, and respective storage capacitors are formed between the storage capacitor wire 18r and each of the pixel electrodes 17mb, 17MB, 17na, and 17NA.

Moreover, respective liquid crystal capacitors are formed between each of the pixel electrodes and the common electrode com.

[0054] Fig. 14 is a timing chart illustrating a driving method of the present liquid crystal display apparatus including the liquid crystal panel (normally black mode) illustrated in Fig. 13. Note that Sx, Sy, SX, and SY represent data signals (data signals) supplied to the data signal lines 15x, 15y, 15X, and 15Y, respectively, GPi, GPj, GPm, and GPn represent gate pulse signals supplied to the scanning signal lines 16i, 16j, 16m, and 16n, respectively, and Csk, Csp, Csq, Csr and Css represent storage capacitor wire signals supplied to the storage capacitor wires 18k, 18p, 18q, 18r, and 18s, respectively. Moreover, (a) of Fig. 15 illustrates a schematic view of a portion of Fig. 14, and (b) and (c) of Fig. 15 are schematic views illustrating a write state of the portion illustrated in (a) of Fig. 15 from the kth horizontal scanning period to the (k+1)th horizontal scanning period in Fig. 14.

[0055] As illustrated in Fig. 14, in the present driving method, two scanning signal lines are selected simultaneously, and data signals whose polarities are reversed per vertical scanning period (1V) are supplied to the data signal lines. In a single vertical scanning period, data signals (signal potentials) respectively supplied to two data signal lines which are associated to one pixel column are made to have different polarities, and data signals that are respectively supplied to two adjacent data signal lines which each are associated to different pixel columns are made to have different polarities. At a timing in which two scanning pulses fall, two scanning pulses rise; simultaneously with a start of a horizontal scanning period corresponding to a current stage, a scanning pulse of the current stage rises, and simultaneously with a start of a horizontal scanning period corresponding to a subsequent stage (termination of the horizontal scanning period corresponding to the current stage), the scanning pulse of the current stage falls. Furthermore, to each of the storage capacitor wires, storage capacitor wire signals having reversed polarities per 4H (horizontal scanning period) are supplied.

[0056] More specifically, in consecutive frames F1 and F2, F1 is driven by the following driving method. First, in F1, the data signal lines 15x and 15X receive data signals of a positive polarity, and the data signal lines 15y and 15Y receive data signals of a negative polarity.

[0057] Simultaneously with a start of the kth horizontal scanning period (i.e. switchover to a data signal corresponding to the kth horizontal scanning period), a pulse Pi of the gate pulse signal GPi and a pulse Pj of the gate pulse signal GPj rise, and simultaneously with a start of the (k+1)th horizontal scanning period (termination of the kth horizontal scanning period), the pulse Pi and the pulse Pj fall. Furthermore, simultaneously with the start of the (k+1)th horizontal scanning period (termination of the kth horizontal scanning period), the storage capacitor wire signal Csk is reversed from the negative polarity to the positive polarity, and the storage capacitor wire signal Csp is reversed from the positive polarity to the negative polarity.

[0058] As a result, as illustrated in (a) and (b) of Fig. 15, the electric potential of the pixel electrode 17ia is of a positive polarity and its effective potential is higher than an electric potential of a data signal written in, thereby causing the sub pixel including the pixel electrode 17ia to be a bright sub-pixel, whereas the electric potential of the pixel electrode 17ib is of a positive polarity and its effective potential is lower than the electric potential of the data signal written in, thereby causing the sub pixel including the pixel electrode 17ib to be a dark sub-pixel. Moreover, an electric potential of the pixel electrode 17IA is of a negative polarity and its effective potential is higher than an electric potential of the data signal written in, thereby causing the sub pixel including the pixel electrode 17IA to be a dark sub-pixel, whereas the electric potential of the pixel electrode 17IB is of a negative polarity and its effective potential is lower than the electric potential of the data signal written in, thereby causing the sub pixel including the pixel electrode 17IB to be a bright sub-pixel. Moreover, the electric potential of the pixel electrode 17ja is of a negative polarity and its effective potential is lower than the electric potential of the data signal written in, thereby causing the sub pixel including the pixel electrode 17ja to be a bright sub-pixel, whereas the electric potential of the pixel electrode 17JA is of a positive polarity and its effective potential is lower than the electric potential of the data signal written in, thereby causing the sub pixel including the pixel electrode 17JA to be a dark sub-pixel. Moreover, a data signal of a negative polarity is written into the pixel electrode 17jb, and a data signal of a positive polarity is written into the pixel electrode 17JB.

[0059] Thereafter, simultaneously with the start of the (k+1)th horizontal scanning period, the pulse Pm of the gate pulse signal GPm and the pulse Pn of the gate pulse signal GPn rise, and simultaneously with the start of the (k+2)th horizontal scanning period, the pulse Pm and the pulse Pn fall. Furthermore, simultaneously with the start of the (k+2)th horizontal scanning period, the storage capacitor wire signal Csq is reversed from the negative polarity to the positive polarity, and the storage capacitor wire signal Csr is reversed from the positive polarity to the negative polarity.

[0060] As a result, as illustrated in (a) and (c) of Fig. 15, the electric potential of the pixel electrode 17jb is of a negative polarity and its effective potential is higher than the electric potential of the data signal written in, thereby causing the sub pixel including the pixel electrode 17jb to be a dark sub-pixel, whereas the electric potential of the pixel electrode 17JB is of a positive polarity and its effective potential is higher than the electric potential of the data signal written in, thereby causing the sub pixel including the pixel electrode 17JB to be a bright sub-pixel. Moreover, the electric potential of the pixel electrode 17ma is of a positive polarity and its effective potential is higher than the electric potential of the data signal written in, thereby causing the sub pixel including the pixel electrode 17ma to be a bright sub-pixel, whereas the electric potential of the pixel electrode 17mb is of a positive polarity and its effective potential is lower than the electric

potential of the data signal written in, thereby causing the sub pixel including the pixel electrode 17mb to be a dark sub-pixel. Moreover, the electric potential of the pixel electrode 17MA is of a negative polarity and its effective potential is higher than the electric potential of the data signal written in, thereby causing the sub pixel including the pixel electrode 17MA to be a dark sub-pixel, whereas the electric potential of the pixel electrode 17MB is of a negative polarity and its effective potential is lower than the electric potential of the data signal written in, thereby causing the sub pixel including the pixel electrode 17MB to be a bright sub-pixel. Moreover, the electric potential of the pixel electrode 17na is of a negative polarity, and its effective potential is lower than the electric potential of the data signal written in, thereby causing the sub pixel of the pixel electrode 17na to be a bright sub-pixel, whereas the electric potential of the pixel electrode 17NA is of a positive polarity and its effective potential is lower than the electric potential of the data signal written in, thereby causing the sub pixel including the pixel electrode 17NA be a dark sub-pixel. Moreover, data signals of the negative polarity are written into the pixel electrode 17nb, and data signals of a positive polarity are written into the pixel electrode 17NB.

[0061] The above allows for having a dot reversal polarity distribution of the data signals written into the pixels in F1, and further allows for displaying a light-and-dark checkered display (display in which bright sub-pixels and dark sub-pixels are alternately aligned in each of the row direction and the column direction).

[0062] On the other hand, the following drive method is performed in F2. First, in F1, the data signal lines 15x and 15X receive data signals of the negative polarity, and the data signal lines 15y and 15Y receive data signals of a positive polarity.

[0063] Simultaneously with a start of the kth horizontal scanning period (i.e., switchover of data signals corresponding to the kth horizontal scanning period), the pulse Pi of the gate pulse signal GPi and the pulse Pj of the gate pulse signal GPj rise, and simultaneously with the start of the (k+1)th horizontal scanning period (termination of the kth horizontal scanning period), the pulse Pi and the pulse Pj fall. Furthermore, simultaneously with the start of the (k+1)th horizontal scanning period (termination of the kth horizontal scanning period), the storage capacitor wire signal Csk is reversed from the positive polarity to the negative polarity, and the storage capacitor wire signal Csp is reversed from the negative polarity to the positive polarity.

[0064] Thereafter, simultaneously with the start of the (k+1)th horizontal scanning period, the pulse Pm of the gate pulse signal GPm and the pulse Pn of the gate pulse signal GPn rise, and simultaneously with the start of the (k+2)th horizontal scanning period, the pulse Pm and the pulse Pn fall. Furthermore, simultaneously with the start of the (k+2)th horizontal scanning period, the storage capacitor wire signal Csq is reversed from the positive polarity to the negative polarity, and the storage capacitor wire signal Csr is reversed from the negative polarity to the positive polarity.

[0065] With the present liquid crystal display apparatus, it is possible to display a halftone with use of the bright and dark sub-pixels, which allows for improving viewing angle characteristics. Moreover, the light-and-dark checkered display allows for preventing striped unevenness, which is caused by having the bright sub pixels or dark sub pixels be consecutively arranged.

[0066] Moreover, also with the present liquid crystal display apparatus, two scanning pulses rise at a timing in which two scanning pulses fall. Accordingly, an effect (fall of electric potential) received by the data signal line due to the fall of the two scanning pulses is canceled out by the effect (rise of electric potential) received by the data signal lines due to the rise of the two scanning pulses. This as a result allows for reducing the ripple (wavelike variation) in the electric potential of the data signal lines in the 1V reversal driving, which prevents the phenomenon that the size of the ripple increases as the supply source of the data signal becomes more distant (see Fig. 36), thereby improving the display quality.

[0067] In the driving method of Fig. 14, simultaneously with the start of the horizontal scanning period corresponding to the current stage the scanning pulse of the current stage rises, and simultaneously with the start of the horizontal scanning period corresponding to a subsequent stage (termination of the horizontal scanning period corresponding to the current stage) the scanning pulse of the current stage falls. However, the driving method is not limited to this example. For example, the scanning pulse of the current stage may be risen simultaneously with a start of a horizontal scanning period corresponding to a preceding stage, and the scanning pulse of the current stage may be fallen simultaneously with a start of the horizontal scanning period corresponding to a subsequent stage (termination of a horizontal scanning period corresponding to the current stage), as illustrated in Fig. 16. In this case, the scanning pulse has a width of 2H.

[0068] More specifically, the pulse Pi and the pulse Pj rise simultaneously with the start of the (k-1)th horizontal scanning period, the pulse Pm and the pulse Pn rise simultaneously with the start of the kth horizontal scanning period, the pulse Pi and the pulse Pj fall simultaneously with the start of the (k+1)th horizontal scanning period (termination of kth horizontal scanning period), and the pulse Pm and the pulse Pn fall simultaneously with the start of the (k+2)th horizontal scanning period.

[0069] The driving method of Fig. 16 allows for precharging in the first half (1H) of the pulse and allow for carrying out a main write in the second half (1H) of the pulse. Hence, it is possible to improve the pixel charging rate. In this case also, two scanning pulses rise at a timing in which two scanning pulses fall, which allows for preventing the phenomenon that the size of the ripple increases as the supply source of the data signal becomes more distant (see Fig. 36), thereby improving the display quality.

[0070] One specific example of the liquid crystal panel of Fig. 13 (portion including pixels 101, 102, 105, and 106) is illustrated as a plan view in Fig. 17 and as a cross sectional view in Fig. 18. In the active matrix substrate of the present liquid crystal panel, the scanning signal lines 16i and 16j which extend in a row direction and storage capacitor wires 18k, 18p, and 18q which extend in the row direction are provided on a transparent substrate 31. A gate insulating film 43 is provided so as to cover these members, and on the gate insulating film 43, a metal layer is formed, which metal layer includes: the data signal lines 15x, 15y, 15X, and 15Y each extending in a column direction; semiconductor layers (i layer and n+ layer) and source electrodes and drain electrodes for each of the transistors 12ia, 12ib, 12ja, 12jb, 12IA, 12IB, 12JA, and 12JB; drain draw-out electrodes 27; and capacitor electrodes 37. Moreover, an inorganic interlayer insulating film 25 is provided so as to cover the metal layer, and an organic interlayer insulating film 26 which is thicker than the inorganic interlayer insulating film 25 is formed on an upper layer of the inorganic interlayer insulating film 25. Furthermore, pixel electrodes 17ia, 17ib, 17ja, 12jb, 17IA, 17IB, 17JA, and 17JB are formed on the organic interlayer insulating film 26, and an alignment film 9 is formed so as to cover these pixel electrodes. The inorganic interlayer insulating film 25 and the organic interlayer insulating film 26 are hollowed through at a section in which contact holes 11 are opened; this allows for the pixel electrodes to be in contact with respective capacitor electrodes 37. Meanwhile, the color filter substrate 30 has a black matrix 13 and a colored layer (color filter layer) 14 formed on the glass substrate 32, and a common electrode (com) 28 is formed on an upper layer of these layers. Furthermore, an alignment film 19 is provided so as to cover the common electrode 28.

[0071] In the present liquid crystal panel, for instance, an edge of the pixel electrode 17ia on an upstream side in the scanning direction overlaps the storage capacitor wire 18k, whereas an edge of the pixel electrode 17ia on a downstream side in scanning direction overlaps an edge of the scanning signal line 16i on the upstream side in the scanning direction. From a plan view perspective, two edges of the pixel electrode 17ia which run along the column direction of the pixel electrode 17ia cover the data signal line 15x and data signal line 15y, respectively. Moreover, an edge of the pixel electrode 17ib on the upstream side in the scanning direction overlaps an edge of the scanning signal line 16i on the downstream side in the scanning direction, whereas an edge of the pixel electrode 17ib on the downstream side in the scanning direction overlaps the storage capacitor wire 18p. From a plan view perspective, the two edges of the pixel electrode 17ib which run along the column direction of the pixel electrode 17ib cover the data signal line 15x and data signal line 15y, respectively. Moreover, a storage capacitor is formed in a part on which the capacitor electrode overlaps the storage capacitor wire electrode in such a manner that a gate insulating film is sandwiched between the capacitor electrode and the storage capacitor wire.

Embodiment 3

[0072] Fig. 19 is an equivalent circuit diagram illustrating a portion of a liquid crystal panel according to Embodiment 3. As illustrated in Fig. 19, dispositions of the data signal lines, the scanning signal lines, the storage capacitor wires, the transistors, and the pixels in the present liquid crystal panel are all the same as those in Fig. 2.

[0073] Two pixel electrodes are provided per pixel: a pixel electrode 17ia of the pixel 101 is connected to the data signal line 15x via the transistor 12i that is connected to the scanning signal line 16i, and a pixel electrode 17ib of the pixel 101 is connected to the pixel electrode 17ia via a coupling capacitor; a pixel electrode 17ja of the pixel 102 is connected to the data signal line 15y via the transistor 12j that is connected to the scanning signal line 16j; a pixel electrode 17jb of the pixel 102 is connected to the pixel electrode 17ja via a coupling capacitor; a pixel electrode 17ma of the pixel 103 is connected to the data signal line 15x via the transistor 12m that is connected to the scanning signal line 16m, and a pixel electrode 17mb of the pixel 103 is connected to the pixel electrode 17ma via a coupling capacitor; a pixel electrode 17na of the pixel 104 is connected to the data signal line 15y via the transistor 12n that is connected to the scanning signal line 16n and a pixel electrode 17nb of the pixel 104 is connected to the pixel electrode 17na via a coupling capacitor; a pixel electrode 17IA of the pixel 105 is connected to the data signal line 15Y via the transistor 12I that is connected to the scanning signal line 16i, and a pixel electrode 17IB of the pixel 105 is connected to the pixel electrode 17IA via a coupling capacitor; and a pixel electrode 17JA of the pixel 106 is connected to the data signal line 15X via the transistor 12J that is connected to the scanning signal line 16j, and a pixel electrode 17JB of the pixel 106 is connected to the pixel electrode 17JA via a coupling capacitor.

[0074] Note that the scanning signal line 16i and the scanning signal line 16i are selected simultaneously, and the scanning signal line 16m and the scanning signal line 16n are selected simultaneously (later described).

[0075] Respective storage capacitors are formed between the storage capacitor wire 18p and each of the pixel electrodes 17ia, 17ib, 17IA, and 17IB, respective storage capacitors are formed between the storage capacitor wire 18q and each of the pixel electrodes 17ja, 17jb, 17JA, and 17JB, respective storage capacitors are formed between the storage capacitor wire 18r and each of the pixel electrodes 17ma, 17mb, 17MA, and 17MB, and respective storage capacitors are formed between the storage capacitor wire 18s and each of the pixel electrodes 17na, 17nb, 17NA, and 17NB. Moreover, although not illustrated, respective liquid crystal capacitors are formed between each of the pixel electrodes and the common electrode.

[0076] Fig. 20 is a timing chart illustrating a driving method of the present liquid crystal display apparatus including the liquid crystal panel (normally black mode) of Fig. 19. Sx, Sy, SX, and SY represent data signals (data signals) that are supplied to the data signal lines 15x, 15y, 15X, and 15Y, respectively, and GPi, GPj, GPm, and GPn represent gate pulse signal supplied to the scanning signal lines 16i, 16j, 16m, and 16n, respectively.

[0077] As illustrated in Fig. 20, the data signal lines and the scanning signal lines are driven as illustrated in Fig. 1. Just one of the two pixel electrodes capacitively coupled within the pixel is connected to a transistor and the other pixel is electrically floating. This makes an electric potential of one of the pixel electrodes (e.g., 17ia) be identical to that of the data signal, and makes an electric potential of other pixel electrode (e.g., 17ib) be identical to the electric potential of the data signal or that close to Vcom (electric potential of the common electrode). Therefore, the electric potentials of the pixel electrodes 17ia, 17ib, 17ja, 17jb, 17IA, 17IB, 17ma, 17mb, 17na, and 17nb become as shown as Via, Vib, Vja, Vjb, VIA, VIB, Vma, Vmb, Vna, and Vnb illustrated in Fig. 20, respectively, and the polarity distribution of each of the pixels and the disposition of the bright and dark sub pixels in each of the pixels in F1 of Fig. 20, are as illustrated in Fig. 21.

[0078] Since it is also possible to display a halftone with use of the bright and dark sub pixels in the present liquid crystal display apparatus, it is possible to improve the viewing angle characteristics.

[0079] Moreover, two scanning pulses rise at a timing in which two scanning pulses fall. Accordingly, the effect (fall of electric potential) received by the data signal lines due to the fall of the two scanning pulses is canceled out by the effect (rise of electric potential) received by the data signal lines due to the rise of the two scanning pulses. This as a result allows for reducing the ripple (wavelike variation) in the electric potential of the data signal lines in the 1V reversal driving, which prevents the phenomenon that the size of the ripple increases as the supply source of the data signal becomes more distant (see Fig. 36), thereby improving the display quality.

Embodiment 4

[0080] Fig. 22 is an equivalent circuit diagram illustrating a portion of a liquid crystal panel according to Embodiment 4. As illustrated in Fig. 22, the dispositions of the data signal lines, the scanning signal lines, the storage capacitor wires and the pixels in the present liquid crystal panel are identical to those in Fig. 2.

[0081] Two pixel electrodes are disposed per pixel: a pixel electrode 17ia of the pixel 101 is connected to the data signal line 15x via a transistor 12ia that is connected to the scanning signal line 16i, and a pixel electrode 17ib is connected to (i) the data signal line 15x via a transistor 12ib that is connected to the scanning signal line 16i and (ii) a capacitor electrode forming a capacitor with the storage capacitor wire 18q, via a transistor 112m that is connected to the scanning signal line 16m; a pixel electrode 17ja of the pixel 102 is connected to the data signal line 15y via a transistor 12ja that is connected to the scanning signal line 16j, and the pixel electrode 17jb is connected to (i) the data signal line 15y via a transistor 12jb that is connected to the scanning signal line 16j and (ii) a capacitor electrode forming a capacitor with the storage capacitor wire 18r, via a transistor 112n that is connected to the scanning signal line 16n; a pixel electrode 17ma of the pixel 103 is connected to the data signal line 15x via a transistor 12ma that is connected to the scanning signal line 16m, and the pixel electrode 17mb is connected to (i) the data signal line 15x via a transistor 12mb that is connected to the scanning signal line 16m and (ii) a capacitor electrode forming a capacitor with the storage capacitor wire 18s, via a transistor 112w that is connected to the scanning signal line 16w; the pixel electrode 17na of the pixel 104 is connected to the data signal line 15y via a transistor 12na that is connected to the scanning signal line 16n, and the pixel electrode 17nb is connected to (i) the data signal line 15y via a transistor 12nb that is connected to the scanning signal line 16n and (ii) a capacitor electrode forming a capacitor with a storage capacitor wire subsequent to (on a downstream side of the scanning direction) the storage capacitor wire 18s via a transistor that is connected to a scanning signal line of a subsequent stage of the scanning signal line 16w; a pixel electrode 17IA of the pixel 105 is connected to the data signal line 15Y via a transistor 12IA that is connected to the scanning signal line 16i, and a pixel electrode 17IB is connected to (i) the data signal line 15Y via a transistor 12IB that is connected to the scanning signal line 16i and (ii) a capacitor electrode forming a capacitor with the storage capacitor wire 18q, via a transistor 112M that is connected to the scanning signal line 16m; and a pixel electrode 17JA of the pixel 106 is connected to the data signal line 15X via a transistor 12JA that is connected to the scanning signal line 16j, and a pixel electrode 17JB is connected to (i) the data signal line 15X via a transistor 12JB that is connected to the scanning signal line 16j and (ii) a capacitor electrode forming a capacitor with the storage capacitor wire 18r, via a transistor 112N that is connected to the scanning signal line 16n.

[0082] Note that the scanning signal line 16i and the scanning signal line 16j are selected simultaneously, and the scanning signal line 16m and the scanning signal line 16n are selected simultaneously (later described).

[0083] Moreover, respective storage capacitors are formed between the storage capacitor wire 18p and each of the pixel electrodes 17ia, 17ib, 17IA, and 17IB, respective storage capacitors are formed between the storage capacitor wire 18q and each of the pixel electrodes 17ja, 17jb, 17JA, and 17JB, respective storage capacitors are formed between the storage capacitor wire 18r and each of the pixel electrodes 17ma, 17mb, 17MA, and 17MB, and respective storage

capacitors are formed between the storage capacitor wire 18s and each of the pixel electrodes 17na, 17nb, 17NA, and 17NB. Moreover, although not illustrated, respective liquid crystal capacitors are formed between each of the pixel electrodes and the common electrode.

[0084] Fig. 23 is a timing chart showing a driving method of the present liquid crystal display apparatus including the liquid crystal panel (normally black mode) of Fig. 22. Note that Sx, Sy, SX, and SY represent data signals (data signals) that are supplied to the data signal lines 15x, 15y, 15X, and 15Y, respectively, and GPi, GPj, GPm, and GPn represent gate pulse signals supplied to the scanning signal lines 16i, 16j, 16m, and 16n, respectively.

[0085] As illustrated in Fig. 23, although the data signal lines and scanning signal lines are driven as illustrated in Fig. 1, the two pixel electrodes disposed in a single pixel are connected to a same data signal line via different transistors, and just one of the two pixel electrodes is connected to a capacitor electrode via a transistor connected to a scanning signal line of a latter stage, which capacitor electrode forms a capacitor with the storage capacitor wire. Hence, an electric potential of the one of the two pixel electrodes becomes same as that of a data signal or that closer to Vcom (electric potential of the common electrode) after the scanning signal line of the latter stage becomes active, and the electric potential of the other pixel electrode becomes an electric potential identical to that of the data signal. Hence, the electric potentials of the pixel electrodes 17ia, 17ib, 17ja, 17jb, 17IA, 17IB, 17ma, 17mb, 17na, 17nb become as shown in Via, Vib, Vja, Vjb, VIA, VIB, Vma, Vmb, Vna, and Vnb of Fig. 23, respectively, and the polarity distribution of the pixels and the disposition of the bright and dark sub pixels of the pixels in F1 of Fig. 23 are as illustrated in Fig. 24.

[0086] Since the present liquid crystal display apparatus is capable of displaying a halftone with use of the bright and dark sub pixels, it is possible to improve the viewing angle characteristics. Furthermore, each of the two pixel electrodes disposed in the one pixel do not become electrically floating, so it is possible to prevent any image sticking and the like of the pixels.

[0087] Moreover, at a timing in which two scanning pulses fall, another two scanning pulses rise. Accordingly, the effect (fall of electric potential) received by the data signal lines due to the fall of the two scanning pulses is canceled out by the effect (rise of electric potential) received by the data signal lines due to the rise of the two scanning pulses. This as a result allows for reducing the ripple (wavelike variation) in the electric potential of the data signal lines in the 1V reversal driving, which prevents the phenomenon that the size of the ripple increases as the supply source of the data signal becomes more distant (see Fig. 36), thereby improving the display quality.

Implementation Example 1

[0088] Fig. 25 is an equivalent circuit diagram illustrating a portion of a liquid crystal panel according to an implementation example. As illustrated in Fig. 25, the dispositions of the data signal lines, the scanning signal lines, the storage capacitor wires and the pixels in the present liquid crystal panel are identical to those in Fig. 13.

[0089] Two pixel electrodes are provided per pixel: the pixel electrode 17ia of the pixel region 101 is connected to the data signal line 15x via the transistor 12ia that is connected to the scanning signal line 16i, and the pixel electrode 17ib of the pixel region 101 is connected to the data signal line 15y via the transistor 12ib that is connected to the scanning signal line 16i; the pixel electrode 17ja of the pixel region 102 is connected to the data signal line 15x via the transistor 12ja that is connected to the scanning signal line 16j, and the pixel electrode 17jb of the pixel region 102 is connected to the data signal line 15y via the transistor 12jb that is connected to the scanning signal line 16j; the pixel electrode 17ma of the pixel region 103 is connected to the data signal line 15x via the transistor 12ma that is connected to the scanning signal line 16m, and the pixel electrode 17mb of the pixel region 103 is connected to the data signal line 15y via the transistor 12mb that is connected to the scanning signal line 16m; the pixel electrode 17na of the pixel 104 is connected to the data signal line 15x via the transistor 12na that is connected to the scanning signal line 16n, and the pixel electrode 17nb of the pixel 104 is connected to the data signal line 15y via the transistor 12nb that is connected to the scanning signal line 16n; the pixel electrode 17IA of the pixel 105 is connected to the data signal line 15X via the transistor 12IA that is connected to the scanning signal line 16i, and the pixel electrode 17IB of the pixel 105 is connected to the data signal line 15Y via the transistor 12IB that is connected to the scanning signal line 16i; and the pixel electrode 17JA of the pixel 106 is connected to the data signal line 15X via the transistor 12JA of the scanning signal line 16j, and the pixel electrode 17JB of the pixel 106 is connected to the data signal line 15Y via the transistor 12JB that is connected to the scanning signal line 16j.

[0090] Moreover, respective storage capacitors are formed between the storage capacitor wire 18k and each of the pixel electrodes 17ia and 17IA, respective storage capacitors are formed between the storage capacitor wire 18p and each of the pixel electrodes 17ib, 17IB, 17ja, and 17JA, respective storage capacitors are formed between the storage capacitor wire 18q and each of the pixel electrodes 17jb, 17JB, 17ma, and 17MA, and respective storage capacitors are formed between the storage capacitor wire 18r and each of the pixel electrodes 17mb, 17MB, 17na, and 17NA. Moreover, although not illustrated, respective liquid crystal capacitors are formed between each of the pixel electrodes and the common electrode.

[0091] Fig. 26 is a timing chart showing a driving method of the present liquid crystal display apparatus including the

liquid crystal panel (normally black mode) of Fig. 25. Sx, Sy, SX, and SY represent data signals (data signals) that are supplied to the data signal lines 15x, 15y, 15X, and 15Y, respectively, and GPi, GPj, GPm, and GPn represent gate pulse signals that are supplied to the scanning signal lines 16i, 16j, 16m, and 16n, respectively.

[0092] As illustrated in Fig. 26, in the present drive method, one scanning signal line is selected and data signals whose polarities are reversed per vertical scanning period (1V) are supplied to the data signal lines. In a single vertical scanning period, data signals (signal potentials) respectively supplied to two data signal lines which are associated to a single pixel column are made to have identical polarities, and data signals that are respectively supplied to two adjacent data signal lines which each are associated with different pixel columns are made to have different polarities. Furthermore, in a single horizontal scanning period, an absolute value (Vcom serving as a standard) of data signals supplied to one of the two data signal lines associated with the single pixel column is made not more than an absolute value of the data signals supplied to the other data signal line.

[0093] At a timing in which a scanning pulse falls, another scanning pulse rises; simultaneously with a start of a horizontal scanning period corresponding to the current stage, a scanning pulse of the current stage rises, and simultaneously with a start of a horizontal scanning period corresponding to a subsequent stage (termination of the horizontal scanning period corresponding to the current stage), the scanning pulse of the current stage falls.

[0094] More specifically, F1 of consecutive frames F1 and F2 is driven by the following driving method. First, in F1, the data signal lines 15x and 15y receive data signals of a positive polarity, and the data signal lines 15X and 15Y receive data signals of a negative polarity.

[0095] Simultaneously with a start of the kth horizontal scanning period (i.e. switchover to a data signal corresponding to the kth horizontal scanning period), the gate pulse signal GPi rises, and simultaneously with a start of the (k+1)th horizontal scanning period (termination of the kth horizontal scanning period), the pulse Pi rises.

[0096] Hence, as illustrated in Figs. 26 and 27, data signals of a positive polarity are written into the pixel electrode 17ia of the pixel 101, and data signals of a positive polarity having an absolute value smaller than that of the data signal written into the pixel electrode 17ia are written into the pixel electrode 17ib. Moreover, data signals of a negative polarity is written into the pixel electrode 17IB of the pixel 105, and data signals of a negative polarity having an absolute value smaller than that of the data signal written into the pixel electrode 17IB are written into the pixel electrode 17IA.

[0097] Moreover, simultaneously with a start of the (k+1)th horizontal scanning period, the pulse Pj of the gate pulse signal GPj rises, and simultaneously with a start of the (k+2)th horizontal scanning period, the pulse Pj falls.

[0098] Hence, as illustrated in Figs. 26 and 27, data signals of a positive polarity are written into the pixel electrode 17ja of the pixel 102, and data signals of a positive polarity having an absolute value smaller than that of the data signal written into the pixel electrode 17ja are written into the pixel electrode 17jb. Moreover, data signals of a negative polarity are written into the pixel electrode 17JB of the pixel 106, and data signals of a negative polarity having an absolute value smaller than that of the data signal written into the pixel electrode 17JB are written into the pixel electrode 17JA.

[0099] Simultaneously with the start of the (k+2)th horizontal scanning period, the pulse Pm of the gate pulse signal GPm rises, and simultaneously with the start of the (k+3)th horizontal scanning period, the pulse Pm falls.

[0100] As a result, as illustrated in Figs. 26 and 27, data signals of a positive polarity are written into the pixel electrode 17ma of the pixel 103, and data signals of a positive polarity having an absolute value smaller than that of the data signals written into the pixel electrode 17ma are written into the pixel electrode 17mb. Moreover, data signals of a negative polarity are written into the pixel electrode 17MB of the pixel 107, and data signals of a negative polarity having an absolute value smaller than that of the data signals written into the pixel electrode 17MB are written into the pixel electrode 17MA.

[0101] Moreover, simultaneously with the (k+3)th horizontal scanning period, the pulse Pn of the gate pulse signal GPn rises, and simultaneously with the start of a (k+4)th horizontal scanning period, the pulse Pn rises.

[0102] As a result, as illustrated in Figs. 26 and 27, data signals of a positive polarity are written into the pixel electrode 17na of the pixel 104, and data signals of a positive polarity having an absolute value smaller than that of the data signals written into the pixel electrode 17na are written into the pixel electrode 17nb. Moreover, data signals of a negative polarity are written into the pixel electrode 17NB of the pixel 108, and data signals of a negative polarity having an absolute value smaller than that of the data signals written into the pixel electrode 17NB are written into the pixel electrode 17NA.

[0103] Since the present liquid crystal display apparatus is capable of displaying a halftone with use of the bright and dark sub pixels, it is possible to improve the viewing angle characteristics. Moreover, the light-and-dark checkered display allows for preventing striped unevenness, which is caused by having the bright sub pixels or dark sub pixels be consecutively arranged.

[0104] Moreover, also with the present liquid crystal display apparatus, at the timing in which one scanning pulse falls, another scanning pulse rises. Accordingly, an effect (fall of electric potential) received by the data signal line due to the fall of the scanning pulse is canceled out by an effect (rise of electric potential) received by the data signal line caused by the rise of a scanning pulse. This as a result allows for reducing the ripple (wavelike variation) in the electric potential of the data signal lines in the 1V reversal driving, which prevents the phenomenon that the size of the ripple increases as the supply source of the data signal becomes more distant (see Fig. 36), thereby improving the display quality.

Implementation Example 2

[0105] Fig. 28 is an equivalent circuit diagram illustrating a portion of a liquid crystal panel according to another implementation example. As illustrated in Fig. 28, in the present liquid crystal panel, data signal lines 15z, 15x, and 15X are arranged in this order, and scanning signal lines 16i, 16j, 16m, 16n, and 16w, each of which extend in a row direction (left-right direction in Fig. 28), are arranged in this order. A pixel 101 is provided associated with an intersection where the data signal line 15x intersects with the scanning signal line 16i, a pixel 102 is provided associated with an intersection where the data signal line 15x intersects with the scanning signal line 16j, a pixel 103 is provided associated with an intersection where the data signal line 15x intersects with the scanning signal line 16m, a pixel 104 is provided associated with an intersection where the data signal line 15x intersects with the scanning signal line 16n, the pixel 105 is provided associated with an intersection where the data signal line 15X intersects with the scanning signal line 16i, a pixel 106 is provided associated with an intersection where the data signal line 15X intersects with the scanning signal line 16j, the pixel 107 is provided associated with an intersection where the data signal line 15X intersects with the scanning signal line 16m, and a pixel 108 is provided associated with an intersection where the data signal line 15X intersects with the scanning signal line 16n. A storage capacitor wire 18p is provided associated with the pixels 101 and 105, a storage capacitor wire 18q is provided associated with the pixels 102 and 106, a storage capacitor wire 18r is provided associated with the pixels 103 and 107, and a storage capacitor wire 18s is provided associated with the pixels 104 and 108.

[0106] On either sides of a pixel column α that includes the pixels 101 to 104 are disposed (i) a pixel column γ and (ii) a pixel column β that includes the pixels 105 to 108. The data signal line 15x is disposed associated with the pixel column α, and the data signal line 15X is disposed associated with the pixel column β.

[0107] Furthermore, one pixel electrode is disposed per pixel: a pixel electrode 17i of the pixel 101 is connected to the data signal line 15x via a transistor 12i that is connected to the scanning signal line 16i; a pixel electrode 17j of the pixel 102 is connected to the data signal line 15x via a transistor 12j that is connected to the scanning signal line 16j; a pixel electrode 17m of the pixel 103 is connected to the data signal line 15x via a transistor 12m that is connected to the scanning signal line 16m; a pixel electrode 17n of the pixel 104 is connected to the data signal line 15x via a transistor 12n that is connected to the scanning signal line 16n; a pixel electrode 17I of the pixel 105 is connected to the data signal line 15X via a transistor 12I that is connected to the scanning signal line 16i; a pixel electrode 17J of the pixel 106 is connected to the data signal line 15X via a transistor 12J that is connected to the scanning signal line 16j; a pixel electrode 17M of the pixel 107 is connected to the data signal line 15X via a transistor 12M that is connected to the scanning signal line 16m; and a pixel electrode 17N of the pixel 108 is connected to the data signal line 15X via a transistor 12N that is connected to the scanning signal line 16n.

[0108] Moreover, respective storage capacitors are formed between the storage capacitor wire 18p and each of the pixel electrodes 17i and 17I, respective storage capacitors are formed between the storage capacitor wire 18q and each of the pixel electrodes 17j and 17J, respective storage capacitors are formed between the storage capacitor wire 18r and each of the pixel electrodes 17m and 17M, and respective storage capacitors are formed between the storage capacitor wire 18s and each of the pixel electrodes 17n and 17N. Furthermore, respective liquid crystal capacitors are formed between each of the pixel electrodes and the common electrode com.

[0109] Fig. 29 is a timing chart illustrating a driving method of the present liquid crystal display apparatus including the liquid crystal panel (normally black mode) illustrated in Fig. 28. Sz, Sx, and SX represent data signals (data signals) that are supplied to the data signal lines 15z, 15x, and 15X, respectively, and GPi, GPj, GPm, and GPn represent gate pulse signals that are supplied to the scanning signal lines 16i, 16j, 16m, and 16n, respectively.

[0110] As illustrated in Fig. 29, in the present drive method, one scanning signal line is selected simultaneously and data signals whose polarities are reversed per vertical scanning period (1V) are supplied to the data signal lines. In a single vertical scanning period, data signals respectively supplied to two adjacent data signal lines disposed associated with different pixel columns are made to have different polarities. At a timing in which one scanning pulse falls, one scanning pulse rises; simultaneously with a start of the horizontal scanning period corresponding to a current stage, a scanning pulse of the current stage rises, and simultaneously with a start of the horizontal scanning period corresponding to a subsequent stage (termination of the horizontal scanning period corresponding to the current stage), the scanning pulse of the current stage falls.

[0111] For example, in F1, the data signal lines 15z and 15X receive data signals of a negative polarity, and the data signal line 15x receives data signals of a positive polarity.

[0112] Simultaneously with the start of the kth horizontal scanning period (i.e. switchover to a data signal corresponding to the kth horizontal scanning period), the pulse Pi of the gate pulse signal GPi rises, and simultaneously with the start of the (k+1)th horizontal scanning period (termination of the kth horizontal scanning period), the pulse Pi falls. Moreover, simultaneously with the start of the (k+1)th horizontal scanning period, the pulse Pj of the gate pulse signal GPj rises, and simultaneously with the start of the (k+2)th horizontal scanning period, the pulse Pj falls. Moreover, simultaneously with the start of the (k+2)th horizontal scanning period, the pulse Pm of the gate pulse signal GPm rises, and simulta-

neously with the (k+3)th horizontal scanning period, the pulse Pm falls. Moreover, simultaneously with the start of the (k+3)th horizontal scanning period, the pulse Pn of the gate pulse signal GPn rises, and simultaneously with the start of the (k+4)th horizontal scanning period, the pulse Pn falls.

[0113] In the present liquid crystal display apparatus, at a timing in which one scanning pulse falls, another one scanning pulse rises. Hence, an effect (fall of electric potential) received by the data signal line due to the fall of the one scanning pulse is canceled out by the effect (rise of electric potential) received by the data signal line due to the rise of another one scanning pulse. As a result, the ripple (wavelike variation) generated in the electric potential of the data signal line can be reduced even in the 1V reversal driving. This allows for preventing the phenomenon that the size of the ripple increases as the supply source of the data signal becomes more distant (see Fig. 36), thereby improving the display quality.

[0114] In the drive method of Fig. 29, the scanning pulse of the current stage rises simultaneously with the start of the horizontal scanning period corresponding to the current stage, and the scanning pulse of the current stage falls simultaneously with a start of the horizontal scanning period of a subsequent stage (termination of the horizontal scanning period corresponding to the current stage). However, the driving method is not limited to this example. For instance, the method may be as illustrated in Fig. 30, in which the scanning pulse of the current stage rises simultaneously with a start of a horizontal scanning period corresponding to a preceding stage, and the scanning pulse of the current stage falls simultaneously with a start of the horizontal scanning period corresponding to a subsequent stage (termination of the horizontal scanning period corresponding to the current stage). In this case, the scanning pulse has a width of 2H.

[0115] More specifically, the pulse Pi rises simultaneously with the start of the (k-1)th horizontal scanning period, the pulse Pj rises simultaneously with the start of the kth horizontal scanning period, and simultaneously with the start of the (k+1)th horizontal scanning period (termination of the kth horizontal scanning period), the pulse Pi falls while the pulse Pm rises. Moreover, simultaneously with the start of the (k+2)th horizontal scanning period, the pulse Pj falls while the pulse Pn rises.

[0116] The drive method of Fig. 30 allows for precharging during a first half (1H) of the pulse and for carrying out a main charge during a second half (1H) of the pulse. This allows for improving the pixel charging rate. Of course in this case also, one scanning pulse rises at a timing in which one scanning pulse falls. This allows for preventing the phenomenon that the size of the ripple increases as the supply source of the data signal becomes more distant (see Fig. 36), thereby improving the display quality.

[0117] In each of the embodiments, 1V reversal driving is used as one type of the LT reversal driving, however the reversal driving is not limited to the LT reversal driving. Alternatively, nV reversal driving may be used (for example, polarities of data signals that are supplied to the data signal lines may be reversed per two frames) or nH reversal driving may be used (for example, polarities of data signals that are supplied to the data signal lines may be reversed per 12H).

[0118] The waveform shown in Fig. 1 and the like of the signal potential that is supplied to the data signal lines is of a case where leading-in of pixel potential at a time when a transistor is turned OFF can be ignored (a case where a center value of the signal potential = Vcom) (for easy description). In a case where the leading-in of the pixel potential cannot be ignored, the center value of the signal potential is to be higher than Vcom, and further in a case where a leading-in amount varies based on gray scales (data signals), the center value is to be varied in accordance with the gray scales (data signals).

[0119] Fig. 31 is a block diagram illustrating a configuration of the present liquid crystal display apparatus. As illustrated in Fig. 31, the present liquid crystal display apparatus includes a display section (liquid crystal panel), a source driver (SD), a gate driver (GD), and a display control circuit. The source driver drives data signal lines, the gate driver drives scanning signal lines, and the display control circuit controls the source driver and the gate driver. A storage capacitor wire driving circuit for driving storage capacitor wires (Cs wires) may also be provided if necessary.

[0120] The display control circuit receives, from an external signal source (e.g., a tuner), a digital video signal Dv representing an image to be displayed, a horizontal sync signal HSY and vertical sync signal VSY corresponding to the digital video signal Dv, and a control signal Dc for controlling a display operation. Moreover, based on these received signals Dv, HSY, VSY, and Dc, the display control circuit generates, as signals for displaying on the display section the image represented by the digital video signal Dv, a data start pulse signal SSP, a data clock signal SCK, a digital image signal DA (signal corresponding to the digital video signal Dv) representing the image to be displayed, a gate start pulse signal GSP, a gate clock signal GCK, and a gate driver output control signal (scanning signal output control signal) GOE. The display control circuit then outputs these signals.

[0121] More specifically, the display control circuit (i) outputs the video signal Dv as the digital image signal DA, after carrying out timing adjustment and the like of the video signal Dv by use of an inner memory as necessary, (ii) generates the data clock signal SCK as a signal made up of a pulse corresponding to pixels in the image that the digital image signal DA represents, (iii) generates the data start pulse signal SSP as a signal that, based on the horizontal sync signal HSY, becomes a high-level (H level) for just a predetermined time per horizontal scanning period, (iv) generates a gate start pulse signal GSP as a signal that, based on the vertical sync signal VSY, becomes a H level for just a predetermined time per frame period (one vertical scanning period), (v) generates a gate clock signal GCK based on the horizontal

sync signal HSY, and (vi) generates a gate driver output control signal GOE based on the horizontal sync signal HSY and control signal Dc.

[0122] Among the signals that are generated in the display control circuit as the aforementioned, the digital image signal DA, a polarity inversion signal POL that controls a polarity of the data signal (data data signal), the data start pulse signal SSP, and the data clock signal SCK are inputted into the source driver; whereas the gate start pulse signal GSP, gate clock signal GCK, and gate driver output control signal GOE are inputted into the gate driver.

[0123] The source driver successively generates, per one horizontal scanning period, an analog potential (data signal) that is equivalent to a pixel value in the scanning signal lines of the image represented by the digital image signal DA, based on the digital image signal DA, the data clock signal SCK, the data start pulse signal SSP, and the polarity inversion signal POL. The source driver then outputs these data signals to the data signal lines.

[0124] The gate driver generates a gate on-pulse signal based on the gate start pulse signal GSP, the gate clock signal GCK, and the gate driver output control signal GOE, and outputs this generated signal to the scanning signal line. This causes the scanning signal lines to be selectively driven.

[0125] By driving the data signal lines and scanning signal lines of the display section (liquid crystal panel) by the source driver and gate driver as described above, a data signal is written into a pixel electrode from the data signal lines via a transistor (TFT) connected to the selected scanning signal line. As a result, a voltage is applied to a liquid crystal layer of the sub pixels, which controls the amount of light transmitted from the backlight. Accordingly, the image represented by the digital video signal Dv is displayed on the sub pixels.

[0126] The following description explains one configuration example of the present liquid crystal display device in a case where the liquid crystal display device is applied to a television receiver. Fig. 32 is a block diagram illustrating a configuration of a liquid crystal display apparatus 800 for use in a television receiver. The liquid crystal display apparatus 800 includes: a liquid crystal display unit 84; a Y/C separation circuit 80, a video chroma circuit 81; an A/D converter 82; a liquid crystal controller 83; a backlight driving circuit 85; a backlight 86; a microcomputer (microcomputer) 87; and a gradation circuit 88. The liquid crystal display unit 84 includes a liquid crystal panel, and a source driver and gate driver for driving the liquid crystal panel.

[0127] In the liquid crystal display apparatus 800 of this configuration, first, a composite color video signal Scv as a television signal is inputted into the Y/C separation circuit 80 from outside, and the composite color video signal Scv is divided into a brightness signal and a color signal. The brightness signal and color signal are converted by the video chroma circuit 81 into analog RGB signals that correspond to the light's three principle colors, and further the analog RGB signals are converted by the A/D converter 82 into digital RGB signals. The digital RGB signals are inputted into the liquid crystal controller 83. Moreover, in the Y/C separation circuit 80, horizontal and vertical sync signals are also retrieved from the composite color video signal Scv inputted from the outside. These sync signals also are inputted into the liquid crystal controller 83 via the microcomputer 87.

[0128] In the liquid crystal display unit 84, the digital RGB signals are inputted from the liquid crystal controller 83 at a predetermined timing, together with a timing signal based on the sync signal. Moreover, in the gradation circuit 88, gradation electric potentials are generated for each of the three principle colors of color display R, G, B. These gradation electric potentials are also supplied to the liquid crystal display unit 84. In the liquid crystal display unit 84, a driving signal (data signal = signal electric potential, scanning signal etc.) is generated by the source driver, gate driver and the like provided inside, based on the RGB signals, the timing signal, and the gradation electric potentials, and a color image is displayed on the inner liquid crystal panel based on the driving signal. In order to display an image by the liquid crystal display unit 84, it is necessary to irradiate light from a rear side of liquid crystal panel inside of the liquid crystal display unit. With the liquid crystal display apparatus 800, light is irradiated on a rear side of the liquid crystal panel by having the backlight driving circuit 85 drive the backlight 86 under control of the microcomputer 87. Control of the entire system including the foregoing processes is carried out by the microcomputer 87. Video signals inputted from the outside (composite color video signal) may be not just video signals based on television broadcast, but may also be video signals captured by a camera and video signals supplied via Internet connection. With use of the liquid crystal display apparatus 800, it is possible to perform image display based on various video signals.

[0129] In a case where an image based on television broadcast is displayed by the liquid crystal display apparatus 800, a tuner section 90 is connected to the liquid crystal display device 800 as illustrated in Fig. 33, thus configuring the present television receiver 701. The tuner section 90 extracts signals of channels to be received among waves (high frequency signals) that are received by an antenna (not illustrated), and converts the extracted signals to intermediate frequency signals. By detecting this intermediate frequency signal, composite color video signals Scv as a television signal are taken out. The composite color video signal Scv is, as already described, inputted into the liquid crystal display apparatus 800, and an image based on this composite color video signal Scv is displayed on the liquid crystal display apparatus 800.

[0130] Fig. 34 is an exploded perspective view of an example illustrating one configuration of the present television receiver. As illustrated in Fig. 34, the present television receiver 701 includes, as its constituents, the liquid crystal display apparatus 800, a first housing 801, and a second housing 806. The first housing 801 and the second housing 806

sandwiches the liquid crystal display apparatus 800 so that the liquid crystal display apparatus 800 is surrounded by the two housings. The first housing 801 has an opening 801a that transmits an image displayed on the liquid crystal display apparatus 800. Moreover, the second housing 806 covers a rear side of the liquid crystal display apparatus 800, and includes an operation circuit 805 for operating the display apparatus 800. Further, the second housing 806 has a supporting member 808 disposed on its lower side.

[0131] A display apparatus of the present invention is a display apparatus including: scanning signal lines; and data signal lines, wherein: each of the data signal lines receives data signals whose polarities are reversed per one vertical scanning period, per plurality of vertical scanning periods, or per plurality of horizontal scanning periods, in one horizontal scanning period, one of two data signal lines receives a data signal having a polarity and the other of the two data signal lines receives another data signal having another polarity, the two data signal lines being arranged adjacent to each other, the scanning signal lines are made sequentially active in sets of N line(s) (N is an integer of not less than 1), and at a timing in which a set of N line(s) of the scanning signal line(s) is deactivated from an active state, another set of N line(s) of the scanning signal line(s) is activated from an inactive state.

[0132] According to the configuration, at a timing at which a set of N line(s) of the scanning signal line(s) is deactivated, another set of N line(s) of the scanning signal line(s) is activated; hence, an effect (e.g., fall of electric potential) received by the data signal lines due to the deactivation of the set of N line(s) of the scanning signal line(s) (e.g., fall of N scanning pulses) is basically canceled by the effect (e.g., rise of electric potential) received by the data signal lines due to activating the set of N line(s) of scanning signal line(s) (e.g., rise of N scanning pulses). This allows for reducing a ripple (wavelike variation) generating in the electric potential of the data signal lines also in LT reversal driving, which allows for preventing a phenomenon that the size of the ripple increases as the supply source of the data signal becomes more distant (see Fig. 36), thereby improving display quality.

[0133] With the present display apparatus, a scanning signal line is activated by a rise of a scanning pulse supplied to the scanning signal line and thereafter is deactivated by a fall of the scanning pulse, or is activated by a fall of a scanning pulse supplied to the scanning signal line and thereafter is deactivated by a rise of the scanning pulse.

[0134] The present display apparatus may be configured in such a manner that the N is not less than 2 (two scanning signal lines are selected simultaneously).

[0135] The present display apparatus may be configured in such a manner that a scanning pulse of a current stage is activated simultaneously with a start of a horizontal scanning period corresponding to the current stage, and the scanning pulse of the current stage is deactivated simultaneously with termination of the horizontal scanning period corresponding to the current stage.

[0136] The present display apparatus may be configured in such a manner that a scanning pulse of a current stage is activated simultaneously with a start of a horizontal scanning period corresponding to a preceding stage, and the scanning pulse of the current stage is deactivated simultaneously with termination of the horizontal scanning period corresponding to the current stage.

[0137] The present display apparatus may be configured further including a spare wire for use in repairing a disconnection of the data signal lines, a repaired data signal line of the data signal lines receiving the data signals from one of its ends as well as receiving the data signals from the other one of its ends via the spare wire.

[0138] The present display apparatus may be configured in such a manner that the N is 2 and two of the scanning signal lines are selected simultaneously, two of the data signal lines are associated with a first pixel column and another two of the data signal lines are associated with a second pixel column adjacent to the first pixel column, each of pixels include at least one pixel electrode, and a pixel electrode in the first pixel column is connected, via a transistor, to any one of the two data signal lines associated with the first pixel column, and a pixel electrode in the second pixel column is connected, via another transistor, to any one of the two data signal lines associated with the second pixel column.

[0139] The present display apparatus may be configured in such a manner that the pixel electrode included in the first pixel column is disposed so that the pixel electrode included in the first pixel column overlaps the two data signal lines associated with the first pixel column, and the pixel electrode included in the second pixel column is disposed so that the pixel electrode included in the second pixel column overlaps the two data signal lines associated with the second pixel column.

[0140] The present display apparatus may be configured in such a manner that in each of the first pixel column and the second pixel column, a pixel electrode of one of two consecutive pixels is connected, via a transistor, to a data signal line different from that connected to the pixel electrode of the other one of the two consecutive pixels via another transistor, and the transistor to which the pixel electrode included in the one of the two consecutive pixels is connected, is connected to one of the two scanning signal lines selected simultaneously, and the transistor to which the pixel electrode included in the other one of the two consecutive pixels is connected, is connected to the other one of the two scanning signal lines selected simultaneously.

[0141] The present display apparatus may be configured in such a manner that in a same horizontal scanning period, the two data signal lines associated with a same pixel column are supplied with data signals of different polarities.

[0142] The present display apparatus may be configured in such a manner that in a same horizontal scanning period,

two adjacent data signal lines being associated with different pixel columns are supplied with data signals of different polarities.

[0143] The present display apparatus may be configured in such a manner that in a same horizontal scanning period, two adjacent data signal lines being associated with different pixel columns are supplied with data signals of identical polarities.

[0144] The present display apparatus may be configured in such a manner thata pixel includes a plurality of pixel electrodes.

[0145] The present display apparatus may be configured further including a plurality of storage capacitor wires, two pixel electrodes provided in a pixel being connected to a same data signal line via different transistors that are connected to a same scanning signal line, one of the two pixel electrodes forming a capacitor with a corresponding one of the storage capacitor wires, and the other one of the two pixel electrodes forming a capacitor with another one of the storage capacitor wires.

[0146] The present display apparatus may be configured in such a manner that two pixel electrodes provided in a pixel are connected to each other via a capacitor, and just one of the two pixel electrodes is connected to a corresponding one of the data signal lines via a transistor that is connected to a corresponding one of the scanning signal lines.

[0147] The present display apparatus may be configured further including a plurality of storage capacitor wires, two pixel electrodes provided in a pixel being connected to a same data signal line via different transistors that are connected to a same scanning signal line, one of the two pixel electrodes being connected to a capacitor electrode via a transistor that is connected to another one of the scanning signal lines, the capacitor electrode forming a capacitor with the storage capacitor wire.

[0148] The present display apparatus may be configured in such a manner that two data signal lines are associated with one pixel, one of two pixel electrodes provided in the pixel is connected to one of the two data signal lines via one of two transistors that are connected to a same scanning signal line, and the other one of the two pixel electrodes is connected to the other one of the two data signal lines that is connected to the other one of the two transistors.

[0149] The present display apparatus may be configured in such a manner that the plurality of scanning signal lines and the plurality of data signal lines are formed on a substrate, the substrate further having a comb-shaped pixel electrode and a common electrode being formed thereon.

[0150] A method of driving the present display apparatus is a method of driving a display apparatus including scanning signal lines and data signal lines, the method including: outputting, to each of the data signal lines, data signals whose polarities are reversed per one vertical scanning period, per plurality of vertical scanning periods, or per plurality of horizontal scanning periods, while in one horizontal scanning period, outputting a data signal having a polarity to one of two data signal lines and outputting another data signal having another polarity to the other of the two data signal lines, the two data signal lines being arranged adjacent to each other; activating the scanning signal lines sequentially in sets of N line(s) (N is an integer of not less than 1); and activating, at a timing in which a set of N line(s) of the scanning signal line(s) is deactivated from an active state, another set of N line(s) of the scanning signal line(s) from an inactive state.

[0151] A present liquid crystal display apparatus includes the display apparatus. Moreover, a present television receiver includes: the liquid crystal display apparatus; and a tuner section configured to receive television broadcast.

Industrial Applicability

[0152] The display apparatus of the present invention is suitably used for a liquid crystal television, for example.

Reference Signs List

[0153]

101 to 108	pixel
12i, 12j, 12m, 12n	transistor
15x, 15y, 15X, 15Y	data signal line
16i, 16j, 16m, 16n	scanning signal line
17i, 17j, 17m, 17n	pixel electrode
18p, 18r, 18s	storage capacitor wire
α, β	pixel column
Pi, Pj, Pm, Pn	pulse (scanning pulse)

Claims

1. A display apparatus comprising:

scanning signal lines (16i, 16j; 16m, 16n; ...); and
data signal lines (15x, 15y; 15X, 15Y; ...), wherein:

each of the data signal lines (15x, 15y; 15X, 15Y; ...) is configured to receive data signals (Sx, Sy, SX, SY, ...) the polarities of which are reversed per one vertical scanning period, per plurality of vertical scanning periods, or per plurality of horizontal scanning periods,
in one horizontal scanning period, one of two data signal lines (15x, 15y; 15X, 15Y; ...); is configured to receive a data signal (Sx, SX) having a first polarity and the other of the two data signal lines (15x, 15y; 15X, 15Y; ...) is configured to receive another data signal (Sy, SY) having a second polarity other than the first polarity, the two data signal lines (15x, 15y; 15X, 15Y; ...) being arranged adjacent to each other,
characterized in that
the scanning signal lines (16i, 16j; 16m, 16n; ...) are made sequentially active in sets of adjacent N lines by applying gate signals to the respective scanning signals lines (16i, 16j; 16m, 16n; ...), where $N \geq 2$,
when adjacent N lines of a first set receive respective gate signals (GPi, GPj) to deactivate the scanning signal lines of the first set from an active state, another adjacent N lines of another second set (16m, 16n) receive respective gate signals (GPm, GPn) to activate the scanning signal lines of said second set (16m, 16n) from an inactive state; and
wherein the sets of adjacent N lines of the signal lines (16i, 16j; 16m, 16n; ...) are identical in consecutive frames (F1, F2).

2. The display apparatus according to claim 1, wherein a scanning signal line (16i, 16j; 16m, 16n; ...) is activated by a rise of a scanning pulse (GPi, GPj; GPm, GPn; ...) supplied to the scanning signal line (16i, 16j; 16m, 16n; ...) and thereafter is deactivated by a fall of the scanning pulse (GPi, GPj; GPm, GPn; ...), or is activated by a fall of a scanning pulse (GPi, GPj; GPm, GPn; ...) supplied to the scanning signal line (16i, 16j; 16m, 16n; ...) and thereafter is deactivated by a rise of the scanning pulse (GPi, GPj; GPm, GPn; ...).

3. The display apparatus according to claim 2, wherein a scanning pulse (GPi, GPj; GPm, GPn; ...) of a current stage is activated simultaneously with a start of a horizontal scanning period corresponding to the current stage, and the scanning pulse (GPi, GPj; GPm, GPn; ...) of the current stage is deactivated simultaneously with termination of the horizontal scanning period corresponding to the current stage.

4. The display apparatus according to claim 2, wherein a scanning pulse (GPi, GPj; GPm, GPn; ...) of a current stage is activated simultaneously with a start of a horizontal scanning period corresponding to a preceding stage, and the scanning pulse (GPi, GPj; GPm, GPn; ...) of the current stage is deactivated simultaneously with termination of the horizontal scanning period corresponding to the current stage.

5. The display apparatus according to any one of claims 1 to 4, further comprising:

a spare wire (PW) for use in repairing a disconnection of the data signal lines (15X, 15y; 15X, 15Y; ...),
a repaired data signal line of the data signal lines (15x, 15y; 15X, 15Y; ...) receiving the data signals (Sx, Sy, SX, SY) from one of its ends as well as receiving the data signals (Sx, Sy, SX, SY) from the other one of its ends via the spare wire.

6. The display apparatus according to any one of claims 1 to 5, wherein:

the N = 2 and two scanning signal lines (16i, 16j; 16m, 16n; ...) is selected simultaneously,
two of the data signal lines (15x, 15y; 15X, 15Y; ...) are associated with a first pixel column (α) and another two of the data signal lines (15x, 15y; 15X, 15Y; ...) are associated with a second pixel column (β) adjacent to the first pixel column,
each of pixels (101, 102, ..., 108) include at least one pixel electrode (17i, 17j, 17m, 17n; 17I, 17J, 17M, 17N), and a pixel electrode (17i, 17j, 17m, 17n) in the first pixel column (α) is connected, via a transistor (12i, 12j, 12m, 12n), to any one of the two data signal lines (15x, 15y; 15X, 15Y; ...) associated with the first pixel column (α), and a pixel electrode (17I, 17J, 17M, 17N) in the second pixel column (β) is connected, via another transistor (12I, 12J, 12M, 12N), to any one of the two data signal lines (15x, 15y; 15X, 15Y; ...) associated with the second

pixel column (β).

7. The display apparatus according to claim 6, wherein the pixel electrode (17i, 17j, 17m, 17n) included in the first pixel column (α) is disposed so that the pixel electrode (17i, 17j, 17m, 17n) included in the first pixel column (α) overlaps the two data signal lines (15x, 15y; 15X, 15Y; ...) associated with the first pixel column (α), and the pixel electrode (17I, 17J, 17M, 17N) included in the second pixel column (β) is disposed so that the pixel electrode (17I, 17J, 17M, 17N) included in the second pixel column (β) overlaps the two data signal lines (15x, 15y; 15X, 15Y; ...) associated with the second pixel column (β).

8. The display apparatus according to claim 6, wherein in each of the first pixel column (α) and the second pixel column (β), a pixel electrode (17i, 17j, 17m, 17n; 17I, 17J, 17M, 17N) of one of two consecutive pixels (101, 102, ..., 108) is connected, via a transistor (12i, 12j, 12m, 12n,), to a data signal line different from that connected to the pixel electrode (17i, 17j, 17m, 17n; 17I, 17J, 17M, 17N) of the other one of the two consecutive pixels (101, 102, ..., 108) via another transistor (12I, 12J, 12M, 12N), and
the transistor to which the pixel electrode (17i, 17j, 17m, 17n; 17I, 17J, 17M, 17N) included in the one of the two consecutive pixels (101, 102, ..., 108) is connected, is connected to one of the two scanning signal lines (16i, 16j; 16m, 16n; ...) selected simultaneously, and the transistor to which the pixel electrode (17i, 17j, 17m, 17n; 17I, 17J, 17M, 17N) included in the other one of the two consecutive pixels (101, 102, ..., 108) is connected, is connected to the other one of the two scanning signal lines (16i, 16j; 16m, 16n; ...) selected simultaneously.

9. The display apparatus according to any one of claims 1 to 8, wherein a pixel (101, 102, ..., 108) includes a plurality of pixel electrodes (17ia, 17ib; 17ja, 17jb; 17ma, 17mb; 17na, 17nb; 17IA, 17IB; 17JA, 17JB; 17MA, 17MB; 17NA, 17NB).

10. The display apparatus according to claim 9, further comprising a plurality of storage capacitor wires (18p, 18q), two pixel electrodes (17ia, 17ib; 17ja, 17jb; 17ma, 17mb; 17na, 17nb; 17IA, 17IB; 17JA, 17JB; 17MA, 17MB; 17NA, 17NB) provided in a pixel (101, 102, ..., 108) being connected to a same data signal line (15x, 15y; 15X, 15Y; ...) via different transistors that are connected to a same scanning signal line (16i, 16j; 16m, 16n; ...), one of the two pixel electrodes forming a capacitor with a corresponding one of the storage capacitor wires (18p, 18q), and the other one of the two pixel electrodes forming a capacitor with another one of the storage capacitor wires (18p, 18q).

11. The display apparatus according to claim 9, wherein two pixel electrodes (17ia, 17ib; 17ja, 17jb; 17ma, 17mb; 17na, 17nb; 17IA, 17IB; 17JA, 17JB; 17MA, 17MB; 17NA, 17NB) provided in a pixel are connected to each other via a capacitor, and just one of the two pixel electrodes is connected to a corresponding one of the data signal lines (15x, 15y; 15X, 15Y; ...) via a transistor that is connected to a corresponding one of the scanning signal lines (16i, 16j; 16m, 16n; ...).

12. The display apparatus according to claim 9, further comprising a plurality of storage capacitor wires (18p, 18q), two pixel electrodes (17ia, 17ib; 17ja, 17jb; 17ma, 17mb; 17na, 17nb; 17IA, 17IB; 17JA, 17JB; 17MA, 17MB; 17NA, 17NB) provided in a pixel (101, 102, ..., 108) being connected to a same data signal line (15x, 15y; 15X, 15Y; ...) via different transistors that are connected to a same scanning signal line (16i, 16j; 16m, 16n; ...), one of the two pixel electrodes being connected to a capacitor electrode via a transistor that is connected to another one of the scanning signal lines (16i, 16j; 16m, 16n; ...), the capacitor electrode forming a capacitor with the storage capacitor wire (18p, 18q).

13. The display apparatus according to claim 9, wherein two data signal lines (15x, 15y; 15X, 15Y; ...) are associated with one pixel (101, 102, ..., 108),
one of two pixel electrodes (17ia, 17ib; 17ja, 17jb; 17ma, 17mb; 17na, 17nb; 17IA, 17IB; 17JA, 17JB; 17MA, 17MB; 17NA, 17NB) provided in the pixel (101, 102, ..., 108) is connected to one of the two data signal lines (15x, 15y; 15X, 15Y; ...) via one of two transistors that are connected to a same scanning signal line (16i, 16j; 16m, 16n; ...), and the other one of the two pixel electrodes is connected to the other one of the two data signal lines (15x, 15y; 15X, 15Y; ...) that is connected to the other one of the two transistors.

14. The display apparatus according to claim 1, wherein the plurality of scanning signal lines (16i, 16j; 16m, 16n; ...) and the plurality of data signal lines (15x, 15y; 15X, 15Y; ...) are formed on a substrate, the substrate further having a comb-shaped pixel electrode and a common electrode being formed thereon.

15. A method of driving a display apparatus including scanning signal lines and data signal lines, the method comprising

the steps of:

outputting, to each of the data signal lines (15x, 15y; 15X, 15Y; ...), data signals (Sx, Sy; SX, SY; ...) whose polarities are reversed per one vertical scanning period, per plurality of vertical scanning periods, or per plurality of horizontal scanning periods, while in one horizontal scanning period,
outputting a data signal (Sx, SX, ...) having a polarity to one of two data signal lines (15x, 15y; 15X, 15Y; ...); and
outputting another data signal (Sy, SY, ...) having another polarity to the other of the two data signal lines (15x, 15y; 15X, 15Y; ...), the two data signal lines being arranged adjacent to each other,
characterized in that
activating the scanning signal lines (16i, 16j; 16m, 16n; ...) sequentially in sets of N lines by applying gate signals to the respective scanning signals lines (16i, 16j; 16m, 16n; ...), whereinN≥2; and
when adjacent N lines of a first set of the scanning signal lines (16i, 16j; 16m, 16n; ...) receive respective gate signals (GPm, GPn) to deactivate the scanning signal lines (16i, 16j; 16m, 16n; ...) of the first set from an active state, another N lines of another, second set of the scanning signal lines (16i, 16j; 16m, 16n; ...) receive respective gate signals (GPm, GPn) to activate the scanning signal lines (16i, 16j; 16m, 16n; ...) of the second set from an inactive state;
wherein the sets of adjacent N lines of the signal lines (16i, 16j; 16m, 16n; ...) are identical in consecutive frames (F1, F2).

Patentansprüche

1. Anzeigevorrichtung, umfassend:

Abtastsignalleitungen (16i, 16j; 16m, 16n; ...) und
Datensignalleitungen (15x, 15y; 15X, 15Y; ...), wobei:

jede der Datensignalleitungen (15x, 15y; 15X, 15Y; ...) dafür konfiguriert ist, Datensignale (Sx, Sy, SX, SY, ...) zu empfangen, deren Polaritäten nach einer vertikalen Abtastperiode, nach mehreren vertikalen Abtastperioden oder nach mehreren horizontalen Abtastperioden umgekehrt werden,
in einer horizontalen Abtastperiode eine von zwei Datensignalleitungen (15x, 15y; 15X, 15Y; ...) dafür konfiguriert ist, ein Datensignal (Sx, SX) zu empfangen, welches eine erste Polarität aufweist, und die andere der zwei Datensignalleitungen (15x, 15y; 15X, 15Y; ...) dafür konfiguriert ist, ein Datensignal (Sy, SY) zu empfangen, welches eine zweite Polarität aufweist, die eine andere als die erste Polarität ist, wobei die zwei Datensignalleitungen (15x, 15y; 15X, 15Y; ...) in Nachbarschaft zueinander angeordnet sind,
dadurch gekennzeichnet, dass
die Abtastsignalleitungen (16i, 16j; 16m, 16n; ...) nacheinander in Gruppen benachbarter N Leitungen aktiviert werden, indem Gate-Signale an die entsprechenden Abtastsignalleitungen (16i, 16j; 16m, 16n; ...) angelegt werden, wobei N ≥ 2,
wenn benachbarte N Leitungen einer ersten Gruppe entsprechende Gate-Signale (GPi, GPj) zum Deaktivieren der Abtastsignalleitungen der ersten Gruppe aus einem aktiven Zustand empfangen, andere benachbarte N Leitungen einer anderen zweiten Gruppe (16m, 16n) entsprechende Gate-Signale (GPm, GPn) zum Aktivieren der Abtastsignalleitungen der zweiten Gruppe (16m, 16n) aus einem inaktiven Zustand empfangen; und
wobei die Gruppen benachbarter N Leitungen der Signalleitungen (16i, 16j; 16m, 16n; ...) in aufeinander folgenden Rahmen (F1, F2) identisch sind.

2. Anzeigevorrichtung nach Anspruch 1, wobei eine Abtastsignalleitung (16i, 16j; 16m, 16n; ...) durch einen Anstieg eines Abtastimpulses (GPi, GPj; GPm, GPn; ...) aktiviert wird, welcher der Abtastsignalleitung (16i, 16j; 16m, 16n; ...) zugeführt wird, und anschließend durch ein Absinken des Abtastimpulses (GPi, GPj; GPm, GPn; ...) deaktiviert wird oder durch ein Absinken eines Abtastimpulses (GPi, GPj; GPm, GPn; ...) aktiviert wird, welcher der Abtastsignalleitung (16i, 16j; 16m, 16n; ...) zugeführt wird, und anschließend durch einen Anstieg des Abtastimpulses (GPi, GPj; GPm, GPn; ...) deaktiviert wird.

3. Anzeigevorrichtung nach Anspruch 2, wobei ein Abtastimpuls (GPi, GPj; GPm, GPn; ...) einer aktuellen Stufe gleichzeitig mit einem Start einer horizontalen Abtastperiode aktiviert wird, welche der aktuellen Stufe entspricht, und der Abtastimpuls (GPi, GPj; GPm, GPn; ...) der aktuellen Stufe gleichzeitig mit der Beendigung der horizontalen Abtastperiode deaktiviert wird, welche der aktuellen Stufe entspricht.

4. Anzeigevorrichtung nach Anspruch 2, wobei ein Abtastimpuls (GPi, GPj; GPm, GPn; ...) einer aktuellen Stufe gleichzeitig mit einem Start einer horizontalen Abtastperiode aktiviert wird, welche einer vorhergehenden Stufe entspricht, und der Abtastimpuls (GPi, GPj; GPm, GPn; ...) der aktuellen Stufe gleichzeitig mit der Beendigung der horizontalen Abtastperiode deaktiviert wird, welche der aktuellen Stufe entspricht.

5. Anzeigevorrichtung nach einem der Ansprüche 1 bis 4, ferner umfassend:

eine überzählige Leitung (PW) zur Verwendung zum Reparieren einer Trennung der Datensignalleitungen (15x, 15y; 15X, 15Y; ...),
wobei eine reparierte Datensignalleitung der Datensignalleitungen (15x, 15y; 15X, 15Y; ...) die Datensignale (Sx, Sy, SX, SY) von einem ihrer Enden empfängt sowie die Datensignale (Sx, Sy, SX, SY) von dem anderen ihrer Enden über die überzählige Leitung empfängt.

6. Anzeigevorrichtung nach einem der Ansprüche 1 bis 5, wobei:

N = 2 und zwei Abtastsignalleitungen (16i, 16j; 16m, 16n; ...) gleichzeitig ausgewählt werden,
zwei der Datensignalleitungen (15x, 15y; 15X, 15Y; ...) zu einer ersten Pixelspalte (α) gehören und zwei andere der Datensignalleitungen (15x, 15y; 15X, 15Y; ...) zu einer zweiten Pixelspalte (β) in Nachbarschaft zu der ersten Pixelspalte gehören,
wobei jedes der Pixel (101, 102, ..., 108) mindestens eine Pixelelektrode (17i, 17j, 17m, 17n; 17I, 17J, 17M, 17N) umfasst und
eine Pixelelektrode (17i, 17j, 17m, 17n) in der ersten Pixelspalte (α) über einen Transistor (12i, 12j, 12m, 12n) mit einer der zwei Datensignalleitungen (15x, 15y; 15X, 15Y; ...) verbunden ist, die zu der ersten Pixelspalte (α) gehört, und eine Pixelelektrode (17I, 17J, 17M, 17N) in der zweiten Pixelspalte (β) über einen anderen Transistor (121, 12J, 12M, 12N) mit einer der zwei Datensignalleitungen (15x, 15y; 15X, 15Y; ...) verbunden ist, die zu der zweiten Pixelspalte (β) gehört.

7. Anzeigevorrichtung nach Anspruch 6, wobei die Pixelelektrode (17i, 17j, 17m, 17n), die in der ersten Pixelspalte (α) enthalten ist, so angeordnet ist, dass die in der ersten Pixelspalte (α) enthaltene Pixelelektrode (17i, 17j, 17m, 17n) die zwei Datensignalleitungen (15x, 15y; 15X, 15Y; ...) überlappt, die zu der ersten Pixelspalte (α) gehören, und die Pixelelektrode (17I, 17J, 17M, 17N), die in der zweiten Pixelspalte (β) enthalten ist, so angeordnet ist, dass die in der zweiten Pixelspalte (β) enthaltene Pixelelektrode (17I, 17J, 17M, 17N) die zwei Datensignalleitungen (15x, 15y; 15X, 15Y; ...) überlappt, die zu der zweiten Pixelspalte (β) gehören.

8. Anzeigevorrichtung nach Anspruch 6, wobei in jeder der ersten Pixelspalte (α) und der zweiten Pixelspalte (β) eine Pixelelektrode (17i, 17j, 17m, 17n, 17I, 17J, 17M, 17N) eines von zwei aufeinander folgenden Pixeln (101, 102, ..., 108) über einen Transistor (12i, 12j, 12m, 12n) mit einer Datensignalleitung verbunden ist, die sich von derjenigen unterscheidet, die über einen anderen Transistor (12I, 12J, 12M, 12N) mit der Pixelelektrode (17i, 17j, 17m, 17n, 17I, 17J, 17M, 17N) des anderen der zwei aufeinander folgenden Pixel (101, 102, ..., 108) verbunden ist, und
der Transistor, mit welchem die Pixelelektrode (17i, 17j, 17m, 17n, 17I, 17J, 17M, 17N) verbunden ist, die in dem einen der zwei aufeinander folgenden Pixel (101, 102, ..., 108) enthalten ist, mit einer der zwei Abtastsignalleitungen (16i, 16j; 16m, 16n; ...) verbunden ist, die gleichzeitig ausgewählt werden, und der Transistor, mit welchem die Pixelelektrode (17i, 17j, 17m, 17n, 17I, 17J, 17M, 17N) verbunden ist, die in dem anderen der zwei aufeinander folgenden Pixel (101, 102, ..., 108) enthalten ist, mit der anderen der zwei Abtastsignalleitungen (16i, 16j; 16m, 16n; ...) verbunden ist, die gleichzeitig ausgewählt werden.

9. Anzeigevorrichtung nach einem der Ansprüche 1 bis 8, wobei ein Pixel (101, 102, ..., 108) mehrere Pixelelektroden (17ia, 17ib; 17ja, 17jb; 17ma, 17mb; 17na, 17nb; 17IA, 17IB; 17JA, 17JB; 17MA, 17MB; 17NA, 17NB) umfasst.

10. Anzeigevorrichtung nach Anspruch 9, ferner umfassend mehrere Speicherkondensatorleitungen (18p, 18q),
wobei zwei Pixelelektroden (17ia, 17ib; 17ja, 17jb; 17ma, 17mb; 17na, 17nb; 17IA, 17IB; 17JA, 17JB; 17MA, 17MB; 17NA, 17NB), die in einem Pixel (101, 102, ..., 108) vorgesehen sind, über verschiedene Transistoren, welche mit einer gleichen Abtastsignalleitung (16i, 16j; 16m, 16n; ...) verbunden sind, mit einer gleichen Datensignalleitung (15x, 15y; 15X, 15Y; ...) verbunden sind, wobei eine der zwei Pixelelektroden mit einer entsprechenden der Speicherkondensatorleitungen (18p, 18q) einen Kondensator bildet und die andere der zwei Pixelelektroden mit einer anderen der Speicherkondensatorleitungen (18p, 18q) einen Kondensator bildet.

11. Anzeigevorrichtung nach Anspruch 9, wobei die zwei Pixelelektroden (17ia, 17ib; 17ja, 17jb; 17ma, 17mb; 17na,

17nb; 17IA, 17IB; 17JA, 17JB; 17MA, 17MB; 17NA, 17NB), die in einem Pixel vorgesehen sind, über einen Kondensator miteinander verbunden sind und nur eine der zwei Pixelelektroden über einen Transistor, der mit einer entsprechenden der Abtastsignalleitungen (16i, 16j; 16m, 16n; ...) verbunden ist, mit einer entsprechenden der Datensignalleitungen (15x, 15y; 15X, 15Y; ...) verbunden ist.

12. Anzeigevorrichtung nach Anspruch 9, ferner umfassend mehrere Speicherkondensatorleitungen (18p, 18q), wobei zwei Pixelelektroden (17ia, 17ib; 17ja, 17jb; 17ma, 17mb; 17na, 17nb; 17IA, 17IB; 17JA, 17JB; 17MA, 17MB; 17NA, 17NB), die in einem Pixel (101, 102, ..., 108) vorgesehen sind, über verschiedene Transistoren, welche mit einer gleichen Abtastsignalleitung (16i, 16j; 16m, 16n; ...) verbunden sind, mit einer gleichen Datensignalleitung (15x, 15y; 15X, 15Y; ...) verbunden sind, wobei eine der zwei Pixelelektroden über einen Transistor, der mit einer anderen der Abtastsignalleitungen (16i, 16j; 16m, 16n; ...) verbunden ist, mit einer Kondensatorelektrode verbunden ist, wobei die Kondensatorelektrode mit der Speicherkondensatorleitung (18p, 18q) einen Kondensator bildet.

13. Anzeigevorrichtung nach Anspruch 9, wobei die Datensignalleitungen (15x, 15y; 15X, 15Y; ...) zu einem Pixel (101, 102, ..., 108) gehören,
wobei eine von zwei Pixelelektroden (17ia, 17ib; 17ja, 17jb; 17ma, 17mb; 17na, 17nb; 17IA, 17IB; 17JA, 17JB; 17MA, 17MB; 17NA, 17NB), die in dem Pixel (101, 102, ..., 108) vorgesehen sind, über einen von zwei Transistoren, welche mit einer gleichen Abtastsignalleitung (16i, 16j; 16m, 16n; ...) verbunden sind, mit einer der zwei Datensignalleitung (15x, 15y; 15X, 15Y; ...) verbunden ist und die andere der zwei Pixelelektroden mit der anderen der zwei Datensignalleitungen (15x, 15y; 15X, 15Y; ...) verbunden ist, die mit dem anderen der zwei Transistoren verbunden ist.

14. Anzeigevorrichtung nach Anspruch 1, wobei die mehreren Abtastsignalleitungen (16i, 16j; 16m, 16n; ...) und die mehreren Datensignalleitungen (15x, 15y; 15X, 15Y; ...) auf einem Substrat ausgebildet sind, wobei das Substrat ferner eine kammförmige Pixelelektrode und eine darauf ausgebildete gemeinsame Elektrode aufweist.

15. Verfahren zum Antreiben der Anzeigevorrichtung, welche Abtastsignalleitungen und Datensignalleitungen umfasst, wobei das Verfahren die Schritte umfasst:

Ausgeben von Datensignalen (Sx, Sy, SX, SY, ...), deren Polaritäten nach einer vertikalen Abtastperiode, nach mehreren vertikalen Abtastperioden oder nach mehreren horizontalen Abtastperioden umgekehrt werden, an jede der Datensignalleitungen (15x, 15y; 15X, 15Y; ...) während einer horizontalen Abtastperiode,
Ausgeben eines Datensignals (Sx, SX, ...), welches eine Polarität aufweist, an eine von zwei Datensignalleitungen (15x, 15y; 15X, 15Y; ...) und
Ausgeben eines anderen Datensignals (Sy, SY, ...) welches eine andere Polarität aufweist, an die andere der zwei Datensignalleitungen (15x, 15y; 15X, 15Y; ...), wobei die zwei Datensignalleitungen in Nachbarschaft zueinander angeordnet sind,
dadurch gekennzeichnet, dass
die Abtastsignalleitungen (16i, 16j; 16m, 16n; ...) nacheinander in Gruppen von N Leitungen aktiviert werden, indem Gate-Signale an die entsprechenden Abtastsignalleitungen (16i, 16j; 16m, 16n; ...) angelegt werden, wobei $N \geq 2$; und
wenn benachbarte N Leitungen einer ersten Gruppe der Abtastsignalleitungen (16i, 16j; 16m, 16n; ...) entsprechende Gate-Signale (GPm, GPn) zum Deaktivieren der Abtastsignalleitungen (16i, 16j; 16m, 16n; ...) der ersten Gruppe aus einem aktiven Zustand empfangen, andere N Leitungen einer anderen, zweiten Gruppe der Abtastsignalleitungen (16i, 16j; 16m, 16n; ...) entsprechende Gate-Signale (GPm, GPn) zum Aktivieren der Abtastsignalleitungen (16i, 16j; 16m, 16n; ...) der zweiten Gruppe aus einem inaktiven Zustand empfangen;
wobei die Gruppen benachbarter N Leitungen der Signalleitungen (16i, 16j; 16m, 16n; ...) in aufeinander folgenden Rahmen (F1, F2) identisch sind.

Revendications

1. Appareil d'affichage comportant :

des lignes de signaux de balayage (16i, 16j ; 16m, 16n ; ...) ; et
des lignes de signaux de données (15x, 15y ; 15X, 15Y ; ...), dans lequel :

chacune des lignes de signaux de données (15x, 15y ; 15X, 15Y ; ...) est configurée de manière à recevoir

des signaux de données (Sx, Sy, SX, SY, ...) dont les polarités sont inversées pour une période de balayage vertical, pour une pluralité de périodes de balayage vertical, ou pour une pluralité de périodes de balayage horizontal ;
dans une période de balayage horizontal, une ligne parmi deux lignes de signaux de données (15x, 15y ; 15X, 15Y ; ...) est configurée de manière à recevoir un signal de données (Sx, SX) présentant une première polarité, et l'autre des deux lignes de signaux de données (15x, 15y ; 15X, 15Y ; ...) est configurée de manière à recevoir un autre signal de données (Sy, SY) présentant une seconde polarité distincte de la première polarité, les deux lignes de signaux de données (15x, 15y ; 15X, 15Y ; ...) étant agencées de manière à être mutuellement adjacentes ;

caractérisé en ce que :

les lignes de signaux de balayage (16i, 16j ; 16m, 16n ; ...) sont rendues séquentiellement actives dans des ensembles de N lignes adjacentes en appliquant des signaux de porte logique aux lignes de signaux de balayage respectives (16i, 16j ; 16m, 16n ; ...), où $N \geq 2$;
lorsque N lignes adjacentes d'un premier ensemble reçoivent des signaux de porte logique respectifs (GPi, GPj) pour désactiver les lignes de signaux de balayage du premier ensemble à partir d'un état actif, d'autres N lignes adjacentes d'un autre second ensemble (16m, 16n) reçoivent des signaux de porte logique respectifs (GPm, GPn) pour activer les lignes de signaux de balayage dudit second ensemble (16m, 16n) à partir d'un état inactif ; et
dans lequel les ensembles de N lignes adjacentes des lignes de signaux (16i, 16j ; 16m, 16n ; ...) sont identiques dans des trames consécutives (F1, F2).

2. Appareil d'affichage selon la revendication 1, dans lequel une ligne de signaux de balayage (16i, 16j ; 16m, 16n ; ...) est activée par une montée d'une impulsion de balayage (GPi, GPj ; GPm, GPn ; ...) fournie à la ligne de signaux de balayage (16i, 16j ; 16m, 16n ; ...), et est subséquemment désactivée par une descente de l'impulsion de balayage (GPi, GPj ; GPm, GPn ; ...), ou est activée par une descente d'une impulsion de balayage (GPi, GPj ; GPm, GPn ; ...) fournie à la ligne de signaux de balayage (16i, 16j ; 16m, 16n ; ...) et est subséquemment désactivée par une montée de l'impulsion de balayage (GPi, GPj ; GPm, GPn ; ...).

3. Appareil d'affichage selon la revendication 2, dans lequel une impulsion de balayage (GPi, GPj ; GPm, GPn ; ...) d'un étage en cours est activée simultanément à un début d'une période de balayage horizontal correspondant à l'étage en cours, et l'impulsion de balayage (GPi, GPj ; GPm, GPn ; ...) de l'étage en cours est désactivée simultanément à la fin de la période de balayage horizontal correspondant à l'étage en cours.

4. Appareil d'affichage selon la revendication 2, dans lequel une impulsion de balayage (GPi, GPj ; GPm, GPn ; ...) d'un étage en cours est activée simultanément à un début d'une période de balayage horizontal correspondant à un étage précédent, et l'impulsion de balayage (GPi, GPj ; GPm, GPn ; ...) de l'étage en cours est désactivée simultanément à la fin de la période de balayage horizontal correspondant à l'étage en cours.

5. Appareil d'affichage selon l'une quelconque des revendications 1 à 4, comportant en outre :

un fil de secours (PW) destiné à être utilisé dans le cadre de la réparation d'une déconnexion des lignes de signaux de données (15x, 15y ; 15X, 15Y ; ...) ;
une ligne de signaux de données réparée des lignes de signaux de données (15x, 15y ; 15X, 15Y ; ...) recevant les signaux de données (Sx, Sy, SX, SY) en provenance de l'une de ses extrémités, et recevant les signaux de données (Sx, Sy, SX, SY) en provenance de l'autre de ses extrémités, par le biais du fil de secours.

6. Appareil d'affichage selon l'une quelconque des revendications 1 à 5, dans lequel :

N = 2, et deux lignes de signaux de balayage (16i, 16j ; 16m, 16n ; ...) sont sélectionnées simultanément ;
deux des lignes de signaux de données (15x, 15y ; 15X, 15Y ; ...) sont associées à une première colonne de pixels (α) et deux autres des lignes de signaux de données (15x, 15y ; 15X, 15Y ; ...) sont associées à une seconde colonne de pixels (β) adjacente à la première colonne de pixels ;
les pixels (101, 102, ..., 108) incluent chacun au moins une électrode de pixel (17i, 17j, 17m, 17n ; 17I, 17J, 17M, 17N) ; et
une électrode de pixel (17i, 17j, 17m, 17n) dans la première colonne de pixels (α) est connectée, par le biais d'un transistor (12i, 12j, 12m, 12n), à l'une quelconque des deux lignes de signaux de données (15x, 15y ; 15X,

15Y ; ...) associées à la première colonne de pixels (α), et une électrode de pixel (17I, 17J, 17M, 17N) dans la seconde colonne de pixels (β) est connectée, par le biais d'un autre transistor (12I, 12J, 12M, 12N), à l'une quelconque des deux lignes de signaux de données (15x, 15y ; 15X, 15Y ; ...) associées à la seconde colonne de pixels (β).

7. Appareil d'affichage selon la revendication 6, dans lequel l'électrode de pixel (17i, 17j, 17m, 17n) incluse dans la première colonne de pixels (α) est disposée de sorte que l'électrode de pixel (17i, 17j, 17m, 17n) incluse dans la première colonne de pixels (α) chevauche les deux lignes de signaux de données (15x, 15y ; 15X, 15Y ; ...) associées à la première colonne de pixels (α), et l'électrode de pixel (17I, 17J, 17M, 17N) incluse dans la seconde colonne de pixels (β) est disposée de sorte que l'électrode de pixel (17I, 17J, 17M, 17N) incluse dans la seconde colonne de pixels (β) chevauche les deux lignes de signaux de données (15x, 15y ; 15X, 15Y ; ...) associées à la seconde colonne de pixels (β).

8. Appareil d'affichage selon la revendication 6, dans lequel, dans chacune de la première colonne de pixels (α) et de la seconde colonne de pixels (β), une électrode de pixel (17i, 17j, 17m, 17n ; 17I, 17J, 17M, 17N) de l'un des deux pixels consécutifs (101, 102, ..., 108) est connectée, par le biais d'un transistor (12i, 12j, 12m, 12n), à une ligne de signaux de données différente de celle connectée à l'électrode de pixel (17i, 17j, 17m, 17n ; 17I, 17J, 17M, 17N) de l'autre pixel des deux pixels consécutifs (101, 102, ..., 108) par le biais d'un autre transistor (12I, 12J, 12M, 12N) ; et le transistor, auquel est connectée l'électrode de pixel (17i, 17j, 17m, 17n ; 17I, 17J, 17M, 17N) incluse dans ledit un pixel des deux pixels consécutifs (101, 102, ..., 108), est connecté à l'une des deux lignes de signaux de balayage (16i, 16j ; 16m, 16n ; ...) sélectionnées simultanément, et le transistor, auquel est connectée l'électrode de pixel (17i, 17j, 17m, 17n ; 17I, 17J, 17M, 17N) incluse dans l'autre pixel des deux pixels consécutifs (101, 102, ..., 108), est connecté à l'autre des deux lignes de signaux de balayage (16i, 16j ; 16m, 16n ; ...) sélectionnées simultanément.

9. Appareil d'affichage selon l'une quelconque des revendications 1 à 8, dans lequel un pixel (101, 102, ..., 108) inclut une pluralité d'électrodes de pixel (17ia, 17ib ; 17ja, 17jb ; 17ma, 17mb ; 17na, 17nb ; 17IA, 17IB ; 17JA, 17JB ; 17MA, 17MB ; 17NA, 17NB).

10. Appareil d'affichage selon la revendication 9, comportant en outre une pluralité de fils de condensateur de stockage (18p, 18q) ;
deux électrodes de pixel (17ia, 17ib ; 17ja, 17jb ; 17ma, 17mb ; 17na, 17nb ; 17IA, 17IB ; 17JA, 17JB ; 17MA, 17MB ; 17NA, 17NB) fournies dans un pixel (101, 102, ..., 108) étant connectées à une même ligne de signaux de données (15x, 15y ; 15X, 15Y ; ...) par le biais de différents transistors qui sont connectés à une même ligne de signaux de balayage (16i, 16j ; 16m, 16n ; ...), l'une des deux électrodes de pixel formant un condensateur avec un fil correspondant des fils de condensateur de stockage (18p, 18q), et l'autre des deux électrodes de pixel formant un condensateur avec un autre des fils de condensateur de stockage (18p, 18q).

11. Appareil d'affichage selon la revendication 9, dans lequel deux électrodes de pixel (17ia, 17ib ; 17ja, 17jb ; 17ma, 17mb ; 17na, 17nb ; 17IA, 17IB ; 17JA, 17JB ; 17MA, 17MB ; 17NA, 17NB) fournies dans un pixel sont mutuellement connectées par le biais d'un condensateur, et une seul des deux électrodes de pixel est connectée à une ligne correspondante des lignes de signaux de données (15x, 15y ; 15X, 15Y ; ...) par le biais d'un transistor qui est connecté à une ligne correspondante des lignes de signaux de balayage (16i, 16j ; 16m, 16n ; ...).

12. Appareil d'affichage selon la revendication 9, comportant en outre une pluralité de fils de condensateur de stockage (18p, 18q) ;
deux électrodes de pixel (17ia, 17ib ; 17ja, 17jb ; 17ma, 17mb ; 17na, 17nb ; 17IA, 17IB ; 17JA, 17JB ; 17MA, 17MB ; 17NA, 17NB) fournies dans un pixel (101, 102, ..., 108) étant connectées à une même ligne de signaux de données (15x, 15y ; 15X, 15Y ; ...) par le biais de différents transistors qui sont connectés à une même ligne de signaux de balayage (16i, 16j ; 16m, 16n ; ...), l'une des deux électrodes de pixel étant connectée à une électrode de condensateur par le biais d'un transistor qui est connecté à une autre des lignes de signaux de balayage (16i, 16j ; 16m, 16n ; ...), l'électrode de condensateur formant un condensateur avec le fil de condensateur de stockage (18p, 18q).

13. Appareil d'affichage selon la revendication 9, dans lequel deux lignes de signaux de données (15x, 15y; 15X, 15Y ; ...) sont associées à un pixel (101, 102, ..., 108) ; l'une des deux électrodes de pixel (17ia, 17ib ; 17ja, 17jb ; 17ma, 17mb ; 17na, 17nb ; 17IA, 17IB ; 17JA, 17JB ; 17MA, 17MB ; 17NA, 17NB) fournies dans le pixel (101, 102, ..., 108) est connectée à l'une des deux lignes de signaux de données (15x, 15y ; 15X, 15Y ; ...) par le biais de l'un des deux transistors qui sont connectés à une même ligne de signaux de balayage (16i, 16j ; 16m, 16n ; ...), et l'autre des deux électrodes de pixel est connectée à l'autre des deux lignes de signaux de données (15x, 15y ;

15X, 15Y ; ...) qui est connectée à l'autre des deux transistors.

14. Appareil d'affichage selon la revendication 1, dans lequel la pluralité de lignes de signaux de balayage (16i, 16j ; 16m, 16n ; ...) et la pluralité de lignes de signaux de données (15x, 15y ; 15X, 15Y ; ...) sont formées sur un substrat, le substrat présentant en outre une électrode de pixel en forme de peigne et une électrode de référence formées sur celui-ci.

15. Procédé de commande d'un appareil d'affichage incluant des lignes de signaux de balayage et des lignes de signaux de données, le procédé comportant les étapes ci-dessous consistant à :

fournir en sortie, dans chacune des lignes de signaux de données (15x, 15y ; 15X, 15Y ; ...), des signaux de données (Sx, Sy ; SX, SY ; ...) dont les polarités sont inversées pour une période de balayage vertical, pour une pluralité de périodes de balayage vertical, ou pour une pluralité de périodes de balayage horizontal, au cours d'une période de balayage horizontal,

fournir en sortie un signal de données (Sx, SX, ...) présentant une polarité à l'une des deux lignes de signaux de données (15x, 15y ; 15X, 15Y ; ...) ; et

fournir en sortie un autre signal de données (Sy, SY, ...) présentant une autre polarité à l'autre des deux lignes de signaux de données (15x, 15y ; 15X, 15Y ; ...), les deux lignes de signaux de données étant agencées de manière à être mutuellement adjacentes ;

caractérisé en ce qu'il comporte les étapes ci-dessous consistant à

activer les lignes de signaux de balayage (16i, 16j ; 16m, 16n ; ...) séquentiellement dans des ensembles de N lignes, en appliquant des signaux de porte logique aux lignes de signaux de balayage respectives (16i, 16j ; 16m, 16n ; ...), dans lequel $N \geq 2$; et

dans lequel lorsque N lignes adjacentes d'un premier ensemble des lignes de signaux de balayage (16i, 16j ; 16m, 16n ; ...) reçoivent des signaux de porte logique respectifs (GPm, GPn) pour désactiver les lignes de signaux de balayage (16i, 16j ; 16m, 16n ; ...) du premier ensemble à partir d'un état actif, N autres lignes d'un autre second ensemble des lignes de signaux de balayage (16i, 16j ; 16m, 16n ; ...) reçoivent des signaux de porte logique respectifs (GPm, GPn) pour activer les lignes de signaux de balayage (16i, 16j ; 16m, 16n ; ...) du second ensemble à partir d'un état inactif ;

dans lequel les ensembles de N lignes adjacentes des lignes de signaux (16i, 16j ; 16m, 16n ; ...) sont identiques dans des trames consécutives (F1, F2).

FIG. 1

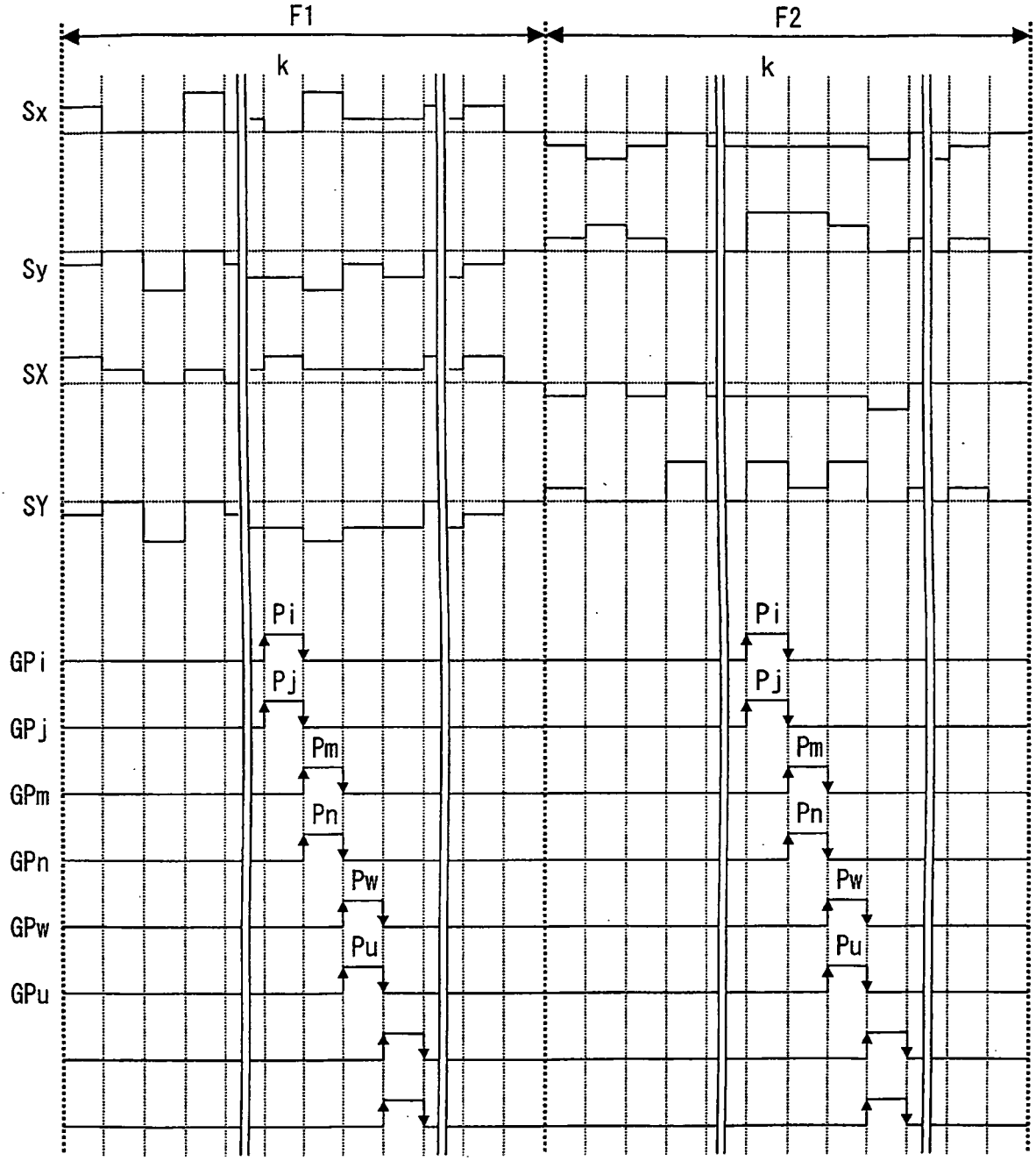


FIG. 2

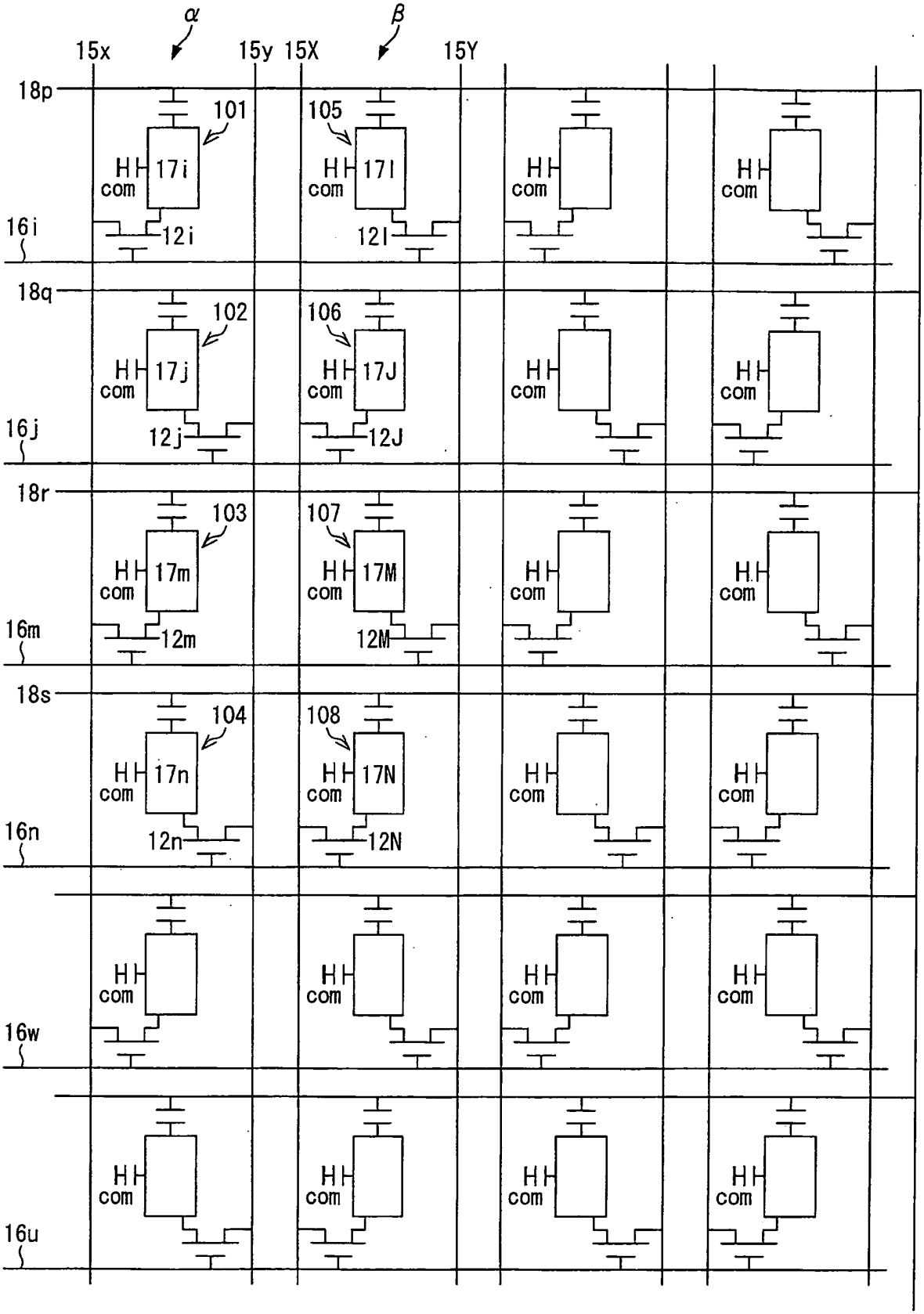

α
β
15x
15y
15X
15Y
18p
18q
18r
18s
16i
16j
16m
16n
16w
16u
101
102
103
104
105
106
107
108
17i
17j
17m
17n
17I
17J
17M
17N
12i
12j
12m
12n
12I
12J
12M
12N
com

FIG. 3

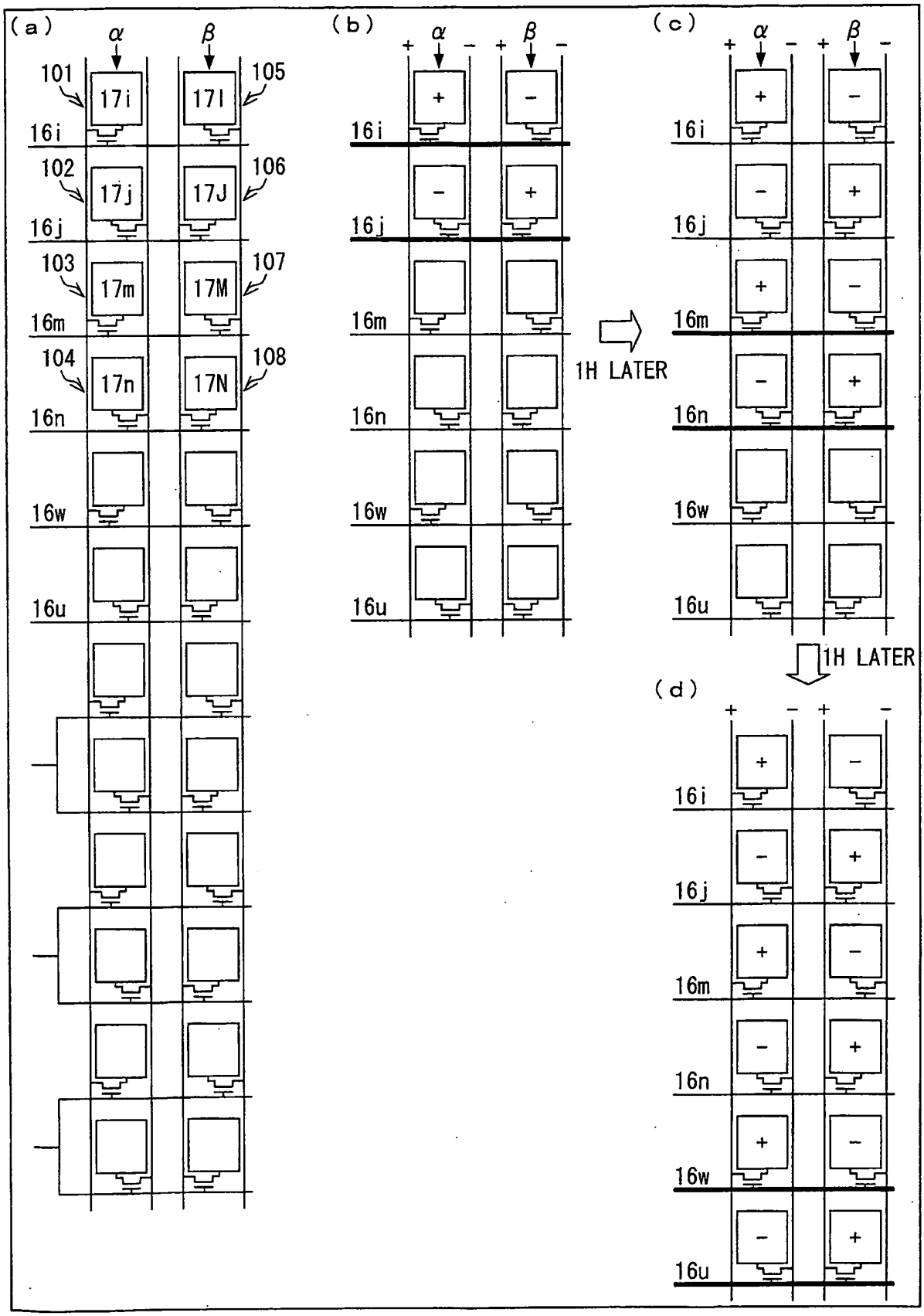

(a)
α
β
101
17i
105
171
16i
102
17j
106
17J
16j
103
17m
107
17M
16m
104
17n
108
17N
16n
16w
16u
(b)
α
β
+
−
16i
16j
16m
16n
16w
16u
1H LATER
(c)
α
β
16i
16j
16m
16n
16w
16u
1H LATER
(d)
16i
16j
16m
16n
16w
16u

FIG. 4

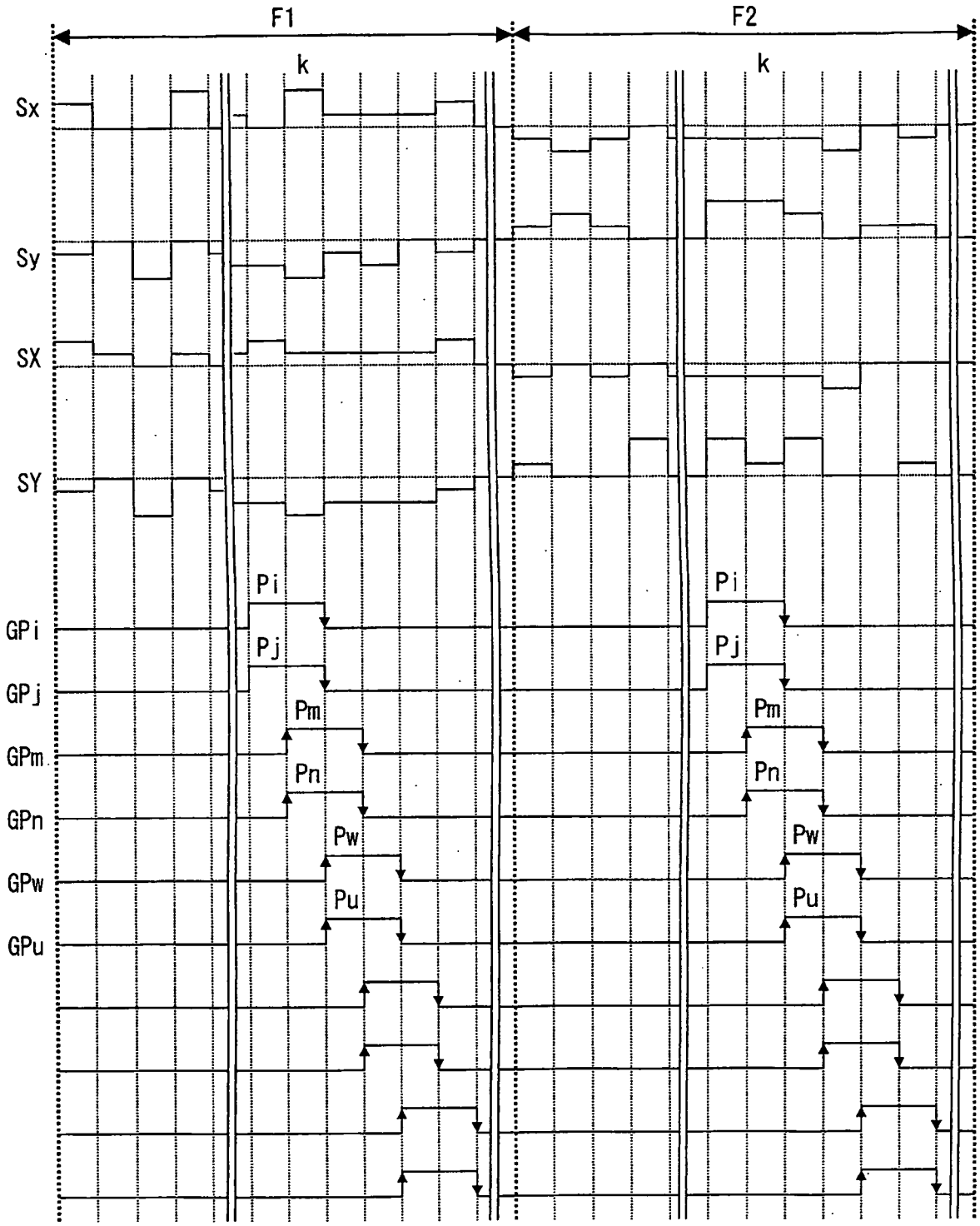


FIG. 5

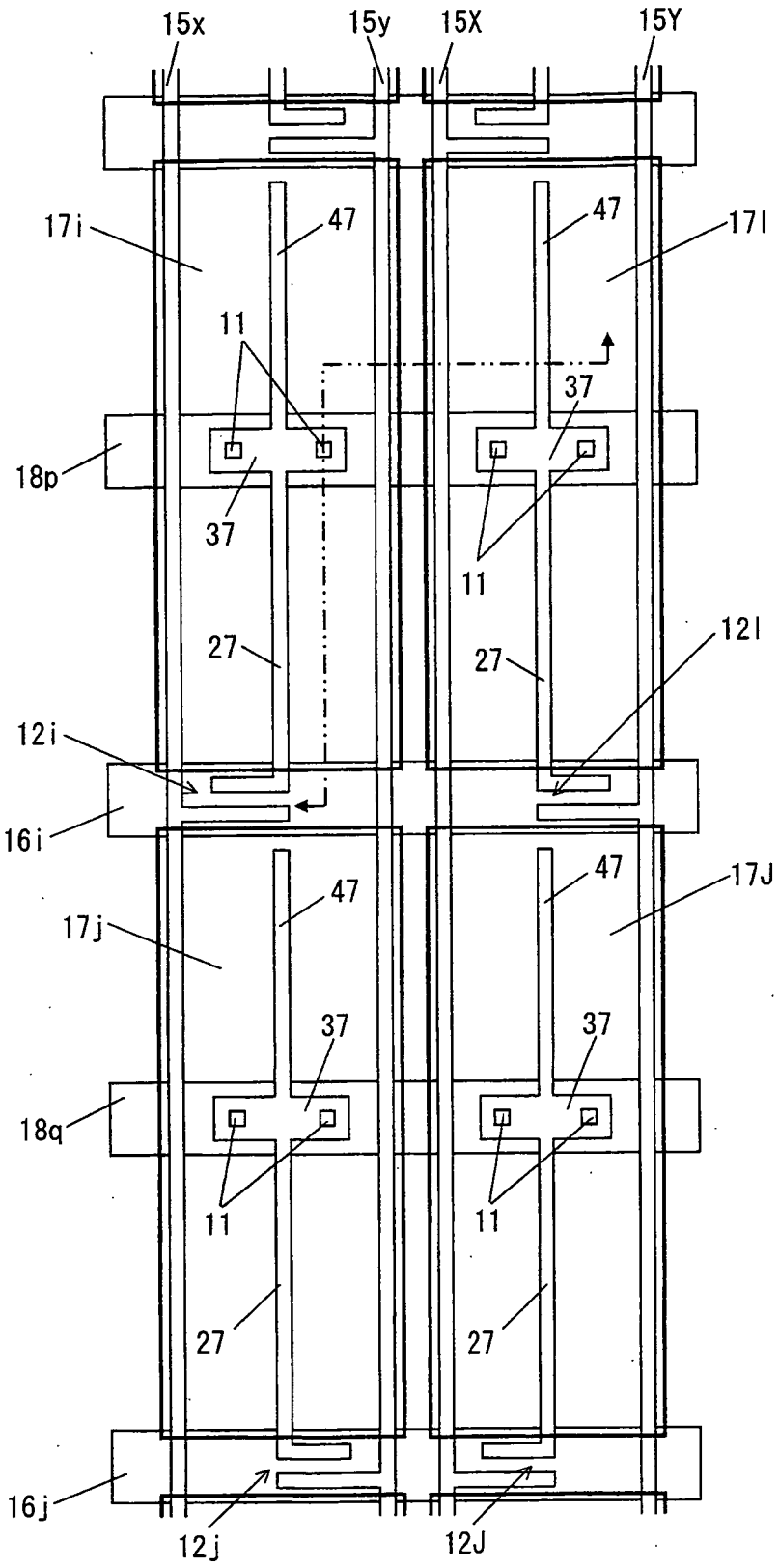

15x
15y
15X
15Y
17i
47
47
17I
11
37
37
18p
37
11
27
27
12I
12i
16i
47
47
17J
17j
37
37
18q
11
11
27
27
16j
12j
12J

FIG. 6

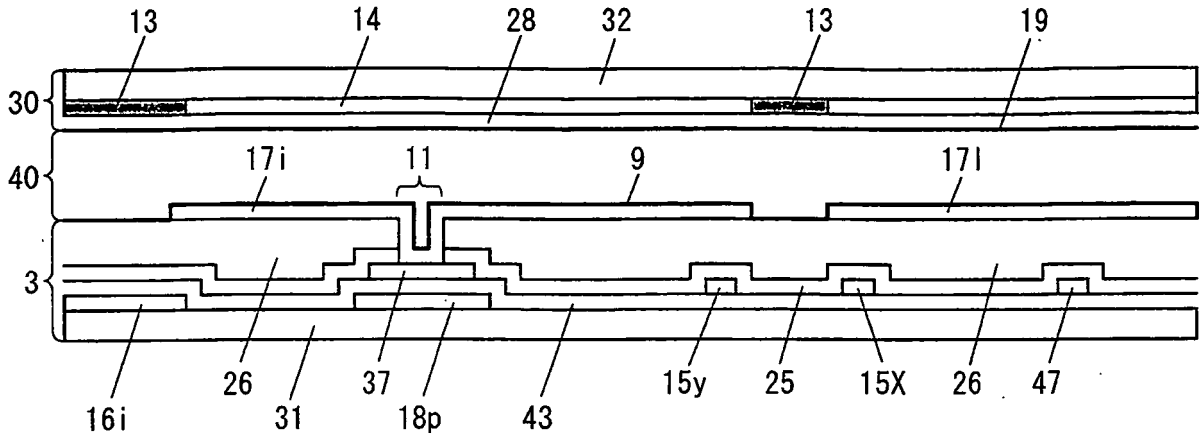

13
14
28
32
13
19
30
40
17i
11
9
17l
3
16i
26
31
37
18p
43
15y
25
15X
26
47

FIG. 7

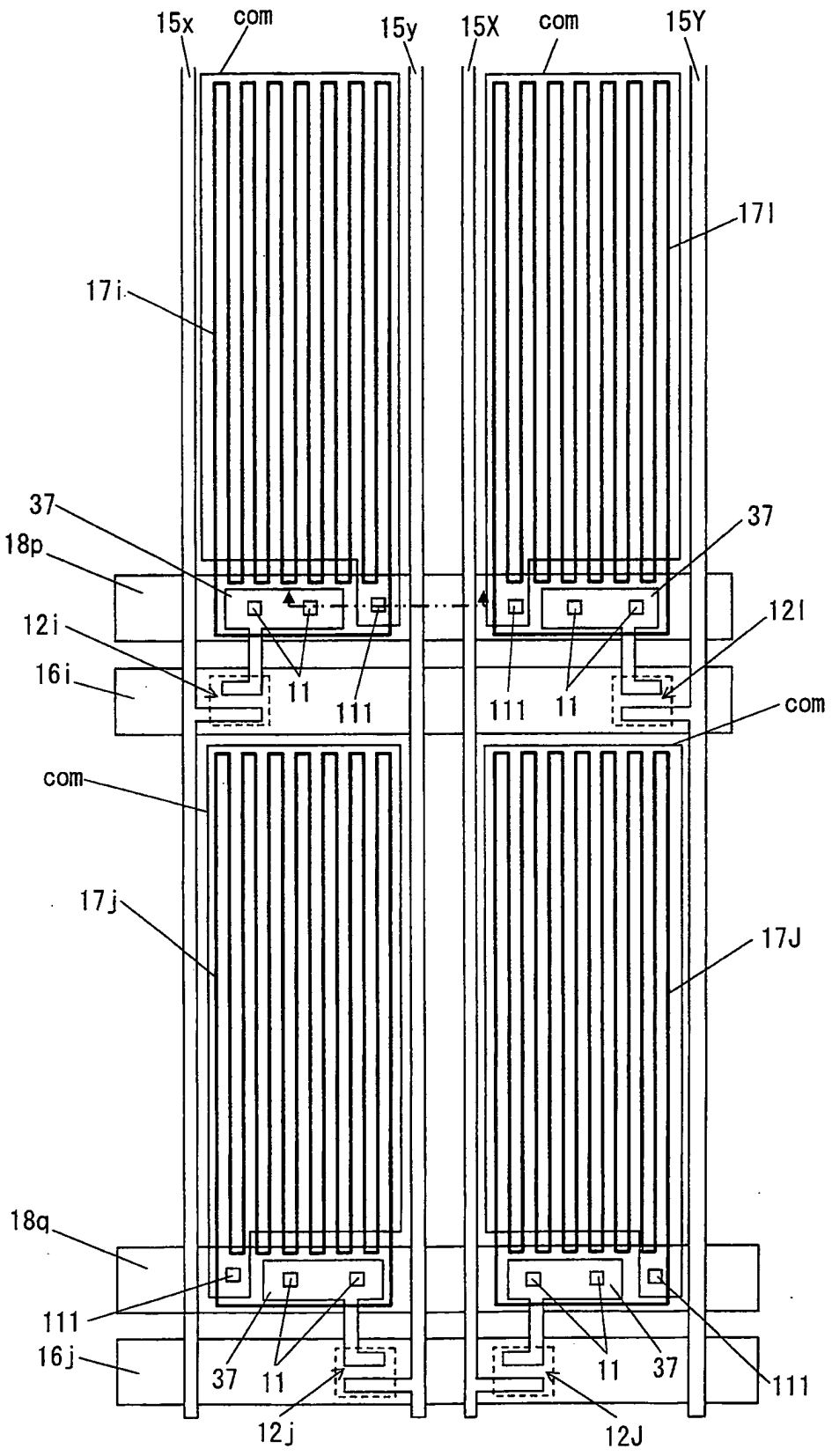

15x
com
15y
15X
com
15Y
17i
17I
37
18p
37
12i
12I
16i
11
111
111
11
com
com
17j
17J
18q
111
16j
37
11
11
37
111
12j
12J

FIG. 8

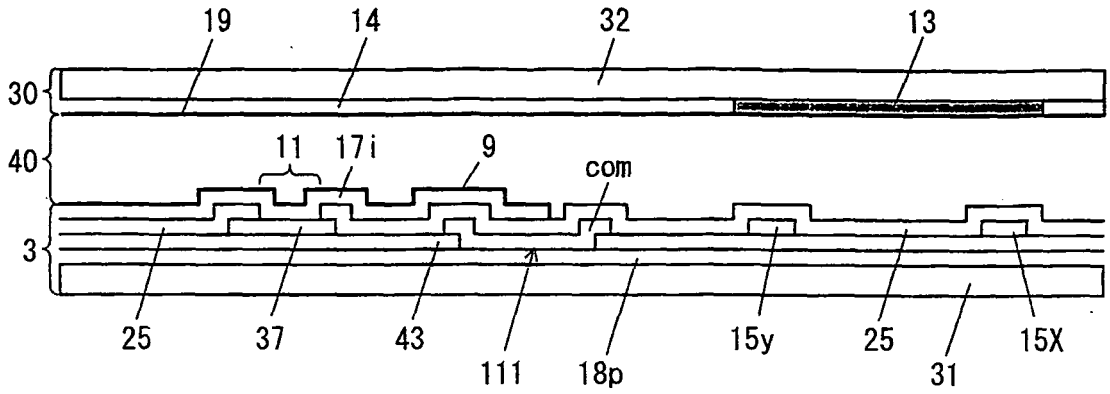


FIG. 9

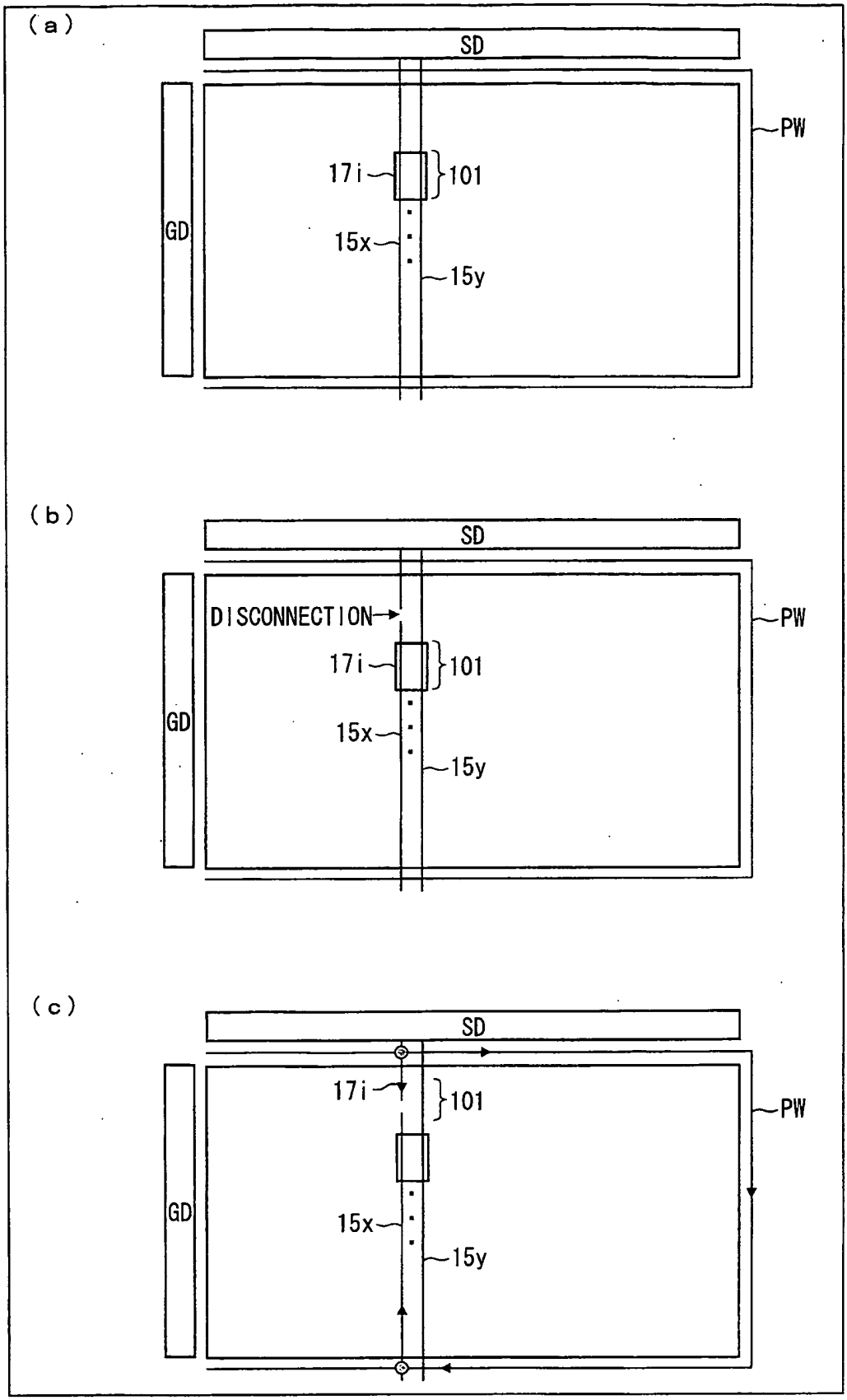

(a)
SD
PW
17i
101
GD
15x
15y
(b)
SD
DISCONNECTION
PW
17i
101
GD
15x
15y
(c)
SD
17i
101
PW
GD
15x
15y

FIG. 10

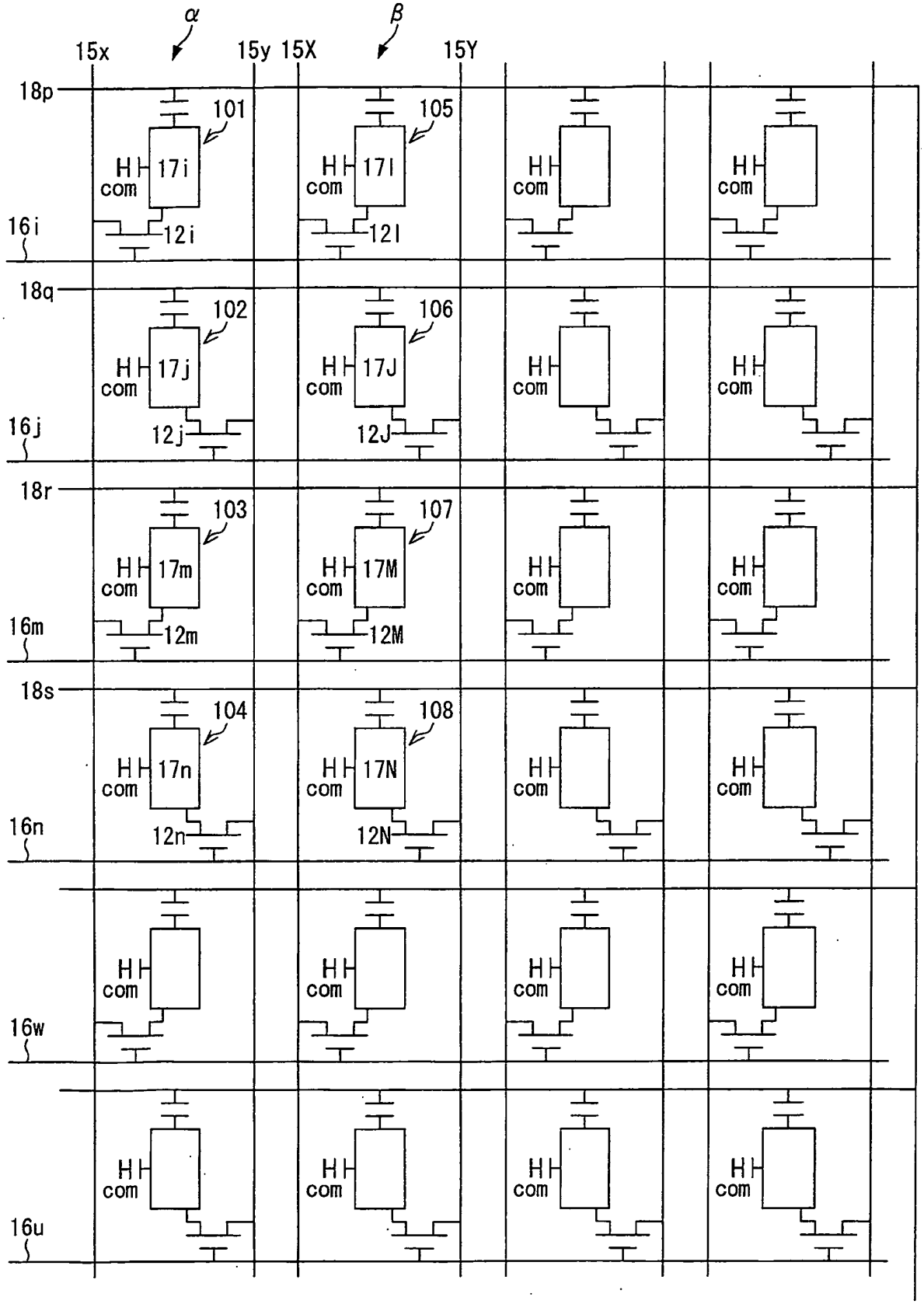

α
β
15x
15y
15X
15Y
18p
18q
18r
18s
16i
16j
16m
16n
16w
16u
101
102
103
104
105
106
107
108
17i
17j
17m
17n
17l
17J
17M
17N
12i
12j
12m
12n
12l
12J
12M
12N
com

FIG. 11

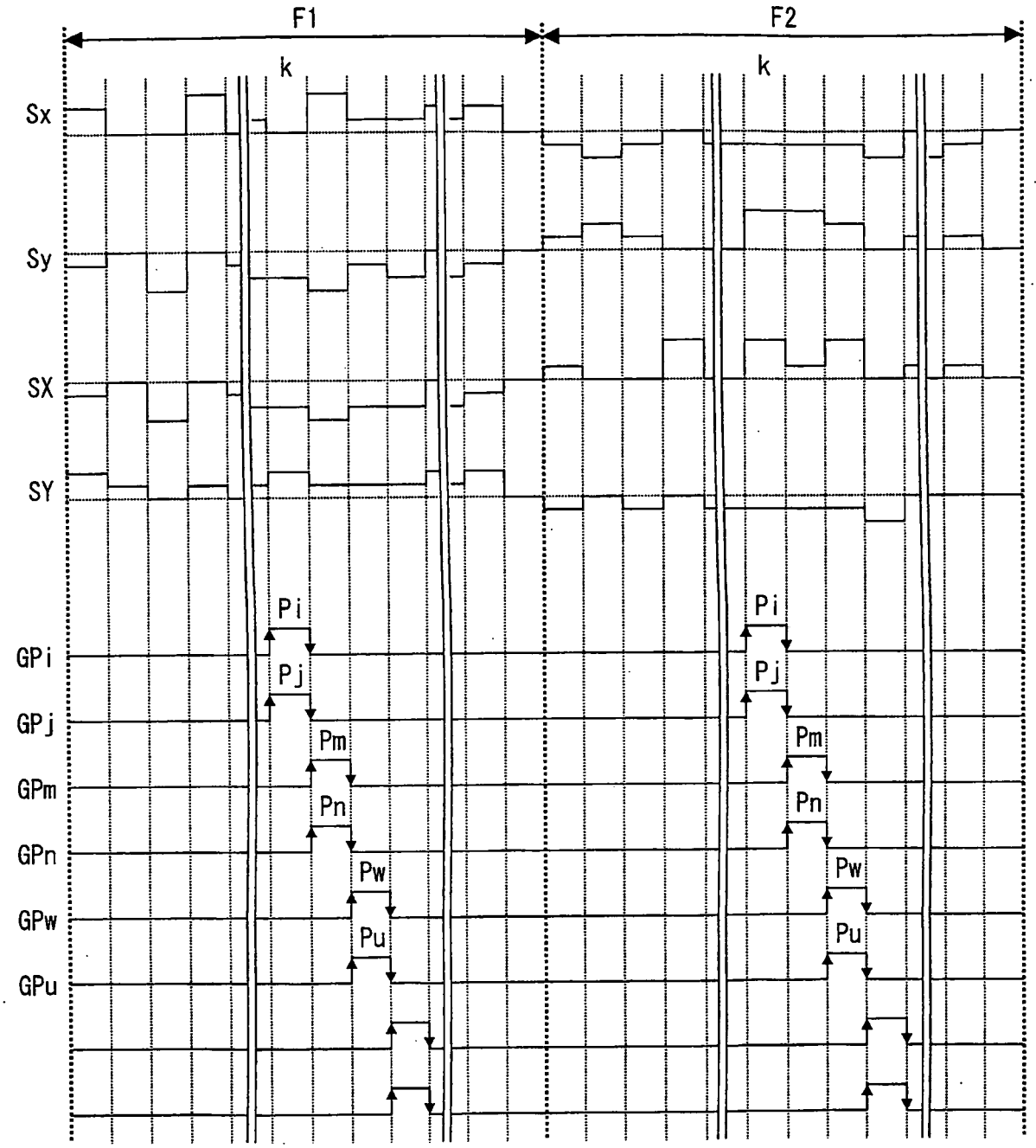

F1
F2
k
k
Sx
Sy
SX
SY
GPi
GPj
GPm
GPn
GPw
GPu
Pi
Pj
Pm
Pn
Pw
Pu
Pi
Pj
Pm
Pn
Pw
Pu

FIG. 12

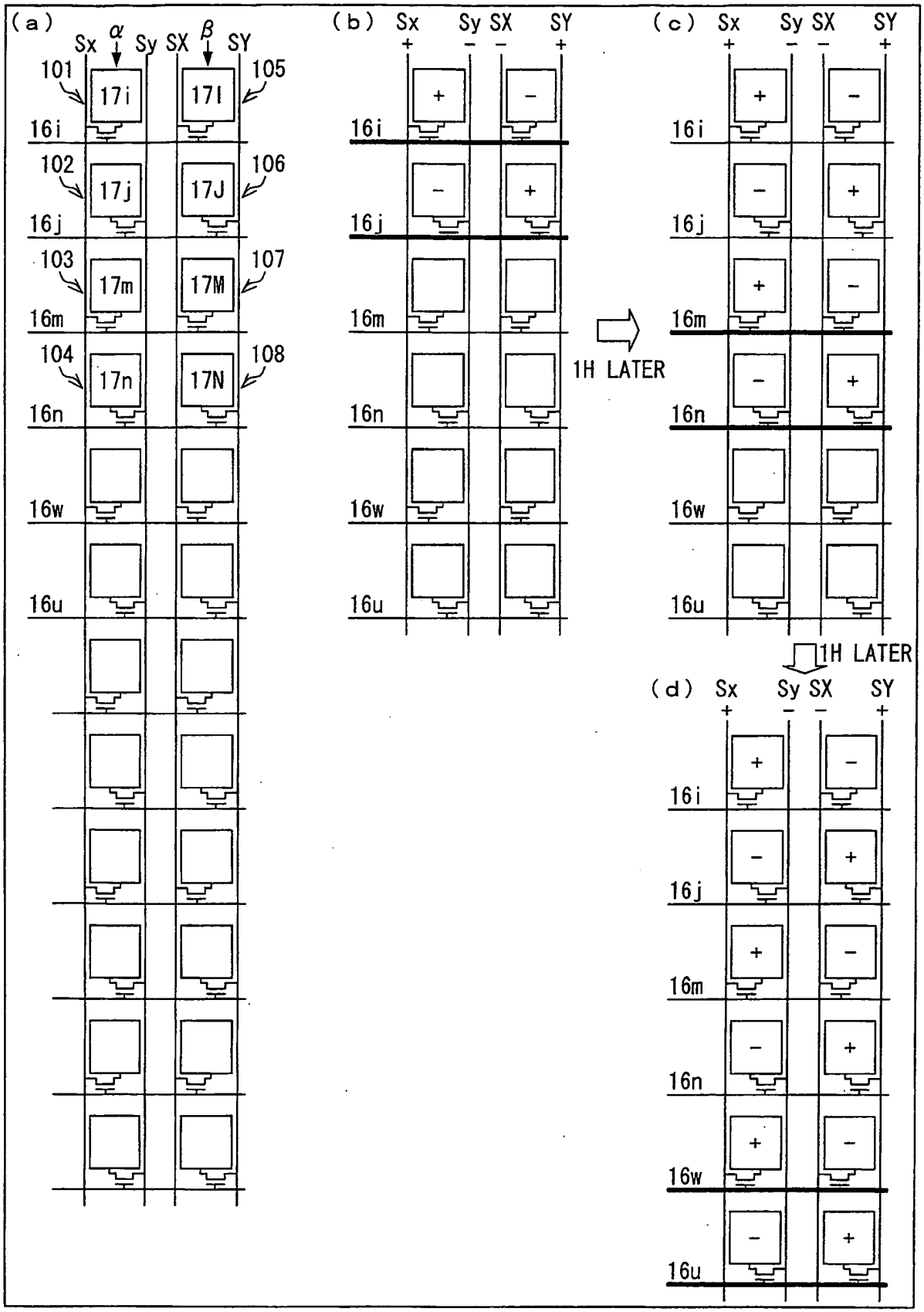

(a)
Sx
α
Sy
SX
β
SY
101
17i
105
16i
102
17j
106
16j
103
17m
107
16m
104
17n
108
16n
16w
16u
(b)
Sx
Sy
SX
SY
16i
16j
16m
16n
16w
16u
1H LATER
(c)
Sx
Sy
SX
SY
16i
16j
16m
16n
16w
16u
1H LATER
(d)
Sx
Sy
SX
SY
16i
16j
16m
16n
16w
16u

FIG. 13

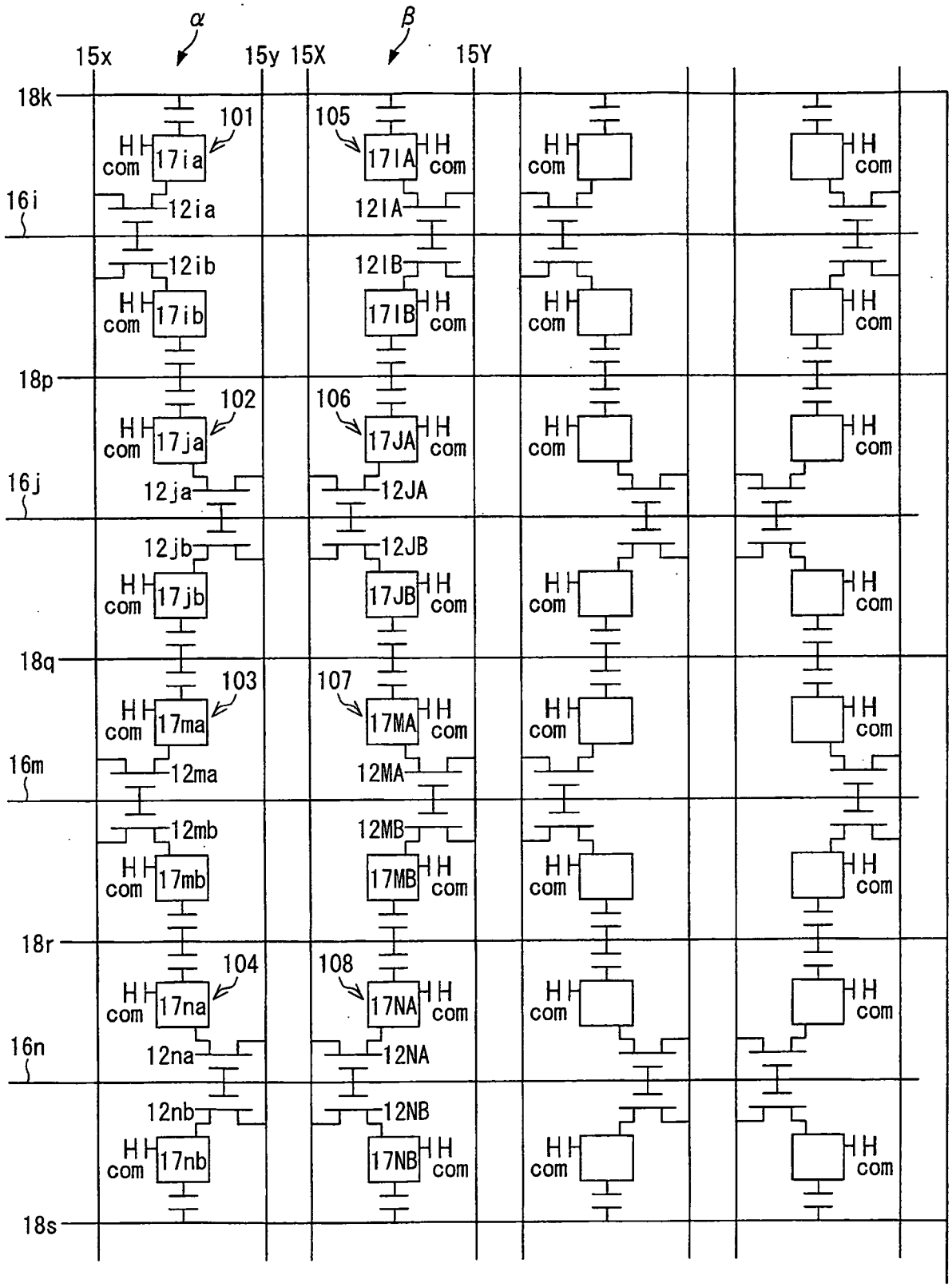

α
β
15x
15y
15X
15Y
18k
18p
18q
18r
18s
16i
16j
16m
16n
101
102
103
104
105
106
107
108
17ia
17ib
17ja
17jb
17ma
17mb
17na
17nb
17IA
17IB
17JA
17JB
17MA
17MB
17NA
17NB
12ia
12ib
12ja
12jb
12ma
12mb
12na
12nb
12IA
12IB
12JA
12JB
12MA
12MB
12NA
12NB
com

FIG. 14

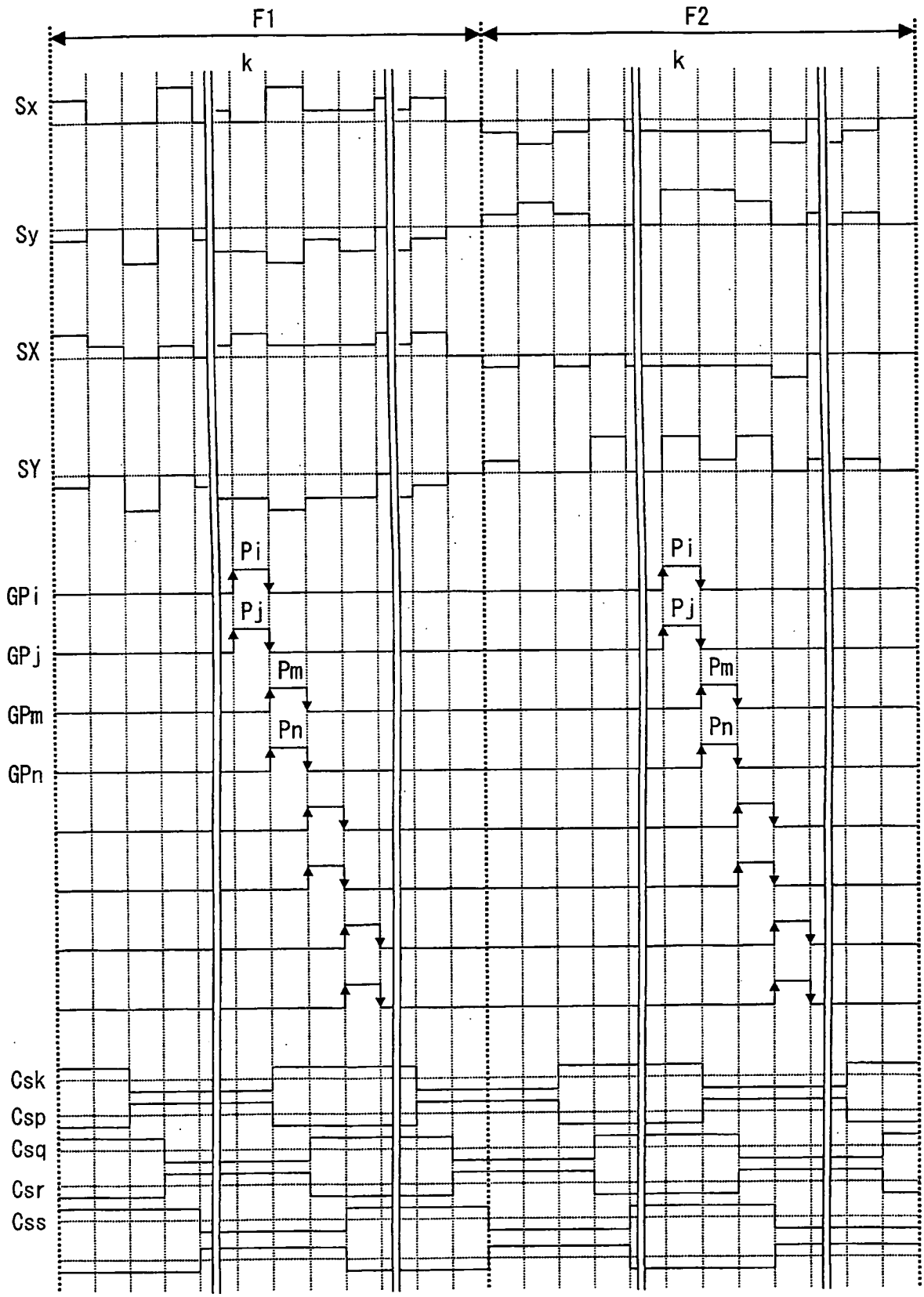


FIG. 15

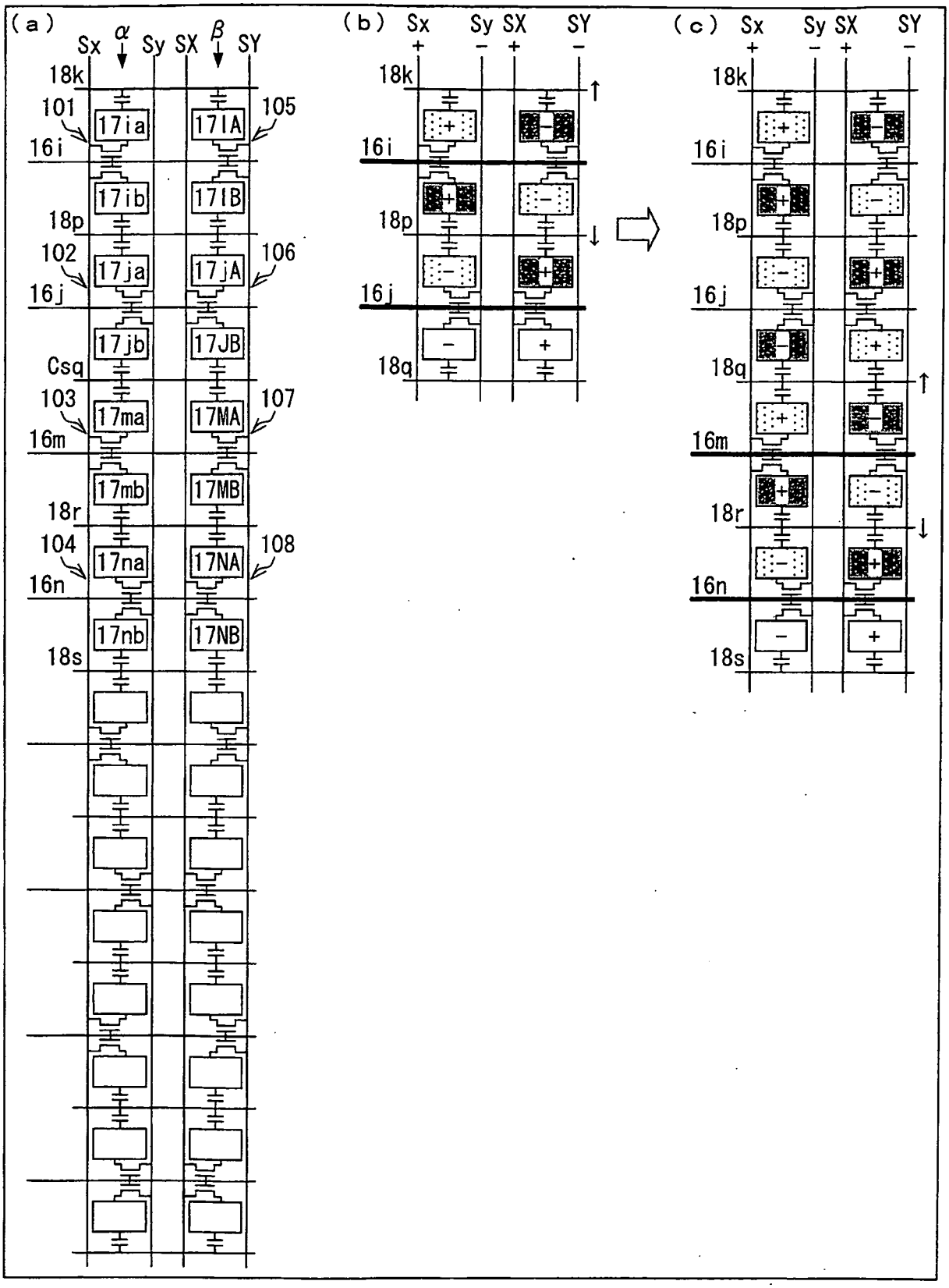

(a)
Sx
α
Sy
SX
β
SY
18k
101
105
16i
17ia
17IA
17ib
17IB
18p
102
106
16j
17ja
17jA
17jb
17JB
Csq
103
107
16m
17ma
17MA
17mb
17MB
18r
104
108
16n
17na
17NA
17nb
17NB
18s
(b)
Sx
Sy
SX
SY
18k
16i
18p
16j
18q
(c)
Sx
Sy
SX
SY
18k
16i
18p
16j
18q
16m
18r
16n
18s

FIG. 16

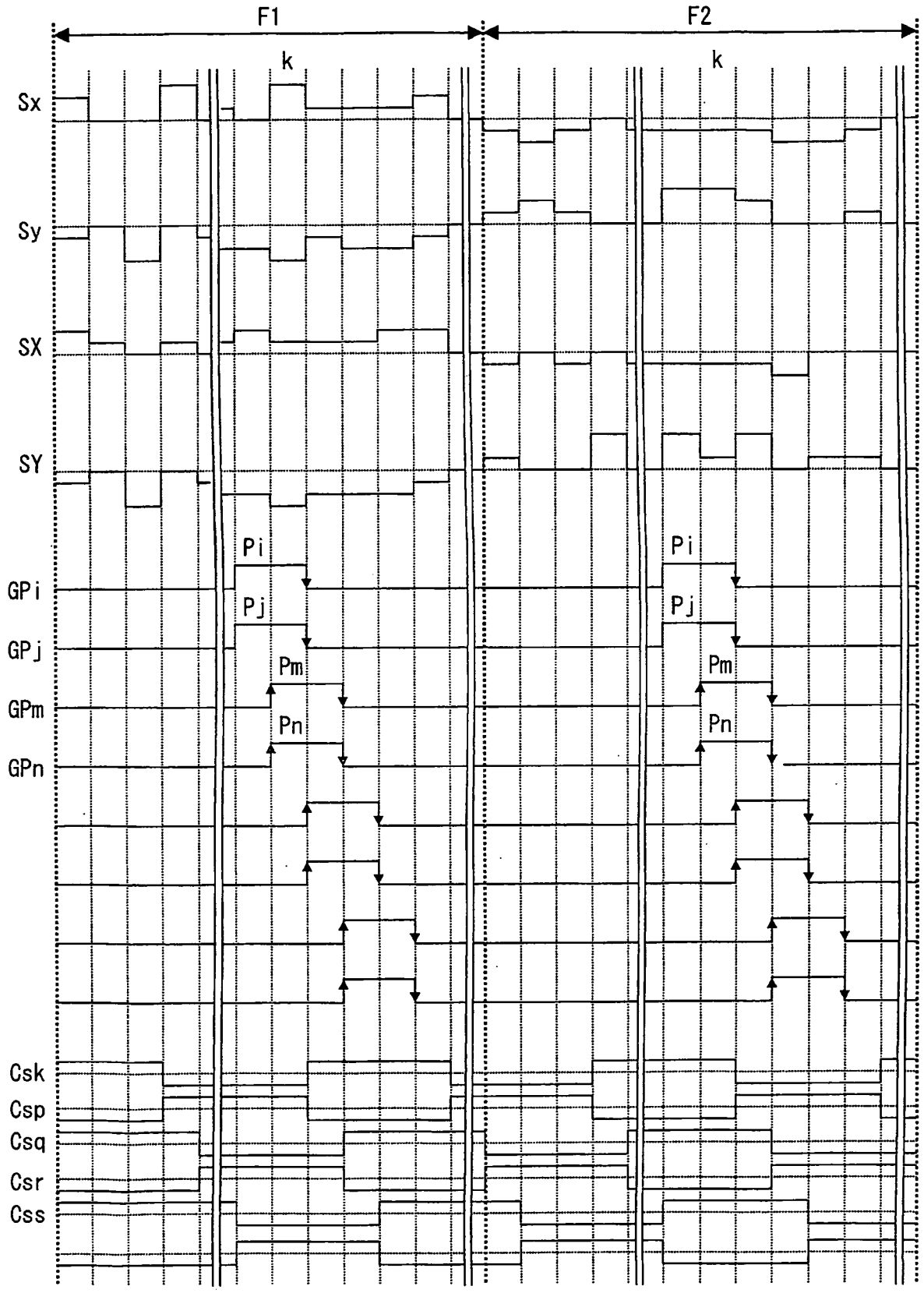

F1
F2
k
k
Sx
Sy
SX
SY
Pi
Pi
GPi
Pj
Pj
GPj
Pm
Pm
GPm
Pn
Pn
GPn
Csk
Csp
Csq
Csr
Css

FIG. 17

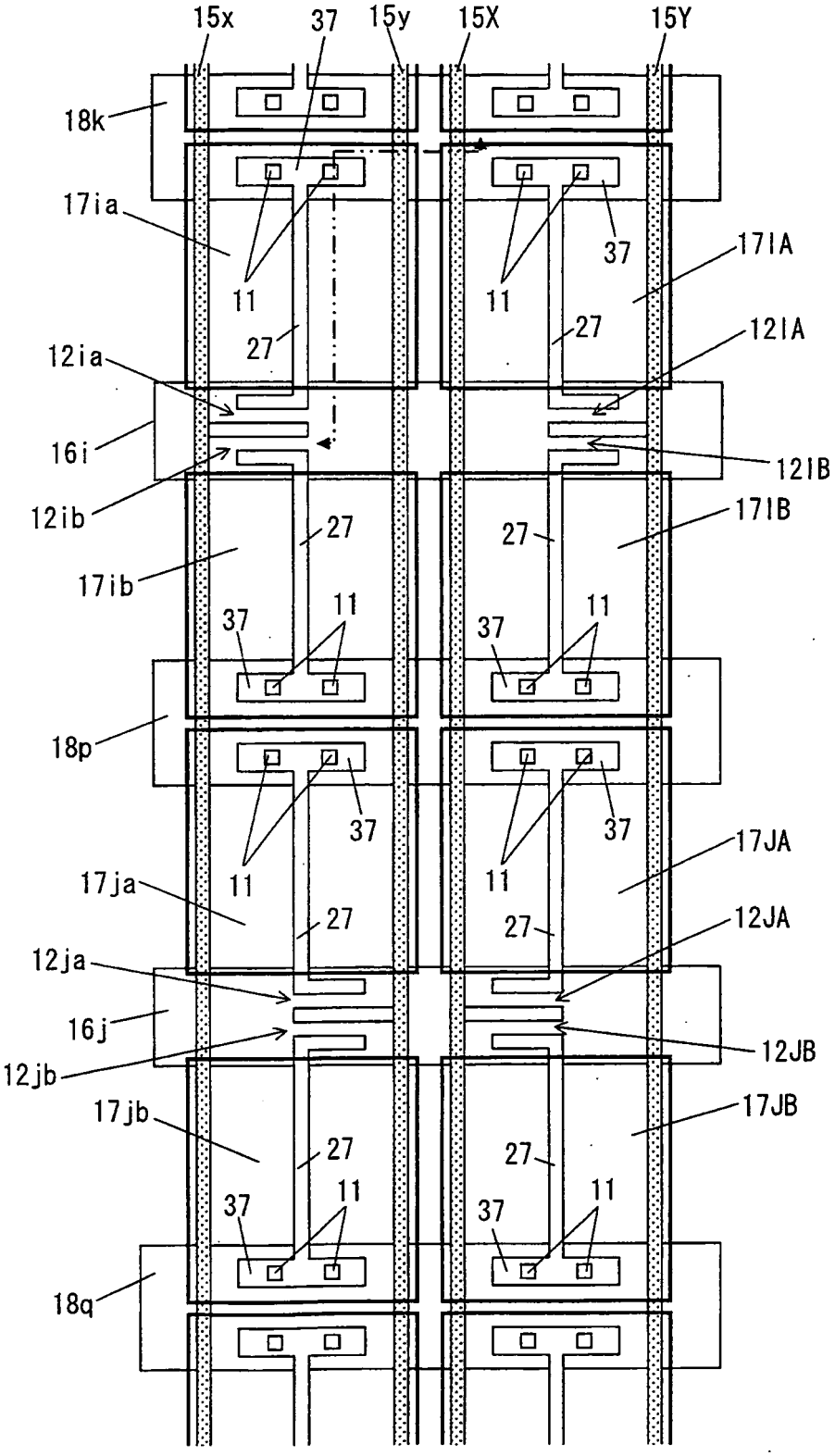

15x
37
15y
15X
15Y
18k
17ia
11
27
37
17IA
12ia
12IA
16i
12IB
12ib
27
17IB
17ib
37
11
18p
17JA
17ja
12JA
12ja
16j
12JB
12jb
17JB
17jb
18q

FIG. 18

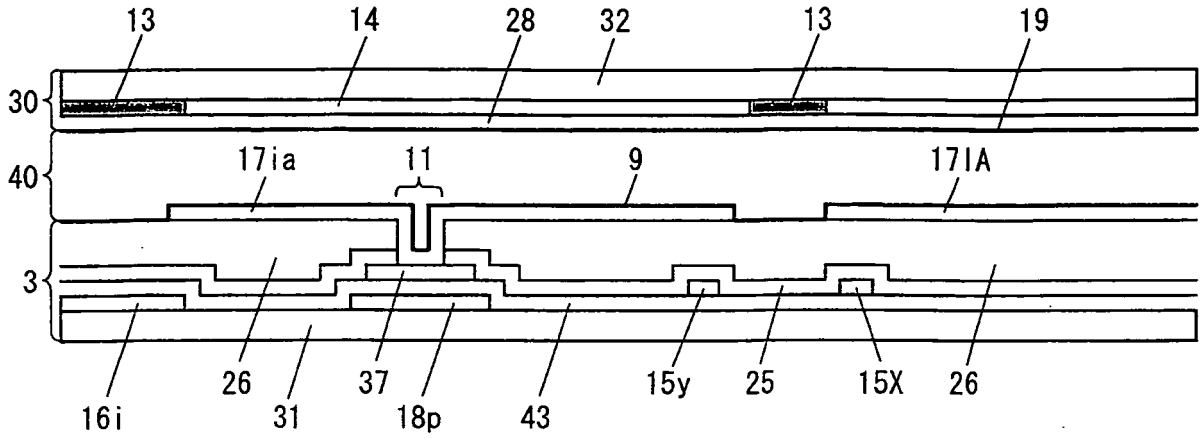

13
14
28
32
13
19
30
40
17ia
11
9
17IA
3
16i
26
31
37
18p
43
15y
25
15X
26

FIG. 19

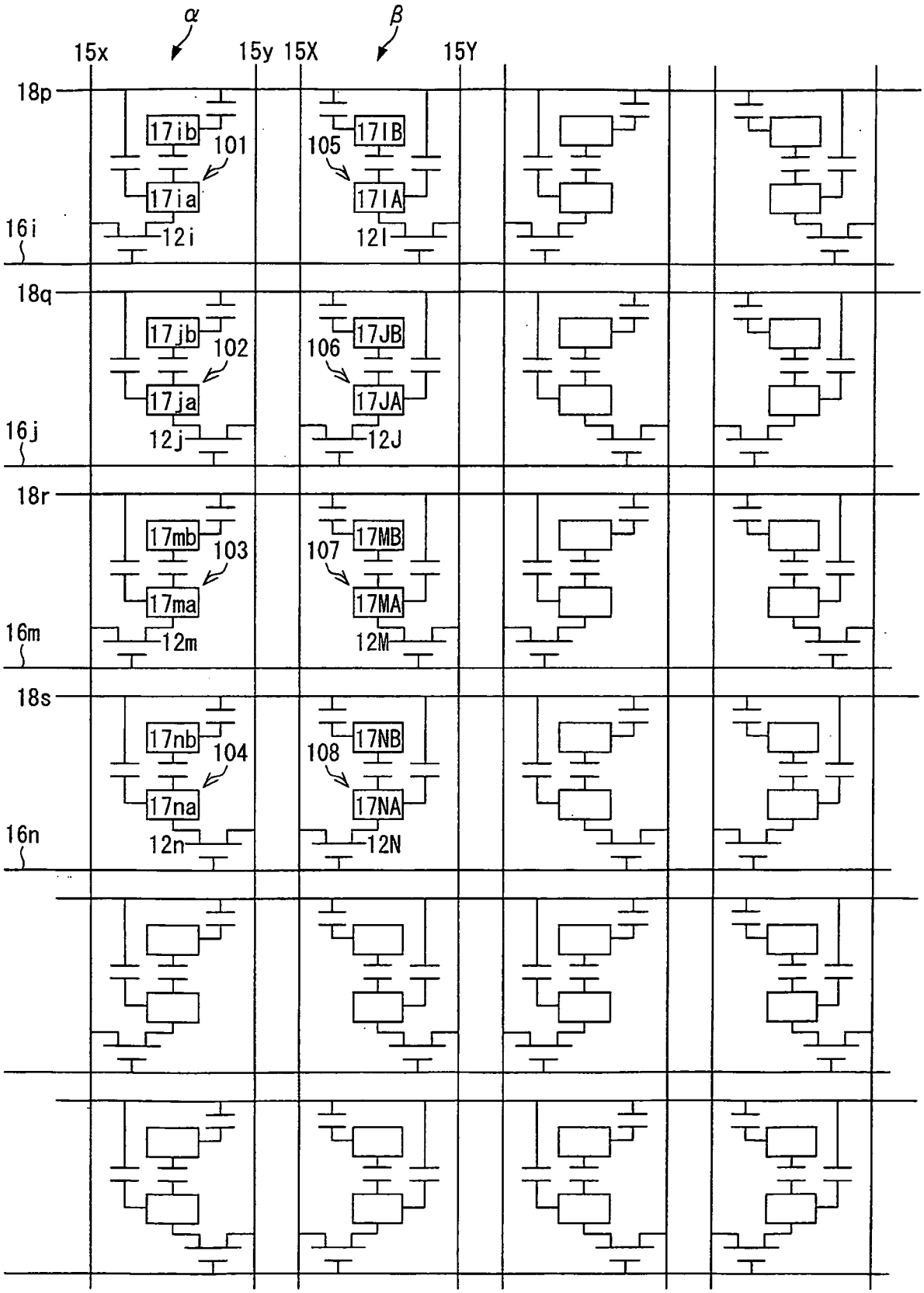

α
β
15x
15y
15X
15Y
18p
18q
18r
18s
16i
16j
16m
16n
17ib
101
17ia
12i
17IB
105
17IA
12I
17jb
102
17ja
12j
17JB
106
17JA
12J
17mb
103
17ma
12m
17MB
107
17MA
12M
17nb
104
17na
12n
17NB
108
17NA
12N

FIG. 20

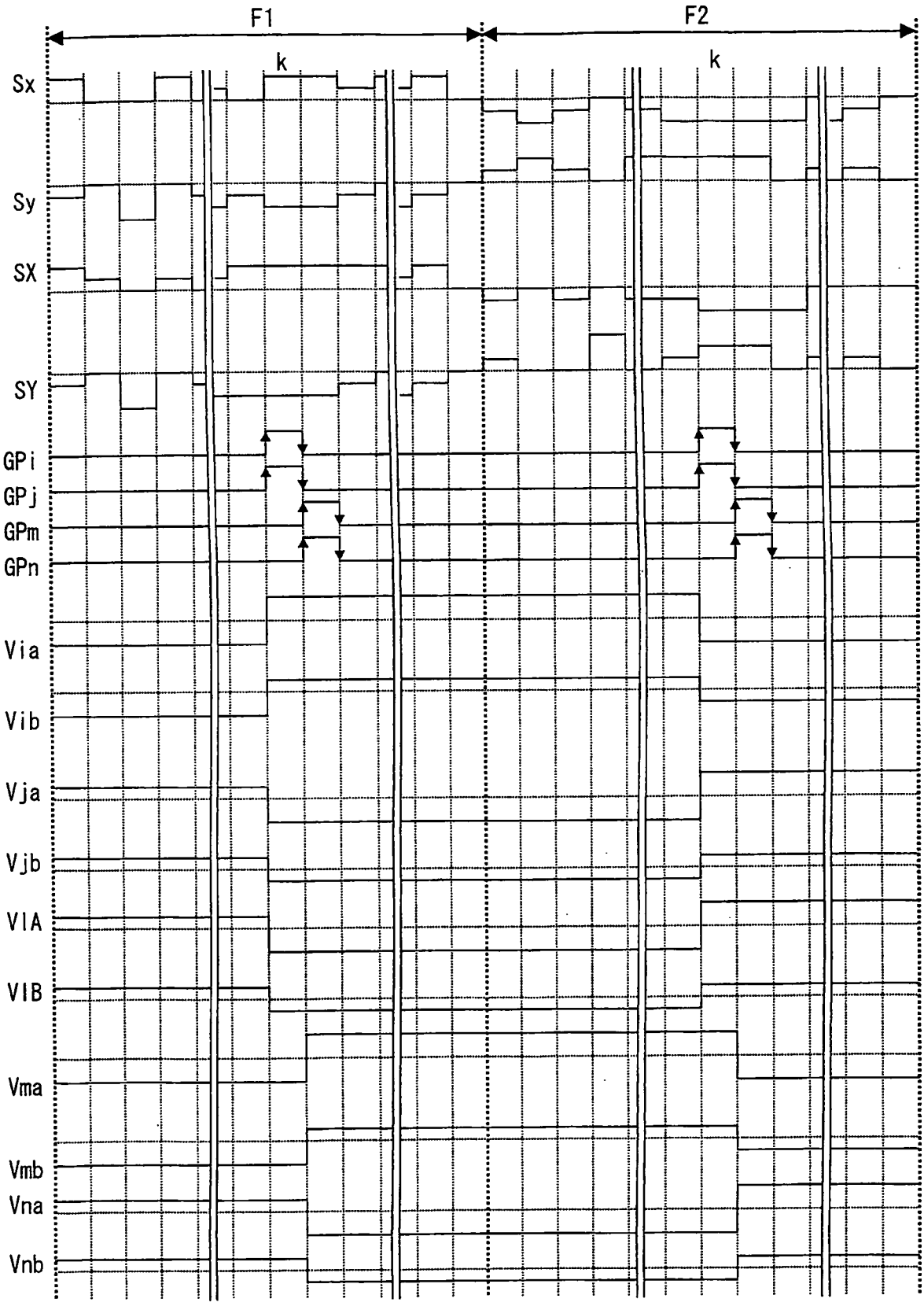

F1
F2
k
k
Sx
Sy
SX
SY
GPi
GPj
GPm
GPn
Via
Vib
Vja
Vjb
VIA
VIB
Vma
Vmb
Vna
Vnb

FIG. 21

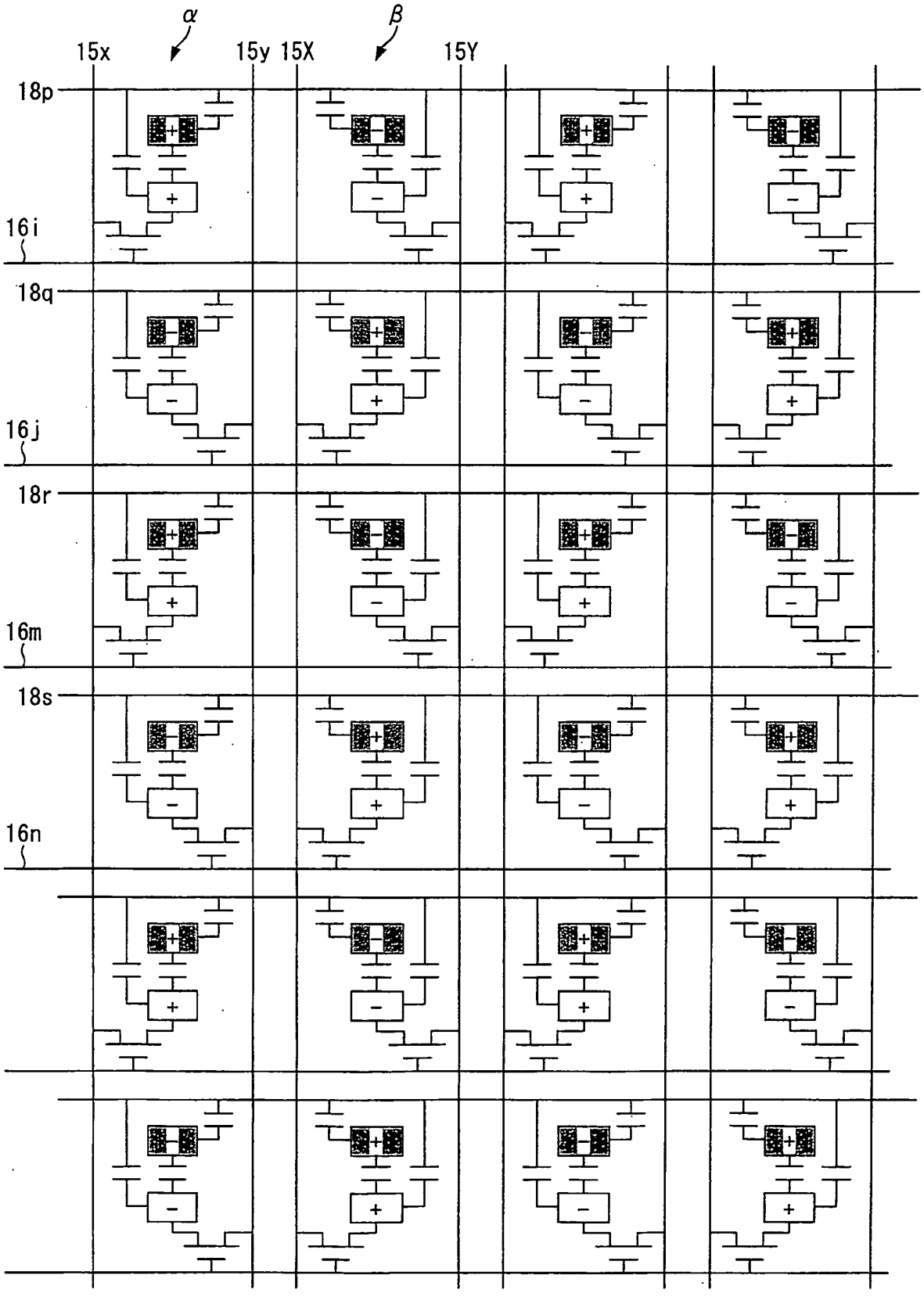


FIG. 22

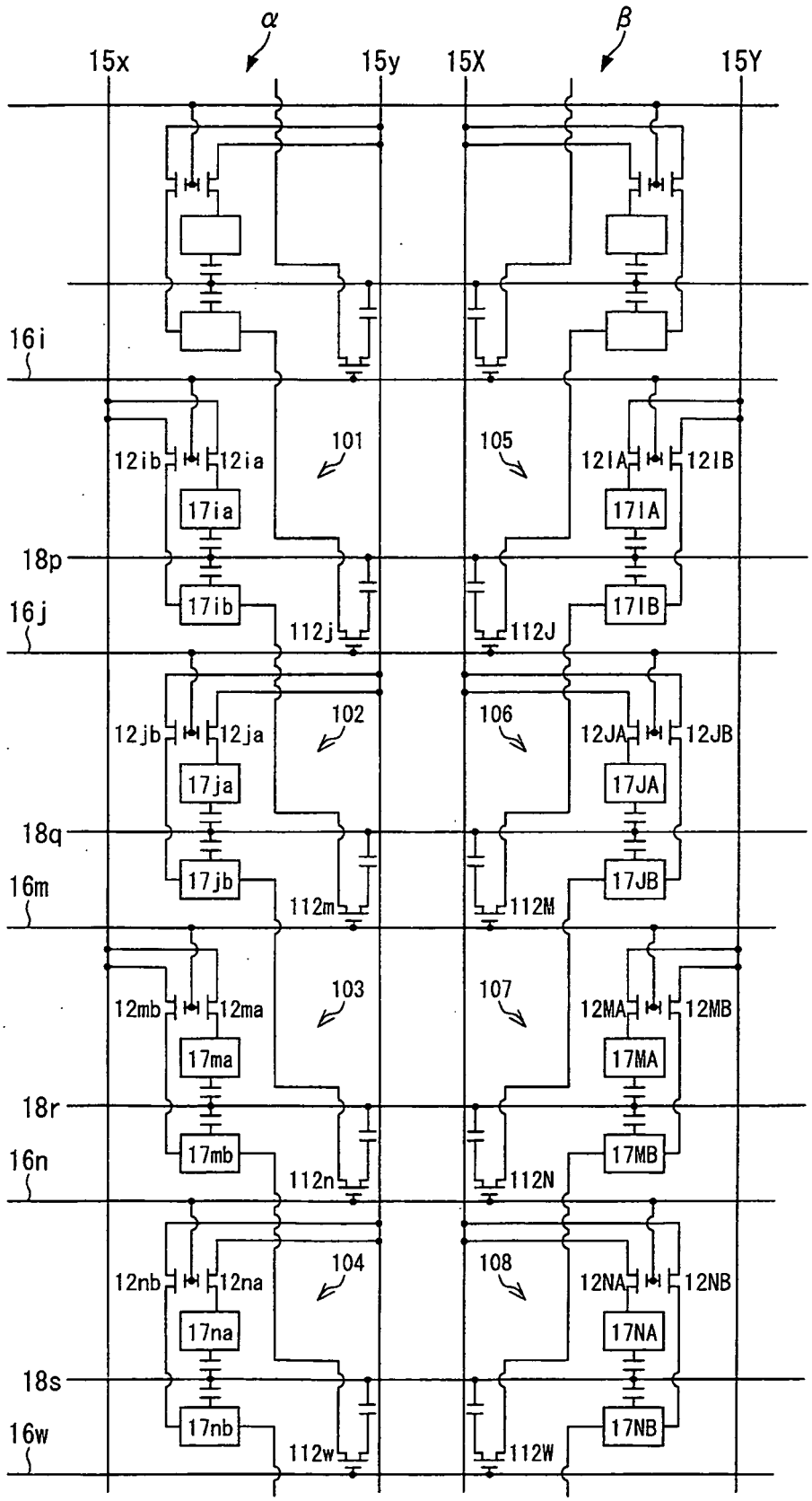

α
β
15x
15y
15X
15Y
16i
16j
16m
16n
16w
18p
18q
18r
18s
12ib
12ia
12jb
12ja
12mb
12ma
12nb
12na
12IA
12IB
12JA
12JB
12MA
12MB
12NA
12NB
17ia
17ib
17ja
17jb
17ma
17mb
17na
17nb
17IA
17IB
17JA
17JB
17MA
17MB
17NA
17NB
101
102
103
104
105
106
107
108
112j
112m
112n
112w
112J
112M
112N
112W

FIG. 23

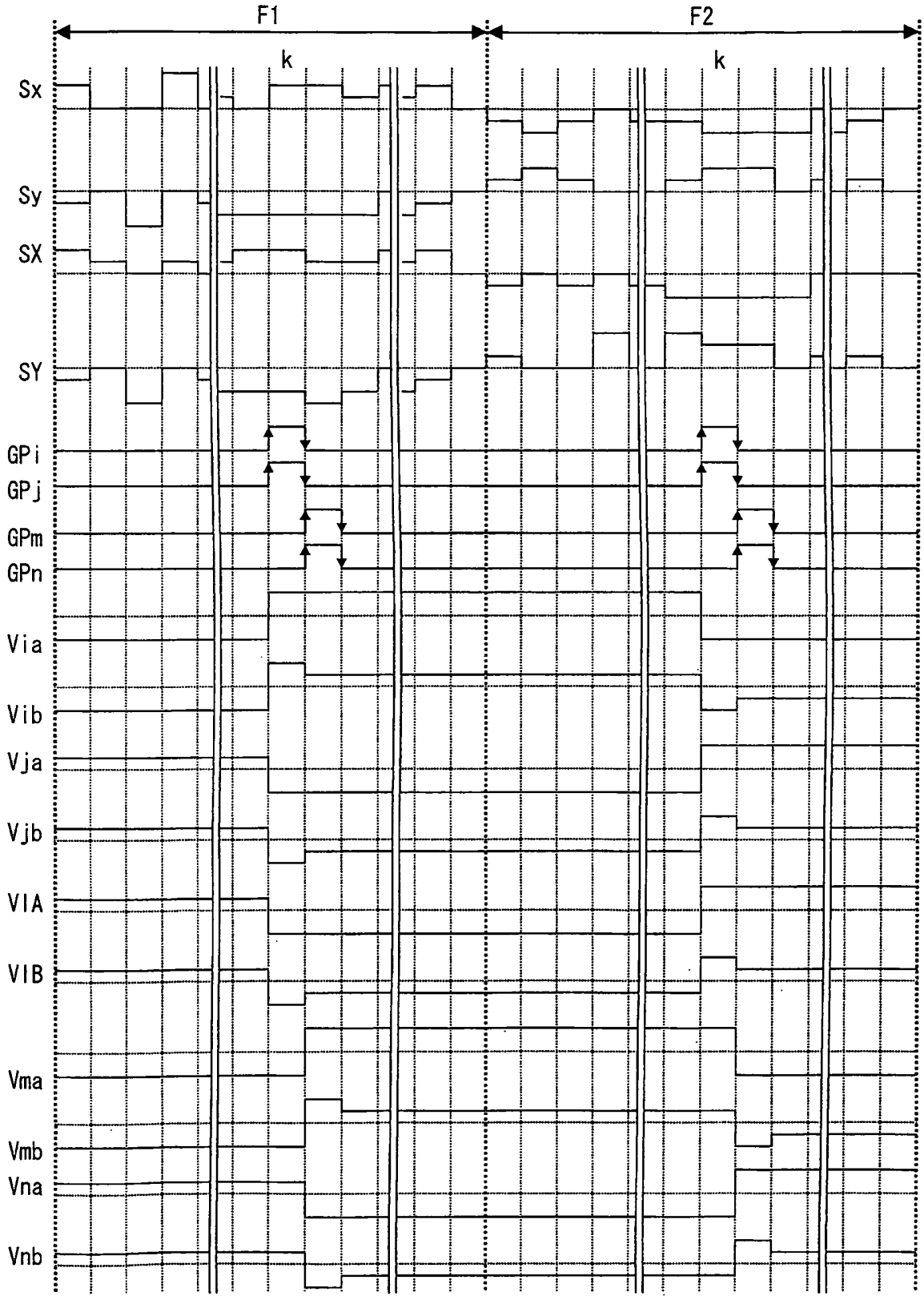

F1
F2
k
k
Sx
Sy
SX
SY
GPi
GPj
GPm
GPn
Via
Vib
Vja
Vjb
VIA
VIB
Vma
Vmb
Vna
Vnb

FIG. 24

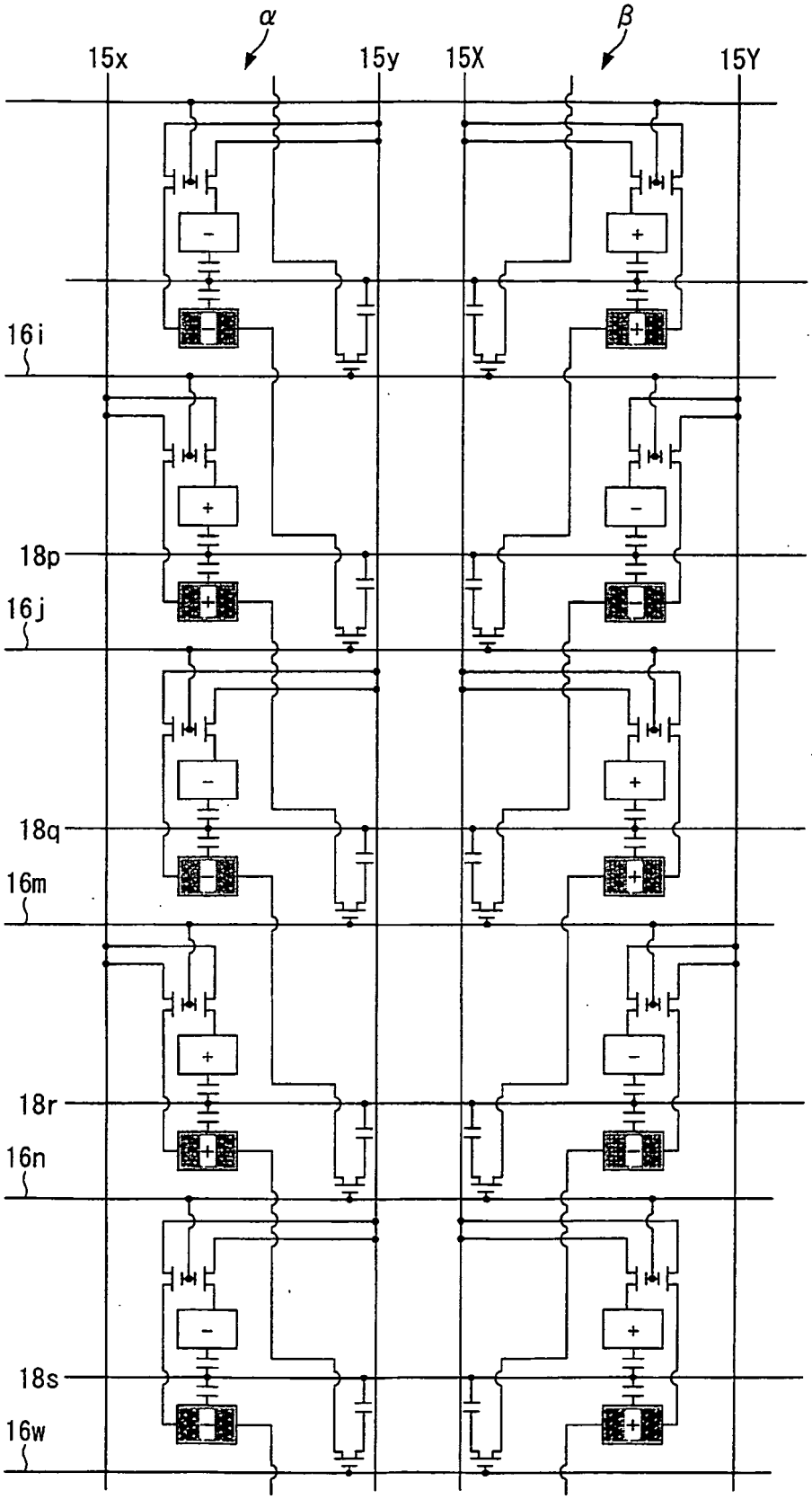


FIG. 25

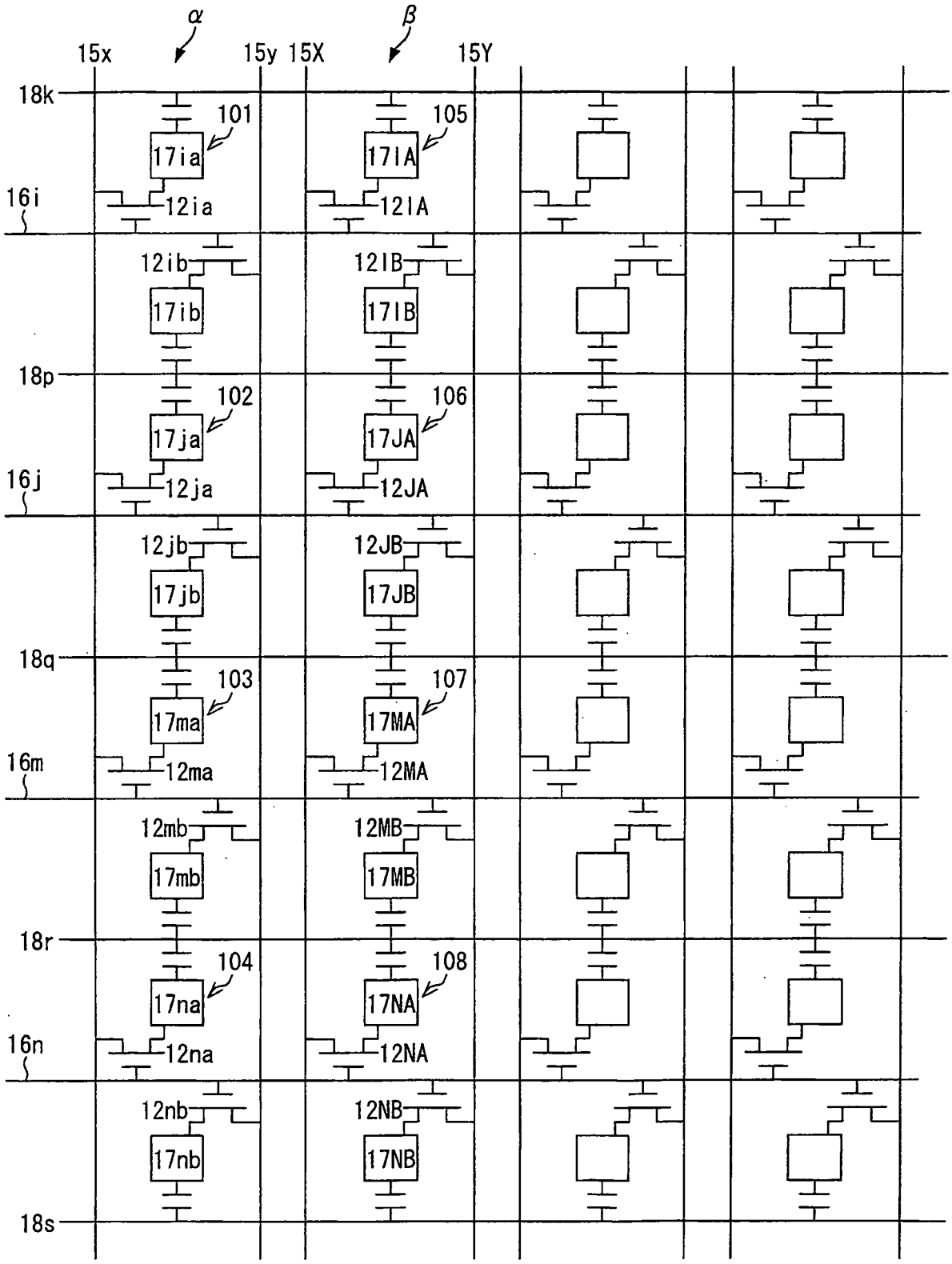

α
β
15x
15y
15X
15Y
18k
18p
18q
18r
18s
16i
16j
16m
16n
101
102
103
104
105
106
107
108
17ia
17ib
17ja
17jb
17ma
17mb
17na
17nb
17IA
17IB
17JA
17JB
17MA
17MB
17NA
17NB
12ia
12ib
12ja
12jb
12ma
12mb
12na
12nb
12IA
12IB
12JA
12JB
12MA
12MB
12NA
12NB

FIG. 26

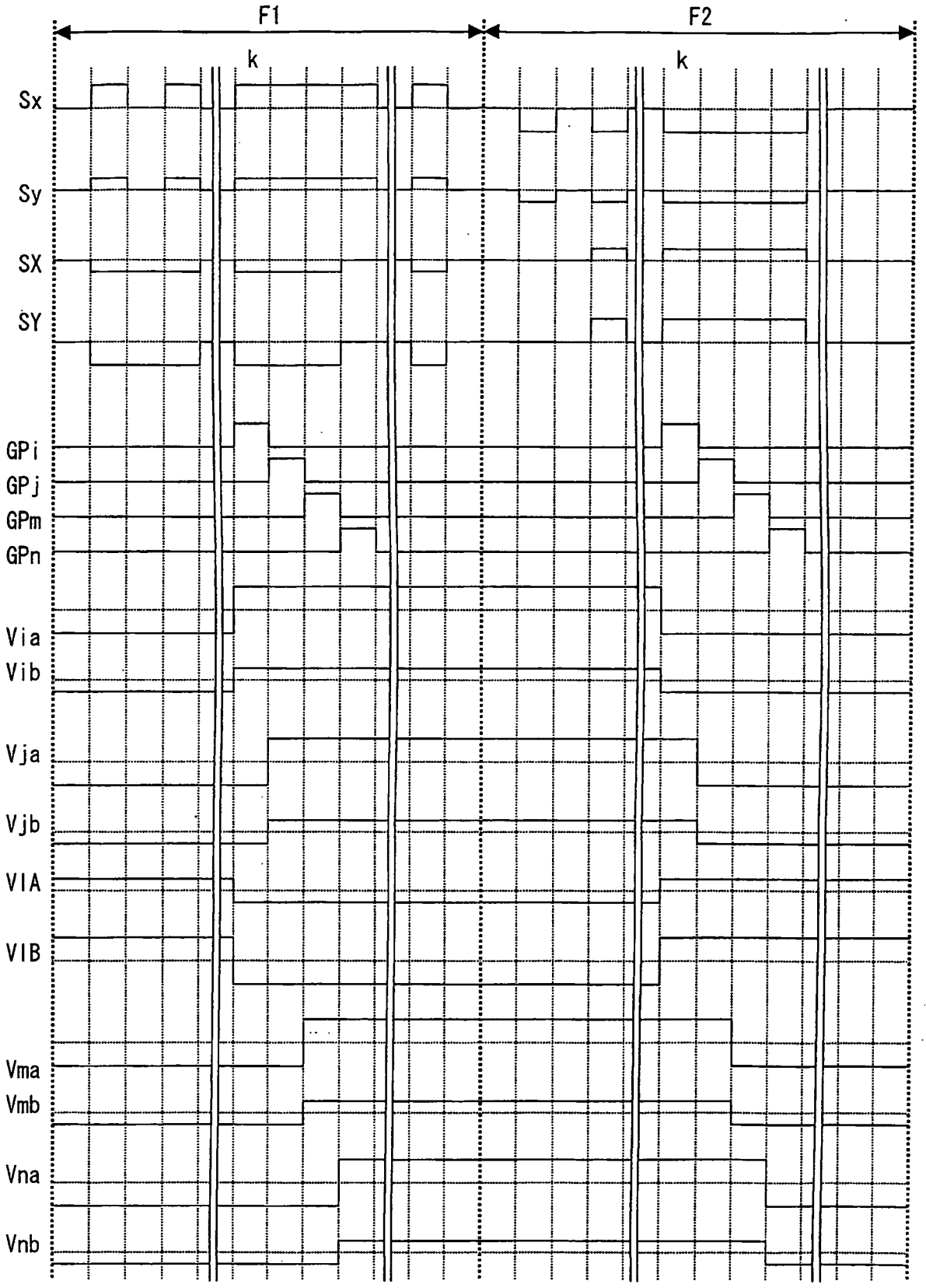

F1
F2
k
k
Sx
Sy
SX
SY
GPi
GPj
GPm
GPn
Via
Vib
Vja
Vjb
VIA
VIB
Vma
Vmb
Vna
Vnb

FIG. 27

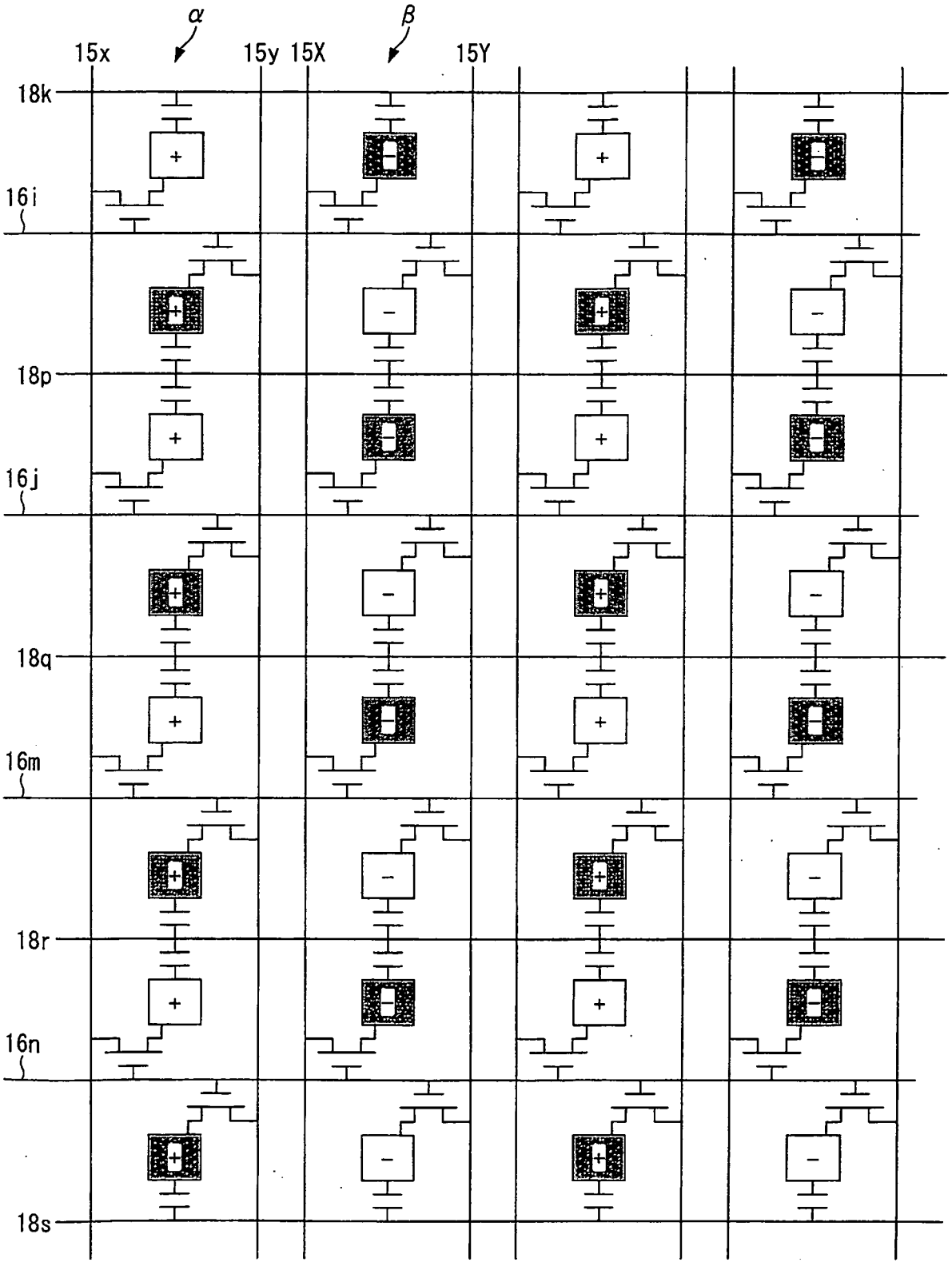


FIG. 28

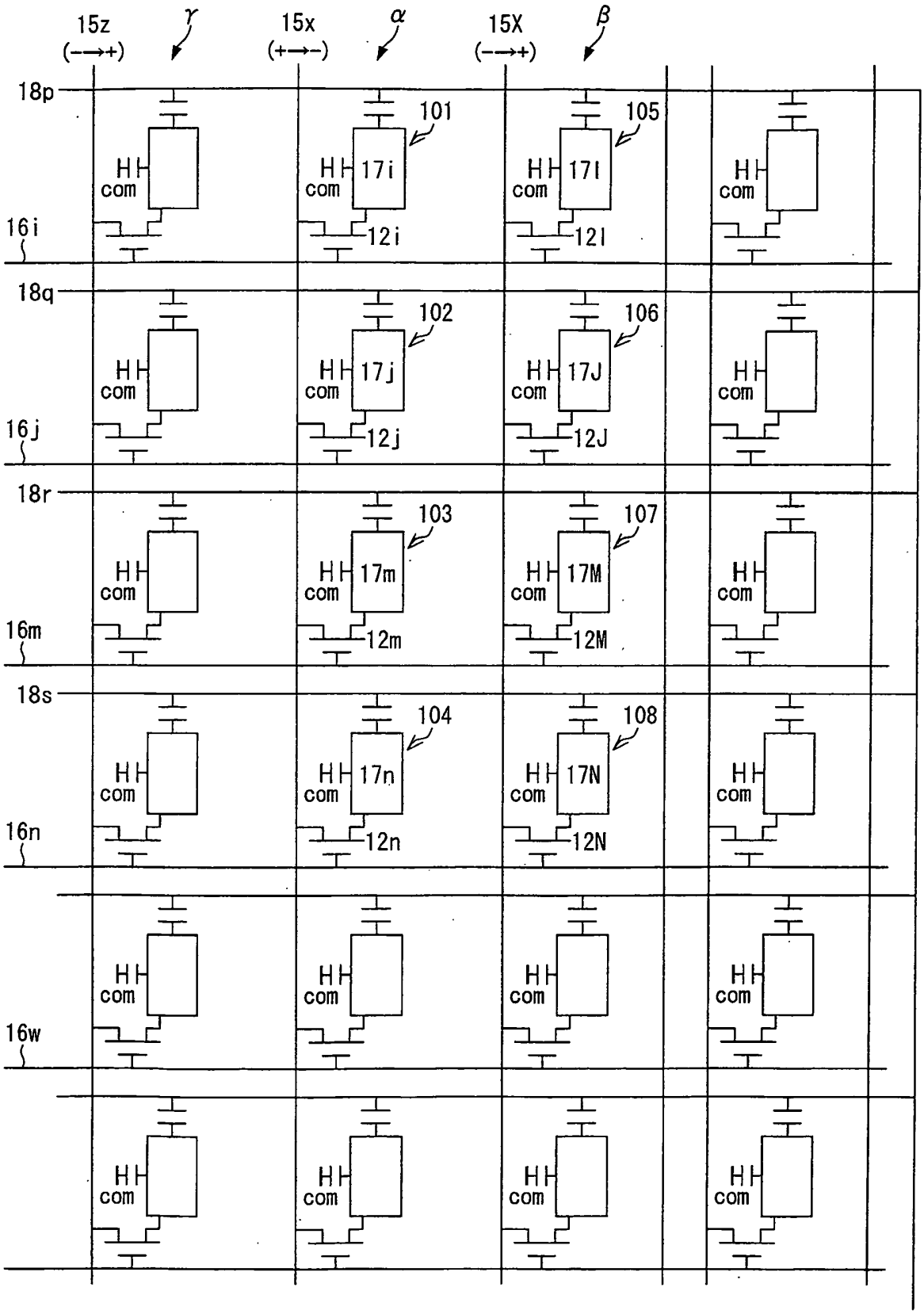

15z
(−→+)
γ
15x
(+→−)
α
15X
(−→+)
β
18p
18q
18r
18s
16i
16j
16m
16n
16w
101
102
103
104
105
106
107
108
17i
17j
17m
17n
17I
17J
17M
17N
12i
12j
12m
12n
12I
12J
12M
12N
com

FIG. 29

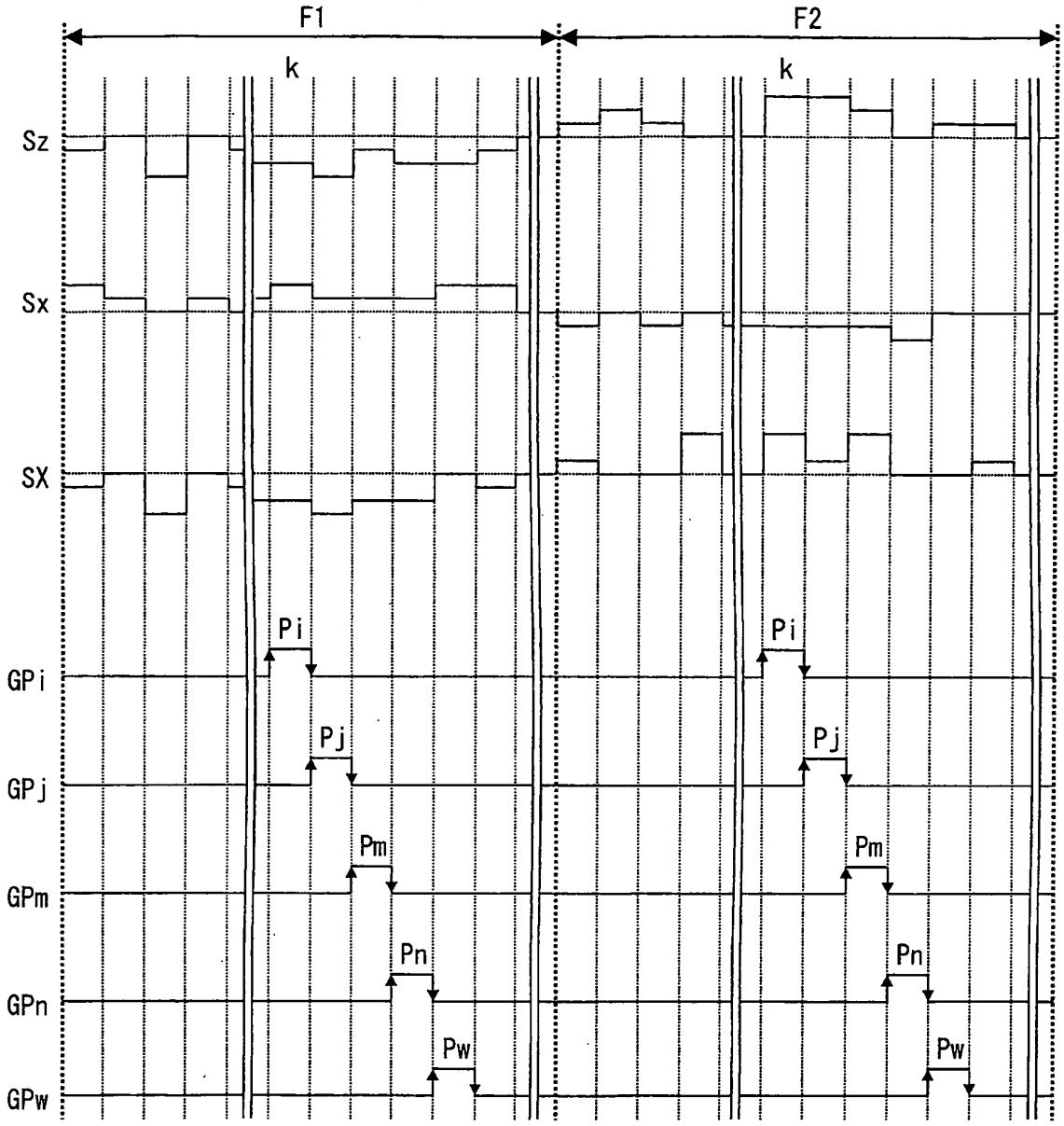


FIG. 30

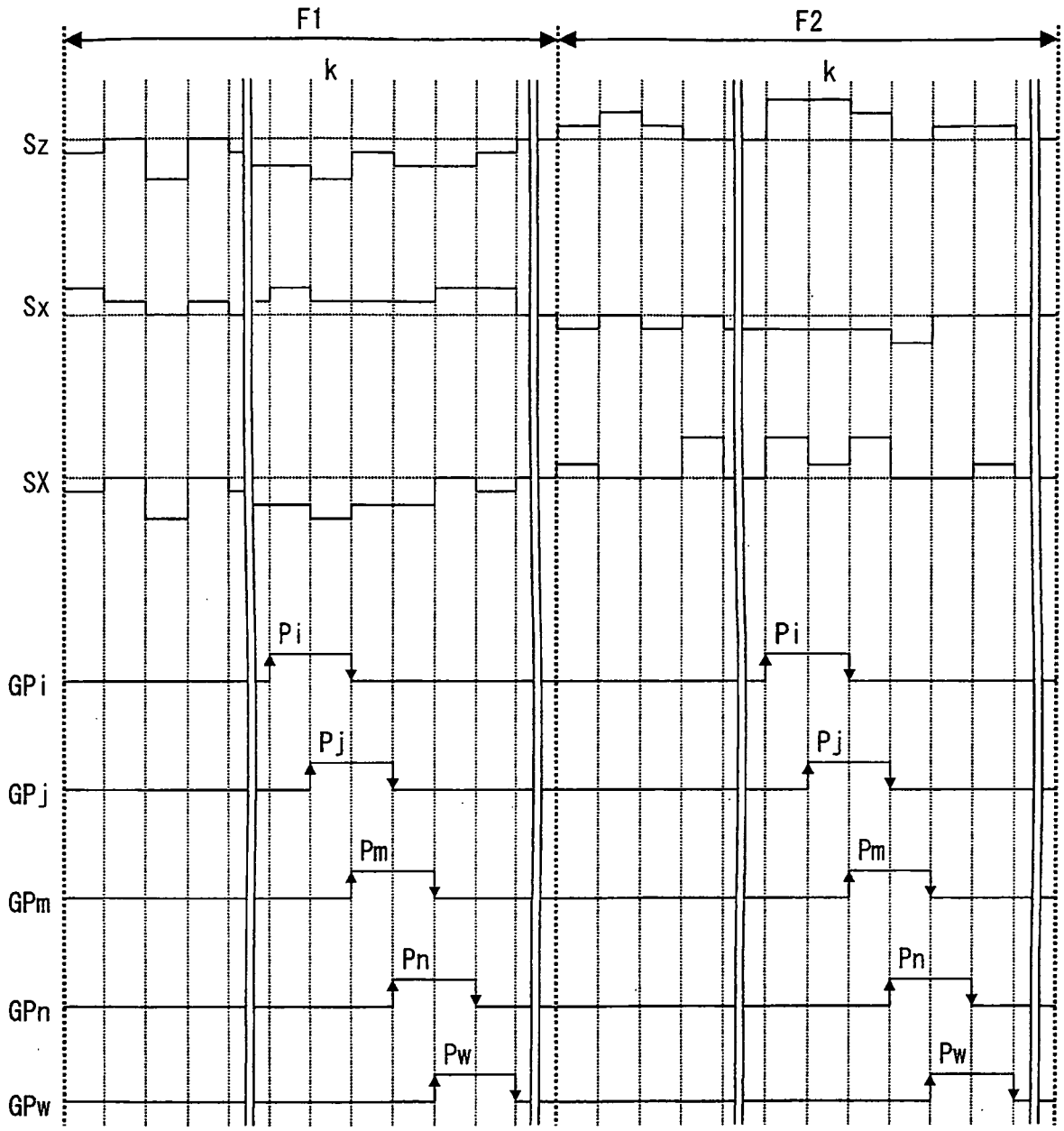


FIG. 31

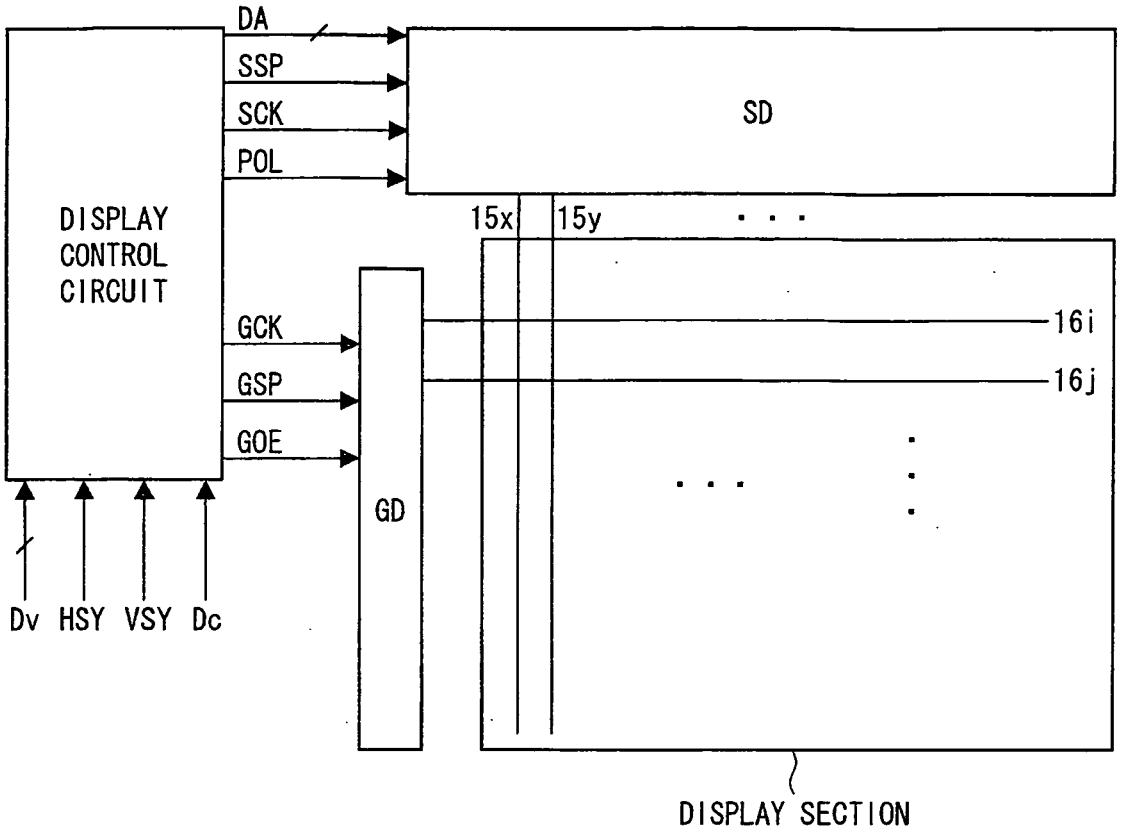

DA
SSP
SCK
POL
SD
DISPLAY
CONTROL
CIRCUIT
15x
15y
GCK
GSP
GOE
GD
16i
16j
Dv
HSY
VSY
Dc
DISPLAY SECTION

FIG. 32

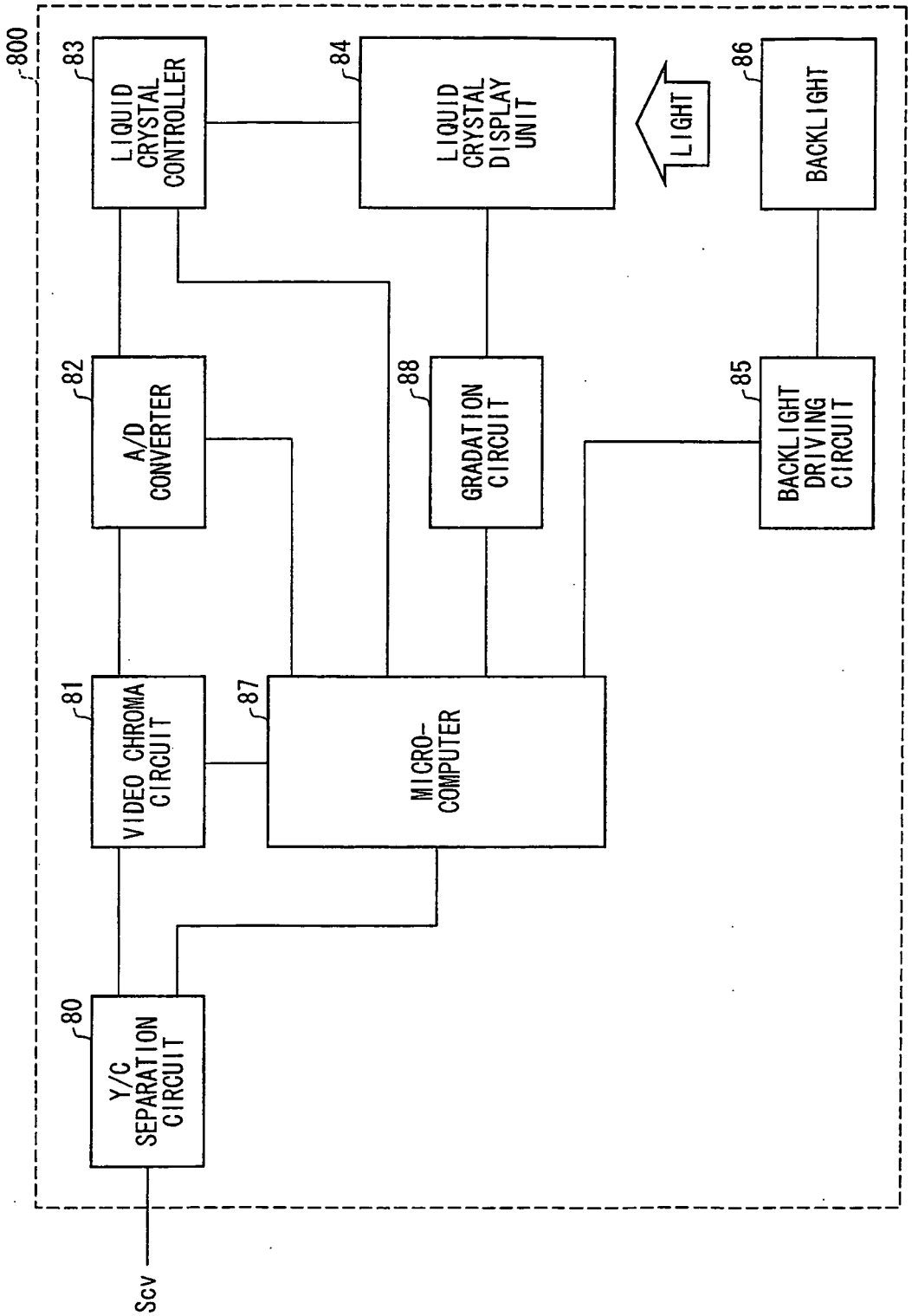

800
83
LIQUID CRYSTAL CONTROLLER
84
LIQUID CRYSTAL DISPLAY UNIT
LIGHT
86
BACKLIGHT
82
A/D CONVERTER
88
GRADATION CIRCUIT
85
BACKLIGHT DRIVING CIRCUIT
81
VIDEO CHROMA CIRCUIT
87
MICRO-COMPUTER
80
Y/C SEPARATION CIRCUIT
Scv

FIG. 33

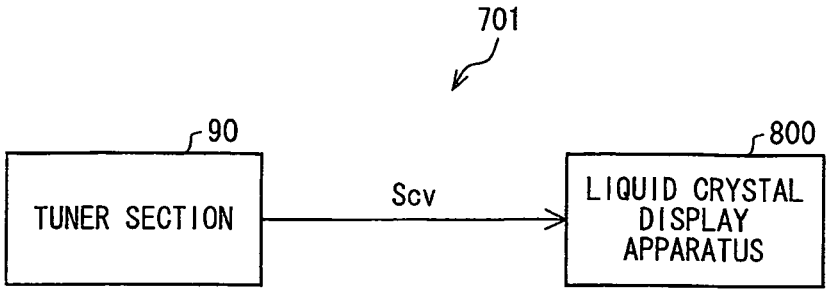

701
90
TUNER SECTION
Scv
800
LIQUID CRYSTAL DISPLAY APPARATUS

FIG. 34

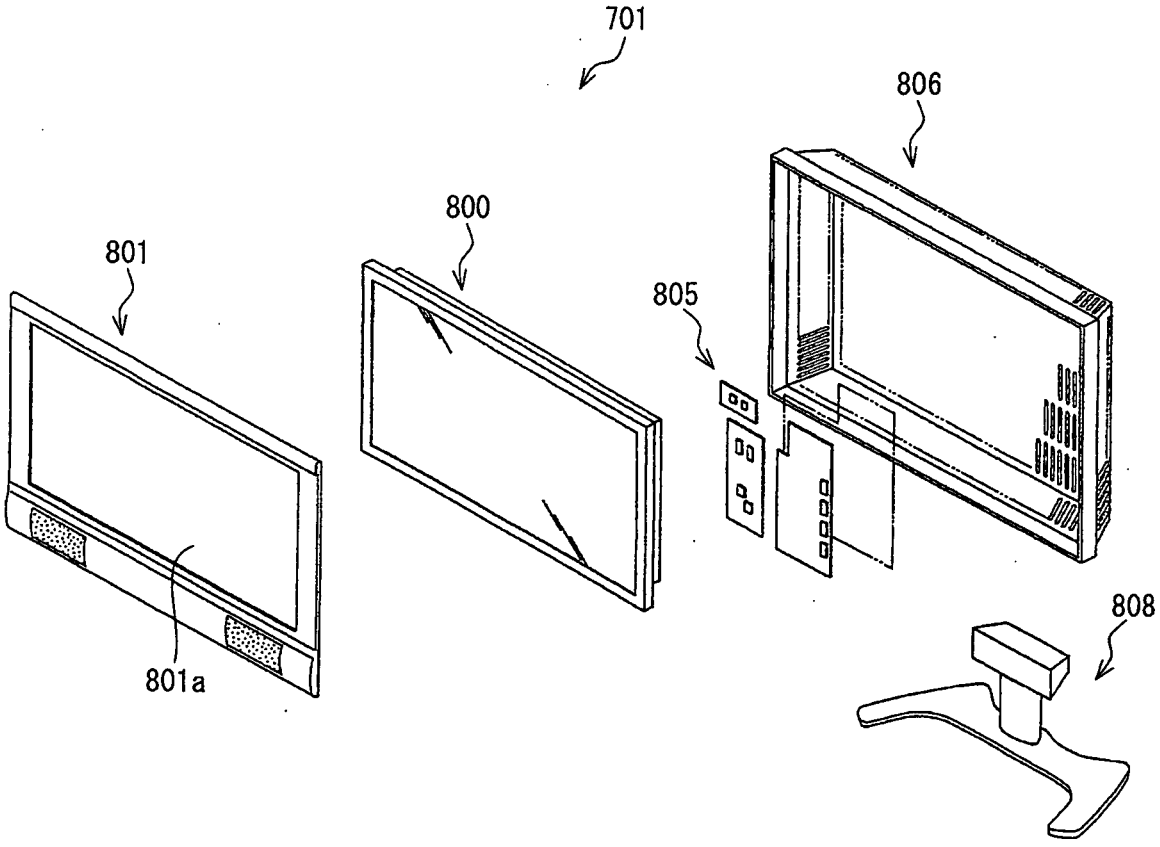

701
806
800
801
805
808
801a

FIG. 35

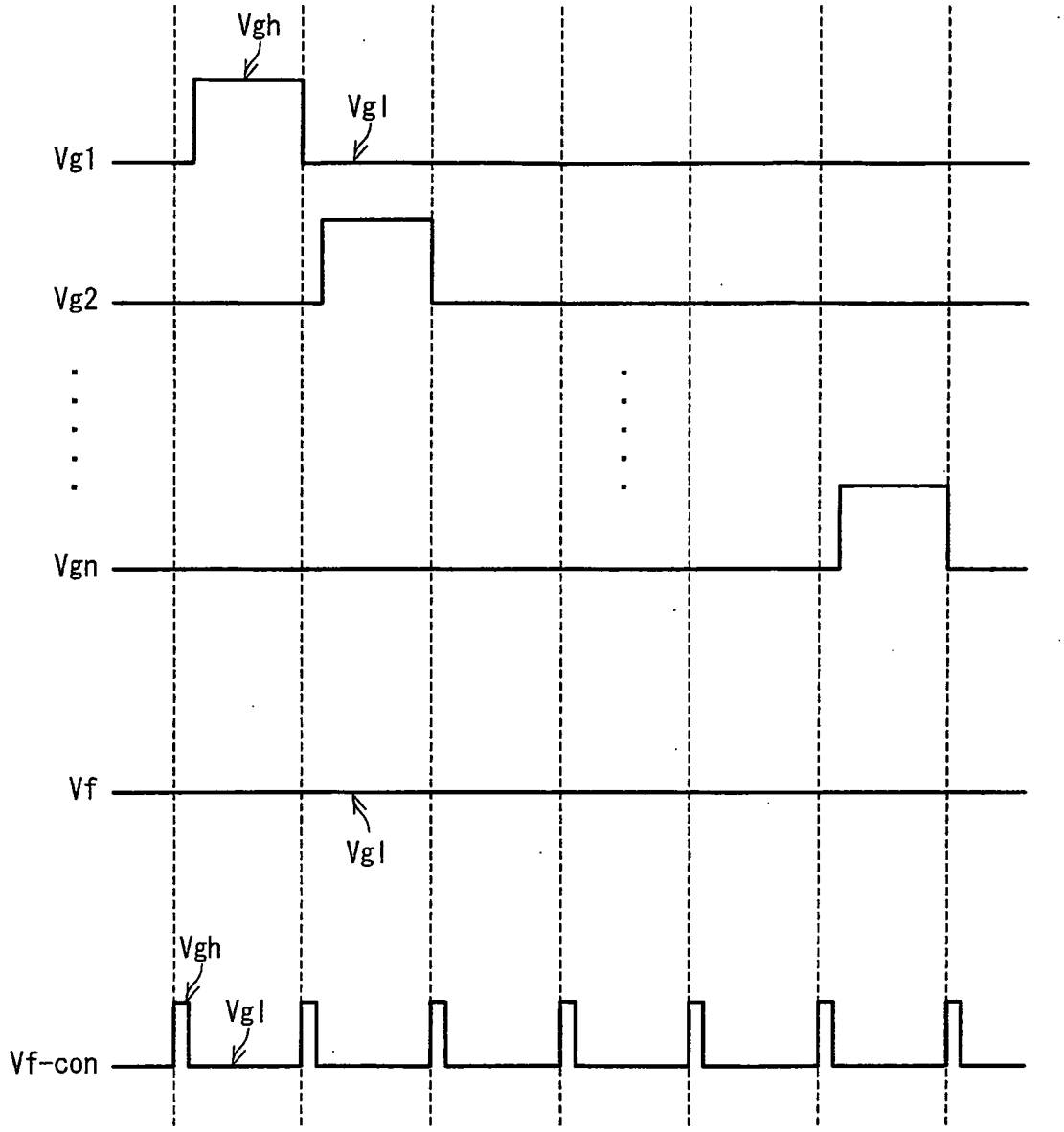
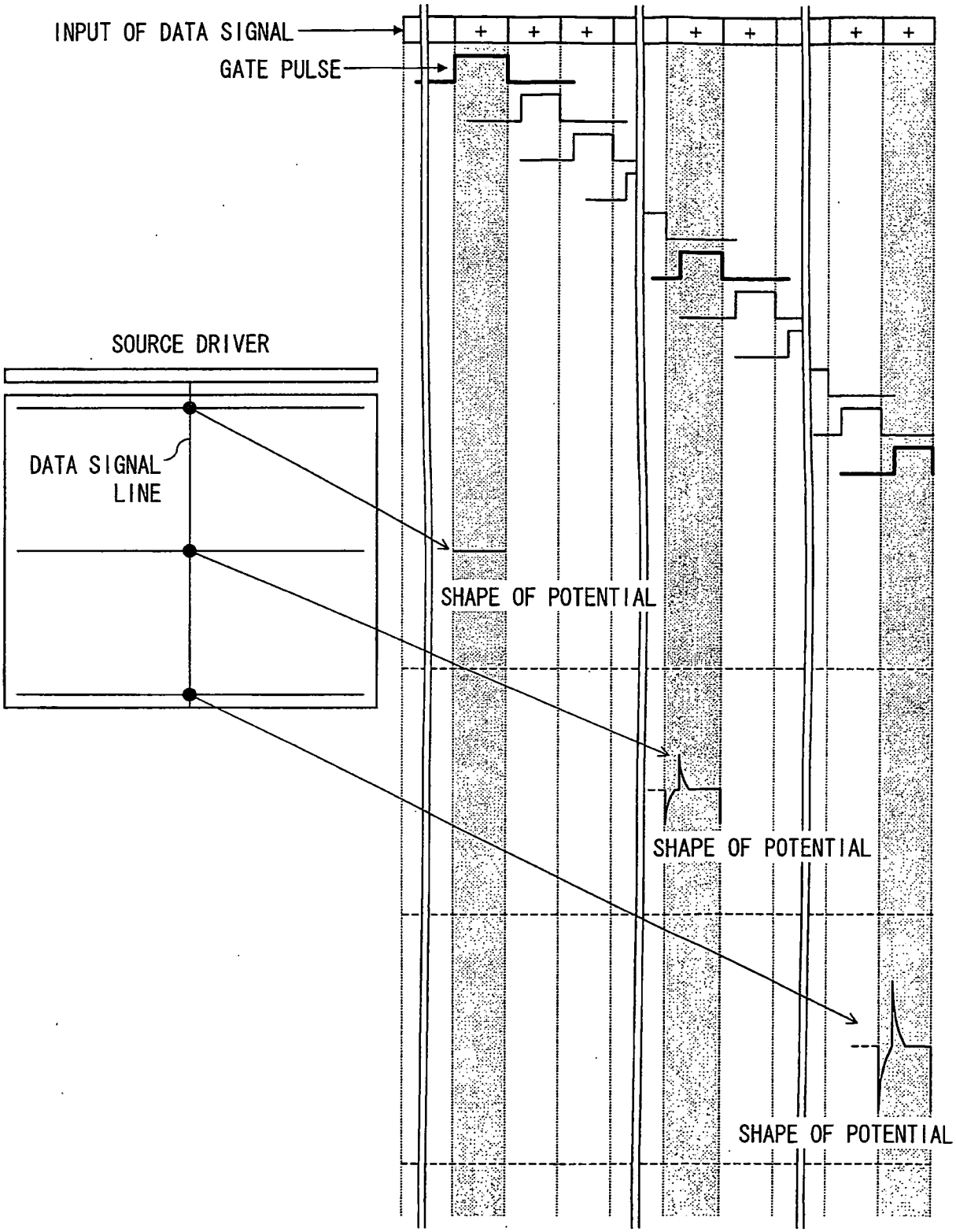


FIG. 36


INPUT OF DATA SIGNAL
GATE PULSE
SOURCE DRIVER
DATA SIGNAL LINE
SHAPE OF POTENTIAL
SHAPE OF POTENTIAL
SHAPE OF POTENTIAL

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- JP 2008009368 A **[0002]**
- US 20060044292 A1 **[0004]**
- US 20060208984 A1 **[0005]**

专利名称(译)	显示装置，液晶显示装置，显示装置的驱动方法和电视接收机		
公开(公告)号	EP2420993B1	公开(公告)日	2018-04-25
申请号	EP2010764184	申请日	2010-02-09
[标]申请(专利权)人(译)	夏普株式会社		
申请(专利权)人(译)	夏普株式会社		
当前申请(专利权)人(译)	夏普株式会社		
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发明人	KITAYAMA, MASAE SHIMOSHIKIRYOH, FUMIKAZU IRIE, KENTAROH		
IPC分类号	G09G3/36 G02F1/133 G09G3/20 G02F1/1362 G09G5/00 H04N5/74		
CPC分类号	G02F1/136286 G09G3/3614 G09G3/3659 G09G5/006 G09G2300/0426 G09G2300/0447 G09G2300/0876 G09G2310/0205 G09G2310/067 G09G2320/0219 G09G2320/0223 G09G2320/0233 G09G2330/08 G09G3/3674 G09G3/3685 H04N5/7408		
优先权	2009097493 2009-04-13 JP		
其他公开文献	EP2420993A1 EP2420993A4		
外部链接	Espacenet		

摘要(译)

本发明的一个目的是即使在长期反转驱动中也减少数据信号线的电位中产生的波纹，并由此改善显示质量。本发明的液晶显示装置包括扫描信号线和数据信号线，其中输出一个扫描脉冲以选择一条扫描信号线，每条数据信号线接收每一垂直扫描周期极性颠倒的数据信号而在一个水平扫描周期中，两条数据信号线中的一条接收具有极性的数据信号，另一条数据信号线接收具有另一极性的另一数据信号，两条数据信号线彼此相邻排列，扫描脉冲以2组为单位连续输出，并且在两个扫描脉冲（例如P 1和P 1）下降的时刻，两个扫描脉冲（例如P m和P n）上升。

FIG. 1