(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) **EP 2 397 891 A1**

(12) **EUROPEAN PATENT APPLICATION**
published in accordance with Art. 153(4) EPC

(43) Date of publication:
21.12.2011 Bulletin 2011/51

(21) Application number: **09840033.6**

(22) Date of filing: **05.11.2009**

(51) Int Cl.:
G02F 1/1368 *(2006.01)* ***G02F 1/1345*** *(2006.01)*
G09F 9/30 *(2006.01)*

(86) International application number:
PCT/JP2009/068905

(87) International publication number:
WO 2010/092714 (19.08.2010 Gazette 2010/33)

(84) Designated Contracting States:
AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO SE SI SK SM TR

(30) Priority: **16.02.2009 JP 2009033132**

(71) Applicant: **Sharp Kabushiki Kaisha**
Osaka-shi, Osaka 545-8522 (JP)

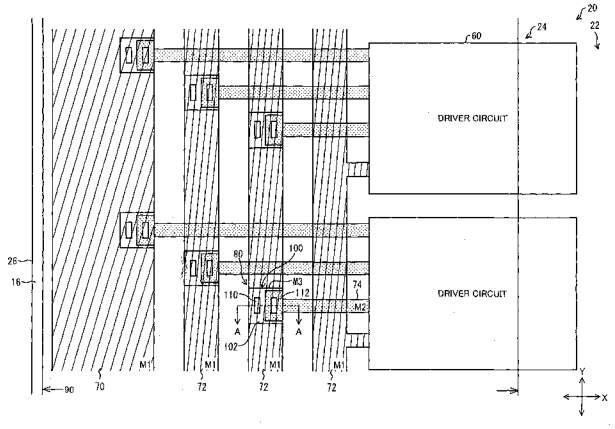
(72) Inventors:
- **Ogasawara, Isao**
  Osaka-shi, Osaka 545-8522 (JP)
- **Yamada, Takaharu**
  Osaka-shi, Osaka 545-8522 (JP)
- **Yoshida, Masahiro**
  Osaka-shi, Osaka 545-8522 (JP)
- **Horiuchi, Satoshi**
  Osaka-shi, Osaka 545-8522 (JP)
- **Tanaka, Shinya**
  Osaka-shi, Osaka 545-8522 (JP)
- **Kikuchi, Tetsuo**
  Osaka-shi, Osaka 545-8522 (JP)

(74) Representative: **Goddar, Heinz J. et al**
Forrester & Boehmert
Pettenkoferstrasse 20-22
80336 München (DE)

(54) TFT ARRAY SUBSTRATE, AND LIQUID CRYSTAL DISPLAY PANEL

(57) The present invention provides a TFT array substrate (20), in which TFT elements and pixel electrodes being correspondingly connected with the TFT elements are arrayed in matrix on an insulating substrate, the TFT array substrate including: gate bus lines made from a first metal material (M1); source bus lines made from a second metal material (M2); pixel electrodes made from a third metal material (M3); a clock wiring (72) made from the first metal material (M1); a branch wiring (74) made from the second metal material (M2); and a connection conductor (102) made from the third metal material (M3), the connection conductor (102) connecting the clock wiring (72) and the branch wiring (74) at a connection part (80) in a periphery area (24), the connection part (80) having a branch-wiring via hole (112), which exposes the branch wiring (74) which is covered with the connection conductor (102), and overlaps the clock wiring (72) at least partly in a plane view.

FIG. 1



EP 2 397 891 A1

Description

Technical Field

[0001] The present invention relates to a TFT array substrate in which TFT elements are provided on an insulating substrate, and to a liquid crystal display panel using the TFT array substrate.

Background Art

[0002] TFT array substrates in which TFT (Thin Film transistor) elements are provided on an insulating substrate have been widely used in display devices (such as liquid crystal panels), and sensor devices. The TFT elements are connected with wirings at their electrodes.

[0003] Specifically, a TFT element is connected with a corresponding gate bus line at its gate electrode, and connected with a corresponding source bus line at its source electrode.

[0004] Moreover, in case where the TFT array substrate is used in a liquid crystal panel, the TFT element is connected with a pixel electrode at its drain electrode.

[0005] In case where the TFT elements are arrayed in matrix, the gate bus lines and the source bus lines are provided perpendicular to each other on the insulating substrate. In this case, the gate bus lines and source bus lines are provided in different layers on the insulating substrate between which an insulating layer is provided, lest the gate bus lines and source bus lines be electrically connected with each other.

(Schematic Configuration of TFT Array Substrate)

[0006] Next, a configuration of the TFT array substrate is schematically described below.

[0007] Fig. 12 is a plane view schematically illustrating a configuration of a TFT array substrate 20.

[0008] As illustrated in Fig. 12, the TFT array substrate 20 has a display area 22 in a central portion thereof in a plane view. In the display area, TFT elements and pixel electrodes correspondingly connected to the TFT elements are arrayed in matrix.

[0009] An area around the display area 22 and in the vicinity of substrate edges 26 of the TFT array substrate 20 is a periphery area 24. In the periphery area 24, a driver circuit 60 and the like are provided.

[0010] One specific example of the driver circuit 60 is a gate driver circuit. Fig. 12 illustrates an exemplary configuration in which the driver circuit 60 is provided in the periphery area 24 on either side of the display area 22 in a horizontal direction (the X direction in Fig. 12).

[0011] In this configuration, the driver 60 is connected with the TFT elements (not illustrated) in the display area 22 via wirings such as the gate bus lines 42.

[0012] Moreover, the TFT array substrate 20 illustrated in Fig. 12 is provided with a driver 62 in the periphery area 24 on one of both sides of the display area 22 in the vertical direction (the Y direction in Fig. 12). The driver 62 and the driving circuits 60 are connected via a gate driver circuit signal wiring 46 such as a clock wiring. Moreover, the driver 62 is connected with the TFT element (not illustrated) in the display area 22 via wirings such as the source bus lines 44.

[0013] Moreover, the TFT array substrate 20 are assembled together with a counter electrode (not illustrated) via a seal 90, thereby constituting a liquid crystal display panel 10. The seal 90 is provided in a frame-like shape along and inside the substrate edges 26 of the TFT array substrate 20.

(Periphery Area)

[0014] Next, based on Fig. 13, the periphery area 24 is described in more details.

[0015] Fig. 13 is a plane view schematically illustrating a configuration of the periphery area 24.

[0016] As illustrated in Fig. 13, the periphery area 24 is provided with not only the driver circuits 60 but also various wirings connected with the driver 62. The wirings are provided between the driver circuits 60 and substrate edges 26 of an insulating substrate 16. Fig. 13 illustrates an example of the TFT array substrate 20 in which a low-potential-side power supply wiring 70, a clock wiring 72, and branch wirings 74 are provided as the wirings. Among the wirings, the low-potential-side power supply wiring 70 and the clock wiring 72 are extended in the vertical direction (Y direction) and the branch wirings 74 are extended in the horizontal direction (X direction). Further, the low-potential-side power supply wiring 70 and the clock wiring 72 are electrically connected with the driver circuit 60 via the branch wirings 74, correspondingly.

(Metal materials etc.)

[0017] Next, metal materials etc. for forming the wirings are explained below.

[0018] The low-potential-side power supply wiring 70 and the clock wiring 72 extended in the Y direction are provided on the insulating substrate in such a manner that the low-potential-side power supply wiring 70 and the clock wiring 72 extended in the Y direction are provided in a layer different from another layer thereon in which the branch wirings 74 extended in the X direction are provided. And, they are formed from different metal materials.

[0019] Fig. 14 is a cross sectional view schematically illustrating a configuration of the TFT array substrate 20.

[0020] As illustrated in Fig. 14, it is generally configured such that a first metal material M1, a first insulating material I1, a second metal material M2, a second insulating material I2, and a third metal material M3 are laminated in this order on the insulating substrate 16. The first metal material M1 is a material from which the gate bus lines 42 are formed. The first insulating material I1 is a material

from which a gate insulating film 50 is formed. The second metal material M2 is a material from which the source bus lines 44 are formed. The second insulating material I2 is a material from which an interlayer insulating film 52 is formed. And the third metal material M3 is a material from which pixel electrodes 48 are formed.

[0021] The low-potential-side power supply wiring 70 and the clock wiring 72 are formed from the first metal material M1, and the branch wirings 74 are formed from the second metal material M2.

[0022] With this configuration, a wiring extended in the X direction can be crossed easily with a wiring extended in the Y direction, without electrically connecting these wirings as illustrated in an intersection part 82 in Fig. 13.

[0023] On the other hand, it is necessary to provide a contact hole in order to establish electrical connection between a wiring extended in the X direction and a wiring extended in the Y direction, as illustrated at a connection portion 80 in Fig. 13.

(Patent Literature 1)

[0024] One conventional configuration of such a contact hole is one as illustrated in Patent Literature 1, for example.

[0025] Fig. 15 is a view illustrating an amorphous silicon thin film transistor liquid crystal display panel as described in Patent Literature 1.

[0026] As illustrated in Fig. 15, a main wiring 150 and a gate electrode 160 are connected electrically via a contact hole 100 provided in a connection portion 80.

Citation List

[Patent Literatures]

[0027]

[Patent Literature 1]
Japanese Translation of PCT Application, Tokuhyo, No. 2005-527856 A (Publication Date: September 15, 2005)
[Patent Literature 2]
US Patent No. 7379148 B2, specification (May 27, 2008)
[Patent Literature 3]
Japanese Patent Application Publication, Tokukai, No. 2006-259691 (Publication Date: September 28, 2006)
[Patent Literature 4]
Japanese Patent Application Publication, Tokukaihei, No. 9-179116 (Publication Date: July 11, 1997)
[Patent Literature 5]
Japanese Patent Application Publication, Tokukai, No. 2006-39524 (Publication Date: February 9, 2006)

Summary of Invention

Technical Problem

[0028] However, the conventional configuration of the contact hole 100 has such a problem that it causes deterioration in display quality of the liquid crystal display panel 100. The following explains the problem.

[0029] Fig. 16 is a view schematically illustrating a configuration of a conventional connection portion 80. Meanwhile, Fig. 17 is a cross sectional view taken across line C-C of Fig. 16.

[0030] As illustrated in Fig. 16, the conventional contact hole 100 is partly on and off the clock wiring 72 when viewed in a plane view. That is, the conventional contact hole 100 has an off-wiring portion 104.

[0031] As illustrated in Fig. 17, the contact hole 100 allows the clock wiring 72 to be connected with the branch wiring 74.

[0032] The clock wiring 72 is formed from the first metal material M 1 from which the layer of the gate bus line 42 is formed. Meanwhile, the branch wiring 74 is formed from the second metal material M2 from which the layer of the source bus line 44 is formed. Therefore, the clock wiring 72 and the branch wiring 74 are formed on the different layers on the insulating substrate 16.

[0033] A connection conductor 102 provided in the contact hole 100 connects the clock wiring 72 with the branch wiring 74. However, the clock wiring 72 and the branch wiring 74 do not overlap each other in the plane view. Accordingly, the connection conductor 102 is so provided that it can connect the clock wiring 72 with the branch wiring 74 in the plane view.

(Via Hole)

[0034] More specifically, through a main-wiring via hole 110, the connection conductor 102 and the clock wiring 72 are connected with each other at a place where the connection conductor 102 and the clock wiring 72 overlap each other in a plane view. Meanwhile, through a branch-wiring via hole 112, the connection conductor 102 and the branch wiring 74 are connected with each other at a place where the connection conductor 102 and the branch wiring 74 overlap each other in a plane view.

[0035] In other words, the contact hole 100 is so configured that the clock wiring 72 and the branch wiring 74 are connected through the two via holes.

[0036] Here, the connection conductor 102 is formed from the third metal material M3, which is a material from which the pixel electrodes are formed.

[0037] In the vicinity of the main-wiring via hole 110, the gate insulating film 50 and the interlayer insulating film 52 intervene between the clock wiring 72 and the connection conductor 102. Accordingly, the main-wiring via hole 110 penetrates the gate insulating film 50 and the interlayer insulating film 52 so as to allow the clock wiring 72 and the connection conductor 102 to be con-

nected with each other.

[0038] Similarly, in the vicinity of the branch-wiring via hole 112, the interlayer insulating film 52 intervenes between the branch wiring 74 and the connection conductor 102. Accordingly, the branch-wiring via hole 112 penetrates the interlayer insulating film 52 so as to allow the branch wiring 74 and the connection conductor 102 to be connected with each other.

(Off-wiring Portion)

[0039] The main-wiring via hole 110 and the branch-wiring via hole 112 are connected via the connection conductor 102.

[0040] The conventional TFT array substrate 20 is so configured that the clock wiring 72 and the branch wiring 74 do not overlap each other in a plane view. That is, the branch wiring 74 is extended just short of clock wiring 72. Accordingly, the connection conductor 102 has an off-wiring portion 104. The off-wiring portion 104 is that portion of the connection conductor 102 which is off the clock wiring 72 in a plane view.

[0041] The off-wiring portion 104 allows the connection between the main-wiring via hole 110 and the branch-wiring via hole 112.

(Seal)

[0042] Next, the seal 90 for bonding the TFT array substrate 20 with the counter substrate.

[0043] The seal 90 is provided in the periphery area 24 of the TFT array substrate 20 so as to be along the substrate edges 26, as illustrated in Fig. 12. As illustrated in Fig. 16, the seal 90 covers the low-potential-side power supply wiring 70, the clock wiring 72, and, partly, the driver circuits 60. That is, in the plane view, the seal 90 overlaps the wiring extended in the X direction, and the wiring extended in the Y direction.

[0044] The seal 90 is so positioned for the sake of sufficiently functioning to bond the TFT array substrate 20 and the counter substrate 18, and reducing an area of the frame portion.

[0045] Because the seal 90 is so positioned, the contact hole 100 is positioned under the seal 90.

(Cell Thickness)

[0046] The conventional liquid crystal display panel 10 likely fails to keep a uniform cell thickness in the vicinity of the seal 90.

[0047] The failure of keeping uniform cell thickness is due to a level difference caused by the contact hole 100 and to differences in width, density, etc. of the wirings provided under the seal 90.

[0048] Especially, the conventional liquid crystal display panel 10 in which the connection conductor 102 has the off-wiring portion is apt to have such an uneven cell thickness.

(Seal Thickness)

[0049] The uneven cell thickness is caused because there are regions with or without the contact hole 100 when viewed along the Y direction. That is, the uneven cell thickness is caused because the seal 90 has an uneven thickness between the two kind regions. In addition to two dent parts due to the main-wiring via hole 110 and the branch-wiring via hole 112, there is a dent portion formed along the Y direction at or near the contact hole 100. The dent portion formed along the Y direction at or near the contact hole 100 likely causes the uneven cell thickness.

[0050] As described above, the conventional liquid crystal display panel 10 likely has an uneven cell thickness due to pattern configuration at or near the contact hole 100 or uneven wiring density at or near the contact hole 100.

(Display Quality)

[0051] The uneven cell thickness likely deteriorates a display quality.

[0052] Moreover, the conventional liquid crystal display panel 10 with the off-wiring portion has such a problem in that the off-wiring portion makes it difficult to perform uniform light irradiation to a light curing resin or the like in case where the light curing resin or the like is provided at or near the contact hole 100. This leads to insufficient curing of the light curing resin. In such a case, a material of the sealing 90 would likely seep in a liquid crystal layer, thereby causing poor display quality.

(Output characteristics of Driver Circuit)

[0053] Further, in response to recent demands for outer dimensional reduction of display panels, the periphery area 24 of the TFT array substrate 20 may be reduced in area, as a result of which inter-wiring distances between wirings such the low-potential-side power supply wiring 70 and clock wiring 72 should be smaller. In this case, the configuration with the off-wiring portion may be a hindrance to the reduction in the inter-wiring distances. That is, the reduction in the inter-wiring distances cannot be done in such a way that an area in which the off-wiring portion overlaps an adjacent wiring is reduced or a distance from the off-wiring portion to such an adjacent wiring is reduced, because, if the off-wiring portion is so arranged, wiring load will be increased, thereby deteriorating the output characteristics of the driver circuits.

[0054] The present invention was accomplished in order to solve the problems, and an object thereof is to provide a TFT array substrate and a liquid crystal display panel, each of which can avoid display quality deterioration caused by an uneven cell thickness.

Solution to Problem

[0055] In order to attain the object, a TFT array substrate according to the present invention is a TFT array substrate, in which TFT elements and pixel electrodes being correspondingly connected with the TFT elements are arrayed in matrix on an insulating substrate, the TFT array substrate including: gate bus lines on the insulating substrate, the gate bus lines being correspondingly connected with the TFT elements and being formed from a first metal material; and source bus lines on the insulating substrate, the source bus lines being correspondingly connected with the TFT elements and being formed from a second metal material, the pixel electrodes being made from a third metal material, the insulating substrate having a display area in which the pixel electrodes are arrayed in matrix, and a periphery area around the display area, the periphery area being provided with driver circuits for driving the TFT elements corresponding thereto, the periphery area being provided with (i) branch wirings being correspondingly connected with the driver circuits, and (ii) a main wring being connected with the branch wirings, the branch wirings being formed from one of the first metal material and the second metal material, the main wiring being formed from the other one of the first metal material and the second metal material, the periphery area being provided with connection parts, at which the main wiring is connected with the respective branch wirings, at each of the connection parts, a connection conductor electrically connecting the main wiring with corresponding one of the branch wirings, the connection conductor being formed from the third metal material, the connection parts each having a branch-wiring via hole through which the corresponding one of the branch wirings, which is covered with the connection conductor, is exposed, at least one of the connection parts being such that at least part of the branch-wiring via hole overlaps with the main wiring in a plane view.

[0056] Moreover, in order to attain the object, a TFT array substrate according to the present invention is a TFT array substrate in which TFT elements and pixel electrodes being correspondingly connected with the TFT elements are arrayed in matrix on an insulating substrate, the TFT array substrate including: gate bus lines on the insulating substrate, the gate bus lines being correspondingly connected with the TFT elements and being formed from a first metal material; and source bus lines on the insulating substrate, the source bus lines being correspondingly connected with the TFT elements and being formed from a second metal material, the pixel electrodes being made from a third metal material, the insulating substrate having a display area in which the pixel electrodes are arrayed in matrix, and a periphery area around the display area, the periphery area being provided with periphery TFT elements for driving the TFT elements corresponding thereto, the periphery area being provided with (i) branch wirings being correspondingly connected with the periphery TFT elements, and (ii) a main wring being connected with the branch wirings, the branch wirings being formed from one of the first metal material and the second metal material, the main wiring being formed from the other one of the first metal material and the second metal material, the periphery area being provided with connection parts, at which the main wiring is connected with the respective branch wirings, at each of the connection parts, a connection conductor electrically connecting the main wiring with corresponding one of the branch wirings, the connection conductor being formed from the third metal material, the connection parts each having a branch-wiring via hole through which the corresponding one of the branch wirings is exposed, provided that the connection conductor covers this exposed portion of the corresponding one of the branch wirings, at least one of the connection parts being such that at least part of the branch-wiring via hole overlaps with the main wiring in a plane view.

[0057] In these configurations, in the connection parts, at least part of the branch-wiring via hole overlaps with the main wiring in a plane view. These configurations makes it difficult for the connection conductor to have a off-wiring portion described above, thereby causing the wiring layer to have more uniform thickness in the direction in which the main wirings extend.

[0058] This makes it easy to prevent the uneven cell thickness, for example, in case where the seal is provided in the periphery area. Thus, it becomes easier to prevent display quality deterioration in the TFT array substrate with any of these configurations.

Advantageous Effects of Invention

[0059] As described above, the TFT array substrate according to the present invention is configured to include: gate bus lines on the insulating substrate, the gate bus lines being correspondingly connected with the TFT elements and being formed from a first metal material; and source bus lines on the insulating substrate, the source bus lines being correspondingly connected with the TFT elements and being formed from a second metal material, the pixel electrodes being made from a third metal material, the insulating substrate having a display area in which the pixel electrodes are arrayed in matrix, and a periphery area around the display area, the periphery area being provided with driver circuits or periphery TFT elements for driving the TFT elements corresponding thereto, the periphery area being provided with (i) branch wirings being correspondingly connected with the driver circuits or periphery TFT elements, and (ii) a main wring being connected with the branch wirings, the branch wirings being formed from one of the first metal material and the second metal material, the main wiring being formed from the other one of the first metal material and the second metal material, the periphery area being provided with connection parts, at which the main wiring is connected with the respective branch wirings, at each of the connection parts, a connection conductor connect-

ing the main wiring with corresponding one of the branch wirings, the connection conductor being formed from the third metal material, the connection parts each having a branch-wiring via hole through which the corresponding one of the branch wirings, which is covered with the connection conductor, is exposed, at least one of the connection parts being such that at least part of the branch-wiring via hole overlaps with the main wiring in a plane view.

[0060] This makes it possible to prevent display quality deterioration caused by uneven cell thickness.

Brief Description of Drawings

[0061]

[Fig. 1]
Fig. 1 is a view schematically illustrating a configuration of a TFT array substrate according to one embodiment of the present invention.
[Fig. 2]
Fig. 2 is a view illustrating a cross section taken along line A-A of Fig. 1.
[Fig. 3]
Fig. 3 is a view schematically illustrating a configuration of a TFT array substrate according to another embodiment of the present invention.
[Fig. 4]
Fig. 4 is a view illustrating a cross section taken along line B-B of Fig. 3.
[Fig. 5]
Fig. 5 is a view schematically illustrating a configuration of a TFT array substrate according to still another embodiment of the present invention.
[Fig. 6]
Fig. 6 is a view schematically illustrating a configuration of a TFT array substrate according to yet another embodiment of the present invention.
[Fig. 7]
Fig. 7 is a view schematically illustrating a configuration of a TFT array substrate according to yet another embodiment of the present invention.
[Fig. 8]
Fig. 8 is a view schematically illustrating a configuration of a TFT array substrate according to yet still another embodiment of the present invention.
[Fig. 9]
Fig. 9 is a view schematically illustrating a configuration of a TFT array substrate according to further another embodiment of the present invention.
[Fig. 10]
Fig. 10 is a view schematically illustrating a configuration of a TFT array substrate according to further another embodiment of the present invention.
[Fig. 11]
Fig. 11 is a view schematically illustrating a configuration of a TFT array substrate according to yet further another embodiment of the present invention.
[Fig. 12]
Fig. 12 is a plane view schematically illustrating a configuration of a TFT array substrate.
[Fig. 13]
Fig. 13 is a plane view schematically illustrating a configuration of a periphery area of the TFT array substrate.
[Fig. 14]
Fig. 14 is a cross sectional view schematically illustrating a configuration of the TFT array substrate.
[Fig. 15]
Fig. 15 is a view illustrating an amorphous silicon thin film transistor liquid crystal display panel as described in Patent Literature 1.
[Fig. 16]
Fig. 16 is a view illustrating a conventional art and schematically illustrating a configuration of a connection portion.
[Fig. 17]
Fig. 17 is a cross sectional view taken along line C-C of Fig. 16.

Description of Embodiments

[0062] In the followings, embodiments of the present invention are described in more details.

[Embodiment 1]

[0063] One embodiment of the present invention is described below referring to Figs. 1 and 2.

[0064] Fig. 1 is a view schematically illustrating a configuration of a TFT array substrate 20 of the present embodiment.

[0065] The schematic configuration of the TFT array substrate 20 of the present embodiment is substantially similar to that of the TFT array substrate 20 explained above referring to Fig. 16.

[0066] That is, various wirings (wiring layer) and driver circuits are provided in a periphery area 24 of the TFT array substrate 20.

[0067] More specifically, the various wirings encompass a low-potential-side power supply wiring 70 (signal wiring for scanning line driver circuits) and clock wirings 72 (signal wiring for scanning line driver circuits) along the Y direction of the TFT array substrate 20. The low-potential-side power supply wiring 70 and clock wirings 72 are each main wirings. More specifically, one low-potential-side power supply wiring 70, and three clock wirings 72 are aligned in this order in a direction of from one substrate edge 26 to a display area 22.

[0068] Moreover, driver circuits 60 (such as gate driver circuits) are provided between these wirings and the display area 22.

[0069] Here, the display area 22 is an area in which TFT elements (not illustrated) and pixel electrodes (not illustrated) connected correspondingly with the TFT elements are arrayed in matrix.

[0070] Further, branch wirings 74 are provided for connecting these wirings correspondingly with the driver circuits 60. The branch wirings 74 are extended in the X direction.

[0071] A contact hole 100 is provided at each of intersection parts 80 at which the branch wirings 74 are connected with the low-potential-side power supply wiring 70 or any of the clock wirings 72 correspondingly.

[0072] The TFT array substrate 20 according to the present embodiment is so configured that a connection conductor 102 has no off-wiring portion 104 described above. In the following, the configuration of the present embodiment is described referring to a connection portion 80 for connection between a clock wiring 72 and a branch wiring 74, for example.

[0073] At the connection portion 80, the clock wiring 72 and the branch wiring 74 are electrically connected with each other through a contact hole 100.

[0074] Referring to Fig. 2, this configuration is described in further details. Fig. 2 is a cross sectional view taken along line A-A of Fig. 1.

[0075] As illustrated in Fig. 2, the contact hole 100 has two via holes, namely, a main-wiring via hole 110 and a branch-wiring via hole 112. Through the main-wiring via hole 110, the connection conductor 102 and the clock wiring 72 are connected with each other. In other words, through the main-wiring via hole 110, the clock wiring 72 (serving as a main wiring) which is covered with the connection conductor 102, is exposed.

[0076] Moreover, through the branch-wiring via hole 112, the connection conductor 102 and the branch wiring 74 are connected with each other. In other words, through the branch-wiring via hole 112, the branch wiring 74 is exposed, provided that the connection conductor 102 covers this exposed portion of the branch wiring 74.

[0077] The clock wiring 72 is formed from a first metal material M 1 from which gate bus lines 42 are formed. Meanwhile, the branch wiring 74 is formed from a second metal material M2 from which source bus lines 44 are formed. Moreover, the connection conductor 102 is formed from a third metal material M3 from which the pixel electrodes 48 are formed.

[0078] These metal materials are laminated on an insulting substrate 16 made of glass in an order of the first metal material M1, the second metal material M2, and the third metal material M3. Between the first metal material M 1 and the second metal material M2, a gate insulating film 50 is provided. The gate insulating film 50 is formed from a first insulating material I1. Moreover, between the second metal material M2 and the third metal material M3, an interlayer insulating film 52 is provided. The interlayer insulating film 52 is formed from a second insulating material I2. Moreover, the first metal material M1 and the second metal material M2 may be, but not limited to, aluminum, molybdenum, tantalum, or the like. Moreover, the third metal material M3 may be, for example, ITO (Indium Tin Oxide) or the like.

[0079] With this configuration, at the main-wiring via hole 110, the connection conductor 102 penetrates the gate insulating film 50 and the interlayer insulating film 52 and is connected with the clock wiring 72.

[0080] Moreover, at the branch-wiring via hole 112, the connection conductor 102 penetrates the interlayer insulating film 52 and is connected with the branch wiring 74.

[0081] Moreover, the TFT array substrate 20 of the present embodiment is so configured that, at the connection portion 80, the clock wiring 72 and branch wiring 74 overlap each other in a plane view.

[0082] Therefore, the connection conductor 102 has no portion under which neither the clock wiring 72 nor the branch wiring 74 is provided. In other words, either the clock wiring 72 or the branch wiring 74 are provided under the connection conductor 102 with no exception. What is meant by the wording "under" the connection conductor 102 or the portion thereof is under these but above the insulating substrate 16.

[0083] In the configuration explained above, the connection conductor 102 has no off-wiring portion in which, in a plane view, the connection conductor 102 does not overlap any of the wirings to which the connection conductor 102 is connected. In other words, in the connection portion 80, the connection conductor 102 is provided only on the wirings to which the connection conductor 102 is connected.

[0084] More specifically, the TFT array substrate 20 exemplified in the present embodiment is so configured that the connection conductor 102 overlaps the clock wiring 72 in a plane view in such a way that both sides of the connection conductor 102 are matched with sides of the clock wiring 72. Therefore, the connection conductor 102 has no portion that is off the clock wiring 72 in a plane view.

[0085] As described above, the connection conductor 102 of the present embodiment overlaps the clock wiring 72 in a plane view in such a way that both sides of the connection conductor 102 are matched with sides of the clock wiring 72, wherein the clock wiring 72 is a wiring undermost between two wirings to which the connection conductor 102 is connected, in other words a wiring that is closer to the insulting substrate 16 between the two wirings to which the connection conductor 102 is connected.

[0086] On the other hand, the branch wiring 74 connected with the clock wiring 72 is extended to overlap the clock wiring 72 in a plane view, unlike the conventional TFT array substrate 20 illustrated in Fig. 16.

[0087] With this configuration, the main-wiring via hole 110 and the branch-wiring via hole 112 can be provided above the clock wiring 72 in a plane view, as illustrated in Fig. 2. Further, with this configuration, the connection conductor 102 for covering and connecting the main-wiring via hole 110 and the branch-wiring via hole 112 can be provided without being off the clock wiring 72 in a plane view.

(Display Quality)

[0088] As described above, the connection conductor 102 is provided without being off the clock wiring 72 in a plane view, thereby making it possible to inhibit uneven cell thickness.

[0089] More specifically, the connection conductor 102 can easily attain a stable surface configuration, because the connection conductor 102 is provided over a uniform conductive layer.

[0090] In the present embodiment, the conductive layer under the whole connection conductor 102 is the clock wiring 72 provided on the insulating substrate 16. Because of this, the connection conductor 102 can easily attain a stable surface configuration.

[0091] Moreover, the connection conductor 102 has no off-wiring portion 104. Therefore, it becomes easier to have a more uniform wiring density under the seal 90 even if a contact hole is provided on a signal wiring for a scanning line driver circuit.

[0092] As a result, it becomes easy to attain uniform cell thickness in the TFT array substrate 20 of the present embodiment.

[0093] Moreover, because uneven cell thickness is thus inhibited, deterioration in display quality is inhibited in the TFT array substrate 20 of the present embodiment.

[0094] This effect of inhibiting the display quality deterioration caused due to the unevenness in the wirings or the like under the seal 90 is especially effective to a configuration in which the interlayer insulating film 52 is not a flattening film such as an organic film.

(Seal Curing)

[0095] Moreover, the TFT array substrate 20 according to the present embodiment makes it easier to cure the seal 90 surely.

[0096] As described above referring to Fig. 12 and the like, the seal 90 for bonding the TFT array substrate 20 and the counter substrate (not illustrated) is provided in the periphery area 24 of the TFT array substrate 20. As a result, the contact holes 100 and their vicinities are covered with the seal 90.

[0097] In many cases, the seal 90 is UV-light curable. Further, in such a case, the seal 90 is irradiated with UV light from below the insulating substrate 16. Herein, the wording "from below the insulating substrate 16" means "from that side of the insulating substrate 16 on which the clock wiring 72 is not provided".

[0098] Further, the clock wiring 72, the branch wiring 74, etc. are not UV permeable in general, because these wirings, etc. are formed from a conductor(s), that is, metal.

[0099] Therefore, it is preferable that the peripheral area 24 in which the seal 90 is provided does not have too much wirings etc. therein. And if the peripheral area 24 has wirings etc. therein, it is preferable that the wirings has uniform density over the peripheral area 24.

[0100] In this regard, the TFT array substrate 20 according to the present embodiment is so configured that the connection conductor 102 has no off-wiring portion 104. More specifically, the connection conductor 102 has no portion that is off the clock wiring 72 in a plane view.

[0101] Consequently, the periphery area 24 has a smaller portion that is provided with the metal.

[0102] Accordingly, it becomes easier to attain more even density in the portion that is provided with the metal. This is attributed to the absence of the off-wiring portion 104 that is a metal protrusion.

[0103] With these reasons, the TFT array substrate 20 according to the present embodiment makes it easy to evenly irradiate light to the seal 90. As a result, the curing of the seal 90 can be surely performed.

[0104] This ensured effect of the seal 90 is particularly effective in a liquid crystal display panel which is manufactured by One-Drop-Fill method for introducing liquid crystal.

(Narrower Frame)

[0105] Moreover, with this configuration in which the connect conductor 102 has no off-wiring portion 104, it is possible to reduce the area occupied by the contact hole 100. Therefore, a wiring area can be smaller, thereby allowing the frame portion of the liquid crystal display panel to be narrower.

[0106] It should be noted that the present invention is not limited to the wiring width exemplified in Fig. 1 in which the clock wirings 72 are identical in wiring width.

[0107] Moreover, it is preferable that the peripheral area 24 has substantially same wiring density at edges (gate edges) in the X direction in Fig. 1 and at edges (source edges) in the Y direction in Fig. 1. Here, the wiring density = wiring width / space.

[0108] Moreover, the clock wirings 72 and the low-potential-side power supply wiring 70 (outer wiring) may or may not be formed from an identical metal material. For example, the low-potential-side power supply wiring 70 may be formed from the second metal material. In such a configuration, the low-potential-side power supply wiring 70 and the branch wiring 74 can be electrically connected without using the contact hole 100.

[0109] Moreover, the present invention is not limited as to how many the low-potential-side power supply wiring 70 is provided, while the present embodiment exemplifies a configuration in which the single low-potential-side power supply wiring 70 is provided. That is, a plurality of low-potential-side power supply wirings 70 may be provided.

[Embodiment 2]

[0110] Another embodiment of the present embodiment is described below, referring to Figs. 3 and 4. Fig. 3 is a view schematically illustrating a configuration of a TFT array substrate 20 according to the present embod-

iment. Moreover, Fig. 4 is a cross-sectional view taken along line B-B of Fig. 3.

[0111] For the sake of easy explanation, like reference numbers are given to members having the like functions similar to those explained in Embodiment 1, and their explanation is not repeated here.

[0112] The TFT array substrate 20 of the present embodiment is different from the TFT array substrate 20 of Embodiment 1 in terms of the configuration of the contact hole 100.

[0113] More specifically, the contact hole 100 of the present embodiment is different from that of Embodiment 1 in terms of how many via holes are provided in one contact hole 100.

[0114] That is, the contact hole 100 of Embodiment 1 has two via holes: the main-wiring via hole 110 and the branch-wiring via hole 112.

[0115] On the other hand, the contact hole 100 of the present embodiment has only one via hole, namely, a single via hole 114 serving as the branch via hole 112. In the following, this configuration is described in more details.

[0116] As illustrated in Fig. 4, the contact hole 100 of the present embodiment is also configured such that a branch wiring 74 overlaps a clock wiring 72 in a plane view. Further, a connection conductor 102 overlaps the clock wiring 72 in a plane view. Moreover, the connection conductor 102 has no off-wiring portion 104 that is off the clock wiring 72.

[0117] Unlike the contact hole 100 in Embodiment 1, the contact hole 100 of the present embodiment is configured such that the branch wiring 74 is provided in the vicinity of a via hole through which the connection conductor 102 is connected with the clock wiring 72.

[0118] Further, the branch wiring 74 is electrically connected with a side wall 116 of the via hole through which the connection conductor 102 and the clock wiring 72 are connected with each other.

[0119] With this configuration, the contact hole 100 of the present embodiment has only one via hole, namely, the single via hole 114, for the connection between the clock wiring 72 and the branch wiring 74.

[0120] Moreover, the TFT array substrate 20 of the present embodiment is provided with a semiconductor layer 86. The semiconductor layer 86 is provided between a gate insulating film 50 and a branch wiring 74. More specifically, the semiconductor layer 86 includes a lower semiconductor layer 86a provided on the gate insulating film 50, and an upper semiconductor layer 86b provided on the lower semiconductor layer 86a.

[0121] The lower semiconductor layer 86a is a general semiconductor layer. Moreover, the upper semiconductor layer 86b is an ohmic contact layer.

[0122] The TFT array substrate 20 of the present embodiment is provided with the semiconductor layer 86, thereby having a taper portion of the ohmic contact layer. The taper portion of the ohmic contact layer can prevent the connection conductor from being disconnected due to unevenness.

[0123] Moreover, the TFT array substrate 20 of the present embodiment is so configured that the branch wiring 74 includes two metal layers. More specifically, the branch wiring 74 includes a lower branch wiring 74a and an upper branch wiring 74b, wherein the insulating substrate 16 is closer to the lower branch wiring 74a than to the upper branch wiring 74b. The lower branch wiring 74a is formed from titanium (Ti), which is a metal material M2a. Meanwhile, the lower branch wiring 74b is formed from aluminum (Al), which is a metal material M2b.

(Modification)

[0124] Referring to Fig. 5, a modification of the TFT array substrate 20 of the present embodiment is described below. Fig. 5 is a view schematically illustrating a configuration of a TFT array substrate 20 according to the modification of the present embodiment.

[0125] The TFT array substrate 20 of the modification illustrated in Fig. 5 has two contact holes 100 for one connection portion 80.

[0126] More specifically, the two contact holes 100 along the Y direction in which the clock wiring 72 is extended. A connection conductor 102 in one of the two contact holes 100 is connected with that in the other one of the two contact holes 100.

[0127] Like the TFT array substrate 20 described above, the connection conductor 102 also overlaps the clock wiring 72 and has no off-wiring portion that is off the clock wiring 72.

[0128] How many contact holes 100 is provided per one connection portion 80 is not limited to two, and may be three or more.

[0129] In the TFT array substrate 20 according to this modification, a plurality of contact holes 100 is provided per one connection portion 80. Thereby, it becomes possible to reduce contact resistance.

[Embodiment 3]

[0130] In the following, yet another embodiment of the present invention is described referring to Figs. 6 and 7. Figs. 6 and 7 are views schematically illustrating a configuration of a TFT array substrate 20 according to the present embodiment.

[0131] For the sake of easy explanation, like reference numbers are given to members having the like functions similar to those explained in each of the aforementioned embodiments, and their explanation is not repeated here.

[0132] The TFT array substrate 20 of the present embodiment is different from each TFT array substrate 20 of the aforementioned embodiments in terms of a wiring shape. More specifically, a wiring extended in the Y direction has a ladder-like shape.

[0133] In examples respectively illustrated in Figs. 6 and 7, a low-potential-side power supply wiring 70, provided in an outer location toward a substrate edge 26

has a ladder-like shape.

[0134] More specifically, the low-potential-side power supply wiring 70 has rectangular void parts 76. In the examples illustrated in Figs. 6 and 7, the void parts 76 are provided in two rows along the Y directions.

[0135] Each portion between the void parts 76 adjacent in the Y direction is a joint portion 78. The joint parts 78 correspond to "footsteps" of the ladder.

[0136] The examples illustrated in Figs. 6 and 7 exemplify configurations in which two ladders are aligned in the X direction. However, the present invention is not limited to the number of "ladders" aligned in the X direction, and the number of ladders aligned in the X direction may be just one or may be three or more.

[0137] As described above, the TFT array substrate 20 of the present embodiment is so configured that a wiring has the void parts 76.

[0138] UV light passes through the void parts 76. Consequently, the area permissive to UV light is increased, thereby ensuring the curing of the seal 90 as explained above.

[Embodiment 4]

[0139] Yet still another embodiment of the present invention is described below, referring to Fig. 8. Fig. 8 is a view schematically illustrating a TFT array substrate 20 of the present embodiment.

[0140] For the sake of easy explanation, like reference numbers are given to members having the like functions similar to those explained in each of the aforementioned embodiments, and their explanation is not repeated here.

[0141] The TFT array substrate 20 of the present embodiment is different from each TFT array substrate 20 of the aforementioned embodiments in terms of the configuration of the wirings extended in the Y direction. More specifically, at each intersection portion 82, a wiring extended in the Y direction has a narrowed portion 84. The intersection parts 82 are intersections at each of which a wiring extended in the Y direction and a wiring extended in the X direction cross each other without being connected with each other electrically.

[0142] As illustrated in Fig. 8, the TFT array substrate 20 of the present embodiment is so configured that each clock wiring 72 is narrowed in width at each intersection at which the clock wiring 72 cross a branch wiring 74. This portion at which the clock wiring 72 (wiring extended in the Y direction) is narrowed in width is the narrowed portion 84. In other words, the narrowed portion 84 is a constricted part of the clock wiring 72.

[0143] in the TFT array substrate 20 of the present embodiment, an area in which the clock wirings 72 and the branch wirings 74 overlap at the intersection parts 82 is reduced by providing the narrowed parts 84 to the clock wirings 72.

[0144] That is, the wirings extended in the Y directions and the wirings extended in the X directions overlap each other in a smaller area.

[0145] With this configuration, capacitance produced between the wirings extended in the Y directions and the wirings extended in the X directions can be reduced at the intersection parts 82.

[0146] The reduction in such capacitance may lead to circuit output characteristics improvement such as inhibition of signal delay.

[0147] As to a way of narrowing the wiring width, the present invention is not limited particularly. That is, the wiring may be narrowed from both sides, or may be narrowed from one side. Moreover, the wiring may be substantially narrowed by having a void portion in the vicinity of a middle of its width. In other words, the overlapping area with a wiring extended in the X direction can be reduced by providing a void portion to a wiring overlapping the wiring extended in the X direction.

(Semiconductor Layer)

[0148] Moreover, a semiconductor layer 86 may be provided, with which the narrowed parts 84 overlap. By providing the semiconductor layer 86, disconnection with the branch wiring and leakage to signal wiring can be inhibited.

[Embodiment 5]

[0149] Further another embodiment is described below, referring to Figs. 9 and 10. Figs. 9 and 10 are views schematically illustrating TFT array substrates 20 according to further another embodiment of the present invention.

[0150] For the sake of easy explanation, like reference numbers are given to members having the like functions similar to those explained in each of the aforementioned embodiments, and their explanation is not repeated here.

[0151] The TFT array substrate 20 according to the present embodiment is different from each TFT array substrate 20 according to the aforementioned embodiment in terms of the configuration of the driver circuit 60 and the configuration of the seal 90.

(Driver Circuit)

[0152] Firstly, the driver circuit 60 is described below.

[0153] In each of the aforementioned embodiments, only one row of the driver circuits 60 is provided in the X direction, and there is no driver circuit between the wirings extended in the Y direction in the periphery area 24. That is, the driver circuit 60 is provided in a border area between the periphery area 24 and the display area 22.

[0154] On the other hand, the TFT array substrate 20 of the present embodiment is so configured to have two rows of the driver circuits 60 in the X direction. Accordingly, a first row of driver circuits 60a and a second row of driver circuits 60b are aligned in the X direction. More specifically, the first row of driver circuits 60a is provided between a low-potential-side power supply wiring 70

(outer wiring) and a clock wiring 72. The second row of driver circuits 60b is provided in the border area between the display area 22 and the periphery are 24.

[0155] In other words, a signal wiring for a scanning line driver circuit is provided between the rows of the driver circuits 60 in an area not covered by the seal 90, that is, between the seal 90 and the display area 22 serving as an active area.

(Seal)

[0156] Next, the seal 90 is described below.

[0157] In each of the aforementioned embodiments, in the periphery area 24, the seal 90 covers all the wirings extended in the Y direction. More specifically, the low-potential-side power supply wiring 70 and all the clock wirings 72 are covered with the seal 90.

[0158] Consequently, the contact holes 100 provided respectively at the connection parts 80 are all covered with the seal 90.

[0159] On the other hand, the TFT array substrate 20 according to the present embodiment is so configured that the seal 90 covers the low-potential-side power supply wiring 70 and part of the first row of driver circuits 60a. The clock wirings 72 and the second row of driver circuit 60b are not covered with the seal 90.

[0160] Consequently, contact holes provided above the clock wirings 72 are not covered with the seal 90.

[0161] With this configuration, the uneven cell thickness is further inhibited in the TFT array substrate 20 of the present embodiment, because the contact holes 100 covered with the seal 90 can be reduced in number.

[0162] Moreover, with this configuration, the signal wiring for the scanning line driver circuit, which signal wiring provided between the first row of driver circuit 60a and the second row of driver circuit 60b, can be narrower in wiring width, thereby making it easier to narrow the frame portion of the liquid crystal display panel.

[0163] The effect of the inhibition of uneven cell thickness can be achieved by providing one or more of the wirings extended in the Y direction (for example, the clock wirings 72) between the first row of driver circuits 60a and the second row of driver circuits 60b in the X direction.

[Embodiment 6]

[0164] Yet further another embodiment of the present invention is described below, referring to Fig. 11. Fig. 11 is a view schematically illustrating configuration of a TFT array substrate 20 according to the present embodiment.

[0165] For the sake of easy explanation, like reference numbers are given to members having the like functions similar to those explained in each of the aforementioned embodiments, and their explanation is not repeated here.

[0166] The TFT array substrate 20 of the present embodiment is different from each TFT array substrate 20 in the aforementioned embodiment in that a low-potential-side power supply wiring 70 is overlapped by some branch wirings 74. More specifically, the branch wiring 74 extended in the X direction so as to overlap the low-potential-side power supply wiring 70 is further extended in the Y direction above the low-potential-side power supply wiring 70. That portion of the branch wiring 74 which is extended in the Y direction above the low-potential-side power supply wiring 70 is referred to as a branch wiring extension portion 88.

[0167] In other words, the TFT array substrate 20 according to the present embodiment is configured such that the area in which the low-potential-side power supply wiring 70 (outer wiring) is provided includes multi metal wiring layers by laminating the first metal material, the second metal material, and the third metal material therein.

[0168] By providing the branch wiring extension portion 88 as described above, it becomes possible that the number of the contact holes 100 is less than the number of the driver circuits 60. In other words, the number of the contact holes provided for the low-potential-side power supply wiring 70 (outer wiring) can be less than the number of the wirings (branch wiring such as the branch wirings 74) branched out of the low-potential-side power supply wiring 70.

[0169] That is, without the branch wiring extension portion 88, it is necessary that each driver circuit 60 (such as first-stage driver circuit 601, second-stage driver circuit 602, third-stage driver circuit 603, fourth-stage driver circuit 604) be provided with a contact hole 100 so as to allow a branch wiring 74 and the low-potential-side power supply wiring 70 to be connected with each other.

[0170] On the other hand, with the branch wiring extension portion 88, the branch wirings 74 respectively corresponding to the driver circuits 60 are electrically connected with the low-potential-side power supply wiring 70 via the branch wiring extension portion 88 provided on the low-potential-side power supply wiring 70. With this configuration, by connecting with the low-potential-side power supply wiring 70 one branch wiring 74 corresponding to any one of the driver circuits 60 via the contact hole 100, the branch wiring(s) 74 corresponding to the other one(s) of the driver circuits 60 is connected with the low-potential-side power supply wiring 70. By this, the number of the contact holes 100 can be reduced.

[0171] In the example illustrated in Fig. 11, the branch wiring 74 corresponding to the second-stage driver circuit 602 and the branch wiring 74 corresponding to the fourth-stage driver circuit 604 are electrically connected with the low-potential-side power supply wiring 70 via the contact holes 100, respectively. Meanwhile, the branch wiring 74 corresponding to the first-stage driver circuit 601 and the branch wiring 74 corresponding to the third-stage driver circuit 603 are connected with the branch wiring extension portion 88, thereby being connected with the low-potential-side power supply wiring 70 but not being connected therewith directly via the contact holes 100.

[0172] With this configuration, it is possible to reduce the number of the contact holes provided under the seal

90. Thereby, it becomes possible to further inhibit the display quality deterioration caused by the uneven cell thickness.

[0173] The TFT array substrate 20 according to the present embodiment may be so configured that the low-potential-side power supply wiring 70, which is an outer wiring closer to the substrate edge 26, has a ladder-like shape as illustrated in Fig. 6 or 7.

[0174] Moreover, in addition to the aforementioned configuration, a connection conductor extension portion of the connection conductor 102 may be provided on and along the low-potential-side power supply wiring 70 (serving as a main wiring), i.e., in an upper layer on the low-potential-side power supply wiring 70, like the branch wiring extension portion 88.

[0175] In this configuration, the branch wirings 74 may be formed from a material identical with that of the main wiring such as the low-potential-side power supply wiring 70, thereby making it possible to electrically connect the branch wirings 74 with the main wiring without the need of the contact holes 100.

[0176] The invention being thus described, it will be obvious that the same way may be varied in many ways. Such variations are not to be regarded as a departure from the spirit and scope of the invention, and all such modifications as would be obvious to one skilled in the art are intended to be included within the scope of the following claims.

[0177] A similar configuration may be adopted in a periphery area in which the signal wiring for a signal (source) driver circuit is provided, even though the above explanation discusses an example in which the configuration is applied to the periphery area in which the scanning wiring for a signal (gate) driver circuit is provided.

[0178] Furthermore, the above explanation discusses an exemplary configuration in which the void parts 76 are provided to the low-potential-side power supply wiring 70. Where to provide the void parts 76 is not limited to the low-potential-side power supply wiring 70, and the clock wiring 72 may have void parts 76, for example. Moreover, apart from the wirings extended in the Y direction, a wiring extended in the X direction, such as the branch wiring 74, may have such void parts 76.

[0179] While the above explanation discusses an exemplary configuration in which the clock wiring 72 has the narrowed parts 84. Where to provide the narrowed portion 84 is not limited to the clock wiring 72. Apart from the wirings extended in the Y direction, a wiring extended in the X direction, such as the branch wiring 74, may have such narrowed parts 84.

[0180] Moreover, the above explanation discusses an exemplary configuration in which the main wirings are formed from the first metal material M1 from which the gate bus lines 42 are formed, and the branch wirings are formed from the second metal material M2 from which the source bus lines 44 are formed. The present invention is not limited to this combination of the wirings and the metal materials, and may be such that the first metal material M1 and the second metal material M2 are exchanged to form these wirings, for example.

[0181] Moreover, in the above explanation, the driver circuits are exemplified as the circuits that, in the periphery area of the insulating substrate, are connected with the main wirings via the branch wirings. The present invention is not limited to the driver circuits in terms of the circuits or element to be connected with the main wirings via the branch wirings, and may be so configured, for example, that the circuits or element to be connected with the main wirings via the branch wirings are peripheral TFT elements provided in the periphery area in order to drive the TFT elements provided in the display area.

[0182] Moreover, a TFT array substrate according to the present invention may be so configured that the main wiring is formed from the first metal material; the branch wirings is formed from the second metal material; and at least one of the connection parts is such that a whole of the branch-wiring via hole overlaps with the main wiring in a plane view.

[0183] Moreover, a TFT array substrate according to the present invention may be so configured that the periphery area is provided with a plurality of the main wirings; and the main wirings except one closest to a substrate edge of the insulating substrate are identical in wiring width.

[0184] Moreover, a TFT array substrate according to the present invention may be so configured that the periphery area is provided with a plurality of the main wirings; and the plurality of the main wirings are identical in wiring width.

[0185] In there configurations, and the main wirings except one closest to a substrate edge of the insulating substrate or all of the main wirings are identical in wiring width.

[0186] This makes it easier to attain uniform wiring density in the peripheral area. Therefore, it is easier to prevent the uneven cell thickness, for example, in the case where the seal is provided in the periphery area. Therefore, it is easy to prevent the display quality deterioration in the TFT array substrate with any of there configurations.

[0187] Moreover, a TFT array substrate according to the present invention may be so configured that the main wiring closest to the substrate edge of the insulating substrate is greater in wiring width than the main wirings except the one closest to the substrate edge of the insulating substrate.

[0188] Moreover, a TFT array substrate according to the present invention may be so configured that the main wiring closest to the substrate edge of the insulating substrate is a low-potential-side power supply wiring.

[0189] Moreover, a TFT array substrate according to the present invention may be so configured that the main wiring closest to the substrate edge of the insulating substrate has void parts.

[0190] Moreover, a TFT array substrate according to the present invention may be so configured that at the

connection parts in a plane view, the connection conductor is provided on the main wiring or main wirings without being off the main wiring or the main wirings.

[0191] With this configuration, the connection conductor is provided only on the main wiring at the connection part in a plane view. That is, there is the main wiring under the connection conductor.

[0192] Consequently, the TFT array substrate with this configuration is such that a particular metal material layer is present under the whole connection conductor. This makes it possible to prevent the uneven cell thickness more effectively.

[0193] Moreover, a TFT array substrate according to the present invention may be so configured that the connection parts each have a main-wiring via hole through which the main wiring or corresponding one of the main wirings is exposed, which is covered with the connection conductor; the branch-wiring via hole allows the corresponding one of the branch wirings to be electrically connected with the connection conductor; and the main-wiring via hole allows the main wiring or the corresponding one of the main wirings to be electrically connected with the connection conductor.

[0194] In this configuration, the connection part has two via holes thereby allowing the main wiring and the branch wiring to be connected with each other.

[0195] Therefore, it is easy to connect the main wiring with the branch wiring surely.

[0196] Moreover, a TFT array substrate according to the present invention may be so configured that in addition to the corresponding one of the branch wirings, the branch-wiring via hole also exposes the main wiring or corresponding one of the main wirings, which is covered with the connection conductor; and

at the branch-wiring via hole, the corresponding one of the branch wirings is electrically connected with the main wiring or the corresponding one of the main wirings.

[0197] In this configuration, the connection part has only one via hole. As a result, it is possible to reduce the number of the contact holes provided to the via holes.

[0198] Furthermore, it become easy to prevent the uneven cell thickness at the connection part.

[0199] Moreover, a TFT array substrate according to the present invention may be so configured that in the periphery area, at least either of the main wiring(s) or the branch wirings has/have void parts in which no metal material is present.

[0200] This configuration changes an effective wiring width, thereby easily providing the wiring with a desired resistance or the like.

[0201] Furthermore, in case where a light-curable resin or the like is provided to the periphery area, this configuration makes it easy to perform uniform irradiation of light to the resin. Accordingly, it becomes easy to cure the resin surely.

[0202] Moreover, a TFT array substrate according to the present invention may be so configured that the periphery area is provided with intersection parts at which the main wiring(s) respectively crosses the branch wirings without being electrically connected with the branch wirings; and at the intersection parts, at least either of the main wiring(s) or the branch wirings has/have a narrowed part at which a wiring width thereof is narrowed.

[0203] With this configuration, it is possible to reduce an area in which the main wiring and the branch wiring overlap with each other.

[0204] As a result, it becomes possible to reduce capacitance produced between the main wiring and branch wiring. Consequently, it becomes easy to prevent signal delay or the like in the wirings, thereby making it easier to improve circuit output characteristics.

[0205] Moreover, a TFT array substrate according to the present invention may be so configured that the periphery area is provided with the plural branch wirings; the branch wirings have and are electrically connected with a branch wiring extension part extended on and along the main wiring or corresponding one of the main wirings.

[0206] Moreover, a TFT array substrate according to the present invention may be so configured that the periphery area is provided with the plural branch wirings; the branch wirings have and are electrically connected with a branch wiring extension part extended on and along a first main wiring, the first main wiring being the main wiring or corresponding one of the main wirings, whereby a number of the connection parts provided on the first main wiring is less than a number of the branch wirings.

[0207] Moreover, a TFT array substrate according to the present invention may be so configured that the connection conductor has a connection conductor extension part on and along the first main wiring.

[0208] In these configurations, the main wirings and the plurality of the branch wirings are connected with each other via the branch wiring extension part or the connection conductor extension part, wherein the branch wiring extension part is a portion of the branch wirings which portion is extended along the main wiring, and the connection conductor extension part is a portion of the connection part which portion is extended along the main wiring.

[0209] These configurations make it possible to reduce the number of the connection parts at which the main wiring and the branch wirings are connected with each other correspondingly. Thereby, it becomes easy to prevent the uneven cell thickness in the periphery area.

[0210] Moreover, a TFT array substrate according to the present invention may be so configured that in the periphery area, at least some of the driver circuits are provided between the connection parts and a substrate edge of the insulating substrate.

[0211] Moreover, a TFT array substrate according to the present invention may be so configured that in the periphery area, at least some of the periphery TFT elements are provided between the connection parts and a substrate edge of the insulating substrate.

[0212] In these configurations, at least some of the driver circuits or the periphery TFT elements are provided between the connection parts and one substrate edge of the insulating substrate.

[0213] As a result, in case where a resin such as the seal or the like is provided in a region of a certain width from the substrate edge, it becomes easy to reduce the number of the connection parts that are covered by the resin.

[0214] Consequently, it becomes easy to prevent the uneven cell thickness in the periphery area.

[0215] Moreover, a TFT array substrate according to the present invention may be so configured that in the periphery area, at least some of the driver circuits are provided between the connection parts and a substrate edge of the insulating substrate; and between the at least some of the driver circuits and the rest of the driver circuits, a main wiring is provided and this main wiring is a clock wiring.

[0216] Moreover, a TFT array substrate according to the present invention may be so configured that in the periphery area, at least some of the periphery TFT elements are provided between the connection parts and a substrate edge of the insulating substrate; and between the at least some of the periphery TFT elements and the rest of the periphery TFT elements, a main wiring is provided and this main wiring is a clock wiring.

[0217] Moreover, a liquid crystal display panel according to the present invention is a liquid crystal display panel comprising: a TFT array substrate as mentioned above; and a counter substrate, being assembled with the TFT array substrate by a seal, the seal being provided in the periphery area.

[0218] Moreover, a liquid crystal display panel according to the present invention may be configured such that the connection parts is under the seal.

[0219] With this configuration, it becomes easy to give a uniform thickness to the seal provided in the periphery area.

[0220] This makes it possible to prevent the display quality deterioration caused by the uneven cell thickness.

[0221] Moreover, a liquid crystal display panel according to the present invention may be configured such that the connection parts is under the seal.

Industrial Applicability

[0222] The present invention makes it possible to prevent display quality deterioration, an is suitable applicable to liquid crystal display apparatuses etc., in which high quality display is required.

Reference Signs List

[0223]

10: Liquid Crystal Display Panel
16: Insulating Substrate
20: TFT Array Substrate
22: Display Area
24: Periphery Area
26: Substrate Edges
42: Gate Bus Lines
44: Source Bus Lines
48: Pixel Electrodes
60: Driver Circuits
70: Low-Potential-Side Power Supply Wiring (Main Wiring)
72: Clock Wirings (Main Wiring)
74: Branch Wirings (Branch Wiring)
76: Void Parts
80: Connection Parts
82: Intersection Parts
84: Narrowed Parts
88: Branch Wiring Extension Portion
90: Seal
102: Connection Conductor
110: Main-wiring via holes
112: Branch-wiring via holes
114: Single Via Holes

Claims

1. A TFT array substrate, in which TFT elements and pixel electrodes being correspondingly connected with the TFT elements are arrayed in matrix on an insulating substrate, the TFT array substrate comprising:

gate bus lines on the insulating substrate, the gate bus lines being correspondingly connected with the TFT elements and being formed from a first metal material; and
source bus lines on the insulating substrate, the source bus lines being correspondingly connected with the TFT elements and being formed from a second metal material,
the pixel electrodes being made from a third metal material,
the insulating substrate having a display area in which the pixel electrodes are arrayed in matrix, and a periphery area around the display area,
the periphery area being provided with driver circuits for driving the TFT elements corresponding thereto,
the periphery area being provided with (i) branch wirings being correspondingly connected with the driver circuits, and (ii) a main wring being connected with the branch wirings,
the branch wirings being formed from one of the first metal material and the second metal material,
the main wiring being formed from the other one of the first metal material and the second metal material,

the periphery area being provided with connection parts, at which the main wiring is connected with the respective branch wirings,
at each of the connection parts, a connection conductor electrically connecting the main wiring with corresponding one of the branch wirings,
the connection conductor being formed from the third metal material,
the connection parts each having a branch-wiring via hole through which the corresponding one of the branch wirings, which is covered with the connection conductor, is exposed,
at least one of the connection parts being such that at least part of the branch-wiring via hole overlaps with the main wiring in a plane view.

2. A TFT array substrate in which TFT elements and pixel electrodes being correspondingly connected with the TFT elements are arrayed in matrix on an insulating substrate, the TFT array substrate comprising:

gate bus lines on the insulating substrate, the gate bus lines being correspondingly connected with the TFT elements and being formed from a first metal material; and
source bus lines on the insulating substrate, the source bus lines being correspondingly connected with the TFT elements and being formed from a second metal material,
the pixel electrodes being made from a third metal material,
the insulating substrate having a display area in which the pixel electrodes are arrayed in matrix, and a periphery area around the display area,
the periphery area being provided with periphery TFT elements for driving the TFT elements corresponding thereto,
the periphery area being provided with (i) branch wirings being correspondingly connected with the periphery TFT elements, and (ii) a main wring being connected with the branch wirings, the branch wirings being formed from one of the first metal material and the second metal material,
the main wiring being formed from the other one of the first metal material and the second metal material,
the periphery area being provided with connection parts, at which the main wiring is connected with the respective branch wirings, at each of the connection parts, a connection conductor electrically connecting the main wiring with corresponding one of the branch wirings,
the connection conductor being formed from the third metal material,
the connection parts each having a branch-wiring via hole through which the corresponding one of the branch wirings is exposed, provided that the connection conductor covers this exposed portion of the corresponding one of the branch wirings,
at least one of the connection parts being such that at least part of the branch-wiring via hole overlaps with the main wiring in a plane view.

3. A TFT array substrate as set forth in claim 1 or 2, wherein:

the main wiring is formed from the first metal material;
the branch wirings is formed from the second metal material; and
at least one of the connection parts is such that a whole of the branch-wiring via hole overlaps with the main wiring in a plane view.

4. A TFT array substrate as set forth in any one of claims 1 to 3, wherein:

the periphery area is provided with a plurality of the main wirings; and
the main wirings except one closest to a substrate edge of the insulating substrate are identical in wiring width.

5. A TFT array substrate as set forth in claim 4, wherein:

the main wiring closest to the substrate edge of the insulating substrate is greater in wiring width than the main wirings except the one closest to the substrate edge of the insulating substrate.

6. A TFT array substrate as set forth in claim 4, wherein:

the main wiring closest to the substrate edge of the insulating substrate is a low-potential-side power supply wiring.

7. A TFT array substrate as set forth in claim 4, wherein:

the main wiring closest to the substrate edge of the insulating substrate has void parts.

8. A TFT array substrate as set forth in any one of claims 1 to 3, wherein:

the periphery area is provided with a plurality of the main wirings; and
the plurality of the main wirings are identical in wiring width.

9. A TFT array substrate as set forth in any one of claims 1 to 8, wherein:

at the connection parts in a plane view, the connection conductor is provided on the main wiring or main wirings without being off the main wiring or the main wirings.

10. A TFT array substrate as set forth in any one of claims 1 to 9, wherein:

the connection parts each have a main-wiring via hole through which the main wiring or corresponding one of the main wirings is exposed, which is covered with the connection conductor;
the branch-wiring via hole allows the corresponding one of the branch wirings to be electrically connected with the connection conductor; and
the main-wiring via hole allows the main wiring or the corresponding one of the main wirings to be electrically connected with the connection conductor.

11. A TFT array substrate as set forth in any one of claims 1 to 9, wherein:

in addition to the corresponding one of the branch wirings, the branch-wiring via hole also exposes the main wiring or corresponding one of the main wirings, which is covered with the connection conductor; and
at the branch-wiring via hole, the corresponding one of the branch wirings is electrically connected with the main wiring or the corresponding one of the main wirings.

12. A TFT array substrate as set forth in any one of claims 1 to 11, wherein:

in the periphery area, at least either of the main wiring(s) or the branch wirings has/have void parts in which no metal material is present.

13. A TFT array substrate as set forth in any one of claims 1 to 12, wherein:

the periphery area is provided with intersection parts at which the main wiring(s) respectively crosses the branch wirings without being electrically connected with the branch wirings; and
at the intersection parts, at least either of the main wiring(s) or the branch wirings has/have a narrowed part at which a wiring width thereof is narrowed.

14. A TFT array substrate as set forth in any one of claims 1 to 13, wherein:

the periphery area is provided with the plural branch wirings;
the branch wirings have and are electrically connected with a branch wiring extension part extended on and along the main wiring or corresponding one of the main wirings.

15. A TFT array substrate as set forth in any one of claims 1 to 13, wherein:

the periphery area is provided with the plural branch wirings;
the branch wirings have and are electrically connected with a branch wiring extension part extended on and along a first main wiring, the first main wiring being the main wiring or corresponding one of the main wirings, whereby a number of the connection parts provided on the first main wiring is less than a number of the branch wirings.

16. A TFT array substrate as set forth in claim 14 or 15, wherein the connection conductor has a connection conductor extension part on and along the first main wiring.

17. A TFT array substrate as set forth in claim 1, wherein:

in the periphery area, at least some of the driver circuits are provided between the connection parts and a substrate edge of the insulating substrate.

18. A TFT array substrate as set forth in claim 17, wherein:

in the periphery area, at least some of the driver circuits are provided between the connection parts and a substrate edge of the insulating substrate; and
between the at least some of the driver circuits and the rest of the driver circuits, a main wiring is provided and this main wiring is a clock wiring.

19. A TFT array substrate as set forth in claim 2, wherein:

in the periphery area, at least some of the periphery TFT elements are provided between the connection parts and a substrate edge of the insulating substrate.

20. A TFT array substrate as set forth in claim 19, wherein:

in the periphery area, at least some of the periphery TFT elements are provided between the connection parts and a substrate edge of the insulating substrate; and
between the at least some of the periphery TFT elements and the rest of the periphery TFT ele-

ments, a main wiring is provided and this main wiring is a clock wiring.

21. A liquid crystal display panel comprising:

a TFT array substrate as set forth in any one of the claims 1 to 20; and
a counter substrate, being assembled with the TFT array substrate by a seal,
the seal being provided in the periphery area.

22. A liquid crystal display panel as set forth in claim 21, wherein the connection parts is under the seal.

23. A liquid crystal display panel as set forth in claim 21 or 22, wherein the seal is cured by using UV light.

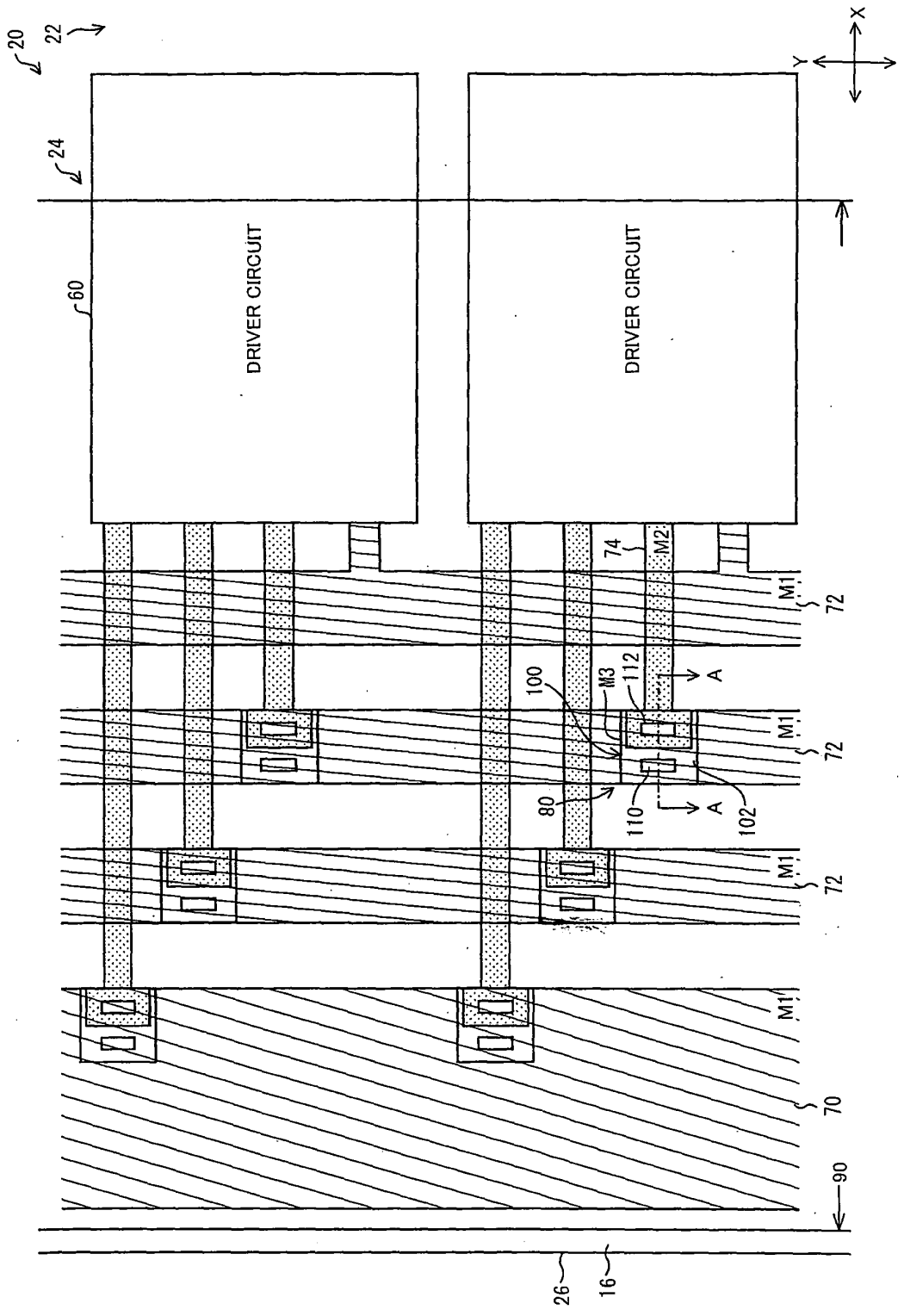

20
22
24
60
DRIVER CIRCUIT
DRIVER CIRCUIT
X
Y
74
M2
M1
72
100
M3
112
A
80
110
102
70
90
26
16

FIG. 1

FIG. 2

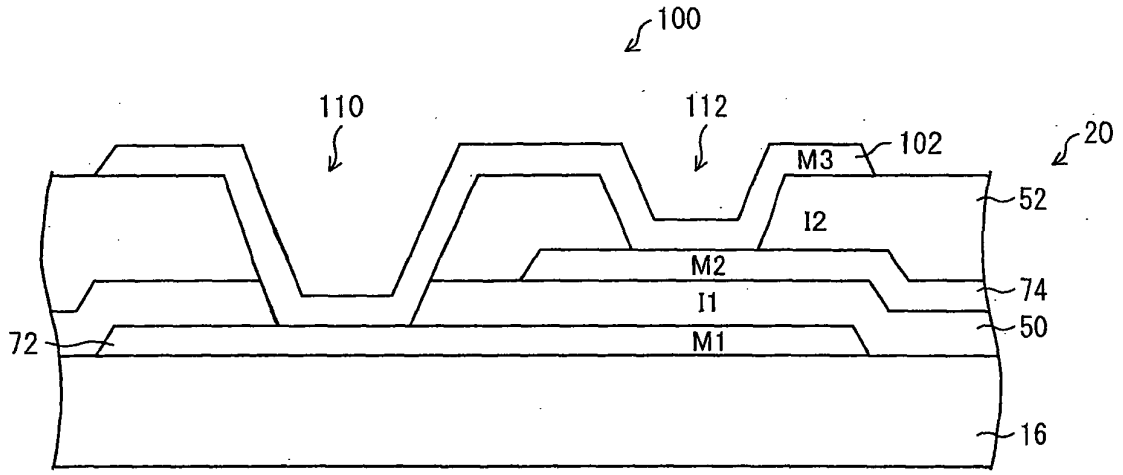


FIG. 3

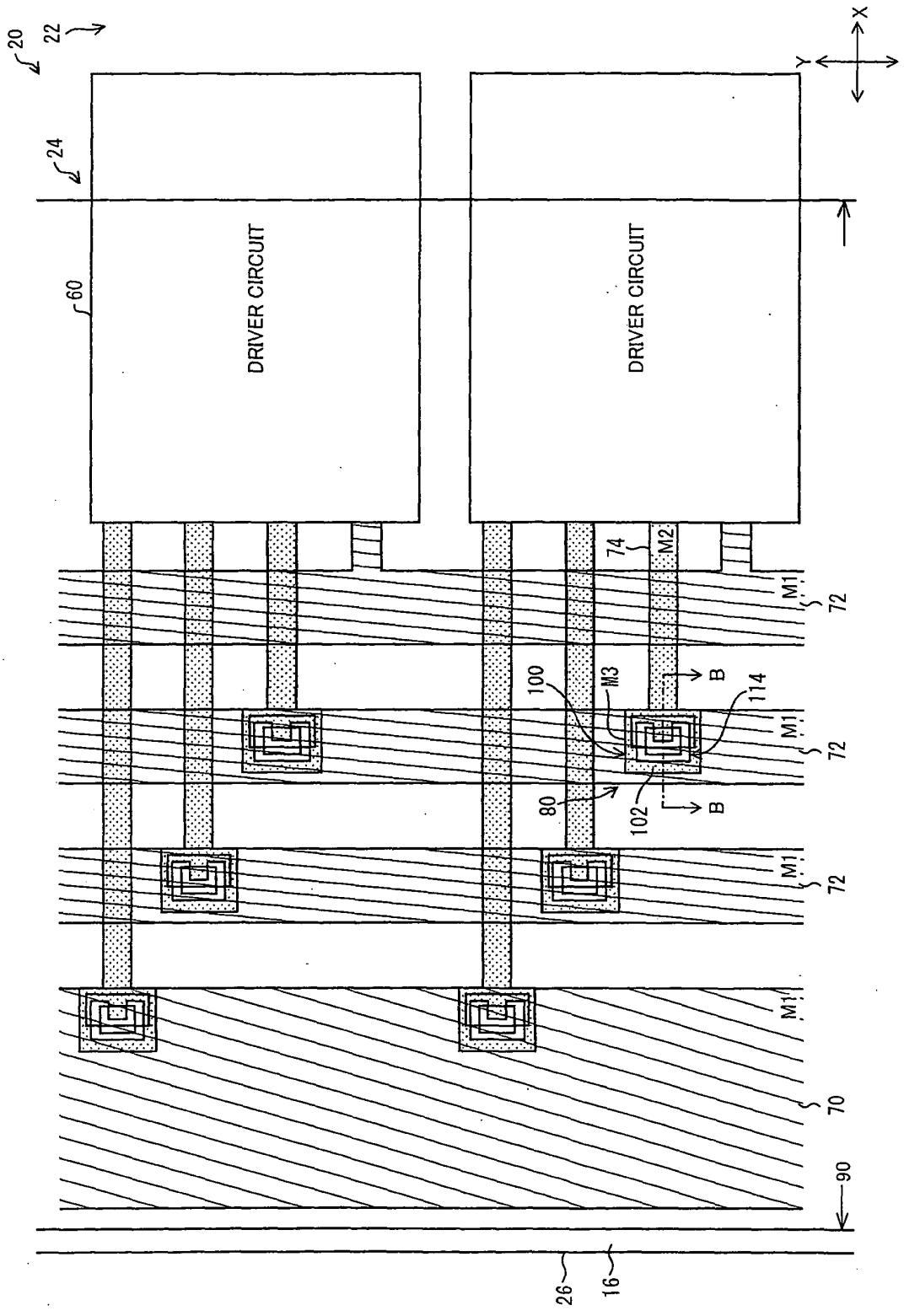

20
22
24
60
DRIVER CIRCUIT
DRIVER CIRCUIT
X
Y
74
M2
M1
72
100
M3
B
114
80
102
70
90
26
16

FIG. 4

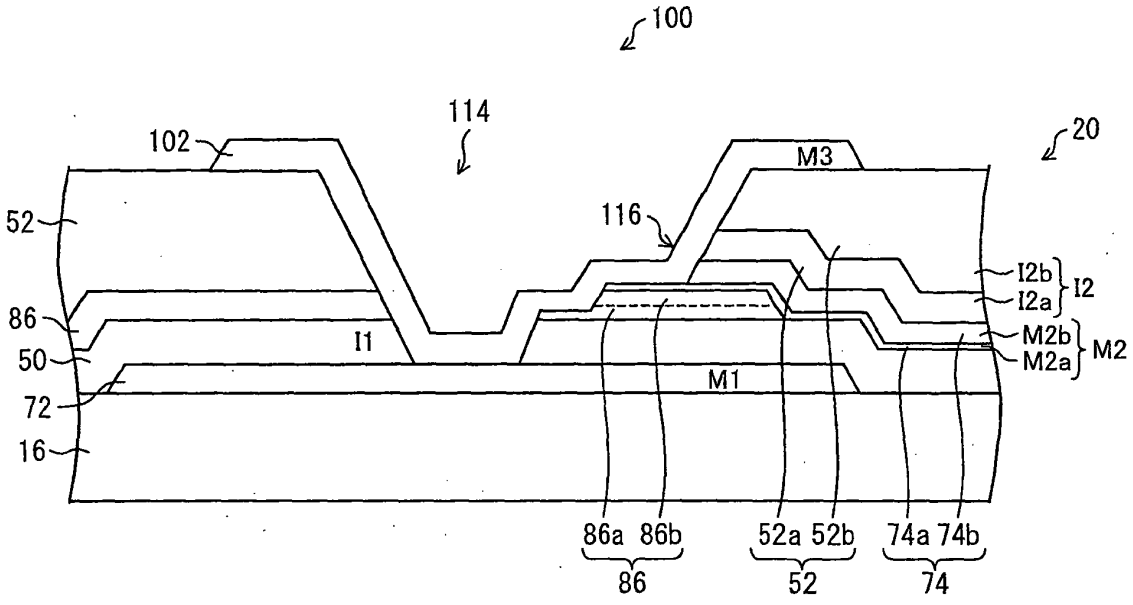

100
114
102
20
M3
52
116
I2b
I2a
I2
86
I1
M2b
M2a
M2
50
M1
72
16
86a 86b
52a 52b
74a 74b
86
52
74

FIG. 5

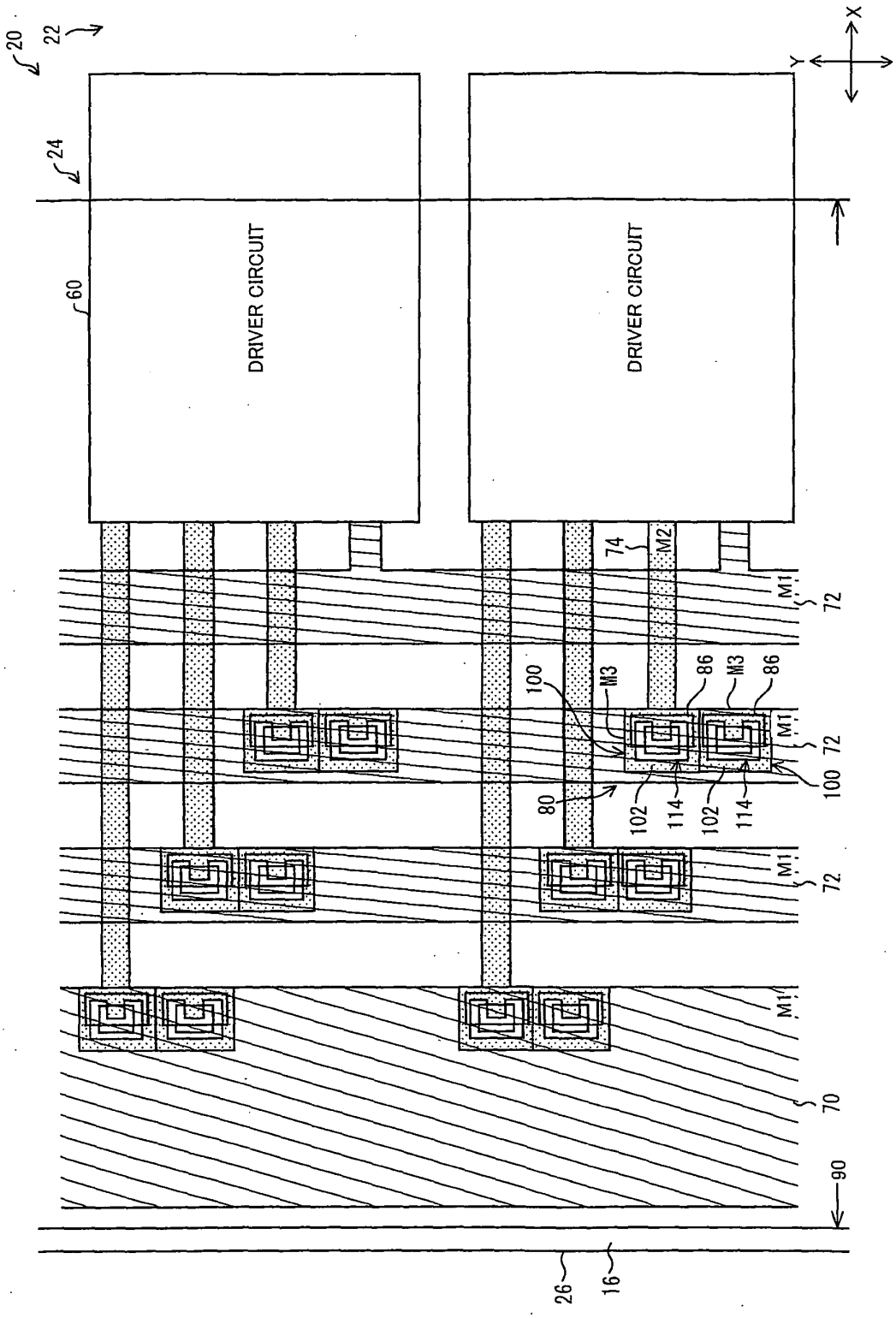

20
22
24
60
DRIVER CIRCUIT
DRIVER CIRCUIT
X
Y
74
M2
M1
72
100
M3
86
M3
86
M1
72
100
80
102
114
102
114
M1
72
M1
70
90
26
16

FIG. 6

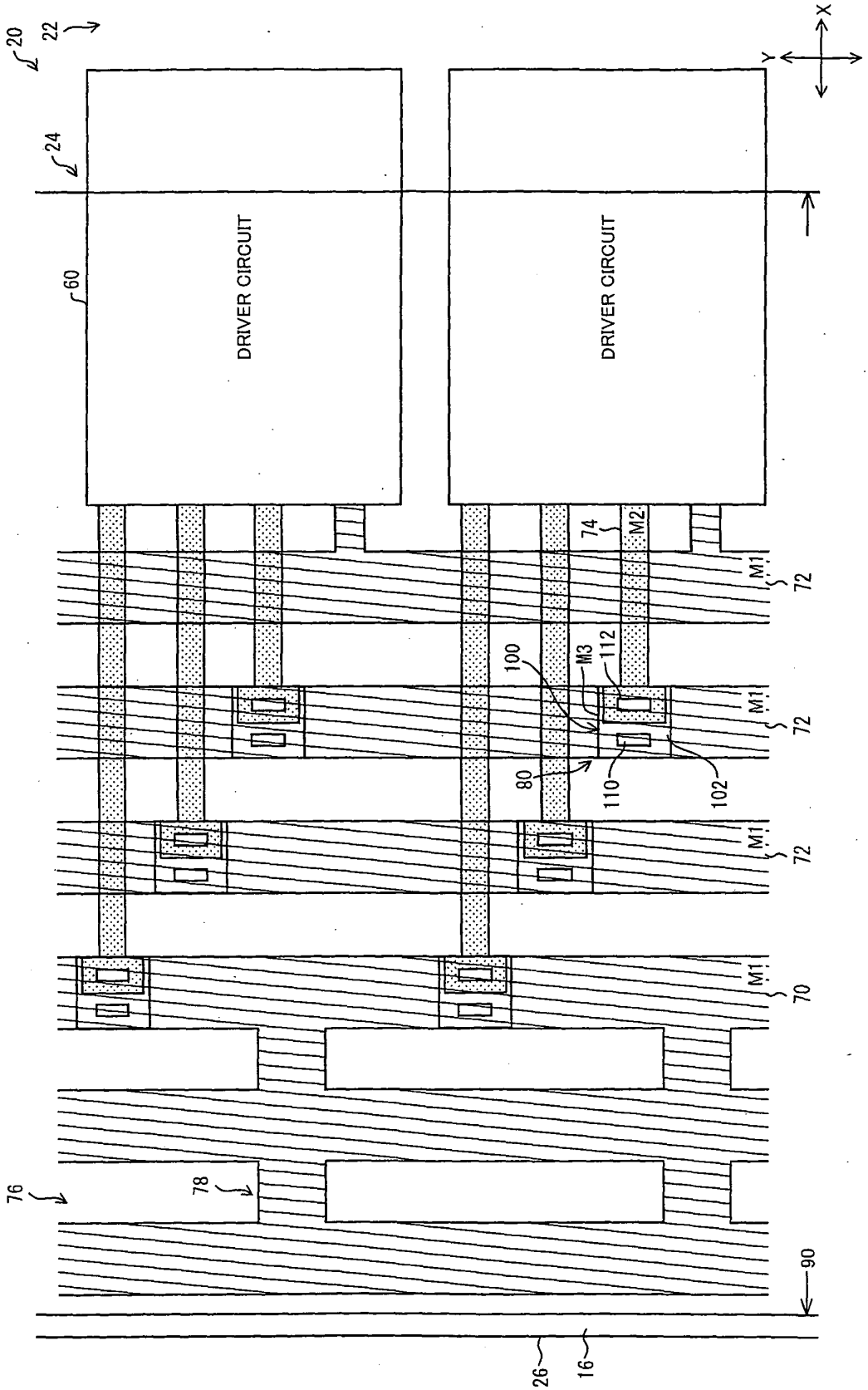
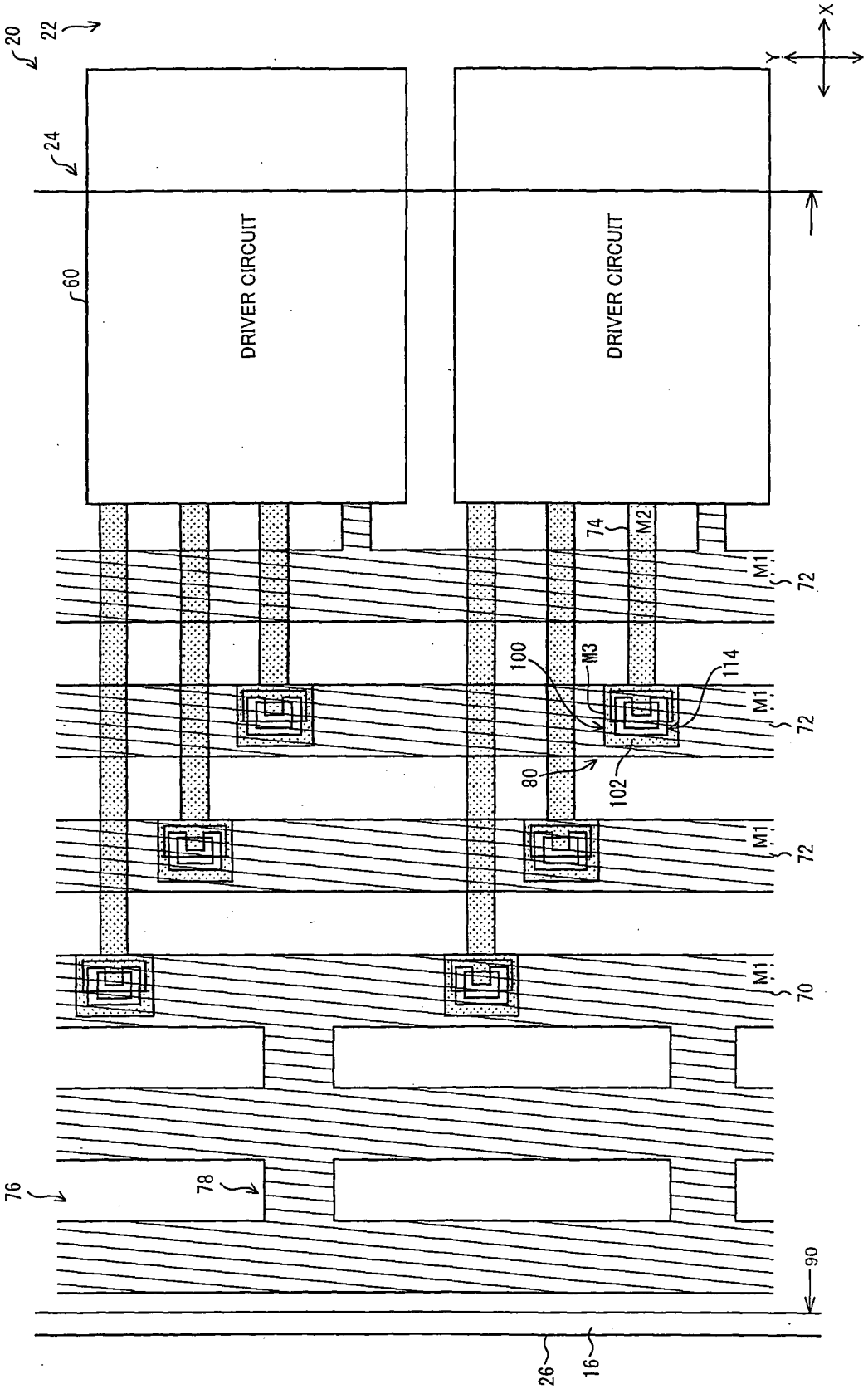

20
22
24
60
DRIVER CIRCUIT
DRIVER CIRCUIT
X
Y
74
M2
M1
72
100
M3
112
80
110
102
70
76
78
90
26
16

FIG. 7


20
22
24
60
DRIVER CIRCUIT
DRIVER CIRCUIT
X
Y
74
M2
M1
72
100
M3
114
80
102
70
76
78
90
26
16

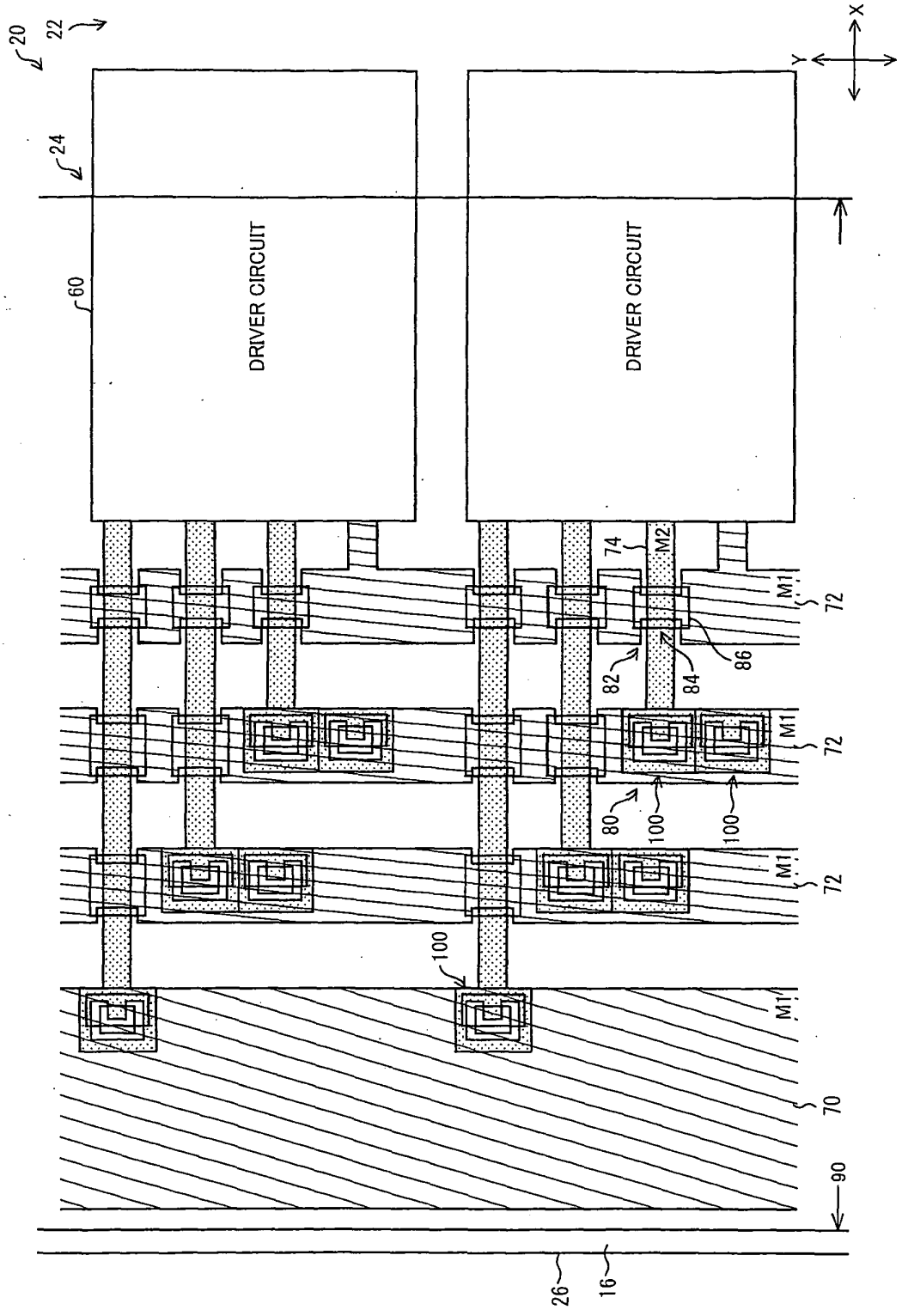

20
22
24
60
DRIVER CIRCUIT
DRIVER CIRCUIT
X
Y
74
M2
M1
72
82
84
86
80
100
100
100
M1
72
M1
72
M1
70
90
26
16

FIG. 8

FIG. 9

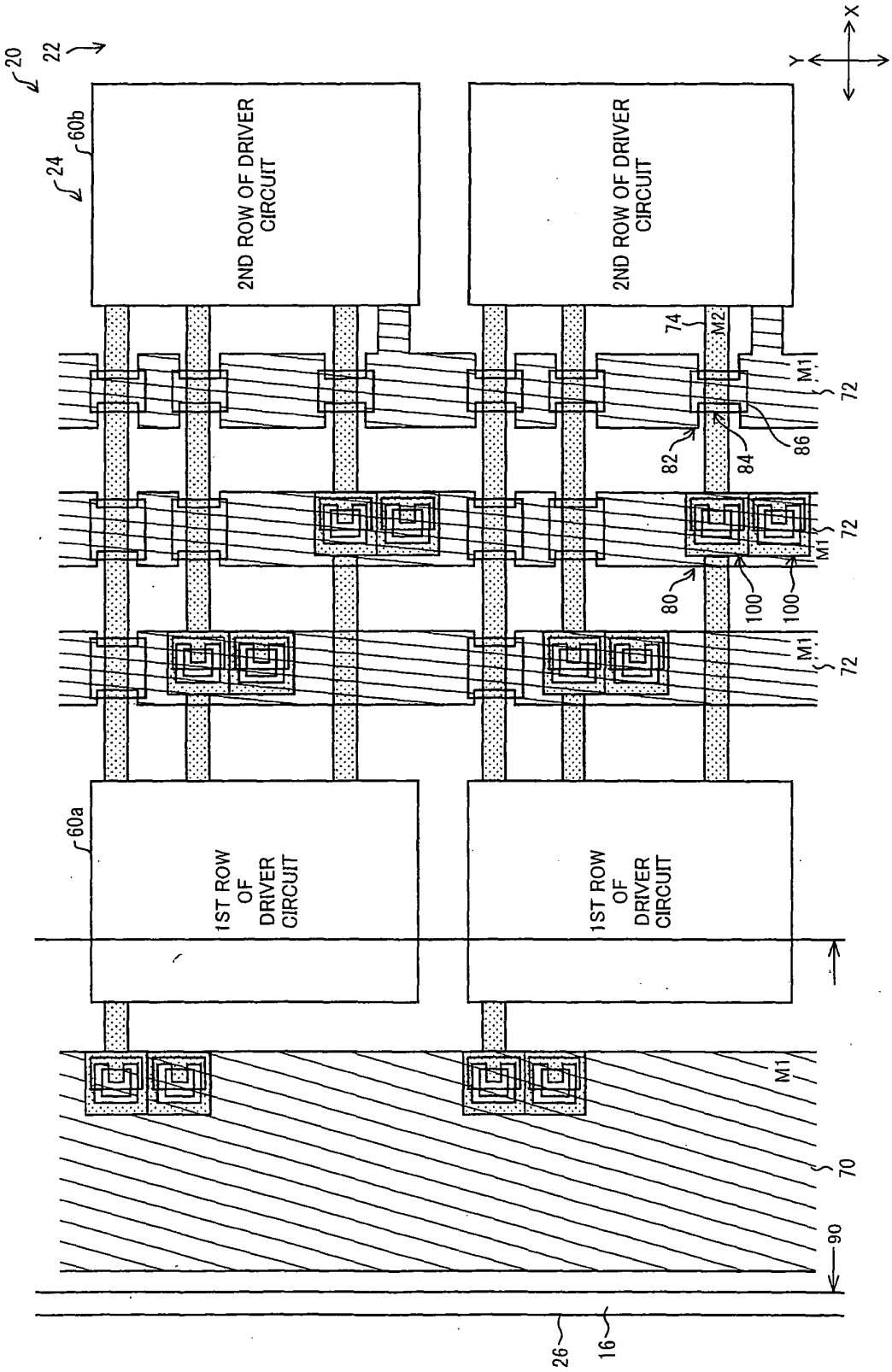

20
22
24
60b
2ND ROW OF DRIVER CIRCUIT
2ND ROW OF DRIVER CIRCUIT
74
M2
M1
72
82
84
86
80
100
100
60a
1ST ROW OF DRIVER CIRCUIT
1ST ROW OF DRIVER CIRCUIT
70
90
26
16
X
Y

FIG. 10

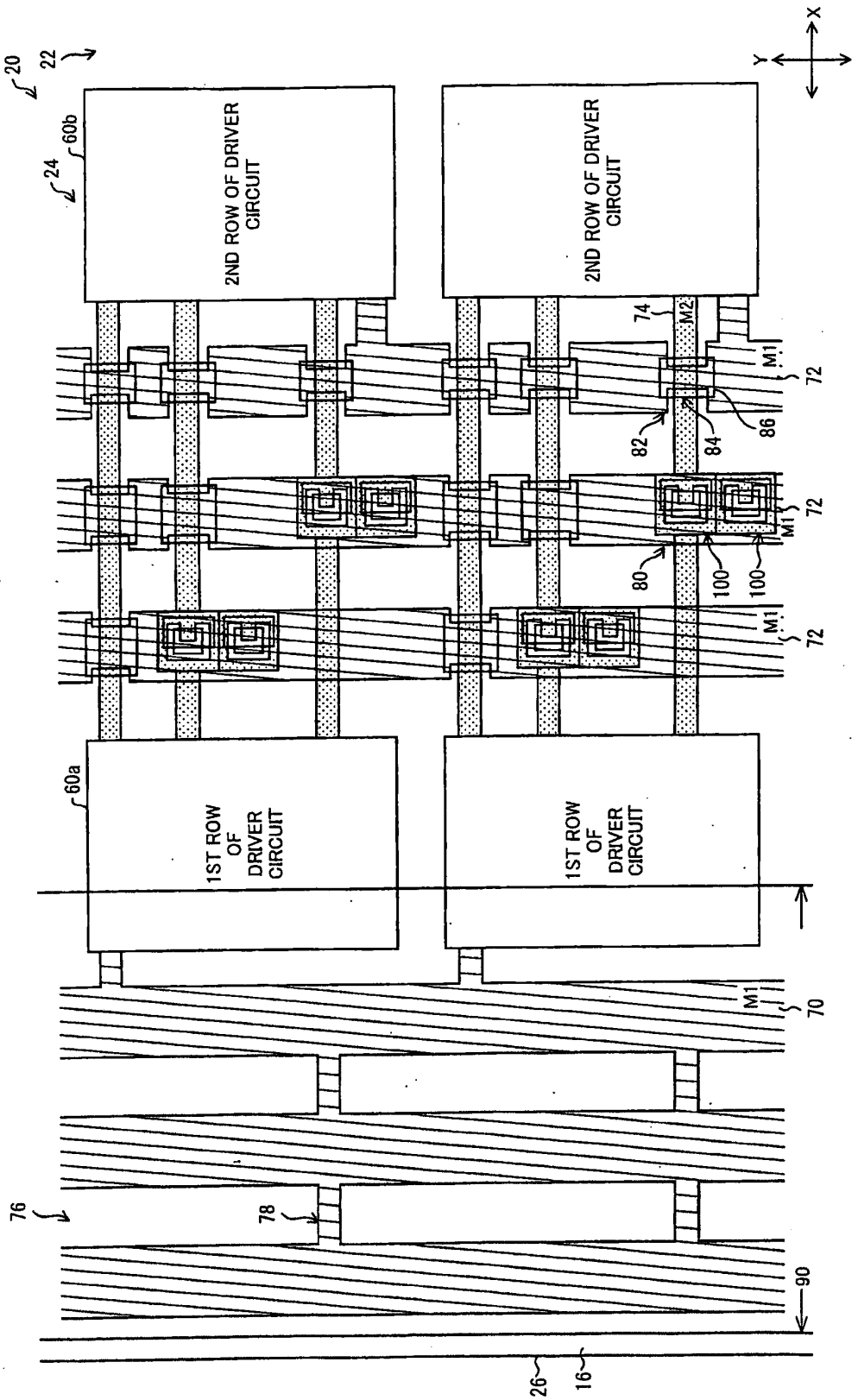

20
22
24
60b
2ND ROW OF DRIVER CIRCUIT
2ND ROW OF DRIVER CIRCUIT
60a
1ST ROW OF DRIVER CIRCUIT
1ST ROW OF DRIVER CIRCUIT
74
M2
M1
72
82
84
86
80
100
100
76
78
70
90
26
16
X
Y

FIG. 11

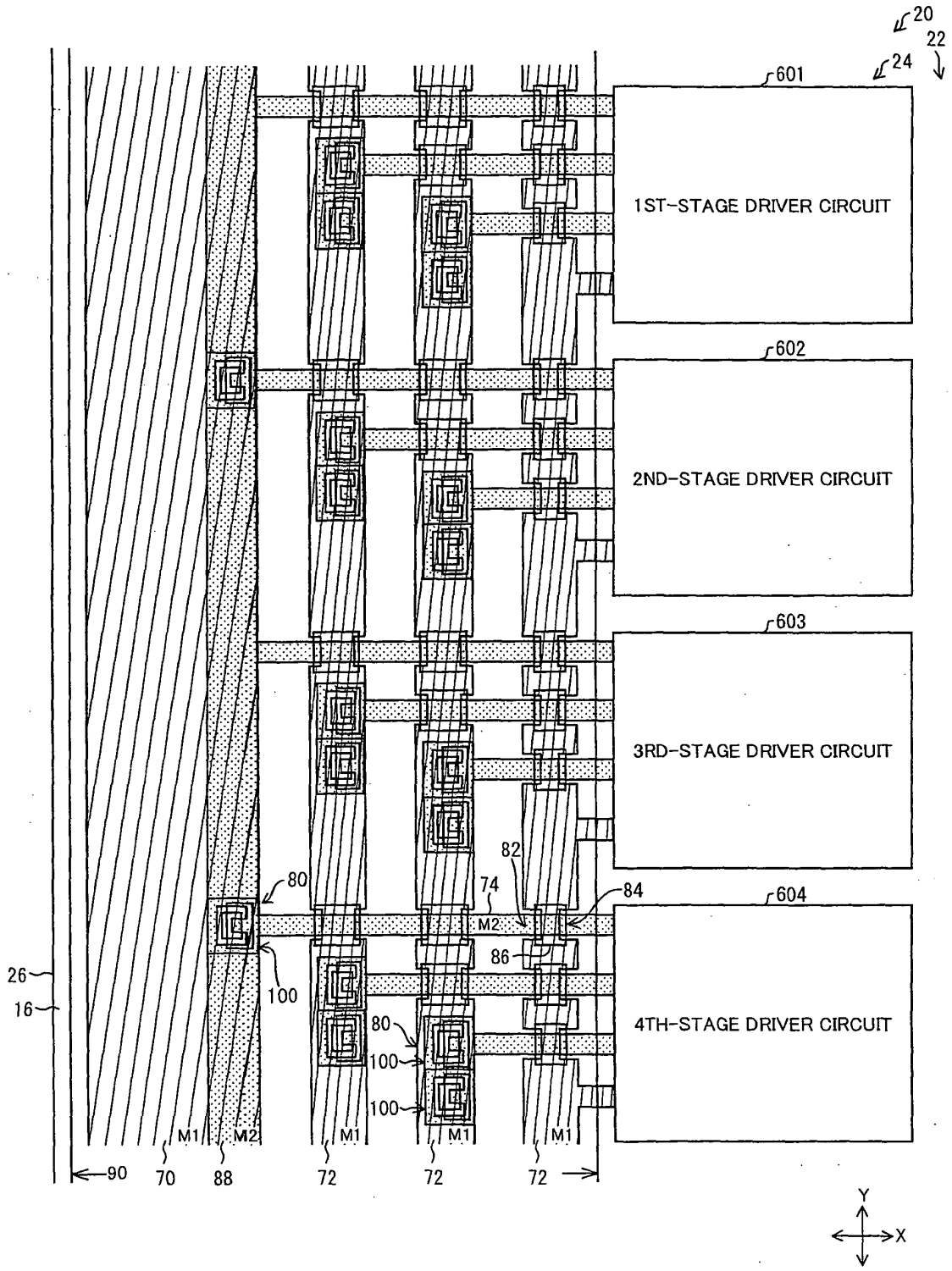

20
22
24
601
1ST-STAGE DRIVER CIRCUIT
602
2ND-STAGE DRIVER CIRCUIT
603
3RD-STAGE DRIVER CIRCUIT
604
4TH-STAGE DRIVER CIRCUIT
82
80
74
84
M2
86
26
16
100
80
100
100
M1
M2
M1
M1
M1
90
70
88
72
72
72
Y
X

FIG. 12

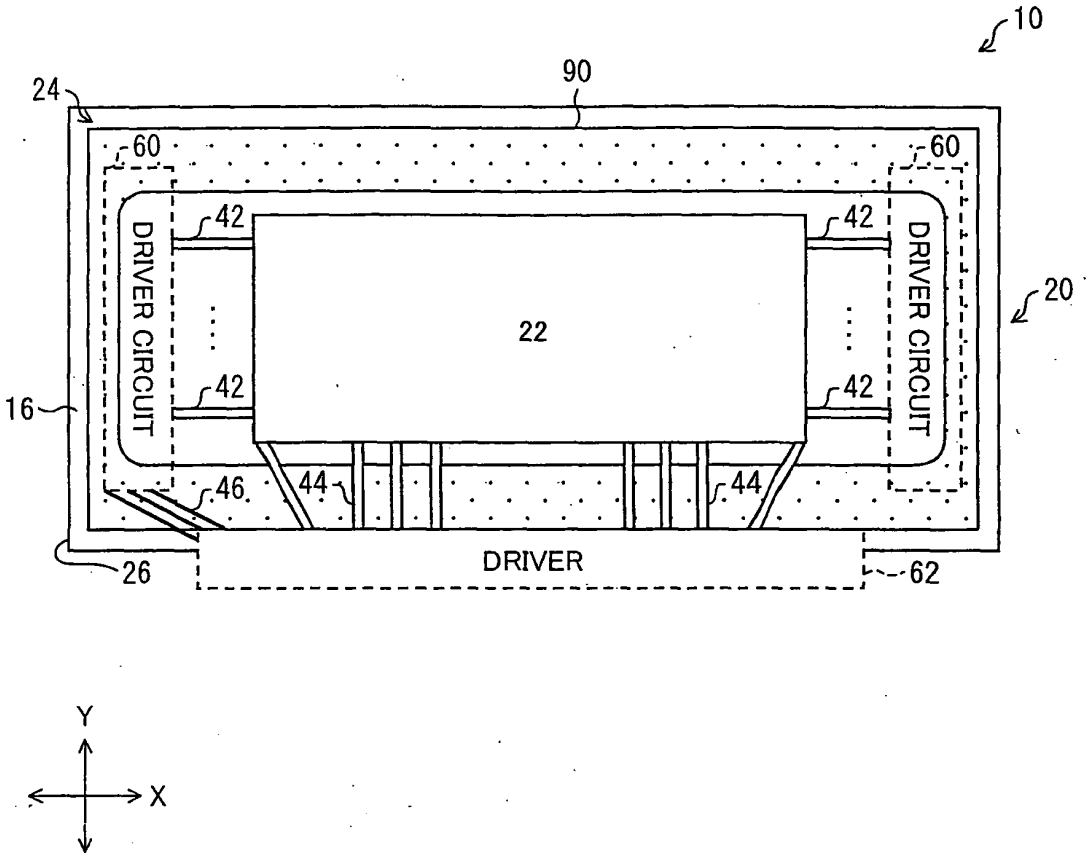

10
90
24
60
60
DRIVER CIRCUIT
42
42
22
42
42
DRIVER CIRCUIT
20
16
46
44
44
26
DRIVER
62
Y
X

FIG. 13

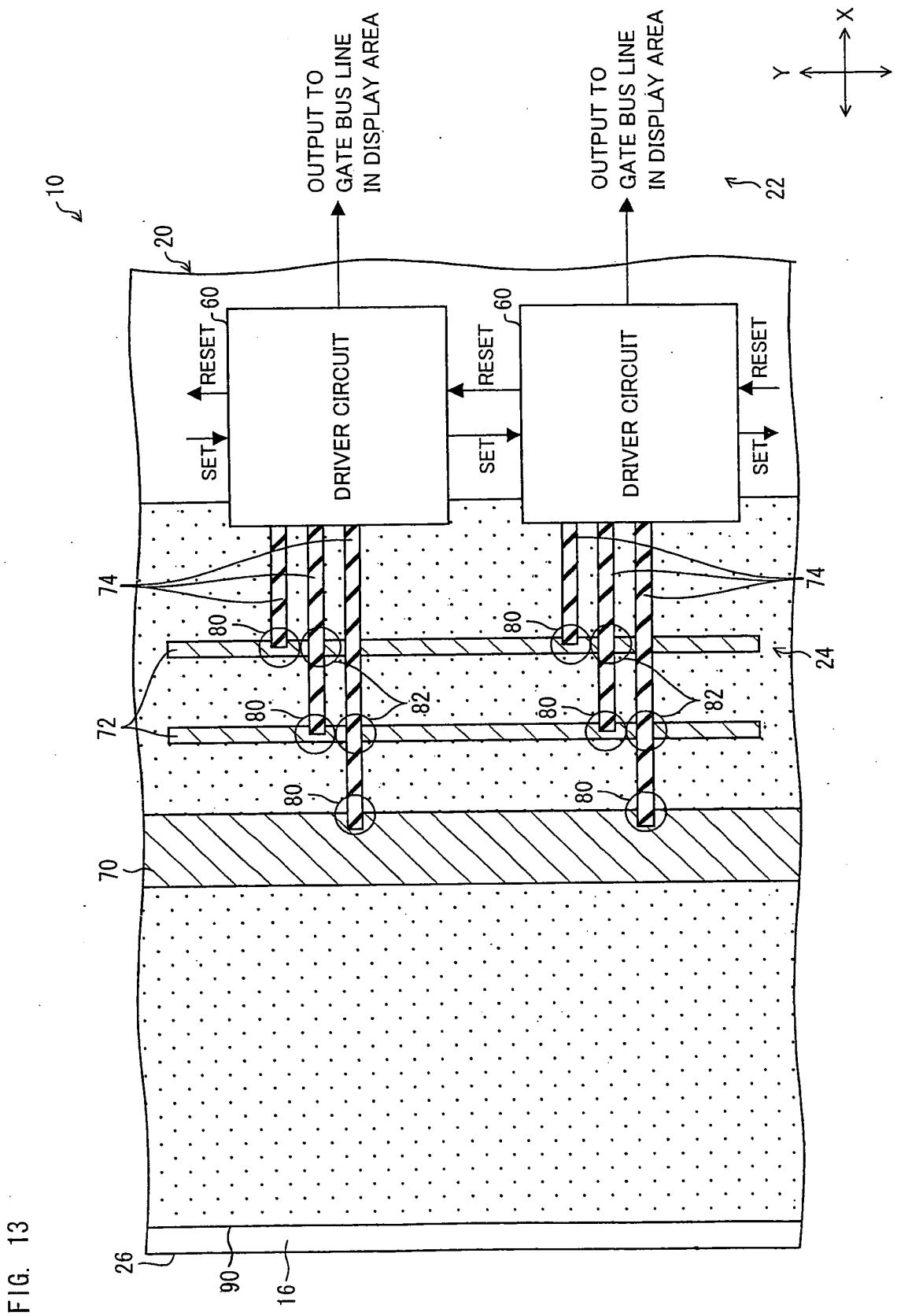
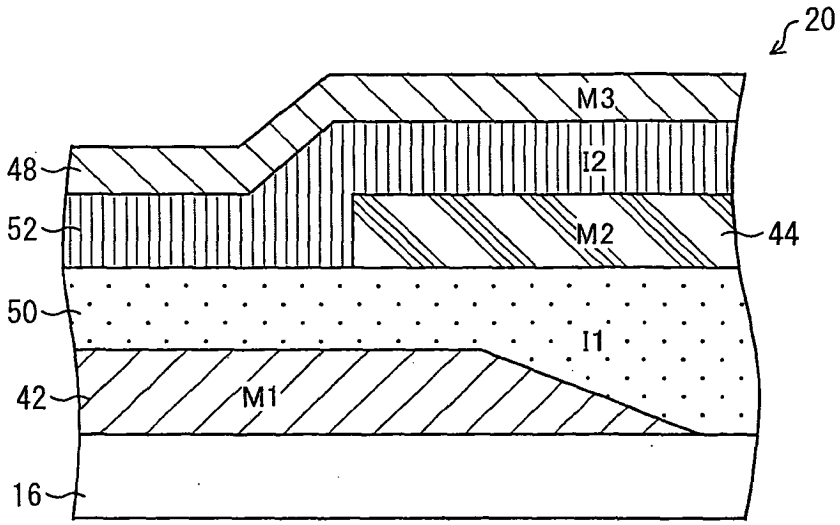

10
20
OUTPUT TO GATE BUS LINE IN DISPLAY AREA
OUTPUT TO GATE BUS LINE IN DISPLAY AREA
22
Y
X
60
RESET
SET
DRIVER CIRCUIT
60
RESET
SET
DRIVER CIRCUIT
RESET
SET
74
74
80
80
80
80
80
80
82
82
24
72
70
26
90
16

FIG. 14



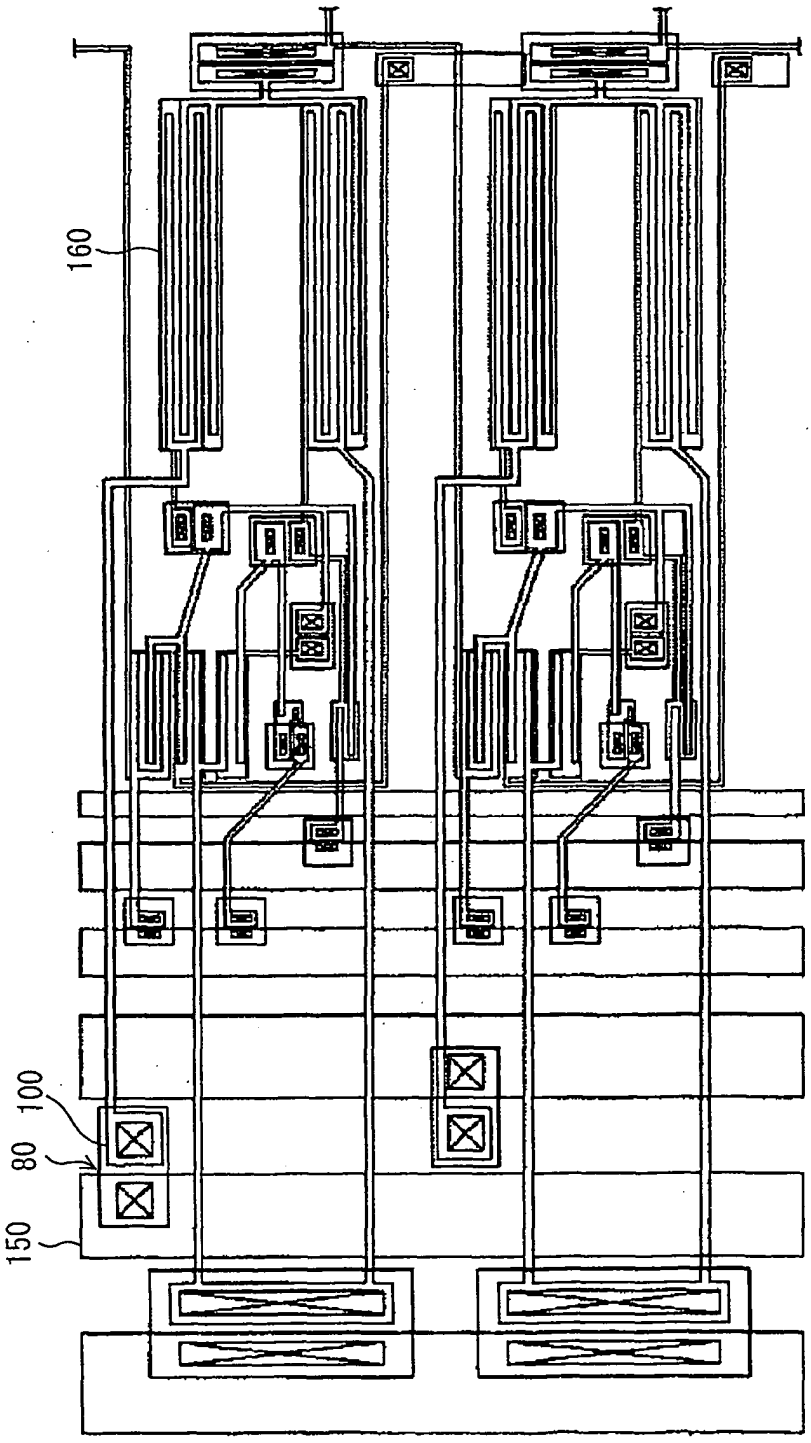


FIG. 15

FIG. 16

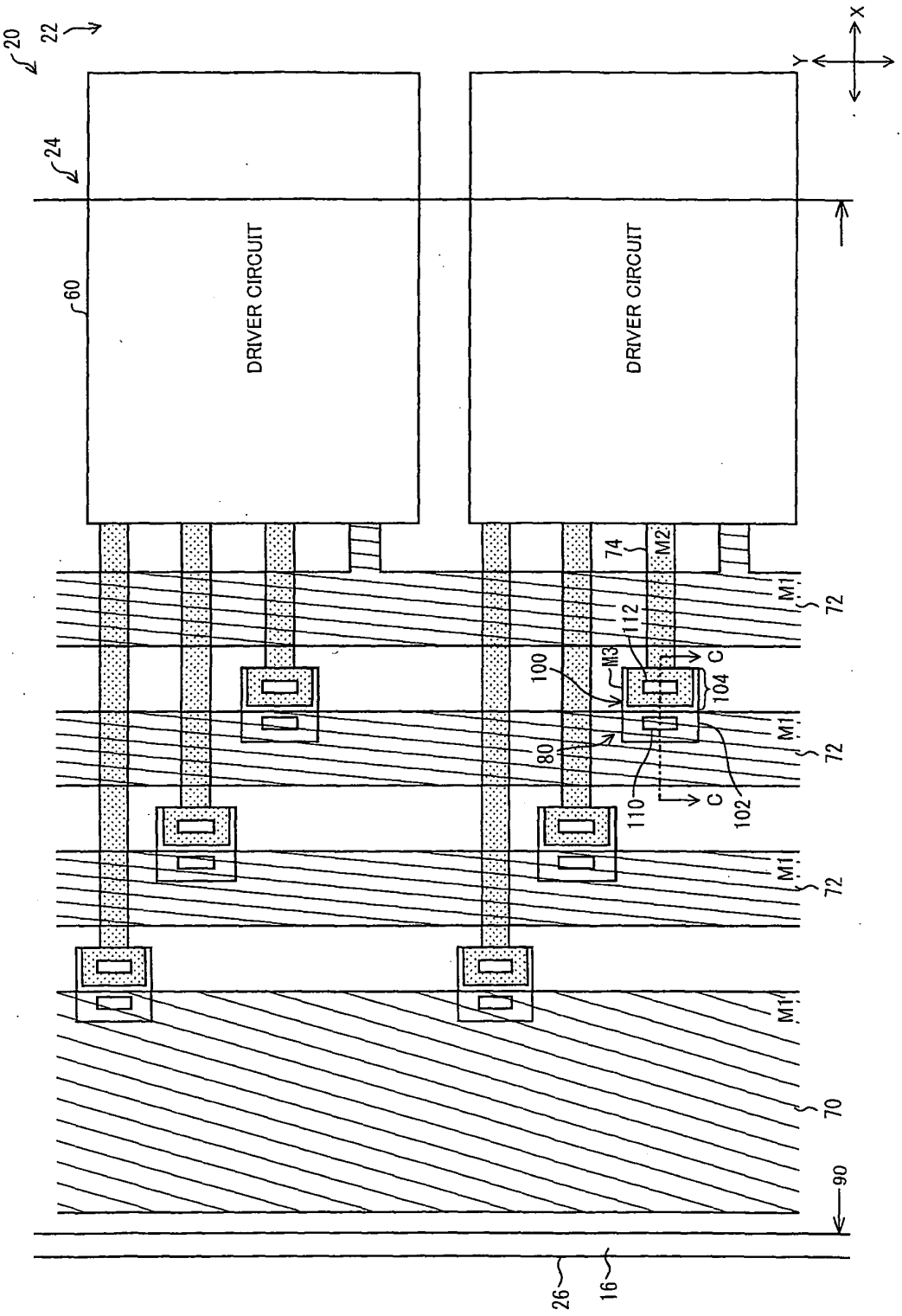
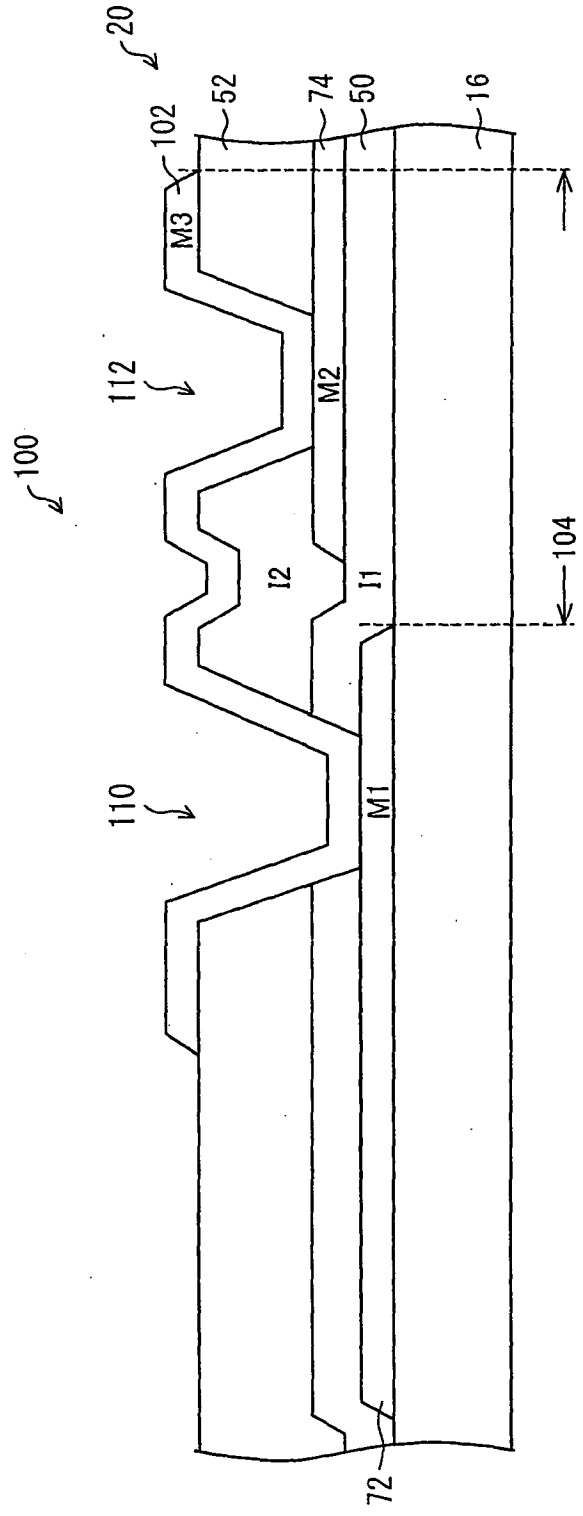

20
22
24
60
DRIVER CIRCUIT
DRIVER CIRCUIT
X
Y
74
M2
M1
72
112
M3
100
104
C
80
110
102
70
90
26
16

FIG. 17



INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2009/068905

A. CLASSIFICATION OF SUBJECT MATTER
G02F1/1368(2006.01)i, *G02F1/1345*(2006.01)i, *G09F9/30*(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G02F1/1368, G02F1/1345, G09F9/30

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1922-1996 Jitsuyo Shinan Toroku Koho 1996-2009
Kokai Jitsuyo Shinan Koho 1971-2009 Toroku Jitsuyo Shinan Koho 1994-2009

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 2009-020199 A (Mitsubishi Electric Corp.), 29 January 2009 (29.01.2009), entire text; all drawings & US 2009/0016001 A1 & CN 101344695 A	1-23
A	JP 2002-040486 A (Seiko Epson Corp.), 06 February 2002 (06.02.2002), entire text; all drawings & US 2001/0050799 A1 & TW 573149 B & KR 10-2004-0103870 A & CN 1333526 A	1-23
A	JP 2000-338521 A (Matsushita Electric Industrial Co., Ltd.), 08 December 2000 (08.12.2000), entire text; all drawings (Family: none)	1-23

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
25 December, 2009 (25.12.09)	12 January, 2010 (12.01.10)
Name and mailing address of the ISA/ Japanese Patent Office Facsimile No.	Authorized officer Telephone No.

Form PCT/ISA/210 (second sheet) (April 2007)

REFERENCES CITED IN THE DESCRIPTION

This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

Patent documents cited in the description

- JP 2005527856A PCT **[0027]**
- US 7379148 B2 **[0027]**
- JP 2006259691 A **[0027]**
- JP 9179116 A **[0027]**
- JP 2006039524 A **[0027]**

专利名称(译)	TFT阵列基板和液晶显示面板		
公开(公告)号	EP2397891A4	公开(公告)日	2012-09-12
申请号	EP2009840033	申请日	2009-11-05
[标]申请(专利权)人(译)	夏普株式会社		
申请(专利权)人(译)	夏普株式会社		
当前申请(专利权)人(译)	夏普株式会社		
[标]发明人	OGASAWARA ISAO YAMADA TAKAHARU YOSHIDA MASAHIRO HORIUCHI SATOSHI TANAKA SHINYA KIKUCHI TETSUO		
发明人	OGASAWARA, ISAO YAMADA, TAKAHARU YOSHIDA, MASAHIRO HORIUCHI, SATOSHI TANAKA, SHINYA KIKUCHI, TETSUO		
IPC分类号	G02F1/1368 G02F1/1345 G09F9/30 G02F1/1362		
CPC分类号	G02F1/136286 G02F1/133345 G02F1/1339 G02F1/134336 G02F1/1345 G02F1/13452 G02F1/13454 H01L27/1222 H01L27/124		
优先权	2009033132 2009-02-16 JP		
其他公开文献	EP2397891A1 EP2397891B1		
外部链接	Espacenet		

摘要(译)

本发明提供一种TFT阵列基板（20），其中与TFT元件对应连接的TFT元件和像素电极以矩阵形式排列在绝缘基板上，该TFT阵列基板包括：由第一金属材料制成的栅极总线（M1）;源极总线由第二金属材料（M2）制成;像素电极由第三金属材料（M3）制成;由第一金属材料（M1）制成的时钟布线（72）;分支布线（74），由第二金属材料（M2）制成;连接导体（102），其由第三金属材料（M3）制成，连接导体（102）将时钟配线（72）和分支配线（74）连接在周边区域（24）的连接部（80）上），连接部分（80）具有分支布线通孔（112），其暴露被连接导体（102）覆盖的分支布线（74），并且至少部分地与时钟布线（72）重叠。平面视图。